34 × 34, 3.2 Gbps Asynchronous Digital Crosspoint Switch

Data Sheet **AD8152**

FEATURES

- Low cost
- Low power: 2.5 V (outputs disabled)
- 34 × 34, fully differential, nonblocking array
- 3.2 Gbps per port NRZ data rate
- Wide power supply range: 2.5 V to 3.3 V
- LVTTL or LVCMOS level control inputs at
  - 2.5 V to 3.3 V
- Low channel jitter: 45 ps p-p
- Drives a backplane directly
- Programmable output swing
  - 100 mV to 1600 mV p-p differential
  - 50 Ω on-chip input/output termination
  - User controlled voltage at the load
    - Minimizes power dissipation
- Dual rank latches
- Available in 256-ball BGA_ED package

APPLICATIONS

- Fiber optic network switching
- High speed serial backplane routing to OC-48 with FEC
- Gigabit ethernet
- Digital video (HDTV)
- Data storage networks

FUNCTIONAL BLOCK DIAGRAM

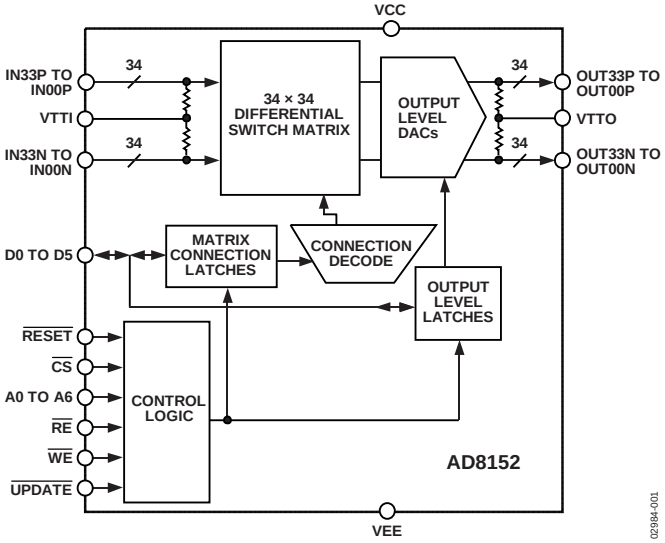

Figure 1.

GENERAL DESCRIPTION

The AD8152 is a breakthrough cross point switch offering a large switch array (34 × 34) on very little power, typically 2.0 W. Additionally, the device operates at data rates up to 3.2 Gbps per port, making it suitable for Sonet/SDH OC-48 with forward error correction (FEC).

The useful supply voltage range of the AD8152 allows the user to operate at LVPECL/CML data levels down to 2.5 V. The control interface is low voltage transistor transistor logic (LVTTL) or low voltage complementary metal-oxide (LVCMOS) compatible on 2.5 V to 3.3 V.

The fully differential signal path of the AD8152 reduces jitter and crosstalk and allows the use of smaller single-ended voltage swings. The device is offered in a 256-ball BGA_ED package that operates over the industrial temperature range of 0°C to 85°C.

Rev. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

9/2019—Rev. A to Rev. B

Updated Format ... Universal
Removed Xstream ... Throughout
Deleted Figure 2; Renumbered Sequentially ... 1
Changes to Features Section, General Description, and Figure 1 ... 1
Deleted Thermal Characteristics Parameters, Table 1 ... 2
Changed Electrical Characteristics Section to Specifications Section ... 3
Added Timing Specifications Section, Table 3; Renumbered Sequentially, and Endnote 1, Table 4 ... 4
Moved Table 2 and Table 4 to Table 6 ... 4
Changes to Timing Specifications Section, Table 2, Table 4, and Table 5 ... 4
Moved Table 7 to Table 11 ... 5
Added Endnote 1 to Table 10 ... 5
Changes to Endnote 1, Table 9, and Table 7 to Table 11 ... 5
Added Timing Diagrams Section ... 6
Moved Figure 2 to Figure 4 ... 6
Moved Figure 5 and Figure 6 ... 7
Added Thermal Resistance Section and Table 13 ... 8
Changes to Table 12 and Figure 7 ... 8
Changes to Figure 8 ... 9
Changes to Table 14 ... 10
Changes to Figure 16 and Figure 18 ... 15
Changes to Figure 21 Caption, Figure 22, Figure 23 Caption, Figure 25 Caption, and Figure 26 ... 16
Added Test Circuits Section ... 18
Changes to Figure 31 to Figure 33 ... 18
Changed Control Interface Section to Theory of Operation Section, A[6:0] Inputs Section to A0 to A6 Inputs Section, D[5:0] Inputs Section to D5 to D0 Inputs Section ... 19
Changes to Output Addressing Section, Connection and Output Current Programming Section, Using the Data Bus Section, and Register Control Signals Section ... 20
Deleted Evaluation Board and PCB Layout Hints Section, Figure 10, and Figure 11 ... 21
Changed Input/Output Coupling Section to Internal Input/Output Termination Section ... 21
Changes to Internal Input/Output Termination Section, Input Coupling Section, and Output Coupling Section ... 21
Deleted Figure 12 to Figure 14, Board Construction or Stack-Up Section, and Bypass Capacitor Layout Section ... 22
Changes to AD8152 Power Consumption Section ... 22
Deleted Figure 15, Figure 16, and Connections for Testing Section ... 23
Changes to Input Termination Resistors Section and Input Stage Section ... 23
Deleted Evaluation Board Control Software Section and Figure 14 ... 24
Changes to Power Saving Consideration Section ... 24
Deleted Figure 18 ... 25
Moved Ordering Guide Section ... 25
Updated Outline Dimensions ... 25
Changes to Ordering Guide ... 25
Deleted Figure 19 ... 26
Deleted Figure 20 ... 27
Deleted Figure 21 ... 28
Deleted Figure 22 ... 29
Deleted Figure 23 ... 30

1/2003—Rev. 0 to Rev. A

Edits to Specifications ... 2

9/2002—Revision 0: Initial Version

SPECIFICATIONS

At 25°C, VCC = 2.5 V to 3.3 V, VEE = 0 V, load resistor (R_L) = 50 Ω, and differential output swing = 800 mV p-p, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Maximum Data Rate/Channel Nonreturn to Zero (NRZ)		3.2			Gbps
Channel Jitter	Data rate ≤ 3.2 Gbps; PRBS $2^{23} - 1$		45		ps p-p
Root Mean Square (RMS) Channel Jitter			<10		ps
Propagation Delay	Input to output		660	800	ps
Propagation Delay Match			±50	±120	ps
Output Rise and Fall Time	20% to 80%		100		ps
INPUT CHARACTERISTICS					
Input Voltage Swing	Single-ended (see Figure 22)	50		1000	mV p-p
Input Voltage Range	Common-mode (see Figure 23)	VEE + 0.8		VCC + 0.2	V
Input Bias Current			2		mA
Input Capacitance			2		pF
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Differential (see Figure 26)	100	800	1600	mV p-p
Output Voltage Range		VCC − 1.2		VCC + 0.2	V
Output Current (I_{OUT})		2		32	mA
Output Capacitance			2		pF
TERMINATION CHARACTERISTICS					
Resistance		43	50	57	Ω
Temperature Coefficient			0.05		Ω/°C
POWER SUPPLY					
Operating Range					
VCC	VEE = 0 V	2.25		3.63	V
Quiescent Current					
VCC	All outputs disabled		32	45	mA
	All outputs enabled		190		mA
VEE	All outputs disabled		32	45	mA
	All outputs enabled		770		mA
	T_{MIN} to T_{MAX}, all outputs enabled		800		mA
LOGIC INPUT CHARACTERISTICS					
Input High (V_{IH})	VCC = 3.3 V	2			V
Input Low (V_{IL})	VCC = 3.3 V			0.8	V
Input High (V_{IH})	VCC = 2.5 V	1.7			V
Input Low (V_{IL})	VCC = 2.5 V			0.7	V
LOGIC OUTPUT CHARACTERISTICS					
Output High (V_{OH})	VCC = 3.3 V, I_{OH} = −2 mA	2.4			V
Output Low (V_{OL})	VCC = 3.3 V, I_{OL} = 2 mA			0.4	V
Output High (V_{OH})	VCC = 2.5 V, I_{OH} = −100 µA	2.1			V
Output Low (V_{OL})	VCC = 2.5 V, I_{OL} = 100 µA			0.2	V

TIMING SPECIFICATIONS

Table 2 to Table 11 list the timing specifications in detail.

Table 2. Bit Descriptions of the Register Address and Register Data Buses

A6	A5 (MSB)	A4	A3	A2	A1	A0 (LSB)	D5 (MSB)	D4	D3	D2	D1	D0 (LSB)
Connection/Current Bit	Output address pins						Data pins					

Table 3. A6 Bit Description

A6 Setting	Description
0	Connection latches
1	Output current level

Table 4. Connection Data and Address Programming Examples

	Output Address Pins						Data Pins (Used to Select Inputs)						
A6	A5 (MSB)	A4	A3	A2	A1	A0 (LSB)	D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	Comments[1]
0	0	0	0	0	0	0	0	0	0	0	0	0	Program IN00x to input OUT00x
0	0	0	0	0	0	0	1	0	0	0	0	1	Program IN33x to input OUT00x
0	1	0	0	0	0	1	0	1	1	1	1	1	Program IN31x to OUT33x
0	1	1	1	1	1	1	0	0	0	0	0	0	Broadcast IN00x to all outputs
0	0	0	0	0	0	0	1	1	1	1	1	1	Disable OUT00x
0	1	0	0	0	0	1	1	1	1	1	1	1	Disable OUT33x
0	1	1	1	1	1	1	1	1	1	1	1	1	Disable all outputs (broadcast)

[1] Where x is either P or N, the positive or negative differential signals for the input and output ports.

Table 5. Output Current Level Data and Address Programming Examples[1]

	Output Address Pins						Data Pins (Used to Select Inputs)						
A6	A5 (MSB)	A4	A3	A2	A1	A0 (LSB)	D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	Comments
1	0	0	0	0	0	0	N/A	N/A	0	0	0	0	Program OUT00x to current—Decimal Code 00 (2 mA)
1	0	0	0	0	0	0	N/A	N/A	1	1	1	1	Program OUT00x to current—Decimal Code 15 (32 mA)
1	1	0	0	0	0	1	N/A	N/A	0	1	1	1	Program OUT33x to current—Decimal Code 07 (16 mA)
1	1	1	1	1	1	1	N/A	N/A	1	0	0	0	Broadcast current—Decimal Code 08 to all outputs (18 mA)

[1] N/A means don't care.

Table 6. Basic Control Strobe Function[1]

$\overline{\text{RESET}}$	$\overline{\text{RS}}$	$\overline{\text{WE}}$	$\overline{\text{RE}}$	$\overline{\text{UPD}}$	Function
0	N/A	N/A	N/A	N/A	Global reset. Disables all outputs and resets all output current to Decimal Code 0111 (16 mA).
1	1	N/A	N/A	N/A	Disable all control signals. Signal matrix/currents remain the same. D5 to D0 are high impedance.
1	0	0	1	N/A	Write enable. Write D5 to D0 data into the first rank register addressed by A6 to A0.
1	0	N/A	0	N/A	Single-output readback. Second rank register data for output A6 to A0 appears on D5 to D0.
1	0	N/A	N/A	0	Global update. Copy all first rank data into second rank registers.
1	0	0	1	0	Transparent write and update. D5 to D0 immediately control programming. Use $\overline{\text{RE}}$ as the gating signal.

[1] N/A means don't care.

Table 7. First Rank Write Cycle

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_{CSW}	Chip select to write enable, setup time	T_A = 25°C, VCC = 3.3 V	0			ns
t_{ASW}	Address to write enable	T_A = 25°C, VCC = 3.3 V	0			ns
t_{DSW}	Data to write enable	T_A = 25°C, VCC = 3.3 V	1			ns
t_{CHW}	Chip select from write enable, hold time	T_A = 25°C, VCC = 3.3 V	0			ns
t_{AHW}	Address from write enable	T_A = 25°C, VCC = 3.3 V	0			ns
t_{DHW}	Data from write enable	T_A = 25°C, VCC = 3.3 V	0			ns
t_{WP}	Width of write enable pulse	T_A = 25°C, VCC = 3.3 V	10			ns

Table 8. Second Rank Update Cycle

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_{CSU}	Chip select to update, setup time	T_A = 25°C, VCC = 3.3 V	0			ns
t_{CHU}	Chip select from update, hold time	T_A = 25°C, VCC = 3.3 V	0			ns
t_{UOE}	Update to output enable times	T_A = 25°C, VCC = 3.3 V		25	45	ns
t_{UOT}	Update to output toggle times	T_A = 25°C, VCC = 3.3 V		25	45	ns
t_{UOD}	Update to output disable times	T_A = 25°C, VCC = 3.3 V		25	45	ns
t_{UW}	Width of update pulse	T_A = 25°C, VCC = 3.3 V	10			ns

Table 9. Transparent Update Cycle

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_{CSU}	Chip select to update, setup time	T_A = 25°C, VCC = 3.3 V	0			ns
t_{CHU}	Chip select from update, hold time	T_A = 25°C, VCC = 3.3 V	0			ns
t_{UOE}	Update to output enable times	T_A = 25°C, VCC = 3.3 V		35	50	ns
t_{WOE}[1]	Write enable to output enable	T_A = 25°C, VCC = 3.3 V		35	50	ns
t_{UOT}	Update to output toggle times	T_A = 25°C, VCC = 3.3 V		25	45	ns
t_{WOT}	Write enable to output reprogram	T_A = 25°C, VCC = 3.3 V		25	45	ns
t_{UOD}[1]	Update to output disable times	T_A = 25°C, VCC = 3.3 V		25	45	ns
t_{WOD}	Write enable to output disabled	T_A = 25°C, VCC = 3.3 V		25	45	ns
t_{WHU}	Write enable to update, setup time	T_A = 25°C, VCC = 3.3 V	0			ns
t_{UW}	Width of update pulse	T_A = 25°C, VCC = 3.3 V	10			ns

[1] Not shown in Figure 4.

Table 10. Second Rank Readback Cycle

Parameter	Description	Test Conditions/Comments[1]	Min	Typ	Max	Unit
t_{CSR}	Chip select to read enable, setup time	T_A = 25°C, VCC = 3.3 V	0			ns
t_{CHR}	Chip select from read enable, hold time	T_A = 25°C, VCC = 3.3 V	0			ns
t_{RHA}	Address from read enable	T_A = 25°C, VCC = 3.3 V	5			ns
t_{RDE}	Data from read enable, enable time	T_A = 25°C, VCC = 3.3 V		15		ns
t_{AA}	Data from address, access time	T_A = 25°C, VCC = 3.3 V		15	30	ns
t_{RDD}	Data from read enable, disable time	T_A = 25°C, VCC = 3.3 V		15		ns

[1] At 25°C, VCC = 2.5 V to 3.3 V, VEE = 0 V, R_L = 50 Ω, and differential output swing = 800 mV p-p, unless otherwise noted.

Table 11. Asynchronous Reset

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_{TOD}	Output disable from reset, disable time	T_A = 25°C, VCC = 3.3 V	10	25		ns
t_{TW}	Width of reset pulse	T_A = 25°C, VCC = 3.3 V	10			ns

Timing Diagrams

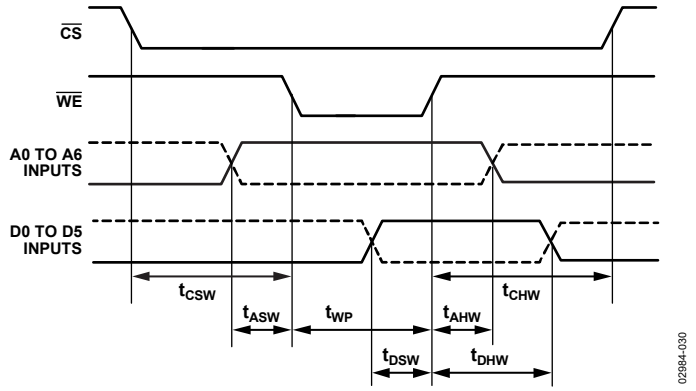

Figure 2. First Rank Write Cycle

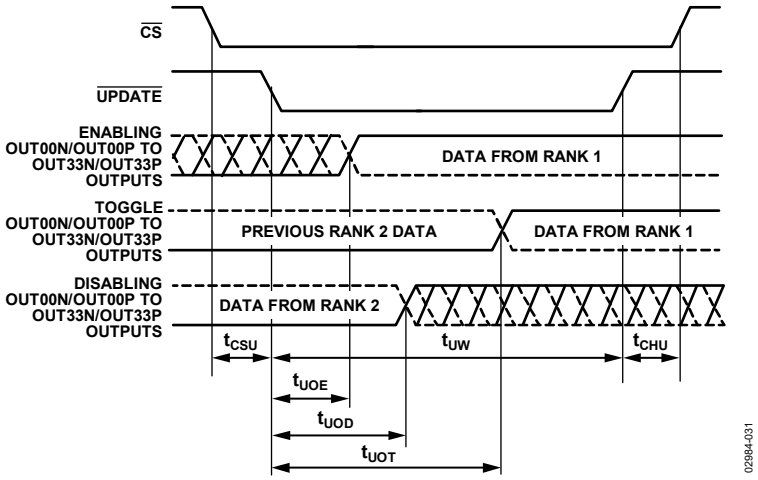

Figure 3. Second Rank Update Cycle

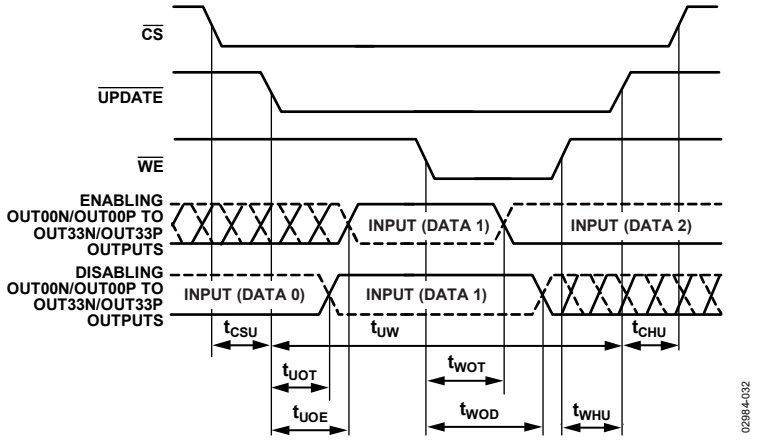

Figure 4. Transparent Write and Update Cycle

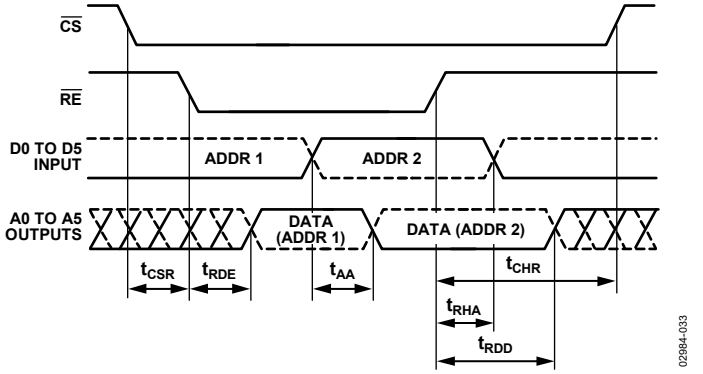

Figure 5. Second Rank Readback Cycle

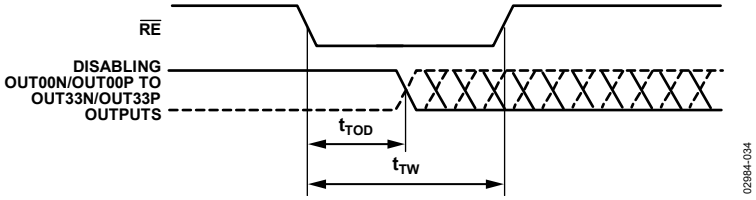

Figure 6. Asynchronous Reset

ABSOLUTE MAXIMUM RATINGS

Table 12.

Parameter	Rating
VCC to VEE	3.7 V
VTTI	VCC + 0.6 V
VTTO	VCC + 0.6 V
Internal Power Dissipation[1]	
Input Voltage	VCC + 0.6 V
Differential Input Voltage	1.7 V
Logic Input Voltage	VEE − 0.3 V < input voltage (V_{IN}) < VCC + 0.6 V
Storage Temperature Range	−65°C to +125°C
Lead Temperature	300°C
Maximum Junction Temperature	175°C

[1] Specification is for the device in free air (T_A = 25°C): θ_{JA} = 9.2°C/W at still air.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8152 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figure 7.

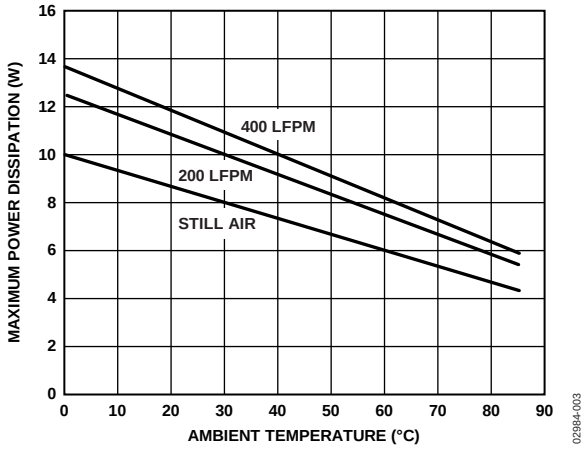

Figure 7. Maximum Power Dissipation vs. Ambient Temperature

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the thermal resistance ambient environment and θ_{JC_TOP} is the thermal resistance to the top of the package.

Thermal resistance values specified in Table 13 are simulated based on JEDEC specifications (unless specified otherwise) and must be used in compliance with JESD51-12.

Table 13. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC_TOP}[2]	Unit
BP-256-3	9.2	0.5	°C/W

[1] Using enhanced heat removal (PCB, heat sink, and airflow) technique improves thermal resistance values.
[2] For the θ_{JC_TOP} test, 100 µm thermal insulation material (TIM) is used. TIM is assumed to have 3.6 W/mK.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

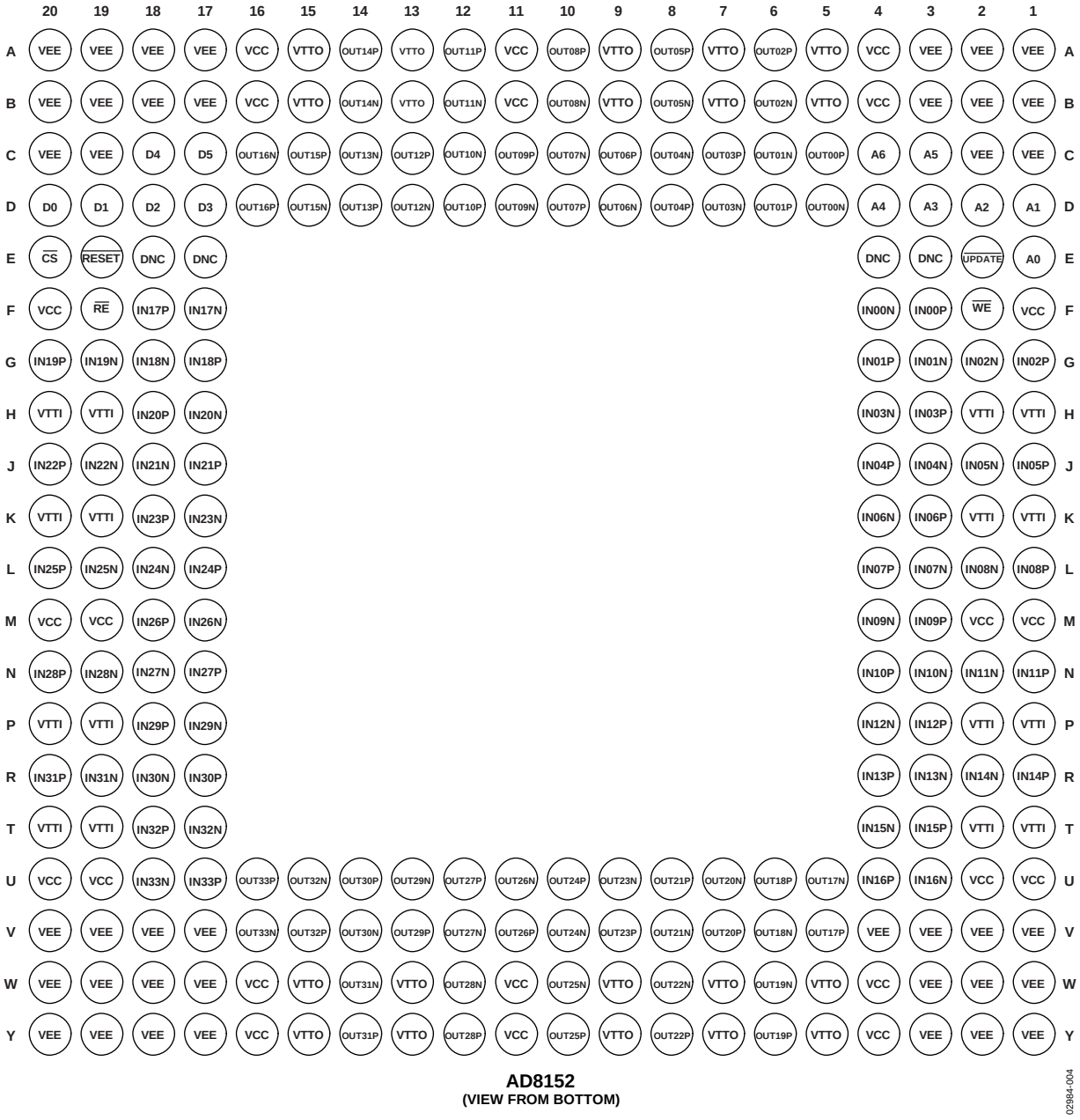

Figure 8. Pin Configuration

Table 14. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1 to A3, A17 to A20, B1 to B3, B17 to B20, C1, C2, C19, C20, V1 to V4, V17 to V20, W1 to W3, W17 to W20, Y1 to Y3, Y17 to Y20	VEE	Power	Negative Supply
A4, A11, A16, B4, B11, B16, F1, F20, M1, M2, M19, M20, U1, U2, U19, U20, W4, W11, W16, Y4, Y11, Y16	VCC	Power	Positive Supply
A5, A7, A9, A13, A15, B5, B7, B9, B13, B15, W5, W7, W9, W13, W15, Y5, Y7, Y9, Y13, Y15	VTTO	Power	Output Termination Supply
A6	OUT02P	I/O	High Speed Output
A8	OUT05P	I/O	High Speed Output
A10	OUT08P	I/O	High Speed Output
A12	OUT11P	I/O	High Speed Output
A14	OUT14P	I/O	High Speed Output
B6	OUT02N	I/O	High Speed Output Complement
B8	OUT05N	I/O	High Speed Output Complement
B10	OUT08N	I/O	High Speed Output Complement
B12	OUT11N	I/O	High Speed Output Complement
B14	OUT14N	I/O	High Speed Output Complement
C3	A5	Control	Output Address Pin (MSB)
C4	A6	Control	Output Address Pin (Connection/Current Control Pin)
C5	OUT00P	I/O	High Speed Output
C6	OUT01N	I/O	High Speed Output Complement
C7	OUT03P	I/O	High Speed Output
C8	OUT04N	I/O	High Speed Output Complement
C9	OUT06P	I/O	High Speed Output
C10	OUT07N	I/O	High Speed Output Complement
C11	OUT09P	I/O	High Speed Output
C12	OUT10N	I/O	High Speed Output Complement
C13	OUT12P	I/O	High Speed Output
C14	OUT13N	I/O	High Speed Output Complement
C15	OUT15P	I/O	High Speed Output
C16	OUT16N	I/O	High Speed Output Complement
C17	D5	Control	Input Address Pin (MSB)
C18	D4	Control	Input Address Pin
D1	A1	Control	Output Address Pin
D2	A2	Control	Output Address Pin
D3	A3	Control	Output Address Pin
D4	A4	Control	Output Address Pin
D5	OUT00N	I/O	High Speed Output Complement
D6	OUT01P	I/O	High Speed Output
D7	OUT03N	I/O	High Speed Output Complement
D8	OUT04P	I/O	High Speed Output
D9	OUT06N	I/O	High Speed Output Complement
D10	OUT07P	I/O	High Speed Output
D11	OUT09N	I/O	High Speed Output Complement
D12	OUT10P	I/O	High Speed Output
D13	OUT12N	I/O	High Speed Output Complement
D14	OUT13P	I/O	High Speed Output
D15	OUT15N	I/O	High Speed Output Complement
D16	OUT16P	I/O	High Speed Output
D17	D3	Control	Input Address Pin
D18	D2	Control	Input Address Pin
D19	D1	Control	Input Address Pin

Pin No.	Mnemonic	Type[1]	Description
D20	D0	Control	Input Address Pin (LSB)
E1	A0	Control	Output Address Pin (LSB)
E2	$\overline{\text{UPDATE}}$	Control	Second Rank Write Enable
E3, E4, E17, E18	DNC		Do Not Connect. Reserved.
E19	$\overline{\text{RESET}}$	Control	Reset/Disable Outputs
E20	$\overline{\text{CS}}$	Control	Chip Select Enable
F2	$\overline{\text{WE}}$	Control	First Rank Write Enable
F3	IN00P	I/O	High Speed Input
F4	IN00N	I/O	High Speed Input Complement
F17	IN17N	I/O	High Speed Input Complement
F18	IN17P	I/O	High Speed Input
F19	$\overline{\text{RE}}$	Control	Readback Enable
G1	IN02P	I/O	High Speed Input
G2	IN02N	I/O	High Speed Input Complement
G3	IN01N	I/O	High Speed Input Complement
G4	IN01P	I/O	High Speed Input
G17	IN18P	I/O	High Speed Input
G18	IN18N	I/O	High Speed Input Complement
G19	IN19N	I/O	High Speed Input Complement
G20	IN19P	I/O	High Speed Input
H1, H2, H19, H20, K1, K2, K19, K20, P1, P2, P19, P20, T1, T2, T19, T20	VTTI	Power	Input Termination Supply
H3	IN03P	I/O	High Speed Input
H4	IN03N	I/O	High Speed Input Complement
H17	IN20N	I/O	High Speed Input Complement
H18	IN20P	I/O	High Speed Input
J1	IN05P	I/O	High Speed Input
J2	IN05N	I/O	High Speed Input Complement
J3	IN04N	I/O	High Speed Input Complement
J4	IN04P	I/O	High Speed Input
J17	IN21P	I/O	High Speed Input
J18	IN21N	I/O	High Speed Input Complement
J19	IN22N	I/O	High Speed Input Complement
J20	IN22P	I/O	High Speed Input
K3	IN06P	I/O	High Speed Input Complement
K4	IN06N	I/O	High Speed Input
K17	IN23N	I/O	High Speed Input Complement
K18	IN23P	I/O	High Speed Input
L1	IN08P	I/O	High Speed Input
L2	IN08N	I/O	High Speed Input Complement
L3	IN07N	I/O	High Speed Input Complement
L4	IN07P	I/O	High Speed Input
L17	IN24P	I/O	High Speed Input
L18	IN24N	I/O	High Speed Input Complement
L19	IN25N	I/O	High Speed Input Complement
L20	IN25P	I/O	High Speed Input
M3	IN09P	I/O	High Speed Input
M4	IN09N	I/O	High Speed Input Complement
M17	IN26N	I/O	High Speed Input Complement
M18	IN26P	I/O	High Speed Input
N1	IN11P	I/O	High Speed Input
N2	IN11N	I/O	High Speed Input Complement
N3	IN10N	I/O	High Speed Input Complement

Pin No.	Mnemonic	Type[1]	Description
N4	IN10P	I/O	High Speed Input
N17	IN27P	I/O	High Speed Input
N18	IN27N	I/O	High Speed Input Complement
N19	IN28N	I/O	High Speed Input Complement
N20	IN28P	I/O	High Speed Input
P3	IN12P	I/O	High Speed Input
P4	IN12N	I/O	High Speed Input Complement
P17	IN29N	I/O	High Speed Input Complement
P18	IN29P	I/O	High Speed Input
R1	IN14P	I/O	High Speed Input
R2	IN14N	I/O	High Speed Input Complement
R3	IN13N	I/O	High Speed Input Complement
R4	IN13P	I/O	High Speed Input
R17	IN30P	I/O	High Speed Input
R18	IN30N	I/O	High Speed Input Complement
R19	IN31N	I/O	High Speed Input Complement
R20	IN31P	I/O	High Speed Input
T3	IN15P	I/O	High Speed Input
T4	IN15N	I/O	High Speed Input Complement
T17	IN32N	I/O	High Speed Input Complement
T18	IN32P	I/O	High Speed Input
U3	IN16N	I/O	High Speed Input Complement
U4	IN16P	I/O	High Speed Input
U5	OUT17N	I/O	High Speed Output Complement
U6	OUT18P	I/O	High Speed Output
U7	OUT20N	I/O	High Speed Output Complement
U8	OUT21P	I/O	High Speed Output
U9	OUT23N	I/O	High Speed Output Complement
U10	OUT24P	I/O	High Speed Output
U11	OUT26N	I/O	High Speed Output Complement
U12	OUT27P	I/O	High Speed Output
U13	OUT29N	I/O	High Speed Output
U14	OUT30P	I/O	High Speed Output
U15	OUT32N	I/O	High Speed Output Complement
U16	OUT33P	I/O	High Speed Output
U17	IN33P	I/O	High Speed Input
U18	IN33N	I/O	High Speed Input Complement
V5	OUT17P	I/O	High Speed Output
V6	OUT18N	I/O	High Speed Output Complement
V7	OUT20P	I/O	High Speed Output
V8	OUT21N	I/O	High Speed Output Complement
V9	OUT23P	I/O	High Speed Output
V10	OUT24N	I/O	High Speed Output Complement
V11	OUT26P	I/O	High Speed Output
V12	OUT27N	I/O	High Speed Output Complement
V13	OUT29P	I/O	High Speed Output
V14	OUT30N	I/O	High Speed Output Complement
V15	OUT32P	I/O	High Speed Output
V16	OUT33N	I/O	High Speed Output Complement
W6	OUT19N	I/O	High Speed Output Complement
W8	OUT22N	I/O	High Speed Output Complement
W10	OUT25N	I/O	High Speed Output Complement

Pin No.	Mnemonic	Type[1]	Description
W12	OUT28N	I/O	High Speed Output Complement
W14	OUT31N	I/O	High Speed Output Complement
Y6	OUT19P	I/O	High Speed Output
Y8	OUT22P	I/O	High Speed Output
Y10	OUT25P	I/O	High Speed Output
Y12	OUT28P	I/O	High Speed Output
Y14	OUT31P	I/O	High Speed Output

[1] I/O stands for input/output.

TYPICAL PERFORMANCE CHARACTERISTICS

2.5 V supply, VCC = VTTI = VTTO, data rate = 3.2 Gbps, PRBS $2^{23}-1$, differential output swing = 800 mV p-p, R_L = 50 Ω, and input amplitude = 0.4 V p-p single-ended, unless otherwise noted.

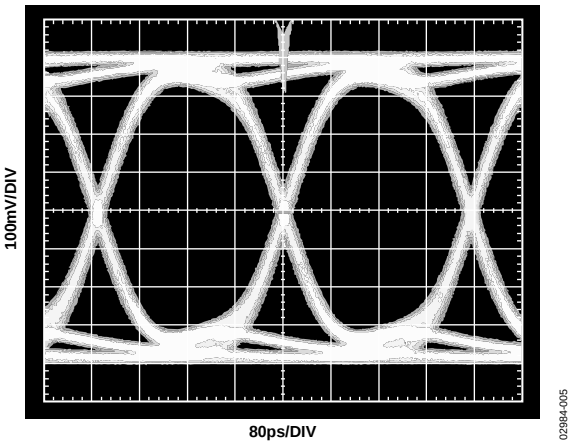

Figure 9. Eye Pattern, 3.2 Gbps

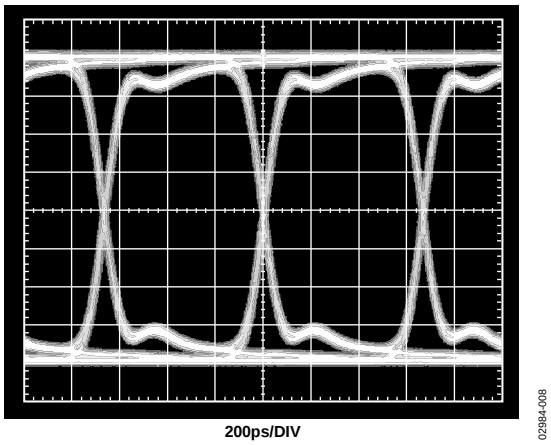

Figure 12. Eye Pattern, 1.5 Gbps

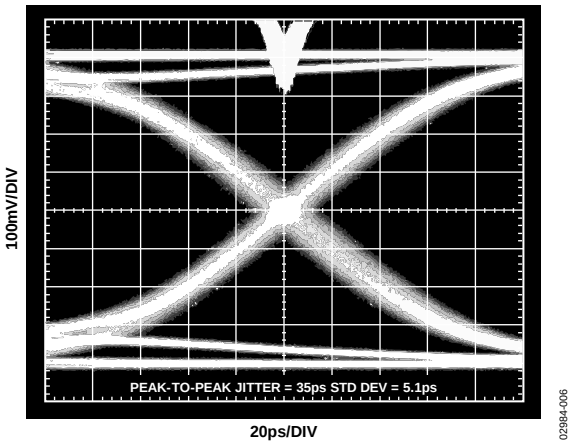

Figure 10. Jitter at 3.2 Gbps

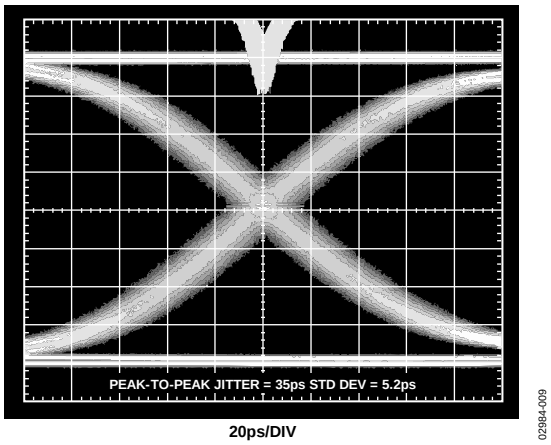

Figure 13. Jitter at 1.5 Gbps

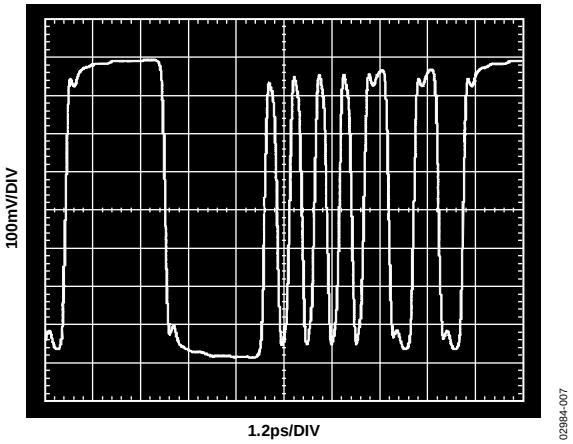

Figure 11. Response, 3.2 Gbps, 32-Bit Pattern
1111 1111 0 000 0000 1010 1010 1100 1100

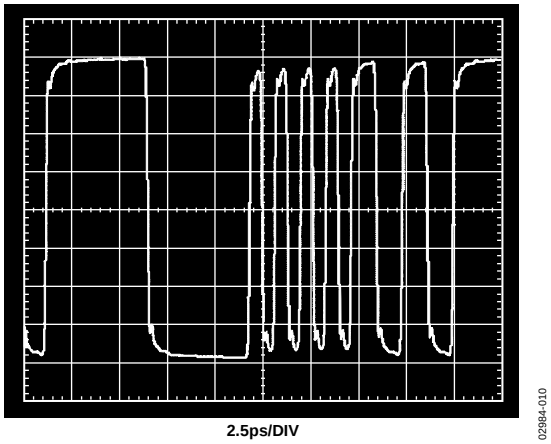

Figure 14. Response, 1.5 Gbps, 32-Bit Pattern
1111 1111 0000 0000 1010 1010 1100 1100

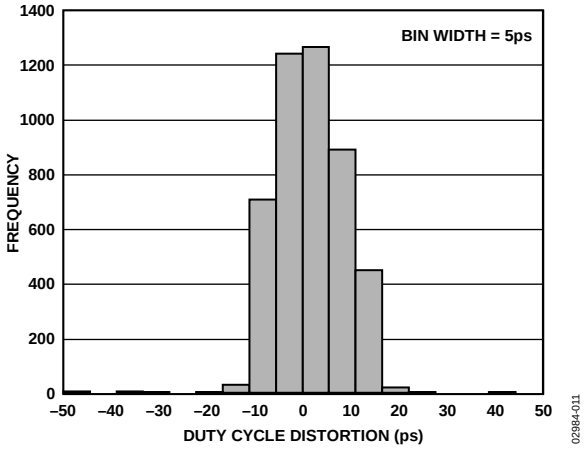

Figure 15. Duty Cycle Distortion Distribution

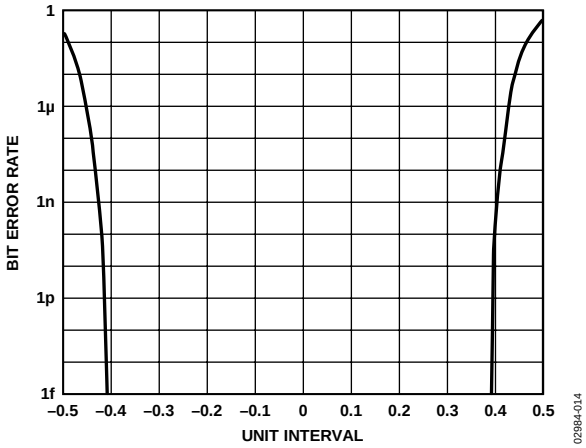

Figure 18. Bit Error Rate vs. Unit Interval

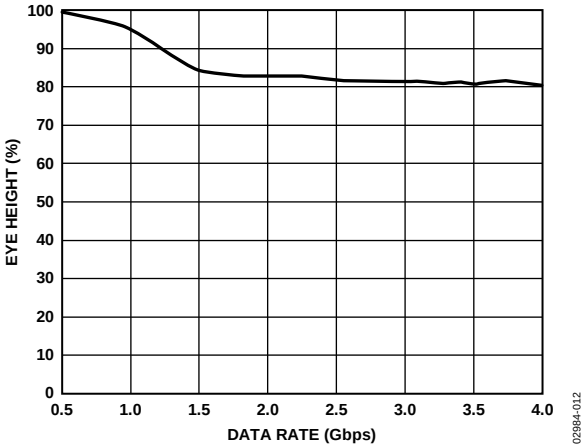

Figure 16. Eye Height vs. Data Rate

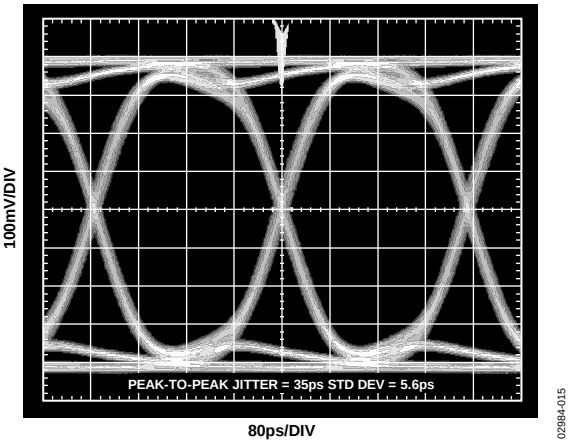

Figure 19. Crosstalk, 3.2 Gbps, Attack Signal Off (See Figure 33)

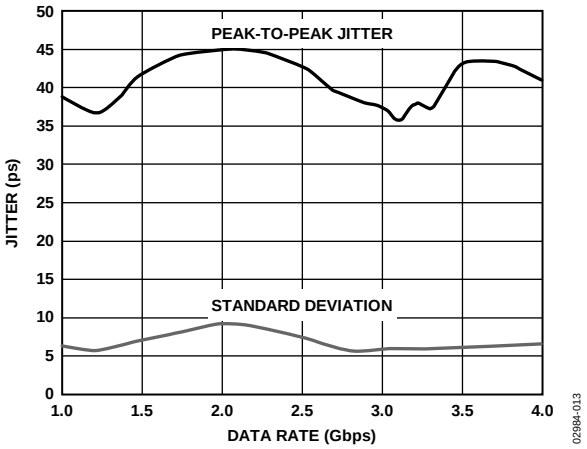

Figure 17. Jitter vs. Data Rate

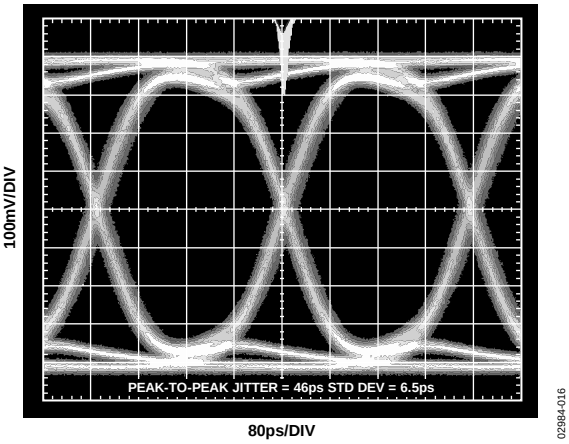

Figure 20. Crosstalk, 3.2 Gbps, Attack Signal On (See Figure 33)

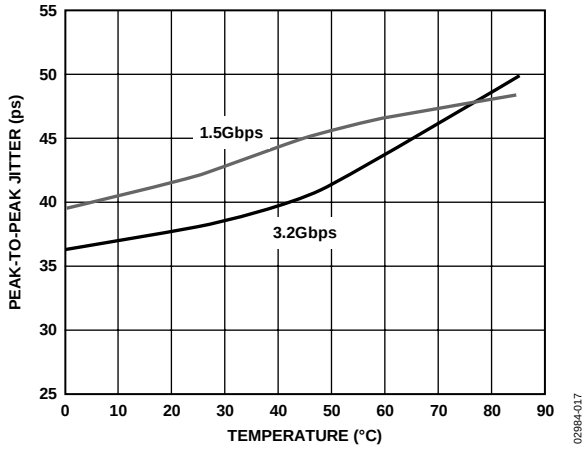

Figure 21. Peak-to-Peak Jitter vs. Temperature

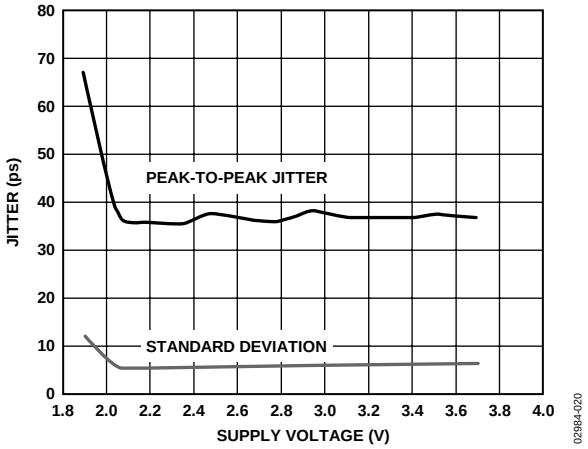

Figure 24. Jitter vs. Supply Voltage

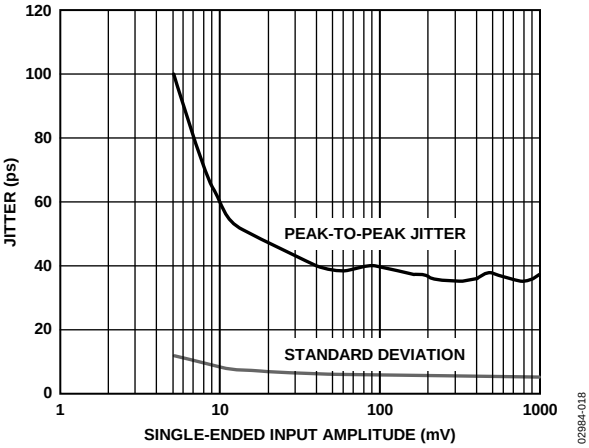

Figure 22. Jitter vs. Single-Ended Input Amplitude

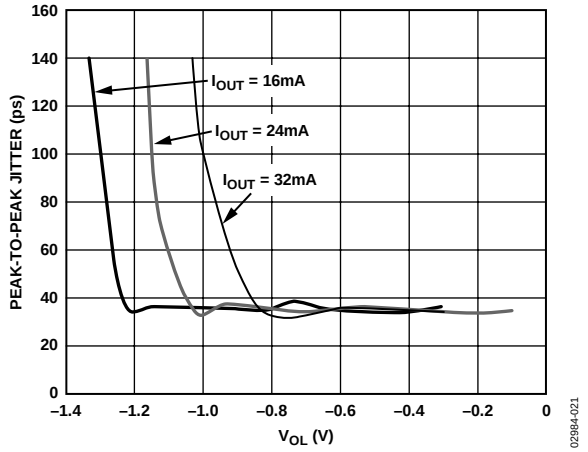

Figure 25. Peak-to-Peak Jitter vs. V_{OL} (Relative to VCC)

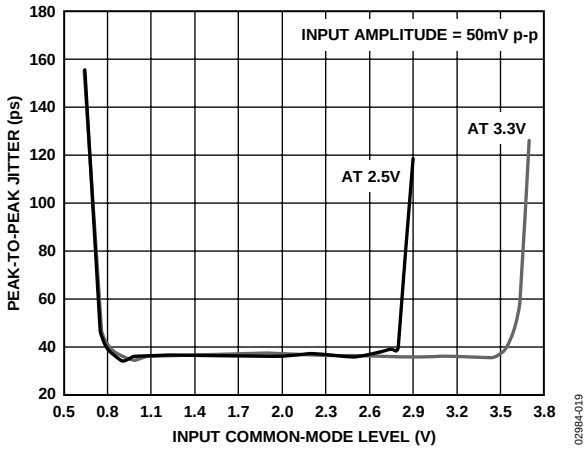

Figure 23. Peak-to-Peak Jitter vs. Input Common-Mode Level

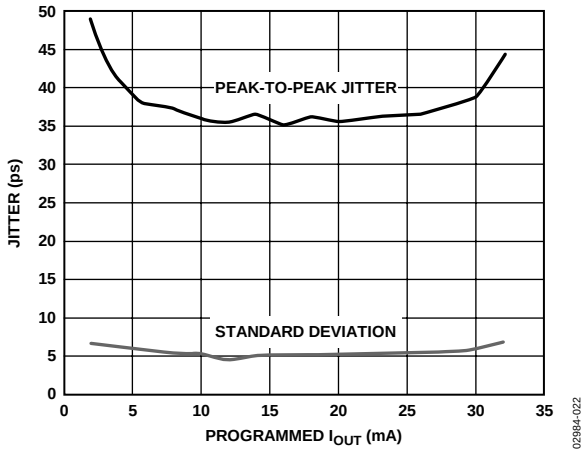

Figure 26. Jitter vs. Programmed I_{OUT}

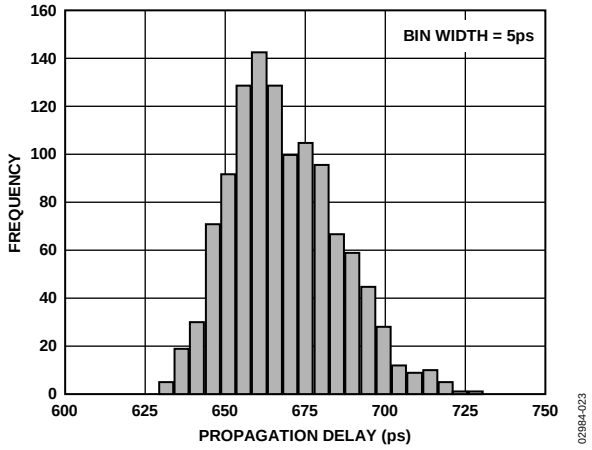

Figure 27. Variation in Propagation Delay

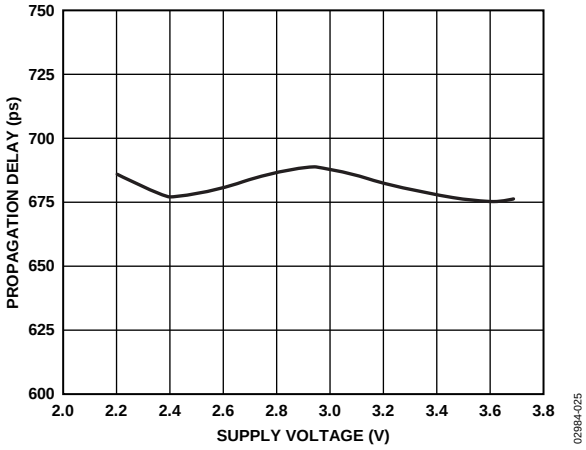

Figure 29. Propagation Delay vs. Supply Voltage

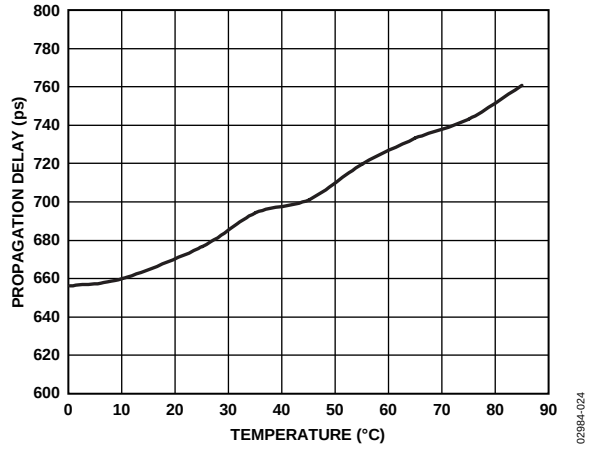

Figure 28. Propagation Delay vs. Temperature

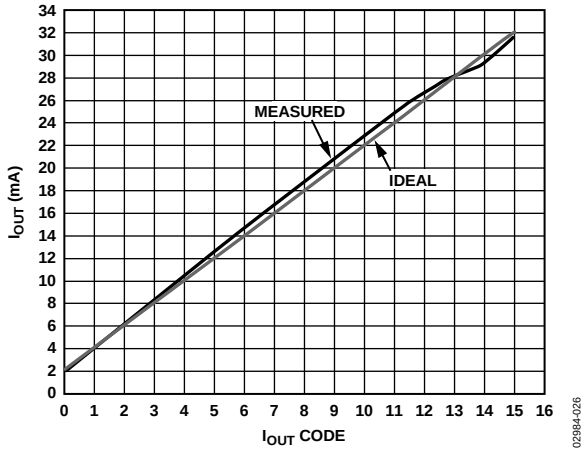

Figure 30. I_{OUT} vs. I_{OUT} Code

TEST CIRCUITS

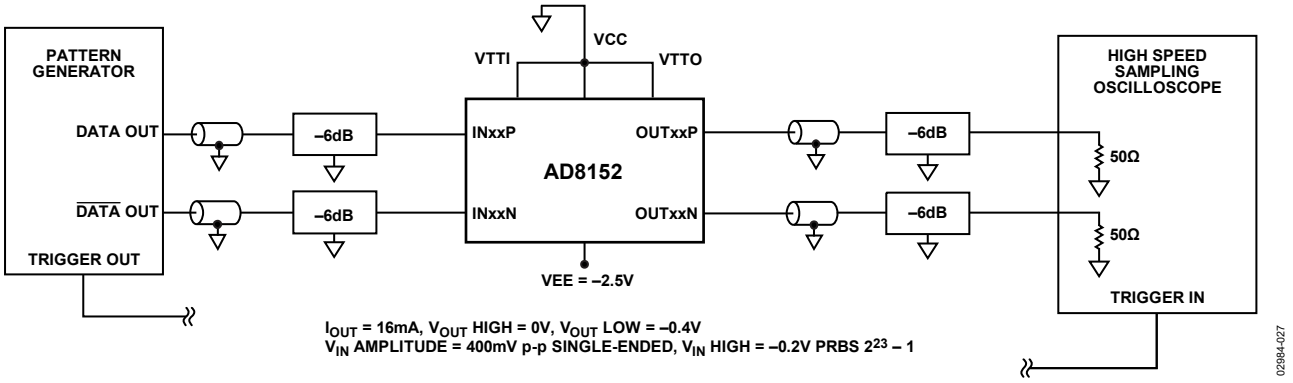

Figure 31. Negative Supply Test Circuit

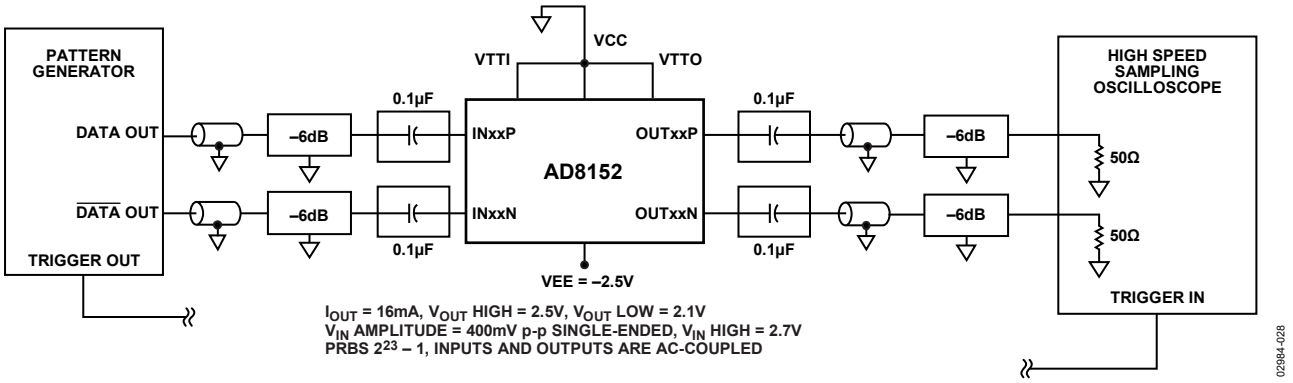

Figure 32. Positive Supply Test Circuit

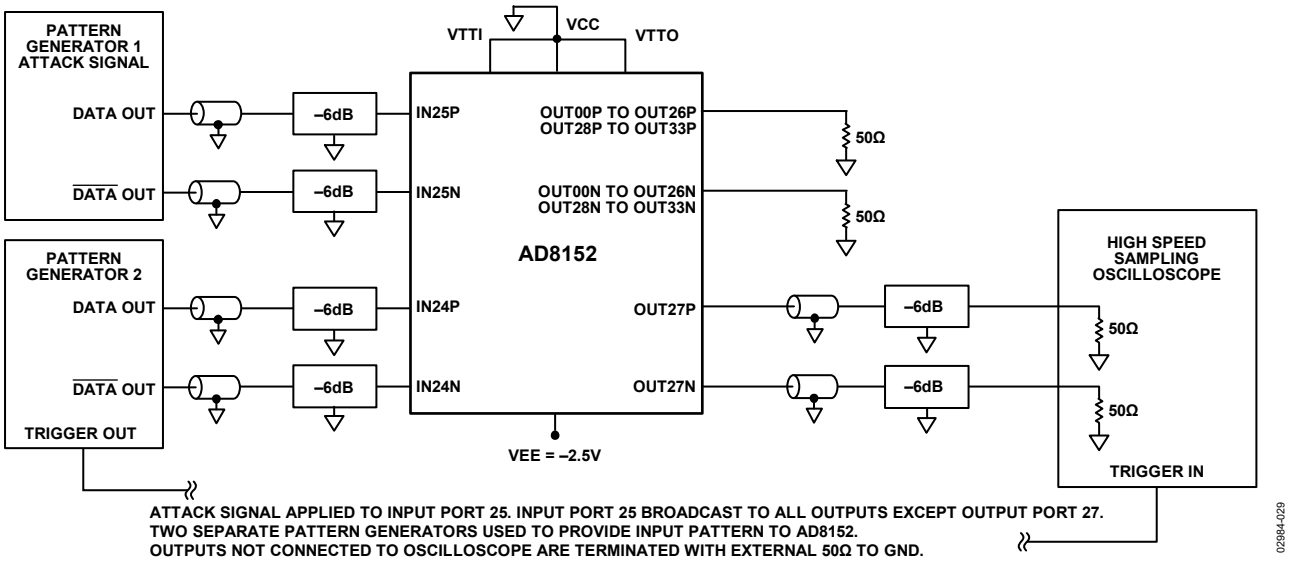

Figure 33. Crosstalk Test Circuit

THEORY OF OPERATION

The AD8152 control interface receives and stores the desired connection matrix and output levels for the 34 input and 34 output signal pairs. The interface consists of 34 rows of double-rank 6-bit latches, one for each output. The 6-bit data-word stored in these latches indicates to which (if any) of the 34 inputs the output is connected, as well as the full-scale output current.

One output at a time can be preprogrammed by addressing the output and writing the desired connection data or output current into the first rank of latches. This process can be repeated until all desired output changes are preprogrammed. All output connections can then be programmed simultaneously by passing the data from the first rank of latches into the second rank. The output connections always reflect the data programmed into the second rank of latches and do not change until the first rank of data is passed into the second rank.

If necessary for system verification, the data in the second rank of latches can be read back from the control interface.

At any time, a reset pulse can be applied to the control interface to globally reset the appropriate second rank data bits, disabling all 34 signal output pairs and resetting the output currents. To facilitate multiple chip address decoding, there is a chip select pin. All logic signals except the reset pulse are ignored, unless the chip select pin is active. The chip select pin disables only the control logic interface and does not change the operation of the signal matrix. The chip select pin does not power down any of the latches thus, any data programmed in the latches is preserved.

All control pins are level sensitive, not edge triggered.

CONTROL PIN DESCRIPTION

A0 to A6 Inputs

A0 to A6 output address pins. The binary encoded address applied to the lower A5 to A0 input pins determines which of the 34 outputs is being programmed (or being read back). The most significant bit, A6, determines whether the data pins contain information for the connection register bank or the output level register bank. Using the broadcast address, A5 to A0 = 111111 simultaneously programs data into all of the outputs.

D5 to D0 Inputs/Outputs

D0 to D5 input configuration or output level data pins. In write mode, when the bank selection bit A6 is low, the binary encoded data applied to Pin D5 to Pin D0 determine which of the 34 inputs is to be connected to the output specified with the A5 pin to A0 pin. The most significant bit is D5 and the least significant bit is D0. To disable an output completely, the input address D5 to D0 = 111111 must be written into the input configuration bank at the desired output address.

In write mode, when the bank selection bit, A6, is high, the binary encoded data applied to Pin D3 to Pin D0 indicate the output current level to be used for the output specified with the A5 pin to A0 pin. The reset default is 0111 for 16 mA. Each LSB is 2 mA.

In readback mode, Pin D5 to Pin D0 are low impedance outputs indicating the data-word stored in the second rank for the output specified with the A5 pin and A0 pin and the bank specified with the A6 bit. The readback drivers are designed to drive high impedances only. Therefore, external drivers connected to D5 to D0 must be disabled during readback mode.

$\overline{\text{WE}}$ Input

$\overline{\text{WE}}$ is the first rank write enable pin. Forcing this pin to logic low allows the data on Pin D5 to Pin D0 to be stored in the first rank latch for the output specified by Pin A6 to Pin A0. The $\overline{\text{WE}}$ pin must be returned to a logic high state after a write cycle to avoid overwriting the first rank data.

$\overline{\text{UPDATE}}$ Input

$\overline{\text{UPDATE}}$ is the second rank write enable pin. Forcing this pin to logic low allows the data stored in all 34 first rank latches (in both banks) to be transferred to the second rank latches. The signal connection matrix is reprogrammed when the second rank data and levels are changed. $\overline{\text{UPDATE}}$ is a global pin, transferring all 34 rows of data at once. It is not necessary to program the address pins. After initial power-up of the device, the first rank data is undefined. It is recommended to preprogram all 17 outputs before performing the first update cycle.

$\overline{\text{RE}}$ Input

$\overline{\text{RE}}$ is the second rank read enable pin. Forcing this pin to logic low enables the output drivers on the bidirectional D5 pin to D0 pin, entering the readback mode of operation. By selecting an output address with the A6 pin to A0 pin and forcing $\overline{\text{RE}}$ to logic low, the 6-bit data stored in the second rank latch for that output address is written to the D5 pin to D0 pin. It is not recommended to write data to the D5 pin to D0 pin externally while in readback mode. The $\overline{\text{RE}}$ pin is a higher priority pin than the $\overline{\text{WE}}$ pin. Therefore, first rank programming is not possible while in readback mode.

$\overline{\text{CS}}$ Input

$\overline{\text{CS}}$ is the chip select pin. This pin must be forced to logic low to program or receive data from the logic interface, with the exception of the $\overline{\text{RESET}}$ pin, described in the $\overline{\text{RESET}}$ Input section. This pin has no effect on the signal pairs and does not alter any of the stored control data.

$\overline{\text{RESET}}$ Input

$\overline{\text{RESET}}$ is the global output disable pin. Forcing the $\overline{\text{RESET}}$ pin to logic low disables all outputs and, regardless of the state of any other pins, sets both ranks of all 34 input connection latches. This logic low immediately disables the 34 output signal pairs in the matrix. The output level information is also changed. It is necessary to momentarily hold $\overline{\text{RESET}}$ at a logic low state when powering up the AD8152 to avoid random internal contention where multiple inputs may be connected to one output. The $\overline{\text{RESET}}$ pin is not gated by the state of the chip select pin, $\overline{\text{CS}}$.

Control Interface Levels

The AD8152 control interface shares the data path supply pins, VCC and VEE. The potential between the positive logic supply (VCC) and the negative supply (VEE) must be at least 2.25 V and no more than 3.63 V. Regardless of the supply, the logic threshold is approximately one-half the supply range, allowing the interface to be used with most LVCMOS and LVTTL logic drivers.

Output Addressing

The AD8152 is programmed using a memory interface module, with parallel address and data buses. Six bits, [A5:A0], are used to address the outputs (see Table 5). By setting the decimal value of these address bits to a value from 0 to 33 inclusive, one of the 34 outputs is uniquely addressed.

One additional decimal code, 63 (all 1s), is used for the broadcast mode. If this address is selected, then all outputs receive the same programming. The remaining addresses in the register space are not valid and are reserved, Decimal Code 34 to Decimal Code 66 inclusive.

Connection and Output Current Programming

A seventh address bit (A6) determines which of two types of programming is selected. If A6 = 0, connection matrix programming (connecting an input to an output) is selected. If A6 = 1, output current programming is selected.

Output Current Programming

A current source in each output can be digitally programmed to any one of 16 different current levels. Changing these current levels changes the amplitude of the output swing that is developed across the internal 50 Ω termination resistors.

To program the current for a particular output, the address is set on Control Pin A5 to Control Pin A0 (Decimal Code 00 to Decimal Code 33), while A6 is set to 1. The four LSBs of the data address, [D3:D0], are then used to select one of the 16 output current levels. D4 and D5 assume the don't care value for output current programming (see Table 5).

To program all outputs to the same current level, set the address bus, A5 to A0, to broadcast Decimal Code 63 with A6 = 1. Address Pin D3 to Address Pin D0 then program all output currents to the same level.

When the current code is set to 0000, a minimum current level of 2 mA is obtained. For any other code, the current can be calculated by (current code) × 2 mA + 2 mA. Refer to Table 5 for current code values. For example, 16 mA can be programmed by Decimal Code 7. This value is 7 × 2 mA + 2 mA = 16 mA.

Using the Data Bus

After determining which output to program (or broadcast to all outputs) and which type of programming (connection/output current) to use, the data bits, [D5:D0], then further define the programming action.

If connection programming (A6 = 0) is selected, the data bits select the input that is to be connected to the addressed output. If the broadcast address is selected, the data bits select the input that is connected to all 34 outputs (see Table 4).

A disable code (Bits[D5:D0] = 63 decimal value, or all 1s) disables (and powers down) the particular output that is addressed. A broadcast can be put into effect by setting Decimal Code 63 on both the address bus and the data bus along with A6 = 0.

Register Control Signals

Several single-ended logic input pins control the register loading associated with the address and data buses described in the Using the Data Bus section. The control functions are tabulated in Table 6

There are dual ranks of registers for the data that programs the AD8152. The first rank registers accumulate the data for the various outputs as they are being programmed one by one. The second rank registers actually control the functions of the device.

The $\overline{\text{RESET}}$ signal resets the connection matrix, disables all outputs, and sets all of the output currents to a default condition at Decimal Code 7. This signal sets the output current to a nominal value of 16 mA. The data in the first rank latches is also reset by the assertion of $\overline{\text{RESET}}$.

The $\overline{\text{CS}}$ signal enables the control interface. If several devices are used in a system with the other control signals bussed, the $\overline{\text{CS}}$ signal can select an individual device to change the programming.

The $\overline{\text{WE}}$ signal enables writing data to the first rank registers. This data does not immediately affect the features of the AD8152.

The $\overline{\text{UPDATE}}$ signal transfers the data from the first rank registers to the second rank registers. After the $\overline{\text{UPDATE}}$ signal is asserted, the data actively controls the AD8152 functions.

The second rank registers can be read back through the data bus. The output is addressed on Bits[A5:A0] and the connection or current is selected via A6. Asserting $\overline{\text{RE}}$ causes the second rank data to appear on the data bus. The $\overline{\text{RE}}$ function dominates over $\overline{\text{WE}}$ if both are asserted at the same time. Broadcast readback is not permitted.

Some typical programming waveforms for the control signals are provided in Figure 34.

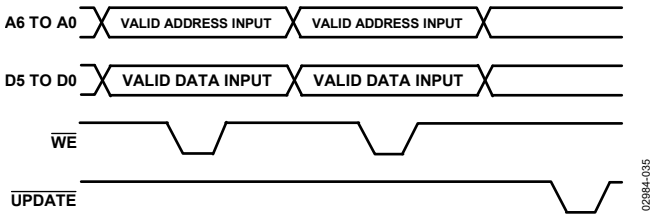

Figure 34. Programming Waveforms

Internal Input/Output Termination

The AD8152 includes 50 Ω termination resistors to match single-ended 50 Ω or 100 Ω transmission lines. All of the input termination resistors connect to one common point called VTTI. Similarly, each of the output termination resistors connects to one common point called VTTO. The voltage can be set independently at VTTI and VTTO to accommodate various interface architectures.

Input Coupling

One way to simplify the input circuit and make it compatible with a wide variety of driving devices is to use ac coupling. This ac coupling has the effect of isolating the dc common-mode levels of the driver and the AD8152 input circuitry. For example, the XAUI interconnect specification for 10 Gbps Ethernet requires ac coupling to ensure that there are no interactions of dc levels between the transmitting and receiving devices.

AC coupling requires that the signal patterns have no long-term dc component, which may occur in any random data stream. Codes such as 8-bit/10-bit, called for in the XAUI specification, are used in many data communications systems to ensure that the data pattern maintains a common-mode balance. This is accomplished by run length limiting (RLL), which sets a maximum limit for the number of 1s or 0s that can occur consecutively. In addition, residual dc components are monitored and modified by keeping track of the running disparity, excess of 1s vs. 0s, or vice versa.

For the AD8152 inputs, ac coupling requires a capacitor in series with each single-ended input signal, as shown in Figure 35. AC coupling is recommended to be done in a manner that does not interfere with the high speed signal integrity of the PCB board. The two critical variables are setting the proper voltage for VTTI and selecting the correct value of coupling capacitors.

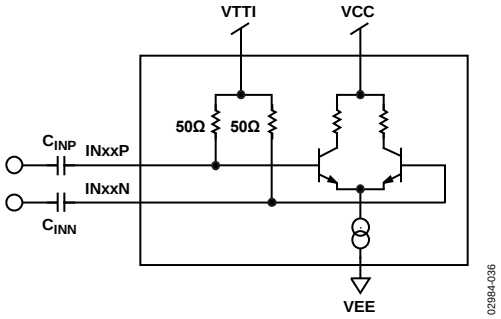

Figure 35. AC Coupling Input Signal from AD8152

On the AD8152 side of the input coupling capacitor, the average value of the single-ended input voltage is at the voltage set at VTTI. The range of allowable voltages is a function of the acceptable input voltages of the active circuitry of the AD8152 inputs and the amplitude of the input signal. The operating input range of the AD8152 extends from VCC + 0.2 V to 0.8 V above VEE.

The total range that is occupied by the input signal is the average value (as established by the voltage applied to VTTI) plus or minus one half the single-ended swing of the signal. For a standard 800 mV p-p differential signal, the single-ended swing is 400 mV p-p. Thus, the signal swings ±200 mV around the average value equal to VTTI.

If VTTI is set equal to VCC, the single-ended signal meets the specifications where the highest input voltage level does not exceed the design compliance threshold of VCC + 0.2 V. The lowest signal-ended input voltage level must be greater than 0.8 V above VEE to maintain compliance with the design specification.

With ac-coupled inputs, there is no power consumption advantage associated with varying VTTI. As a practical matter, it may be desirable to set VTTI at the same voltage as VTTO so that only one supply is necessary.

Output Coupling

Each single-ended output of the AD8152 has a 50 Ω termination resistor that ties to VTTO. The differential termination tied to VTTO is 25 Ω. When VTTO is varied, it changes the common-mode levels of the outputs and the power dissipation of the output stages when enabled.

The individual output currents are programmable. Varying this output current changes the lower level of the output voltage (and thus the peak-to-peak swing) and changes the power dissipation in the output stages. To obtain a standard 800 mV p-p differential output (single-ended = 400 mV p-p), it is recommended to program the output current to 16 mA.

If the AD8152 drives another device that is ac-coupled, there is no interaction of the dc levels on each side of the coupling capacitors (see Figure 36). The dc levels for the AD8152 can be calculated independently of the levels of the driven device. The upper allowable setting for VTTO is 0.2 V higher than VCC.

To save power, VTTO can be lowered. The lowest level for VTTO is determined by the lowest output level allowable (V_{OL}) by the AD8152 output when the output signal is logically low. It is recommended that the output does not go lower than 1.0 V below VCC. If the single-ended swing of an output is 400 mV p-p, the lowest that VTTO can go is 0.6 V below VCC. For more information on V_{OL}, see Figure 25.

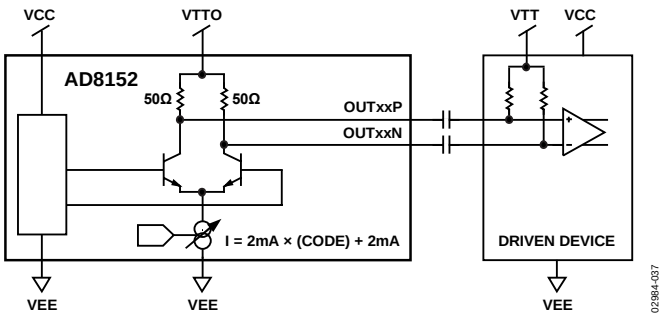

Figure 36. AC Coupling Output Signal from AD8152

AD8152 POWER CONSUMPTION

Several sections of the AD8152 draw varying levels of power depending on the supply voltages, the type of input/output coupling used, and the status of the AD8152 operation. Figure 37 shows a block diagram of these sections. The AD8152 contains six main circuit blocks that determine the overall power consumption of the device. Table 15 summarizes the power consumption of each section and is a useful guide as the next sections are reviewed.

The first section is the input termination resistors. The power dissipated in the termination resistors is the result of being driven by the respective driving stage. DC power may also be dissipated in the input termination resistors if the inputs are dc-coupled and the driving source reference is a dc voltage that is not equal to VTTI.

In the next section, the active part of the input stages, each input is powered only when it is selected. If an input is not selected, it is powered down. Thus, the total number of active inputs affects the total power consumption. The core of the device performs the crosspoint switch matrix that draws a fixed quiescent current whenever the AD8152 is powered from VCC to VEE.

An output predriver section draws a current that is proportional to the programmed output current, I_{OUT}. This current always flows from VCC to VEE. The predriver current is treated separately from the output current, which flows from VTTO, and may not be the same voltage as VCC.

The final section is the outputs. For an individual output, the programmed output current flows through two separate paths. One path is the on-chip termination resistor, and the other path is the transmission line and the destination termination resistor. The nominal parallel impedance of these two paths is 25 Ω. The sum of these two currents flows through the switches and the current source of the AD8152 output circuit, and then out through VEE.

The power dissipated in the transmission line and destination resistor does not dissipate in the AD8152 but must be supplied from the power supply and is factored into the overall system power. The current in the on-chip termination resistors and output current source dissipates power in the AD8152.

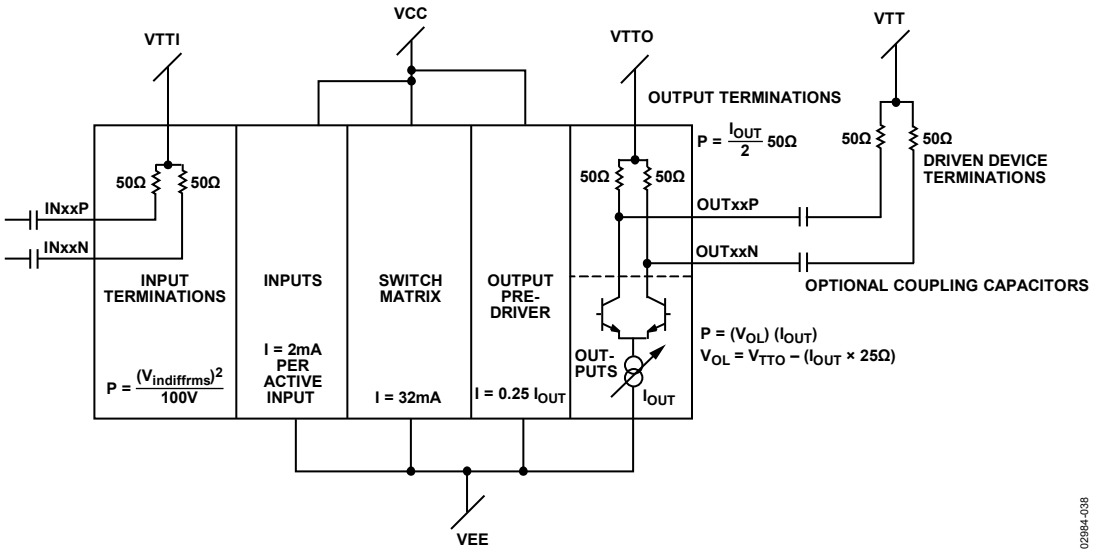

Figure 37. Power Consumption Block Diagram

Table 15. Power Consumption

Parameter	Input Termination Resistors	Input Stage	Core	Output Predriver	Output Termination Resistors	Output Switch + Current Source	Total Power
Quiescent Current	N/A	N/A	32 mA	N/A	N/A	N/A	N/A
Current per Active Channel	$V_{IN}/(R_{TERMINATION})$	2 mA	N/A	0.25 × I_{OUT}	0.5 × I_{OUT}	I_{OUT}	N/A
Current per Active Channel for Differential	N/A	N/A	N/A	N/A	N/A	N/A	N/A
V_{IN} = 800 mV p-p Sine	566 mV rms/100	N/A	N/A	N/A	N/A	N/A	N/A
V_{OUT} = 800 mV p-p	= 5.66 mA	2 mA	4 mA	4 mA	8 mA	16 mA	N/A
2.5 V Operation (VCC – VEE = 2.5 V, VTTO = 2.5 V, I_{OUT} = 16 mA)							
Per Channel Power	3.2 mW	5 mW		10 mW	8 mW	33.6 mW	N/A
Power for All Channels Active	108.8 mW	170 mW	80 mW	340 mW	272 mW	1.03 W	2.0 W
Percentage of Total Power	5%	8%	4%	17%	13.6%	51%	N/A
3.3 V Operation (VCC – VEE = 3.3 V, VTTO = 3.3 V, I_{OUT} = 16 mA)							
Per Channel Power	3.2 mW	6.6 mW		13.2 mW	8 mW	46.4 mW	N/A
Power for All Channels Active	108.8 mW	224 mW	106 mW	449 mW	272 mW	1.47 W	2.63 W
Percentage of Total Power	4%	9%	4%	17%	10%	56%	N/A

Input Termination Resistors

The power dissipated in the input termination resistors is delivered by the driving source. First, assume the driving waveform for an individual input is a differential square wave with an amplitude of V_{INPP}. Then the power dissipated in this input is $(V_{INPP})^2/2R_{TERM}$, where R_{TERM} is the termination resistor.

If dc coupling is used, a dc current flows from VTTI through the termination resistors if the dc voltage of the drive circuit is not equal to VTTI. The additional power in each input termination resistor is the current multiplied by the 50 Ω value of the input terminations.

For a point of reference, assume a channel has a sinusoidal input of 800 mV p-p differential. The power dissipated for a single input is 3.2 mW. If all 34 input channels are driven the same, the power in the input terminations is 109 mW.

Input Stage

The input stages are powered down when not in use. Approximately 2 mA flows through an enabled input from VCC to VEE. Thus, the power dissipated by an enabled input is 5 mW for a supply of 2.5 V and 6.6 mW for a 3.3 V supply. When all 34 inputs are enabled, the total power consumed in the input stage is approximately 170 mW (VCC = 2.5 V) and 224 mW (VCC = 3.3 V).

Switch Matrix

The switch matrix draws a fixed 32 mA when the AD8152 is powered. This current flows from VCC to VEE. The power dissipation from this current is 80 mW at 2.5 V and 106 mW at 3.3 V.

Output Predrivers

The output predrivers draw additional current when each output is enabled. This extra current is proportional to the programmed output current. The extra predriver current for a channel is 25% of the programmed output current for that channel. This current also flows from VCC to VEE.

When an output is enabled and programmed to 16 mA, an additional 4 mA flows in the predriver section. This predriver current dissipates either 10 mW at 2.5 V or 13.2 mW at 3.3 V for an individual output.

For all enabled 34 outputs and programmed to 16 mA, the predriver power is 340 mW at 2.5 V or 449 mW at 3.3 V.

OUTPUTS

The output current is forced by a current source that is programmed to a variable amount of current from 2 mA to 32 mA in 2 mA steps. For the two logic switch states, this output current flows through an on-chip termination resistor and a parallel path to the destination device and termination resistor. The power in this parallel path is not dissipated by the AD8152.

The nominal programmed output current is 16 mA. With the two parallel 50 Ω resistors at each collector (25 Ω equivalent), this current creates a 400 mV p-p swing in each half of the circuit. The differential output voltage is 800 mV p-p.

Under steady state conditions and with a data pattern that is run length limited so that the low frequency content is significantly higher than the RC pole formed by the coupling capacitor and the termination resistors, the common-mode level at the AD8152 outputs is 400 mV lower than VTTO. Each output then swings ±200 mV from this level, which is a 400 mV p-p single-ended output swing.

At the high level, there is 200 mV across the termination resistor, which dissipates a power of 0.8 mW. At the low level, the 600 mV across the termination resistor dissipates a power of 7.2 mW. Because the output signal is essentially 50% duty cycle, the average power dissipated is the average of these two values or 4 mW. By symmetry, the other differential output dissipates the same power. The total power dissipated through the on-chip termination resistor is approximately 8 mW per channel for each output, or 272 mW for all 34 outputs.

The full output current (from both on- and off-chip termination resistors) flows in the lower part of each output. This current flows only in the side that is on, or in the low state (V_{OL}). This voltage is 600 mV below the dc level at VTTO.

Thus, for VTTO = 2.5 V, V_{OL} = 1.9 V, and the power dissipation for I_{OUT} = 16 mA is 30.4 mA. For all 34 channels, the power is 1.03 W.

If VTTO = 3.3 V, then V_{OL} = 2.7 V. The single power is 43.2 mW and the power for all 34 channels is 1.47 W.

If VTTO = 2.5 V, then the additional power is given by 16 mA × ((2.5 V − (16 mA × 25 Ω)) = 33.6 mW. Thus, the total AD8152 power dissipation for this output is 37.6 mW.

If all 34 outputs are enabled with the same I_{OUT}, the total power dissipation is 1.28 W. Thus, it can be seen that the outputs are the major contributor to the power dissipation.

Power Saving Considerations

Although the AD8152 power consumption is very low compared to similar devices, careful control of the operating conditions can yield even further power savings. Significant power reduction can be achieved by operating the device at a lower voltage. Compared to 3.3 V operation, a supply voltage of 2.5 V can result in power savings of about 25%. There is virtually no performance penalty when operating at lower voltage.

A second measure is to disable outputs when they are not being used, either on a static basis, if the output is not used, or on a dynamic basis, if the output does not have a constant stream of traffic.

Because the majority of the power dissipated is in the output stage, some of the flexibility can be used to lower the power consumption.

First, the output current can be programmed to the lowest programmable value to maintain bit error rate (BER) performance. If an output circuit always has a short length and the receiver has acceptable sensitivity, a lower output current can be used.

It is also possible to lower the voltage on VTTO to lower the power dissipation. The amount that VTTO can be lowered is dependent on the lowest V_{OL} of all the output. This V_{OL} value is determined by the output that is operating at the highest programmed output current because V_{OL} = VTTO − (I_{OUT} × 25 Ω).

OUTLINE DIMENSIONS

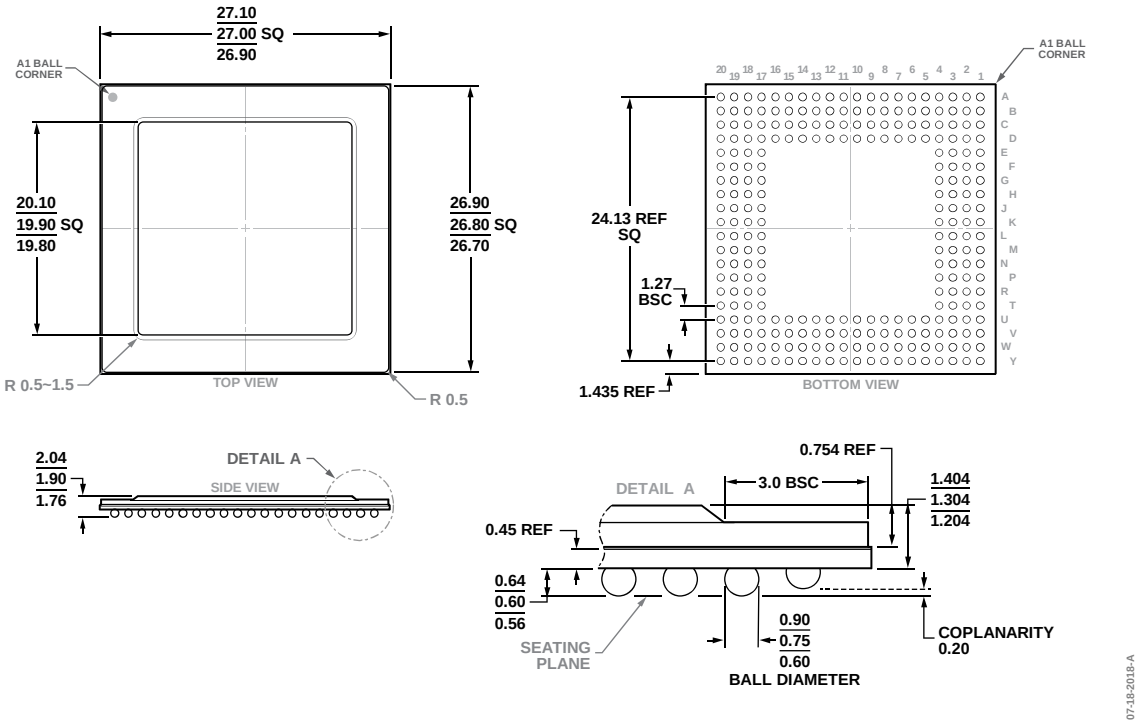

Figure 38. 256-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]
(BP-256-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8152JBPZ	0°C to 85°C	256-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]	BP-256-3

[1] Z = RoHS Compliant Part.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Analogue & Digital Crosspoint ICs ***category:***

Click to view products by Analog Devices ***manufacturer:***

Other Similar products are found below :

MT093AE1 MT8808AE1 ADV3203ASWZ AD8177ABPZ ISPGDX240VA-4B388 VSC3308YKU ISPGDX240VA-4BN388 LX256EV-5FN484C AD8112JSTZ AD8115ASTZ SN65LVCP22D ADV3205JSTZ SY89540UMY AD75019JPZ AD75019JPZ-REEL AD8106ASTZ AD8107ASTZ AD8108ASTZ AD8110ASTZ AD8111ASTZ AD8116JSTZ AD8152JBPZ AD8153ACPZ AD8155ACPZ AD8158ACPZ AD8159ASVZ ADN4604ASVZ AD8153ACPZ-RL7 ADN4600ACPZ ADV3201ASWZ ADV3226ACPZ ADV3227ACPZ ADV3228ACPZ ADV3229ACPZ HMC858LC4B HMC857LC5 MAX4550CAI+ EL4544IGZ HA4314BCPZ MAX9152EUE+T MAX3840ETJ+ MAX4360EAX+ MAX4360EAX+T MAX4549EAX+ MAX4570CWI+ MAX4549EAX+T MAX4570CAI+ MT8806AP1 MAX9152EUE+ MAX9392EHJ+