700 MHz, 5 mA 4-to-1 Video Multiplexer

AD8184

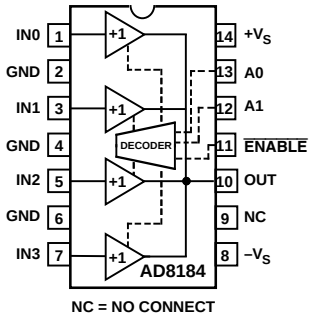
FEATURES

Single and Dual 2-to-1 Also Available (AD8180 and AD8182)
Fully Buffered Inputs and Outputs
Fast Channel Switching: 10 ns
High Speed
> 700 MHz Bandwidth (–3 dB)
> 750 V/μs Slew Rate
Fast Settling Time of 15 ns to 0.1%
Excellent Video Specifications (R_L > 2 kΩ)
Gain Flatness of 0.1 dB of 75 MHz
0.01% Differential Gain Error, R_L = 10 kΩ
0.01° Differential Phase Error, R_L = 10 kΩ
Low Power: 4.4 mA
Low Glitch: < 25 mV
Low All-Hostile Crosstalk of –95 dB @ 5 MHz
High "OFF" Isolation of –115 dB @ 5 MHz
Low Cost
Fast Output Disable Feature for Connecting Multiple Devices

APPLICATIONS

Pin Compatible with HA4314* and GX4314*
Video Switchers and Routers
Pixel Switching for "Picture-In-Picture"
Switching in LCD and Plasma Displays

FUNCTIONAL BLOCK DIAGRAM



NC = NO CONNECT

Table I. Truth Table

$\overline{\text{ENABLE}}$	A1	A0	OUTPUT
0	0	0	IN0
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	X	X	High Z

PRODUCT DESCRIPTION

The AD8184 is a high speed 4-to-1 multiplexer. It offers –3 dB signal bandwidth of 700 MHz along with a slew rate of 750 V/μs. With 95 dB of crosstalk and 115 dB isolation, it is useful in many high speed applications. The differential gain and differential phase error of 0.01% and 0.01°, along with 0.1 dB flatness of 75 MHz, make AD8184 ideal for professional video multiplexing. It offers 10 ns switching time, making it an excellent choice for pixel switching (picture-in-picture) while consuming less than 4.5 mA on ±5 V supply voltage.

The AD8184 offers a high speed disable feature allowing the output to be put into a high impedance state. This allows multiple outputs to be connected together for cascading stages while the "OFF" channels do not load the output bus. It operates on voltage supplies of ±5 V and is offered in 14-lead PDIP and SOIC packages.

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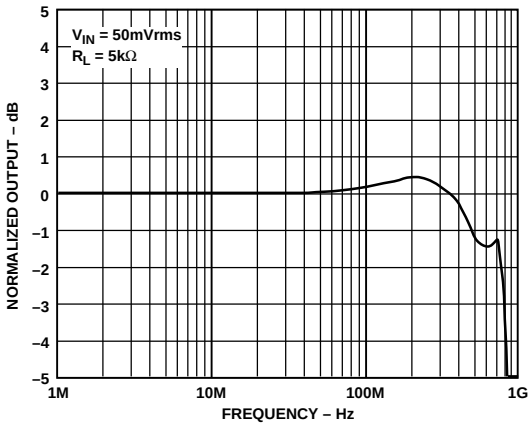

Figure 1. Small Signal Frequency Response

REV. 0

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AD8184—SPECIFICATIONS (@ T_A = +25°C, V_S = ±5 V, R_L = 2 kΩ unless otherwise noted)

Parameter		Conditions	AD8184A Min	Typ	Max	Units
SWITCHING CHARACTERISTICS						
Channel Switching Time[1]		Channel-to-Channel				
50% Logic to 10% Output Settling		IN0 = +1 V, IN1 = –1 V		5		ns
50% Logic to 90% Output Settling				10		ns
50% Logic to 99.9% Output Settling				15		ns
$\overline{\text{ENABLE}}$ to Channel ON Time[2]		A0, A1 = 0 or 1				
50% Logic to 90% Output Settling		IN0 = +1 V, –1 V or IN1 = –1 V, +1 V		12		ns
$\overline{\text{ENABLE}}$ to Channel OFF Time[2]		A0, A1 = 0 or 1				
50% Logic to 90% Output Settling		IN1 = +1 V, –1 V or IN1 = –1 V, +1 V		22		ns
Channel Switching Transient (Glitch)[3]		All Inputs Are Grounded		±25		mV
DIGITAL INPUTS						
Logic "1" Voltage		A0, A1 and $\overline{\text{ENABLE}}$ Inputs	2.0			V
Logic "0" Voltage		A0, A1 and $\overline{\text{ENABLE}}$ Inputs			0.8	V
Logic "1" Input Current		A0, A1, $\overline{\text{ENABLE}}$ = +4 V		10	200	nA
Logic "0" Input Current		A0, A1, $\overline{\text{ENABLE}}$ = +0.4 V		2	3	µA
DYNAMIC PERFORMANCE						
–3 dB Bandwidth (Small Signal)[4]	AD8184AR	V_{IN} = 50 mV rms, R_L = 5 kΩ	550	700		MHz
–3 dB Bandwidth (Large Signal)	AD8184AR	V_{IN} = 1 V rms, R_L = 5 kΩ	105	135		MHz
0.1 dB Bandwidth[4, 5]	AD8184AR	V_{IN} = 50 mV rms, R_L = 5 kΩ	60	75		MHz
Slew Rate		2 V Step	600	750		V/µs
Settling Time to 0.1%		2 V Step		15		ns
DISTORTION/NOISE PERFORMANCE						
Differential Gain		f = 3.58 MHz, R_L = 2 kΩ		0.2		%
		R_L = 10 kΩ		0.01	0.02	%
Differential Phase		f = 3.58 MHz, R_L = 2 kΩ		0.2		Degrees
		R_L = 10 kΩ		0.01	0.02	Degrees
All Hostile Crosstalk[6]	AD8184AR	f = 5 MHz		–95		dB
		f = 30 MHz		–78		dB
OFF Isolation[7]	AD8184AR	f = 5 MHz, R_L = 30 Ω		–115		dB
Voltage Noise		f = 30 MHz		4.5		nV/√Hz
Total Harmonic Distortion		f_C = 10 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–74		dBc
DC/TRANSFER CHARACTERISTICS						
Voltage Gain[8]		V_{IN} = ±1 V		0.982		V/V
Input Offset Voltage				2	8	mV
		T_{MIN} to T_{MAX}			15	mV
Input Offset Voltage Drift				5		µV/°C
Input Offset Voltage Matching		Channel-to-Channel		0.6	3	mV
Input Bias Current				2.5	7.5	µA
		T_{MIN} to T_{MAX}			9.5	µA
Input Bias Current Drift				5		nA/°C
INPUT CHARACTERISTICS						
Input Resistance			1.0	2.4		MΩ
Input Capacitance		Channel Enabled (R Package)		1.6		pF
		Channel Disabled (R Package)		1.6		pF
Input Voltage Range				±3.3		V
OUTPUT CHARACTERISTICS						
Output Voltage Swing		V_{IN} = ±4 V, R_L = 2 kΩ[9]	±3.15	±3.2		V
Short Circuit Current				30		mA
Output Resistance		Enabled		28	33	Ω
		Disabled		10		MΩ
Output Capacitance		Disabled (R Package)		3.2		pF
POWER SUPPLY						
Operating Range			±4		±6	V
Power Supply Rejection Ratio	+PSRR	$+V_S$ = +4.5 V to +5.5 V, $–V_S$ = –5 V	54	57		dB
	–PSRR	$–V_S$ = –4.5 V to –5.5 V, $+V_S$ = +5 V	51	54		dB
Quiescent Current		Enabled		4.4	5.2	mA
		T_{MIN} to T_{MAX}			5.7	mA
		Disabled		2.1	2.9	mA
		T_{MIN} to T_{MAX}			2.9	mA
OPERATING TEMPERATURE RANGE			–40		+85	°C

NOTES
[1]$\overline{\text{ENABLE}}$ pin is grounded. IN0 and IN2 = +1 V dc, IN1 and IN3 = –1 V dc. A0 is driven with a 0 V to +5 V pulse, A1 is grounded. Measure transition time from 50% of the A0 input value (+2.5 V) and 10% (or 90%) of the total output voltage transition from IN0 channel voltage (+1 V) to IN1 (–1 V), or vice versa. All inputs are measured in a similar manner using A0 and A1 to select the channels.
[2]$\overline{\text{ENABLE}}$ pin is driven with 0 V to +5 V pulse (with 3 ns edges). The state of the A0 and A1 pins determines which input is activated (refer to Table I). Set IN0 and IN2 = +1 V dc, IN1 and IN3 = –1 V dc, and measure transition time from 50% of $\overline{\text{ENABLE}}$ pulse (+2.5 V) to 90% of the total output voltage change. In Figure 4, Δt_{OFF} is the disable time, Δt_{ON} is the enable time.
[3]All inputs are grounded. A0 input is driven with 0 V to +5 V pulse, A1 is grounded. The output is monitored. Speeding the edges of the A0 pulse increases the glitch magnitude due to coupling via the ground plane. Removing the A0 and A1 terminations will lower the glitch, as does increasing R_L.
[4]Decreasing R_L slightly lowers the bandwidth. Increasing C_L significantly lowers the bandwidth (see Figure 18).
[5]A resistor (R_S) placed in series with the multiplexer inputs serves to optimize 0.1 dB flatness, but is not required (see Figure 19.)
[6]Select an input that is not being driven (i.e., A0 and A1 are logic 0, IN0 is selected); drive all other inputs with V_{IN} = 0.707 V rms and monitor the output at f = 5 and 30 MHz. R_L = 2 kΩ (see Figure 12).
[7]Multiplexer is disabled (i.e., $\overline{\text{ENABLE}}$ = logic 1) and all inputs are driven simultaneously with V_{IN} = 0.446 V rms. Output is monitored at f = 5 and 30 MHz. R_L = 30 Ω to simulate R_{ON} of one enabled multiplexer within a system (see Figure 13). In this mode the output impedance is very high (typ 10 MΩ), and the signal couples across the package; the load impedance determines the crosstalk.
[8]Voltage gain decreases for lower values of R_L. The resistive divider formed by the multiplexers enables output resistance (28 Ω) and R_L causes a gain that increases as R_L decreases (i.e., the voltage gain is approximately 0.97 V/V [3% gain error] for R_L = 1 kΩ).
[9]Larger values of R_L provide wider output voltage swings, as well as better gain accuracy. See Note 8.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 12.6 V
Internal Power Dissipation[2]
AD8184 14-Lead Plastic (N) . . . . . 1.6 Watts
AD8184 14-Lead Small Outline (R) . . . . . 1.0 Watts
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . Observe Power Derating Curves
Storage Temperature Range
N & R Package . . . . . –65°C to +125°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air: 14-pin plastic package: θ_{JA} = 75°C/Watt
14-pin SOIC package: θ_{JA} = 120°C/Watt, where $P_D = (T_J - T_A)/\theta_{JA}$.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8184AN	–40°C to +85°C	14-Lead Plastic DIP	N-14
AD8184AR	–40°C to +85°C	14-Lead Narrow SOIC	R-14
AD8184AR-REEL	–40°C to +85°C	Reel 14-Lead SOIC	R-14
AD8184-EB	Evaluation Board	For AD8184R	

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8184 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD8184 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figure 2.

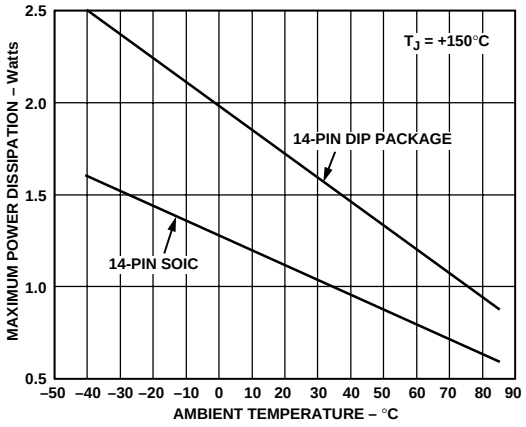
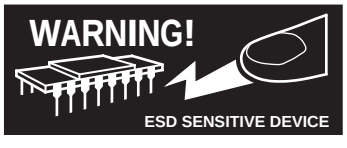


Figure 2. Maximum Power Dissipation vs. Temperature

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8184 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD8184–Typical Performance Curves

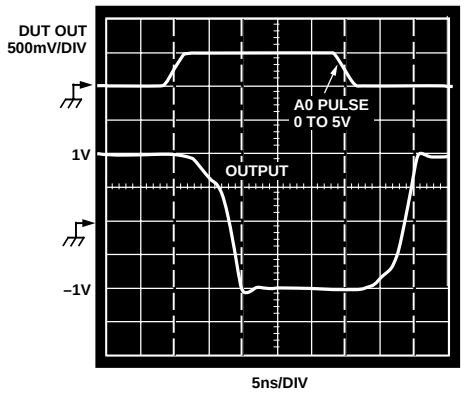


Figure 3 Channel Switching Characteristics

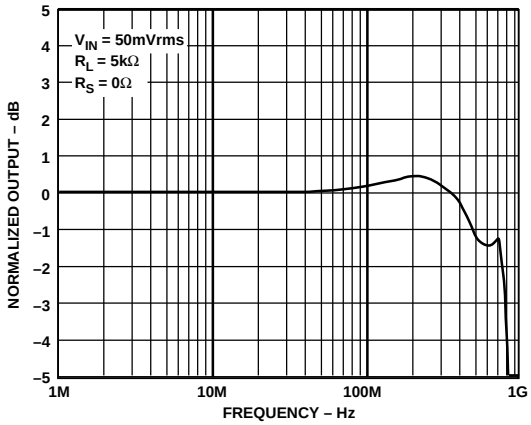


Figure 6. Small Signal Frequency Response

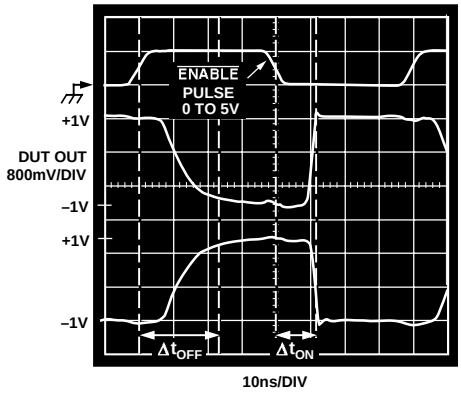


Figure 4. Enable and Disable Switching Characteristics

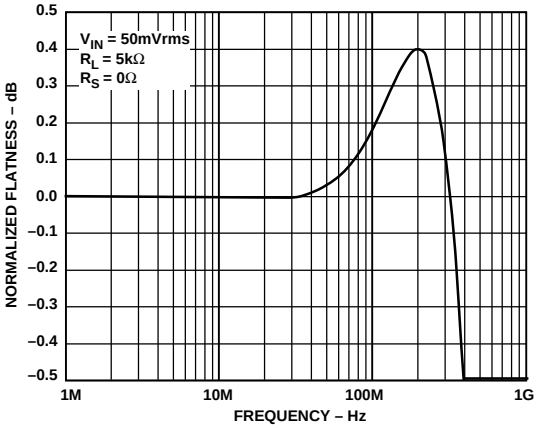


Figure 7. Gain Flatness vs. Frequency

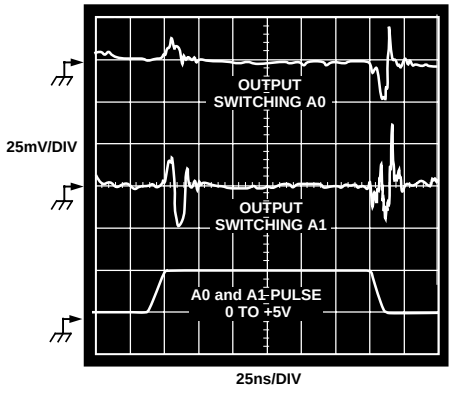


Figure 5. Channel Switching Transient (Glitch)

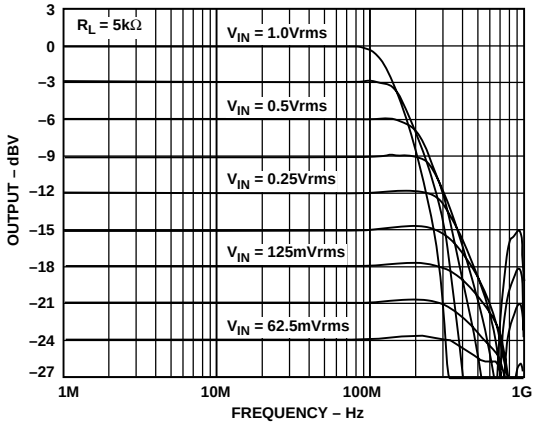


Figure 8. Large Signal Frequency Response

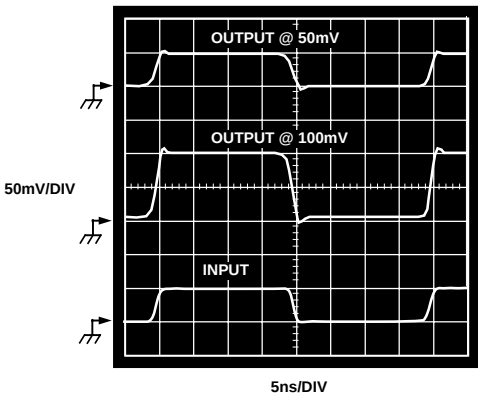


Figure 9. Small Signal Transient Response

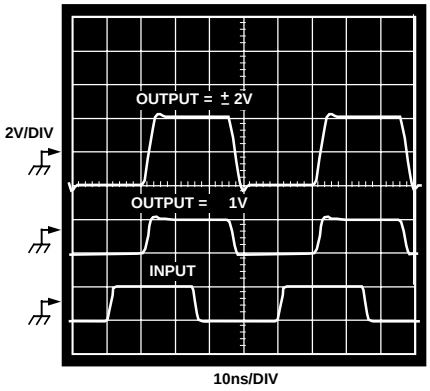


Figure 10. Large Signal Transient Response

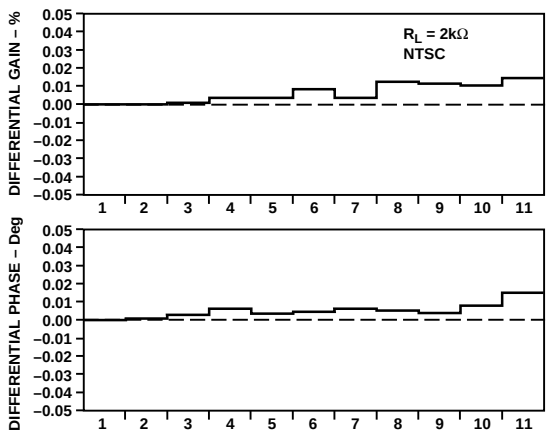


Figure 11. Differential Gain and Phase Error

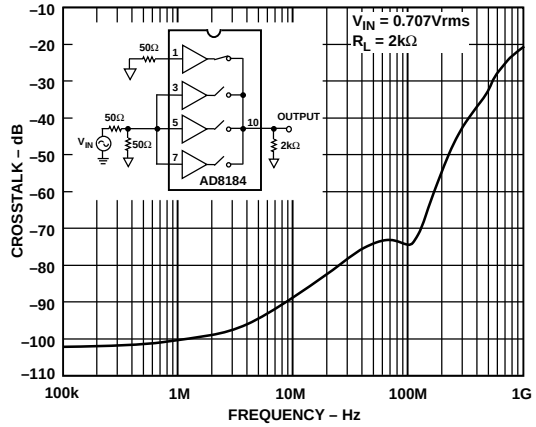


Figure 12. All-Hostile Crosstalk vs. Frequency

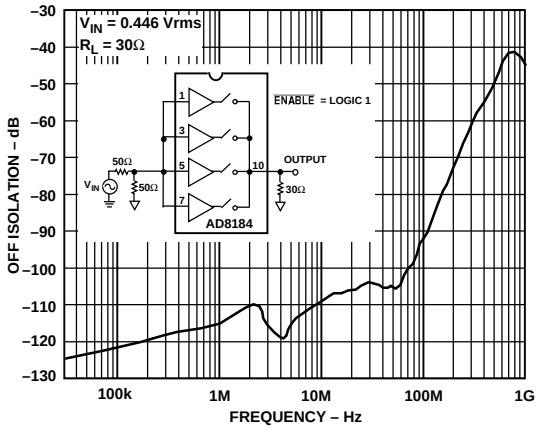


Figure 13. "OFF" Isolation vs. Frequency

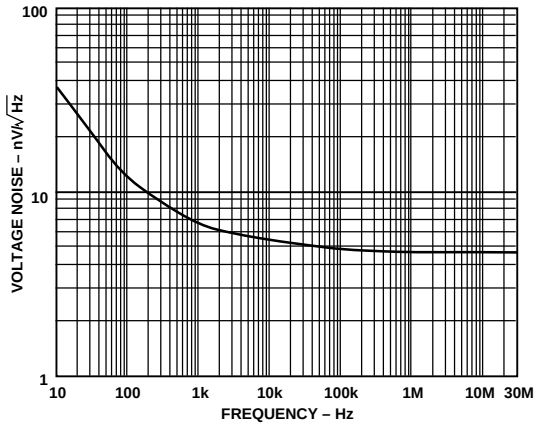


Figure 14. Voltage Noise vs. Frequency

AD8184–Typical Performance Curves

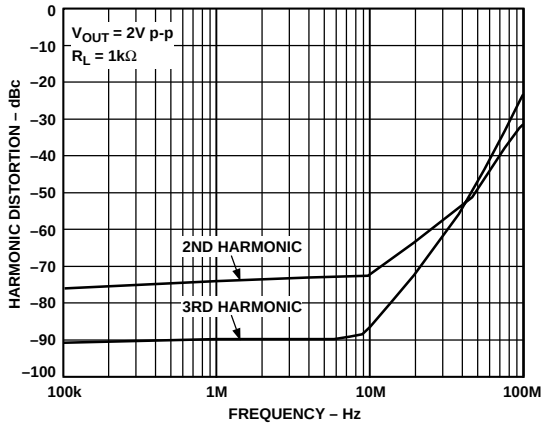


Figure 15. Harmonic Distortion vs. Frequency

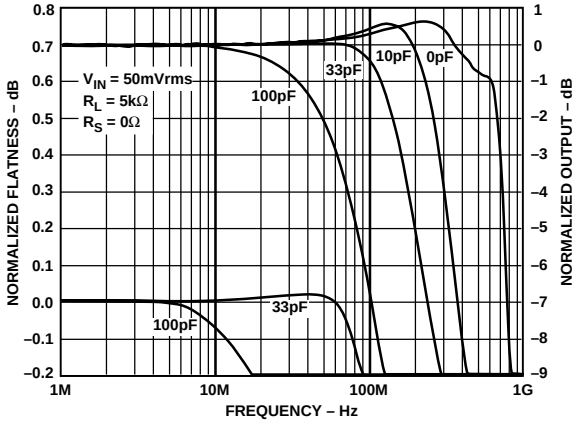


Figure 18. Frequency Response vs. Capacitive Load

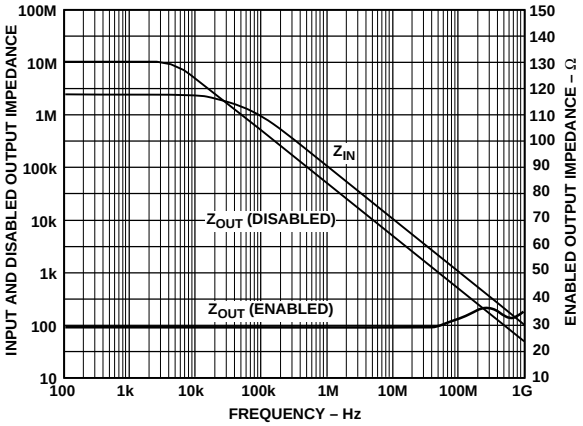


Figure 16. Output & Input Impedance vs. Frequency

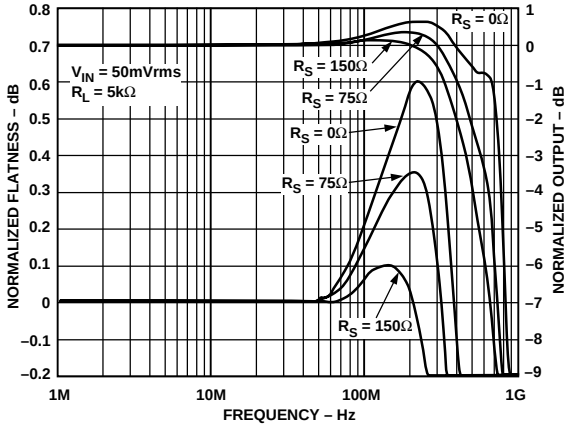


Figure 19. Frequency Response vs. Input Series Resistance

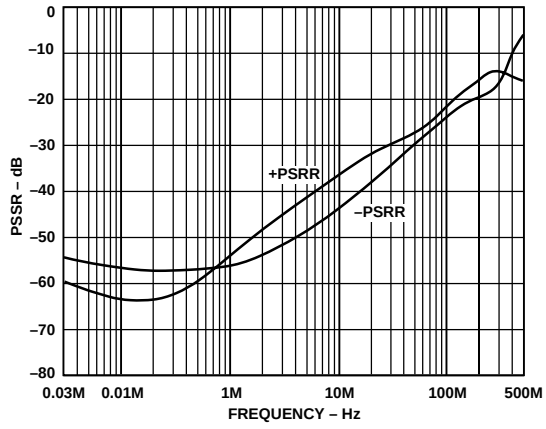


Figure 17. Power Supply Rejection vs. Frequency

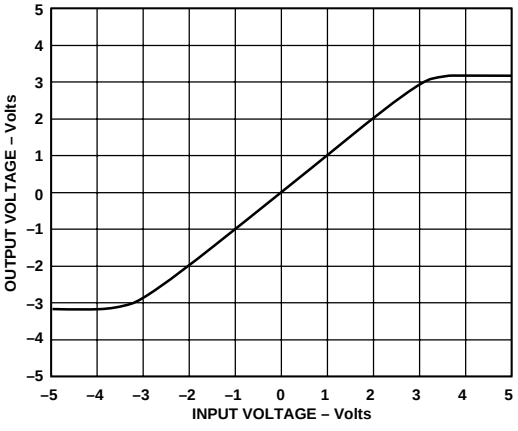


Figure 20. Output Voltage vs. Input Voltage, R_L = 2 kΩ

THEORY OF OPERATION

The AD8184 video multiplexer is designed for fast switching (10 ns) and wide bandwidth (> 700 MHz). This performance is attained with low power dissipation (4.4 mA, enabled) through the use of proprietary circuit techniques and a dielectrically-isolated complementary bipolar process. This device has a fast disable function that allows the outputs of several muxes to be wired in parallel to form a larger mux with little degradation in switching time. The low disabled output capacitance (3.2 pF) helps to preserve the system bandwidth in larger matrices. Unlike earlier CMOS switches, the switched open-loop buffer architecture of the AD8184 provides a unidirectional signal path with minimal switching glitches and constant, low input capacitance. Since the input impedance of these muxes is nearly independent of the load impedance and the state of the mux, the frequency response of the ON channels in a large switch matrix is not affected by fanout.

Figure 21 shows a block diagram and simplified schematic of the AD8184, which contains four switched buffers (S0–S3) that share a common output. The decoder logic translates TTL-compatible logic inputs (A0, A1 and $\overline{\text{ENABLE}}$) to internal, differential ECL levels for fast, low-glitch switching. The A0 (LSB) and A1 (MSB) control inputs constitute a two-bit binary word that determines which of the four buffers is enabled, unless the $\overline{\text{ENABLE}}$ input is HIGH, in which case all buffers are disabled and the output is switched to a high impedance state.

Each open-loop buffer is implemented as a complementary emitter follower that provides high input impedance, symmetric slew rate and load drive, and high output-to-input isolation due to its β^2 current gain. The selected buffer is biased ON by fast switched current sources that allow the buffer to turn on quickly. Dedicated flatness circuits, combined with the open-loop architecture of the AD8184, keep peaking low (typically < 0.5 dB) when driving high capacitive loads, without the need for external series resistors at the input or output. If better flatness response is desired, an input series resistance (R_S) may be used (refer to Figure 19), although this will increase crosstalk. The dc gain of the AD8184 is almost independent of load for R_L > 10 kΩ. For heavier loads, the dc gain is approximately that of the voltage divider formed by the output impedance of the mux (typically 28 Ω and R_L).

High speed disable clamp circuits (not shown) at the bases of Q3 and Q4 allow the buffers to turn off quickly and cleanly without dissipating much power once off. Moreover, these clamps shunt displacement currents flowing through the junction capacitances of Q1 and Q2 away from the bases of Q3 and Q4 and to ac ground through low impedances. The two-pole high-pass frequency response of the T switch formed by these clamps is a significant improvement over the one-pole high pass response of a simple series CMOS switch. As a result, board and package parasitics, especially stray capacitance between inputs and outputs, may limit the achievable crosstalk and off isolation.

LAYOUT CONSIDERATIONS:

Realizing the high speed performance attainable with the AD8184 requires careful attention to board layout and component selection. Proper RF design techniques and low parasitic component selection are mandatory.

Wire wrap boards, prototype boards and sockets are not recommended because of their high parasitic inductance and capacitance. Instead, surface-mount components should be directly soldered to a printed circuit board (PCB). The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance ground path. To reduce stray capacitance the ground plane should be removed from the area near input and output pins.

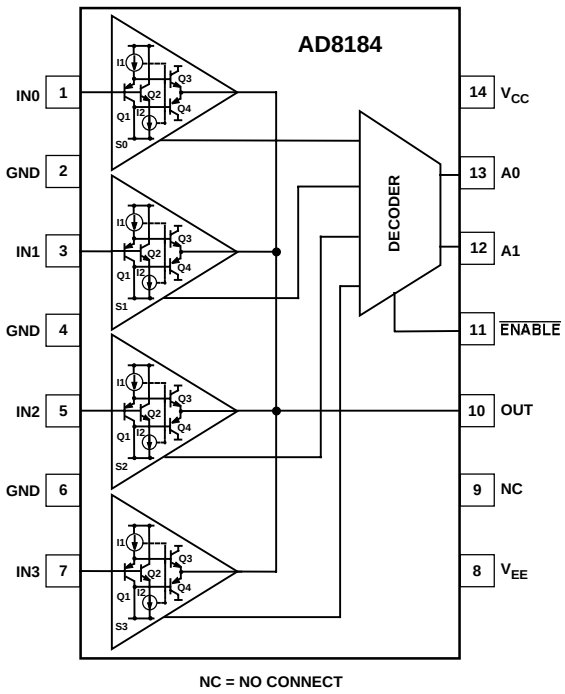


Figure 21. Block Diagram and Simplified Schematic of the AD8184 Multiplexer

Chip capacitors should be used for supply bypassing. One end of the capacitor should be connected to the ground plane and the other within 1/4 inch of each power pin. An additional large (4.7 µF–10 µF) tantalum capacitor should be connected in parallel with each of the smaller capacitors for low impedance supply bypassing over a broad range of frequencies.

Signal traces should be as short as possible. Stripline or microstrip techniques should be used for long (longer than about 1 inch) signal traces. These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end using surface mount components.

Careful layout is imperative to minimize crosstalk. Guards (ground or supply traces) must be run between all signal traces to limit direct capacitive coupling. Input and output signal lines should fan out away from the mux as much as possible. If multiple signal layers are available, a buried stripline structure having ground plane above, below and between signal traces will have the best crosstalk performance.

Return currents flowing through termination resistors can also increase crosstalk if these currents flow in sections of the finite-impedance ground circuit shared between more than one input or output. Minimizing the inductance and resistance of the ground plane can reduce this effect, but further care should be taken in positioning the terminations. Terminating cables directly at the connectors will minimize the return current flowing on the board, but the signal trace between the connector and the mux will look like an open stub and will degrade the frequency response. Moving the termination resistors close to the input pins will improve the frequency response, but the terminations from neighboring inputs should not have a common ground return.

APPLICATIONS

A Buffered 4-to-1 Multiplexer

In applications where the output of a multiplexer must drive a back-terminated 75 Ω line (R_L = 75 Ω + 75 Ω), it is necessary to buffer the output of the AD8184. In the example in Figure 22, this is accomplished using the AD8009 high speed current feedback op amp. The amplifier is configured with a gain of 2 to compensate for the signal halving due to termination at the multiplexer input. This gives the overall circuit a gain of unity.

If lower speed can be tolerated, a number of other amplifiers can replace the AD8009 op amp in the above circuit. In general there is a trade-off between bandwidth and power consumption. Table II summarizes the bandwidth and power consumption characteristics of these op amps.

Table II. Amplifier Options for Multiplexer Buffering

Op Amp	Comments
AD8009	Highest Bandwidth, (G = +2) = 700 MHz, I_{SY} = 14 mA
AD8001	Lower Power Consumption, Bandwidth (G = +2) = 440 MHz, I_{SY} = 5 mA
AD8011	Lower Power Consumption, Bandwidth (G = +2) = 210 MHz, I_{SY} = 1 mA
AD8079	Fixed Gain Dual Amplifier (2 or 2.2), Bandwidth = 260 MHz, I_{SY} = 5 mA Per Amp
AD8005	Lowest Power Consumption, Bandwidth (G = +2) = 170 MHz, I_{SY} = 400 µA

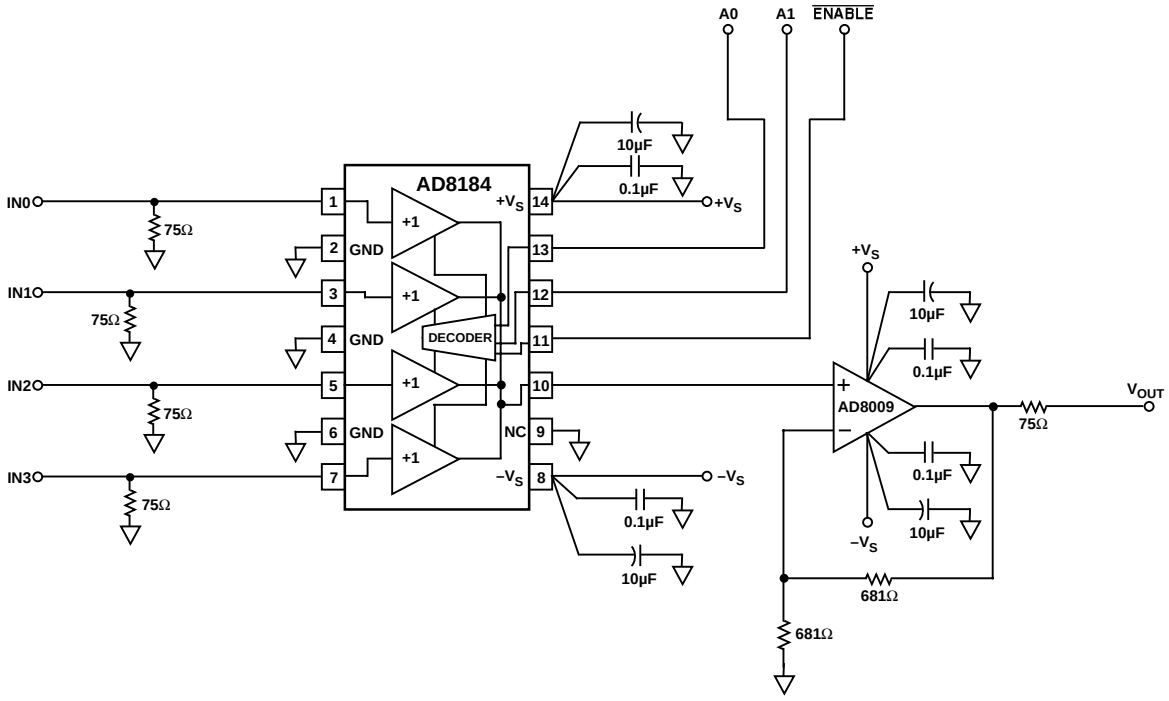


Figure 22. A Buffered 4-to-1 Multiplexer

Color Document Scanner

Figure 23 shows a block diagram of a Color Document Scanner. Charge Coupled Devices (CCDs) find widespread use in scanner applications. A monochrome CCD delivers a serial stream of voltages levels, each level being proportional to the light shining on that cell. In the case of the color image scanner shown, there are three output streams, representing red, green and blue. Interlaced with the stream of voltage levels is a voltage representing the reset level (or black level) of each cell. A Correlated Double Sampler (CDS) subtracts these two voltages from each other in order to eliminate the relatively large offsets common with CCDs.

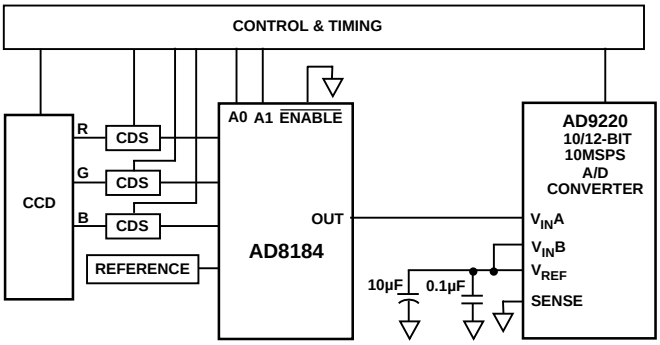


Figure 23. Color Document Scanner

The next step in the data acquisition process involves digitizing the three signal streams. Assuming that the analog-to-digital converter chosen has a fast enough sample rate, multiplexing the three streams into a single ADC is generally more economical than using one ADC per channel. In the example shown, we use the AD8184 as the multiplexer.

Because of its high bandwidth, the AD8184 is capable of driving the switched capacitor input stage of the AD9220 without additional buffering. In addition to having the required bandwidth, it is necessary to consider the settling time of the multiplexer. In this case, the ADC has a sample rate of 10 MHz, which corresponds to a sampling period of 100 ns. Typically, one phase of the sampling clock is used for conversion (i.e., all levels are held steady) and the other is used for switching and settling to the next channel. Assuming a 50% duty cycle, the signal chain must settle within 50 ns. With a settling time to 0.1% of 15 ns, the multiplexer easily satisfies this criterion.

In the example shown, the fourth (spare) channel of the AD8184 is used to measure a reference voltage. This voltage would probably be measured less frequently than the R, G and B signals. Multiplexing a reference voltage offers the advantage that any temperature drift effects caused by the multiplexer will equally impact the reference voltage and the to-be-measured signals. If the fourth channel is unused, it is good design practice to permanently tie it to ground.

A 4 × 4 Crosspoint Switch

While large crosspoint arrays are best constructed using highly integrated devices such as the AD8116, 16 × 16 crosspoint switch, smaller or irregular sized arrays can be constructed using 4-to-1 multiplexers such as the AD8184. The circuit below shows a 4 × 4 array, constructed using the AD8184 and buffered using the AD8079, a dual, fixed gain of 2 or 2.2, video amplifier.

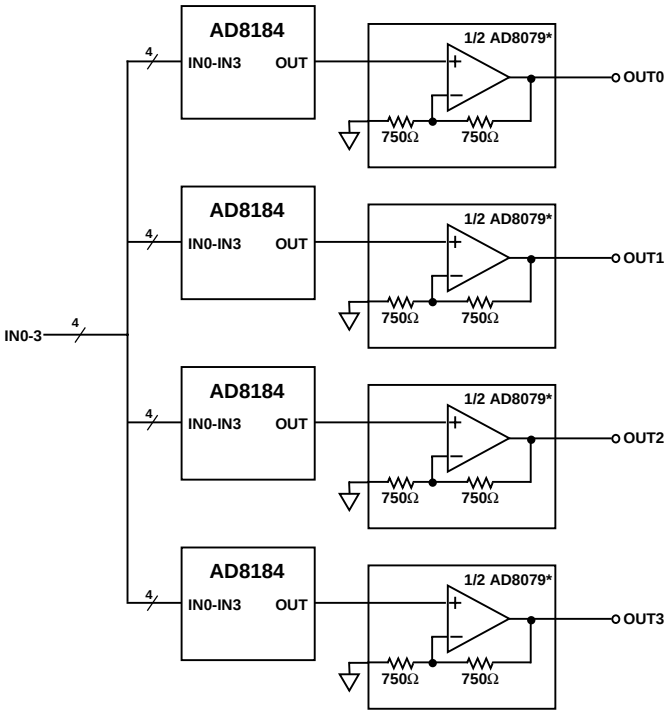


Figure 24. 4× 4 Crosspoint Switch

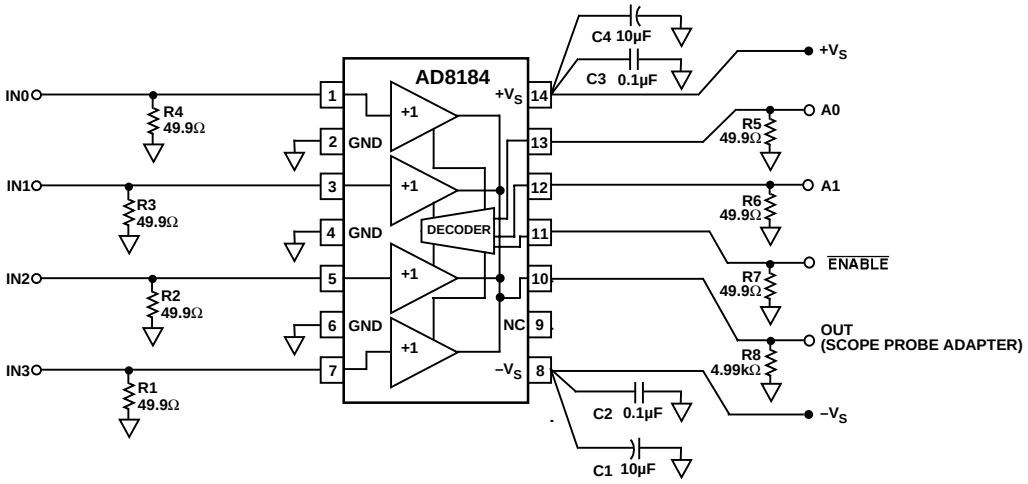


Figure 25. AD8184AR Evaluation Board

EVALUATION BOARD

An evaluation board is available for the AD8184. It has been carefully laid out and tested to demonstrate the specified high speed performance of the devices. Figure 25 shows the schematic of the evaluation board. For ordering information, please refer to the Ordering Guide.

Figure 26 shows the silkscreen of the component side and Figure 28 shows the silkscreen of the solder side. Figures 27 and 29 show the layout of the component side and solder side respectively.

The evaluation board is provided with 49.9 Ω termination resistors on all inputs. This is to allow the performance to be evaluated at very high frequencies where 50 Ω termination is most popular. To use the evaluation board in video applications, the termination resistors should be replaced with 75 Ω resistors.

The FR4 board type has the following stripline dimensions: 60-mil width, 12-mil gap between center conductor and outside ground plane “island” and 62-mil board thickness.

The multiplexer output is loaded with a 4.99 kΩ resistor. For connection to external instruments, an oscilloscope probe adapter is provided. This allows direct connection of an FET probe to the board. For verification of data sheet specifications, use of an FET probe is recommended because of its low input capacitance. The probe adapter used on the board has the same footprint as SMA, SMB and SMC type connectors, allowing easy replacement if necessary.

The side-launched SMA connectors on the analog and digital inputs can also be replaced by top-mount SMA, SMB or SMC type connectors. When using top-mount connectors, the stripline on the outside 1/8" of the board edge should be removed with an X-acto blade as this unused stripline acts as an open stub, which could degrade the small-signal frequency response of the multiplexer.

Input termination resistor placement on the evaluation board is critical to reducing crosstalk. Each termination resistor is oriented so that the ground return currents flow counterclockwise to the ground plane “island.” Although the direction of this ground current flow is arbitrary, it is important that no two input or output termination resistors share a connection to the same ground “island.”

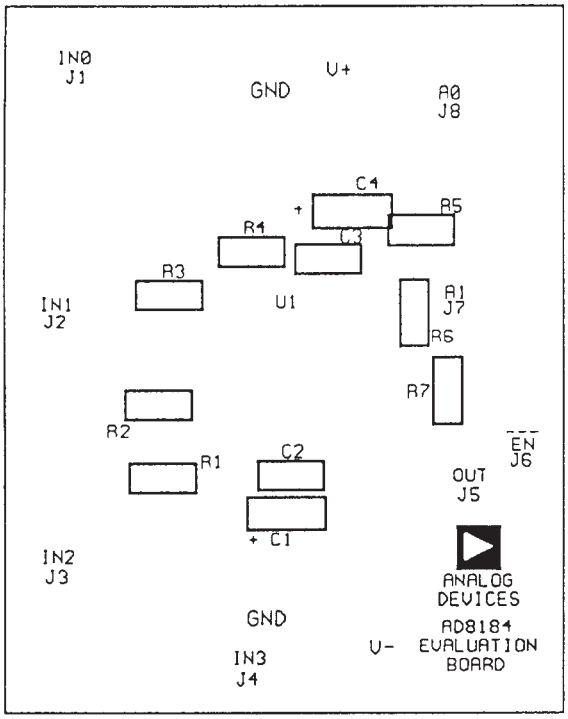


Figure 26. Component Side Silkscreen

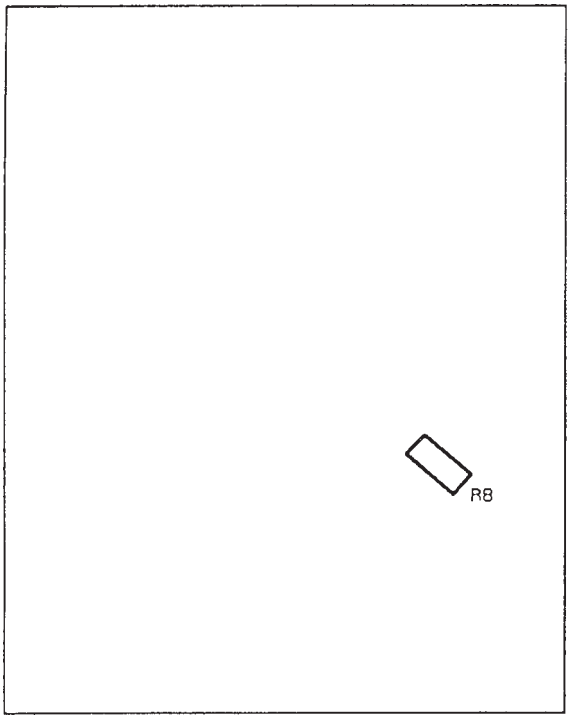


Figure 28. Solder Side Silkscreen

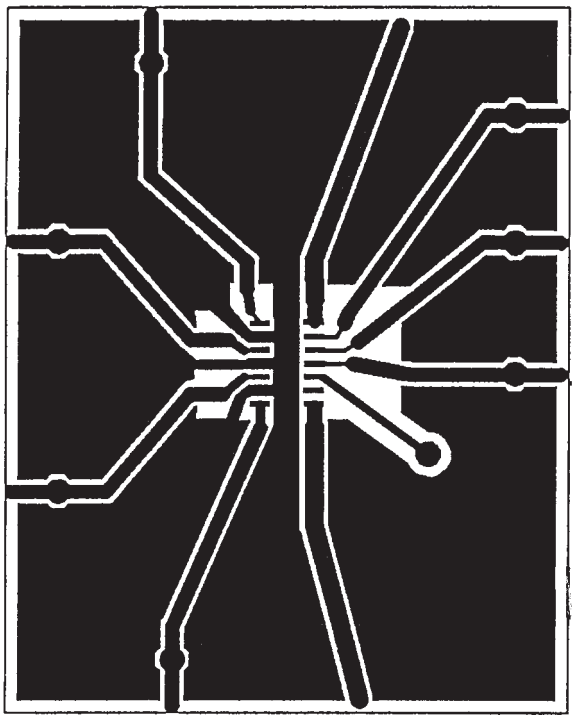


Figure 27. Board Layout (Component Side)

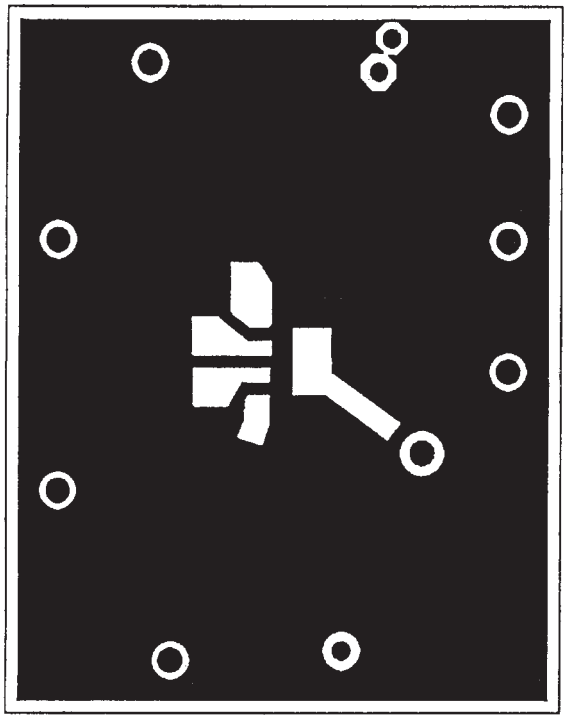
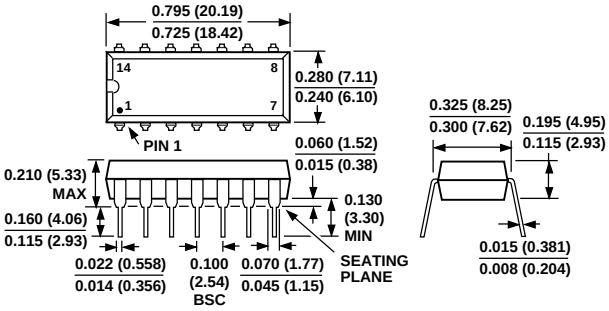


Figure 29. Board Layout (Solder Side)

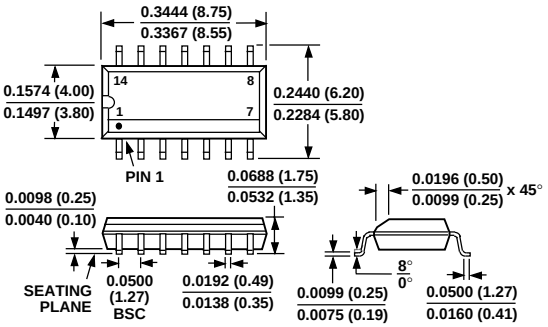
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead Plastic DIP
(N-14)



14-Lead SOIC
(R-14)



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