350 MHz Single-Supply (5 V) Triple 2:1 Multiplexers

AD8188/AD8189

FEATURES

- Fully buffered inputs and outputs
- Fast channel-to-channel switching: 4 ns
- Single-supply operation (5 V)
- High speed
  - 350 MHz bandwidth (−3 dB) @ 200 mV p-p
  - 300 MHz bandwidth (−3 dB) @ 2 V p-p
  - Slew rate: 1000 V/µs
- Fast settling time: 7 ns to 0.1%
- Low current: 19 mA/20 mA
- Excellent video specifications: load resistor (R_L) = 150 Ω
- Differential gain error: 0.05%
- Differential phase error: 0.05°
- Low glitch
- All hostile crosstalk
  - −84 dB @ 5 MHz
  - −52 dB @ 100 MHz
- High off isolation: −95 dB @ 5 MHz
- Low cost
- Fast, high impedance disable feature for connecting multiple outputs
- Logic-shifted outputs

APPLICATIONS

- Switching RGB in LCD and plasma displays
- RGB video switchers and routers

FUNCTIONAL BLOCK DIAGRAM

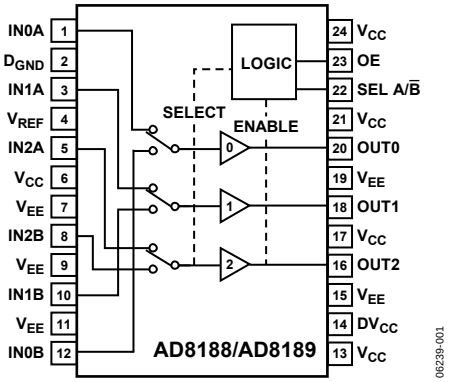

Figure 1.

GENERAL DESCRIPTION

The AD8188 (G = 1) and AD8189 (G = 2) are high speed, single-supply, triple 2-to-1 multiplexers. They offer −3 dB small signal bandwidth of 350 MHz and −3 dB large signal bandwidth of 300 MHz, along with a slew rate in excess of 1000 V/µs. With −84 dB of all hostile crosstalk and −95 dB off isolation, the parts are well suited for many high speed applications. The differential gain and differential phase error of 0.05% and 0.05° respectively, along with 0.1 dB flatness to 70 MHz, make the AD8188 and AD8189 ideal for professional and component video multiplexing. The parts offer 4 ns switching time, making them an excellent choice for switching video signals, while consuming less than 20 mA on a single 5 V supply (100 mW). Both devices have a high speed disable feature that sets the outputs into a high impedance state. This allows the building of larger input arrays while minimizing off-channel output loading. The devices are offered in a 24-lead TSSOP.

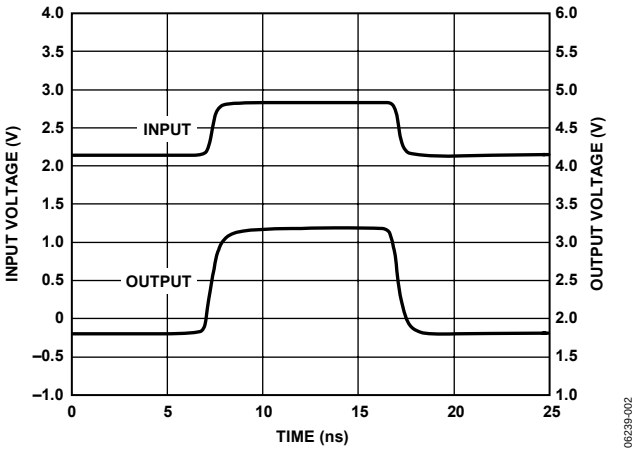

Figure 2. AD8189 Video Amplitude Pulse Response, V_{OUT} = 1.4 V p-p, R_L = 150 Ω

Rev. 0

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REVISION HISTORY

10/06—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C. For the AD8188, V_S = 5 V, R_L = 1 kΩ to 2.5 V. For the AD8189, V_S = 5 V, V_{REF} = 2.5 V, R_L = 150 Ω to 2.5 V; unless otherwise noted.

Table 1.

		AD8188/AD8189			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE					
−3 dB Bandwidth (Small Signal)	V_{OUT} = 200 mV p-p		350		MHz
−3 dB Bandwidth (Large Signal)	V_{OUT} = 2 V p-p		300		MHz
0.1 dB Flatness	V_{OUT} = 200 mV p-p		70		MHz
Slew Rate (10% to 90% Rise Time)	V_{OUT} = 2 V p-p, R_L = 150 Ω		1000		V/µs
Settling Time to 0.1%	V_{IN} = 1 V Step, R_L = 150 Ω		6/7.5		ns
NOISE/DISTORTION PERFORMANCE					
Differential Gain	3.58 MHz, R_L = 150 Ω		0.05		%
Differential Phase	3.58 MHz, R_L = 150 Ω		0.05		Degrees
All Hostile Crosstalk	5 MHz		−84/−78		dB
	100 MHz		−52/−48		dB
Channel-to-Channel Crosstalk, RTI	5 MHz		−90/−85		dB
Off Isolation	5 MHz		−84/−95		dB
Input Voltage Noise	f = 100 kHz to 100 MHz		7/9		nV/√Hz
DC PERFORMANCE					
Voltage Gain Error	No load		0.1	±0.3/±0.6	%
Voltage Gain Error Matching	Channel A to Channel B		0.04	±0.2/±0.2	%
V_{REF} Gain Error	1 kΩ load		0.04	±0.6	%
Input Offset Voltage			0.2/0.5	±6.5/±7.0	mV
	T_{MIN} to T_{MAX}		±8.0		mV
Input Offset Voltage Matching	Channel A to Channel B		0.2	±5.0/±5.5	mV
Input Offset Drift			10/5		µV/°C
Input Bias Current			1.5	4/4	µA
V_{REF} Bias Current (AD8189 Only)			1.0		µA
INPUT CHARACTERISTICS					
Input Resistance	@ 100 kHz		1.8/1.3		MΩ
Input Capacitance			0.9/1.0		pF
Input Voltage Range (About Midsupply)	IN0A, IN0B, IN1A, IN1B, IN2A, IN2B		±1.2		V
	V_{REF}		+0.9/−1.2		V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 1 kΩ	3.1/2.8	3.2/3.0		V p-p
	R_L = 150 Ω	2.8/2.5	3.0/2.7		V p-p
Short-Circuit Current			85		mA
Output Resistance	Enabled @ 100 kHz		0.2/0.35		Ω
	Disabled @ 100 kHz		1000/600		kΩ
Output Capacitance	Disabled		1.5/2.0		pF
POWER SUPPLY					
Operating Range		3.5		5.5	V
Power Supply Rejection Ratio	+PSRR, V_{CC} = 4.5 V to 5.5 V, V_{EE} = 0 V		−72/−61		dB
	−PSRR, V_{EE} = −0.5 V to +0.5 V, V_{CC} = 5.0 V		−76/−72		dB
Quiescent Current	All channels on		18.5/19.5	21.5/22.5	mA
	All channels off		3.5/4.5	4.5/5.5	mA
	T_{MIN} to T_{MAX}, all channels on	15		23	mA
SWITCHING CHARACTERISTICS					
Channel-to-Channel Switching Time	50% logic to 50% output settling, INxA = +1 V, INxB = −1 V		3.6/4		ns
Enable-to-Channel On Time	50% logic to 50% output settling, input = 1 V		4/3.8		ns

Parameter	Conditions	AD8188/AD8189 Min	Typ	Max	Unit
Disable-to-Channel Off Time	50% logic to 50% output settling, input = 1 V		17/5		ns
Channel Switching Transient (Glitch)	All channels grounded		21/45		mV
Output Enable Transient (Glitch)	All channels grounded		64/118		mV
DIGITAL INPUTS					
Logic 1 Voltage	SEL A/$\overline{B}$, OE	1.6			V
Logic 0 Voltage	SEL A/$\overline{B}$, OE			0.6	V
Logic 1 Input Current	SEL A/$\overline{B}$, OE = 2.0 V		45		nA
Logic 0 Input Current	SEL A/$\overline{B}$, OE = 0.5 V		2		µA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter[1]	Rating
Supply Voltage	5.5 V
DV_{CC} to D_{GND}	5.5 V
DV_{CC} to V_{EE}	8.0 V
V_{CC} to D_{GND}	8.0 V
IN0A, IN0B, IN1A, IN1B, IN2A, IN2B, V_{REF}	$V_{EE} \le V_{IN} \le V_{CC}$
SEL A/$\overline{B}$, OE	$D_{GND} \le V_{IN} \le V_{CC}$
Output Short-Circuit Operation	Indefinite
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering, 10 sec)	300°C

[1] Specification is for device in free air (T_A = 25°C).

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}[2]	θ_{JC}	Unit
24-Lead TSSOP[1]	85	20	°C/W

[1] Maximum internal power dissipation (PD) should be derated for ambient temperature (T_A) such that PD < (150°C T_A)/θ_{JA}.
[2] θ_{JA} is on a 4-layer board (2s 2p).

MAXIMUM POWER DISSIPATION

The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8188/AD8189 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figure 3.

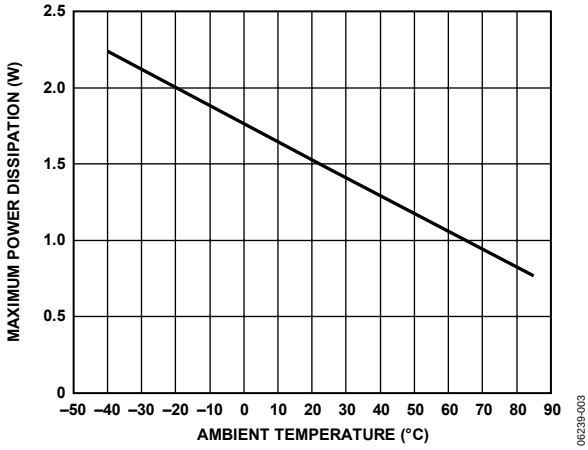

Figure 3. Maximum Power Dissipation vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

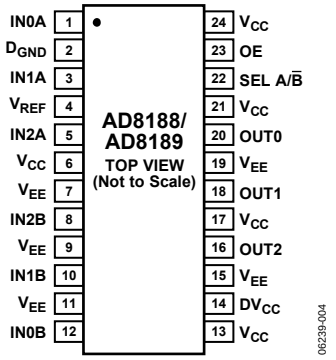

Figure 4. AD8188/AD8189 Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN0A	Input, High-Z_{IN}. Routed to OUT0 when A is selected.
2	D_{GND}	Ground Reference for Digital Control Circuitry.
3	IN1A	Input, High-Z_{IN}. Routed to OUT1 when A is selected.
4	V_{REF}	AD8188: Bypass point for internal reference. Does not affect dc level of output. AD8189: Input to reference buffers for all channels. Can be used to offset the outputs.
5	IN2A	Input, High-Z_{IN}. Routed to OUT2 when A is selected.
6, 13, 17, 21, 24	V_{CC}	Positive Analog Supply. Nominally 5 V higher than V_{EE}.
7, 9, 11, 15, 19	V_{EE}	Negative Analog Supply.
8	IN2B	Input, High-Z_{IN}. Routed to OUT2 when B is selected.
10	IN1B	Input, High-Z_{IN}. Routed to OUT1 when B is selected.
12	IN0B	Input, High-Z_{IN}. Routed to OUT0 when B is selected.
14	DV_{CC}	Positive Supply for Digital Control Circuitry. Referenced to D_{GND}.
16	OUT2	Output. Can connect to IN2A, IN2B, or disable.
18	OUT1	Output. Can connect to IN1A, IN1B, or disable.
20	OUT0	Output. Can connect to IN0A, IN0B, or disable.
22	SEL A/$\overline{B}$	Logic high selects the three A inputs. Logic low selects the three B inputs.
23	OE	Output Enable. Logic high enables the three outputs.

Table 5. Truth Table

SEL A/$\overline{B}$	OE	OUT
0	0	High-Z
1	0	High-Z
1	1	INxA
0	1	INxB

TYPICAL PERFORMANCE CHARACTERISTICS

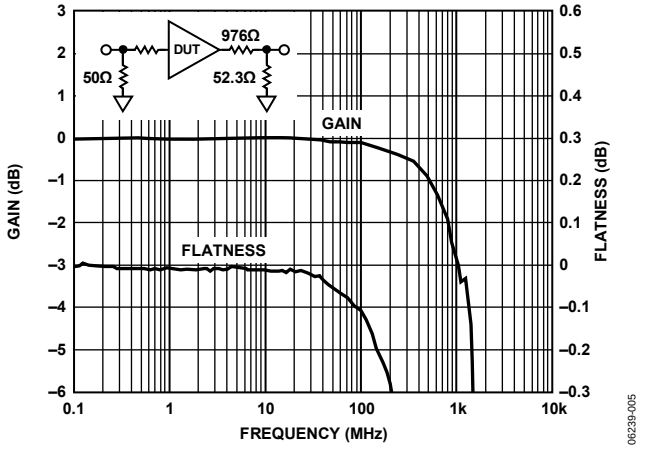

Figure 5. AD8188 Frequency Response, V_{OUT} = 200 mV p-p, R_L = 1 kΩ

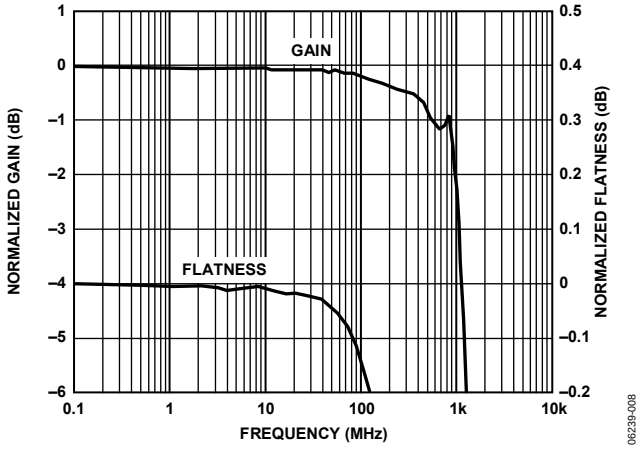

Figure 8. AD8189 Frequency Response, V_{OUT} = 200 mV p-p, R_L = 150 Ω

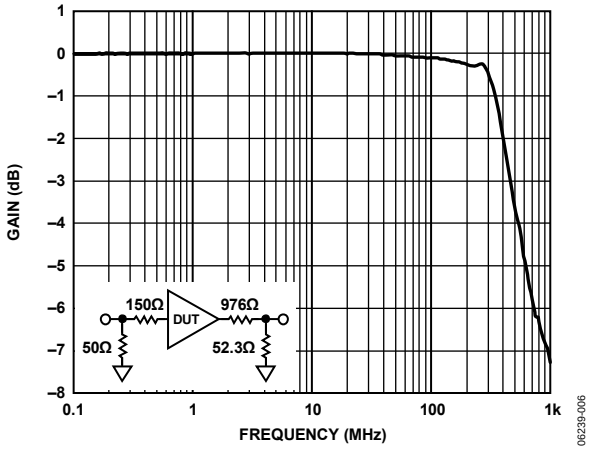

Figure 6. AD8188 Frequency Response, V_{OUT} = 2 V p-p, R_L = 1 kΩ

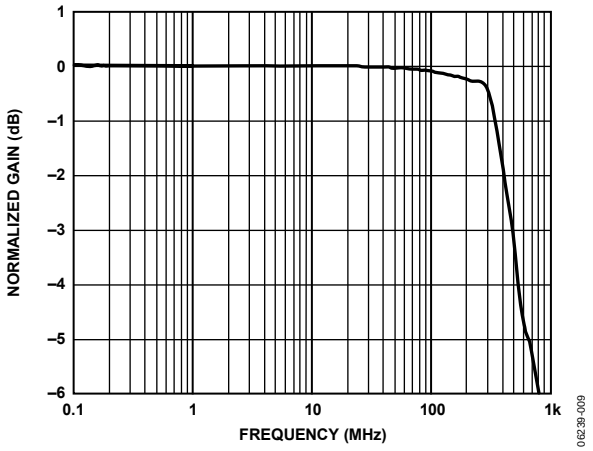

Figure 9. AD8189 Frequency Response, V_{OUT} = 2 V p-p, R_L = 150 Ω

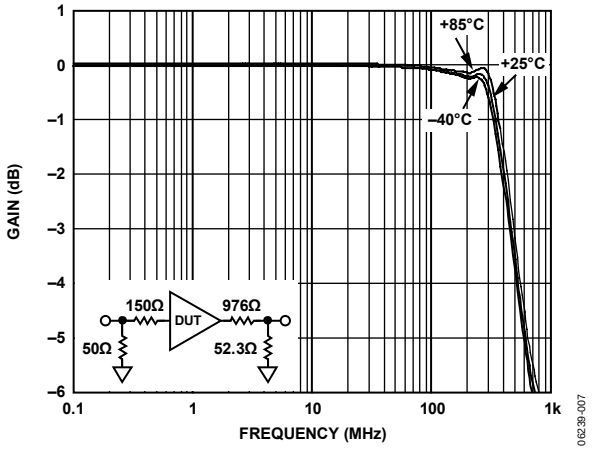

Figure 7. AD8188 Large Signal Bandwidth vs. Temperature, V_{OUT} = 2 V p-p, R_L = 1 kΩ

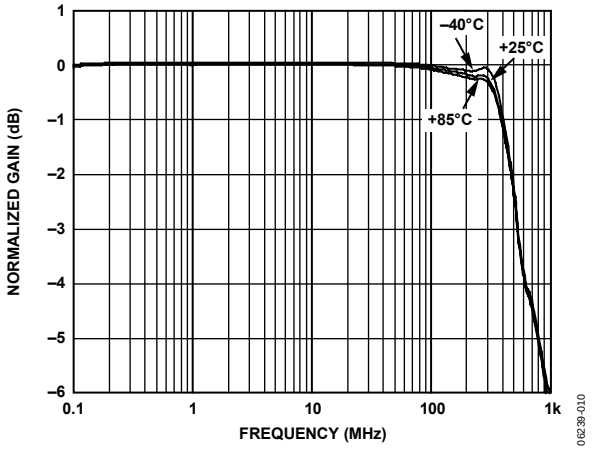

Figure 10. AD8189 Large Signal Bandwidth vs. Temperature, V_{OUT} = 2 V p-p, R_L = 150 Ω

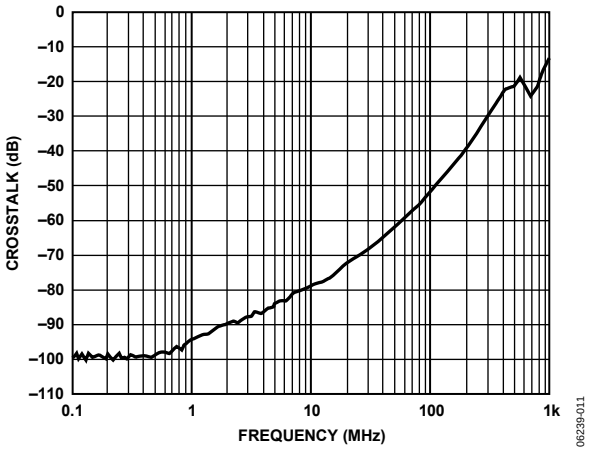

Figure 11. AD8188 All Hostile Crosstalk vs. Frequency (Drive All INxA, Listen to Output with INxB Selected)

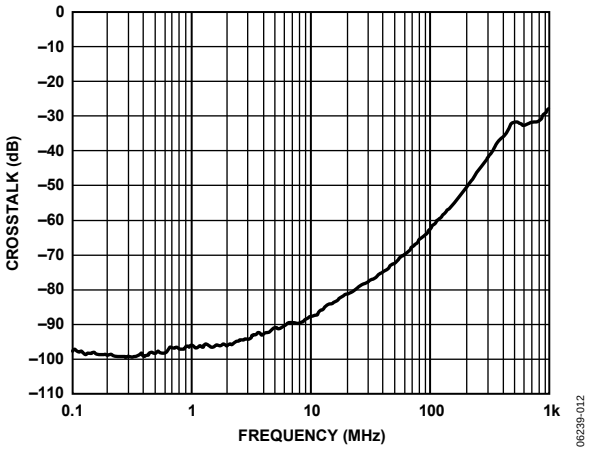

Figure 12. AD8188 Adjacent Channel Crosstalk vs. Frequency (Drive One INxA, Listen to an Adjacent Output with INxB Selected)

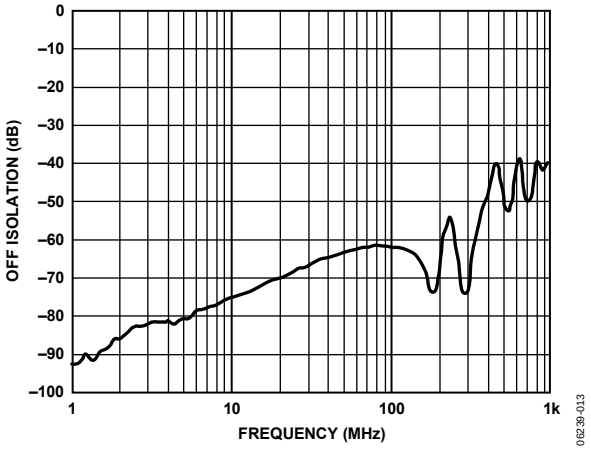

Figure 13. AD8188 Off Isolation vs. Frequency (Drive Inputs with OE Tied Low)

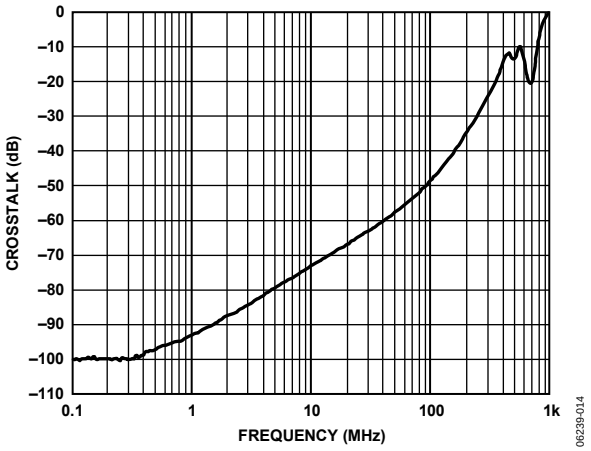

Figure 14. AD8189 All Hostile Crosstalk vs. Frequency (Drive All INxA, Listen to Output with INxB Selected)

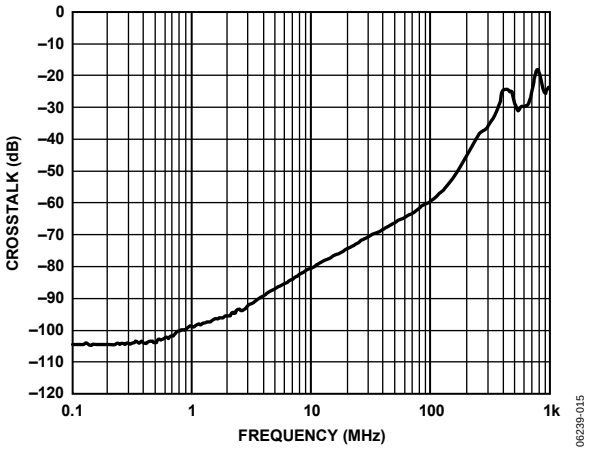

Figure 15. AD8189 Adjacent Channel Crosstalk vs. Frequency (Drive One INxA, Listen to an Adjacent Output with INxB Selected)

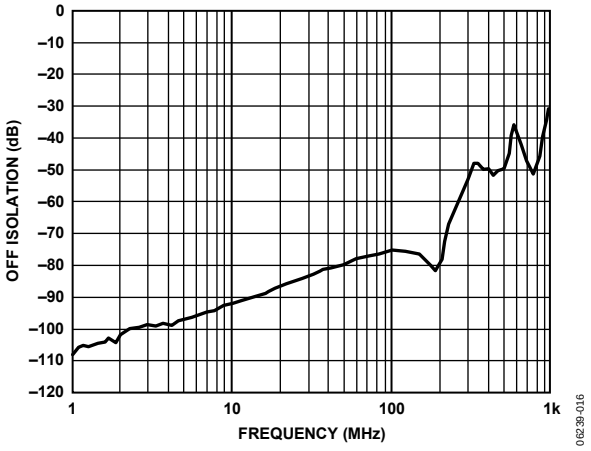

Figure 16. AD8189 Off Isolation vs. Frequency (Drive Inputs with OE Tied Low)

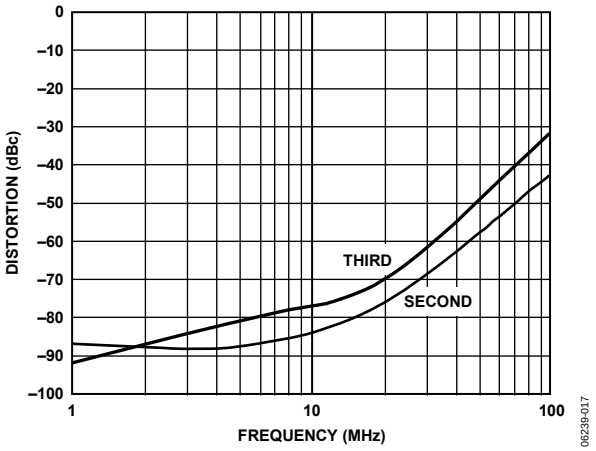

Figure 17. AD8188 THD vs. Frequency, V_{OUT} = 2 V p-p, R_L = 150 Ω

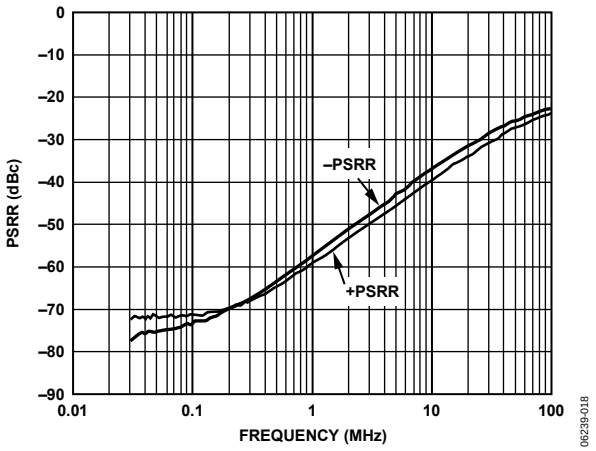

Figure 18. AD8188 PSRR vs. Frequency, R_L = 150 Ω

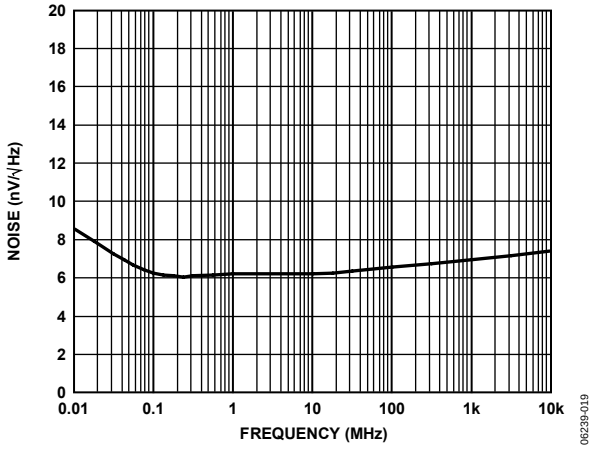

Figure 19. AD8188 Input Voltage Noise vs. Frequency

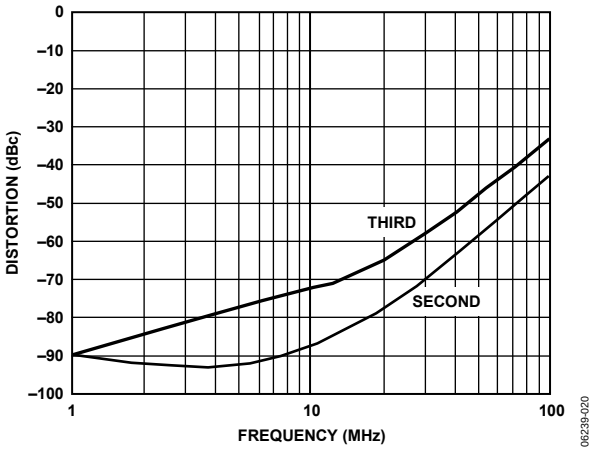

Figure 20. AD8189 THD vs. Frequency, V_{OUT} = 2 V p-p, R_L = 150 Ω

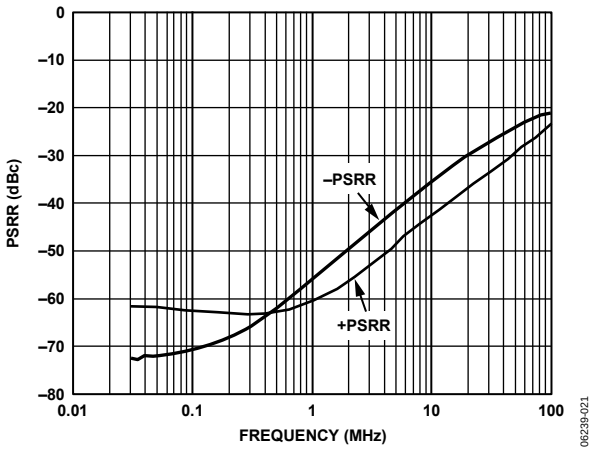

Figure 21. AD8189 PSRR vs. Frequency, R_L = 150 Ω

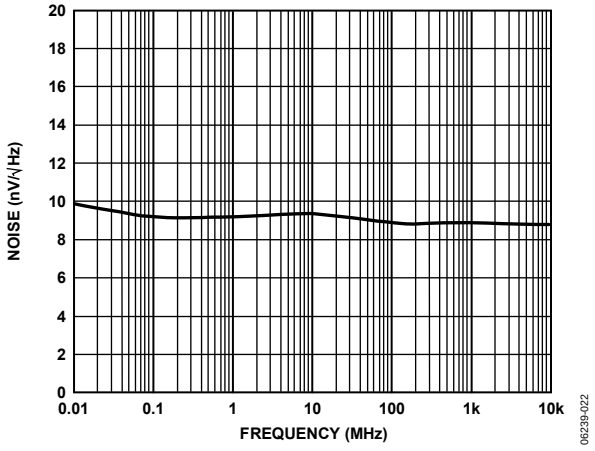

Figure 22. AD8189 Input Voltage Noise vs. Frequency

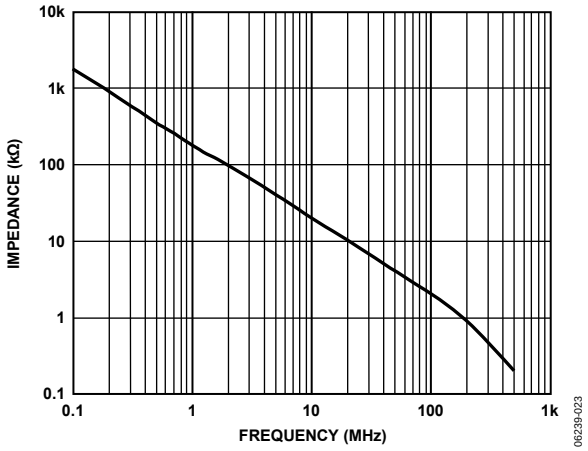

Figure 23. AD8188 Input Impedance vs. Frequency

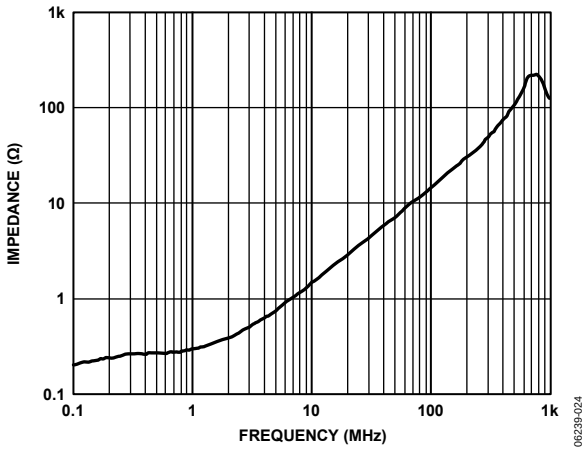

Figure 24. AD8188 Enabled Output Impedance vs. Frequency

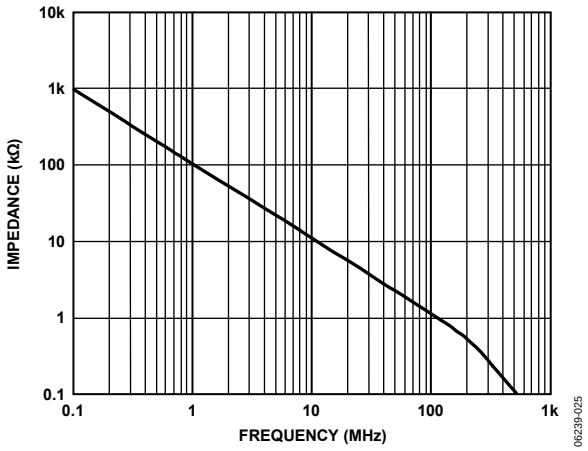

Figure 25. AD8188 Disabled Output Impedance vs. Frequency

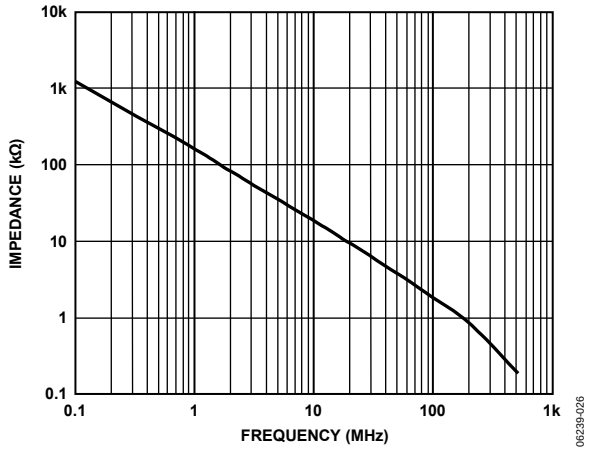

Figure 26. AD8189 Input Impedance vs. Frequency

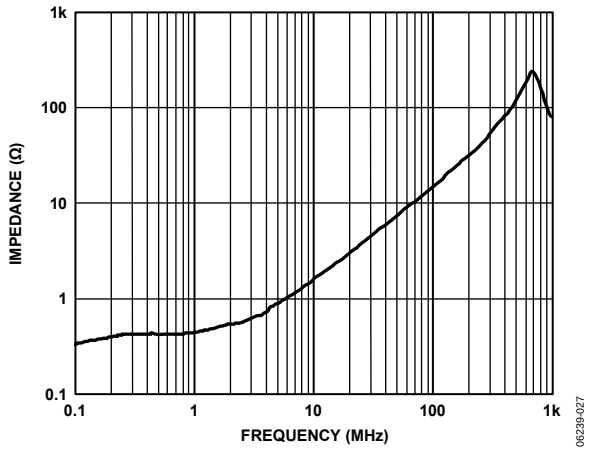

Figure 27. AD8189 Enabled Output Impedance vs. Frequency

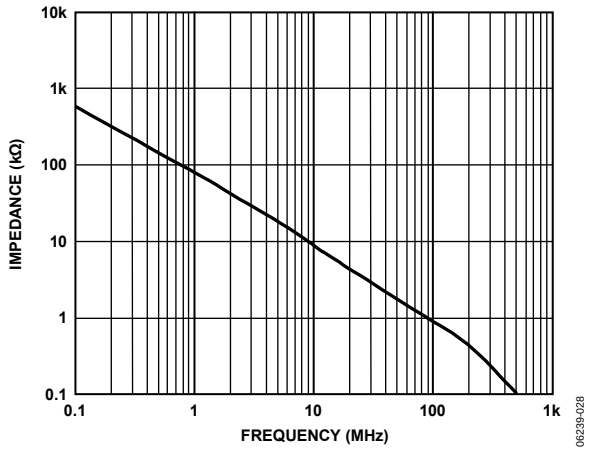

Figure 28. AD8189 Disabled Output Impedance vs. Frequency

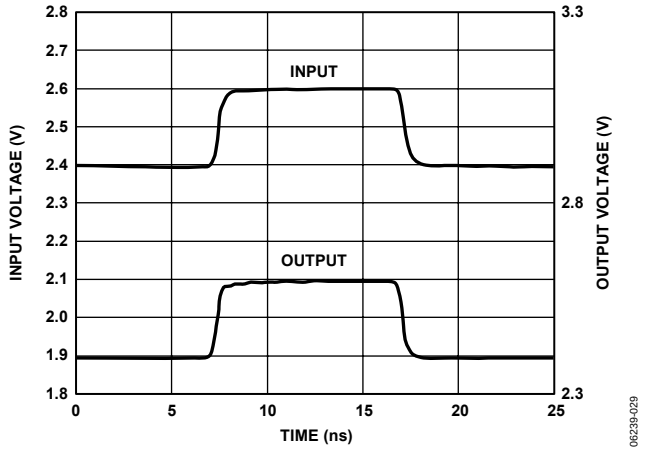

Figure 29. AD8188 Small Signal Pulse Response, V_{OUT} = 200 mV p-p, R_L = 1 kΩ

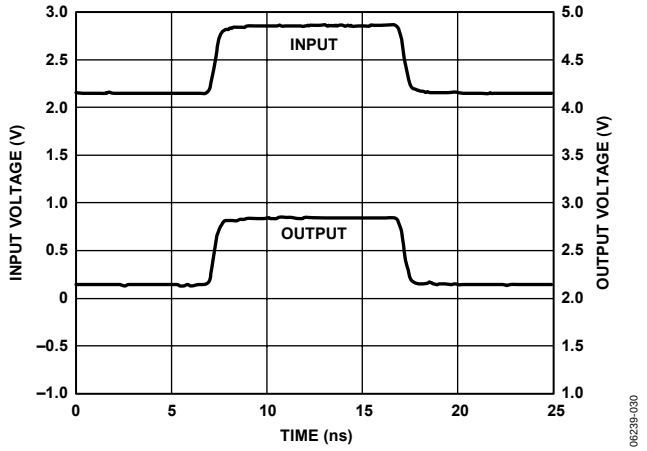

Figure 30. AD8188 Video Amplitude Pulse Response, V_{OUT} = 700 mV p-p, R_L = 1 kΩ

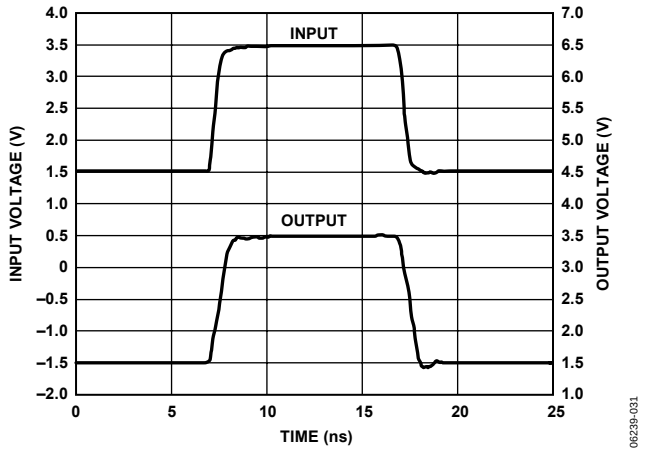

Figure 31. AD8188 Large Signal Pulse Response, V_{OUT} = 2 V p-p, R_L = 1 kΩ

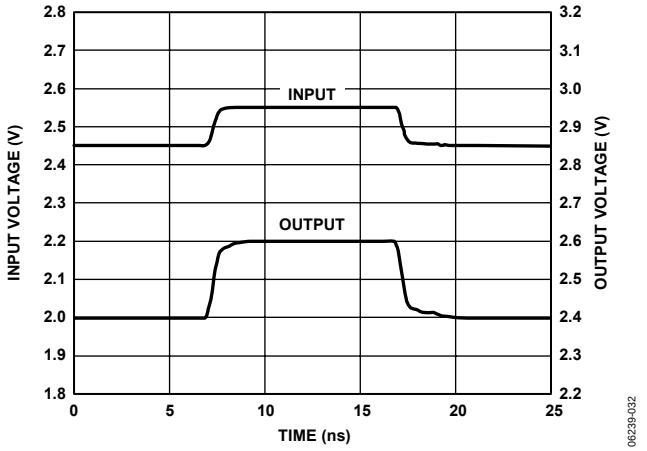

Figure 32. AD8189 Small Signal Pulse Response, V_{OUT} = 200 mV p-p, R_L = 150 kΩ

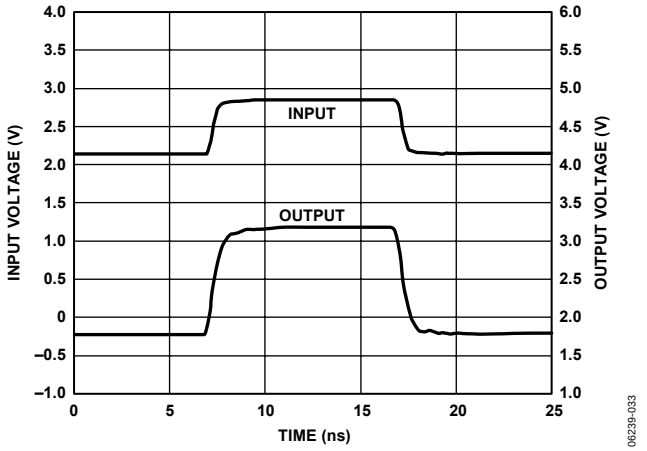

Figure 33. AD8189 Video Amplitude Pulse Response, V_{OUT} = 1.4 V p-p, R_L = 150 kΩ

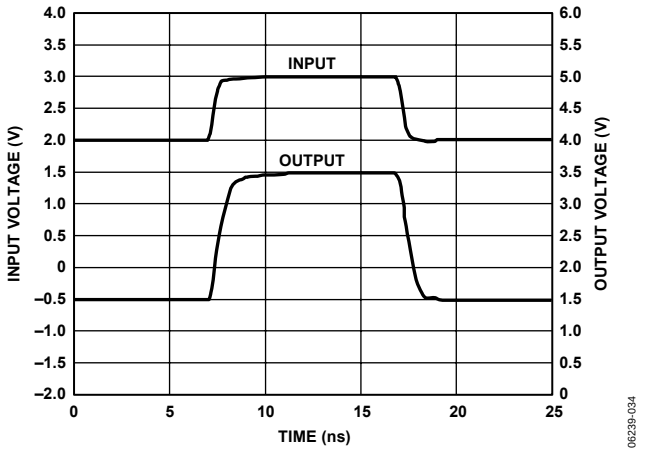

Figure 34. AD8189 Large Signal Pulse Response, V_{OUT} = 2 V p-p, R_L = 150 kΩ

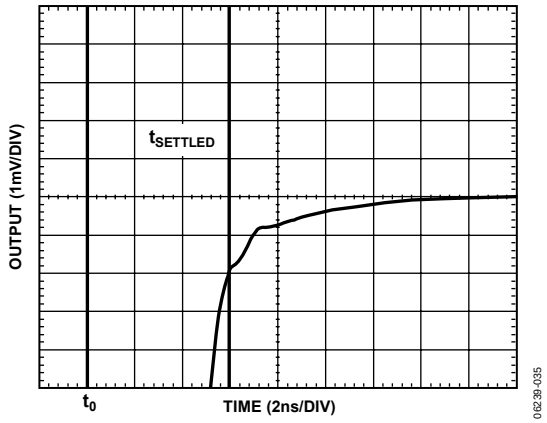

Figure 35. AD8188 Settling Time (0.1%), V_{OUT} = 2 V Step, R_L = 1 kΩ

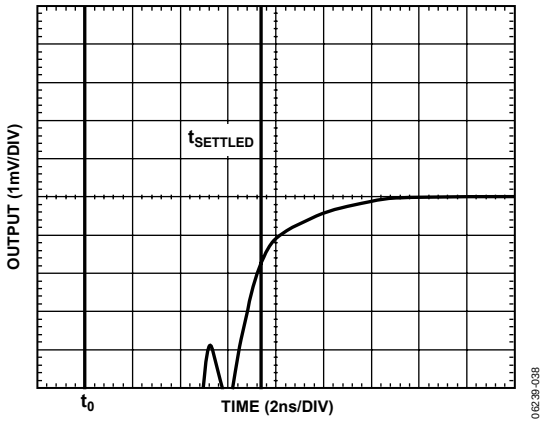

Figure 38. AD8189 Settling Time (0.1%), V_{OUT} = 2 V Step, R_L = 150 Ω

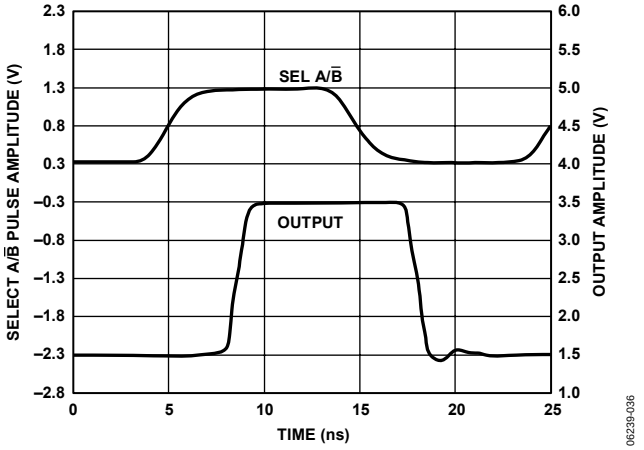

Figure 36. AD8188 Channel-to-Channel Switching Time, V_{OUT} = 2 V p-p, INxA = 3.5 V, INxB = 1.5 V

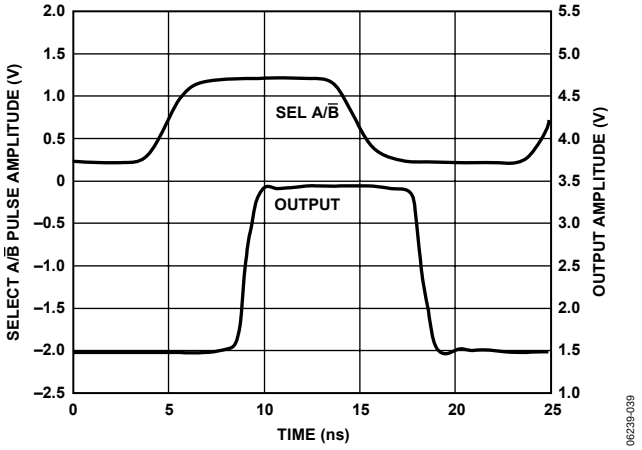

Figure 39. AD8189 Channel-to-Channel Switching Time, V_{OUT} = 2 V p-p, INxA = 3.0 V, INxB = 2.0 V

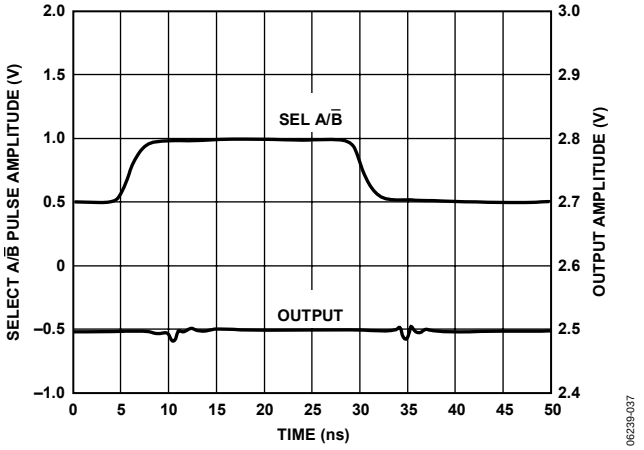

Figure 37. AD8188 Channel Switching Transient (Glitch), INxA = INxB = 0 V

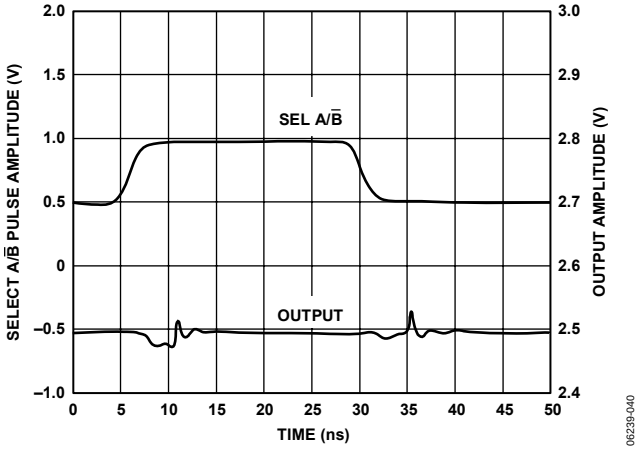

Figure 40. AD8189 Channel Switching Transient (Glitch), INxA = INxB = V_{REF} = 0 V

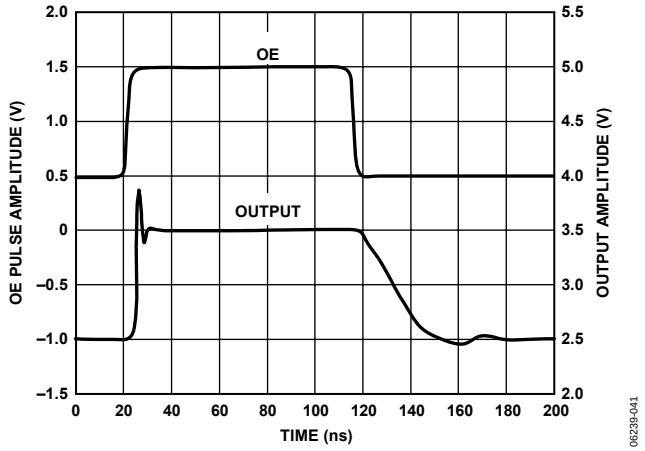

Figure 41. AD8188 Enable On/Off Time, V_{OUT} = 0 V to 1 V

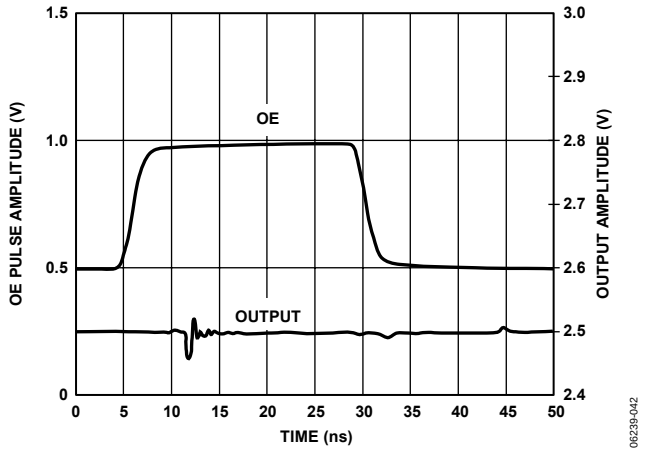

Figure 42. AD8188 Channel Enable/Disable Transient (Glitch)

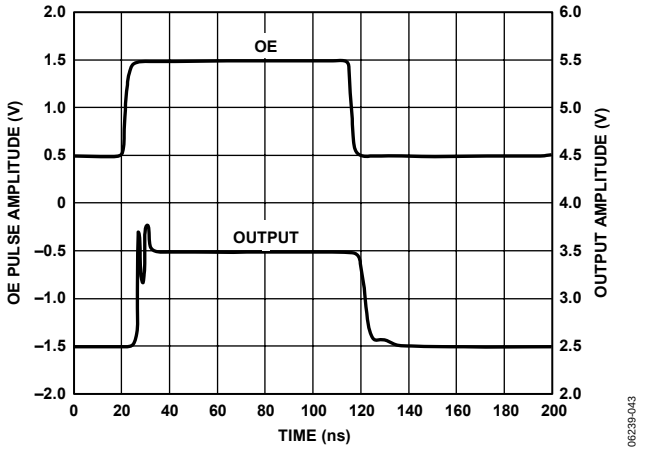

Figure 43. AD8189 Enable On/Off Time, V_{OUT} = 0 V to 1 V

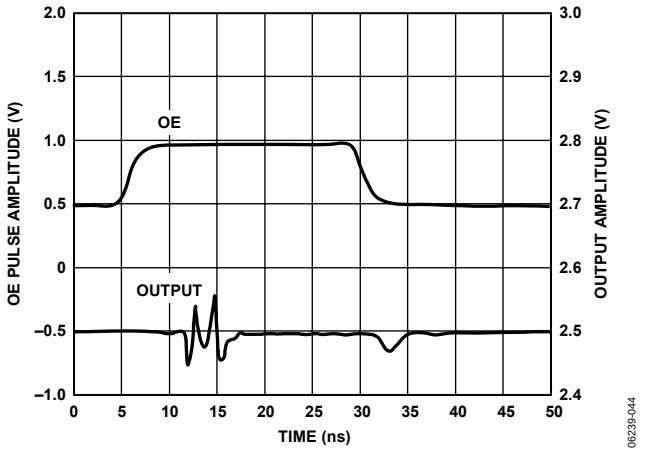

Figure 44. AD8189 Channel Enable/Disable Transient (Glitch)

THEORY OF OPERATION

The AD8188 (G = 1) and AD8189 (G = 2) are single-supply, triple 2:1 multiplexers with TTL-compatible global input switching and output-enable control. Optimized for selecting between two RGB (red, green, blue) video sources, the devices have high peak slew rates, maintaining their bandwidth for large signals. Additionally, the multiplexers are compensated for high phase margin, minimizing overshoot for good pixel resolution. The multiplexers also have respectable video specifications and are superior for switching NTSC or PAL composite signals.

The multiplexers are organized as three independent channels, each with two input transconductance stages and one output transimpedance stage. The appropriate input transconductance stages are selected via one logic pin (SEL A/$\overline{B}$) such that all three outputs simultaneously switch input connections. The unused input stages are disabled with a proprietary clamp circuit to provide excellent crosstalk isolation between on and off inputs while protecting the disabled devices from damaging reverse base-emitter voltage stress. No additional input buffering is necessary, resulting in low input capacitance and high input impedance without additional signal degradation.

The transconductance stage is a high slew rate, class AB circuit that sources signal current into a high impedance node. Each output stage contains a compensation network and is buffered to the output by a complementary emitter-follower stage. Voltage feedback sets the gain with the AD8188 configured as a unity gain follower, and the AD8189 configured as a gain-of-two amplifier with a feedback network. This architecture provides drive for a reverse-terminated video load (150 Ω) with low differential gain and phase errors, while consuming relatively little power. Careful chip layout and biasing result in excellent crosstalk isolation between channels.

HIGH IMPEDANCE DISABLE

The output-enable logic pin (OE) of the AD8188 and AD8189 controls whether the three outputs are enabled or disabled to a high impedance state. The high impedance disable allows larger matrices to be built by busing the outputs together.

In the case of the AD8189 (G = 2), the reference buffers also disable to a state of high output impedance. This feature prevents the feedback network of a disabled channel from loading the output, which is valuable when busing together the outputs of several muxes.

OFF ISOLATION

The off isolation performance of the signal path is dependent upon the value of the load resistor, R_L. For calculating off isolation, the signal path can be modeled as a simple high-pass network with an effective capacitance of 3 fF. Off isolation improves as the load resistance is decreased. In the case of the AD8188, off isolation is specified with a 1 kΩ load. However, a practical application would likely gang the outputs of multiple muxes. In this case, the proper load resistance for the off isolation calculation is the output impedance of an enabled AD8188, typically less than a 1/10 Ω.

FULL POWER BANDWIDTH VS. –3 dB LARGE SIGNAL BANDWIDTH

Note that full power bandwidth for an undistorted sinusoidal signal is often calculated using the peak slew rate from the equation

$$Full\ Power\ Bandwidth = \frac{Peak\ Slew\ Rate}{2\pi \times Sinusoid\ Amplitude}$$

The peak slew rate is not the same as the average slew rate. The average slew rate is typically specified as the ratio

$$\frac{\Delta V_{OUT}}{\Delta t}$$

measured between the 20% and 80% output levels of a sufficiently large output pulse. For a natural response, the peak slew rate can be 2.7 times larger than the average slew rate. Therefore, calculating a full power bandwidth with a specified average slew rate gives a pessimistic result. See the Specifications section for the large-signal bandwidth and average slew rate for both the AD8188 and AD8189 (large signal bandwidth is defined as the −3 dB point measured on a 2 V p-p output sine wave). Figure 17 and Figure 20 contain plots for the second- and third-order harmonic distortion. Specifying these three aspects of the signal path's large signal dynamics allows the user to predict system behavior for either pulse or sinusoid waveforms.

SINGLE-SUPPLY CONSIDERATIONS

The AD8188 and AD8189 offer superior large signal dynamics. The trade-off is that the input and output compliance is limited to ~1.3 V from either rail when driving a 150 Ω load. The following sections address some challenges of designing video systems within a single 5 V supply.

The AD8188

The AD8188 is internally wired as a unity-gain follower. Its inputs and outputs can both swing to within ~1.3 V of either rail. This affords the user 2.4 V of dynamic range at input and output that should be enough for most video signals, whether the inputs are ac- or dc-coupled. In both cases, the choice of output termination voltage determines the quiescent load current.

For improved supply rejection, the V_{REF} pin should be tied to an ac ground (the more quiet the supply, the better). Internally, the V_{REF} pin connects to one terminal of an on-chip capacitor. The capacitor's other terminal connects to an internal node. The consequence of building this bypass capacitor on-chip is twofold. First, the V_{REF} pin on the AD8188 draws no input bias current. (Contrast this to the case of the AD8189, where the V_{REF} pin typically draws 2 μA of input bias current.) Second, on the AD8188, the V_{REF} pin can be tied to any voltage within the supply range.

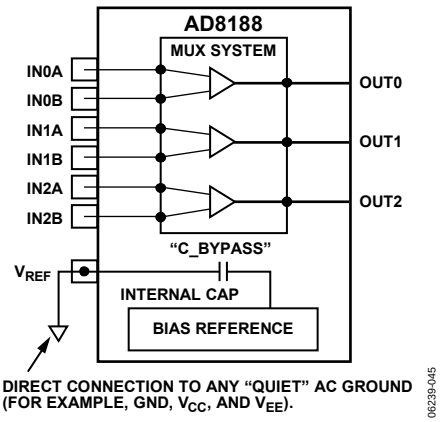

Figure 45. V_{REF} Pin Connection for AD8188 (Differs from AD8189)

The AD8189

The AD8189 uses on-chip feedback resistors to realize the gain-of-two function. To provide low crosstalk and a high output impedance when disabled, each set of 500 Ω feedback resistors is terminated by a dedicated reference buffer. A reference buffer is a high speed op amp configured as a unity-gain follower. The three reference buffers, one for each channel, share a single, high impedance input, the V_{REF} pin (see Figure 46). V_{REF} input bias current is typically less than 2 μA.

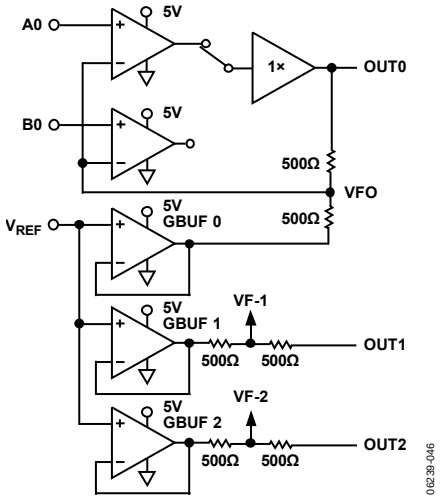

Figure 46. Conceptual Diagram of a Single Multiplexer Channel, G = 2

This configuration has a few implications for single-supply operation:

- On the AD8189, V_{REF} cannot be tied to the most negative analog supply, V_{EE}. The limits on reference voltage are (see Figure 47):

  V_{EE} + 1.3 V < V_{REF} × V_{CC} − 1.6 V

  1.3 V < V_{REF}, 3.4 V on 0 V/5 V supplies

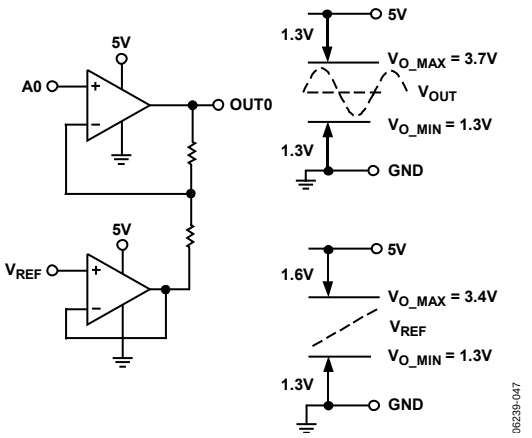

Figure 47. Output Compliance of Main Amplifier Channel and Ground Buffer

- The signal at the V_{REF} pin appears at each output. Therefore, V_{REF} should be tied to a well bypassed, low impedance source. Using superposition, it is shown that

  $V_{OUT} = 2 \times V_{IN} - V_{REF}$

- To maximize the output dynamic range, the reference voltage should be chosen with care. For example, consider amplifying a 700 mV video signal with a sync pulse 300 mV below black level. If the user decides to set V_{REF} at black level to preferentially run video signals on the faster NPN transistor path, the AD8189 allows a reference voltage as low as 1.3 V + 300 mV = 1.6 V. If the AD8189 is used, the sync pulse is amplified to 600 mV. Therefore, the lower limit on V_{REF} becomes 1.3 V + 600 mV = 1.9 V. For routing RGB video, an advantageous configuration is to employ +3 V and −2 V supplies, in which case V_{REF} can be tied to ground.

If system considerations prevent running the multiplexer on split supplies, a false ground reference should be employed. A low impedance reference can be synthesized with a second operational amplifier. Alternately, a well bypassed resistor divider can be used. Refer to the Applications section for further explanation and more examples.

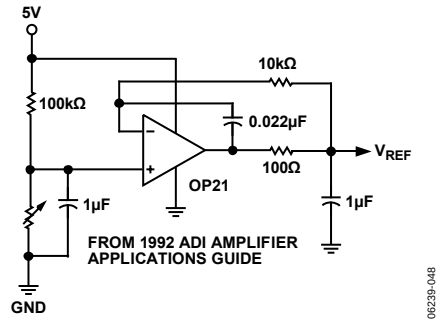

Figure 48. Synthesis of a False Ground Reference

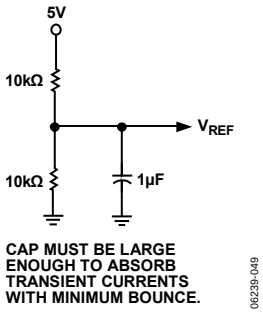

Figure 49. Alternate Method for Synthesis of a False Ground Reference

AC-COUPLED INPUTS

Using ac-coupled inputs presents an interesting challenge for video systems operating from a single 5 V supply. In NTSC and PAL video systems, 700 mV is the approximate difference between the maximum signal voltage and black level. It is assumed that sync has been stripped. However, given the two pathological cases shown in Figure 50, a dynamic range of twice the maximum signal swing is required if the inputs are to be ac-coupled. A possible solution is to use a dc restore circuit before the mux.

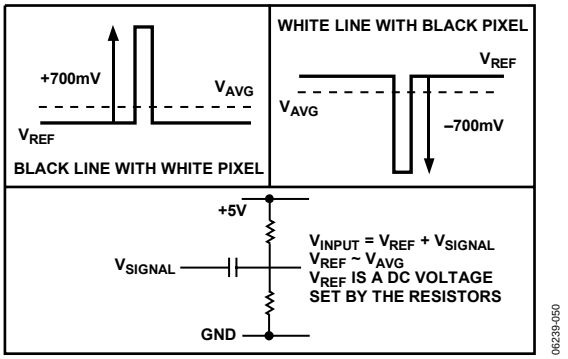

Figure 50. Pathological Case for Input Dynamic Range

TOLERANCE TO CAPACITIVE LOAD

Op amps are sensitive to reactive loads. A capacitive load at the output appears in parallel with an effective resistance (R_{EFF}) of

$$R_{EFF} = (R_L \parallel r_O)$$

where R_L is the discrete resistive load, and r_O is the open loop output impedance, approximately 15 Ω for these muxes.

The load pole (f_{LOAD}) at

$$f_{LOAD} = \frac{1}{2\pi R_{EFF} C_L}$$

can seriously degrade phase margin and, therefore, stability. The old workaround is to place a small series resistor directly at the output to isolate the load pole. While effective, this ruse also affects the dc and termination characteristics of a 75 Ω system. The AD8188 and AD8189 are built with a variable compensation scheme that senses the output reactance and trades bandwidth for phase margin, ensuring faster settling and lower overshoot at higher capacitive loads.

SECONDARY SUPPLIES AND SUPPLY BYPASSING

The high current output transistors are given their own supply pins (Pin 15, Pin 17, Pin 19, and Pin 21) to reduce supply noise on-chip and to improve output isolation. Because these secondary, high current supply pins are not connected on-chip to the primary analog supplies, V_{CC}/V_{EE} (Pin 6, Pin 7, Pin 9, Pin 11, Pin 13, and Pin 24), some care should be taken to ensure that the supply bypass capacitors are connected to the correct pins. At a minimum, the primary supplies should be bypassed. Pin 6 and Pin 7 can be a convenient place to accomplish this. Stacked power and ground planes are a convenient way to bypass the high current supply pins (see Figure 51).

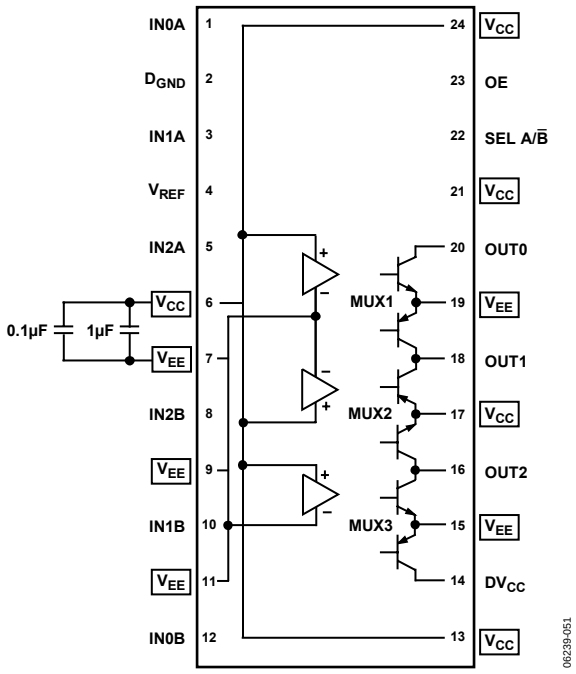

Figure 51. Detail of Primary and Secondary Supplies

SPLIT-SUPPLY OPERATION

Operating from split supplies (for example, [+3 V/−2 V] or ±2.5 V) simplifies the selection of the V_{REF} voltage and load resistor termination voltage. In this case, it is convenient to tie V_{REF} to ground. The logic inputs are internally level-shifted to allow the digital supplies and logic inputs to operate from 0 V and 5 V when powering the analog circuits from split supplies. The maximum voltage difference between DV_{CC} and V_{EE} must not exceed 8 V (see Figure 52).

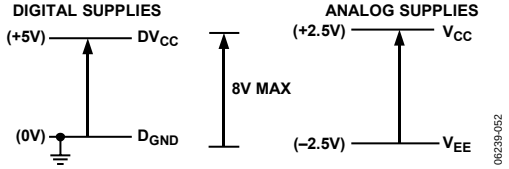

Figure 52. Split-Supply Operation

APPLICATIONS

SINGLE-SUPPLY OPERATION

The AD8188/AD8189 are targeted mainly for use in single-supply 5 V systems. For operating on these supplies, both V_{EE} and D_{GND} should be tied to ground, and the control logic pins should be referenced to ground. Normally, the DV_{CC} supply needs to be set to the same positive supply as the driving logic.

For dc-coupled, single-supply operation, it is necessary to set an appropriate input dc level that is within the specified range of the amplifier. For the unity-gain AD8188, the output dc level is the same as the input, while for the gain-of-two AD8189, the V_{REF} input can be biased to obtain an appropriate output dc level.

Figure 53 shows a circuit that provides a gain-of-two and is dc-coupled. The video input signals must have a dc bias from their source of approximately 1.5 V. This same voltage is applied to V_{REF} of the AD8189. The result is that when the video signal is at 1.5 V, the output is also at the same voltage. This is close to the lower dynamic range of both the input and the output.

When the input goes most positive, which is 700 mV above the black level for a standard video signal, it reaches a value of 2.2 V, and there is enough headroom for the signal. On the output side, the magnitude of the signal changes by 1.4 V, making the maximum output voltage 2.2 V + 1.4 V = 3.6 V. This is just within the dynamic range of the output of the part.

AC-COUPLING

AD8188

When a video signal is ac-coupled, the amount of dynamic range required to handle the signal can potentially be double the amount required for dc-coupled operation. For the unity-gain AD8188, there is still enough dynamic range to handle an ac-coupled, standard video signal with 700 mV p-p amplitude. If the input is biased at 2.5 V dc, the input signal can potentially go 700 mV both above and below this point. The resulting 1.8 V and 2.2 V are within the input signal range for single 5 V operation. Because the part is unity-gain, the outputs follow the inputs, and there is adequate range at the output as well.

When the AD8188 is operated from a single supply of 5 V and ground, ac-coupling is often useful. This is particularly true when the input signals are a typical RGB source from a PC. These signals go all the way to ground at the most negative, outside of the AD8188 input range, when its negative supply is ground. The closest that the input can go to ground is typically 1.3 V.

There are several basic methods for ac-coupling the inputs. They all consist of a series capacitor followed by a circuit for setting the dc operating point of the input and then the AD8188 input. If a termination is provided, it should be located before the series coupling capacitor.

The different circuits vary in the means used to establish the dc operating point after the coupling capacitor. A straightforward way to do this is to use a voltage divider for each input. However, because there are six inputs altogether, 12 resistors are required to set all of the dc operating points. This means many components in a small space, but the circuit has the advantage of having the lowest crosstalk among any of the inputs. This circuit is shown in Figure 54.

A circuit that uses the minimum number of resistors can be designed. First, create a node, V_{MID}, which serves as the bias voltage for all of the inputs. Then, a single resistor is used to connect from each input (inside the ac-coupling capacitor) and V_{MID} (see Figure 55).

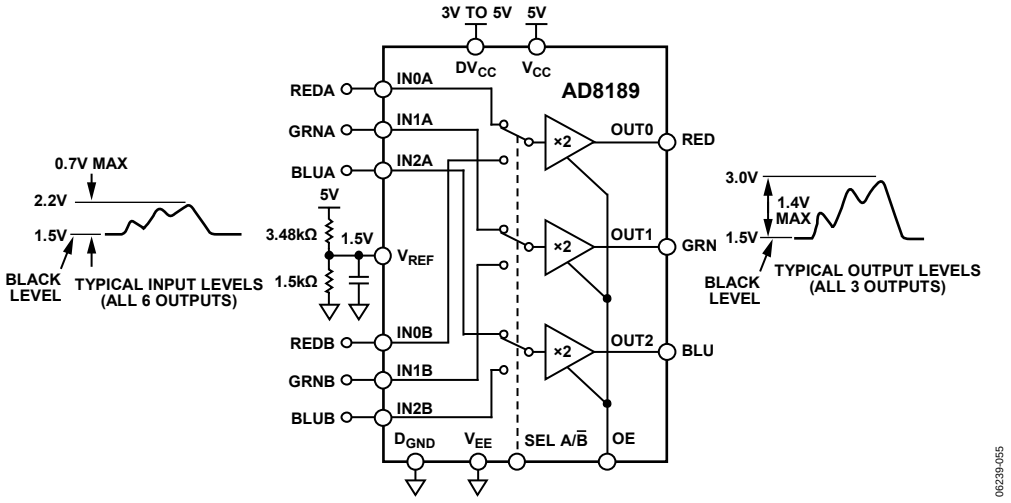

Figure 53. AD8189 DC-Coupled (Bypassing and Logic Not Shown)

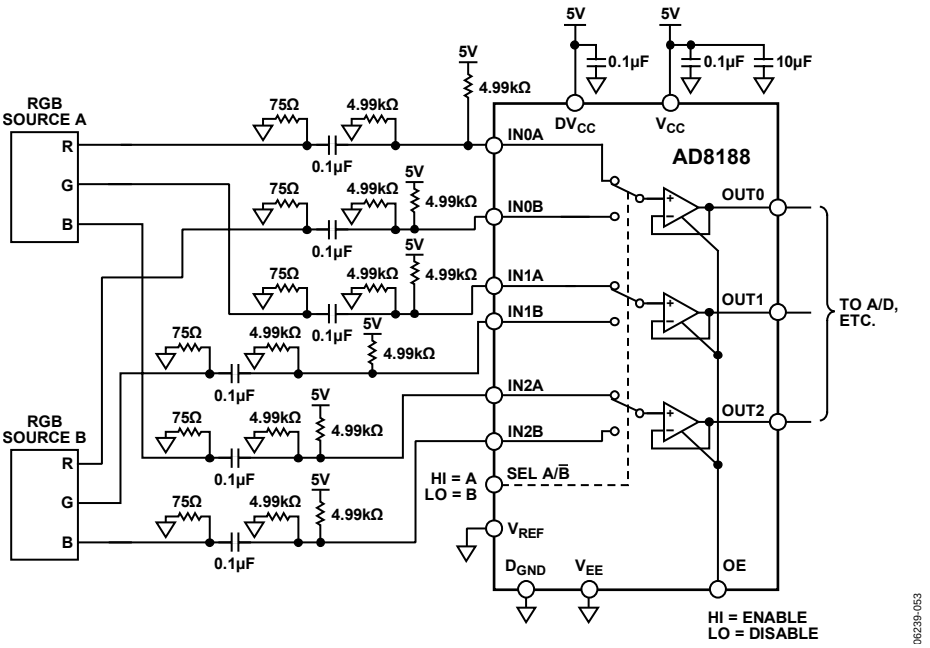

Figure 54. AD8188 AC-Coupling Using Separate Voltage Dividers

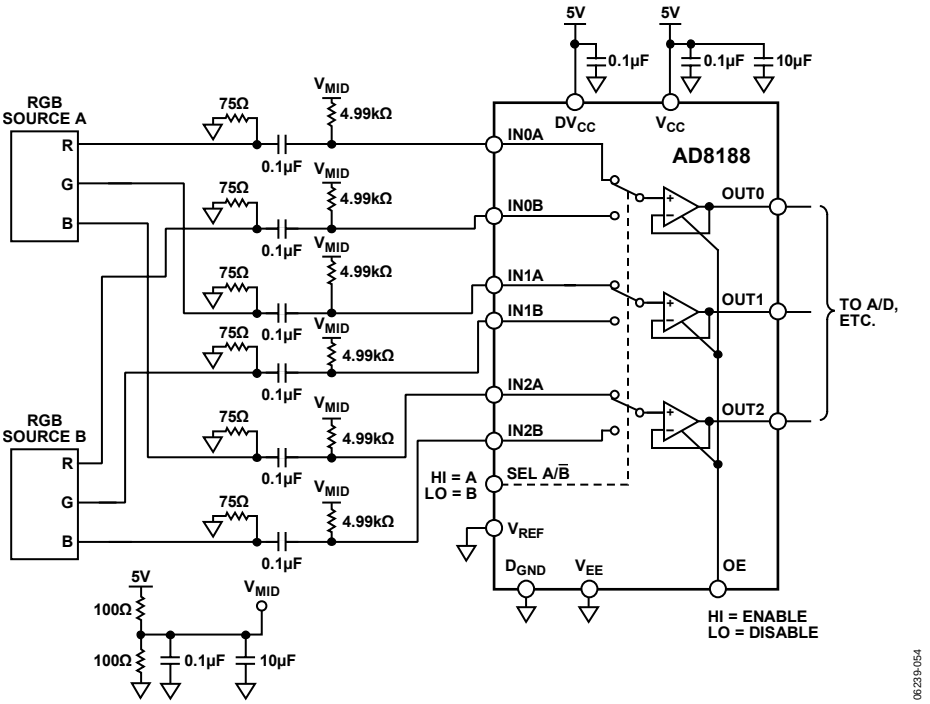

Figure 55. AD8188 AC-Coupling Using a Single V_{MID} Reference

The circuit in Figure 55 can increase the crosstalk between inputs, because each input signal creates a small signal on V_{MID} due to its nonzero impedance. There are several means to minimize this. First, make the impedance of the V_{MID} divider small. Small resistor values lower the dc resistance, and good bypassing to ground minimizes the ac impedance. It is also possible to use a voltage regulator or another system supply voltage if it is the correct value. It should be close to the mid-supply voltage of the AD8188.

The second technique for minimizing crosstalk is to use large resistor values to connect from the inputs to V_{MID}. The major factor limiting the value of these resistors is offset caused by the input bias current (I_B) that must flow through these resistors to the AD8188 inputs. The typical I_B for an AD8188 input is 1.5 µA, which causes an offset voltage of 1.5 mV per 1 kΩ of resistance.

These two techniques can also be combined. Typically, crosstalk between the RGB signals from the same source is less objectionable than crosstalk between two different sources. The former can cause a color or luminance shift, but spatially, everything is coherent. However, the crosstalk signals from two uncorrelated sources can create ghost images that are far more objectionable.

A technique for minimizing crosstalk between two different sources is to create two separate V_{MID} circuits. Then, the inputs from each source can be connected to their own V_{MID} node, minimizing crosstalk between sources.

AD8189

When using the gain-of-two AD8189 in a simple ac-coupled application, there is a dynamic range limitation at the output caused by its higher gain. At the output, the gain-of-two produces a signal swing of 1.4 V, but the ac-coupling doubles this required amount to 2.8 V. The AD8189 outputs can only swing from 1.4 V to 3.6 V on a 5 V supply, so there are only 2.2 V of dynamic signal swing available at the output.

A standard means for reducing the dynamic range requirements of an ac-coupled video signal is to use a dc restore. This circuit works to limit the dynamic range requirements by clamping the black level of the video signal to a fixed level at the input to the amplifier. This prevents the video content of the signal from varying the black level, as happens in a simple ac-coupled circuit.

DC RESTORE

After ac-coupling a video signal, it is necessary to use a dc restore to establish where the black level is. Usually, this appears at the end of a video signal chain. This dc restore circuit needs to have the required accuracy for the system. It compensates for all the offsets of the preceding stages. Therefore, if a dc restore circuit is to be used only for dynamic range limiting, it does not require great dc accuracy.

A dc restore circuit using the AD8189 is shown in Figure 56. Two separate sources of RGB video are ac-coupled to the 0.1 µF input capacitors of the AD8189. The input points of the AD8189 are switched to a 1.5 V reference by the ADG786, which works in the following manner:

- The SEL A/$\overline{B}$ signal selects the A or B input to the AD8189. It also selects the switch positions in the ADG786 such that the same selected inputs are connected to V_{REF} when $\overline{EN}$ is low.
- During the horizontal interval, all of the RGB input signals are at a flat black level. A logic signal that is low during $\overline{HSYNC}$ is applied to the $\overline{EN}$ of the ADG786. This closes the switches and clamps the black level to 1.5 V. At all other times, the switches are off and the node at the inputs to the AD8189 floats.

There are two considerations for sizing the input coupling capacitors. One is the time constant during the H-pulse clamping. The other is the droop associated with the capacitor discharge due to the input bias current of the AD8189. For the former, it is better to have a small capacitor, but for the latter, a larger capacitor is better.

The on resistance of the ADG786 and the coupling capacitor form the time constant of the input clamp. The ADG786 on resistance is 5 Ω maximum. With a 0.1 µF capacitor, a time constant of 0.5 µs is created. Thus, a sync pulse of greater than 2.5 µs causes less than 1% error. This is not critical because the black level from successive lines is very close and the voltage changes little from line to line.

A rough approximation of the horizontal line time for a graphics system is 30 µs. This varies depending on the resolution and the vertical rate. The coupling capacitor needs to hold the voltage relatively constant during this time, while the input bias current of the AD8189 discharges it.

The change in voltage is I_B times the line time divided by the capacitance. With an I_B of 2.5 µA, a line time of 30 µs, and a 0.1 µF coupling capacitor, the amount of droop is 0.75 mV. This is roughly 0.1% of the full video amplitude and is not observable in the video display.

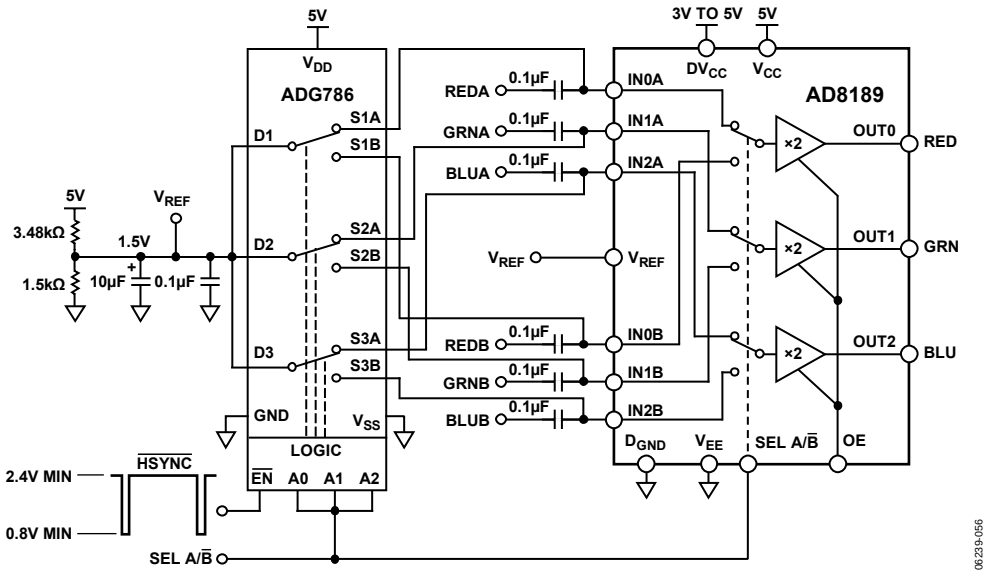

Figure 56. AD8189 AC-Coupled with DC Restore

HIGH SPEED DESIGN CONSIDERATIONS

The AD8188/AD8189 are extremely high speed switching amplifiers for routing the highest resolution graphic signals. Extra care is required in the circuit design and layout to ensure that the full resolution of the video is realized.

First, the board should have at least one layer of a solid ground plane. Long signal paths should be referenced to a ground plane as controlled-impedance traces. All bypass capacitors should be very close to the pins of the part with minimum extra circuit length in the path. It is also helpful to have a large V_{CC} plane on a circuit board layer that is closely spaced to the ground plane. This creates a low inductance interplane capacitance, which is very helpful in supplying the fast transient currents that the part demands during high resolution signal transitions.

EVALUATION BOARD

An evaluation board has been designed and is offered for running the AD8188/AD8189 on a single supply. The inputs and outputs are ac-coupled and terminated with 75 Ω resistors. For the AD8189, a potentiometer is provided to allow setting V_{REF} at any value between V_{CC} and ground.

The logic control signals can be statically set by adding or removing a jumper. If a fast signal is required to drive the logic pins, an SMA connector can be used to deliver the signal, and a place for a termination resistor is provided.

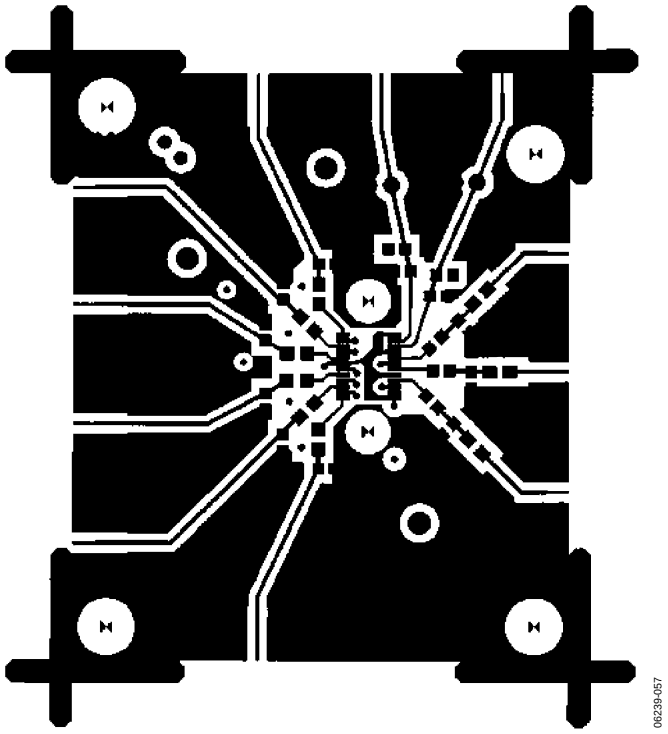

Figure 57. Component Side Board Layout

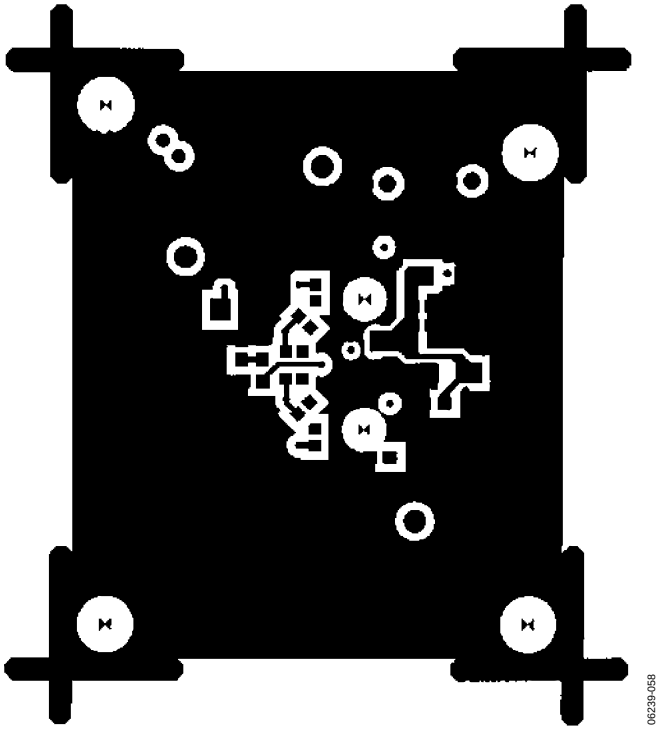

Figure 58. Circuit Side Board Layout

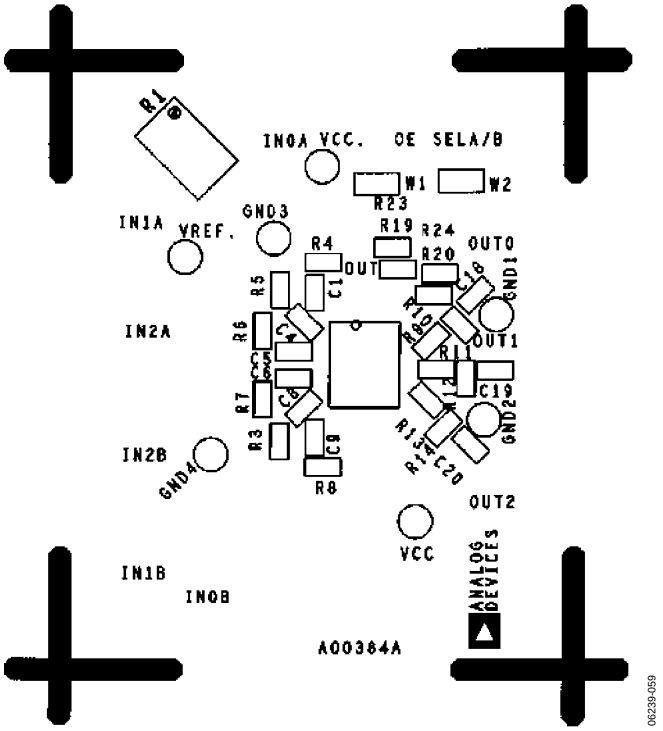

Figure 59. Component Side Silkscreen

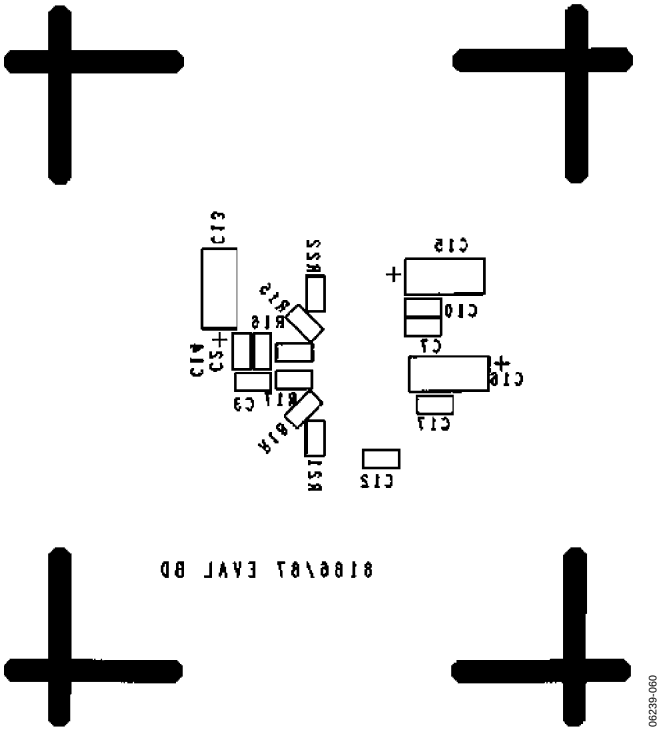

Figure 60. Circuit Side Silkscreen

SCHEMATICS

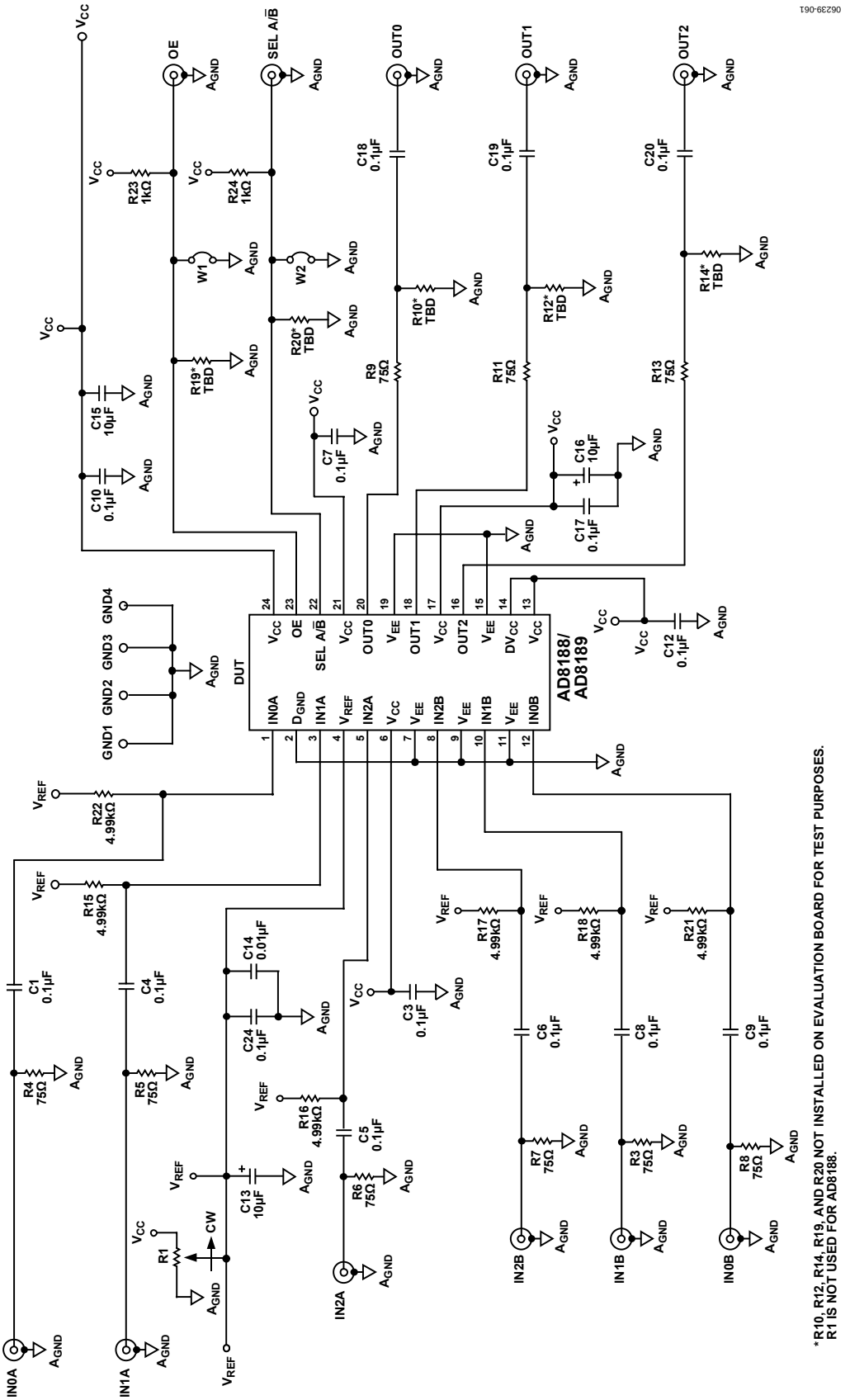

Figure 61. Single-Supply Evaluation Board

OUTLINE DIMENSIONS

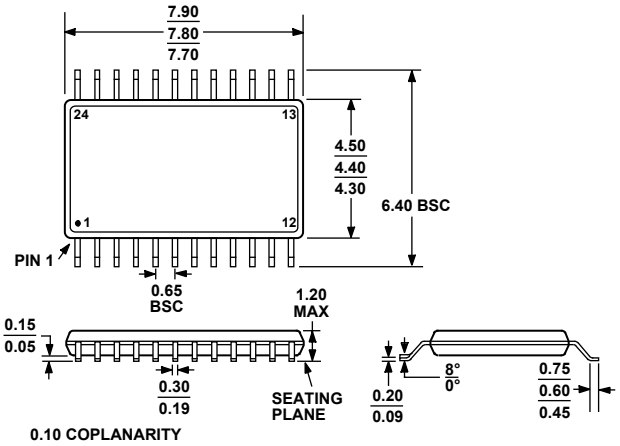

Figure 62. 24-Lead Thin Shrink Small Outline Package [TSSOP]
[RU-24]
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8188ARUZ[1]	–40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD8188ARUZ-RL[1]	–40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP], 13" Reel	RU-24
AD8188ARUZ-R7[1]	–40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP], 7" Reel	RU-24
AD8189ARUZ[1]	–40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
AD8189ARUZ-RL[1]	–40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP], 13" Reel	RU-24
AD8189ARUZ-R7[1]	–40°C to +85°C	24-Lead Thin Shrink Small Outline Package [TSSOP], 7" Reel	RU-24
AD8188Z-EVALZ[1]		Evaluation Board	
AD8189Z-EVALZ[1]		Evaluation Board	

[1] Z = Pb-free part.

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