110 V High Voltage, 1 A High Current, Arbitrary Waveform Generator with Integrated 14-Bit High Speed DAC

FEATURES

- Wide high voltage supply range: ±12 V to ±55 V
- High Output Capability
  - Output voltage range: Up to ±40 V
  - High output current drive: 1 A continuous
  - High slew rate: ≥1800 V/µs into 1000 pF load
  - Large signal bandwidth: 1 MHz
- Extensive Programming and Diagnostics
  - 14-bit resolution arbitrary waveform generation (AWG) mode
  - 16 level analog pattern generation (APG) mode
  - Digitally programmable current, voltage and thermal fault monitoring and protection
  - Programmable supply current with shutdown mode
- Design-in Friendly
  - Unlimited capacitive load drive with external compensation and slew control
  - Package: 80-pin, 12mm x 12mm TQFP
    - EPAD-up package for mountable heatsink
  - Operating temperature range: −40 °C to +85 °C

APPLICATIONS

- Automatic test equipment (ATE)
- Display panel formation and testing
- Piezo drivers
- Programmable power supplies

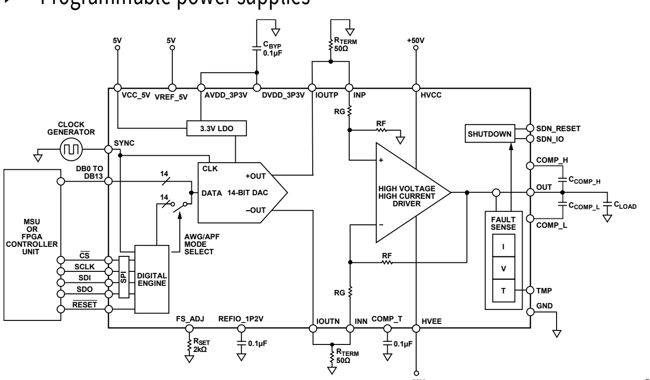

Figure 1. Simplified Functional Block Diagram

GENERAL DESCRIPTION

The AD8460 is a "bits in, power out" high voltage, high-power, high-speed driver optimized for large output current (up to ±1 A) and high slew rate (up to ±1800 V/µs) at high voltage (up to ±40 V) into capacitive loads. Combining a 14-bit high-speed DAC, a high voltage, high output current (HV-HI) analog driver, and fault monitoring and protection circuits, the AD8460 is ideally suited for high power applications such as arbitrary waveform generation (AWG), programmable power supplies, and high voltage automated test equipment (ATE).

A proprietary high-voltage BCDMOS process, novel high voltage architecture, and thermally enhanced package from Analog Devices Inc. enable this high-performance driver. A digital engine implements user-configurable features: modes for digital input, programmable supply current, and fault monitoring and programmable protection settings for output current, output voltage, and junction temperature. Analog features extend functionality: external compensation enables unlimited capacitive load drive, programmable shutdown delay, and full-scale adjustment. The AD8460 operates on high voltage dual supplies up to ±55 V and a single low voltage supply of 5 V.

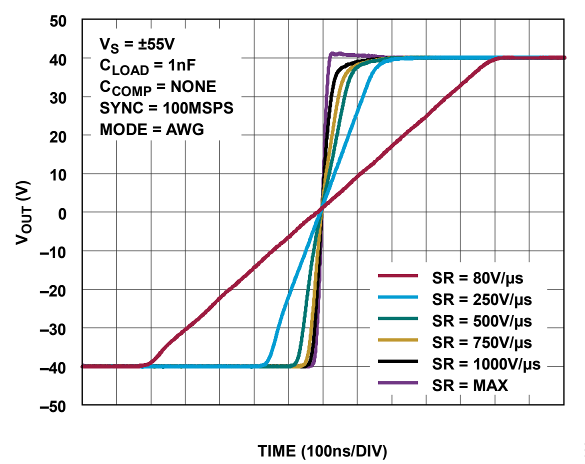

Figure 2. Large Signal Pulse Response vs. Edge Speed with External Slew Control

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110 V High Voltage, 1 A High Current, Arbitrary Waveform Generator with Integrated 14-Bit High Speed DAC

FUNCTIONAL BLOCK DIAGRAM

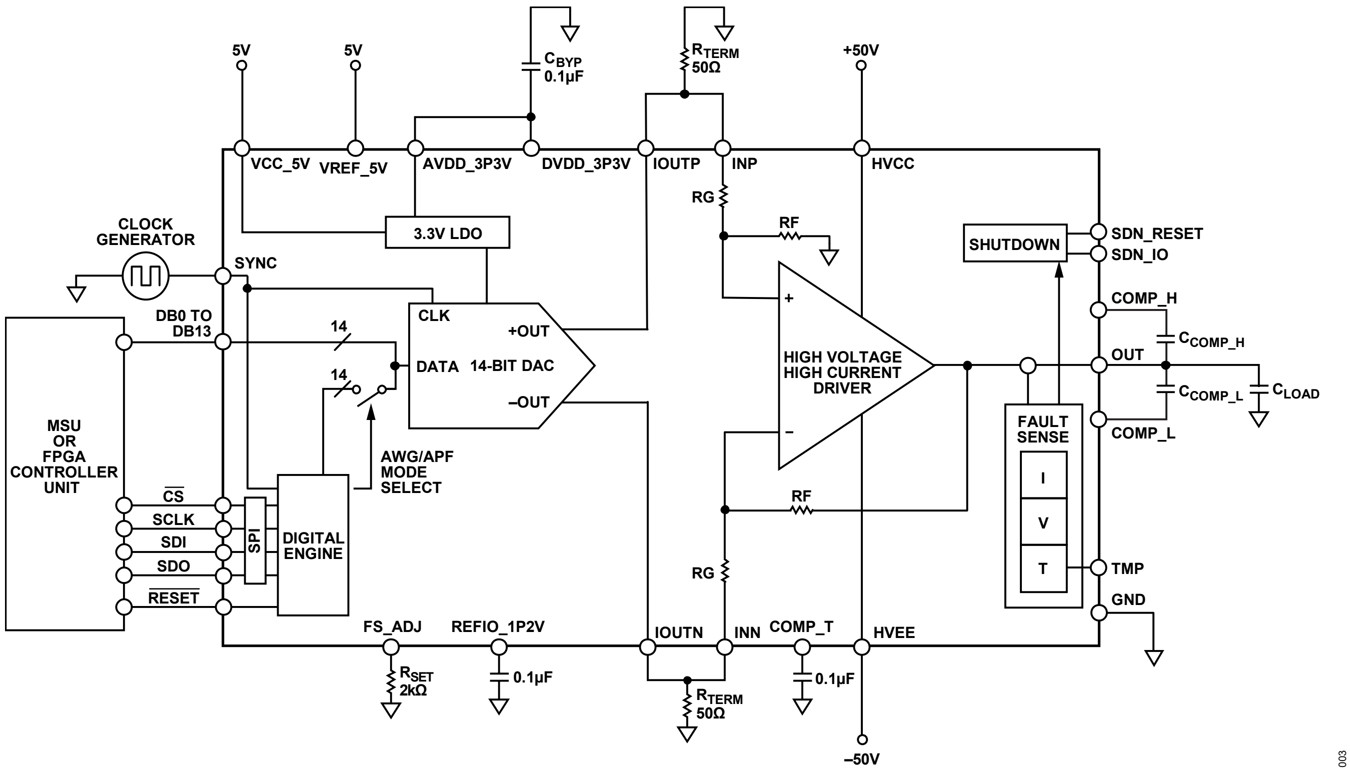

Figure 3. Functional Block Diagram

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REVISION HISTORY

10/2023 - Rev. 0

SPECIFICATIONS

Table 1. Electrical Characteristics

(HVCC = +50 V, HVEE = −50 V, SET_IQ = 0x00, VCC_5V = +5 V, VREF_5V = +5 V, REFIO_1P2V = +1.2 V, R_{TERM} = 50 Ω, R_{SET} to FS_ADJ = 2 kΩ, COMP_L, COMP_H = 0 pF, C_{LOAD} = 1 nF, T_C = 30°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Small Signal Bandwidth	f_{3db}	V_{OUT} = 0.1 V p-p, T_J = 85°C. See *Figure 27*.		4.3		MHz
Large Signal Bandwidth[1]		V_{OUT} = 80 V p-p. See *Figure 26*.		1		MHz
Slew Rate, 20% to 80%	SR_{RISE}	V_{OUT} = 80 V p-p. See *Figure 8*.		2100		V/µs
	SR_{FALL}	V_{OUT} = 80 V p-p. See *Figure 9*.		1800		V/µs
Output 1% Settling Time	t_{ST}	V_{OUT} = 40 V p-p. See *Figure 4.*		13.5		µs
Output 0.1% Settling Time	t_{ST}	V_{OUT} = 40 V p-p. See *Figure 4.*		39.5		µs
NOISE/DISTORTION PERFORMANCE						
Output Noise Spectral Density	V_N	C_{LOAD} = 0 nF, T_J = 85°C, f = 100 kHz		0.6		µV/√Hz
Harmonic Distortion, HD2/HD3		V_{OUT} = 80 V p-p, 1 kHz		−66		dBc
		V_{OUT} = 80 V p-p, 100 kHz		−70		dBc
OUTPUT DC ACCURACY[2]						
Output Offset Error	V_{OS}			4	25	mV
	V_{OS_TC}	T_C = 30°C to 85°C		0.16		mV/°C
Gain Error[3]	V_{GAIN_ERROR}	V_{OUT} = 80 V p-p		0.24	0.45	% FSR
	$V_{GAIN\_ERROR\_TC}$	T_C = 30°C to 85°C		0.002		% FSR/°C
Integral Nonlinearity	INL		−17	+3/−8	12	LSB
Differential Nonlinearity	DNL		−10	+0.3/−4	4	LSB
OUTPUT CHARACTERISTICS						
Output Voltage Range[4]	V_{OUT}			±40		V
Output Headroom	V_{OUT_H}	I_{OUT} = 0.25 A, T_J = 85°C. See *Figure 43*.		HVCC − 2.2		V
		I_{OUT} = 1 A, T_J = 85°C. See *Figure 43*.		HVCC − 5		V
Output Footroom	V_{OUT_L}	I_{OUT} = -0.25 A, T_J = 85°C. See *Figure 43*.		HVEE + 3.3		V
		I_{OUT} = -1 A, T_J = 85°C. See *Figure 43*.		HVEE + 11.1		V

(HVCC = +50 V, HVEE = −50 V, SET_IQ = 0x00, VCC_5V = +5 V, VREF_5V = +5 V, REFIO_1P2V = +1.2 V, R_{TERM} = 50 Ω, R_{SET} to FS_ADJ = 2 kΩ, COMP_L, COMP_H = 0 pF, C_{LOAD} = 1 nF, T_C = 30°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Continuous Output Current Drive[5]	I_{OUT}			1		A
Peak Instantaneous Output Current Drive[6]	I_{OUT}			2.6/−2.2		A
Output Resistance During Shutdown	Z_{OUT_SDN}	See *Figure 47*.		27		kΩ
IOUTP, IOUTN						
Compliance Range	V_{IOUTP_N}		−1		1.25	V
REFERENCE INPUT						
Input Range	VREF_5V[7]			5		V
Input Range	REFIO_1P2V		0.12	1.2	1.25	V
Input Resistance	VREF_5V			34		kΩ
	REFIO_1P2V	Average input resistance over REFIO_1P2V input range.		15		kΩ
REFERENCE OUTPUT						
Output Voltage	REFIO_1P2V		1.195	1.22	1.245	V
		T_C = 30°C to 85°C		17		µV/°C
Output Current Drive				100		µA
SDN_IO SPECIFICATIONS						
Output Voltage Range	SDN_IO	SDN_IO Floating	0		V_{CC}_5V	V
Shutdown Threshold	SDN_IO_{RISING}		2.54	2.56	2.57	V
	$SDN\_IO_{FALLING}$		2.45	2.47	2.48	V
Output Current Drive Sink	SDN_IO_{SNK}			−180		µA
Output Current Drive Source	SDN_IO_{SRC}			180		µA
Turn Off Time	SDN_IO_{TOFF}	SDN_IO > SDN_IO_{RISING} to shutdown. See *DELAYED SHUTDOWN*		400		ns
DC OVERCURRENT PROTECTION						
Sourcing Setpoint Range Max				1		A
Sourcing Code Range			0x06		0x40	
Sinking Setpoint Range Max				-1		A

(HVCC = +50 V, HVEE = −50 V, SET_IQ = 0x00, VCC_5V = +5 V, VREF_5V = +5 V, REFIO_1P2V = +1.2 V, R_{TERM} = 50 Ω, R_{SET} to FS_ADJ = 2 kΩ, COMP_L, COMP_H = 0 pF, C_{LOAD} = 1 nF, T_C = 30°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Sinking Code Range			0x40		0x06	
Setpoint Resolution				15.625		mA/lsb
Setpoint Accuracy		Code = 0x06, 93.75 mA		3.6		%
DC OVERVOLTAGE PROTECTION						
Positive Voltage Setpoint Range Max				55		V
Positive Code Range			0x01		0x1C	
Negative Voltage Setpoint Range Max				−55		V
Negative Code Range			0x1C		0x01	
Setpoint Resolution				1.953		V/lsb
Setpoint Accuracy		Code = 0x10, 31.25 V		1.4		%
DC OVERTEMPERATURE PROTECTION						
Setpoint Range[8]		Max		150		°C
Setpoint Range		Min		20		°C
Code Range			0x2C		0x40	
Setpoint Resolution				6.51		°C/lsb
Setpoint Accuracy		Code = 0x40, T_J = 150°C		2.3		%
TEMPERATURE MONITOR SPECIFICATIONS						
Initial Voltage	$TMP\_V_{INITIAL}$	T_J = 30°C	1.75	1.78	1.81	V
Scaling	TMP_TC			6		mV/°C
SYNC INPUT[9,10]						
Input High Voltage	VIH_{SYNC}		2		3.47	V
Input Low Voltage	VIL_{SYNC}		0		0.8	V
Input Current	I_{L_SYNC}		−1		1	µA
Input Capacitance	C_{SYNC}			12		pF
PARALLEL INTERFACE INPUTS (DB0 to DB13)[9,10]						
Input High Voltage	$VIH_{PARALLEL}$		2		3.47	V
Input Low Voltage	$VIL_{PARALLEL}$		0		0.8	V
Input Current	$I_{L\_PARALLEL}$		−1		1	µA
Input Capacitance	$C_{PARALLEL}$			8		pF
SPI INTERFACE INPUTS (SCLK, SDI, $\overline{CS}$)[9,10]						
Input High Voltage	VIH_{SPI}		2.4		3.47	V

(HVCC = +50 V, HVEE = −50 V, SET_IQ = 0x00, VCC_5V = +5 V, VREF_5V = +5 V, REFIO_1P2V = +1.2 V, R_{TERM} = 50 Ω, R_{SET} to FS_ADJ = 2 kΩ, COMP_L, COMP_H = 0 pF, C_{LOAD} = 1 nF, T_C = 30°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Input Low Voltage	VIL_{SPI}		0		0.8	V
Input Current	I_{L_SPI}		−1		1	µA
Input Capacitance	C_{SPI}			5		pF
SPI INTERFACE OUTPUT (SDO)[9,10]						
Output High Voltage	VOH_{SDO}		2.4		3.31	V
Output Low Voltage	VOL_{SDO}		0		0.4	V
High Impedance Input Current	I_{L_SDO}		−60		60	µA
Output Capacitance	C_{SDO}			5		pF
$\overline{\text{RESET}}$ DIGITAL INPUT[9,10]						
Input High Voltage	VIH_{RESET}		2.4		3.47	V
Input Low Voltage	VIL_{RESET}		0		0.8	V
Input Current	I_{L_RESET}		−1		1	µA
Input Capacitance	C_{RESET}			5		pF
Minimum Duration				10		ns
SDN_RESET Specifications[9,10]						
Input High Voltage	VIH_{SDN_RESET}		2.4		3.47	V
Input Low Voltage	VIL_{SDN_RESET}		0		0.8	V
Input Current	$I_{L\_SDN\_RESET}$		−10		10	µA
Input Capacitance	C_{SDN_RESET}			5		pF
POWER SUPPLIES						
Operation Range	HVCC		12		55	V
	HVEE		−55		−12	V
	VCC_5V		4.9	5	5.5	V
Quiescent Current (Enabled)	I_{HVCC}	See *PROGRAMMABLE QUIESCENT CURRENT*.		22.5	26.5	mA
	I_{HVEE}	See *PROGRAMMABLE QUIESCENT CURRENT*.	−26.5	−22.5		mA
	I_{VCC_5V}			39	41.5	mA

(HVCC = +50 V, HVEE = −50 V, SET_IQ = 0x00, VCC_5V = +5 V, VREF_5V = +5 V, REFIO_1P2V = +1.2 V, R_{TERM} = 50 Ω, R_{SET} to FS_ADJ = 2 kΩ, COMP_L, COMP_H = 0 pF, C_{LOAD} = 1 nF, T_C = 30°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Quiescent Current (Shutdown)	I_{HVCC}			120	160	µA
		HVCC = + 12 V		80		µA
	I_{HVEE}		−160	−120		µA
		HVEE = −12 V		-80		µA
	I_{VCC_5V}			10.5	13.5	mA
Power Supply Rejection Ratio	$PSRR_{HVCC}$	HVCC = + 12 V to + 55 V, HVEE = -50V		93		dB
	$PSRR_{HVEE}$	HVCC = + 50 V, HVEE = -12 V to -55 V		106		dB
	$PSRR_{VCC\_5V}$	VCC_5V = 4.9 V to + 5.5 V		86		dB

1 Large signal bandwidth may be limited by thermal design. Refer to *Thermal Management* section.

2 These specifications are referred to the output of the AD8460.

3 FSR = Full scale range

4 This output voltage swing is set by the device's default configuration.

5 See *Thermal Management* section for more details.

6 The AD8460 has been lifetime tested with a 1 nF load, driven with an 80 Vp-p square wave at 1 kHz.

7 See the VREF_5V section for details on the effects of supply variations on this pin.

8 The absolute maximum junction temperature is 150°C.

9 Guaranteed by design and characterization, not production tested.

10 T_J = 30 °C to 105 °C

Table 2. TIMING CHARACTERISTICS

(HVCC = +50 V, HVEE = −50 V, SET_IQ = 0x00, VCC_5V = +5 V, VREF_5V = +5 V, REFIO_1P2V = +1.2 V, R_{TERM} = 50 Ω, R_{SET} to FS_ADJ = 2 kΩ, COMP_L, COMP_H = 0 pF, C_{LOAD} = 1 nF, T_J = 30 °C to 105 °C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
SYNC CLOCK RATE[1]						
Maximum Clock Rate	$SYNC_{AWG}$	AWG Mode (Parallel Data Inputs)[2]		100		MHz
	$SYNC_{APG}$	APG Mode (Serial Data Inputs)		20		MHz
PARALLEL TIMING[1]						
Input Setup Time	t_{S_PAR}		4			ns
Input Hold Time	t_{H_PAR}		4			ns
Latch Pulse Width	t_{LPW}		4			ns
Output Propagation Delay	t_{PD}			45		ns
SPI TIMING[1]						
SCLK Frequency	f_{SCLK}				20	MHz
Pulse Width High	t_{HI}		24			ns
Pulse Width Low	t_{LO}		20			ns
Setup $\overline{CS}$ to SCLK Edge	t_{S_SPI}		5			ns
Hold SCLK to $\overline{CS}$ High	t_{H_SPI}		5			ns
Setup Time SDI to SCLK High	t_{DS}		5			ns
Hold Time SDI to SCLK Low	t_{DH}		5			ns
Data Valid SCLK to SDO	t_{ACCESS}				10	ns
SDO Data Release	t_Z				10	ns

1 Guaranteed by design and characterization, not production tested.

2 For details on the maximum achievable output frequency, see *Figure 26* and *Thermal Management* section.

Timing Diagrams

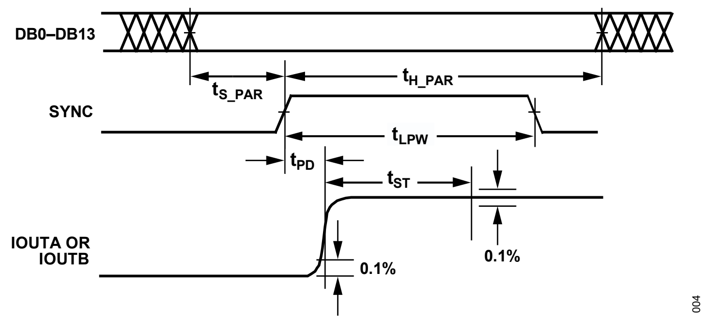

Figure 4. Parallel Inputs Timing Diagram

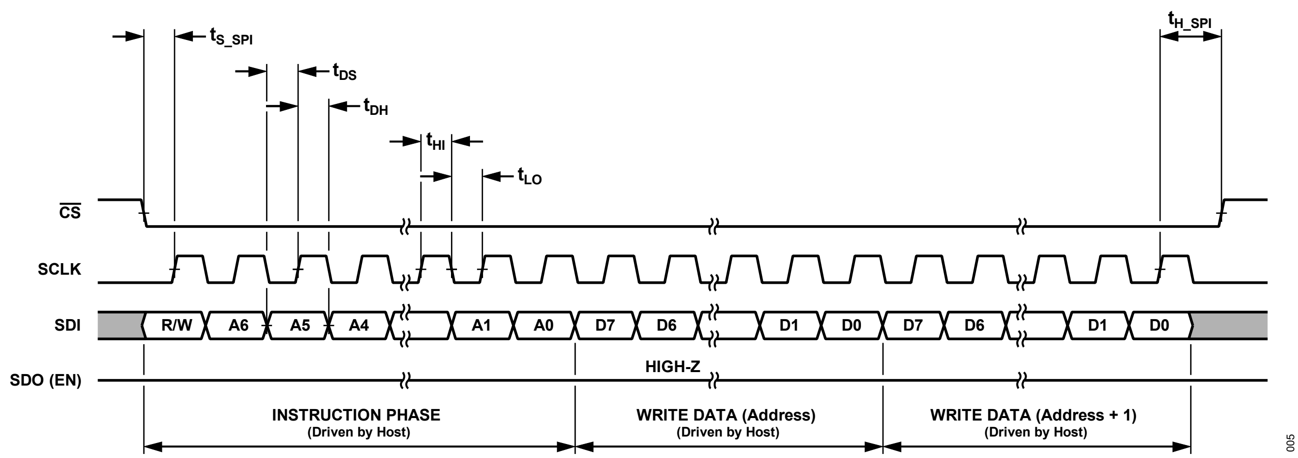

Figure 5. SPI Timing Diagram (Write Operation)

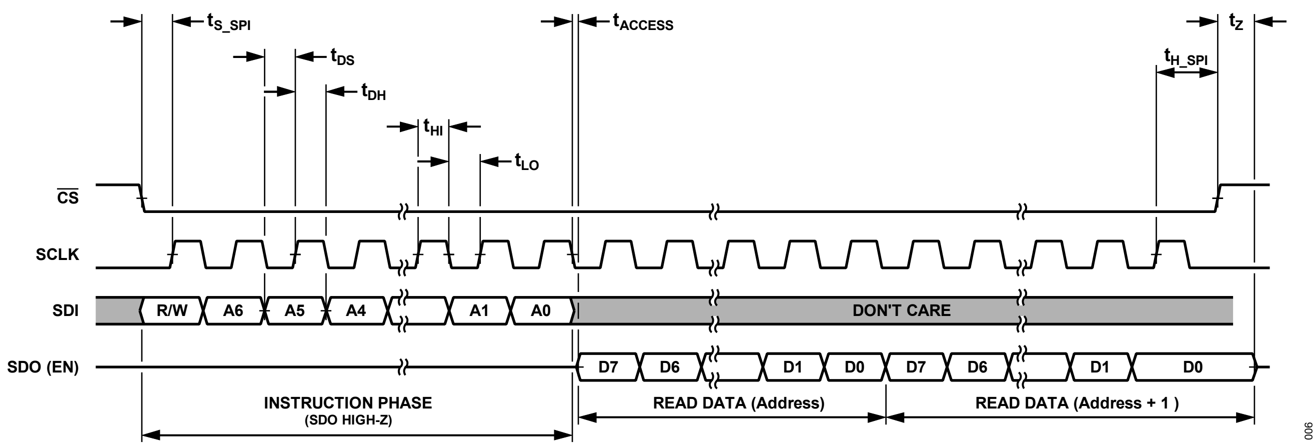

Figure 6. SPI Timing Diagram (Read Operation)

ABSOLUTE MAXIMUM RATINGS

T_A = 25 °C, unless otherwise specified.

Table 3. Absolute Maximum Ratings

PARAMETER	RATING
HVCC to HVEE	115V
OUT	HVEE − 0.3V to HVCC + 0.3V
COMP_H	HVCC − 5V to HVCC + 0.3V
COMP_L	HVEE − 0.3V to HVEE + 5V
COMP_T to GND	−0.3V to VCC_5V + 0.3V
VCC_5V to GND	−0.3V to +6V
SYNC, DB0 – DB13 to GND	−0.3V to DVDD_3P3V + 0.3V
VREF_5V to GND	−0.3V to VCC_5V + 0.3V or +5.85 V (whichever is less)
DVDD_3P3V to GND	−0.3V to 3.6V
AVDD_3P3V to GND	−0.3V to 3.6V
SCLK, /CS, SDIO, SDO to GND	−0.3V to VCC_5V + 0.3V
REFIO_1P2V to GND	−0.3V to AVDD_3P3V + 0.3V
FS_ADJ to GND	−0.3V to AVDD_3P3V + 0.3V
IOUTP, IOUTN to GND	−1V to AVDD_3P3V + 0.3V
SYNC Clock to GND	−0.3V to DVDD_3P3V +0.3V
$\overline{\text{RESET}}$ to GND	−0.3V to VCC_5V + 0.3V
SDN_IO, SDN_RESET to GND	−0.3V to VCC_5V + 0.3V
TMP to GND	−0.3V to VCC_5V + 0.3V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range[1]	−40°C to +85°C
Junction Temperature (T_J)[2]	+150°C
Peak Solder Reflow Temperature[3]	IPC/JEDEC J-STD-020

1 Subject to T_J <=150 °C

2 Extended operation of Tj at or near the absolute maximum junction temperature rating accelerates device aging. Ensure proper thermal management.

3 RoHS-compliant assemblies (20 sec to 40 sec)

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required. To keep the junction temperature (T_J) below the absolute maximum rating, it is typically required to incorporate thermal management techniques. See the *Thermal Management* section for more details.

θ_{JA} is the natural convection, junction-to-ambient thermal resistance. θ_{JC} is the junction-to-case thermal resistance.

Table 4. Thermal Resistance

Package Type[1]	θ_{JA}[2]	θ_{JC}[3]	θ_{JC}[2]	Unit
80-Lead TQFP (SV-80-7)	39.5	1.1	2.3	°C/W

[1] Thermal impedance simulated values based on JEDEC JESD-51. For θ_{JA} with heatsink and airflow. See the *Thermal Management* section.

[2] Includes derating across the die.

[3] Equal power dissipation across the die.

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only. Human body model (HBM) per ANSI/ESDA/JEDEC JS-001. Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

Table 5. AD8460 80-Lead TQFP

ESD Model	Withstand Threshold (V)	Class
HBM	± 1000	1C
FICDM	± 1000	C3

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

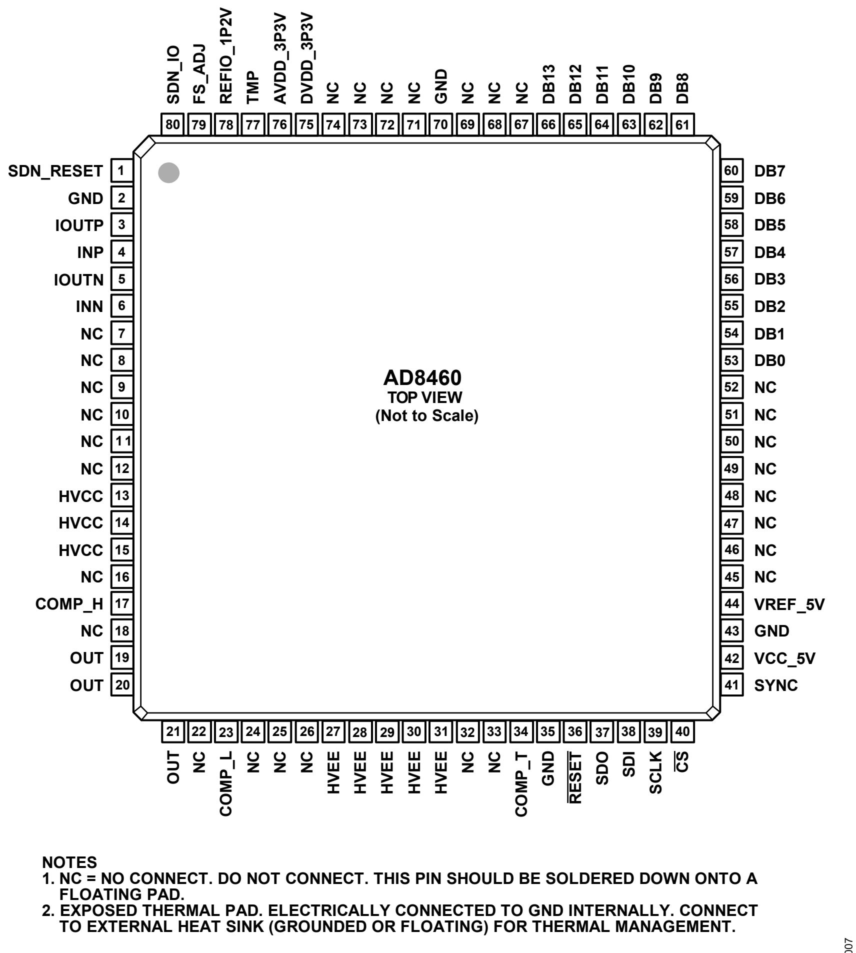

Figure 7. Top View with Pin 1 in Upper Left and Pin Numbers Ascending Anticlockwise

Table 6. Pin Function Descriptions

PIN	NAME	DESCRIPTION
1	SDN_RESET	Shutdown reset input (active high).
2	GND	Ground (analog and digital).
3	IOUTP	DAC current output. Connect to INP. Requires an external, precision, low drift 50 Ω with 0.1% tolerance resistor from IOUTP to GND.
4	INP	High voltage driver noninverting input. Connect to IOUTP.
5	IOUTN	DAC complementary current output. Connect to INN. Requires an external, precision, low drift 50 Ω with 0.1% tolerance resistor from IOUTN to GND.
6	INN	High voltage driver inverting input. Connect to IOUTN.
7 to 12	NC	Do not connect. This pin should be soldered down onto a floating pad.

13 to 15	HVCC	High voltage positive power supply.
16	NC	Do not connect. This pin should be soldered down onto a floating pad.
17	COMP_H	High side compensation. Depending on capacitive load drive requirements, this may be left floating or connected to OUT through a capacitor. See the *OUTPUT COMPENSATION (COMP_H AND COMP_L)* section for more details.
18	NC	Do not connect. This pin should be soldered down onto a floating pad.
19 to 21	OUT	High voltage analog output.
22	NC	Do not connect. This pin should be soldered down onto a floating pad.
23	COMP_L	Low side compensation. Depending on capacitive load drive requirements, this may be left floating or connected to OUT through a capacitor. See the *OUTPUT COMPENSATION (COMP_H AND COMP_L)* section for more details.
24 to 26	NC	Do not connect. These pins should be soldered down onto a floating pad.
27 to 31	HVEE	High voltage negative power supply.
32 to 33	NC	Do not connect. These pins should be soldered down onto a floating pad.
34	COMP_T	Thermal monitor compensation. Connect a 0.1 µF capacitor to GND.
35	GND	Ground (analog and digital).
36	$\overline{\text{RESET}}$	Digital reset (active low, 3.3 V logic).
37	SDO	SPI serial data output (3.3 V logic).
38	SDI	SPI serial data input (3.3 V logic)
39	SCLK	SPI serial clock input (3.3 V logic).
40	$\overline{\text{CS}}$	SPI chip select input (active low, 3.3 V logic).
41	SYNC	Sync clock input for internal DAC data (3.3 V logic).
42	VCC_5V	Low voltage power supply (5 V).
43	GND	Ground (analog and digital).
44	VREF_5V	Reference voltage for analog low voltage and protection threshold DACs. Connect VREF_5V to an external 5 V reference or VCC_5V (reduced accuracy). See the *VREF_5V* section for more details on power sequencing.
45 to 52	NC	Do not connect. This pin should be soldered down onto a floating pad.
53	DB0	DAC LSB (3.3 V logic). AWG mode data input. DB0 must be NC or floated in APG mode.
54 to 65	DB1 to DB12	DAC data bits [1:12] (3.3 V logic). AWG mode data inputs. DB1 to DB12 must be NC or floated in APG mode.
66	DB13	DAC MSB (3.3 V logic). AWG mode data input. DB13 must be NC or floated in APG mode.
67 to 69	NC	Do not connect. These pins should be soldered down onto a floating pad.
70	GND	Ground (analog and digital).
71 to 74	NC	Do not connect. This pin should be soldered down onto a floating pad.
75	DVDD_3P3V	Digital supply bypass. Connect directly to AVDD_3P3V. Requires 0.1 µF capacitor to GND.

76	AVDD_3P3V	Analog supply bypass. Output of internal 3.3 V LDO. Requires 0.1 µF capacitor to GND.
77	TMP	Junction temperature monitor output voltage.
78	REFIO_1P2V	Reference input/output for internal DAC. Connect to external 1.2 V reference or output of 1.2 V reference output (reduced accuracy). Requires 0.1 µF capacitor to GND.
79	FS_ADJ	DAC full-scale current output adjust. Requires 2 kΩ resistor to GND. For more information about full-scale adjustment, see the *FULL-SCALE ADJUSTMENT* section.
80	SDN_IO	Shutdown input/output (Shutdown active high). Connect capacitor to GND for shutdown delay.
	EPAD	Exposed thermal pad. Electrically connected to GND internally. Connect to external heat sink (grounded or floating) for thermal management.

INTERPRETING TYPICAL PERFORMANCE CURVES

The AD8460's performance parameters are fundamentally dependent on junction temperature (T_J), which may be significantly higher than ambient temperature (T_A). For this reason, all AD8460 typical performance curves (TPCs) relating to temperature are represented as a function of T_J (axis at bottom of plot), which can be measured through the TMP pin. See the TMP section for information on direct die temperature measurement.

To present a complete picture, T_A is shown as an alternative scale at the top of the plot. Refer to T_A scale for estimation of junction temperature when the TMP pin is not monitored. The relation between TJ and TA is valid for the default thermal management configuration and the specified test conditions indicated for each plot. See the *Thermal Management* section for the relationship among T_J, T_A, and power dissipation.

Finally, note that each curve on a temperature−based TPC has both a solid and a dashed section. The solid portion represents typical performance that is exhibited when using the recommended passive heat sinking configuration. The dashed portion represents typical performance that is achievable when using active thermal management, such as with forced air or liquid cooling. See the *Thermal Management* section for more information.

TYPICAL PERFORMANCE CHARACTERISTICS

HVCC = + 50 V, HVEE = - 50 V, SET_IQ = 0x00, VCC_5V = + 5 V, VREF_5V = + 5 V, REFIO_1P2V = + 1.2 V, R_{TERM} = 50 Ω, R_{SET} to FS_ADJ = 2 kΩ, COMP_L, COMP_H = 0 pF, C_{LOAD} = 1 nF, T_C = 30°C, unless otherwise noted.

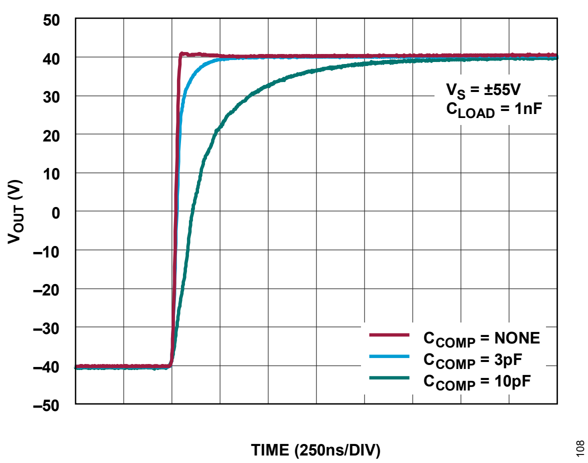

Figure 8. Large Signal Pulse Response vs. C_{COMP}, Rising Edge, C_{LOAD} = 1 nF

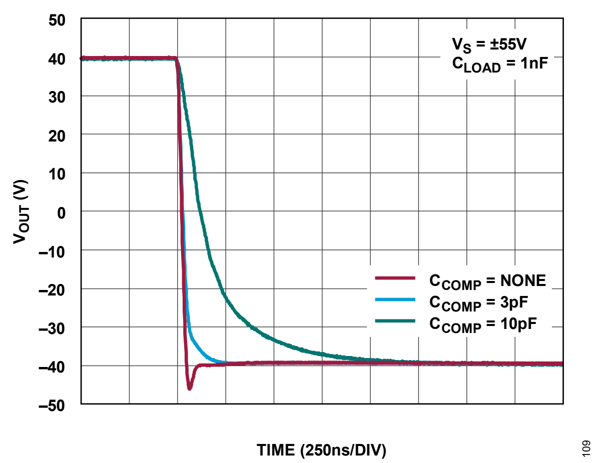

Figure 9. Falling Edge - Large Signal Pulse Response vs. C_{COMP}, Falling Edge, C_{LOAD} = 1 nF

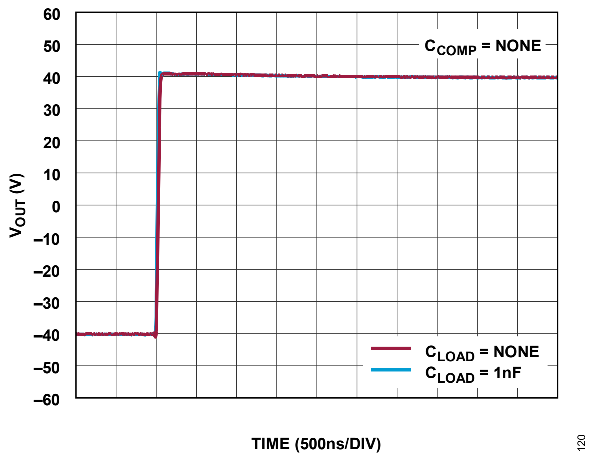

Figure 10. Large Signal Pulse Response vs. C_{LOAD}, Rising Edge

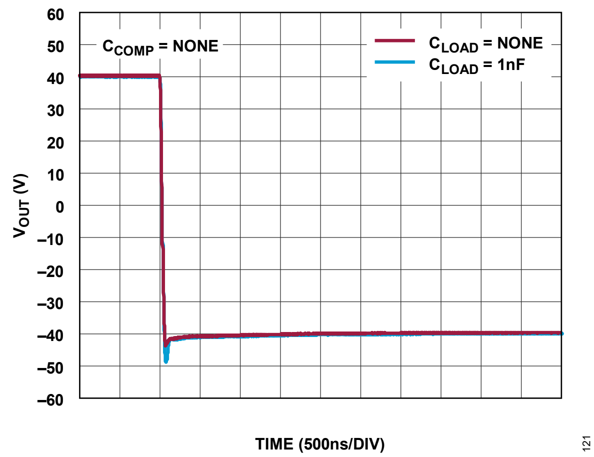

Figure 11. Large Signal Pulse Response vs. C_{LOAD}, Falling Edge

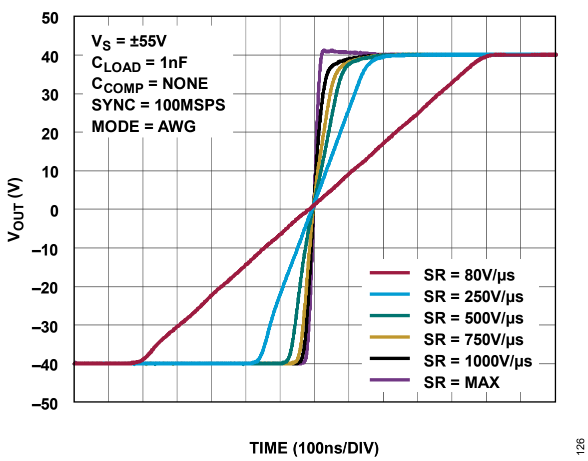

Figure 12. Large Signal Pulse Response vs. Edge Speed, C_{LOAD} = 1 nF, C_{COMP} = None

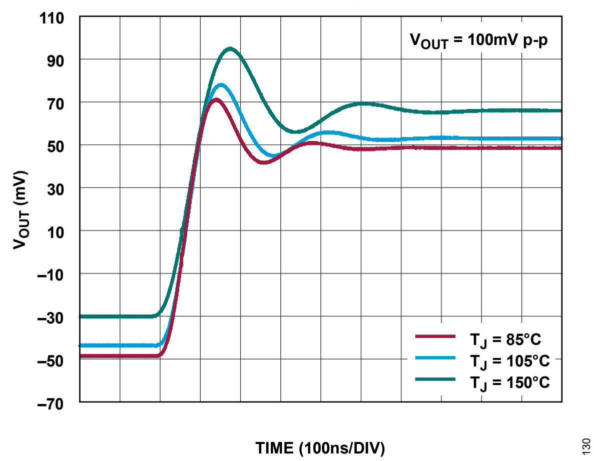

Figure 13. Small Signal Pulse Response vs. Temperature, Rising Edge, V_{OUT} = 100 mV p-p

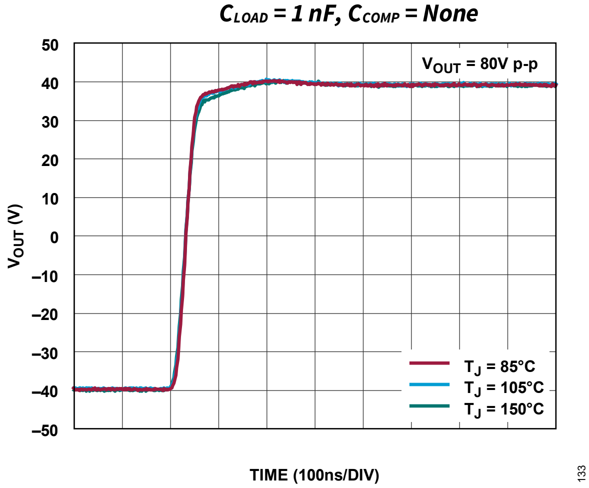

Figure 14. Large Signal Pulse Response vs. Temperature, Rising Edge

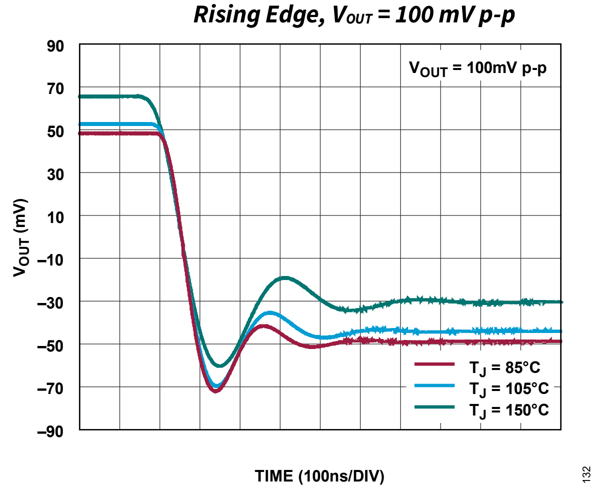

Figure 15. Small Signal Pulse Response vs. Temperature, Falling Edge, V_{OUT} = 100 mV p-p

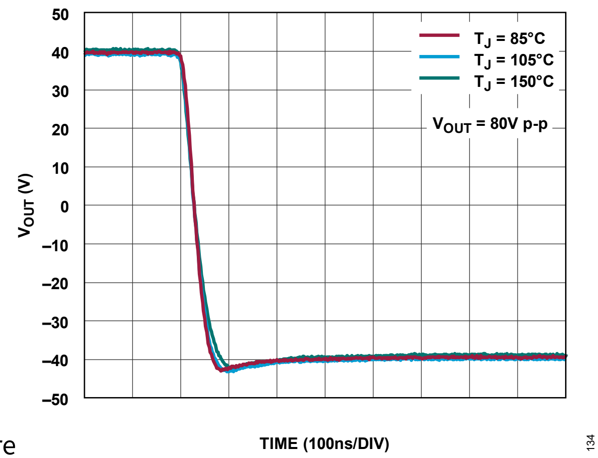

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Figure 16. Large Signal Pulse Response vs. Temperature, Falling Edge

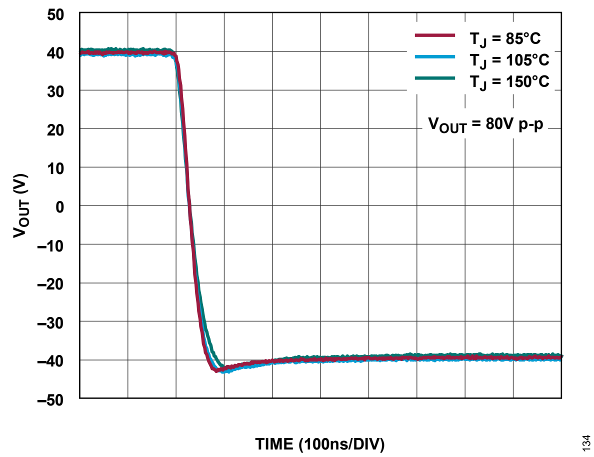

Figure 17. Pulse Response vs. Temperature, Falling Edge, V_{OUT} = 80 V p-p

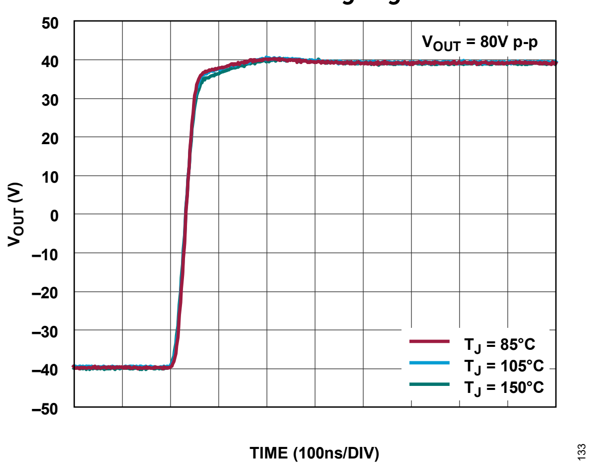

Figure 18. Pulse Response vs. Temperature, Rising Edge, V_{OUT} = 80 V p-p

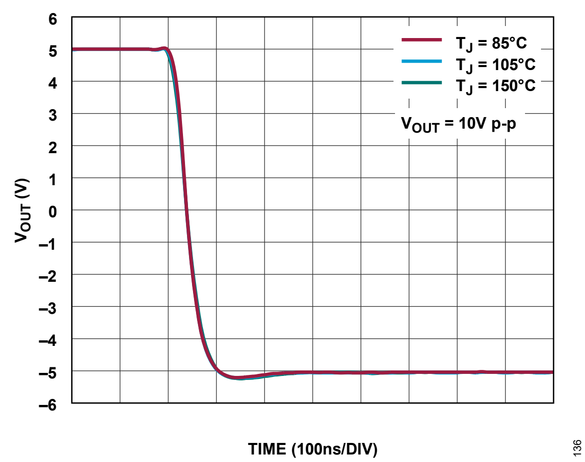

Figure 19. Pulse Response vs. Temperature, Falling Edge, V_{OUT} = 10 V p-p

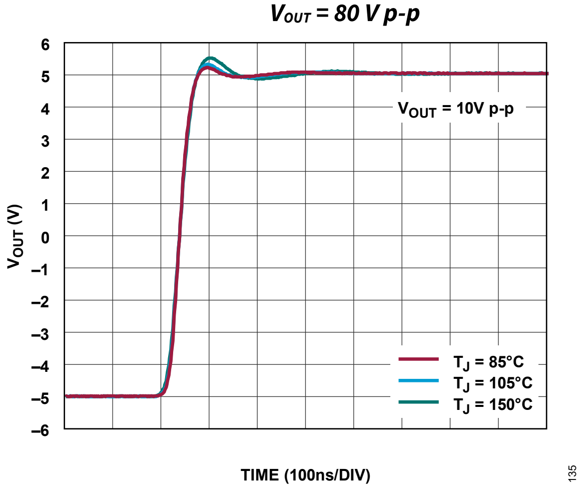

Figure 20. Pulse Response vs. Temperature, Rising Edge, V_{OUT} = 10 V p-p

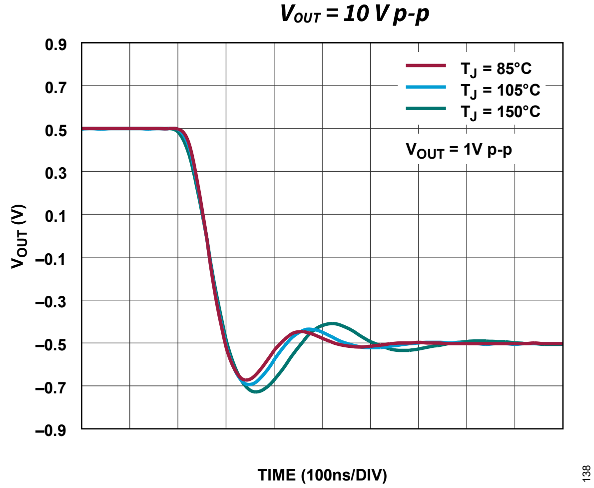

Figure 21. Pulse Response vs. Temperature, Falling Edge, V_{OUT} = 1 V p-p

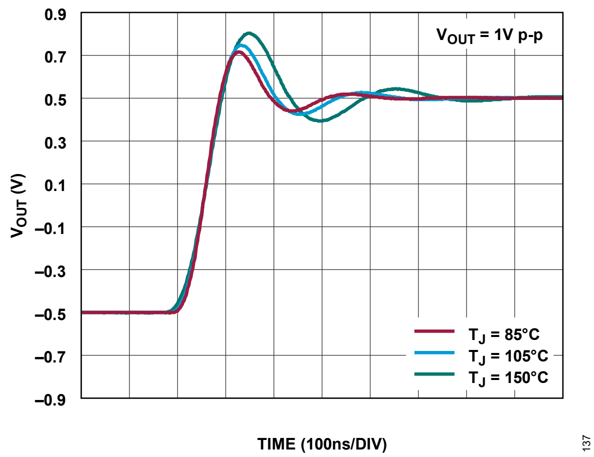

Figure 22. Pulse Response vs. Temperature, Rising Edge, V_{OUT} = 1 V p-p

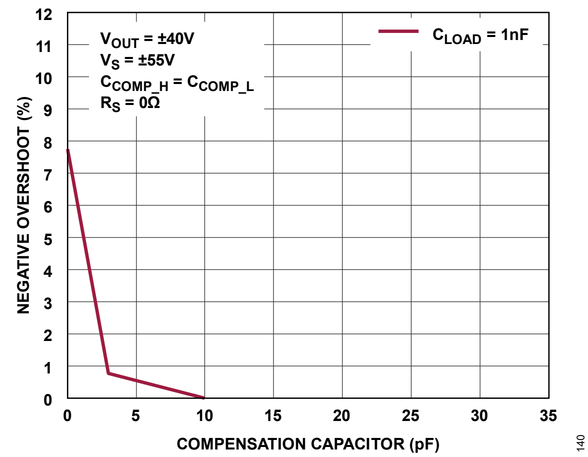

Figure 23. Large Signal Pulse Response Overshoot vs. C_{LOAD} and C_{COMP}, Negative Overshoot

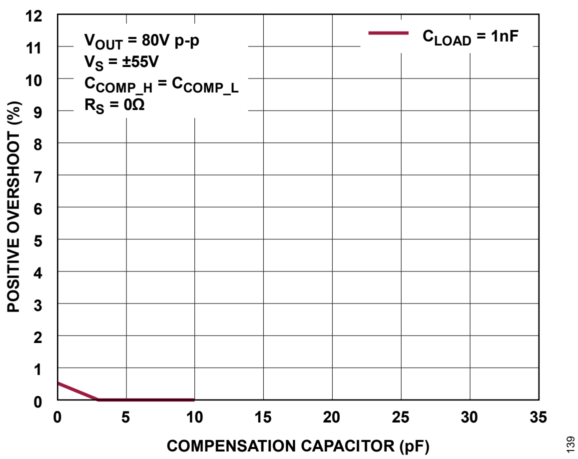

Figure 24. Large Signal Pulse Response Overshoot vs. C_{LOAD} and C_{COMP}, Positive Overshoot

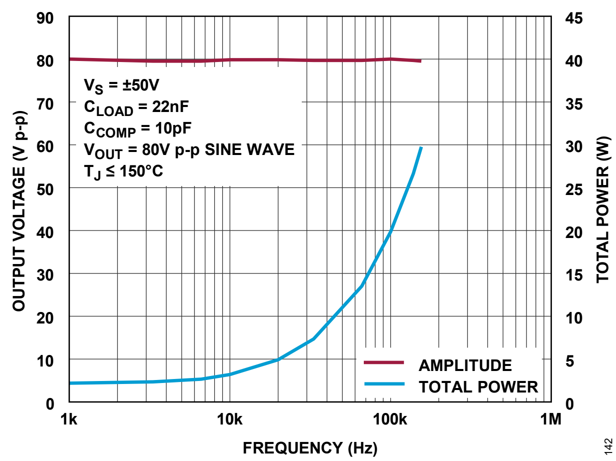

Figure 25. Large Signal Bandwidth, C_{LOAD} = 22 nF, C_{COMP} = 10 pF

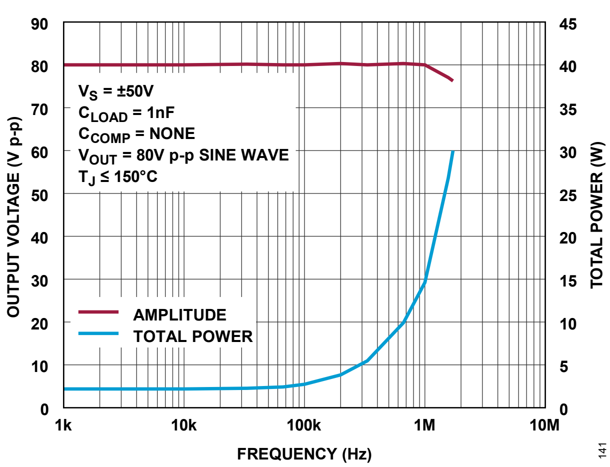

Figure 26. Large Signal Bandwidth, C_{LOAD} = 1 nF, C_{COMP} = None

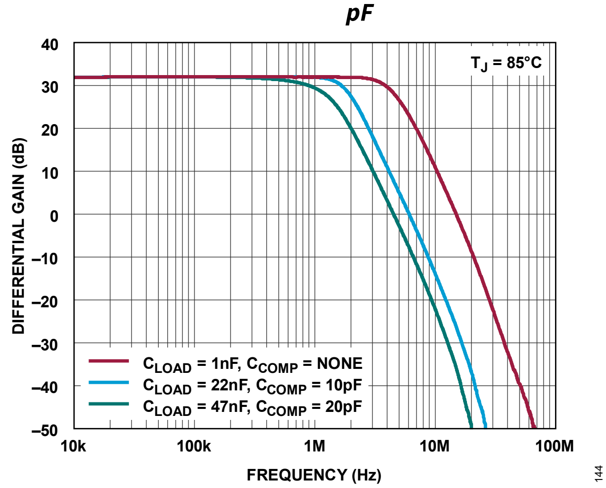

Figure 27. Small Signal Frequency Response vs. C_{LOAD}, T_J = 85 °C

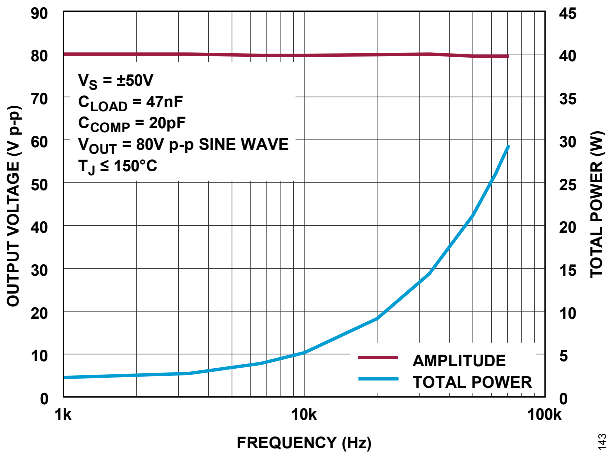

Figure 28. Large Signal Bandwidth, C_{LOAD} = 47 nF, C_{COMP} = 20 pF

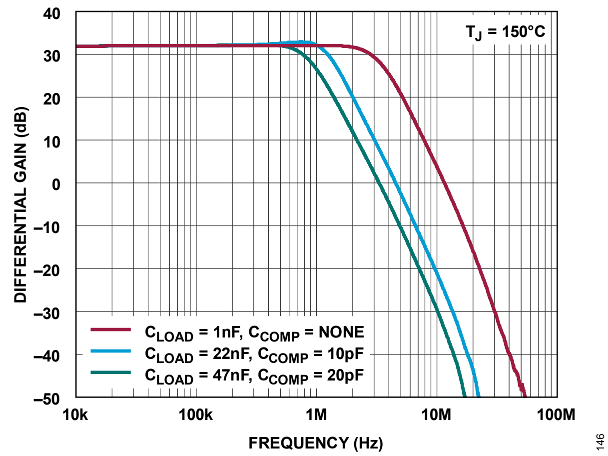

Figure 29. Small Signal Frequency Response vs. C_{LOAD}, T_J = 150 °C

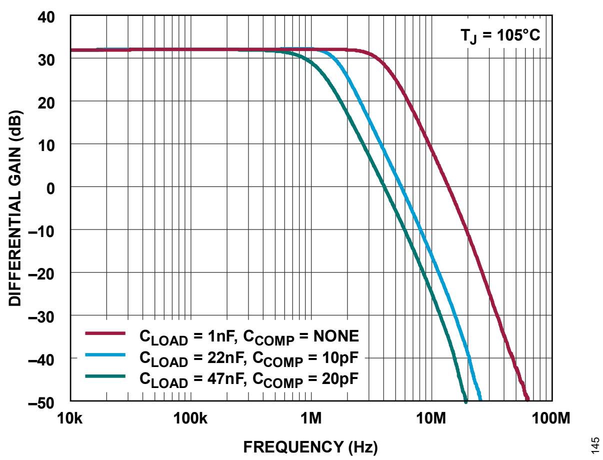

Figure 30. Small Signal Frequency Response vs. C_{LOAD}, T_J = 105 °C

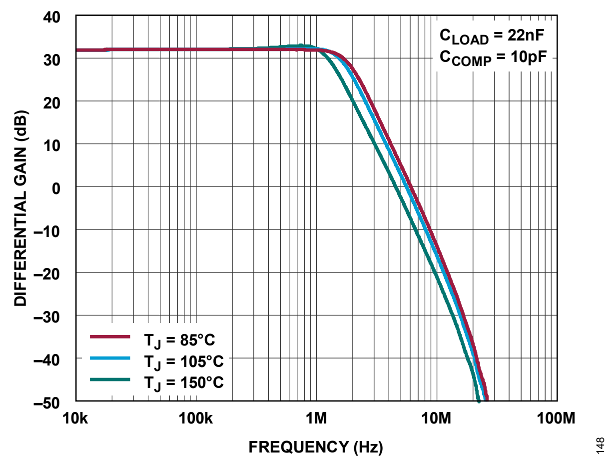

Figure 31. Small Signal Frequency Response vs. Temperature, C_{LOAD} = 22 nF, C_{COMP} = 10 pF

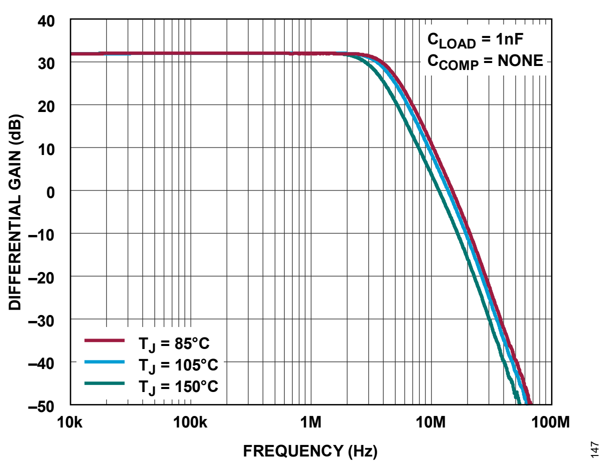

Figure 32. Small Signal Frequency Response vs. Temperature, C_{LOAD} = 1 nF, C_{COMP} = None

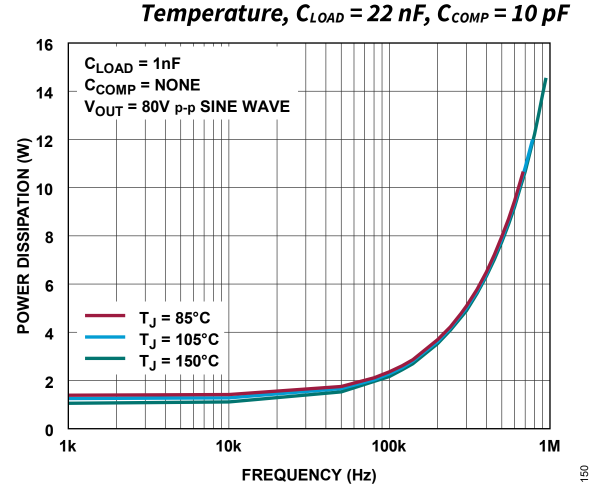

Figure 33. Large Signal Frequency Response vs. Temperature, C_{LOAD} = 1 nF, C_{COMP} = None

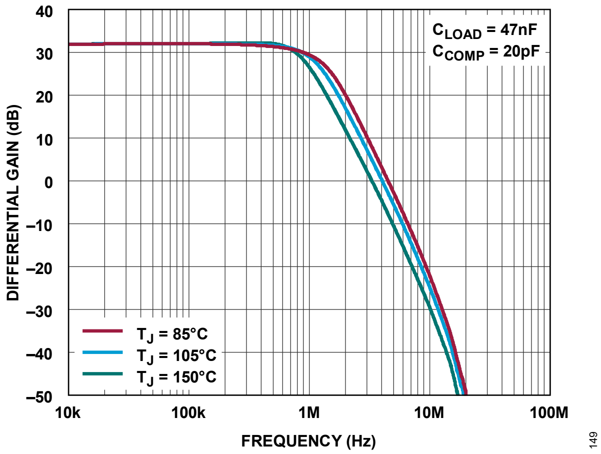

Figure 34. Small Signal Frequency Response vs. Temperature, C_{LOAD} = 47 nF, C_{COMP} = 20 pF

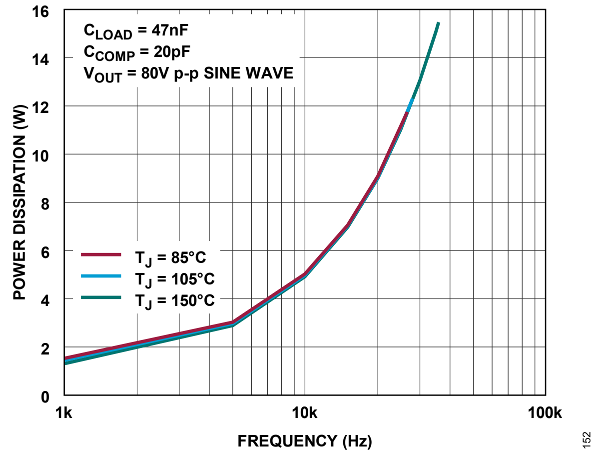

Figure 35. Large Signal Frequency Response vs. Temperature, C_{LOAD} = 47 nF, C_{COMP} = 20pF

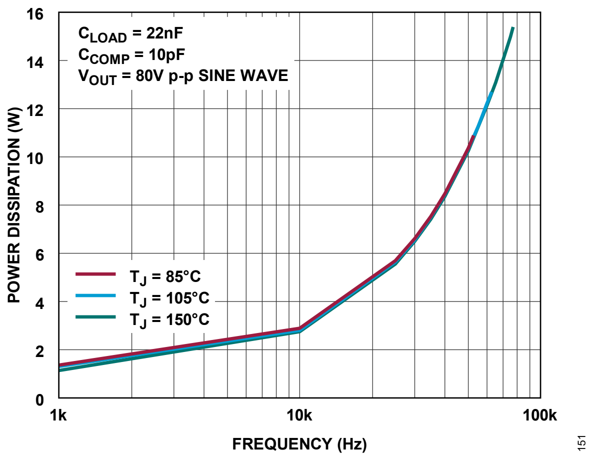

Figure 36. Large Signal Frequency Response vs. Temperature, C_{LOAD} = 22 nF, C_{COMP} = 10pF

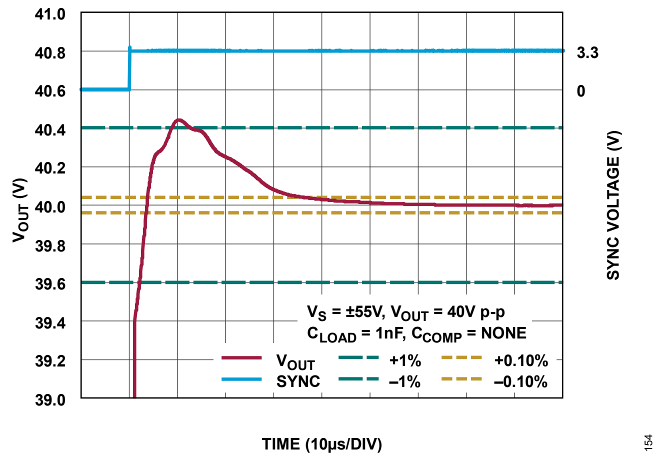

Figure 37. Settling Time to 0.1% and 1%, V_{OUT} = 40 Vp-p, V_S = ±55 V, C_{LOAD} = 1 nF, C_{COMP} = None

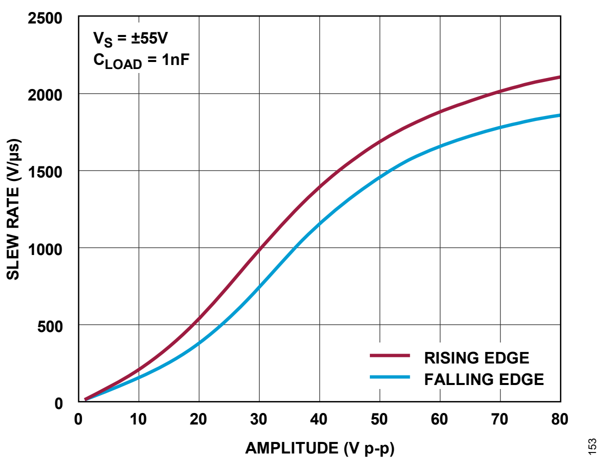

Figure 38. Slew Rate vs. Output Amplitude

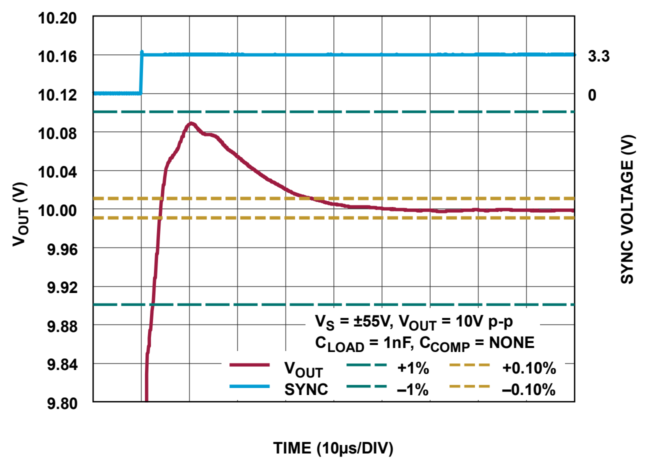

Figure 39. Settling Time to 0.1% and 1%, V_{OUT} = 10 Vp-p, V_S = ±55 V, C_{LOAD} = 1 nF, C_{COMP} = None

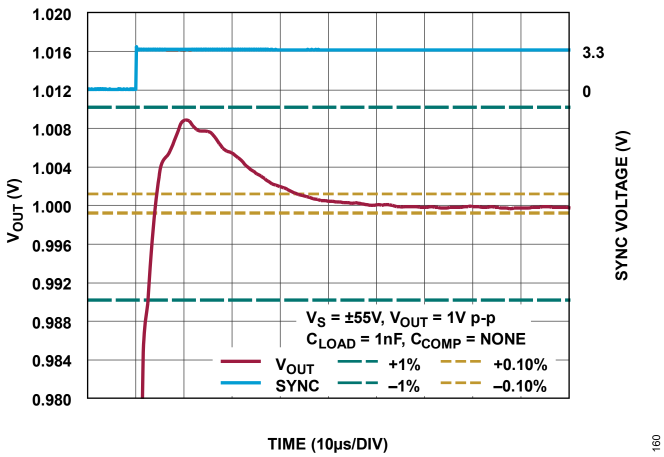

Figure 40. Settling Time to 0.1% and 1%, V_{OUT} = 1 Vp-p, V_S = ±55 V, C_{LOAD} = 1 nF, C_{COMP} = None

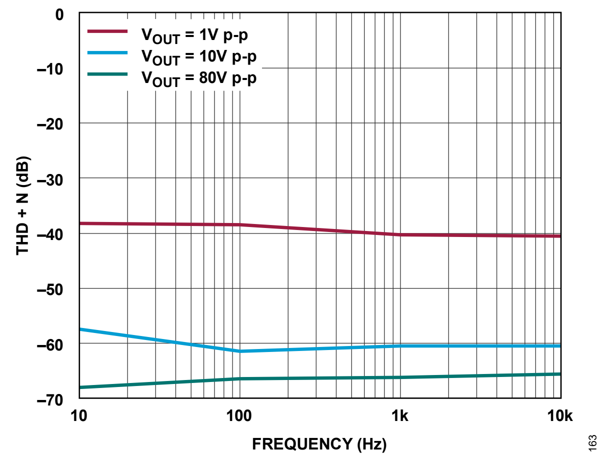

Figure 41. Total Harmonic Distortion and Noise vs. Frequency at Various Large Output Swings

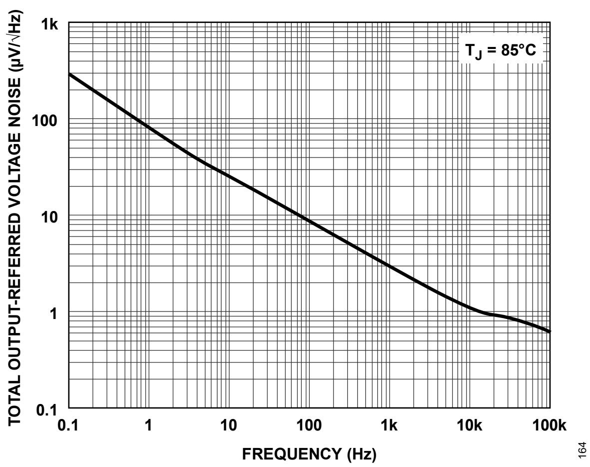

Figure 42. Total Output Noise vs. Frequency

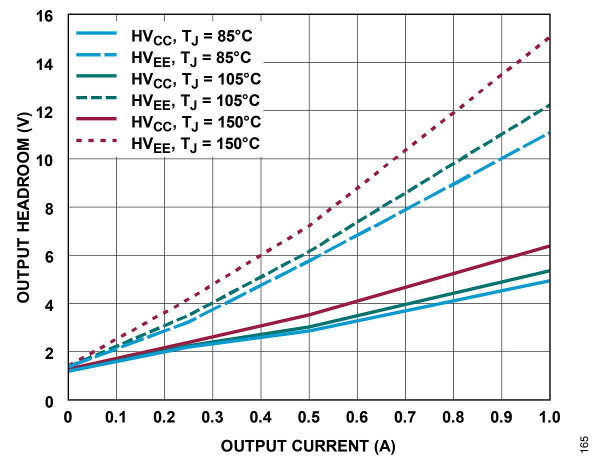

Figure 43. Output Headroom vs. Output Current and Temperature

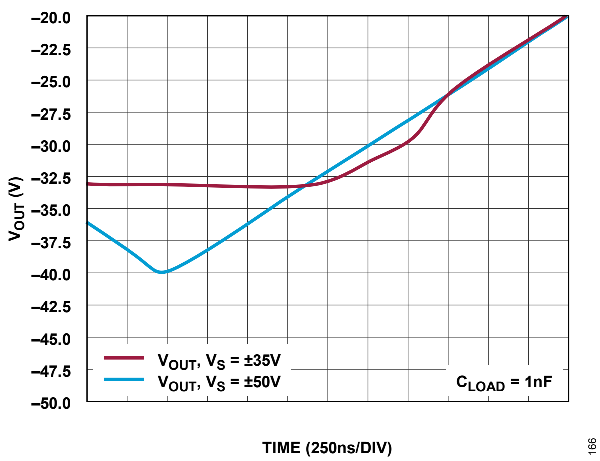

Figure 44. Output Overdrive Recovery vs. Time, Rising

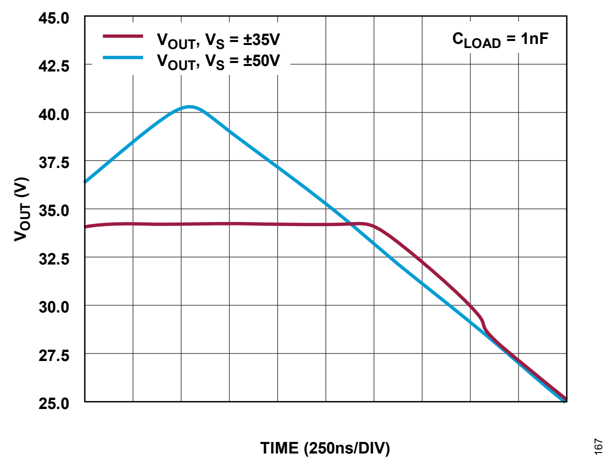

Figure 45. Output Overdrive Recovery vs. Time, Falling

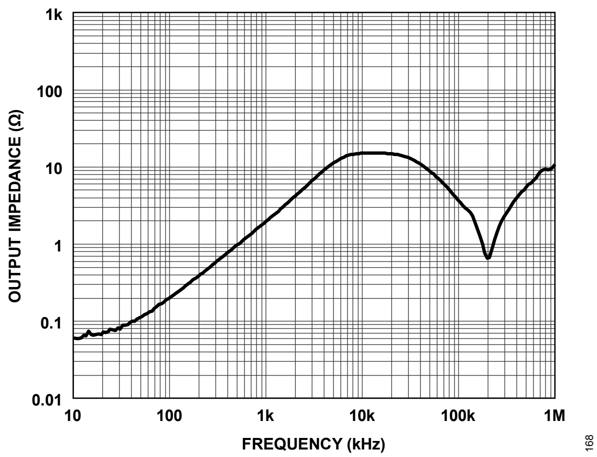

Figure 46. Output Impedance vs. Frequency, Enabled

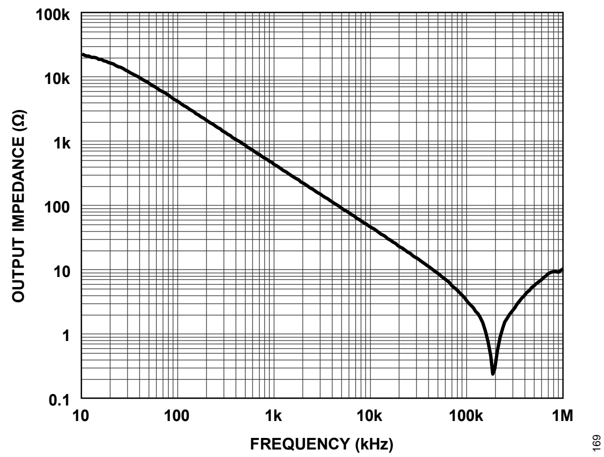

Figure 47. Output Impedance vs. Frequency, Disabled

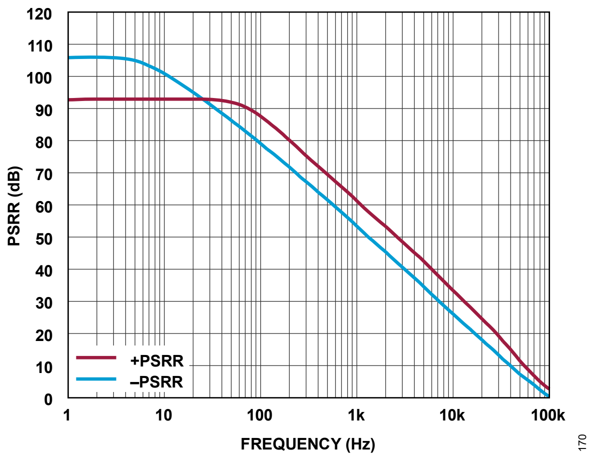

Figure 48. PSRR vs. Frequency, HVCC and HVEE, $V_S = \pm 50$ V

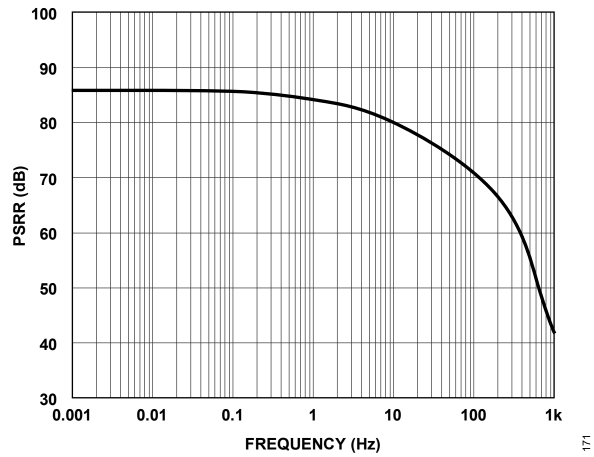

Figure 49. PSRR vs. Frequency, VCC_5V, VCC_5V = 5 V

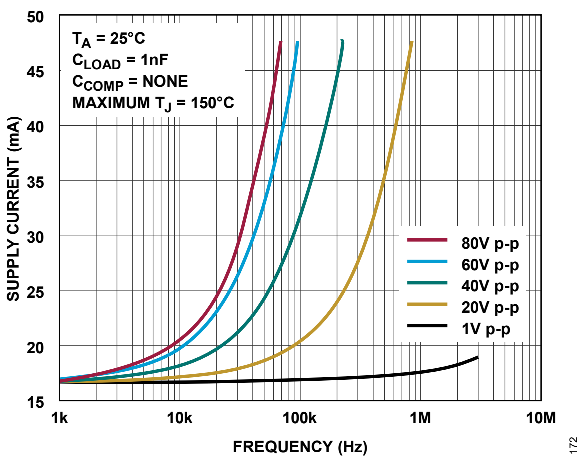

Figure 50. Supply Current and Amplitude vs. Frequency, Square Wave, No Heatsink, C_{LOAD} = 1 nF, C_{COMP} = None

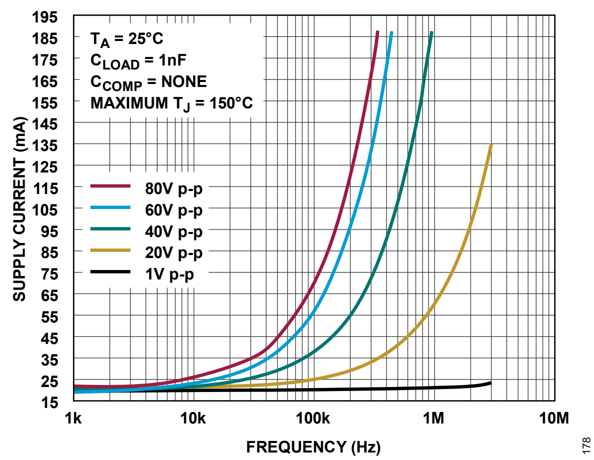

Figure 51. Supply Current and Amplitude vs. Frequency Square Wave, with Heatsink, C_{LOAD} = 1 nF, C_{COMP} = None

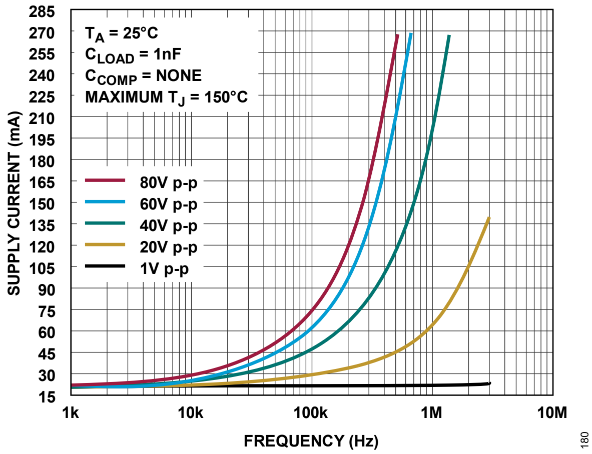

Figure 52. Supply Current and Amplitude vs. Frequency Square Wave, with Heatsink and Airflow, C_{LOAD} = 1 nF, C_{COMP} = None

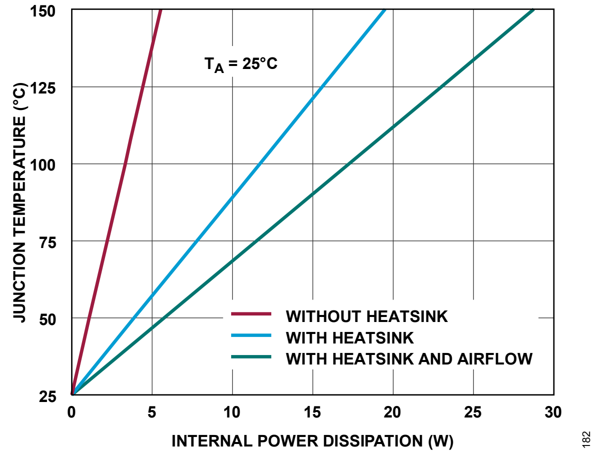

Figure 53. Junction Temperature vs. Internal Power Dissipation

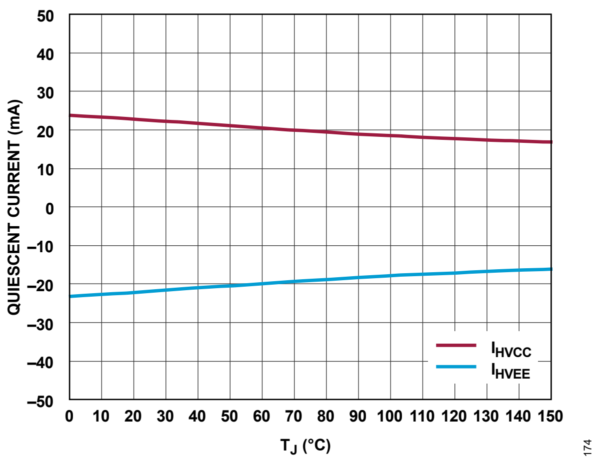

Figure 54. High Voltage Quiescent Supply Current vs. Temperature, V_S = ±50 V

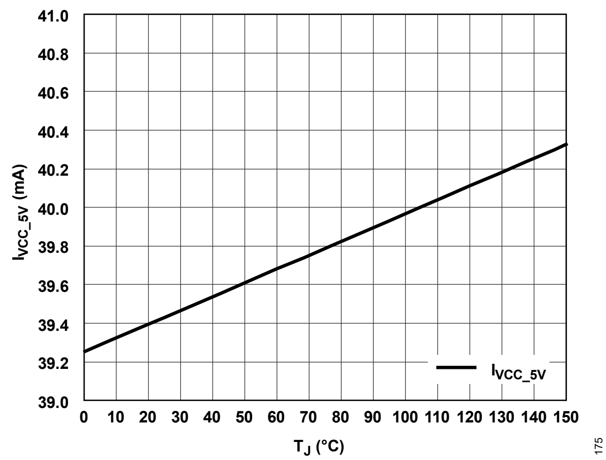

Figure 55. VCC_5V Quiescent Supply Current vs. Temperature, VCC_5V = 5 V

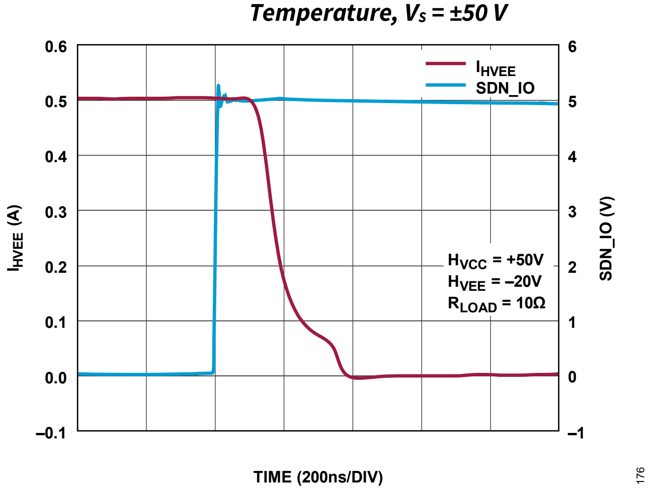

Figure 56. Shutdown Response vs. Time

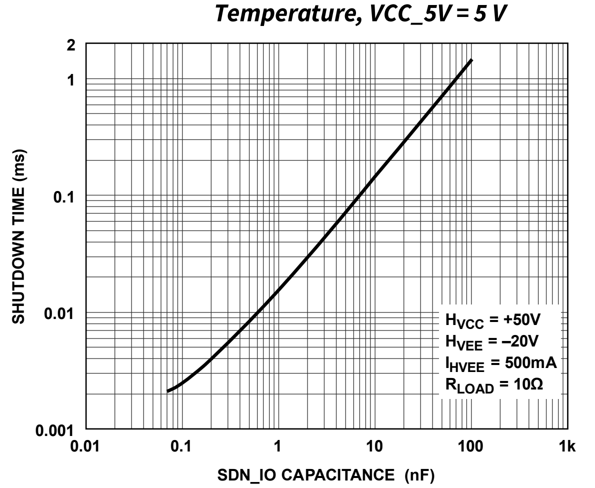

Figure 57. Shutdown Response vs. SDNIO Capacitance

TERMINOLOGY

Alarm

Alarm refers to the detection of any of the five fault conditions monitored by the protection system: overcurrent (sourcing or sinking), overvoltage (positive or negative), or overtemperature. The alarm flag is customizable to either self-clear upon fault clear, or latch the alarm state as evidence of fault occurrence. When any alarm is latched, it must be cleared.

Analog Pattern Generation (APG) Mode

The APG mode is analogous to the operation of a digital pattern generator. In the AD8460, an analog pattern of up to 16 sequential elements may be created, with each element containing an analog voltage rather than a digital voltage (logic state). Each analog voltage value is represented by 14-bit data. Voltage data is loaded serially through serial peripheral interface (SPI) into pattern memory prior to updating driver output. The APG mode is recommended for simple, repetitive waveforms consisting of sequential voltage levels.

Arbitrary Waveform Generation (AWG) Mode

The AWG mode is analogous to the operation of an arbitrary waveform generator. Digital data is presented in parallel fashion to the DAC and the driver output is updated synchronously with the data transfer, allowing waveforms to be created in real time. The AWG mode is recommended for complex or non-repetitive waveforms.

Arm

To arm the protection system is to put the driver into a mode where it detects an alarm condition and shuts down the device.

Disarm

To disarm the driver is to put it into a state where it ignores an alarm condition and does not shut down the device. Use extreme caution when the driver is disarmed as it is unprotected from faults and possible damage.

Fault

A fault is any of the five overload conditions detectable by the protection system. Any fault triggers an alarm, though an alarm must exist for some minimum (user-adjustable) duration to force a shutdown.

Protection System

The protection system comprises limit-setting DACs, comparators, and logic gates that detect faults according to user-specified limits. See *Figure 64* for a block diagram showing basic functionality.

Reserved

Reserved refers to internal registers not for user access.

Safe Operating Area (SOA)

The safe operating area is a two-dimensional envelope bounded by parameters the user must manage to prevent damage from overheating.

Shutdown and Sleep

Both shutdown and sleep refer to a state of inactivity characterized by floating (high impedance) output and greatly reduced power consumption. Shutdown may be initiated by the user, by pulsing SDN_IO high, or may be initiated by the protection system in response to an alarm of sufficient duration. If there is any parasitic or added capacitance to SDN_IO, wait until the SDN_IO voltage goes below its threshold voltage before trying to exit shutdown. To exit shutdown, use any of the following three ways:

- Pulse SDN_RESET high, then leave low.

- Pulse the HV_RESET bit high through two SPI commands (drive high, then drive low).
- Pulse SDN_IO low, then float.

Sleep refers to a non-latching state of inactivity like shutdown, but which is initiated (HV_SLEEP = 0) and terminated (HV_SLEEP = 1) through SPI commands. Sleep supersedes all commands that use the SDN_IO shutdown mechanism, both fault-initiated and user-initiated. See *Figure 64* for a logic diagram of the protection system and shutdown mechanism.

Slew Boost

Slew boost refers to a design feature of the AD8460 that increases supply current during fast input signal transitions, permitting faster output slew without the continuous power-dissipation penalty of conventional high-speed amplifiers.

Span

Span refers to the difference between the highest and lowest output values. The AD8460 has a nominal span of 80 V (+40 V - (−40 V)).

THEORY OF OPERATION

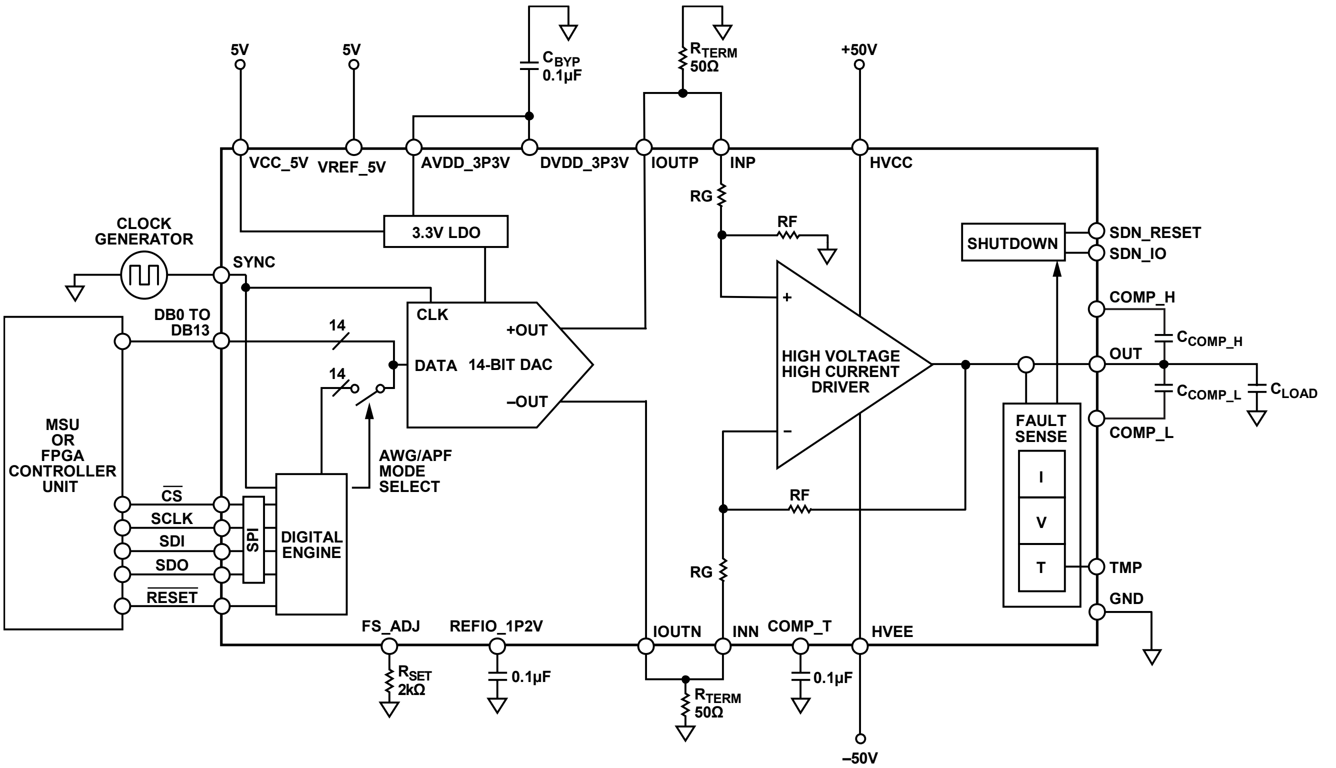

Figure 58. AD8460 Standard Configuration

Overview

The AD8460 is a "bits in, power out" high voltage, high-power, high-speed driver optimized for large output current (up to ±1 A) and high slew rate (up to ±1800 V/µs) at high voltage (up to ±40 V) into capacitive loads. Combining a 14-bit high-speed DAC, a high voltage, high output current (HV-HI) analog driver, and fault monitoring and protection circuits, the AD8460 is ideally suited for high power applications such as arbitrary waveform generation (AWG), programmable power supplies, and high voltage automated test equipment (ATE).

The input to the system is provided as a 14 bit digital DAC code. The part can either operate in the analog pattern generation (APG) or arbitrary waveform generation (AWG) mode. In the APG mode, SPI communication is used to write up to 16 levels into digital registers, and clocking SYNC updates the output, serially proceeding to each next level in the table. In the AWG mode, the DAC uses 14 parallel digital inputs DB0 to DB13, and clocking SYNC updates the output. See *INPUT AND MODE OF OPERATION* .

With configurable DAC parameters R_{SET}, V_{REFIO_1P2V}, and R_{TERM} = 50 Ω, the driver output transfer function is equal to:

$$V_{OUT} = \left(80\ V \times \left(\frac{DAC\ CODE}{2^{14}}\right) - 40\ V\right) \times \left(\frac{2\ k\Omega}{R_{SET}}\right) \times \left(\frac{V_{REFIO_{1P2V}}}{1.2\ V}\right)$$

Under conventional V_{REFIO_1P2V} = 1.2 V, R_{SET} = 2 kΩ, and R_{TERM} = 50 Ω, the driver output transfer function simplifies to:

$$V_{OUT} = \left(80\ V \times \left(\frac{DAC\ CODE}{2^{14}}\right) - 40\ V\right)$$

The maximum output swing is established by the internal DAC configuration. See *FULL-SCALE ADJUSTMENT*.

The AD8460 requires dual high voltage (up to ±55 V) power supplies at HVCC and HVEE, and a single low voltage (5 V) power supply at VCC_5V. The part generates 3.3 V internally from a LDO output at AVDD_3P3V, and DVDD_3P3V is an internal digital supply bypass point that should be connected to AVDD_3P3V. See *POWER SUPPLIES AND DECOUPLING*.

A reference of 5 V is required at VREF_5V to provide the reference voltage for analog low voltage and protection threshold DACs. Connect VREF_5V to an external 5 V reference or to VCC_5V (reduced accuracy). The AD8460 utilizes a reference of 1.2 V at REFIO_1P2V to provide the reference voltage for the high-speed DAC. Connect REFIO_1P2V to an external 1.2 V reference or float to use the internal 1.2 V reference, which can give rise to reduced accuracy. See *REFERENCE OPERATION*. An external resistor R_{SET} connected to FS_ADJ establishes the internal DAC's reference current I_{REF}. When R_{SET} = 2 kΩ, as in *Figure 58*, the DAC's full scale complementary output currents are set to the nominal value of 20 mA. See *FULL-SCALE ADJUSTMENT.*

The DAC and the high-voltage, high-current (HV-HI) output driver can be connected externally through pin IOUTP and INP on the high side, and pin IOUTN and INN on the low side. The termination resistors (R_{TERM}) set the inputs to the HV-HI driver. The R_{TERM} resistors are recommended to be high precision 50 Ω. The % tolerance on the R_{TERM} corresponds to possible error at the output. Typically, a tolerance of 0.1% is recommended in systems that balance precision and cost. 0.01% resistors are recommended for higher precision systems.

In addition to drive capability, the AD8460 provides a suite of features relating to fault monitoring and load protection. The part features a junction temperature monitor providing voltage at output indicating junction temperature up to 2.5 V at maximum junction temperature of 150 °C. The digital engine allows for programmable output current limit (source current and/or sink current), programmable output voltage limit (positive voltage and/or negative voltage), and programmable temperature limit (maximum junction temperature). See *SHUTDOWN PROTECTION SETTINGS*.

INITIAL POWER-UP

POWER SUPPLIES AND DECOUPLING

The AD8460 requires dual high voltage supplies in the range of ±12 V to ±50 V at HVCC and HVEE, as well as a single 5 V low voltage supply at VCC_5V. Bypass all supply pins to ground using high quality, low ESR 0.1 µF capacitors.

Place bypass capacitors as close to the supply pins as possible, with a short, direct connection to the PCB's analog ground plane. Additionally, place four 1.2 µF ceramic capacitors from each high voltage supply to ground to provide good low frequency bypassing, and to provide the needed current to support large, fast-slewing signals. Low-inductance planes are recommended for high voltage supply routing.

AVDD_3P3V is the analog supply bypass point for the internal 3.3 V LDO. AVDD_3P3V requires a 0.1 µF bypass capacitor from AVDD_3P3V to GND. Connect AVDD_3P3V to DVDD_3P3V.

VREF_5V

VREF_5V sets the reference voltage for internal alarm threshold DACs and needs to be biased. A precise 5 V reference IC is recommended. Alternatively, VREF_5V can be connected to VCC_5V (reduced accuracy).

A reduced accuracy VREF_5V reference shifts the internal LDO reference voltage and causes the SDN_IO shutdown voltage, overvoltage, and overtemperature thresholds to vary from table specified values. For example, if a 5 V reference with 1% tolerance at VREF_5V is utilized, these levels may vary 1% from typical values.

The order of VCC_5V and VREF_5V power-on affects the initial state of the HV-HI driver. See *POWER SUPPLY SEQUENCING*.

POWER SUPPLY SEQUENCING

DVDD_3P3V must be tied to AVDD_3P3V before power-up. The high voltage power supplies (HVCC and HVEE) and VCC_5V may be brought up individually, in any order.

AD8460 can be powered up in shutdown or active mode. Powering the AD8460 in shutdown mode is recommended and this can be accomplished by powering on VCC_5V before VREF_5V. After initial power-up in shutdown mode, the SDN_IO pin must be pulled low to ensure the AD8460 is turned on. Subsequently, floating the SDN_IO pin enables the fault monitoring and protection feature while the AD8460 remains on. When powering down, bring VREF_5V down first, then bring down VCC_5V.

If VCC_5V is powered on connected to VREF_5V, the part powers on with the driver enabled and DAC disabled. Use extreme caution when powering up in active mode as the output voltage can power on at high voltage. This may result in high output current.

REFERENCE OPERATION

The AD8460 internal DAC contains an internal 1.2 V band gap reference. The internal reference cannot be disabled, but can be easily overridden by an external reference for greater output accuracy. *Figure 59* shows a representative circuit of the band gap reference. Pin REFIO_1P2V serves as either an output or an input depending on whether the internal or an external reference is used. To use the internal reference, simply decouple the REFIO_1P2V pin to GND with a 0.1 µF capacitor. The internal reference voltage is present at REFIO_1P2V. If the voltage at REFIO_1P2V is to be used anywhere else in the circuit, an external buffer amplifier with an input bias current of less than 100 nA should be used. *Figure 60* shows an example of buffered internal reference configuration.

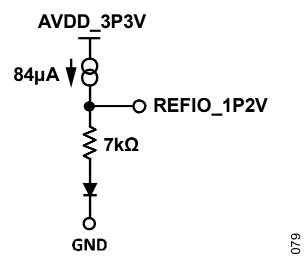

Figure 59. Representative Circuit of Internal Reference

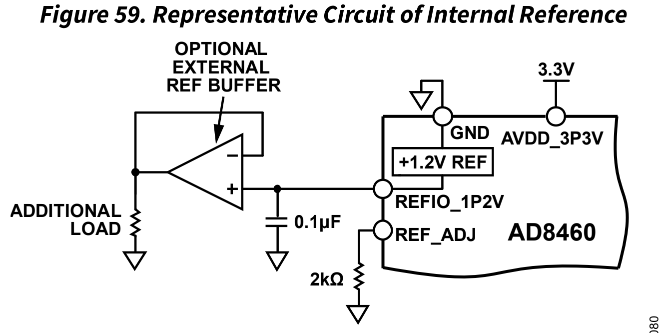

Figure 60. Buffered Internal Reference Configuration

An external reference can be applied to REFIO_1P2V, as shown in *Figure 61*. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1 µF compensation capacitor may not be required since the internal reference is overridden, and the relatively high input impedance of REFIO_1P2V minimizes loading of the external reference.

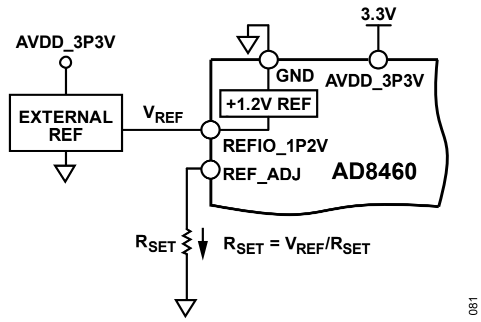

Figure 61. External Reference Configuration

INPUT AND MODE OF OPERATION

The AD8460 can generate waveforms in either the analog pattern generation (APG) or arbitrary waveform generation (AWG) mode.

The APG mode is used when the desired waveform is a series of sequential DC voltage levels, and edge speed control is not a requirement. In the APG mode, a pattern of up to 16 discrete DC voltage levels is loaded serially into pattern memory through the SPI. After a pattern is loaded, SYNC is used to clock pattern data to the output. 14-bit data is latched into the DAC on the rising edge of SYNC, and the data pointer advances to the next register on the subsequent falling edge. After the final value in pattern memory is sent to the DAC, the data pointer returns to the first data register and the pattern loops as long as SYNC is clocked. In the APG mode, the parallel data port (pins DB13:DB0) must be floated, as these pins are driven internally by the digital engine.

In the AWG mode, 14-bit digital input data representing the desired waveform is loaded through the parallel interface (pins DB13:DB0) and clocked in on the rising edge of SYNC, corresponding to conventional parallel mode high-speed DAC usage to update the output. The AWG mode is used when complex waveforms, specific edge speeds, or digital predistortion are required. *Table 7* briefly compares the APG and AWG input modes.

Table 7. Comparing the APG and AWG Input Modes

Mode	Input Type	Output Waveform	Adjustable Edge Speed	Pre-distortion
APG	Serial through SPI	Pulses	Limited to 16 levels	Limited to 16 levels
AWG	Parallel	Complex waveforms	Yes	Yes

ANALOG PATTERN GENERATION (APG)

To enable the APG mode, set the APG_MODE_ENABLE bit to (1) in the CTRL_REG_02 register and then set WAVE_GEN_MODE bit to (1) in the CTRL_REG_00 register.

The pattern is generated in non-real time and data is loaded serially through SPI into pattern memory prior to updating the driver output. The SYNC signal loads the DAC input on its rising edge based on the values in the pattern memory in the HVDAC_DATA_REGMAP and updates the driver output on its falling edge. The pattern loops if SYNC is pulsed. The maximum SYNC rate for APG mode is 20 MHz.

In HVDAC_DATA_REGMAP, each 14 bit level is stored in a combination of two 8 bit registers, containing the low order byte and high order byte. For example, the first level in the pattern is stored in HVDAC_DATA_BYTE_00 and HVDAC_DATA_BYTE_01, If the first level is 14 bit binary sequence $b_{13}b_{12}b_{11}b_{10}b_9b_8b_7b_6b_5b_4b_3b_2b_1b_0$, HVDAC_DATA_BYTE_00 contains the 8 low order bits (binary $b_7b_6b_5b_4b_3b_2b_1b_0$), and HVDAC_DATA_BYTE_01 contains the 8 high order bits (binary $b_\emptyset b_\emptyset b_{13}b_{12}b_{11}b_{10}b_9b_8$), where the first two bits are reserved. The second level in the pattern is stored in HVDAC_DATA_BYTE_02 and HVDAC_DATA_BYTE_03, and so forth.

The default pattern memory value produces a 4-level, ±20 V up-down sequential staircase waveform at a frequency defined by the SYNC clock rate, as shown in *Figure 62*. These default values may be overwritten through SPI. The APG mode generates analog pattern of up to 16 sequential voltage levels. The pulse width for each voltage level is defined by the SYNC clock rate and can be calculated by:

$$Pulse\ Width = \frac{\frac{1}{SYNC\ Clock\ Rate}}{\#\ of\ Sequential\ Voltage\ Levels}$$

Assume the SYNC clock rate is 1 MHz and the output is a 2-level sequential pulse, the pulse width is:

$$Pulse\ Width = \frac{\frac{1}{1\ MHz}}{2} = 0.5\ \mu s$$

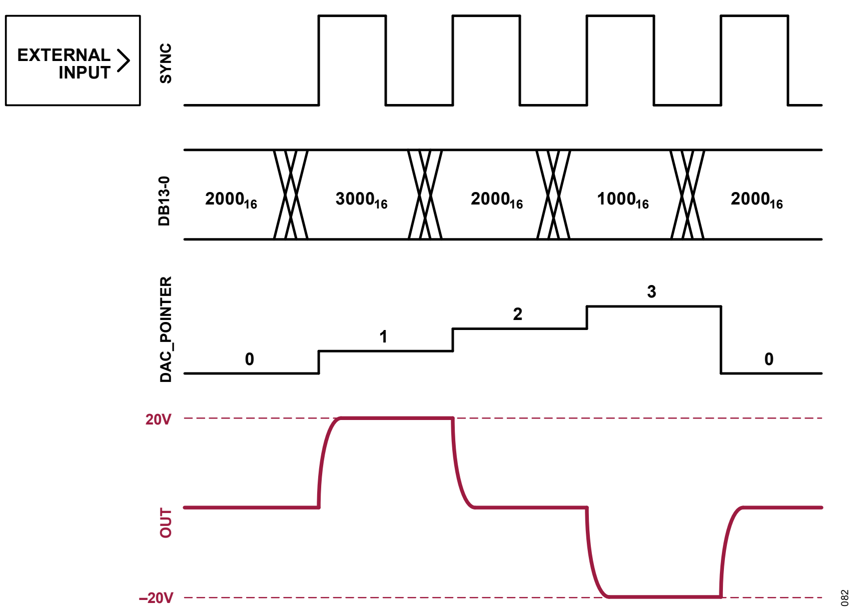

Figure 62. APG Mode Reference Example

ARBITRARY WAVEFORM GENERATION (AWG)

The AD8460 powers on by default in the AWG mode.

Clear the APG_MODE_ENABLE bit to 0 in the CTRL_REG_02 register and clear the WAVE_GEN_MODE bit to 0 in the CTRL_REG_00 register to select the AWG mode. The waveform is generated in real-time and data is loaded into registers through the parallel data port. The SYNC signal loads the HVDAC on its rising edge and updates the driver output on its falling edge. The maximum SYNC rate for the AWG mode is 100 MHz.

In the AWG mode, operation is essentially that of a high-speed DAC. The user provides 14-bit parallel data to pins DB0 to DB13 and provides a SYNC clock. Data is usually provided through the user field-programmable gate array (FPGA).

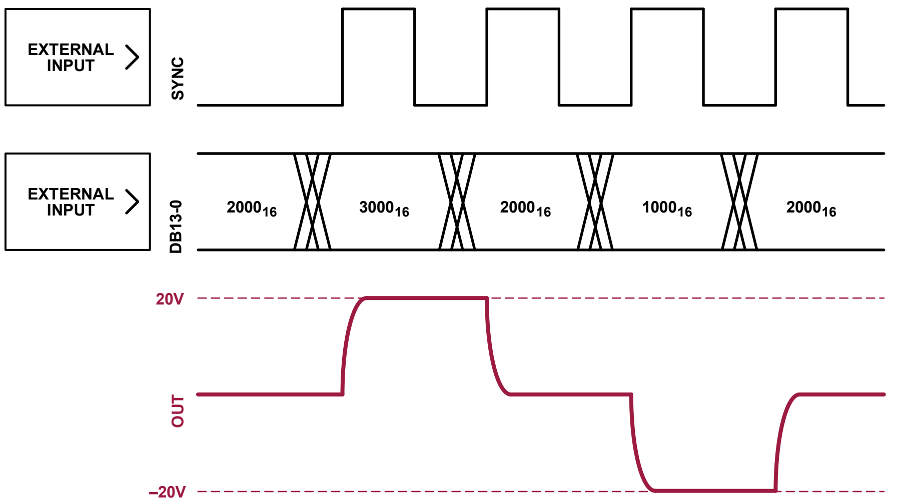

Figure 63. AWG Mode Reference Example

PREDISTORTION AND ADJUSTABLE INPUT EDGE SPEED

Capacitive loading, cable length, and edge speed may produce distortion in the AD8460's transient settling characteristic, such as overshoot and ringing. The AWG mode allows the users to modify the waveform data to minimize this distortion. The modifications include adding an inverse characteristic to improve the shape of the response or adjusting the input edge to a slower speed.

The predistortion feature creates an input waveshape with undershoot, which can be used to compensate the overshoot for a given load. While this can be done in both the AWG and APG modes, the AWG mode provides higher resolution and therefore better distortion cancellation in all but the simplest waveforms.

In the AWG mode, it is possible to provide input data to the DAC at a higher sample rate, using a faster SYNC clock than is available in the APG mode. This allows the user to shape the input edges to smaller steps. By increasing the steps width, the user can adjust the input edge speed to any user-specified value. A slower edge speed reduces overshoot on a given cap load.

The number of steps needed during an edge event is calculated by Eq. 1:

$$n_{STEPS} = \frac{AMPLITUDE_{P-P}\ (V) \times f_{SYNC}\ (MHz)}{EDGE\ SPEED\ \left(\frac{V}{\mu s}\right)} \quad \text{(Eq. 1)}$$

For a 100 MHz clock and a step of 80 V, 100 steps are needed. To produce a linear output, the number of bits per step is $\lfloor 2^{14}/n_{STEPS} \rfloor$, in this case 163. A state machine can be implemented in HDL to control an edge event, or the edge may be a part of a longer pattern of codes. Examples of edge speed can be found in *Figure 12* in the *Typical Performance Characteristics* section.

OUTPUT CURRENT DRIVE

The AD8460's output stage is constructed with cascoded, double diffused, metal-oxide-semiconductor (DMOS) high voltage transistors and is optimized for high currents into capacitive loads. It is designed to generate edge speeds of up to 1800 V/µs and deliver ±1 A continuously with proper thermal management. The default heatsink for AD8460 is Wakefield-Vette P/N 518-95AB and active cooling is preferred for higher power dissipation applications. See *Thermal Management* for thermal related details.

The AD8460's protection system is highly configurable to suit a wide variety of applications. To provide maximum flexibility across applications, the AD8460 integrates independent monitoring of output current (sourcing and sinking), output voltage (positive and negative), and die temperature, providing protection for the driver and its load against five individual faults. See *FAULT MONITORING AND PROTECTION* for details.

The AD8460 is configured with protection features disabled by default. Use SPI to enable and program the protection features. For manual overtemperature shutdown, tie SDN_IO pin to TMP. The shutdown response time can be adjustable through a capacitor on SDN_IO pin. See *SHUTDOWN CONTROL (SDN_IO)* for delayed shutdown and manual thermal shutdown.

FAULT MONITORING AND PROTECTION

Fault monitoring and protection are implemented by setting thresholds and arming the protection system for each fault type individually. Thresholds are programmed through SPI for the desired protections to be implemented. Exceeding a programmed threshold triggers an alarm and shuts down the AD8460. *Figure 64* shows the control logic for the fault monitoring and protection.

Each of the five monitored faults has four digital registers associated with it:

1. A programmable threshold. The threshold can be programmed through register 0x08 (CTL_REG_08) through 0x0C (CTL_REG_12), bit [6:0]. See *SHUTDOWN PROTECTION SETTINGS* for ranges and resolutions settings.
2. ARM. The ARM can be programmed through register 0x08 (CTL_REG_08) through 0x0C (CTL_REG_12), bit [7]. Setting the corresponding ARM to (1) directs the protection system to shut down in response to an alarm. Setting the corresponding ARM to (0) disarms the protection system, inhibiting shutdown in case of an alarm. There is no protection from faults when ARM is (0).
3. ALARM indicator flags. ALARM indicator flags can be read and cleared through register 0x0E (CTRL_ REG_14). ALARM indicator flags are set to (1) by the protection system if a fault occurs while the protection system is armed. ALARM remains at (1) for as long the fault condition persists and returns to (0) when the fault condition clears. If the ALARM forces a shutdown of the driver, the driver remains in shutdown even if the fault condition clears and the ALARM flag resets. The ALARM bits indicate the status of the fault conditions. Once the ALARM clears, it may not be possible to determine what fault(s) occurred previously. See the ALARM_LATCH function for transient faults detections. To clear an ALARM indicator flag, write a (1) to the respective ALARM register bit.
4. ALARM_LATCH is set by the user to latch any ALARM flag, preserving evidence of any transient fault that may occur. ALARM_LATCH can be programed through register 0x0D (CTRL_REG_13). When an ALARM_LATCH is enabled and when an ALARM indicator flag is triggered, the ALARM indicator flag remains even if the associated fault condition clears. This is helpful in identifying transient faults. To clear an ALARM_LATCH flag, write a (0) to the respective ALARM_LATCH register bit.

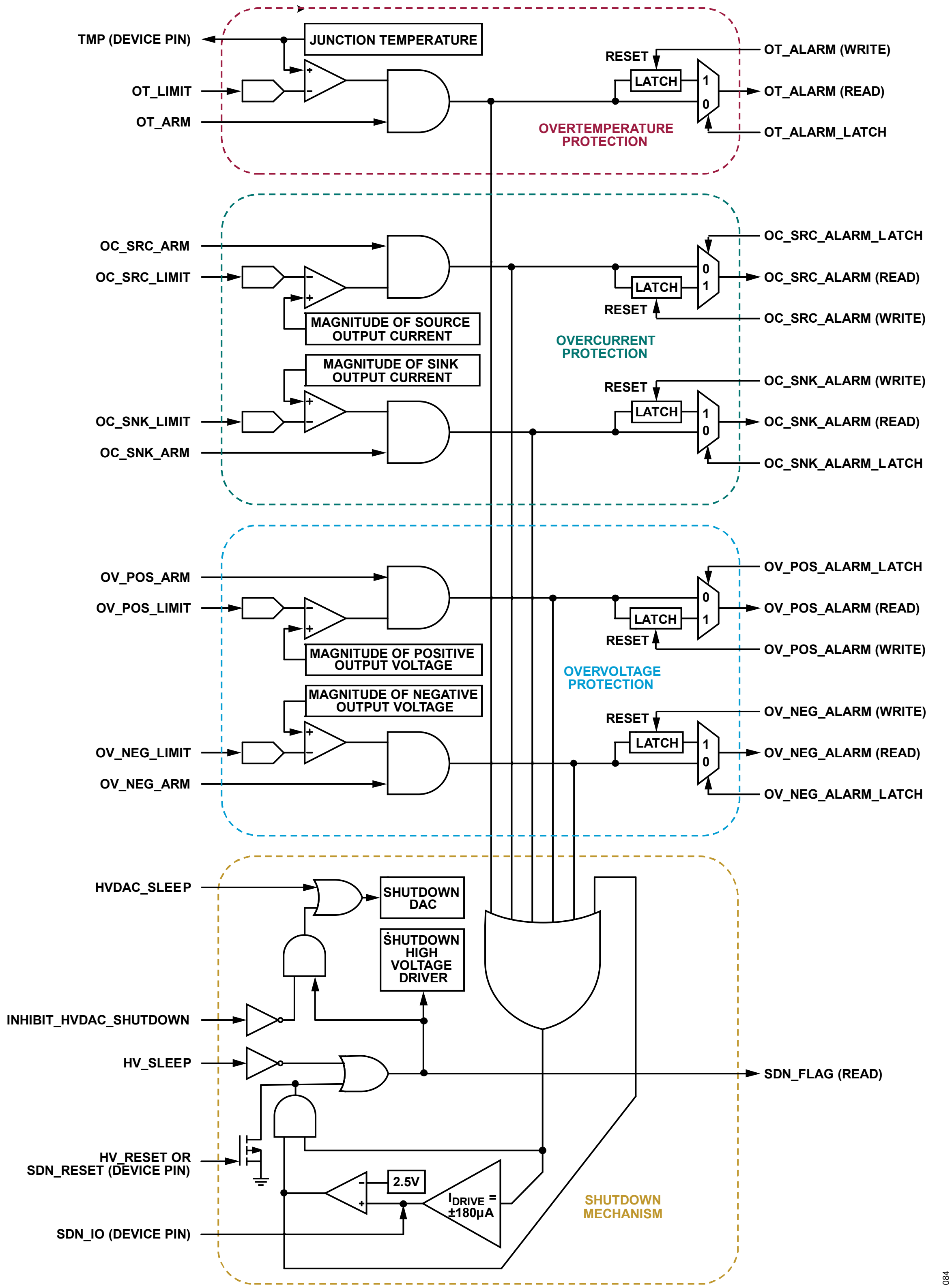

Figure 64. Fault Monitoring and Protection Control Logic

FAULT-INITIATED SHUTDOWN PROTECTION FEATURES

The AD8460 is equipped with a power saving shutdown feature through SDN_IO. The shutdown can be either user-initiated to reduce power dissipation or fault-initiated by AD8460's protection system to prevent part damage. See *SHUTDOWN CONTROL (SDN_IO)* for user-initiated shutdown details. The AD8460 monitors five operating conditions internally and may be configured to shut down if any programmable alarm limit is exceeded:

- Sourcing overcurrent limit (to +1 A)
- Sinking overcurrent limit (to −1 A)
- Positive overvoltage limit (to +55 V)
- Negative overvoltage limit (to −55 V)
- Junction overtemperature limit (T_J = 20°C to T_J = 150°C)

See *Table 24* through *Table 28* or register addresses assigned to these limits.

Any of the five internal fault monitors latch the SDN_IO pin high if an alarm condition is detected. The latch condition persists until the fault condition is cleared and the AD8460 is re-enabled.

To re-enable the driver after shutdown, pulse the HV_RESET bit high through two SPI (drive high, then drive low). The AD8460 can also be re-enabled by pulsing SDN_RESET high, then leaving it low or pulling SDN_IO low and then floating the SDN_IO pin. This re-enables the fault monitoring and protection. The digital resource used to pulse SDN_IO low must be capable of driving ~180 µA to override SDN_IO's high state. See *SHUTDOWN CONTROL (SDN_IO)* for details.

SHUTDOWN PROTECTION SETTINGS

The code range for the shutdown protection features exceeds the device's operational range; the range is selected to optimize linearity and accuracy at the limitations of the part, where shutdown control is most critical. It should be noted that the values from *Table 9* to *Table 11* are rounded values to trigger at values that are smaller than the desired trigger point and are not the exact values based on the conversion factor from the code to threshold value.

Table 8 shows the shutdown ranges and resolutions.

Table 8. Shutdown Protection Ranges and Resolution

FAULT TYPE	NOMINAL RANGE	NOMINAL RESOLUTION
Overcurrent	±1 A	15.625 mA
Overvoltage	±55 V	1.953V
Overtemperature	Up to TJ = 150°C	6.51°C

PROGRAMMING OVERCURRENT PROTECTION

The threshold programming resolution (1 LSB) for overcurrent protection is nominally 15.625 mA.

To convert code to current threshold:

$$Current\ Threshold\ (mA) = Code_{Decimal}(LSB) \times 15.625 \left(\frac{mA}{LSB}\right)$$

To convert current to code:

$$Code_{Decimal}(LSB) = \frac{15.625 \left(\frac{mA}{LSB}\right)}{Current\ Threshold\ (mA)}$$

If the user converts the desired current into a code in decimal, round down the calculated value to the nearest integer. Plug the integer value back into the code-to-current-threshold equation to determine the actual temperature threshold value.

See *Table 9* for typical threshold codes tied to common operating currents.

See the *PROGRAMMING SHUTDOWN THRESHOLD SETTINGS* on how to properly program the shutdown threshold settings.

Table 9. Typical Threshold Codes for Operating Currents

BINARY CODE	HEXADECIMAL VALUE	DECIMAL VALUE	CURRENT (mA)
0000011	0x03	3	50
0000110	0x06	6	100
0010011	0x13	19	300
0100000	0x21	32	500
1000000	0x40	64	1000

PROGRAMMING OVERVOLTAGE PROTECTION

The threshold programming resolution (1 LSB) for overvoltage protection is nominally 1.953 V.

To convert code to voltage threshold:

$$Voltage\ Threshold\ (V) = Code_{Decimal}(LSB) \times 1.953\left(\frac{V}{LSB}\right)$$

To convert voltage to code:

$$Code_{Decimal}(LSB) = \frac{1.953\left(\frac{V}{LSB}\right)}{Voltage\ Threshold\ (V)}$$

If the user converts the desired voltage into a code in decimal, round down the calculated value to the nearest integer. Plug the integer value back into the code-to-voltage-threshold equation to determine the actual temperature threshold value.

See *Table 10* for typical threshold codes tied to common operating voltages.

See the *PROGRAMMING SHUTDOWN THRESHOLD SETTINGS* section on how to properly program the shutdown threshold settings.

Table 10.Typical Threshold Codes for Operating Voltages

BINARY CODE	HEXADECIMAL CODE	DECIMAL CODE	VOLTAGE (V)
0000101	0x05	5	10
0001010	0x0A	10	20
0001111	0x0F	15	30
0010100	0x14	20	40

BINARY CODE	HEXADECIMAL CODE	DECIMAL CODE	VOLTAGE (V)
0011100	0x1C	28	55

PROGRAMMING OVERTEMPERATURE PROTECTION

The threshold programming resolution (1 LSB) for overtemperature protection is nominally 6.51°C.

To convert code to temperature:

$$Temperature\ Threshold\ (°C) = Code_{Decimal}(LSB) * 6.51 \left(\frac{°C}{LSB}\right) - 266.64\ (°C)$$

To convert temperature to code:

$$Code_{Decimal}(LSB) = Temperature\ Threshold\ (°C) + \frac{266.64\ (LSB)}{6.51 \left(\frac{°C}{LSB}\right)}$$

If the user converts the desired temperature into a code in decimal, round down the calculated value to the nearest integer. Plug the integer value back into the code-to-temperature equation to determine the actual temperature threshold value.

See *Table 11* for typical threshold codes tied to common operating temperatures.

See the *PROGRAMMING SHUTDOWN THRESHOLD SETTINGS* section on how to properly program the shutdown threshold settings.

Table 11.Typical Threshold Codes for Operating Temperatures

BINARY CODE	HEXADECIMAL VALUE	DECIMAL VALUE	KELVIN TEMPERATURE	CELSIUS TEMPERATURE
0101100	0x2C	44	293	20
0110110	0x36	54	358	85
0111001	0x39	57	377	104
0111011	0x3B	59	396	123
1000000	0x40	64	423	150

PROGRAMMING SHUTDOWN THRESHOLD SETTINGS

The register map in *Table 18* shows that the 8-bit registers, CTRL_REG_08 through CTRL_REG_12, are used to arm the five internal fault monitors and program the desired threshold value. For these internal fault monitoring registers, bit 7 is used for toggling the protection feature on or off, and bits [6:0] are used for setting the alarm threshold. It is important to note that the binary codes in *Table 9* to *Table 11* are bits [6:0] when programming the registers for fault monitoring and does not include bit 7 in the calculations.

Follow the order of the subsequent steps to properly program threshold settings into the internal fault monitoring registers and turn on each fault monitoring feature:

- Program bits [6:0] with the desired threshold code.
- Program bit [7] to a value of a (1) to enable protection and rewrite to bits [6:0] with the desired threshold code again.

SHUTDOWN CONTROL (SDN_IO)

The HV-HI output driver is disabled when SDN_IO is high. As directed in the power-up section, it is recommended to power-up with SDN_IO high so that the output driver is in shutdown mode and then bringing SDN_IO low once the desired AD8460 configuration is written over SPI. Subsequently, floating the SDN_IO pin enables the fault monitoring and protection feature while the AD8460 remains on. SDN_IO sinks ~180 µA to override SDN_IO's high state.

When SDN_IO is floated, the driver is controlled by SPI commands. SDN_IO has both input and output functionality. The user can drive the SDN_IO pin to enable/disable the amplifier or monitoring the SDN_IO. When SDN_IO is floated or connected to a high impedance digital pin such as a microcontroller GPIO, SDN_IO serves as a flag for any of the internal alarm conditions.

When SDN_IO is pulled high, the AD8460's HVCC and HVEE supply currents are reduced to ~120 µA and the internal high voltage driver is disabled. The output goes to high impedance (~27 kΩ). The shutdown state is latched and the driver remains in shutdown even when SDN_IO is floated. To enable the AD8460 from shutdown, pulling SDN_IO low and following by floating the SDN_IO is required to enable the shutdown protection features.

When SDN_IO is held low, the output is continuously enabled, and shutdown is inhibited. Use caution in this case as the device is unprotected from overstress. Holding SDN_IO low disables the shutdown protection features.

DELAYED SHUTDOWN

The user may add delay to the AD8460's shutdown response time to improve noise immunity, by means of an external capacitor from SDN_IO to ground. The capacitor value is chosen so that the desired delay equals the time required for the voltage on SDN_IO to ramp from 0 V to its threshold voltage of 2.5 V under a constant current of 180 µA. The capacitor value C_{SDNIO} is calculated according to the relationship:

$$C_{SDNIO} = \frac{(180\ \mu A \times t)}{2.5\ V}$$

where, t is the desired delay time.

Note: The chosen delay applies to all internally-detected alarms (current, voltage, and temperature).

For example, to add a 5 µs delay so that short duration current or voltage spikes do not cause a shutdown, a capacitor is needed between SDN_IO and ground, with value:

$$C_{SDNIO} = \frac{(180\ \mu A \times 5\ \mu s)}{2.5\ V} = 360\ pF$$

Note that parasitic capacitance on the PCB impacts the shutdown response time. The values seen in *Figure 65* are the total capacitance on the SDN_IO pin, which includes the PCB's parasitic capacitance and added capacitor. In this example, any alarm condition shorter than 5 µs in duration does not trigger a shutdown. *Figure 65* shows the AD8460's shutdown response time vs. various capacitance.

Alarm latching is particularly useful when delayed shutdown is implemented. In the previous example, a fault of less than 5 µs duration does not trigger a shutdown, but the occurrence of a fault may be of interest for troubleshooting purposes. When the ALARM_LATCH is true (1), the states of the corresponding ALARM flags may be polled through SPI to see if any faults are detected, even if the event is too short to force a shutdown.

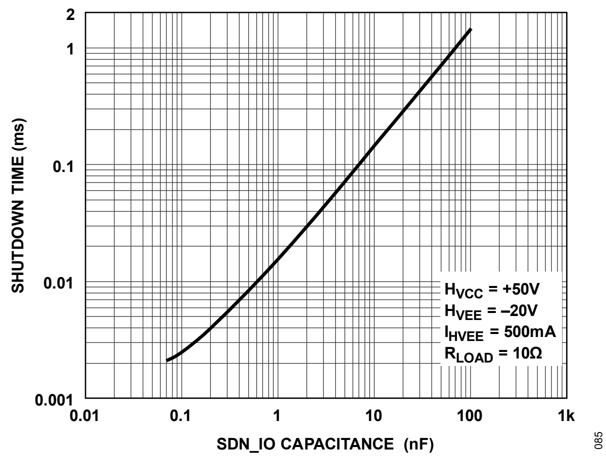

Figure 65. Shutdown Response Time vs. Various C_{SDN_IO}

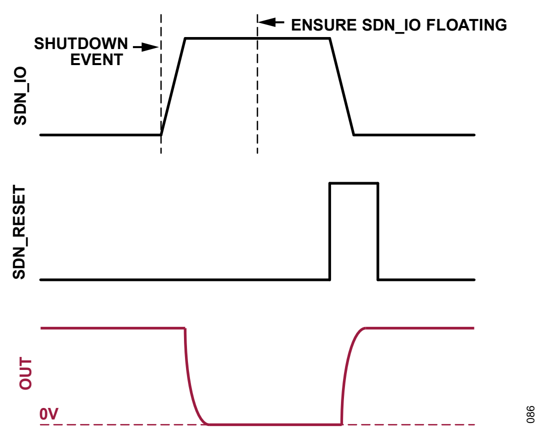

Figure 66. Shutdown Response Sequence

MANUAL THERMAL SHUTDOWN

The AD8460 features an optional manual thermal shutdown at T_J = 150 °C without the need for SPI communication and programming. This manual shutdown feature is only valid for thermal shutdown. The overcurrent and overvoltage protection still require SPI communication and programming.

To enable the manual thermal shutdown, tie TMP directly to SDN_IO, as shown in *Figure 67.* In this configuration, the TMP pin's analog output voltage reaches the SDN_IO's logic high threshold at approximately T_J = 150 °C, activating shutdown mode. The AD8460 does not self-reset when the die temperature has cooled below 150 °C. The AD8460 remains in shutdown until resequencing the power supplies or the SDN_IO pin.

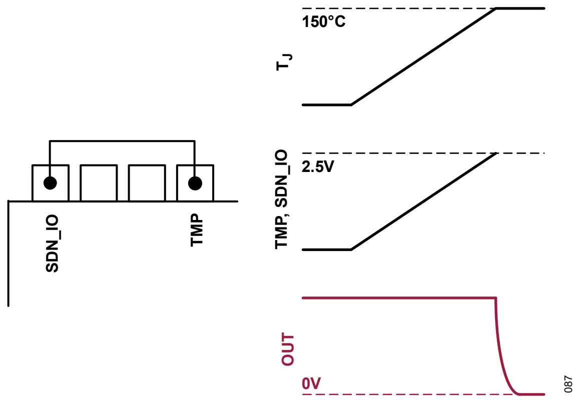

Figure 67. TMP and SDN_IO pin Configuration for Manual Thermal Shutdown

POWER ON RESET (POR) AND $\overline{\text{RESET}}$

The AD8460 executes a digital reset upon power-on. Power-on-reset (POR) resets all digital registers to default, including all alarm thresholds while powering-on the AD8460. The protection system is inactive upon power-on by default. Use caution in operating the device before any alarm thresholds are set and the protection system is enabled. Reset to defaults can also be commanded at any time through the SOFT_RESET register bit. See *Table 22* for more information on SOFT_RESET.

The default power-on configuration is:

- Driver output enabled
- Protection system disabled
- Waveform generation mode set to AWG
- Simple demonstration pattern loaded in pattern memory
- Nominal quiescent current
- DAC in shutdown

Manual POR can be achieved by pulling $\overline{\text{RESET}}$ LOW and then HIGH, which resets all the digital registers to default.

SLEEP CONTROL AND OTHER REGISTER RELATED FEATURES

SLEEP CONTROL

HV_SLEEP: Setting the HV_SLEEP register (0x00, bit 4) LOW puts the high voltage driver into sleep mode. The HVCC and HVEE supply currents drop to ~120 µA and OUT goes to a high impedance state (~27 kΩ). The sleep mode is initiated through SPI command only. Setting the HV_SLEEP register bit HIGH restores the driver to its active state. Note that the output stage is high impedance in the sleep mode. When driving a capacitive load, the output voltage drifts as the load capacitor discharges.

HVDAC_SLEEP: This register allows the user to shut down the HVDAC to save power. The VCC_5V supply currents drop to 10.5 mA, and the HVCC and HVEE supply currents drop to 120 µA. HVDAC_SLEEP permits a modest amount of additional power savings over HV_SLEEP alone when in sleep mode. The HVDAC is in sleep mode by default at initial power-on or start-up.

INHIBIT_HVDAC_SHUTDOWN: By default, the HVDAC shuts down with the HV driver when a shutdown is commanded. INHIBIT_ HVDAC_SHUTDOWN allows the option to keep the HVDAC powered-up in the event of a shutdown command.

OTHER FEATURES

Other features implemented in the AD8460 that may be useful in certain applications are:

- CHIP_ID: This read-only register contains the code 0x46.
- DIE_REV: This 4-bit read-only register contains the code 0x4.

SLEW BOOST

The AD8460's output amplifier employs a slew boosting architecture to enhance high-speed signal fidelity. Slew boost is a variable-enhancement mechanism that increases quiescent current in proportion to the instantaneous differential voltage sensed at the inputs to the operational amplifier within the HV driver. As with any voltage-feedback operational amplifier, the inputs are kept very nearly equal through negative feedback. In cases where the output is unable to keep up with a rapidly changing input (disrupting the feedback loop), the inputs momentarily begin to move apart. This differential signal induces the slew boost circuit to increase supply current, allowing the output to slew faster, and restores the disrupted feedback signal.

The additional current is typically needed for about 50 ns to 100 ns but increases power dissipation significantly during that time. The amount of additional self-heating that occurs as a result of this depends on the signal dynamics. For instance, for a 100 kHz square wave with a period of 10 µs, the slew boost is only active for 1% of the waveform's period, resulting in a small increase in overall power dissipation.

The dynamic safe operating area (SOA) is shown in the *SAFE OPERATING AREA* section. The dynamic SOA shows the connection between the output swing and the maximum input/output frequency for a pulse response. If slew-boost is activated frequently, as a high-frequency square wave might require, power dissipation increases dramatically and may push the device outside its dynamic SOA. To expand the dynamic SOA curve, use additional thermal management or limit the input/output edge speed, which limits the current produced by the slew boosting circuit and reduces the internal power dissipation.

THERMAL MONITORING (TMP)

Monitoring die temperature in the AD8460 is accomplished by measuring its TMP pin voltage relative to GND. This pin's analog output voltage is proportional to die temperature and is converted to degrees Celsius using the formula:

$$T\ (^{0}C) = \frac{(VTMP - 1.6\ V)}{6\,\frac{mV}{°C}}$$

More precise temperature readings can be achieved through a one-time room temperature calibration of the TMP pin.

The AD8460's thermal monitoring capability is independent of any overtemperature shutdown threshold and may be used whether or not TMP is strapped to SDN_IO. Note: If TMP is monitored while strapped to SDN_IO, a high impedance must be maintained by the user's monitoring circuit so that loading does not interfere with the shutdown function. Failure to maintain a high impedance on SDN_IO may result in damage to the AD8460 by inhibiting thermal shutdown.

OUTPUT COMPENSATION (COMP_H AND COMP_L)

Pulse response may be optimized for different capacitive loads by means of the COMP_H and COMP_L pins. Place a capacitor from both COMP_H to OUT and COMP_L to OUT to reduce overshoot in the step response. See *Figure 68* and *Figure 69* for information on selecting the compensation capacitors. Note that these must be high voltage types to withstand the full-scale range of the output signal; minimum 100 V capacitors are recommended when running on the nominal ±50 V supplies. If supplies are brought up to ±55 V, the minimum voltage rating of capacitors used needs to be increased to 110 V accordingly.

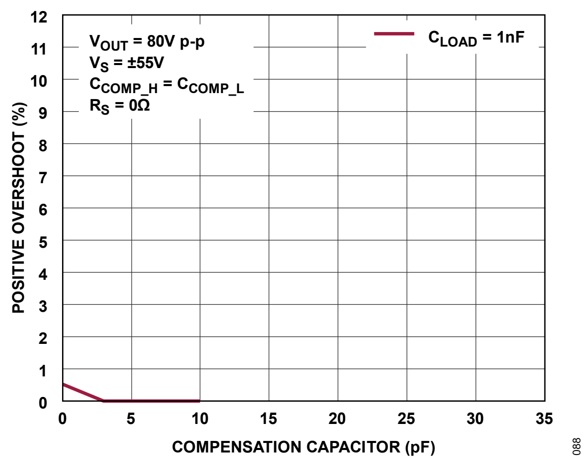

Figure 68. Large Signal Pulse Response Overshoot vs. C_{LOAD} and C_{COMP}, Positive Overshoot

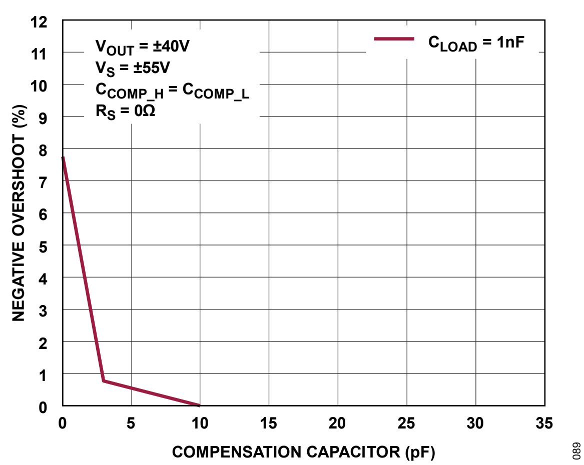

Figure 69. Large Signal Pulse Response Overshoot vs. C_{LOAD} and C_{COMP}, Negative Overshoot

THERMAL COMPENSATION (COMP_T)

Place a 0.1 µF capacitor from COMP_T to ground. This compensation capacitor is required for stable output of TMP as junction temperature monitor.

PROGRAMMABLE QUIESCENT CURRENT

Quiescent power dissipation may be reduced for applications that do not require maximum dynamic performance. Programming reduced supply current lowers power dissipation and lowers junction temperature at the expense of speed, slew rate, settling time, capacitive load drive, and noise.

This feature is controlled in CTRL_REG_04: SET_IQ and allows for adjusting the supply current up or down relative to the nominal supply current. The MSB sets the polarity of the supply current adjust: (0) is a decrease in supply current, whereas (1) is an increase in supply current. The remaining bits [6:0] are a monotonic but nonlinear control of the supply current across the span of codes. From SET_IQ = 0x00, the part is at nominal supply current, bits [6:0] can be increased up to limit SET_IQ = 0x7F, where the part sees zero supply current, resulting in quiescent current starved shutdown. From SET_IQ = 0x80, the part is again at nominal supply current, and bits [6:0] can be increased up to SET_IQ = 0xFF, where the part is at roughly double the nominal supply current. Exercise extreme caution if increasing supply current, noting the thermal effects of the increased supply current, where self-heating can increase junction temperature and must be monitored appropriately.

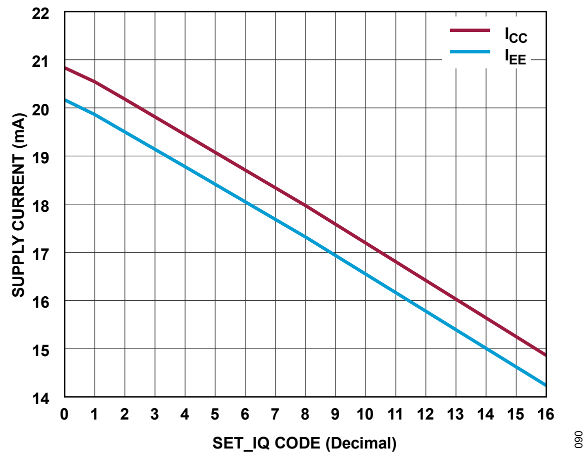

Figure 70. Quiescent Current vs. Code

APPLICATIONS INFORMATION

Thermal Management

PCB Thermal Design

The AD8460's innovative EPAD-up package greatly reduces thermal management constraints on the PCB layout. Conventional EPAD-down packages require copper-filled vias or expensive solid copper coins pressed into the PCB for thermal conduction to a heat sink on the underside of the board. EPAD-up allows the heat sink to be mounted to the top of the AD8460, freeing up component space on the secondary side of the PCB, and eliminating the need for through-board thermal relief. Four small mounting holes are needed to secure the recommended heat sink to the PCB, and these are located outside of the AD8460's immediate area. Component heights on the primary side of the PCB in the area beneath the heat sink must be smaller than the minimum height of the AD8460, as illustrated in *Figure 71*.

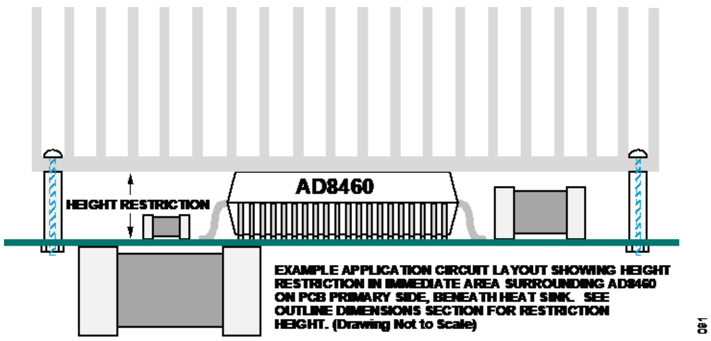

Figure 71.Component Height Restriction Beneath Heat Sink

To maximize heat transfer, attach the heat sink to the EPAD, as shown in *Figure 71*, using a high conductivity thermal interface material (TIM).

POWER DISSIPATION

Under quiescent conditions and maximum supply voltage, with the default heat sink, the AD8460 dissipates ~2.475 W, which produces a 15.84 °C rise over ambient temperature.

Under heavier loading conditions, the increase in die temperature is greater. It is recommended that T_J be continuously monitored at the TMP pin to manage die temperature under different internal power dissipation levels. Alternatively, when operating at a constant power level, die temperature can be estimated based on the package's θ_{JA} of 22.6 °C/watt when operating without a heatsink. Where the thermal setup of the AD8460 utilizes a heatsink, one should expect to have a junction-to-ambient thermal resistance θ_{JA_SYSTEM} (with recommended heatsink Wakefield-Vette P/N 518-95AB and TIM GC Electronics type Z9 heat sink compound) of 6.4°C/watt. The following equation is the basic formula used for calculating junction temperature for a specific power dissipation and ambient temperature.

$$T_J = \theta_{JA\_SYSTEM} * P_{DISS} + T_A$$

For example, if dissipating 10 W internally at an ambient temperature of 25 °C with a heatsink and TIM in the thermal stackup for the EVAL-AD8460SDZ, T_J can be expected to climb to:

$$25\ °C + (6.4\ °C/W\ \times 10\ W) = 89\ °C$$

Note that ~19.5 W internal power dissipation pushes T_J to its maximum rated value of 150 °C when using default heatsink in an environment with natural convection.

Thermal resistance values effectively show how much a certain portion of a thermal stackup heats up for a specified power dissipation. The equations below are the basic equations for determining the junction to ambient thermal resistance for a thermal stackup that uses thermal paste and heatsink. The θ_{JA_SYSTEM} should be designed to meet the user's thermal requirements. Using the junction-to-case thermal resistance (θ_{JC}) and thermal resistance of the thermal interface material (θ_{TIM}), compute the thermal resistance (θ_{HS}) of the required heat sink with the following equation.

$$\theta_{HS} = \left(\frac{T_J - T_A}{P_{DISS}}\right) - (\theta_{JC} + \theta_{TIM})$$

$$\theta_{JA\_SYSTEM} = \theta_{HS} + \theta_{JC} + \theta_{TIM}$$

High-performance applications involving maximum power delivery at high duty cycles may require active cooling to effectively reduce θ_{JA_SYSTEM} and continuous monitoring of T_J.

For lower power applications, or if forced air convection is used, a smaller heat sink may be sufficient.

Table 12 shows the thermal resistances for different conditions when using the evaluation board, EVAL-AD8460SDZ at T_A = 25 °C. The fan used is the Sunon Fans EE80251S2-1000U-999 with air flow of 37 CFM. The heatsink used is the Wakefield-Vette P/N 518-95AB. The TIM is the GC Electronics type Z9 heat sink compound.

Table 12. θ_{JA_SYSTEM} for Different Thermal Stackups on the EVAL-AD8460SDZ

Heatsink	Air flow	θ_(JA_SYSTEM) (°C/W)
No	No	22.6
Yes	No	6.4
	Yes	4.4

SAFE OPERATING AREA

The safe operating area (SOA) represents the power handling capability of the device under various conditions. The power dissipation of the AD8460 occurs primarily from the slew boosting circuit and output stage. The SOA curves are unique to the conditions under which they are developed, such as PCB, heat sink, airflow, and ambient temperatures. In addition, all SOA curves are derated and are with respect to hotspots on the die. Typically, it is assumed the power dissipation is uniform across the whole die of a part, but, the reality is that the power dissipation is typically concentrated in certain areas based on the application. In high power applications, the output stage of an amplifier is where the hotspots commonly exist since the output stage transistors are where power is dissipated when driving a load. To preserve the lifespan of the silicon, it is recommended to utilize the SOA plots to estimate an optimal temperature for each specific application. Ensure that usage of the AD8460 remains within the published DC SOA and dynamic SOA curves, also monitoring the junction temperature using the TMP pin voltage ($V_{TMP} \leq 2.5$ V).

Long-term usage of the AD8460 at or near maximum junction temperature of 150 °C may result in a reduction of expected lifespan of the product due to accelerated thermal stresses.

A thermal model for simulation of the AD8460 is forthcoming to enable customers to evaluate thermal performance of the AD8460 under different configurations.

DC SOA

Figure 72 shows that the DC safe operating area (SOA) is a curve of output current vs. output stage supply voltage differential (V_S to V_{OUT}), under which the amplifier can operate at a safe junction temperature (T_J). The area under the curves of *Figure 72* shows the operational boundaries of the AD8460 for using the AD8460 evaluation board that maintains a $T_J \leq 150°C$.

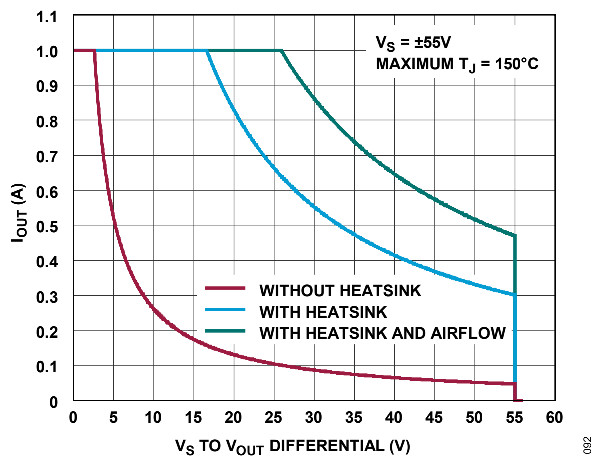

Figure 72. DC SOA without Heatsink, with Default Heatsink, with Default Heatsink and Fan, T_A = 25 °C

All testing was done in the natural convection of a lab. Forced air convection in any of the test cases effectively lowers θ_{JA} and moves the corresponding curve toward the upper right, expanding the SOA. For more information on the AD8460 evaluation board, refer to the AD8460 user guide. In *Figure 72*, the horizontal line at 1 A is the output current drive of the AD8460. The curved section maintains a fixed power dissipation that results in a junction temperature (TJ) of 150°C or less. Note that the x-axis is the output stage VCE (HVCC − V_{OUT} or V_{OUT} − HVEE) developed across the relevant output transistor and ends at a maximum VCE of 55 V.

Dynamic SOA

Figure 73 illustrates the maximum square-wave amplitude that can be generated continuously without exceeding absolute maximum temperature, plotted versus frequency with a specified capacitive load and specified heat sink.

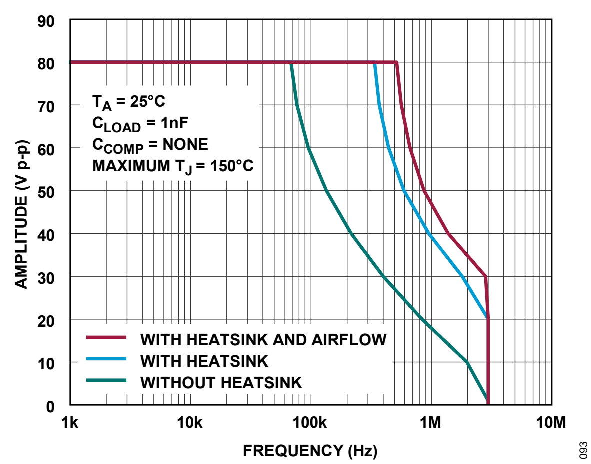

Figure 73. Dynamic SOA without Heatsink, with Default Heatsink, with Default Heatsink and Fan, C_{LOAD} = 1 nF, T_A = 25 °C

The *Slew Boost* section discusses how the AD8460 consumes significant dynamic supply current during high-slew transitions. Above a particular frequency (load-dependent), the electrical power consumption required to slew ±full scale exceeds the device's ability to dissipate while remaining below absolute maximum junction temperature. Additional thermal management can be leveraged to expand the SOA.

Limiting Dynamic Peak Current for >1nF Loads

The AD8460 can drive 1 A continuously by design, assuming appropriate thermal management as outlined in the *Thermal Management* section.

The AD8460 has also been qualified to drive 80 Vp-p square-wave pulses into a 1 nF load without external compensation or slew control. This corresponds to +2.6 A/−2.2 A peak, with a ~35 ns pulse width, as specified in the electrical characteristics.

If driving pulses into >1 nF loads, to remain within the qualified device conditions, the peak current should be limited to the continuous output current drive of 1 A. To ensure this, the user must implement digital slew rate control to limit the peak current when driving these loads.

The current into a capacitor can be calculated using the formula:

$$I = C\frac{dV}{dt}$$

This generates the following table of maximum slew rate that ensures a peak current of ≤ 1 A. Also outlined are the minimum f_{SYNC} frequencies required to drive 80 Vp-p as these slew rates digitally.

Table 13.Maximum Slew vs. Capacitive Load

Capacitance	Maximum Slew Rate	Minimum f_{SYNC}
10 nF	100 V/µs	20 MHz
22 nF	45 V/µs	9.1 MHz
47 nF	21 V/µs	4.3 MHz

To implement a digital slew control, the number of steps needed during an edge event is calculated by:

$$n_{STEPS} = \frac{Amplitude_{P-P} \times f_{SYNC}}{EDGE\ SPEED}$$

For loads <47 nF, it is recommended to ensure each digital step is ≤5 V to limit the peak dynamic current. This corrosponds to a n_{STEPS} ≥ 16 for an 80 Vp-p $Amplitude_{P-P}$. *Table 13* shows the minimum f_{SYNC} frequencies to ensure at least 16 steps at the maximum edge speed. For loads >47 nF, a greater number of n_{STEPS} is recommended.

FULL-SCALE ADJUSTMENT

Using HV supplies of ±50 V, the default configuration shown in *Figure 58* produces a 80 V span centered at zero volts. Modify the output voltage span in three different ways:

- Forcing REFIO_1P2V externally with a user-supplied voltage reference.
- Changing the value of R_{SET} to reduce the value of I_{REF}.

Note: The output span is defined by the HVDAC's external configuration and is unaffected by changes in HVCC and HVEE, provided there is sufficient headroom between HV supplies and programmed output range. See *Figure 43* for more information about headroom requirements. Insufficient HV supply headroom may result in output signal clipping.

FULL-SCALE REDUCTION

For applications requiring dynamically-adjustable span, there are two methods to achieve a reduced programmable output voltage span.

Under the conventional setup, R_{TERM} = 50 Ω, R_{SET} and REFIO_1P2V can be adjusted to achieve a lower output voltage span. The output transfer function simplifies to:

$$V_{OUT} = \left(80\ V \times \left(\frac{DAC\ CODE}{2^{14}}\right) - 40\ V\right) \times \left(\frac{2\ k\Omega}{R_{SET}}\right) \times \left(\frac{V_{REFIO_{1P2V}}}{1.2\ V}\right)$$

The range of R_{SET} is 2 $k\Omega$ to 20 $k\Omega$, which can be used to change the output voltage range from +/−40 V to +/−4 V, respectively. Because R_{SET} is a hardware item, this is a good option for applications that do not require changes in span once the hardware configuration is implemented. Note that the AD8460's output voltage range cannot be increased by reducing R_{SET}. See *Table 14* for a list of various RSET values for a specific output voltage span.

Table 14.Typical Output Voltage Span for Constant REFIO_1P2V with Various RSET values

Output Voltage Range (Vpp)	RSET (Ω)	REFIO_1P2V (V)
80	2000	1.2
60	2666.7	1.2
40	4000	1.2
20	8000	1.2
10	16000	1.2
8	20000	1.2

Alternatively, a reduced programmable voltage span may be implemented by forcing REFIO_1P2V externally with a user-supplied voltage reference. This is done by driving REFIO_1P2V with a voltage in the range of 1.2 V maximum to as low as 0.12 V, which can be used to change the output voltage range from +/−40 V to +/−4 V, respectively. This is the recommended option for applications requiring dynamically-adjustable span.

Table 15.Typical Output Voltage Span for Constant RSET with Various REFIO_1P2V

Output Voltage Range (Vpp)	RSET (Ω)	REFIO_1P2V (V)
80	2000	1.2
60	2000	0.9
40	2000	0.6
20	2000	0.3
10	2000	0.15
8	2000	0.12

For precision applications, it is recommended to use a high precision 1.2 V to drive REFIO_1P2V. This allows for the best dynamic performance when the device is under normal operation. The internal reference from REFIO_1P2V can drift in performance with changes in temperature. See *Table 15* for a list of various REFIO_1P2V values for a specific output voltage span.

LAYOUT

When designing the PCB, it is important to incorporate thermal layout techniques in addition to the standard electrical layout practices. Thermal considerations involve attention to trace thickness, thermal vias, ground and power layers, and large copper areas for power supply areas. The high voltage power supply lines (HVCC, HVEE) should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Decouple the power supply (HVCC, HVEE, AVDD_3P3V, DVDD_3P3V, VCC_5V, and VREF_5V) PCB entry points and the pins of the AD8460 with low ESR ceramic capacitors. The decoupling capacitors should be placed close to the AD8460 and connected using short and wide traces to provide low impedance paths and reduce the effect of glitches on the power supply lines. Lower ESR, ESL decoupling capacitors on HVCC, HVEE pins help reduce voltage ripple and glitches. For supplies with multiple pins (HVCC, HVEE), it is recommended that these pins be tied together and that each supply be decoupled only once. Place the smallest value capacitor on the same side of the board as the AD8460 and as close as possible to the amplifier power supply pins with the ground end of the capacitor directly to the ground plane.

Because this product has analog and digital functions, it is important to separate and confine the analog and digital sections to certain areas of the PCB proximal to the AD8460. Allow the analog ground plane to run under the AD8460 to avoid noise coupling. Avoid running digital lines under the AD8460 because these couple noise onto the die, unless there is a ground plane acting as shield. Fast switching digital signals such as SYNC or clock should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the analog traces. Traces on adjacent PCB layers should run at right angles to each other to reduce effects from coupling and feedthrough throughout the board. Avoid crossover of digital and analog signals. Use at least one ground plane, and it can be common or split between the digital and analog section. In the latter case, join the planes underneath the AD8460 devices.

TOP LEVEL DIGITAL REGISTER ASSIGNMENT

Table 16.Digital Register Map Instance Summary

Name	Module	Address
AD8460_CTRL_REGMAP	AD8460_CTRL_REGMAP	0x00
AD8460_CALIBRATION_FACTORS_REGMAP	RESERVED	0x20
AD8460_CALIBRATION_CTRL_REGMAP	RESERVED	0x40
AD8460_HVDAC_DATA_REGMAP	AD8460_HVDAC_DATA_REGMAP	0x60

DEVICE CONTROL REGISTER SUMMARY AND MAP

Table 17.Control Register Summary

Address	Name	Description	Reset	Access
0x00	CTRL_REG_00	General device control registers. See *Table 18.*	0x10	R/W
0x01	CTRL_REG_01	General device control registers. See *Table 18.*	0x08	R/W
0x02	CTRL_REG_02	General device control registers. See *Table 18.*	0x03	R/W
0x03	CTRL_REG_03	General device control registers. See *Table 18.*	0x00	R/W
0x04	CTRL_REG_04	General device control registers. See *Table 18.*	0x00	R/W
0x05	CTRL_REG_05	Reserved		
0x06 to 0x07	CTRL_REG_06 - CTRL_REG_07	Reserved		
0x08	CTRL_REG_08	General device control registers. See *Table 18.*	0x00	R/W
0x09	CTRL_REG_09	General device control registers. See *Table 18.*	0x00	R/W
0x0A	CTRL_REG_10	General device control registers. See *Table 18.*	0x00	R/W
0x0B	CTRL_REG_11	General device control registers. See *Table 18.*	0x00	R/W
0x0C	CTRL_REG_12	General device control registers. See *Table 18.*	0x00	R/W
0x0D	CTRL_REG_13	General device control registers. See *Table 18.*	0x00	R/W
0x0E	CTRL_REG_14	General device control registers. See *Table 18.*	0x00	R/CLR
0x0F to 0x18	CTRL_REG_15 to CTRL_REG_24	Reserved		
0x19	CTRL_REG_25	General device control registers. See *Table 18.*	0x00	R
0x1A	CTRL_REG_26	General device control registers. See *Table 18.*	0x46	R

Note: R/W means read and write; R/CLR means read and clear. See the *FAULT MONITORING AND PROTECTION* section for a description of R/CLR.

Table 18. Control Register Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	CTRL_ REG_00	[7:0]	HV_RESET	RESERVED	RESERVED	HV_SLEEP	RESERVED			WAVE_GEN_ MODE	0x10	R/W
0x01	CTRL_ REG_01	[7:0]	RESERVED		INHIBIT_HVDAC_SHUTDOWN	RESERVED	HVDAC_ SLEEP	RESERVED	HVDAC_DATA_FORMAT	RESERVED	0x08	R/W
0x02	CTRL_ REG_02	[7:0]	RESERVED		APG_MODE_ENABLE	SYNC_EDGE	PATTERN_DEPTH				0x03	R/W
0x03	CTRL_ REG_03	[7:0]	RESERVED							SOFT_RESET	0x00	R/W
0x04	CTRL_ REG_04	[7:0]	SET_IQ								0x00	R/W
0x05	CTRL_ REG_05	[7:0]	RESERVED									
0x08	CTRL_ REG_08	[7:0]	OC_SRC_ARM	OC_SRC_LIMIT							0x00	R/W
0x09	CTRL_ REG_09	[7:0]	OC_SNK_ARM	OC_SNK_LIMIT							0x00	R/W
0x0A	CTRL_ REG_10	[7:0]	OV_POS_ARM	OV_POS_LIMIT							0x00	R/W
0x0B	CTRL_ REG_11	[7:0]	OV_NEG_ARM	OV_NEG_LIMIT							0x00	R/W
0x0C	CTRL_ REG_12	[7:0]	OT_ARM	OT_LIMIT							0x00	R/W
0x0D	CTRL_ REG_13	[7:0]	RESERVED			OC_SRC_ ALARM_ LATCH	OC_SNK_ ALARM_ LATCH	OV_POS_ ALARM_ LATCH	OV_NEG_ ALARM_ LATCH	OT_ALARM_ LATCH	0x00	R/W
0x0E	CTRL_ REG_14	[7:0]	SHUTDOWN_ FLAG	RESERVED		OC_SRC_ ALARM	OC_SNK_ ALARM	OV_POS_ ALARM	OV_NEG_ ALARM	OT_ ALARM	0x00	R/ CLR

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x19	CTRL_REG_25	[7:0]	RESERVED				DIE_REV				0x04	R
0x1A	CTRL_REG_26	[7:0]	CHIP_ID								0x46	R

CONTROL REGISTER DETAILS

Table 19.Bit Descriptions for CTRL_REG_00

Bits	Bit Name	Description	Reset	Access
7	HV_RESET	Reset HV shutdown latch. (0) Default: No reset. HV shutdown can occur. (1) Clear shutdown latch and re-enable HV driver from shutdown. Not self-clearing: to reset write “1” then “0”, else HV shutdown is suppressed while reset is enabled.	0x0	R/W
6	RESERVED	Reserved. Do not write.		
5	RESERVED	Reserved. Do not write.		
4	HV_SLEEP	Shutdown HV driver. (0) HV driver is shutdown. HV quiescent current decreases, and output of amplifier is floating (high impedance). This overrides all other mechanisms (SDN_IO and protection features). (1) Default: HV driver is enabled but can still be shutdown through other mechanisms (SDN_IO and protection features).	0x1	R/W
[3:1]	RESERVED	Reserved. Do not write.		
0	WAVE_GEN_MODE	Selects waveform generation mode for HVDAC data source. (0) Default: Arbitrary waveform generation (AWG) mode. (1) Analog pattern generation (APG) mode. Must set APG_MODE_ENABLE in CTRL_REG_02.	0x0	R/W

Table 20. Bit Descriptions for CTRL_REG_01

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved. Do not write.		
5	INHIBIT_HVDAC_SHUTDOWN	Set whether HV shutdown also shuts down DAC. (0) Default: HV driver shutdown also shuts down DAC. (1) HV driver shutdown does not shutdown DAC. DAC remains on when HV driver is shutdown.	0x0	R/W
4	RESERVED	Reserved. Do not write.		
3	HVDAC_SLEEP	Shutdown DAC. (0) Default: DAC is enabled. (1) DAC is shutdown. DAC quiescent current decreases, and output	0x1	R/W
2	RESERVED	Reserved. Do not write.		
1	HVDAC_DATA_FORMAT	HVDAC 14-bit data input format. (0) Straight binary. (1) Two's complement.	0x0	R/W
0	RESERVED	Reserved. Do not write.		

Table 21. Bit Descriptions for CTRL_REG_02

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved. Do not write.		
5	APG_MODE_ENABLE	Enable bit to toggle analog pattern generator (APG) mode. (0) Default: APG mode disabled. (1) APG mode enabled if WAVE_GEN_MODE in CTRL_REG_00 also enabled.	0x0	R/W
4	SYNC_EDGE	Toggle rising edge versus falling edge of SYNC for update of DAC in APG mode. (0) Default: Clock DAC on rising edge of SYNC. (1) Clock DAC on falling edge of SYNC.	0x0	R/W
[3:0]	PATTERN_DEPTH	Pattern depth of APG mode table of levels. This value is the index after which data index returns to zero when clocking. Default value is 0x3, corresponding to 4-level pattern. Maximum value is 0xF, corresponding to 16-level pattern.	0x3	R/W

Table 22. Bit Descriptions for CTRL_REG_03

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved. Do not write.		
0	SOFT_RESET	Reset digital engine. (0) Default: Digital engine active (1) Clear all register values (including this one, self-clearing) and initiate reboot sequence of digital engine.	0x0	R/W

Table 23. Bit Descriptions for CTRL_REG_04

Bits	Bit Name	Description	Reset	Access
[7:0]	SET_IQ	Program quiescent current of HV driver. Default of 0x0 puts part at nominal supply current. Bit 7 (MSB) is polarity bit: (0) is quiescent current reduction, (1) is quiescent current increase. Bits 6:0 are monotonic but nonlinear change to supply current. See *PROGRAMMABLE QUIESCENT CURRENT*.	0x0	R/W

Table 24. Bit Descriptions for CTRL_REG_05

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved. Do not write.		

Table 25. Bit Descriptions for CTRL_REG_08

Bits	Bit Name	Description	Reset	Access
7	OC_SRC_ARM	Enable overcurrent (source) protection. (0) Default: Protection is disabled. (1) Protection is enabled, monitoring output source current.	0x0	R/W
[6:0]	OC_SRC_LIMIT	Set level of overcurrent (source) protection. See *PROGRAMMING OVERCURRENT PROTECTION.*	0x0	R/W

Table 26. Bit Descriptions for CTRL_REG_09

Bits	Bit Name	Description	Reset	Access
7	OC_SNK_ARM	Enable overcurrent (sink) protection. (0) Default: Protection is disabled. (1) Protection is enabled, monitoring output sink current.	0x0	R/W
[6:0]	OC_SNK_LIMIT	Set level of overcurrent (sink) protection. See *PROGRAMMING OVERCURRENT PROTECTION.*	0x0	R/W

Table 27. Bit Descriptions for CTRL_REG_10

Bits	Bit Name	Description	Reset	Access
7	OV_POS_ARM	Enable overvoltage (positive) protection. (0) Default: Protection is disabled. (1) Protection is enabled, monitoring positive output voltage.	0x0	R/W
[6:0]	OV_POS_LIMIT	Set level of overvoltage (positive) protection. See *PROGRAMMING OVERVOLTAGE PROTECTION*	0x0	R/W

Table 28. Bit Descriptions for CTRL_REG_11

Bits	Bit Name	Description	Reset	Access
7	OV_NEG_ARM	Enable overvoltage (negative) protection. (0) Default: Protection is disabled. (1) Protection is enabled, monitoring negative output voltage.	0x0	R/W
[6:0]	OV_NEG_LIMIT	Set level of overvoltage (negative) protection. See *PROGRAMMING OVERVOLTAGE PROTECTION*	0x0	R/W

Table 29. Bit Descriptions for CTRL_REG_12

Bits	Bit Name	Description	Reset	Access
7	OT_ARM	Enable overtemperature (T_J) protection. (0) Default: Protection is disabled. (1) Protection is enabled, monitoring junction temperature.	0x0	R/W
[6:0]	OT_LIMIT	Set level of overtemperature (T_J) protection. See *PROGRAMMING OVERTEMPERATURE PROTECTION.*	0x0	R/W

Table 30. Bit Descriptions for CTRL_REG_13

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved. Do not write.		
4	OC_SRC_ALARM_LATCH	Enable overcurrent (source) alarm latch. (0) Default: Latch is disabled. OC_SRC_ALARM self-clears if overcurrent (source) fault clears. (1) Enable latch of OC_SRC_ALARM flag, latched high If overcurrent (source) fault detected	0x0	R/W
3	OC_SNK_ALARM_LATCH	Enable overcurrent (sink) alarm latch. (0) Default: Latch is disabled. OC_SNK_ALARM self-clears if overcurrent (sink) fault clears. (1) Enable latch of OC_SNK_ALARM flag, latched high If overcurrent (sink) fault detected	0x0	R/W

Bits	Bit Name	Description	Reset	Access
2	OV_POS_ALARM_LATCH	Enable overvoltage (positive) alarm latch. (0) Default: Latch is disabled. OV_POS_ALARM self-clears if overvoltage (positive) fault clears. (1) Enable latch of OV_POS_ALARM flag, latched high If overvoltage (positive) fault detected	0x0	R/W
1	OV_NEG_ALARM_LATCH	Enable overvoltage (negative) alarm latch. (0) Default: Latch is disabled. OV_NEG_ALARM self-clears if overvoltage (negative) fault clears. (1) Enable latch of OV_NEG_ALARM flag, latched high If overvoltage (negative) fault detected	0x0	R/W
0	OT_ALARM_LATCH	Enable overtemperature (T_J) alarm latch. (0) Default: Latch is disabled. OT_ALARM self-clears if overtemperature (T_J) fault clears. (1) Enable latch of OT_ALARM flag, latched high If overtemperature (T_J) fault detected	0x0	R/W

Table 31. Bit Descriptions for CTRL_REG_14

Bits	Bit Name	Description	Reset	Access[1]
7	SHUTDOWN_FLAG	Indicates HV shutdown state. (0) Default: HV driver is enabled. (1) HV driver is shutdown.	0x0	R
[6:5]	RESERVED	Reserved. Do not write.		
4	OC_SRC_ALARM	Overcurrent (source) alarm flag. (1) Indicates overcurrent (source) fault event. If latched, write to clear.	0x0	R/CLR
3	OC_SNK_ALARM	Overcurrent (sink) alarm flag. (1) Indicates overcurrent (sink) fault event. If latched, write to clear.	0x0	R/CLR
2	OV_POS_ALARM	Overvoltage (positive) alarm flag. (1) Indicates overvoltage (positive) fault event. If latched, write to clear.	0x0	R/CLR
1	OV_NEG_ALARM	Overvoltage (negative) alarm flag. (1) Indicates overvoltage (negative) fault event. If latched, write to clear.	0x0	R/CLR
0	OT_ALARM	Overtemperature (T_J) alarm flag. (1) Indicates overtemperature (T_J) fault event. If latched, write to clear.	0x0	R/CLR

Table 32. Bit Descriptions for CTRL_REG_25

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved. Do not write.		
[3:0]	DIE_REV	Register indicating AD8460 silicon revision.	0x4	R

Table 33. Bit Descriptions for CTRL_REG_26

Bits	Bit Name	Description	Reset	Access
[7:0]	CHIP_ID	Register indicating chip ID of AD8460.	0x46	R

[1] CLR denotes that an alarm flag is cleared by writing a ‘1’ to the corresponding register bit.

HVDAC DATA REGISTER (PATTERN MEMORY) SUMMARY

Table 34.HVDAC Data Summary

Address	Name	Description	Reset[1]	Access
0x60	HVDAC_DATA_BYTE_00	HVDAC data word 0, low-order byte.	0x00	R/W
0x61	HVDAC_DATA_BYTE_01	HVDAC data word 0, high-order byte.	0x20	R/W
0x62	HVDAC_DATA_BYTE_02	HVDAC data word 1, low-order byte.	0x00	R/W
0x63	HVDAC_DATA_BYTE_03	HVDAC data word 1, high-order byte.	0x30	R/W
0x64	HVDAC_DATA_BYTE_04	HVDAC data word 2, low-order byte.	0x00	R/W
0x65	HVDAC_DATA_BYTE_05	HVDAC data word 2, high-order byte.	0x20	R/W
0x66	HVDAC_DATA_BYTE_06	HVDAC data word 3, low-order byte.	0x00	R/W
0x67	HVDAC_DATA_BYTE_07	HVDAC data word 3, high-order byte.	0x10	R/W
0x68	HVDAC_DATA_BYTE_08	HVDAC data word 4, low-order byte.	0x00	R/W
0x69	HVDAC_DATA_BYTE_09	HVDAC data word 4, high-order byte.	0x00	R/W
0x6A	HVDAC_DATA_BYTE_10	HVDAC data word 5, low-order byte.	0x00	R/W
0x6B	HVDAC_DATA_BYTE_11	HVDAC data word 5, high-order byte.	0x00	R/W
0x6C	HVDAC_DATA_BYTE_12	HVDAC data word 6, low-order byte.	0x00	R/W
0x6D	HVDAC_DATA_BYTE_13	HVDAC data word 6, high-order byte.	0x00	R/W
0x6E	HVDAC_DATA_BYTE_14	HVDAC data word 7, low-order byte.	0x00	R/W
0x6F	HVDAC_DATA_BYTE_15	HVDAC data word 7, high-order byte.	0x00	R/W
0x70	HVDAC_DATA_BYTE_16	HVDAC data word 8, low-order byte.	0x00	R/W
0x71	HVDAC_DATA_BYTE_17	HVDAC data word 8, high-order byte.	0x00	R/W
0x72	HVDAC_DATA_BYTE_18	HVDAC data word 9, low-order byte.	0x00	R/W
0x73	HVDAC_DATA_BYTE_19	HVDAC data word 9, high-order byte.	0x00	R/W
0x74	HVDAC_DATA_BYTE_20	HVDAC data word 10, low-order byte.	0x00	R/W
0x75	HVDAC_DATA_BYTE_21	HVDAC data word 10, high-order byte.	0x00	R/W
0x76	HVDAC_DATA_BYTE_22	HVDAC data word 11, low-order byte.	0x00	R/W
0x77	HVDAC_DATA_BYTE_23	HVDAC data word 11, high-order byte.	0x00	R/W

Address	Name	Description	Reset[1]	Access
0x78	HVDAC_DATA_BYTE_24	HVDAC data word 12, low-order byte.	0x00	R/W
0x79	HVDAC_DATA_BYTE_25	HVDAC data word 12, high-order byte.	0x00	R/W
0x7A	HVDAC_DATA_BYTE_26	HVDAC data word 13, low-order byte.	0x00	R/W
0x7B	HVDAC_DATA_BYTE_27	HVDAC data word 13, high-order byte.	0x00	R/W
0x7C	HVDAC_DATA_BYTE_28	HVDAC data word 14, low-order byte.	0x00	R/W
0x7D	HVDAC_DATA_BYTE_29	HVDAC data word 14, high-order byte.	0x00	R/W
0x7E	HVDAC_DATA_BYTE_30	HVDAC data word 15, low-order byte.	0x00	R/W
0x7F	HVDAC_DATA_BYTE_31	HVDAC data word 15, high-order byte.	0x00	R/W

[1] Note that HVDAC_DATA_WORD_00 through HVDAC_DATA_WORD_03 default to non-zero codes, which produces a ½ scale triangle wave at a frequency defined by the SYNC clock rate in analog pattern generation mode. These values may be overwritten through SPI.

Table 35. HVDAC_DATA_REGMAP (Pattern Memory) Register Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset[1]	Access
0x60	HVDAC_DATA_BYTE_00	[7:0]	HVDAC_DATA_WORD_00[7:0]								0x00	R/W
0x61	HVDAC_DATA_BYTE_01	[7:0]	RESERVED		HVDAC_DATA_WORD_00[13:8]						0x20	R/W
0x62	HVDAC_DATA_BYTE_02	[7:0]	HVDAC_DATA_WORD_01[7:0]								0x00	R/W
0x63	HVDAC_DATA_BYTE_03	[7:0]	RESERVED		HVDAC_DATA_WORD_01[13:8]						0x30	R/W
0x64	HVDAC_DATA_BYTE_04	[7:0]	HVDAC_DATA_WORD_02[7:0]								0x00	R/W
0x65	HVDAC_DATA_BYTE_05	[7:0]	RESERVED		HVDAC_DATA_WORD_02[13:8]						0x20	R/W
0x66	HVDAC_DATA_BYTE_06	[7:0]	HVDAC_DATA_WORD_03[7:0]								0x00	R/W
0x67	HVDAC_DATA_BYTE_07	[7:0]	RESERVED		HVDAC_DATA_WORD_03[13:8]						0x10	R/W

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset [1]	Access
0x68	HVDAC_DATA_BYTE_08	[7:0]	HVDAC_DATA_WORD_04[7:0]								0x00	R/W
0x69	HVDAC_DATA_BYTE_09	[7:0]	RESERVED		HVDAC_DATA_WORD_04[13:8]						0x00	R/W
0x6A	HVDAC_DATA_BYTE_10	[7:0]	HVDAC_DATA_WORD_05[7:0]								0x00	R/W
0x6B	HVDAC_DATA_BYTE_11	[7:0]	RESERVED		HVDAC_DATA_WORD_05[13:8]						0x00	R/W
0x6C	HVDAC_DATA_BYTE_12	[7:0]	HVDAC_DATA_WORD_06[7:0]								0x00	R/W
0x6D	HVDAC_DATA_BYTE_13	[7:0]	RESERVED		HVDAC_DATA_WORD_06[13:8]						0x00	R/W
0x6E	HVDAC_DATA_BYTE_14	[7:0]	HVDAC_DATA_WORD_07[7:0]								0x00	R/W
0x6F	HVDAC_DATA_BYTE_15	[7:0]	RESERVED		HVDAC_DATA_WORD_07[13:8]						0x00	R/W
0x70	HVDAC_DATA_BYTE_16	[7:0]	HVDAC_DATA_WORD_08[7:0]								0x00	R/W
0x71	HVDAC_DATA_BYTE_17	[7:0]	RESERVED		HVDAC_DATA_WORD_08[13:8]						0x00	R/W
0x72	HVDAC_DATA_BYTE_18	[7:0]	HVDAC_DATA_WORD_09[7:0]								0x00	R/W
0x73	HVDAC_DATA_BYTE_19	[7:0]	RESERVED		HVDAC_DATA_WORD_09[13:8]						0x00	R/W
0x74	HVDAC_DATA_BYTE_20	[7:0]	HVDAC_DATA_WORD_10[7:0]								0x00	R/W
0x75	HVDAC_DATA_BYTE_21	[7:0]	RESERVED		HVDAC_DATA_WORD_10[13:8]						0x00	R/W
0x76	HVDAC_DATA_BYTE_22	[7:0]	HVDAC_DATA_WORD_11[7:0]								0x00	R/W
0x77	HVDAC_DATA_BYTE_23	[7:0]	RESERVED		HVDAC_DATA_WORD_11[13:8]						0x00	R/W

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset [1]	Access
0x78	HVDAC_DATA_BYTE_24	[7:0]	HVDAC_DATA_WORD_12[7:0]								0x00	R/W
0x79	HVDAC_DATA_BYTE_25	[7:0]	RESERVED		HVDAC_DATA_WORD_12[13:8]						0x00	R/W
0x7A	HVDAC_DATA_BYTE_26	[7:0]	HVDAC_DATA_WORD_13[7:0]								0x00	R/W
0x7B	HVDAC_DATA_BYTE_27	[7:0]	RESERVED		HVDAC_DATA_WORD_13[13:8]						0x00	R/W
0x7C	HVDAC_DATA_BYTE_28	[7:0]	HVDAC_DATA_WORD_14[7:0]								0x00	R/W
0x7D	HVDAC_DATA_BYTE_29	[7:0]	RESERVED		HVDAC_DATA_WORD_14[13:8]						0x00	R/W
0x7E	HVDAC_DATA_BYTE_30	[7:0]	HVDAC_DATA_WORD_15[7:0]								0x00	R/W
0x7F	HVDAC_DATA_BYTE_31	[7:0]	RESERVED		HVDAC_DATA_WORD_15[13:8]						0x00	R/W

[1] Note that HVDAC_DATA_WORD_00 through HVDAC_DATA_WORD_03 default to non-zero codes, which produces a 4-level staircase waveform at ±20 V (0 V, +20 V, 0 V, −20 V) without the need for user programming, with timing defined by the user-provided SYNC clock. These values may be overwritten through SPI for the user's own analog pattern.

HVDAC DATA REGISTER (PATTERN MEMORY) DETAILS

HVDAC data, low-order byte of 14-bit analog pattern data.

Table 36. Bit Descriptions for HVDAC_DATA_BYTE_00

Bits	Bit Name	Description	Reset	Access
[7:0]	HVDAC_DATA_WORD_00[7:0]	HVDAC data word, low-order byte, all bits used.	0x0	R/W

HVDAC data, high-order byte of 14-bit analog pattern data.

Table 37. Bit Descriptions for HVDAC_DATA_BYTE_01

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED			
[5:0]	HVDAC_DATA_WORD_00[13:8]	HVDAC data word, high-order byte, 6 LSBs used.	0x20	R/W

Table 38. Bit Descriptions for HVDAC_DATA_BYTE_02

Bits	Bit Name	Description	Reset	Access
[7:0]	HVDAC_DATA_WORD_01[7:0]	HVDAC data word, low-order byte, all bits used.	0x0	R/W

HVDAC data, high-order byte of 14-bit analog pattern data.

Table 39. Bit Descriptions for HVDAC_DATA_BYTE_03

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED			
[5:0]	HVDAC_DATA_WORD_01[13:8]	HVDAC data word, high-order byte, 6 LSBs used.	0x30	R/W

HVDAC data, low-order byte of 14-bit analog pattern data.

Table 40. Bit Descriptions for HVDAC_DATA_BYTE_04

Bits	Bit Name	Description	Reset	Access
[7:0]	HVDAC_DATA_WORD_02[7:0]	HVDAC data word, low-order byte, all bits used.	0x0	R/W

HVDAC data, high-order byte of 14-bit analog pattern data.

Table 41. Bit Descriptions for HVDAC_DATA_BYTE_05

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED			
[5:0]	HVDAC_DATA_WORD_02[13:8]	HVDAC data word, high-order byte, 6 LSBs used.	0x20	R/W

HVDAC data, low-order byte of 14-bit analog pattern data.

Table 42. Bit Descriptions for HVDAC_DATA_BYTE_06

Bits	Bit Name	Description	Reset	Access
[7:0]	HVDAC_DATA_WORD_03[7:0]	HVDAC data word, low-order byte, all bits used.	0x0	R/W

HVDAC data, high-order byte of 14-bit analog pattern data.

Table 43. Bit Descriptions for HVDAC_DATA_BYTE_07

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED			
[5:0]	HVDAC_DATA_WORD_03[13:8]	HVDAC data word, high-order byte, 6 LSBs used.	0x10	R/W

All remaining pattern memory registers (HVDAC_DATA_BYTE_08 through HVDAC_DATA_BYTE_31) follow the same format of low-order byte and high-order byte shown in *Table 39*. Note that the default value for these registers is 0x0.

HVDAC data, low-order byte of 14-bit analog pattern data.

Table 44. Bit Descriptions for HVDAC_DATA_BYTE_08

Bits	Bit Name	Description	Reset	Access
[7:0]	HVDAC_DATA_WORD_04[7:0]	HVDAC data word, low-order byte, all bits used.	0x0	R/W

HVDAC data, high-order byte of 14-bit analog pattern data.

Table 45. Bit Descriptions for HVDAC_DATA_BYTE_09

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED			
[5:0]	HVDAC_DATA_WORD_04[13:8]	HVDAC data word, high-order byte, 6 LSBs used.	0x0	R/W

HVDAC data, low-order byte of 14-bit analog pattern data.

Table 46. Bit Descriptions for HVDAC_DATA_BYTE_10

Bits	Bit Name	Description	Reset	Access
[7:0]	HVDAC_DATA_WORD_05[7:0]	HVDAC data word, low-order byte, all bits used.	0x0	R/W

HVDAC data, high-order byte of 14-bit analog pattern data.

Table 47. Bit Descriptions for HVDAC_DATA_BYTE_11

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED			
[5:0]	HVDAC_DATA_WORD_05[13:8]	HVDAC data word, high-order byte, 6 LSBs used.	0x0	R/W

HVDAC data, low-order byte of 14-bit analog pattern data.

Table 48. Bit Descriptions for HVDAC_DATA_BYTE_12

Bits	Bit Name	Description	Reset	Access
[7:0]	HVDAC_DATA_WORD_06[7:0]	HVDAC data word, low-order byte, all bits used.	0x0	R/W

HVDAC data, high-order byte of 14-bit analog pattern data.

Table 49. Bit Descriptions for HVDAC_DATA_BYTE_13

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED			
[5:0]	HVDAC_DATA_WORD_06[13:8]	HVDAC data word, high-order byte, 6 LSBs used.	0x0	R/W

HVDAC data, low-order byte of 14-bit analog pattern data.

Table 50. Bit Descriptions for HVDAC_DATA_BYTE_14

Bits	Bit Name	Description	Reset	Access
[7:0]	HVDAC_DATA_WORD_07[7:0]	HVDAC data word, low-order byte, all bits used.	0x0	R/W

HVDAC data, high-order byte of 14-bit analog pattern data.

Table 51. Bit Descriptions for HVDAC_DATA_BYTE_15

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED			
[5:0]	HVDAC_DATA_WORD_07[13:8]	HVDAC data word, high-order byte, 6 LSBs used.	0x0	R/W

HVDAC data, low-order byte of 14-bit analog pattern data.

Table 52. Bit Descriptions for HVDAC_DATA_BYTE_16

Bits	Bit Name	Description	Reset	Access
[7:0]	HVDAC_DATA_WORD_08[7:0]	HVDAC data word, low-order byte, all bits used.	0x0	R/W

HVDAC data, high-order byte of 14-bit analog pattern data.

Table 53. Bit Descriptions for HVDAC_DATA_BYTE_17

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED			
[5:0]	HVDAC_DATA_WORD_08[13:8]	HVDAC data word, high-order byte, 6 LSBs used.	0x0	R/W

HVDAC data, low-order byte of 14-bit analog pattern data.

Table 54. Bit Descriptions for HVDAC_DATA_BYTE_18

Bits	Bit Name	Description	Reset	Access
[7:0]	HVDAC_DATA_WORD_09[7:0]	HVDAC data word, low-order byte, all bits used.	0x0	R/W

HVDAC data, high-order byte of 14-bit analog pattern data.

Table 55. Bit Descriptions for HVDAC_DATA_BYTE_19

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED			
[5:0]	HVDAC_DATA_WORD_09[13:8]	HVDAC data word, high-order byte, 6 LSBs used.	0x0	R/W

HVDAC data, low-order byte of 14-bit analog pattern data.

Table 56. Bit Descriptions for HVDAC_DATA_BYTE_20

Bits	Bit Name	Description	Reset	Access
[7:0]	HVDAC_DATA_WORD_10[7:0]	HVDAC data word, low-order byte, all bits used.	0x0	R/W

HVDAC data, high-order byte of 14-bit analog pattern data.

Table 57. Bit Descriptions for HVDAC_DATA_BYTE_21

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED			
[5:0]	HVDAC_DATA_WORD_10[13:8]	HVDAC data word, high-order byte, 6 LSBs used.	0x0	R/W

HVDAC data, low-order byte of 14-bit analog pattern data.

Table 58. Bit Descriptions for HVDAC_DATA_BYTE_22

Bits	Bit Name	Description	Reset	Access
[7:0]	HVDAC_DATA_WORD_11[7:0]	HVDAC data word, low-order byte, all bits used.	0x0	R/W

HVDAC data, high-order byte of 14-bit analog pattern data.

Table 59. Bit Descriptions for HVDAC_DATA_BYTE_23

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED			
[5:0]	HVDAC_DATA_WORD_11[13:8]	HVDAC data word, high-order byte, 6 LSBs used.	0x0	R/W

HVDAC data, low-order byte of 14-bit analog pattern data.

Table 60. Bit Descriptions for HVDAC_DATA_BYTE_24

Bits	Bit Name	Description	Reset	Access
[7:0]	HVDAC_DATA_WORD_12[7:0]	HVDAC data word, low-order byte, all bits used.	0x0	R/W

HVDAC data, high-order byte of 14-bit analog pattern data.

Table 61. Bit Descriptions for HVDAC_DATA_BYTE_25

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED			
[5:0]	HVDAC_DATA_WORD_12[13:8]	HVDAC data word, high-order byte, 6 LSBs used.	0x0	R/W

HVDAC data, low-order byte of 14-bit analog pattern data.

Table 62. Bit Descriptions for HVDAC_DATA_BYTE_26

Bits	Bit Name	Description	Reset	Access
[7:0]	HVDAC_DATA_WORD_13[7:0]	HVDAC data word, low-order byte, all bits used.	0x0	R/W

HVDAC data, high-order byte of 14-bit analog pattern data.

Table 63. Bit Descriptions for HVDAC_DATA_BYTE_27

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED			
[5:0]	HVDAC_DATA_WORD_13[13:8]	HVDAC data word, high-order byte, 6 LSBs used.	0x0	R/W

HVDAC data, low-order byte of 14-bit analog pattern data.

Table 64. Bit Descriptions for HVDAC_DATA_BYTE_28

Bits	Bit Name	Description	Reset	Access
[7:0]	HVDAC_DATA_WORD_14[7:0]	HVDAC data word, low-order byte, all bits used.	0x0	R/W

HVDAC data, high-order byte of 14-bit analog pattern data.

Table 65. Bit Descriptions for HVDAC_DATA_BYTE_29

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED			
[5:0]	HVDAC_DATA_WORD_14[13:8]	HVDAC data word, high-order byte, 6 LSBs used.	0x0	R/W

HVDAC data, low-order byte of 14-bit analog pattern data.

Table 66. Bit Descriptions for HVDAC_DATA_BYTE_30

Bits	Bit Name	Description	Reset	Access
[7:0]	HVDAC_DATA_WORD_15[7:0]	HVDAC data word, low-order byte, all bits used.	0x0	R/W

HVDAC data, high-order byte of 14-bit analog pattern data.

Table 67. Bit Descriptions for HVDAC_DATA_BYTE_31

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED			
[5:0]	HVDAC_DATA_WORD_15[13:8]	HVDAC data word, high-order byte, 6 LSBs used.	0x0	R/W

OUTLINE DIMENSIONS

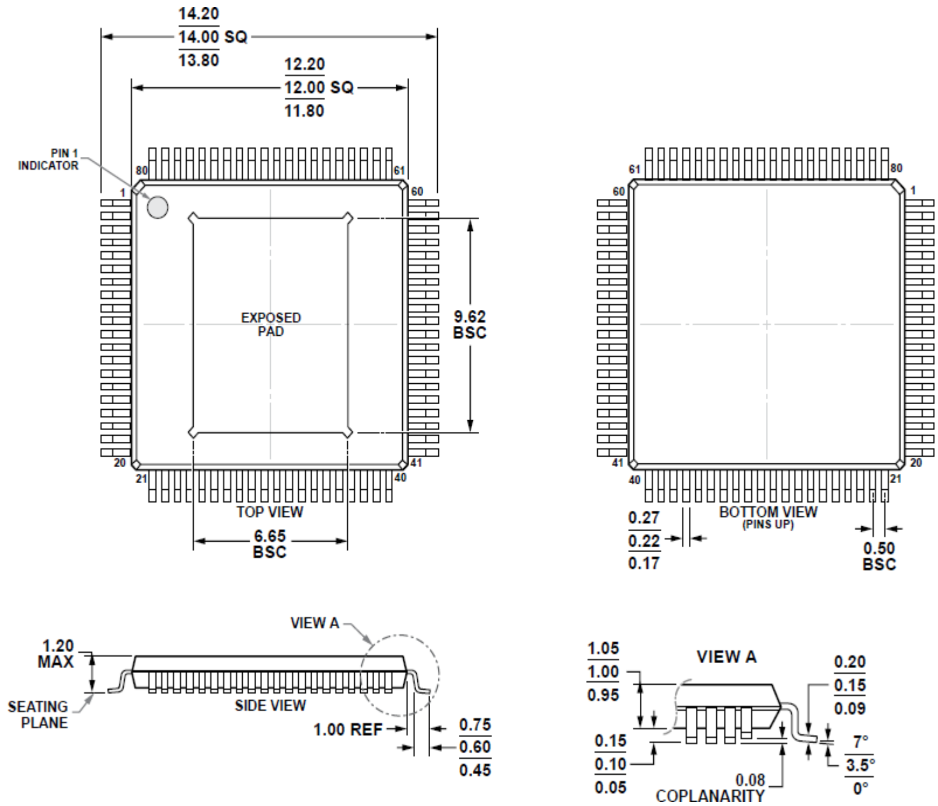

***Figure 74.** 80-Lead Thin Quad Flat Package, Exposed Pad TQFP, SV-80-7, Dimensions shown in milimeters*

ORDERING GUIDE

Model	Temperature Range	Package Description	Packing Quantity	Package Option
AD8460BSVZ	-40 °C to 85 °C	80-Lead TQFP		SV-80-7
AD8460BSVZ-RL	-40 °C to 85 °C	80-Lead TQFP	1000	SV-80-7

EVALUATION BOARD

Model	Description
EVAL-AD8460SDZ	Evaluation Board for 80-Lead Thin Quad Flat Package