Rail-to-Rail, Fast, Low Power 2.5 V to 5.5 V, Single-Supply TTL/CMOS Comparator

Data Sheet **AD8468**

FEATURES

Fully specified rail to rail at V_{CC} = 2.5 V to 5.5 V
Input common-mode voltage from −0.2 V to V_{CC} + 0.2 V
Low glitch CMOS-/TTL-compatible output stage
40 ns propagation delay
Low power: 2 mW at 2.5 V
Shutdown pin
Power supply rejection > 60 dB
−40°C to +125°C operation
Qualified for automotive applications

APPLICATIONS

Automotive applications
High speed instrumentation
Clock and data signal restoration
Logic level shifting or translation
High speed line receivers
Threshold detection
Peak and zero-crossing detectors
High speed trigger circuitry
Pulse-width modulators
Current-/voltage-controlled oscillators

FUNCTIONAL BLOCK DIAGRAM

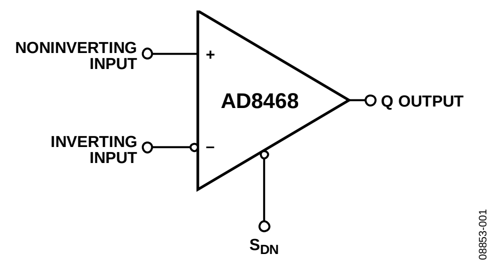

Figure 1.

GENERAL DESCRIPTION

The AD8468 is a fast comparator fabricated on XFCB2.0, an Analog Devices, Inc., proprietary process. This comparator is exceptionally versatile and easy to use. Features include an input range from −0.2 V to V_{CC} + 0.2 V, low noise, TTL-/CMOS-compatible output drivers, and shutdown inputs. The device offers 40 ns propagation delays driving a 15 pF load with 10 mV overdrive on 500 μA typical supply current.

A flexible power supply scheme allows the device to operate with a single 2.5 V positive supply with a −0.2 V to + 2.7 V input signal range and up to a 5.5 V positive supply with a −0.2 V to +5.7 V input signal range.

The TTL-/CMOS-compatible output stage is designed to drive up to 15 pF with full rated timing specifications and to degrade in a graceful and linear fashion as additional capacitance is added. The input stage of the comparator offers robust protection against large input overdrive, and the outputs do not phase reverse when the valid input signal range is exceeded.

The AD8468 is available in a tiny 6-lead SC70 package with a single-ended output and a shutdown pin.

Rev. A Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

10/15—Rev. 0 to Rev. A

Changes to Table 2 ... 4

10/10—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5 V, T_A = −40°C to +125°C. Typical values are T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC INPUT CHARACTERISTICS						
Voltage Range	V_P, V_N	V_{CC} = 2.5 V to 5.5 V	−0.2		V_{CC} + 0.2	V
Common-Mode Range		V_{CC} = 2.5 V to 5.5 V	−0.2		V_{CC} + 0.2	V
Differential Voltage		V_{CC} = 2.5 V to 5.5 V			V_{CC}	V
Offset Voltage	V_{OS}		−10.0	±3	+10.0	mV
Bias Current	I_P, I_N		−0.4		+0.4	µA
Offset Current			−1.0		+1.0	µA
Capacitance	C_P, C_N			1		pF
Resistance, Differential Mode		−0.5 V to V_{CC} + 0.5 V	200		7000	kΩ
Resistance, Common Mode		−0.5 V to V_{CC} + 0.5 V	100		4000	kΩ
Active Gain	A_V			80		dB
Common-Mode Rejection	CMRR	V_{CC} = 2.5 V, V_{CM} = −0.2 V to +2.7 V	45			dB
		V_{CC} = 5.5 V	45			dB
SHUTDOWN PIN CHARACTERISTICS[1]						
V_{IH}		Comparator is operating	2.0		V_{CC}	V
V_{IL}		Shutdown guaranteed	−0.2	+0.4	+0.4	V
I_{IH}		V_{IH} = V_{CC}	−6		+6	µA
Sleep Time	t_{SD}	I_{CC} < 100 µA		300		ns
Wake-Up Time	t_H	V_{PP} = 10 mV, output valid		150		ns
DC OUTPUT CHARACTERISTICS						
Output Voltage High Level	V_{OH}	I_{OH} = 0.8 mA	V_{CC} − 0.4			V
Output Voltage Low Level	V_{OL}	I_{OL} = 0.8 mA			0.4	V
AC PERFORMANCE[2]						
Rise Time/Fall Time	t_R, t_F	10% to 90%, V_{CC} = 2.5 V		25 to 50		ns
		10% to 90%, V_{CC} = 5.5 V		45 to 75		ns
Propagation Delay	t_{PD}	V_{OD} = 10 mV, V_{CC} = 2.5 V		30 to 50		ns
		V_{OD} = 50 mV, V_{CC} = 5.5 V		35 to 60		ns
Propagation Delay Skew—Rising to Falling Transition		V_{CC} = 2.5 V		4.5		ns
		V_{CC} = 5.5 V		8		ns
Overdrive Dispersion		10 mV < V_{OD} < 125 mV		12		ns
Common-Mode Dispersion		−0.2 V < V_{CM} < V_{CC} + 0.2 V		1.5		ns
POWER SUPPLY						
Supply Voltage Range	V_{CC}		2.5		5.5	V
Positive Supply Current	I_{VCC}	V_{CC} = 2.5 V		550	800	µA
		V_{CC} = 5.5 V		800	1300	µA
Power Dissipation	P_D	V_{CC} = 2.5 V		1.375	2.0	mW
		V_{CC} = 5.5 V		4.95	7.15	mW
Power Supply Rejection Ratio	PSRR	V_{CC} = 2.5 V to 5.5 V	−50			dB
Shutdown Current	I_{SD}	V_{CC} = 2.5 V to 5.5 V		250	350	µA

[1] The output is in a high impedance mode when the device is in shutdown mode. Note that this feature should be used with care because the enable/disable time is much longer than with a true tristate output.
[2] V_{IN} = 100 mV square input at 1 MHz, V_{CM} = 0 V, C_L = 15 pF, V_{CCI} = 2.5 V, unless otherwise noted.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltages	
Supply Voltage (V_{CC} to GND)	−0.5 V to +6.0 V
Input Voltages	
Input Voltage	−0.5 V to V_{CC} + 0.5 V
Maximum Input/Output Current	±50 mA
Current	
Input Current (into V_P, V_N)[1]	±10 mA
Shutdown Control Pin	
Applied Voltage (S_{DN} to GND)	−0.5 V to V_{CC} + 0.5 V
Maximum Input/Output Current	±50 mA
Output Current	±50 mA
Temperature	
Operating Temperature, Ambient	−40°C to +125°C
Operating Temperature, Junction	150°C

[1] Input pins have clamp diodes to the power supply pins. Limit input current to 10 mA or less whenever input signals exceed the power supply rail by 0.5 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	Unit
6-Lead SC70	426	°C/W

[1] Measurement in still air.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

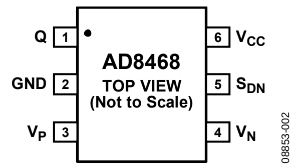

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Q	Noninverting Output. Q is at logic high if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N.
2	GND	Ground.
3	V_P	Noninverting Analog Input.
4	V_N	Inverting Analog Input.
5	S_{DN}	Shutdown. Drive this pin low to shut down the device.
6	V_{CC}	V_{CC} Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 2.5 V, T_A = 25°C, unless otherwise noted.

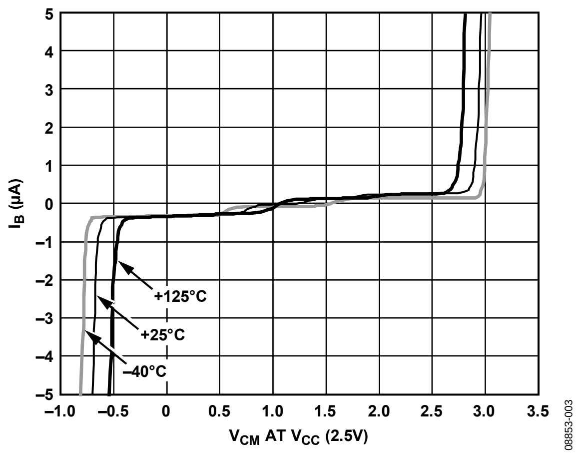

Figure 3. Input Bias Current vs. Input Common-Mode Voltage

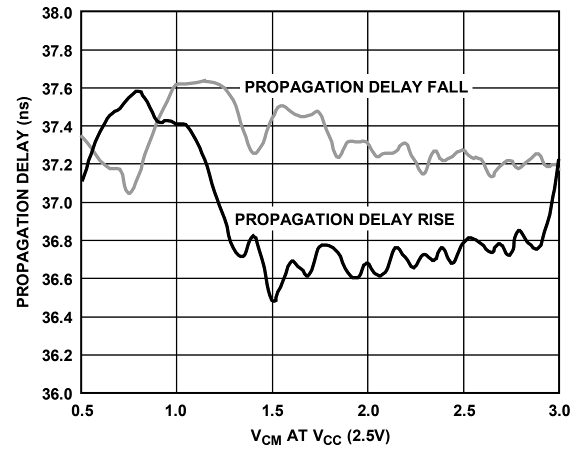

Figure 6. Propagation Delay vs. Input Common-Mode Voltage

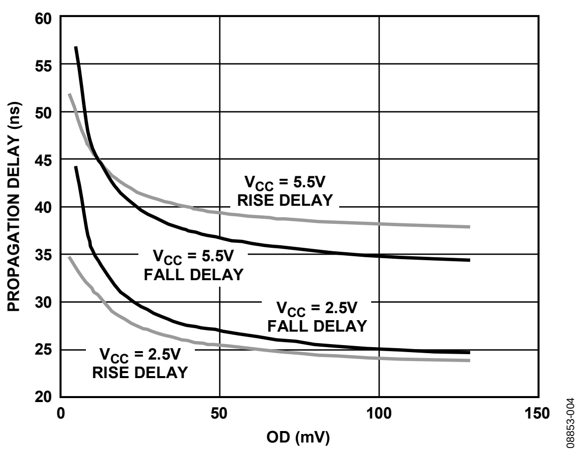

Figure 4. Propagation Delay vs. Input Overdrive at V_{CC} = 2.5 V and 5.5 V

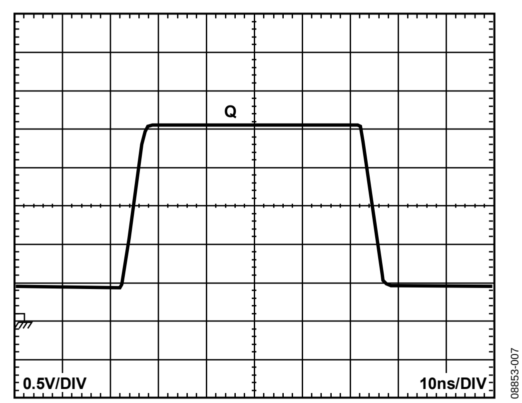

Figure 7. 1 MHz Output Voltage Waveform, V_{CC} = 2.5 V

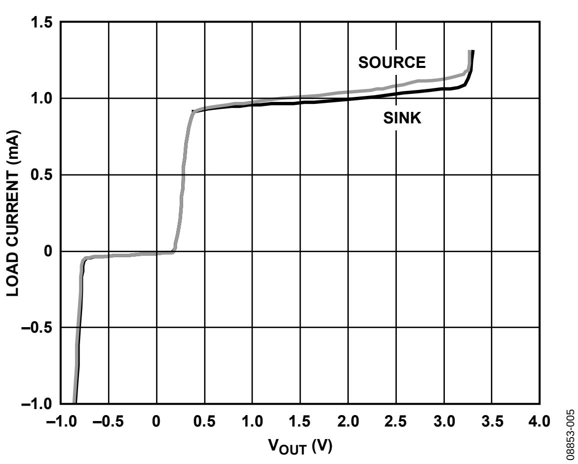

Figure 5. Load Current vs. V_{OH}/V_{OL}

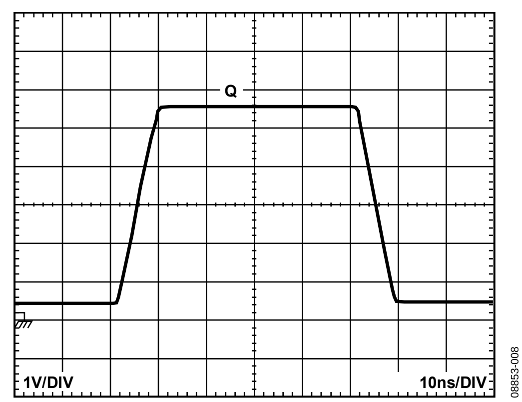

Figure 8. 1 MHz Output Voltage Waveform, V_{CC} = 5.5 V

APPLICATIONS INFORMATION

POWER/GROUND LAYOUT AND BYPASSING

The AD8468 comparator is a high speed device. Despite the low noise output stage, it is essential to use proper high speed design techniques to achieve the specified performance. Because comparators are uncompensated amplifiers, feedback in any phase relationship is likely to cause oscillations or undesired hysteresis. Of critical importance is the use of low impedance supply planes, particularly the output supply plane (V_{CC}) and the ground plane (GND). Individual supply planes are recommended as part of a multilayer board. Providing the lowest inductance return path for switching currents ensures the best possible performance in the target application.

It is also important to adequately bypass the input and output supplies. A 0.1 μF bypass capacitor should be placed as close as possible to the V_{CC} supply pin. The capacitor should be connected to the GND plane with redundant vias placed to provide a physically short return path for output currents flowing back from ground to the V_{CC} pin. High frequency bypass capacitors should be carefully selected for minimum inductance and ESR. Parasitic layout inductance should also be strictly controlled to maximize the effectiveness of the bypass at high frequencies.

TTL-/CMOS-COMPATIBLE OUTPUT STAGE

Specified propagation delay performance can be achieved only by keeping the capacitive load at or below the specified minimums. The output of the AD8468 is designed to directly drive one Schottky TTL, three low power Schottky TTL loads, or the equivalent. For large fanouts, buses, or transmission lines, use an appropriate buffer to maintain the excellent speed and stability of the comparator.

With the rated 15 pF load capacitance applied, more than half of the total device propagation delay is output stage slew time. Because of this, the total propagation delay decreases as V_{CC} decreases, and instability in the power supply may appear as excess delay dispersion.

Delay is measured to the 50% point for whatever supply is in use; thus, the fastest times are observed with the V_{CC} supply at 2.5 V, and larger values are observed when driving loads that switch at other levels.

Overdrive and input slew rate dispersions are not significantly affected by output loading and V_{CC} variations.

The TTL-/CMOS-compatible output stage is shown in the simplified schematic diagram (see Figure 9). Because of its inherent symmetry and generally good behavior, this output stage is readily adaptable for driving various filters and other unusual loads.

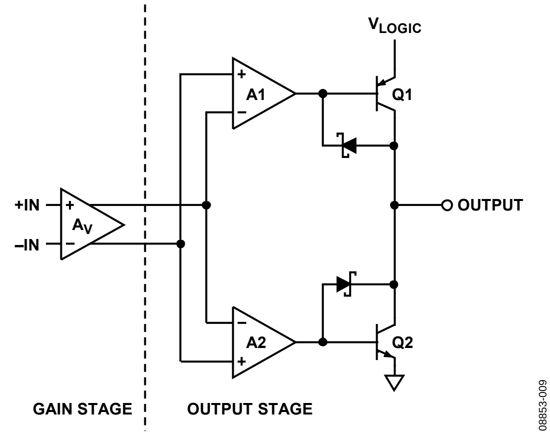

Figure 9. Simplified Schematic Diagram of the TTL-/CMOS-Compatible Output Stage

OPTIMIZING PERFORMANCE

As with any high speed comparator, proper design and layout techniques are essential for obtaining the specified performance. Stray capacitance, inductance, common power and ground impedances, or other layout issues can severely limit performance and can often cause oscillation. The source impedance should be minimized as much as is practicable. High source impedance, in combination with the parasitic input capacitance of the comparator, causes an undesirable degradation in bandwidth at the input, thus degrading the overall response. Higher impedances encourage undesired coupling.

COMPARATOR PROPAGATION DELAY DISPERSION

The AD8468 comparator is designed to reduce propagation delay dispersion over a wide input overdrive range of 10 mV to V_{CC} − 1 V. Propagation delay dispersion is the variation in propagation delay that results from a change in the degree of overdrive or slew rate (how far or how fast the input signal exceeds the switching threshold). See Figure 10 and Figure 11.

Propagation delay dispersion is a specification that becomes important in high speed, time-critical applications, such as data communication, automatic test and measurement, and instrumentation. It is also important in event-driven applications, such as pulse spectroscopy, nuclear instrumentation, and medical imaging.

The AD8468 overdrive dispersion is typically <12 ns as the overdrive varies from 10 mV to 125 mV. This specification applies to both positive and negative signals because the device has very closely matched delays for both positive-going and negative-going inputs and very low output skews. Remember to add the actual device offset to the overdrive for repeatable dispersion measurements.

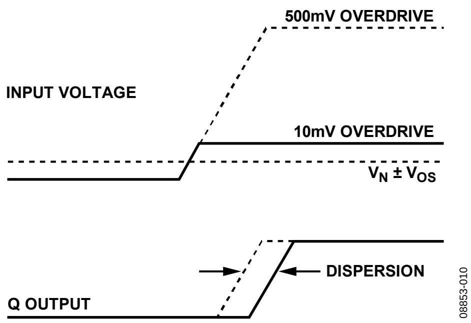

Figure 10. Propagation Delay—Overdrive Dispersion

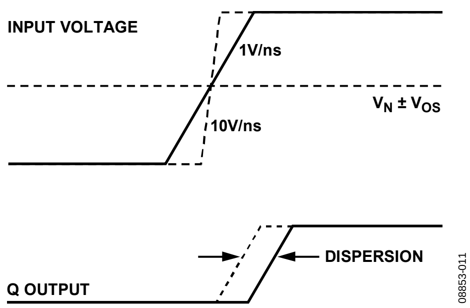

Figure 11. Propagation Delay—Slew Rate Dispersion

CROSSOVER BIAS POINT

Rail-to-rail inputs of this type, in both op amps and comparators, have a dual front-end design. Certain devices are active near the V_{CC} rail and others are active near the V_{EE} rail or ground. At some predetermined point in the common-mode range, a crossover occurs. At this point, normally $V_{CC}/2$, the direction of the bias current reverses, and there are changes in measured offset voltages and currents.

The AD8468 slightly elaborates on this scheme. Crossover points can be found at approximately 0.8 V and 1.6 V.

MINIMUM INPUT SLEW RATE REQUIREMENT

With the rated load capacitance and normal good PC board design practice, as discussed in the Optimizing Performance section, these comparators should be stable at any input slew rate with no hysteresis. Broadband noise from the input stage is observed in place of the violent chattering seen with most other high speed comparators. With additional capacitive loading or poor bypassing, oscillation may be encountered. These oscillations are due to the high gain bandwidth of the comparator in combination with feedback through parasitics in the package and PC board. In many applications, chattering is not harmful.

TYPICAL APPLICATION CIRCUITS

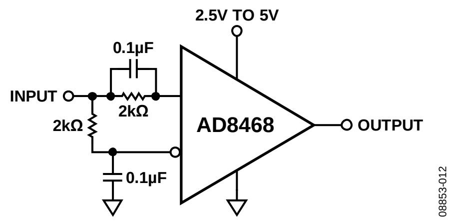

Figure 12. Self-Biased, 50% Slicer

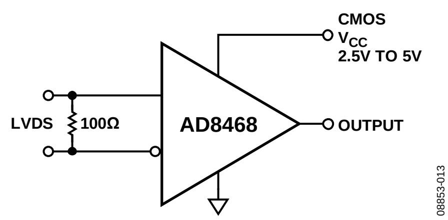

Figure 13. LVDS-to-CMOS Receiver

OUTLINE DIMENSIONS

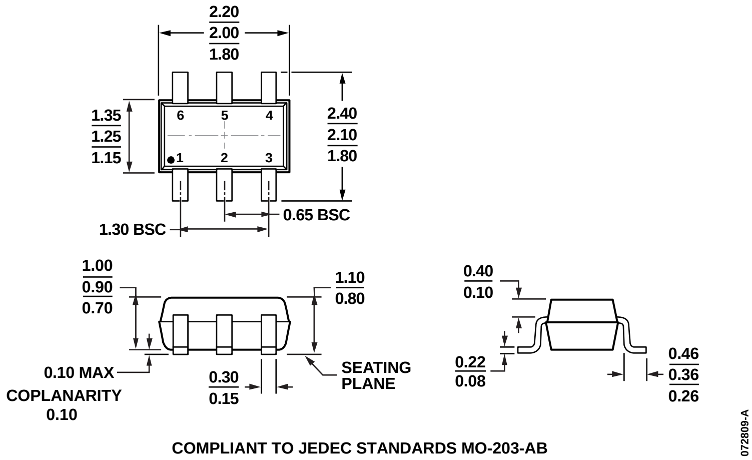

Figure 14. 6-Lead Thin Shrink Small Outline Transistor Package [SC70] (KS-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8468WBKSZ-R7	−40°C to +125°C	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	Y3F
AD8468WBKSZ-RL	−40°C to +125°C	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	Y3F

[1] Z = RoHS Compliant Part.

AUTOMOTIVE PRODUCTS

The AD8468WBKSZ models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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