

FEATURES

- Supply current: 1 μ A maximum
- Offset voltage: 1 mV maximum
- Single-supply or dual-supply operation
- Rail-to-rail input and output
- No phase reversal
- Unity gain stable

APPLICATIONS

- Portable equipment
- Remote sensors
- Low power filters
- Threshold detectors
- Current sensing

GENERAL DESCRIPTION

The AD8500 is a low power, precision CMOS op amp featuring a maximum supply current of 1 μ A. The AD8500 has a maximum offset voltage of 1 mV and a typical input bias current of 1 pA; it operates rail-to-rail on both the input and output. The AD8500 can operate from a single-supply voltage of +1.8 V to +5.5 V or a dual-supply voltage of ± 0.9 V to ± 2.75 V.

With its low power consumption, low input bias current, and rail-to-rail input and output, the AD8500 is ideally suited for a variety of battery-powered portable applications. Potential applications include ECGs, pulse monitors, glucose meters, smoke and fire detectors, vibration monitors, and backup battery sensors.

PIN CONFIGURATION

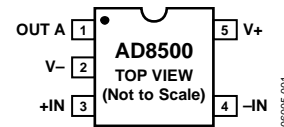


Figure 1. 5-Lead SC70

The ability to swing rail-to-rail at both the input and output helps maximize dynamic range and signal-to-noise ratio in systems that operate at very low voltages. The low offset voltage allows the AD8500 to be used in systems with high gain without having excessively large output offset errors, and it provides high accuracy without the need for system calibration.

The AD8500 is fully specified over the industrial temperature range (-40°C to $+85^{\circ}\text{C}$) and is operational over the extended industrial temperature range (-40°C to $+125^{\circ}\text{C}$). It is available in a 5-lead, SC70 surface-mount package.

Table 1. Low Supply Current Op Amps

| Supply Current | 1 μ A | 10 μ A | 20 μ A |
|----------------|-----------|------------|------------|
| Single | AD8500 | | |
| Dual | AD8502 | ADA4505-2 | AD8506 |
| Quad | AD8504 | ADA4505-4 | AD8508 |

Rev. B

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REVISION HISTORY

2/09—Rev. A to Rev. B

| | |
|---|---|
| Added Table 1; Renumbered Sequentially | 1 |
| Changes to Typical Performance Characteristics Section..... | 6 |

8/06—Rev. 0 to Rev. A

| | |
|--|-----------|
| Updated Format..... | Universal |
| Changes to Figure 17, Figure 18, and Figure 19 | 8 |

4/06—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

@ $V_S = 5\text{ V}$, $V_{CM} = V_S/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------------------------|--|-------|----------|------|------------------------------|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | V_{OS} | $0\text{ V} < V_{CM} < 5\text{ V}$ | | 0.235 | 1 | mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ | | 3 | 10 | $\mu\text{V}/^\circ\text{C}$ |
| Input Voltage Range | | | -0.3 | | +5.3 | V |
| Input Bias Current | I_B | $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ | | 1 | 10 | pA |
| | | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | | | 100 | pA |
| | | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | | | 600 | pA |
| Input Offset Current | I_{OS} | $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ | | 0.5 | 5 | pA |
| | | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | | | 50 | pA |
| | | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | | | 100 | pA |
| Common-Mode Rejection Ratio | CMRR | $0\text{ V} < V_{CM} < 5\text{ V}$ | 75 | 90 | | dB |
| | | $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ | 70 | 90 | | dB |
| Large Signal Voltage Gain | A_{VO} | $0.1\text{ V} < V_{OUT} < 4.9\text{ V}$ | 98 | 120 | | dB |
| | | $0.1\text{ V} < V_{OUT} < 4.9\text{ V}; -40^\circ\text{C} < T_A < +85^\circ\text{C}$ | 80 | | | dB |
| Input Capacitance | C_{DIFF} C_{CM} | | | 2 4.5 | | pF pF |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | V_{OH} | $R_{LOAD} = 100\text{ k}\Omega$ to GND | 4.970 | 4.995 | | V |
| | | $R_{LOAD} = 10\text{ k}\Omega$ to GND | 4.900 | 4.960 | | V |
| Output Voltage Low | V_{OL} | $R_{LOAD} = 100\text{ k}\Omega$ to V_S | | 0.85 | 5 | mV |
| | | $R_{LOAD} = 10\text{ k}\Omega$ to V_S | | 6.5 | 15 | mV |
| Short-Circuit Current | I_{SC} | $V_{OUT} = \text{GND}$ | | ± 5 | | mA |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $1.8\text{ V} < V_S < 5\text{ V}$ | 90 | 110 | | dB |
| | | $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ | 80 | | | dB |
| Supply Current/Amplifier | I_{SY} | $V_O = V_S/2$ | | 0.75 | 1 | μA |
| | | $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ | | | 1.5 | μA |
| | | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | | | 2 | μA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | | | 0.004 | | V/ μs |
| Gain Bandwidth Product | GBP | | | 7 | | kHz |
| Phase Margin | ϕ_O | | | 60 | | Degrees |
| NOISE PERFORMANCE | | | | | | |
| Peak-to-Peak Noise | | 0.1 Hz to 10 Hz | | 6 | | $\mu\text{V p-p}$ |
| Voltage Noise Density | e_n | $f = 1\text{ kHz}$ | | 190 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| Current Noise Density | i_n | $f = 1\text{ kHz}$ | | 0.1 | | $\text{pA}/\sqrt{\text{Hz}}$ |

AD8500

@ $V_S = 1.8\text{ V}$, $V_{CM} = V_S/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------------------------|--|-------|----------|------|------------------------------|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | V_{OS} | $0\text{ V} < V_{CM} < 1.8\text{ V}$ | | 0.235 | 1 | mV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ | | 3.5 | 12 | $\mu\text{V}/^\circ\text{C}$ |
| Input Voltage Range | | | -0.3 | | +2.1 | V |
| Input Bias Current | I_B | $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ | | 1 | 10 | pA |
| | | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | | | 100 | pA |
| | | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | | | 600 | pA |
| Input Offset Current | I_{OS} | $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ | | 0.5 | 5 | pA |
| | | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | | | 50 | pA |
| | | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | | | 100 | pA |
| Common-Mode Rejection Ratio | CMRR | $0\text{ V} < V_{CM} < 1.8\text{ V}$ | 65 | 85 | | dB |
| | | $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ | 60 | 83 | | dB |
| Large Signal Voltage Gain | A_{VO} | $0.1\text{ V} < V_{OUT} < 1.7\text{ V}$ | 88 | 115 | | dB |
| | | $0.1\text{ V} < V_{OUT} < 1.7\text{ V}; -40^\circ\text{C} < T_A < +85^\circ\text{C}$ | 70 | | | dB |
| Input Capacitance | C_{DIFF} C_{CM} | | | 2 4.5 | | pF pF |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage High | V_{OH} | $R_{LOAD} = 100\text{ k}\Omega$ to GND | 1.790 | 1.798 | | V |
| | | $R_{LOAD} = 10\text{ k}\Omega$ to GND | 1.760 | 1.783 | | V |
| Output Voltage Low | V_{OL} | $R_{LOAD} = 100\text{ k}\Omega$ to V_S | | 0.70 | 5 | mV |
| | | $R_{LOAD} = 10\text{ k}\Omega$ to V_S | | 5 | 15 | mV |
| Short-Circuit Current | I_{SC} | | | ± 2 | | mA |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $1.8\text{ V} < V_S < 5\text{ V}$ | 90 | 110 | | dB |
| | | $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ | 80 | | | dB |
| Supply Current/Amplifier | I_{SY} | $V_O = V_S/2$ | | 0.65 | 1 | μA |
| | | $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ | | | 1.5 | μA |
| | | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | | | 2 | μA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | | | 0.004 | | V/ μs |
| Gain Bandwidth Product | GBP | | | 7 | | kHz |
| Phase Margin | ϕ_O | | | 60 | | Degrees |
| NOISE PERFORMANCE | | | | | | |
| Peak-to-Peak Noise | | 0.1 Hz to 10 Hz | | 6 | | $\mu\text{V p-p}$ |
| Voltage Noise Density | e_n | $f = 1\text{ kHz}$ | | 190 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| Current Noise Density | i_n | $f = 1\text{ kHz}$ | | 0.1 | | $\text{pA}/\sqrt{\text{Hz}}$ |

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

| Parameter | Rating |
|--------------------------------------|--|
| Supply Voltage | 6 V |
| Input Voltage | $V_{SS} - 0.4\text{ V}$ to $V_{DD} + 0.4\text{ V}$ |
| Differential Input Voltage | $\pm 6\text{ V}$ |
| Output Short-Circuit Duration to GND | Indefinite |
| Storage Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Operating Temperature Range | -40°C to $+125^\circ\text{C}$ |
| Junction Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Lead Temperature (Soldering, 60 sec) | 300°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply at 25°C , unless otherwise noted.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Characteristics

| Package Type | θ_{JA} | θ_{JC} | Unit |
|--------------------|---------------|---------------|---------------------------|
| 5-Lead SC70 (KS-5) | 376 | 126 | $^\circ\text{C}/\text{W}$ |

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

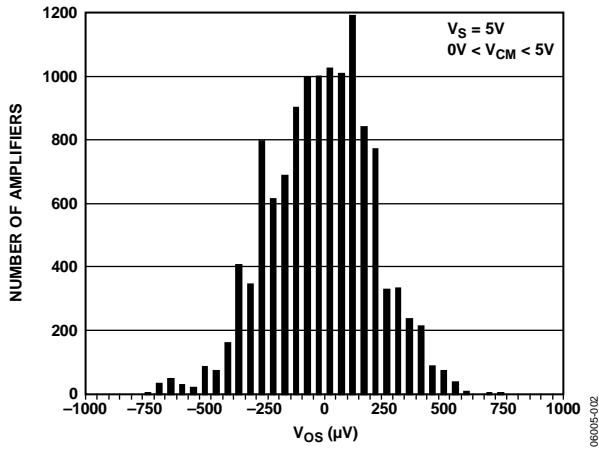


Figure 2. Input Offset Voltage Distribution

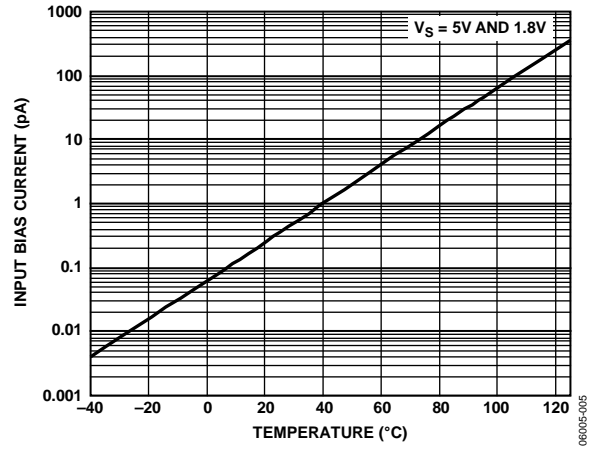


Figure 5. Input Bias Current vs. Temperature

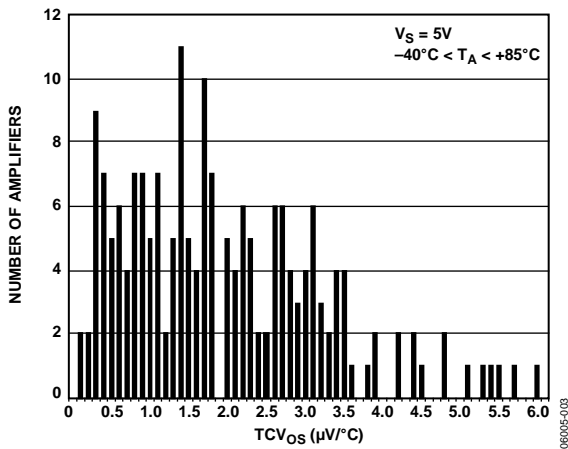


Figure 3. Input Offset Voltage Drift Distribution

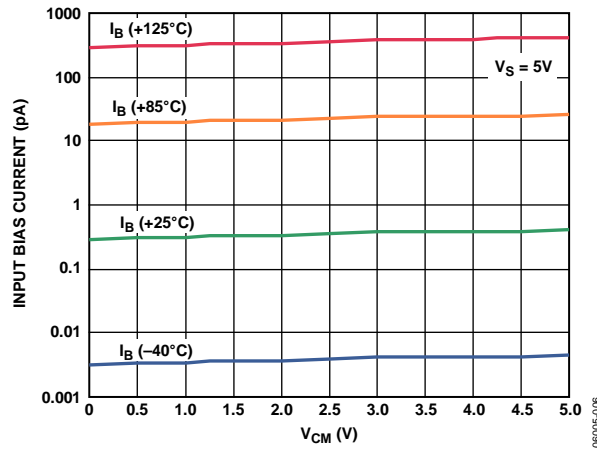


Figure 6. Input Bias Current vs. Common-Mode Voltage

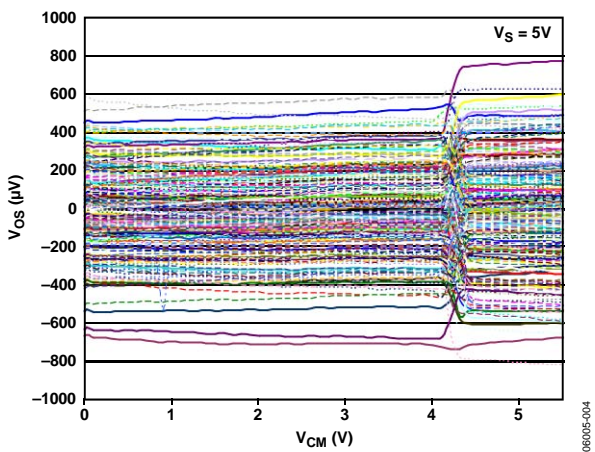


Figure 4. Input Offset Voltage vs. Common-Mode Voltage

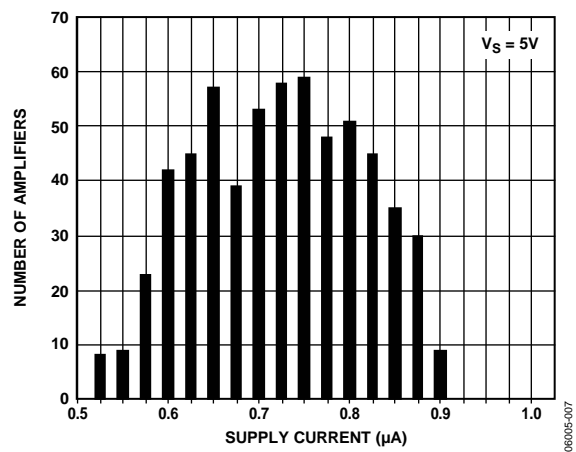


Figure 7. Supply Current Distribution

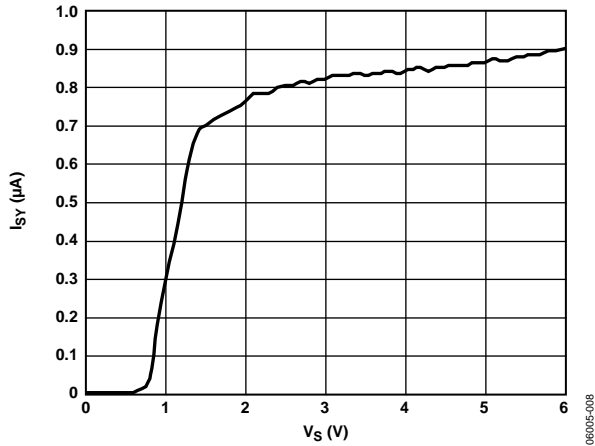


Figure 8. Supply Current vs. Supply Voltage

06005-008

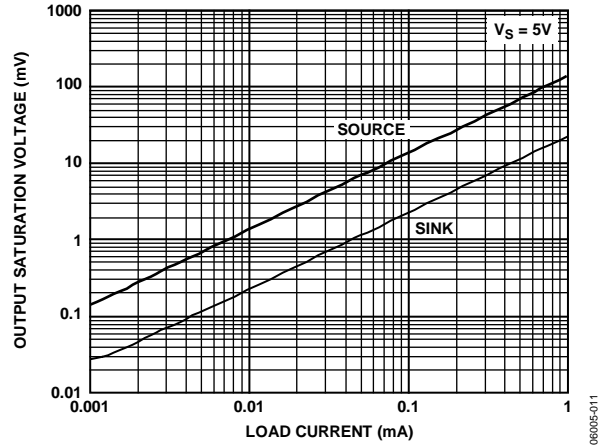


Figure 11. Output Saturation Voltage vs. Load Current

06005-011

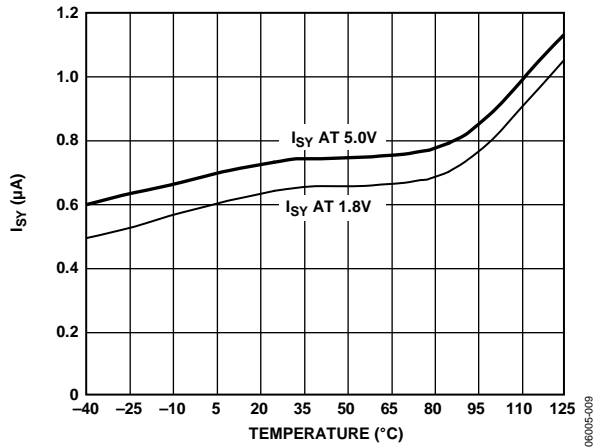


Figure 9. Supply Current vs. Temperature

06005-009

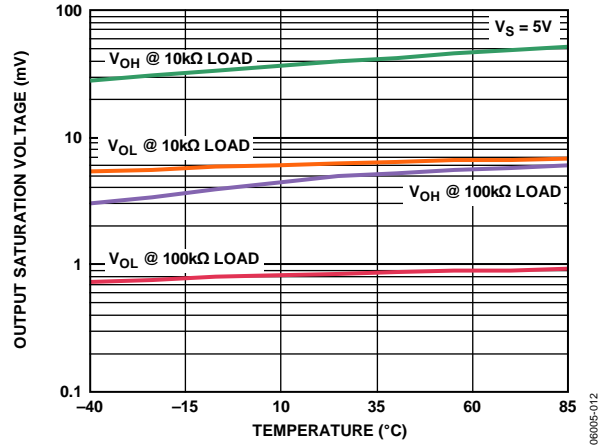


Figure 12. Output Saturation Voltage vs. Temperature

06005-012

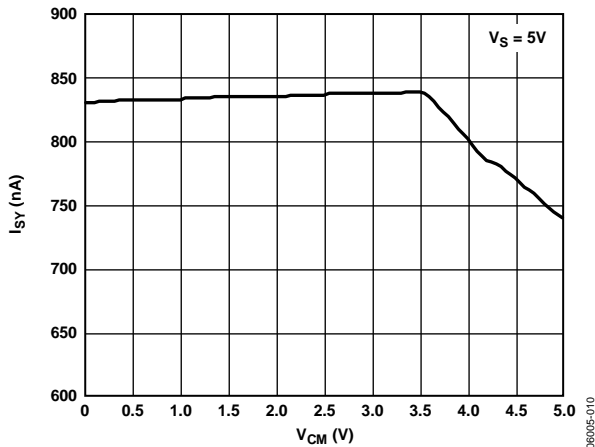


Figure 10. Supply Current vs. Input Common-Mode Voltage

06005-010

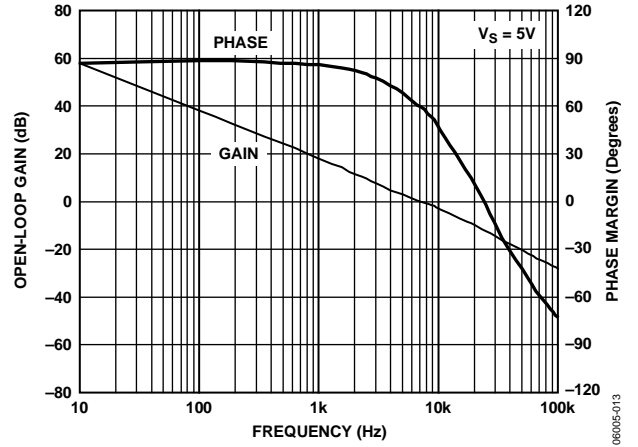


Figure 13. Open-Loop Gain and Phase vs. Frequency

06005-013

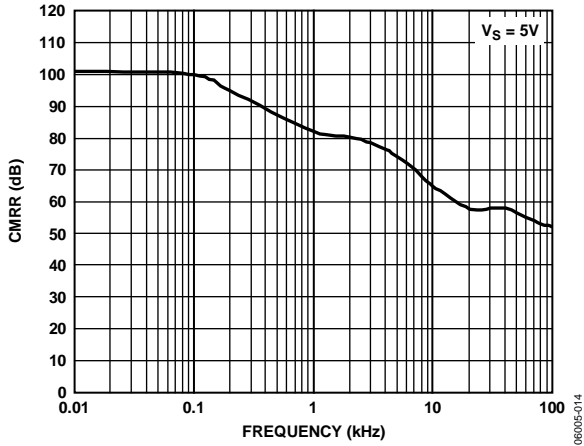


Figure 14. CMRR vs. Frequency

06005-014

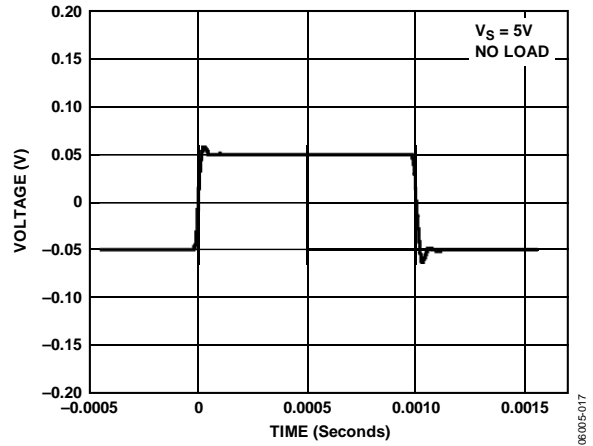


Figure 17. Small Signal Transient Response

06005-017

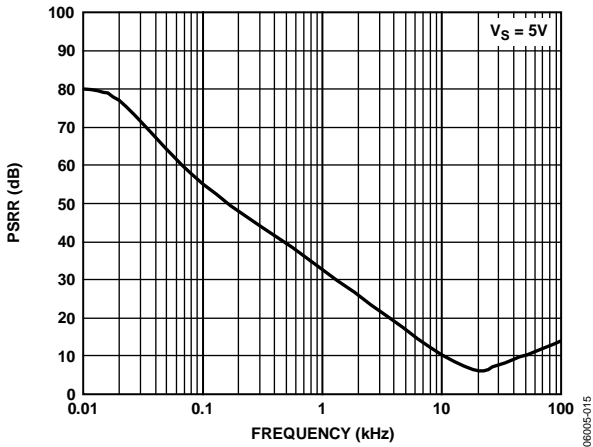


Figure 15. PSRR vs. Frequency

06005-015

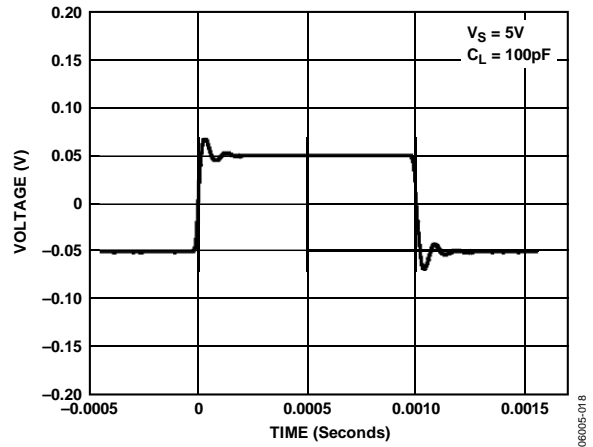


Figure 18. Small Signal Transient Response

06005-018

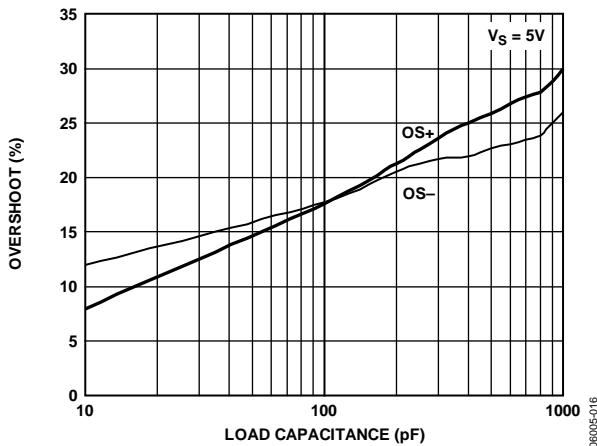


Figure 16. Small Signal Overshoot vs. Load Capacitance

06005-016

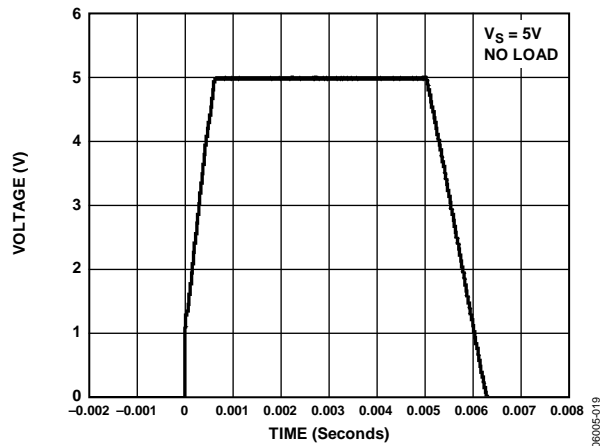


Figure 19. Large Signal Transient Response

06005-019

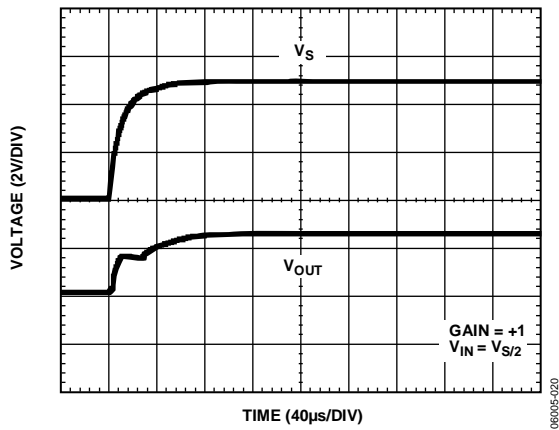


Figure 20. Turn-On Transient Response

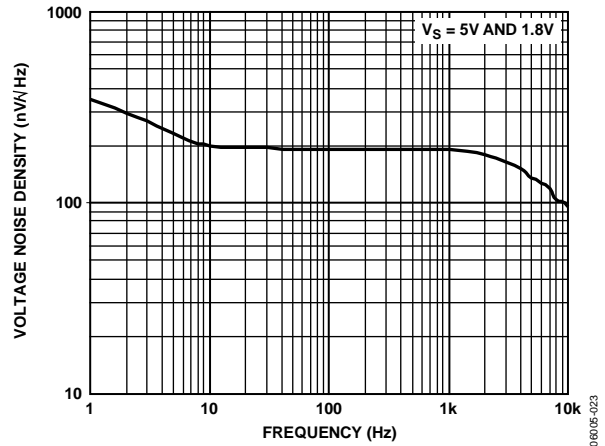


Figure 23. Voltage Noise Density

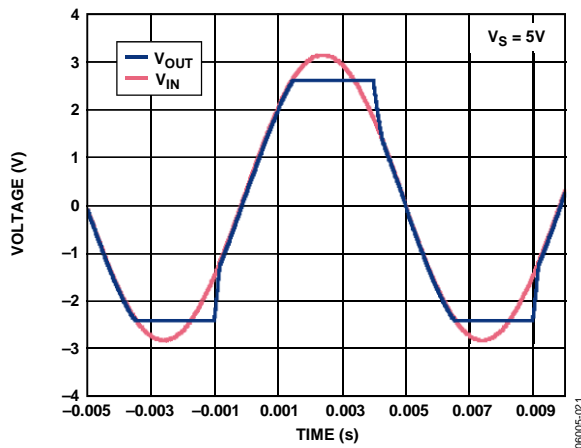


Figure 21. No Phase Reversal

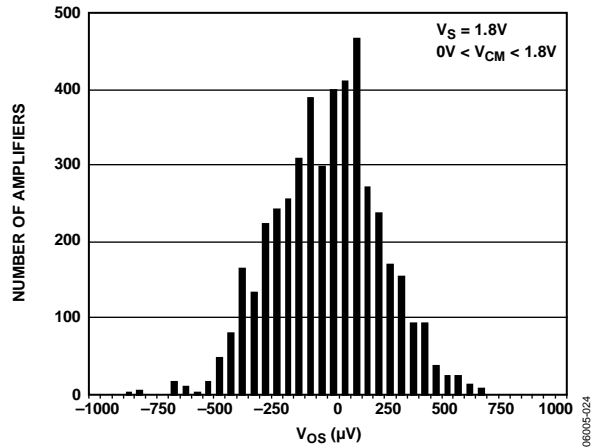


Figure 24. Input Offset Voltage Distribution

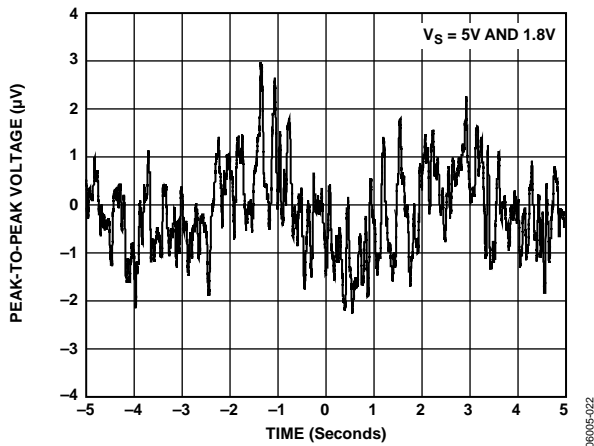


Figure 22. 0.1 Hz to 10 Hz Input Voltage Noise

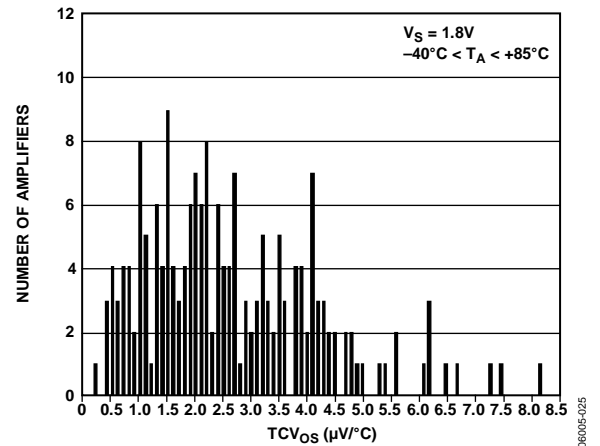


Figure 25. Input Offset Voltage Drift Distribution

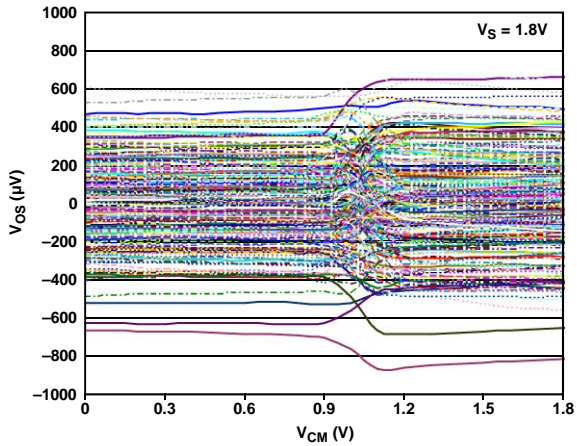


Figure 26. Input Offset Voltage vs. Input Common-Mode Voltage

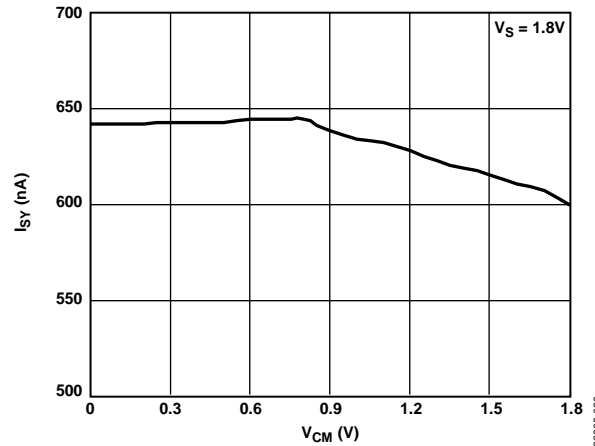


Figure 29. Supply Current vs. Input Common-Mode Voltage

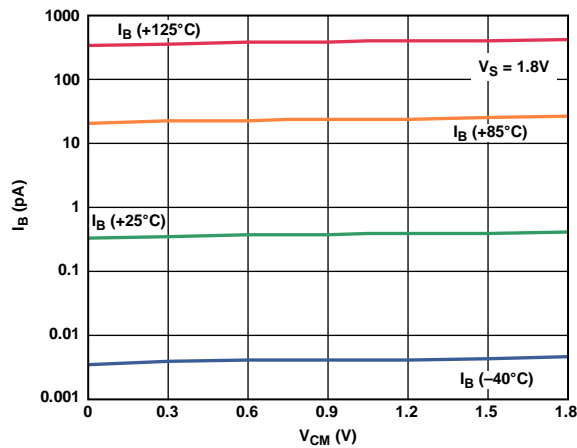


Figure 27. Input Bias Current vs. Input Common-Mode Voltage

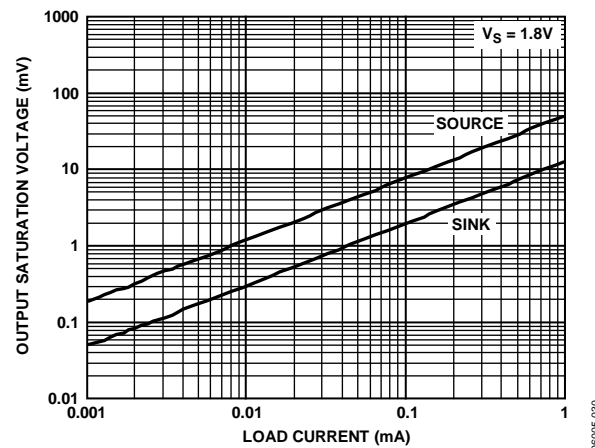


Figure 30. Output Saturation Voltage vs. Load Current

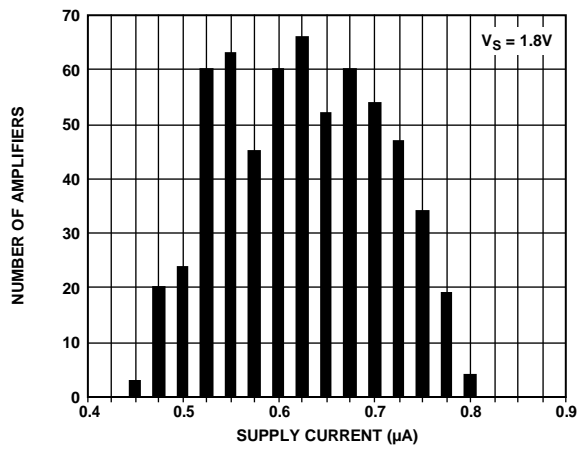


Figure 28. Supply Current Distribution

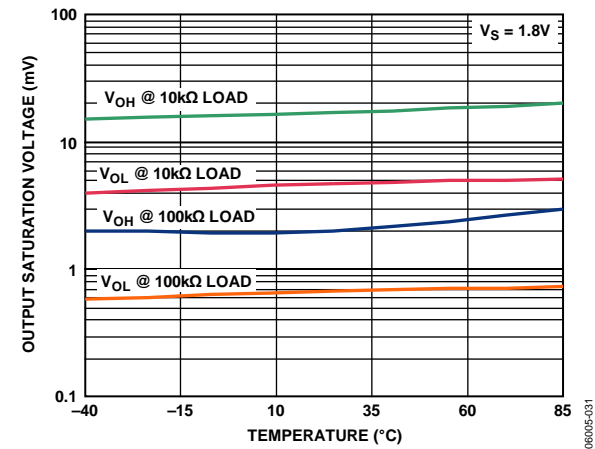


Figure 31. Output Saturation Voltage vs. Temperature

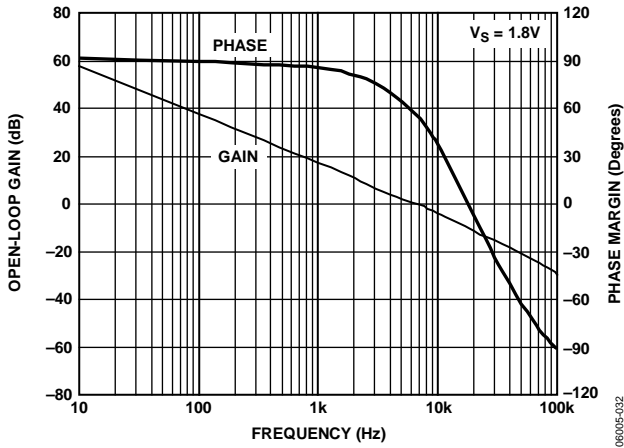


Figure 32. Open-Loop Gain and Phase vs. Frequency

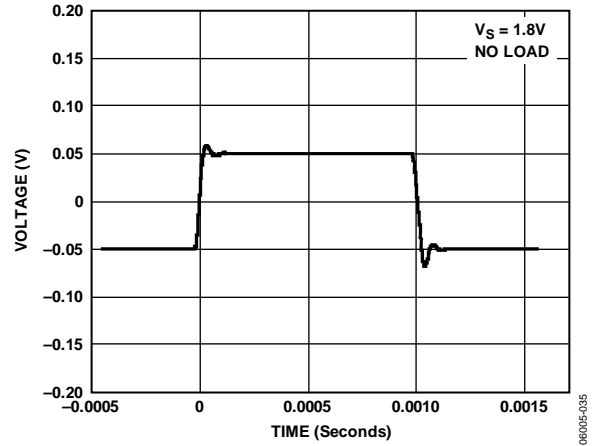


Figure 35. Small Signal Transient Response

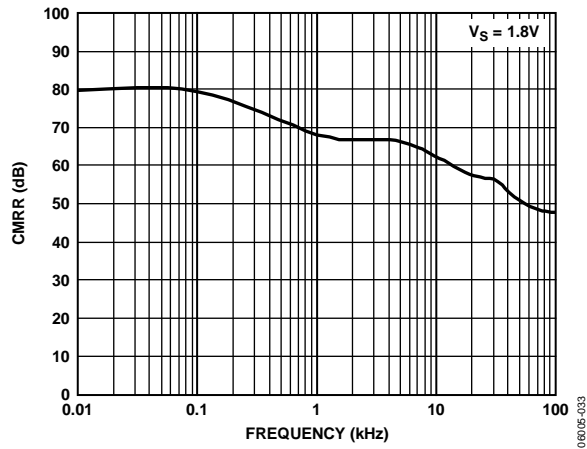


Figure 33. CMRR vs. Frequency

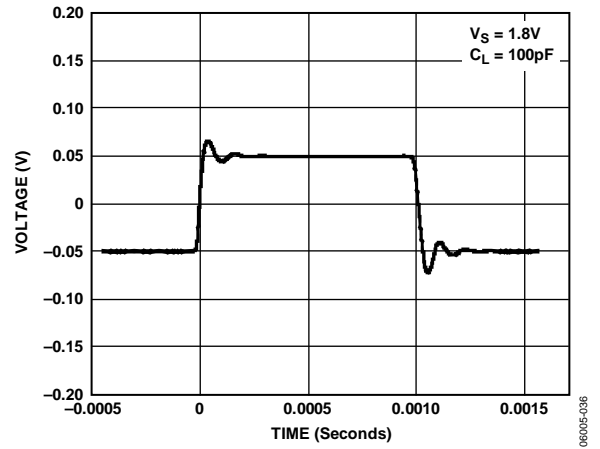


Figure 36. Small Signal Transient Response

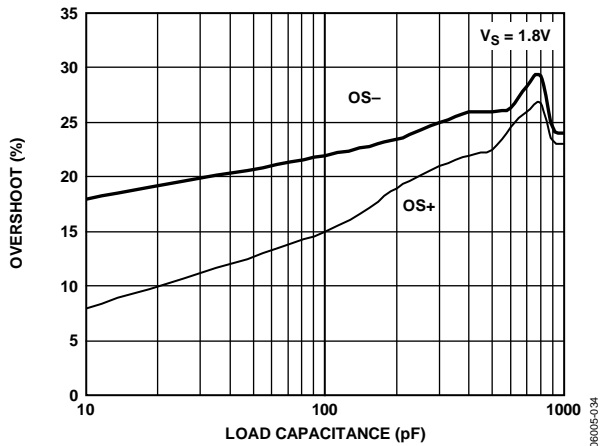


Figure 34. Small Signal Overshoot vs. Load Capacitance

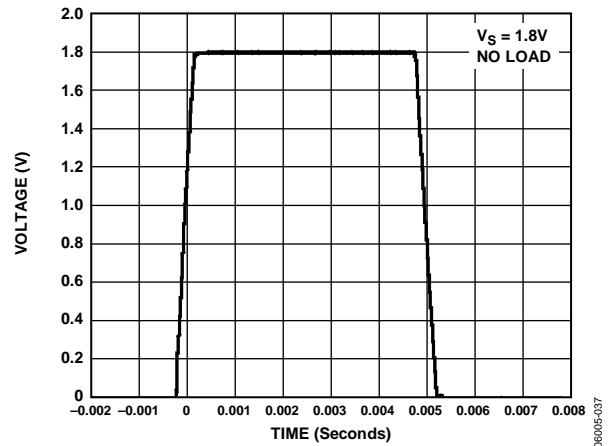
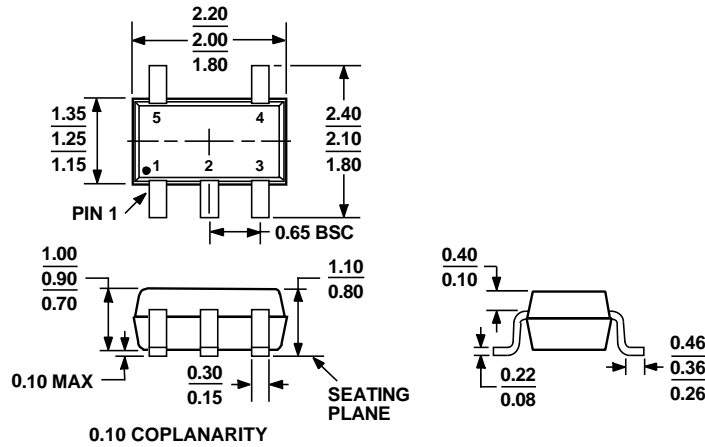


Figure 37. Large Signal Transient Response

AD8500

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-203-AA

Figure 38. 5-Lead Thin Shrink Small Outline Transistor Package [SC70] (KS-5)

Dimensions shown in millimeters

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding |
|-------------------------------|-------------------|---------------------|----------------|----------|
| AD8500AKSZ-R2 ¹ | -40°C to +125°C | 5-Lead SC70 | KS-5 | A0F |
| AD8500AKSZ-REEL ¹ | -40°C to +125°C | 5-Lead SC70 | KS-5 | A0F |
| AD8500AKSZ-REEL7 ¹ | -40°C to +125°C | 5-Lead SC70 | KS-5 | A0F |

¹ Z = RoHS Compliant Part.

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[561681F](#) [LT6005HGN#PBF](#) [LT6238CGN#PBF](#) [LT6238HGN#PBF](#) [OP05CN8#PBF](#) [LT6020IDD-1#PBF](#) [LT1124CS8#TR](#)
[NCV20166SN2T1G](#) [NCS20166SN2T1G](#) [NCS21802MUTBG](#) [LT1637MPS8](#) [LT1498IS8](#) [LT1492CS8](#) [TLC27L7CP](#) [TLV2473CDR](#)
[LMP2234AMA/NOPB](#) [LMP7707MA/NOPB](#) [5962-8859301M2A](#) [LMP2231AMAE/NOPB](#) [LMP2234AMTE/NOPB](#) [LMC6022IM/NOPB](#)
[LMC6024IM/NOPB](#) [LMC6081IMX/NOPB](#) [LMP2011MA/NOPB](#) [LMP2231AMFE/NOPB](#) [LMP2232BMA/NOPB](#) [LMP2234AMAE/NOPB](#)
[LMP7717MAE/NOPB](#) [LMV2011MA/NOPB](#) [LT1013DDR](#) [TL034ACDR](#) [TLC2201AMDG4](#) [TLE2024BMDWG4](#) [TS9222IYDT](#)
[TLV2474AQDRG4Q1](#) [TLV2472QDRQ1](#) [TLC4502IDR](#) [TLC27M2ACP](#) [TLC2652Q-8DG4](#) [OPA2107APG4](#) [TL054AIDR](#) [AD8619WARZ-](#)
[R7](#) [TLC272CD](#) [AD8539ARMZ](#) [LTC6084HDD#PBF](#) [LTC1050CN8#PBF](#) [LT1996AIDD#PBF](#) [LT1112CN8#PBF](#) [LTC6087CDD#PBF](#)
[LT1078S8#PBF](#)