1.8 V to 5 V Auto-Zero, In-Amp with Shutdown

AD8553

FEATURES

Low offset voltage: 20 µV max
Low input offset drift: 0.1 µV/°C max
High CMR: 120 dB min @ G = 100
Low noise: 0.7 µV p-p from 0.01 Hz to 10 Hz
Wide gain range: 0.1 to 10,000
Single-supply operation: 1.8 V to 5.5 V
Rail-to-rail output
Shutdown capability

APPLICATIONS

Strain gauge
Weigh scales
Pressure sensors
Laser diode control loops
Portable medical instruments
Thermocouple amplifiers

PIN CONFIGURATION

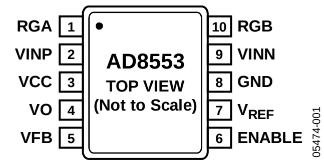

Figure 1. 10-Lead MSOP

GENERAL DESCRIPTION

The AD8553 is a precision instrumentation amplifier featuring low noise, rail-to-rail output and a power-saving shutdown mode. The AD8553 also features low offset voltage and drift coupled with high common-mode rejection. In shutdown mode, the total supply current is reduced to less than 4 µA. The AD8553 is capable of operating from 1.8 V to 5.5 V.

With a low offset voltage of 20 µV, an offset voltage drift of 0.1 µV/°C, and a voltage noise of only 0.7 µV p-p (0.01 Hz to 10 Hz), the AD8553 is ideal for applications where error sources cannot be tolerated. Precision instrumentation, position and pressure sensors, medical instrumentation, and strain gauge amplifiers benefit from the low noise, low input bias current, and high common-mode rejection. The small footprint and low cost are ideal for high volume applications.

The small package and low power consumption allow maximum channel density and minimum board size for space-critical equipment and portable systems.

The AD8553 is specified over the industrial temperature range from −40°C to +85°C. The AD8553 is available in a Pb-free, 10-lead MSOP.

Rev. A

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REVISION HISTORY

8/10—Rev. 0 to Rev. A

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10/05—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0 V, V_{CM} = 2.5 V, V_{REF} = V_{CC}/2, V_{IN} = V_{INP} − V_{INN}, R_{LOAD} = 10 kΩ, T_A = 25°C, G = 100, unless specified. See Table 5 for gain setting resistor values. Temperature specifications guaranteed by characterization.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}	G = 1000		4	20	μV
		G = 100		4	20	μV
		G = 10		15	50	μV
		G = 1		120	375	μV
vs. Temperature	$\Delta V_{OS}/\Delta T$	G = 1000, −40°C ≤ T_A ≤ +85°C		0.02	0.1	μV/°C
		G = 100, −40°C ≤ T_A ≤ +85°C		0.02	0.1	μV/°C
		G = 10, −40°C ≤ T_A ≤ +85°C		0.1	0.3	μV/°C
		G = 1, −40°C ≤ T_A ≤ +85°C		1	3	μV/°C
Input Bias Current	I_B			0.4	1	nA
		−40°C ≤ T_A ≤ +85°C			2	nA
Input Offset Current	I_{OS}				2	nA
VREF Pin Current	I_{REF}			0.01	1	nA
Input Operating Impedance						
Differential				50‖1		MΩ‖pF
Common Mode				10‖10		GΩ‖pF
Input Voltage Range			0		3.3	V
Common-Mode Rejection	CMR	G = 100, V_{CM} = 0 V to 3.3 V, −40°C ≤ T_A ≤ +85°C	120	140		dB
		G = 10, V_{CM} = 0 V to 3.3 V, −40°C ≤ T_A ≤ +85°C	100	120		dB
Gain Error		G = 100, V_{CM} = 12.125 mV, V_O = 0.075 V to 4.925 V		0.10	0.3	%
		G = 10, V_{CM} = 121.25 mV , V_O = 0.075 V to 4.925 V		0.15	0.4	%
Gain Drift		G = 10, 100, 1000, −40°C ≤ T_A ≤ +85°C		5	25	ppm/°C
		G = 1, −40°C ≤ T_A ≤ +85°C		30	50	ppm/°C
Nonlinearity		G = 100, V_{CM} = 12.125 mV, V_O = 0.075 V to 4.925 V		0.001	0.003	% FS
		G = 10, V_{CM} = 121.25 mV, V_O = 0.075 V to 4.925 V		0.040	0.060	% FS
V_{REF} Range			0.8		4.2	V
OUTPUT CHARACTERISITICS						
Output Voltage High	V_{OH}		4.925			V
Output Voltage Low	V_{OL}				0.075	V
Short-Circuit Current	I_{SC}			±35		mA
POWER SUPPLY						
Power Supply Rejection	PSR	G = 100, V_S = 1.8 V to 5.5 V, V_{CM} = 0 V	100	120		dB
		G = 10, V_S = 1.8 V to 5.5 V, V_{CM} = 0 V	90	110		dB
Supply Current	I_{SY}	I_O = 0 mA, V_{IN} = 0 V		1.1	1.3	mA
		−40°C ≤ T_A ≤ +85°C			1.5	mA
Supply Current Shutdown Mode	I_{SD}			2	4	μA
ENABLE INPUTS						
Logic High Voltage			2.40			V
Logic Low Voltage					0.80	V
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	f = 0.01 Hz to 10 Hz		0.7		μV p-p
Voltage Noise Density	e_n	G = 100, f = 1 kHz		30		nV/√Hz
		G = 10, f = 1 kHz		150		nV/√Hz
Internal Clock Frequency				60		kHz
Signal Bandwidth[1]		G = 1 to 1000		1		kHz

[1] Higher bandwidths result in higher noise.

V_S = 1.8 V, V_{CM} = -0 V, V_{REF} = V_S/2, V_{IN} = V_{INP} − V_{INN}, R_{LOAD} = 10 kΩ, T_A = 25°C, G = 100, unless specified. See Table 5 for gain setting resistor values. Temperature specifications guaranteed by characterization.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}	G = 1000		3	20	µV
		G = 100		3	20	µV
		G = 10		14	50	µV
		G = 1		130	375	µV
Vs. Temperature	$\Delta V_{OS}/\Delta T$	G = 1000, −40°C ≤ T_A ≤ +85°C		0.02	0.25	µV/°C
		G = 100, −40°C ≤ T_A ≤ +85°C		0.02	0.25	µV/°C
		G = 10, −40°C ≤ T_A ≤ +85°C		0.1	3	µV/°C
		G = 1, −40°C ≤ T_A ≤ +85°C		1	10	µV/°C
Input Bias Current	I_B			0.05	1	nA
		−40°C ≤ T_A ≤ +85°C			2	nA
Input Offset Current	I_{OS}				2	nA
VREF Pin Current	I_{REF}			0.02	1	nA
Input Operating Impedance						
Differential				50‖1		MΩ‖pF
Common Mode				10‖10		GΩ‖pF
Input Voltage Range			0		0.15	V
Common-Mode Rejection	CMR	G = 100, V_{CM} = 0 V to 0.15 V, −40°C ≤ T_A ≤ +85°C	100	110		dB
		G = 10, V_{CM} = 0 V to 0.15 V, −40°C ≤ T_A ≤ +85°C	90	110		dB
Gain Error		G = 100, V_{CM} =4.125 mV, V_O = 0.075 V to 1.725 V		0.2	0.4	%
		G = 10, V_{CM} = 41.25 mV, V_O = 0.075 V to 1.725 V		0.2	0.4	%
Gain Drift		G = 10, 100, 1000, −40°C ≤ T_A ≤ +85°C			25	ppm/°C
		G = 1, −40°C ≤ T_A ≤ +85°C			50	ppm/°C
Nonlinearity		G = 100, V_{CM} = 4.125 mV, V_O = 0.075 V to 1.725 V		0.003		% FS
		G = 10, V_{CM} = 41.25 mV, V_O = 0.075 V to 1.725 V		0.010		% FS
V_{REF} Range			0.8		1.0	V
OUTPUT CHARACTERISITICS						
Output Voltage High	V_{OH}		1.725			V
Output Voltage Low	V_{OL}				0.075	V
Short-Circuit Current	I_{SC}			±5		mA
POWER SUPPLY						
Power Supply Rejection	PSR	G = 100, V_S = 1.8 V to 5.5 V, V_{CM} = 0 V	100	120		dB
Supply Current	I_{SY}	I_O = 0 mA, V_{IN} = 0 V		0.8	1.2	mA
		−40°C ≤ T_A ≤ +85°C			1.4	mA
Supply Current Shutdown Mode	I_{SD}			2	4	µA
ENABLE INPUTS						
Logic High Voltage			1.4			V
Logic Low Voltage					0.5	V
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	f = 0.01 Hz to 10 Hz		0.7		µV p-p
Voltage Noise Density	e_n	G = 100, f = 1 kHz		30		nV/√Hz
		G = 10, f = 1 kHz		150		nV/√Hz
Internal Clock Frequency				60		kHz
Signal Bandwidth[1]		G = 1 to 1000		1		kHz

[1] Higher bandwidths result in higher noise.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Ratings
Supply Voltage	6 V
Input Voltage	$+V_{SUPPLY}$
Differential Input Voltage[1]	$\pm V_{SUPPLY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range (RM Package)	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range (RM Package)	−65°C to +150°C
Lead Temperature Range (Soldering, 10 sec)	300°C

[1] Differential input voltage is limited to ±5.0 V, the supply voltage, or whichever is less.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4.

Package Type	θ_{JA}[1]	θ_{JC}	Unit
10-Lead MSOP (RM)	110	32.2	°C/W

[1] θ_{JA} is specified for the nominal conditions, that is, θ_{JA} is specified for the device soldered on a circuit board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, G = 100, unless specified, see Table 5 for gain setting resistor values. Filters as noted are the combination of R2/C2 and R3/C3 as in Figure 31.

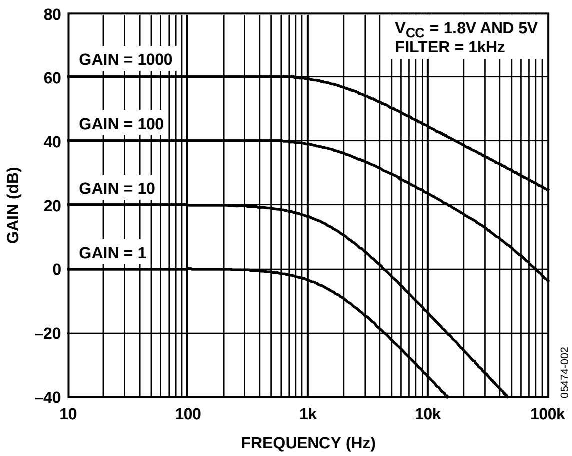

Figure 2. Gain vs. Frequency

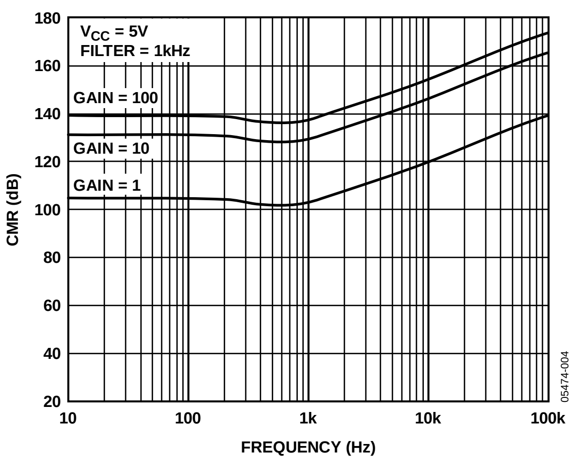

Figure 3. Common-Mode Rejection (CMR) vs. Frequency

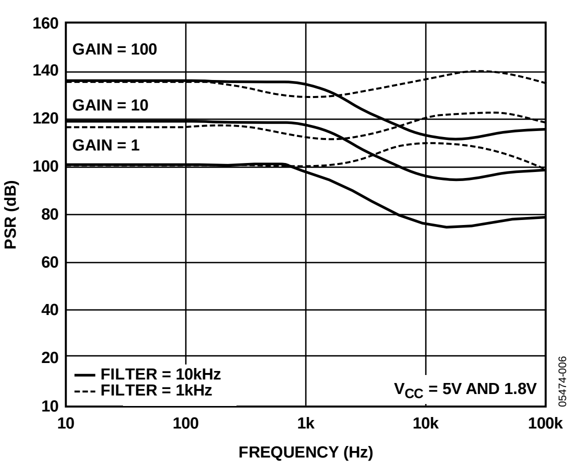

Figure 4. Power Supply Rejection vs. Frequency

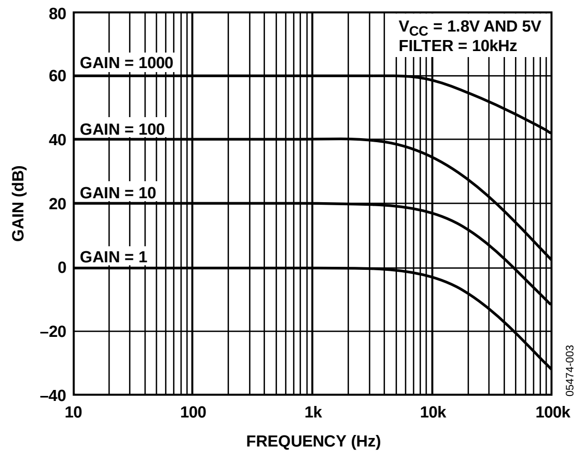

Figure 5. Gain vs. Frequency

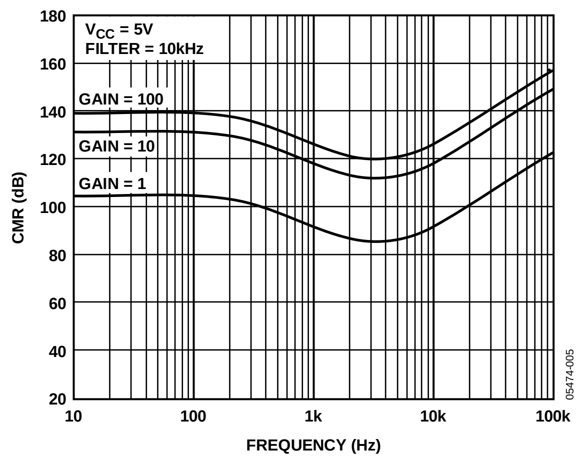

Figure 6. Common-Mode Rejection (CMR) vs. Frequency

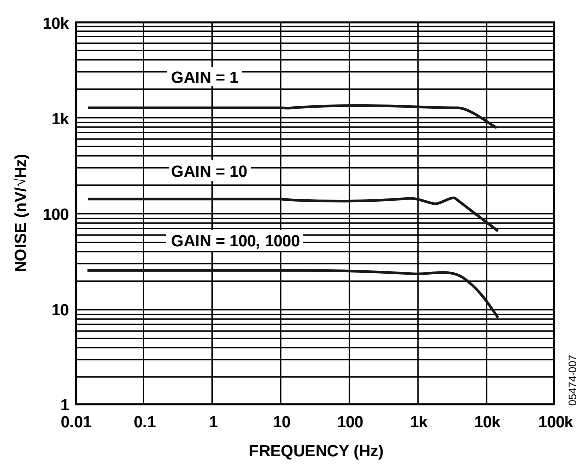

Figure 7. Voltage Noise Density

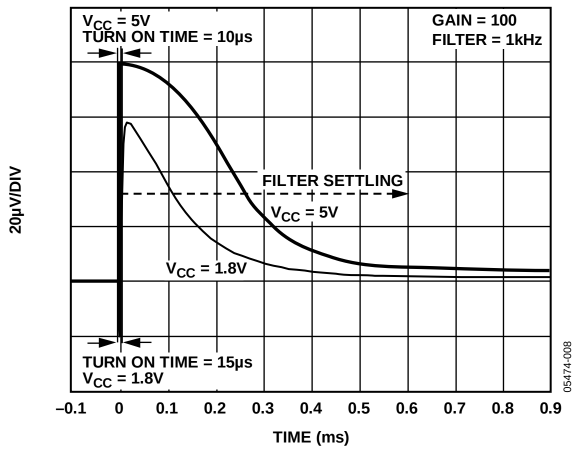

Figure 8. Input Offset Voltage vs. Turn-On Time

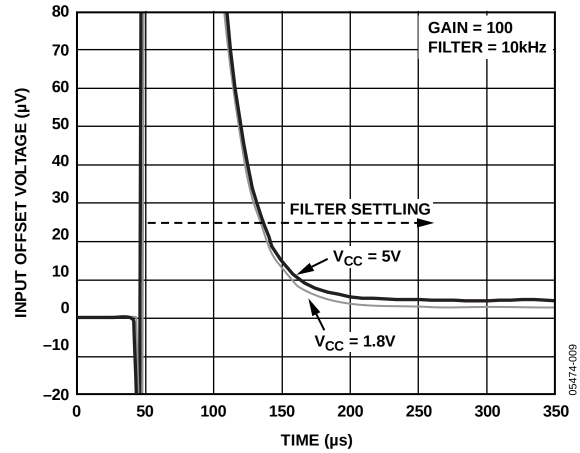

Figure 11. Input Offset Voltage vs. Turn-On Time

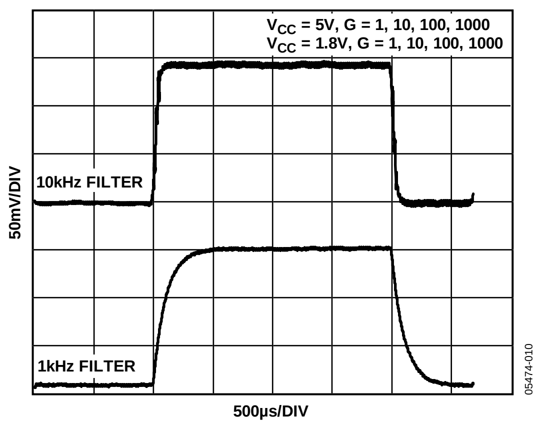

Figure 9. Small Signal Step Response

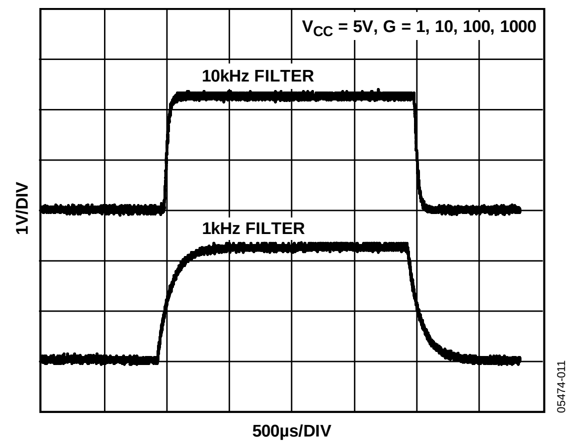

Figure 12. Large Signal Step Response

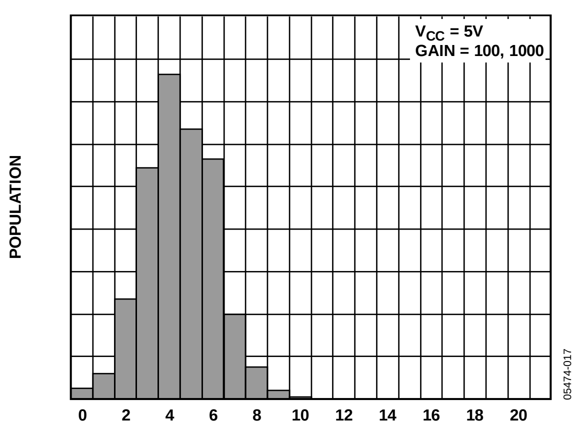

Figure 10. Input Offset Voltage (µV)

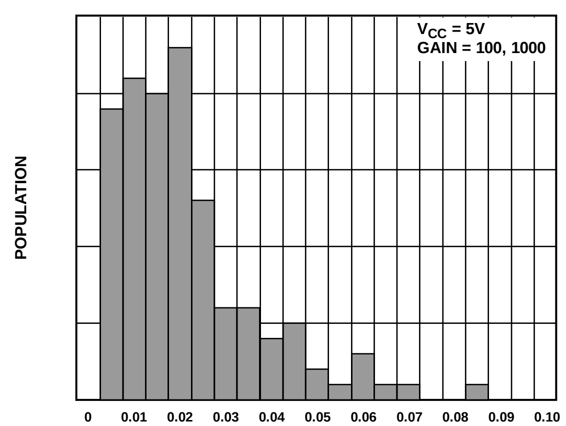

Figure 13. Input Offset Voltage Drift (µV/°C)

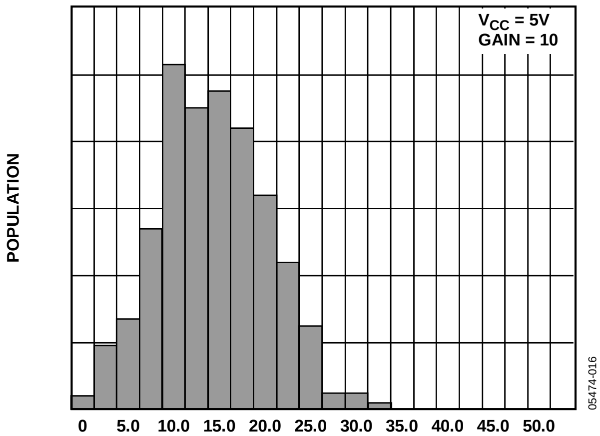

Figure 14. Input Offset Voltage (μV)

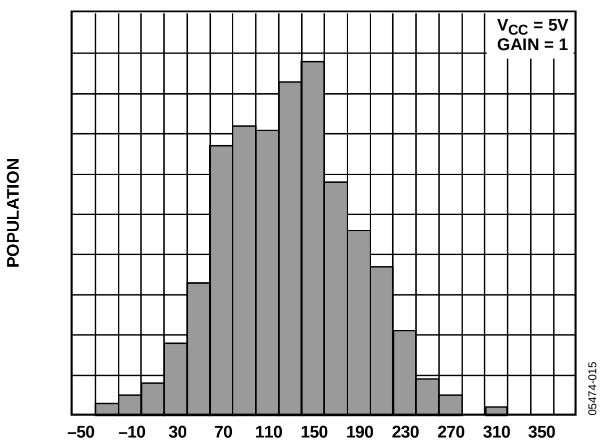

Figure 15. Input Offset Voltage (μV)

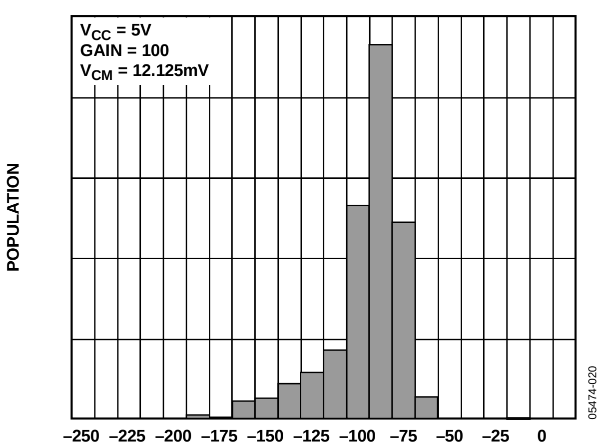

Figure 16. Gain Error (m%)

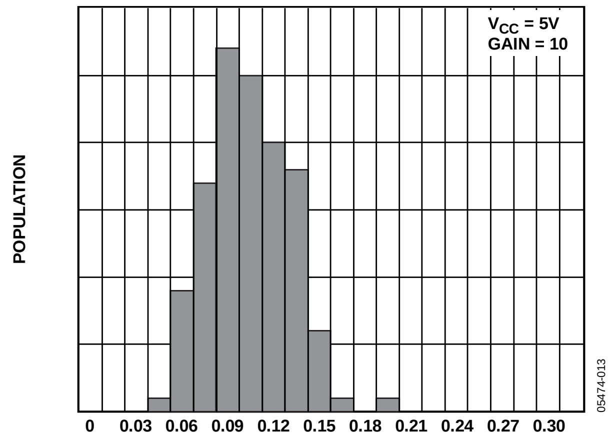

Figure 17. Input Offset Voltage Drift (μV/°C)

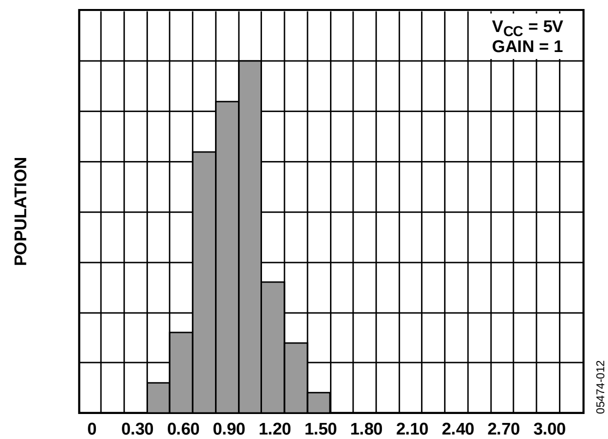

Figure 18. Input Offset Voltage Drift (μV/°C)

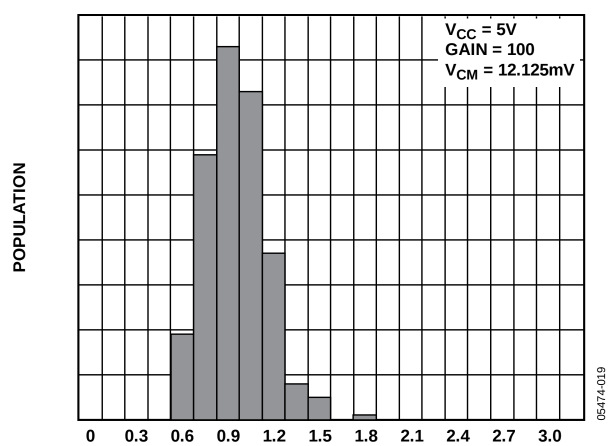

Figure 19. Nonlinearity (m%)

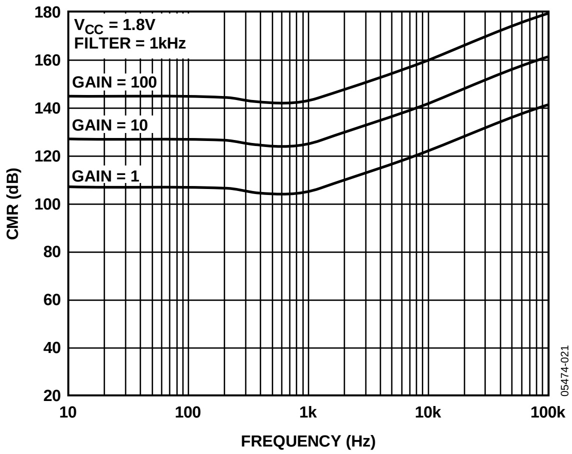

Figure 20. Common-Mode Rejection (CMR) vs. Frequency

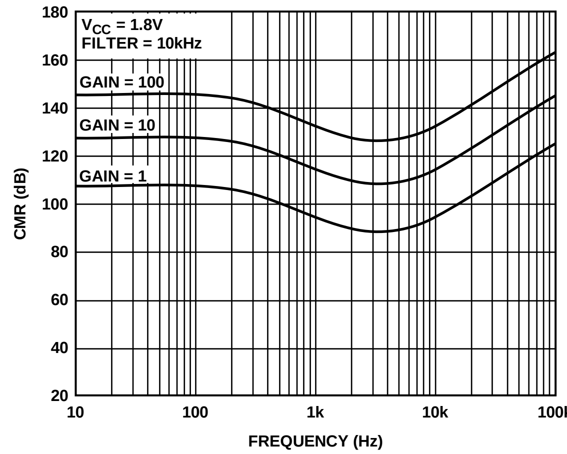

Figure 23. Common-Mode Rejection (CMR) vs. Frequency

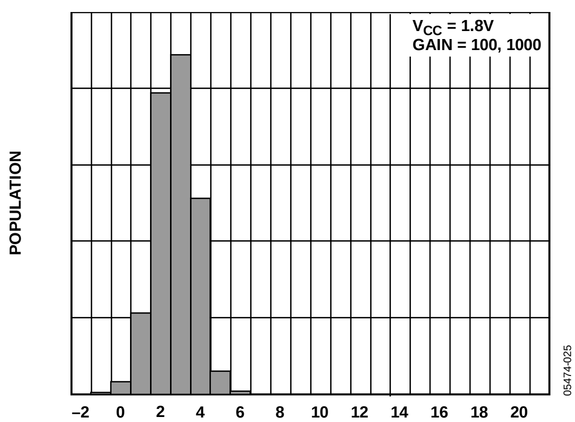

Figure 21. Input Offset Voltage (μV)

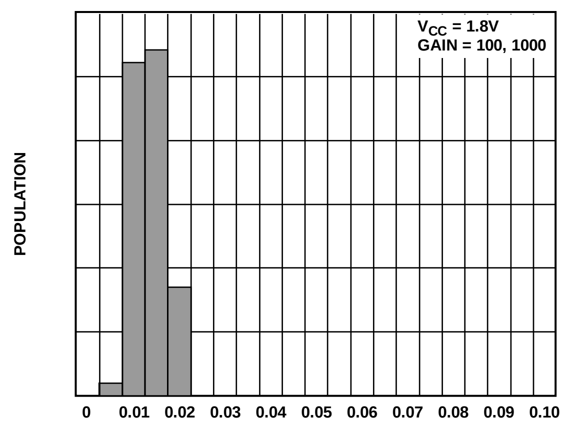

Figure 24. Input Offset Voltage Drift (μV/°C)

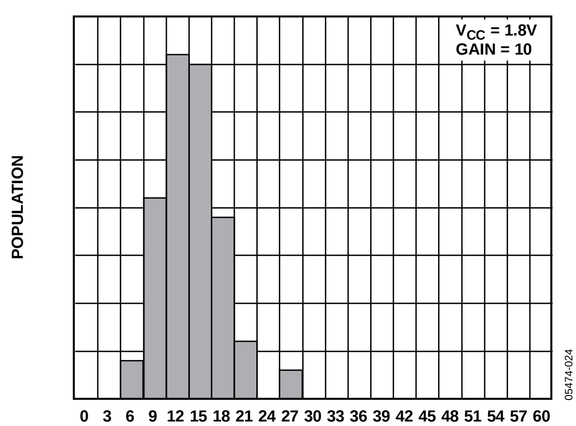

Figure 22. Input Offset Voltage (μV)

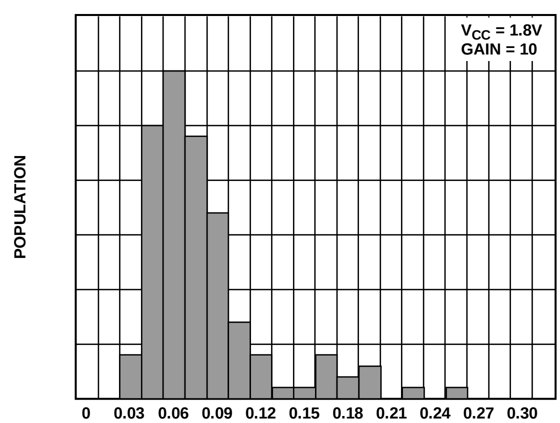

Figure 25. Input Offset Voltage Drift (μV/°C)

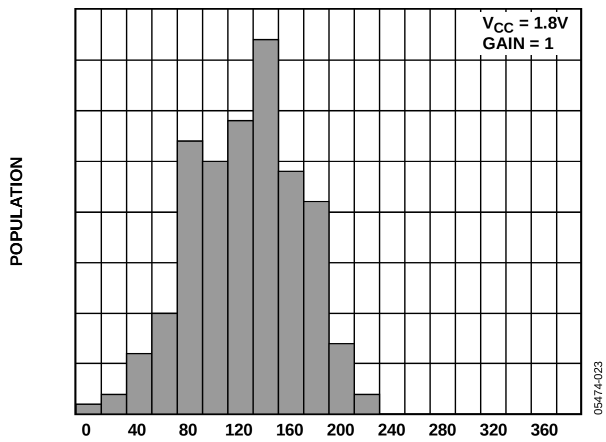

Figure 26. Input Offset Voltage (μV)

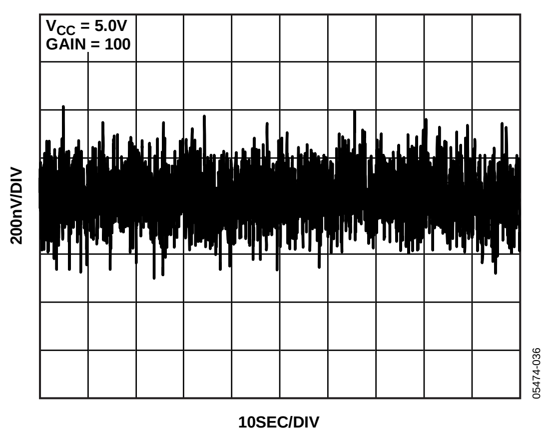

Figure 27. 0.01 Hz to 10 Hz Voltage Noise

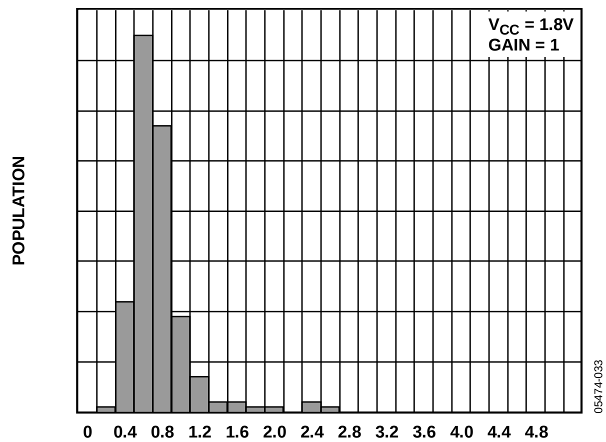

Figure 28. Input Offset Voltage Drift (μV/°C)

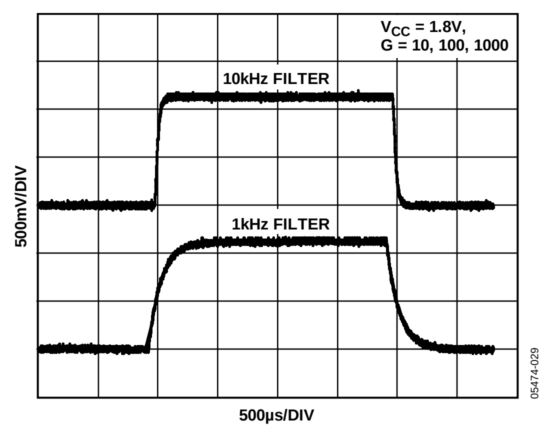

Figure 29. Large Signal Step Response

THEORY OF OPERATION

The AD8553 is a precision current-mode correction instrumentation amplifier capable of single-supply operation. The current-mode correction topology results in excellent accuracy without the need for trimmed resistors on the die.

Figure 30 shows a simplified diagram illustrating the basic operation of the AD8553 (without correction). The circuit consists of a voltage-to-current amplifier (M1 to M6), followed by a current-to-voltage amplifier (R2 and A1). Application of a differential input voltage forces a current through External Resistor R1, resulting in conversion of the input voltage to a signal current. Transistor M3 to Transistor M6 transfer twice this signal current to the inverting input of the op amp A1. Amplifier A1 and External Resistor R2 form a current-to-voltage converter to produce a rail-to-rail output voltage at V_{OUT}.

Op amp A1 is a high precision auto-zero amplifier. This amplifier preserves the performance of the autocorrecting, current-mode amplifier topology while offering the user a true voltage-in, voltage-out instrumentation amplifier. Offset errors are corrected internally.

An external reference voltage is applied to the noninverting input of A1 to set the output reference level. External Capacitor C2 is used to filter out correction noise.

The pinout of the AD8553 allows the user to access the signal current from the output of the voltage-to-current converter (Pin 5). The user can choose to use the AD8553 as a current-output device instead of a voltage-output device. See Figure 35 for circuit connections.

HIGH PSR AND CMR

Common-mode rejection and power supply rejection indicate the amount that the offset voltage of an amplifier changes when its common-mode input voltage or power supply voltage changes. The autocorrection architecture of the AD8553 continuously corrects for offset errors, including those induced by changes in input or supply voltage, resulting in exceptional rejection performance. The continuous autocorrection provides great CMR and PSR performances over the entire operating temperature range (−40°C to +85°C).

The parasitic resistance in series with R2 does not degrade CMR but causes a small gain error and a very small offset error. Therefore, an external buffer amplifier is not required to drive the V_{REF} pin to maintain excellent CMR performance. This helps reduce system costs over conventional instrumentation amplifiers.

1/f NOISE CORRECTION

Flicker noise, also known as 1/f noise, is noise inherent in the physics of semiconductor devices and decreases 10 dB per decade. The 1/f corner frequency of an amplifier is the frequency at which the flicker noise is equal to the broadband noise of the amplifier. At lower frequencies, flicker noise dominates causing large errors in low frequency or dc applications.

Flicker noise is seen effectively as a slowly varying offset error, which is reduced by the autocorrection topology of the AD8553. This allows the AD8553 to have lower noise near dc than standard low noise instrumentation amplifiers.

APPLICATIONS

GAIN SELECTION (GAIN-SETTING RESISTORS)

The gain of the AD8553 is set according to

$$G = 2 \times (R2/R1) \quad (1)$$

Table 5 lists the recommended resistor values. Resistor R1 must be at least 3.92 kΩ for proper operation. Use of resistors larger than the recommended values results in higher offset and higher noise.

Gain accuracy depends on the matching of R1 and R2. Any mismatch in resistor values results in a gain error. Resistor value errors due to drift affect gain by the amount indicated by Equation 1. However, due to the current-mode operation of the AD8553, a mismatch in R1 and R2 does not degrade the CMR.

Care should be taken when selecting and positioning the gain setting resistors. The resistors should be made of the same material and package style. Surface-mount resistors are recommended. They should be positioned as close together as possible to minimize TC errors.

To maintain good CMR vs. frequency, the parasitic capacitance on the R1 gain setting pins should be minimized and matched. This also helps maintain a low gain error at $G < 10$.

If resistor trimming is required to set a precise gain, trim Resistor R2 only. Using a potentiometer for R1 degrades the amplifier's performance.

REFERENCE CONNECTION

Unlike traditional three op amp instrumentation amplifiers, parasitic resistance in series with V_{REF} (Pin 7) does not degrade CMR performance. This allows the AD8553 to attain its extremely high CMR performance without the use of an external buffer amplifier to drive the V_{REF} pin, which is required by industry-standard instrumentation amplifiers. This helps save valuable printed circuit board space and minimizes system costs.

For optimal performance in single-supply applications, V_{REF} should be set with a low noise precision voltage reference. However, for a lower system cost, the reference voltage can be set with a simple resistor voltage divider between the supply and ground (see Figure 31). This configuration results in degraded output offset performance if the resistors deviate from their ideal values. In dual-supply applications, V_{REF} can simply be connected to ground.

The V_{REF} pin current is approximately 20 pA, and as a result, an external buffer is not required.

DISABLE FUNCTION

The AD8553 provides a shutdown function to conserve power when the device is not needed. Although there is a 1 µA pull-up current on the ENABLE pin, Pin 6 should be connected to the positive supply for normal operation and to the negative supply to turn the device off. It is not recommended to leave Pin 6 floating.

Turn-on time upon switching Pin 6 high is dominated by the output filters. When the device is disabled, the output becomes high impedance enabling muxing application of multiple AD8553 instrumentation amplifiers.

OUTPUT FILTERING

Filter Capacitor C2 is required to limit the amount of switching noise present at the output. The recommended bandwidth of the filter created by C2 and R2 is 1.4 kHz. The user should first select R1 and R2 based on the desired gain, then select C2 based on

$$C2 = 1/(1400 \times 2 \times \pi \times R2) \quad (2)$$

Addition of another single-pole RC filter of 1.4 kHz on the output (R3 and C3 in Figure 31 to Figure 33) is required for bandwidths greater than 10 Hz. These two filters produce an overall bandwidth of 1 kHz.

When driving an ADC, the recommended values for the second filter are R3 = 100 Ω and C3 = 1 µF. This filter is required to achieve the specified performance. It also acts as an antialiasing filter for the ADC. If a sampling ADC is not being driven, the value of the capacitor can be reduced, but the filter frequency should remain unchanged.

For applications with low bandwidths (<10 Hz), only the first filter is required. In this case, the high frequency noise from the auto-zero amplifier (output amplifier) is not filtered before the following stage.

CLOCK FEEDTHROUGH

The AD8553 uses two synchronized clocks to perform the autocorrection. The input voltage-to-current amplifiers are corrected at 60 kHz.

Trace amounts of these clock frequencies can be observed at the output. The amount of feedthrough is dependent upon the gain, because the autocorrection noise has an input and output referred term. The correction feedthrough is also dependent upon the values of the external filters R2/C2, and R3/C3.

LOW IMPEDANCE OUTPUT

For applications where a low output impedance is required, the circuit in Figure 33 should be used. This provides the same filtering performance as shown in the configuration in Figure 34.

MAXIMIZING PERFORMANCE THROUGH PROPER LAYOUT

To achieve the maximum performance of the AD8553, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board.

Care must be taken to minimize parasitic capacitance on Pin 1 and Pin 10 (Resistor R1 connections). Traces from Pin 1 and Pin 10 to R1 should be kept short and symmetric. Excessive capacitance on these pins will result in a gain error. This effect is most prominent at low gains (G < 10).

For high impedance sources, the PC board traces from the AD8553 inputs should be kept to a minimum to reduce input bias current errors.

POWER SUPPLY BYPASSING

The AD8553 uses internally generated clock signals to perform the autocorrection. As a result, proper bypassing is necessary to achieve optimum performance. Inadequate or improper bypassing of the supply lines can lead to excessive noise and offset voltage.

A 0.1 μF surface-mount capacitor should be connected between the supply lines. This capacitor is necessary to minimize ripple from the correction clocks inside the IC. For dual-supply operation (see Figure 33), a 0.1 μF (ceramic) surface-mount capacitor should be connected from each supply pin to ground.

For single-supply operation, a 0.1 μF surface-mount capacitor should be connected from the supply line to ground.

All bypass capacitors should be positioned as close to the DUT supply pins as possible, especially the bypass capacitor between the supplies. Placement of the bypass capacitor on the back of the board directly under the DUT is preferred.

INPUT OVERVOLTAGE PROTECTION

All terminals of the AD8553 are protected against ESD. In the case of a dc overload voltage beyond either supply, a large current would flow directly through the ESD protection diodes. If such a condition should occur, an external resistor should be used in series with the inputs to limit current for voltages beyond the supply rails. The AD8553 can safely handle 5 mA of continuous current, resulting in an external resistor selection of $R_{EXT} = (V_{IN} - V_S)/5$ mA.

CAPACITIVE LOAD DRIVE

The output buffer, Pin 4, can drive capacitive loads up to 100 pF.

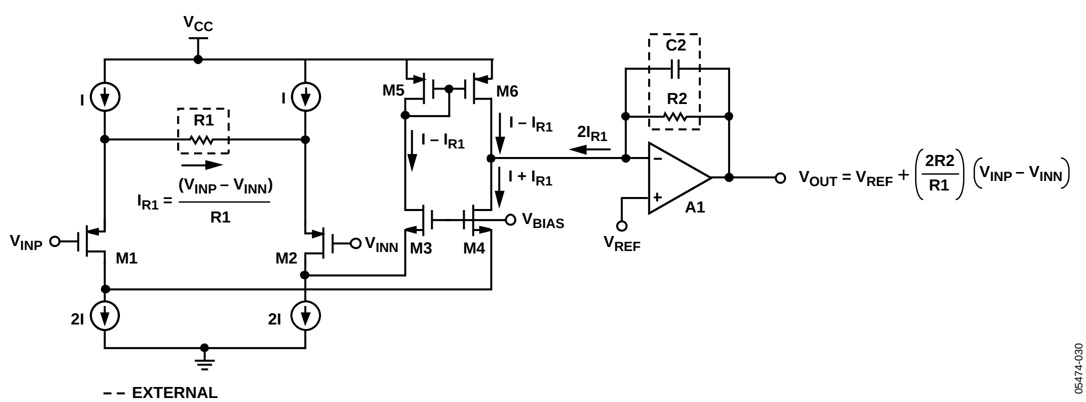

Figure 30. Simplified AD8553 Schematic

CIRCUIT DIAGRAMS/CONNECTIONS

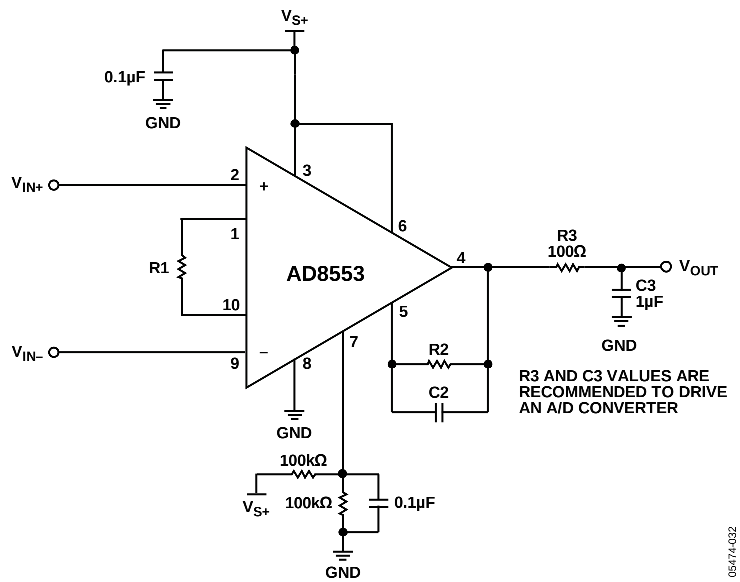

Figure 31. Single-Supply Connection Diagram Using Voltage Divider Reference

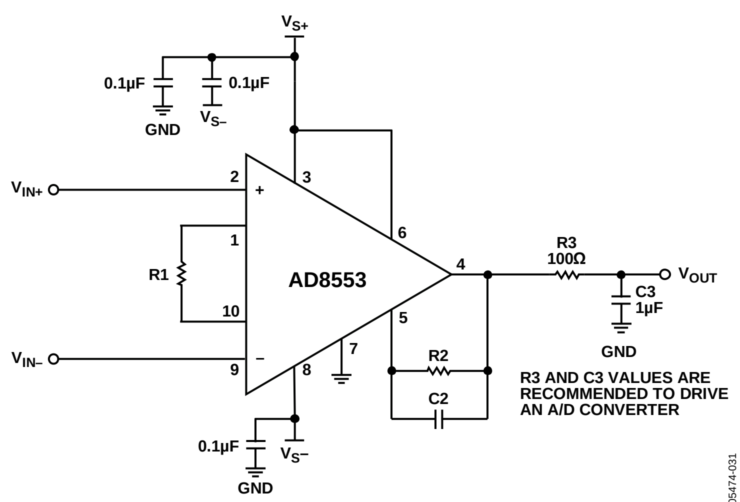

Figure 32. Dual-Supply Connection Diagram

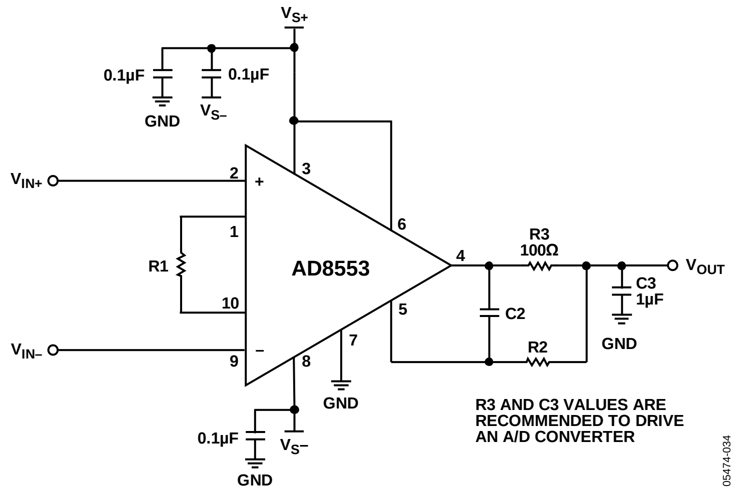

Figure 33. Dual-Supply Connection Diagram with Low Impedance Output

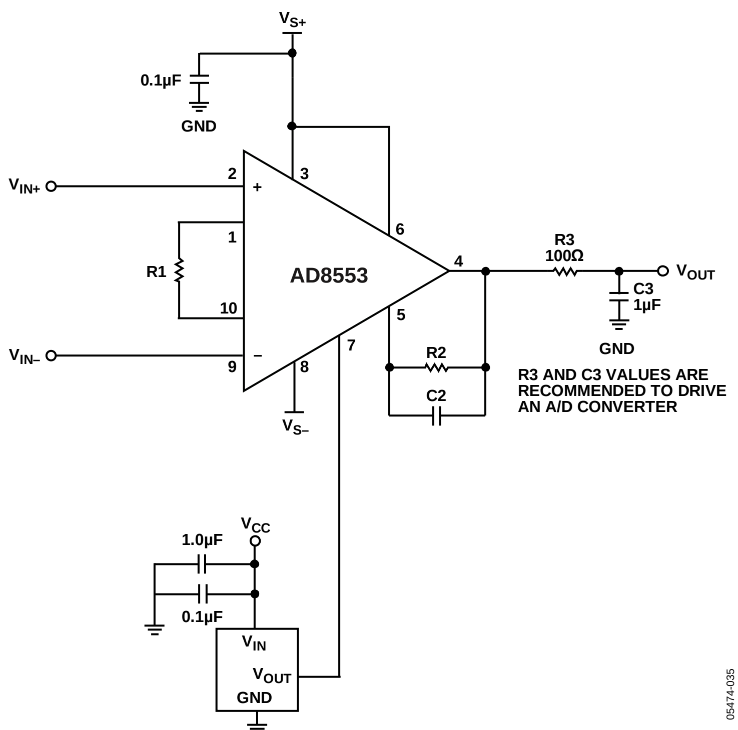

Figure 34. Dual-Supply Connection Diagram Using IC Voltage Reference

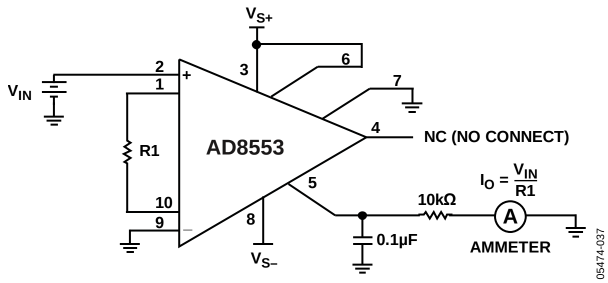

Figure 35. Voltage-to-Current Converter, 0 µA to 30 µA Source

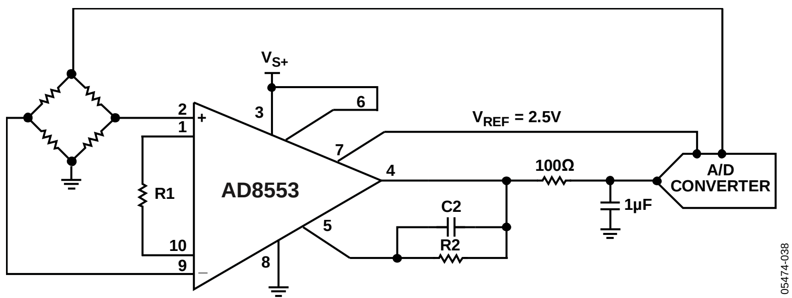

Figure 36. Example of an AD8553 Driving a Converter at V_{S+} = 5 V

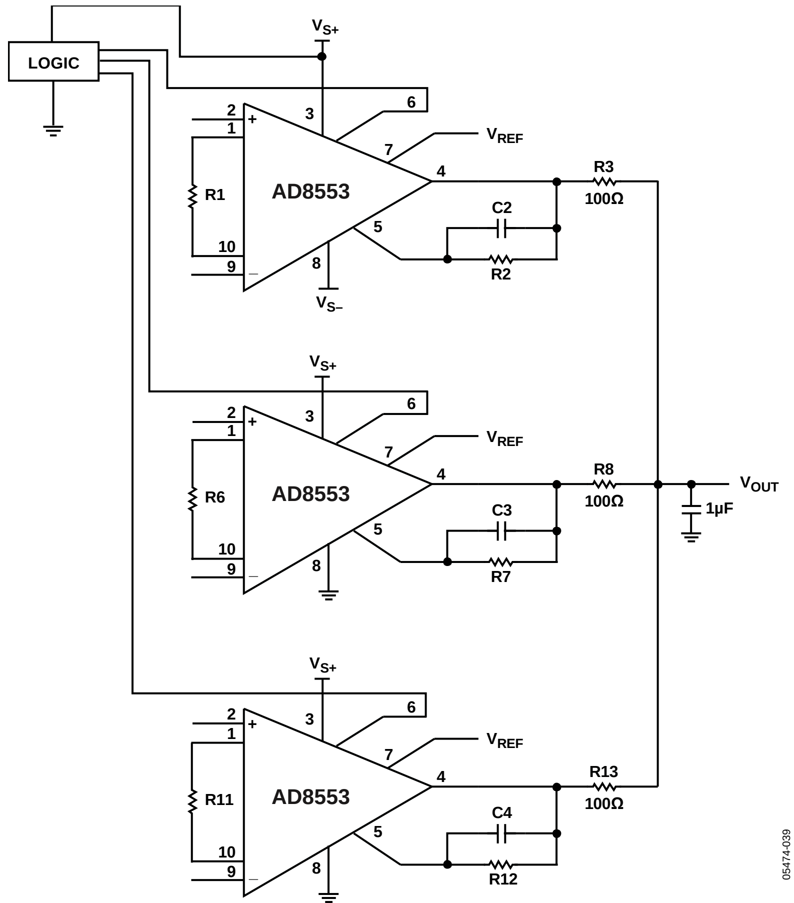

Figure 37. Multiplexed Output

Table 5. Recommended External Component Values for Selected Gains

Desired Gain (V/V)	R1 (Ω)	R2 || C2 (Ω || F)	Calculated Gain
1	200 k	100 k || 1200p	1
2	100 k	100 k || 1200p	2
5	40.2 k	100 k || 1200p	4.975
10	20 k	100 k || 1200p	10
50	4.02 k	100 k || 1200p	49.75
100	3.92 k	196 k || 560p	100
500	3.92 k	976 k || 120p	497.95
1000	3.92 k	1.96 M || 56p	1000

OUTLINE DIMENSIONS

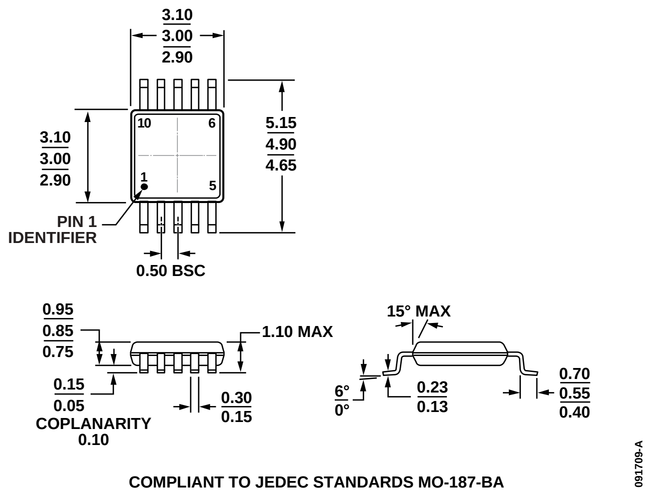

Figure 38. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8553ARMZ	−40°C to +85°C	10-Lead MSOP	RM-10	A09
AD8553ARMZ-REEL	−40°C to +85°C	10-Lead MSOP	RM-10	A09

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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