

FEATURES

- Low voltage noise density: 1.15 nV/ $\sqrt{\text{Hz}}$ at 1 kHz**
- Low distortion: -120 dB total harmonic distortion plus noise (THD + N) at 1 kHz**
- Peak-to-peak noise: 76 nV p-p at 0.1 Hz to 10 Hz**
- Slew rate: 15 V/ μs at $V_{\text{SY}} = \pm 15$ V**
- Wide gain bandwidth product: 10 MHz**
- Supply current per amplifier: 5.0 mA typical at $V_{\text{SY}} = \pm 15$ V**
- Low offset voltage: 10 μV typical at $V_{\text{SY}} = \pm 15$ V**
- Common-mode rejection ratio (CMRR): 120 dB minimum**
- Unity-gain stable**
- Dual-supply operation: ± 15 V**

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)**
- Extended temperature range: -55°C to $+125^{\circ}\text{C}$**
- Controlled manufacturing baseline**
- One assembly/test site**
- One fabrication site**
- Enhanced product change notification**
- Qualification data available on request**

APPLICATIONS

- Professional audio preamplifiers**
- ATE/precision testers**
- Imaging systems**
- Medical/physiological measurements**
- Precision detectors/instruments**
- Precision data conversions**

GENERAL DESCRIPTION

The [AD8599-EP](#) is a very low noise, low distortion op amp ideal for use as a preamplifier. The low noise of 1.15 nV/ $\sqrt{\text{Hz}}$ and low harmonic distortion of -120 dB (or better) at audio bandwidths give the [AD8599-EP](#) the wide dynamic range necessary for preamplifiers in audio, medical, and instrumentation applications. The excellent slew rate of 15 V/ μs and 10 MHz gain bandwidth product make the [AD8599-EP](#) highly suitable for medical applications. The low distortion and fast settling time make the [AD8599-EP](#) ideal for buffering high resolution data converters.

PIN CONFIGURATION

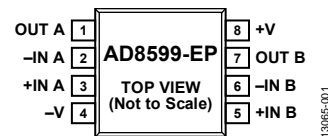


Figure 1.

130065-001

The [AD8599-EP](#) is available in an 8-lead SOIC package. It is specified over a -55°C to $+125^{\circ}\text{C}$ temperature range.

Additional application and technical information can be found in the [AD8599](#) data sheet.

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REVISION HISTORY

8/15—Revision 0: Initial Version

SPECIFICATIONS

$V_{SY} = \pm 15\text{ V}$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 1.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|-----------------------------------|--------------------------|--|-------|----------|-------|------------------------------|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | V_{OS} | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | 10 | 120 | μV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | 0.8 | 300 | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current | I_B | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | 25 | 200 | nA |
| Input Offset Current | I_{OS} | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | 50 | 200 | nA |
| Input Voltage Range | IVR | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | -12.5 | | +12.5 | V |
| Common-Mode Rejection Ratio | CMRR | $-12.5\text{ V} \leq V_{CM} \leq +12.5\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 120 | 135 | | dB |
| Large Signal Voltage Gain | A_{VO} | $R_L \geq 600\ \Omega$, $V_O = -11\text{ V to } +11\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 110 | 116 | | dB |
| Input Capacitance | | | | | | |
| Differential Capacitance | C_{DIFF} | | | 12.1 | | pF |
| Common-Mode Capacitance | C_{CM} | | | 5.1 | | pF |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage | | | | | | |
| High | V_{OH} | $R_L = 600\ \Omega$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 13.1 | 13.4 | | V |
| | | $R_L = 2\ \text{k}\Omega$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 12.8 | 13.7 | | V |
| | | $R_L = 600\ \Omega$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 13.5 | 13.7 | | V |
| | | $R_L = 2\ \text{k}\Omega$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 13.2 | | | V |
| Low | V_{OL} | $R_L = 600\ \Omega$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | -13.2 | -12.9 | V |
| | | $R_L = 2\ \text{k}\Omega$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | | -12.8 | V |
| | | $R_L = 600\ \Omega$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | -13.5 | -13.4 | V |
| | | $R_L = 2\ \text{k}\Omega$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | | -13.3 | V |
| Output Short-Circuit Current | I_{SC} | | | ± 52 | | mA |
| Closed-Loop Output Impedance | Z_{OUT} | At 1 MHz, $A_{VO} = 1$ | | 5 | | Ω |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_{SY} = \pm 18\text{ V to } \pm 4.5\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 120 | 140 | | dB |
| Supply Current per Amplifier | I_{SY} | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | 118 | 5.0 | 5.7 | dB |
| | | | | | 6.75 | mA |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $A_{VO} = -1$, $R_L = 2\ \text{k}\Omega$ $A_{VO} = 1$, $R_L = 2\ \text{k}\Omega$ | | 16 | | V/ μs |
| Settling Time | t_S | To 0.01%, step = 10 V | | 15 | | V/ μs |
| Gain Bandwidth Product | GBP | | | 2 | | μs |
| Phase Margin | Φ_M | | | 10 | | MHz |
| | | | | 65 | | Degrees |
| NOISE PERFORMANCE | | | | | | |
| Peak-to-Peak Noise | e_n p-p | 0.1 Hz to 10 Hz | | 76 | | nV p-p |
| Voltage Noise Density | e_n | $f = 1\ \text{kHz}$ | | 1.07 | 1.15 | nV/ $\sqrt{\text{Hz}}$ |
| | | $f = 10\ \text{Hz}$ | | | 1.5 | nV/ $\sqrt{\text{Hz}}$ |
| Correlated Current Noise | | $f = 1\ \text{kHz}$ | | 1.9 | | pA/ $\sqrt{\text{Hz}}$ |
| | | $f = 10\ \text{Hz}$ | | 4.3 | | pA/ $\sqrt{\text{Hz}}$ |
| Uncorrelated Current Noise | | $f = 1\ \text{kHz}$ | | 2.3 | | pA/ $\sqrt{\text{Hz}}$ |
| | | $f = 10\ \text{Hz}$ | | 5.3 | | pA/ $\sqrt{\text{Hz}}$ |
| Total Harmonic Distortion + Noise | THD + N | $G = 1$, $R_L \geq 1\ \text{k}\Omega$, $f = 1\ \text{kHz}$, $V_{RMS} = 3\text{ V}$ | | -120 | | dB |
| Channel Separation | CS | $f = 10\ \text{kHz}$ | | -120 | | dB |

ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter | Rating |
|---|--------------------------|
| Supply Voltage | ±18 V |
| Input Voltage | $-V \leq V_{IN} \leq +V$ |
| Differential Input Voltage ¹ | ±1 V |
| Output Short-Circuit to GND | Indefinite |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range | −55°C to +125°C |
| Lead Temperature (Soldering 60 sec) | 300°C |
| Junction Temperature | 150°C |

¹ If the differential input voltage exceeds 1 V, limit the current to 5 mA.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified with the device soldered on a circuit board with its exposed paddle soldered to a pad (if applicable) on a 4-layer JEDEC standard PCB with zero air flow.

Table 3.

| Package Type | θ_{JA} | θ_{JC} | Unit |
|-------------------|---------------|---------------|------|
| 8-Lead SOIC (R-8) | 120 | 36 | °C/W |

POWER SEQUENCING

Apply the op amp supplies simultaneously. The op amp supplies must be stable before any input signals are applied. In any case, the input current must be limited to 5 mA.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

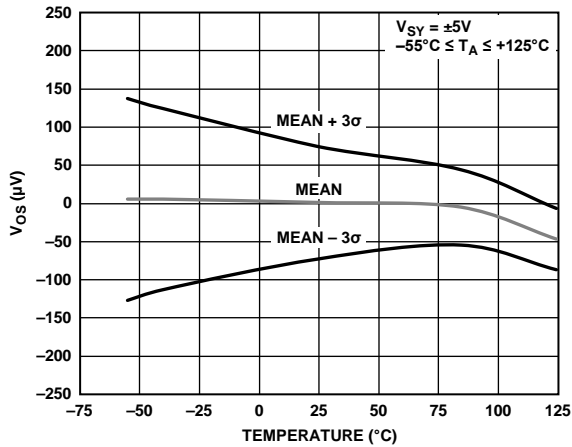


Figure 2. Input Offset Voltage (V_{OS}) Distribution, $V_{SY} = \pm 5 V$

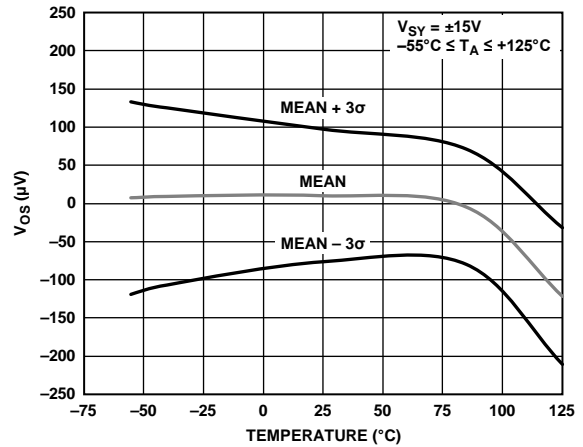


Figure 5. Input Offset Voltage (V_{OS}) Distribution, $V_{SY} = \pm 15 V$

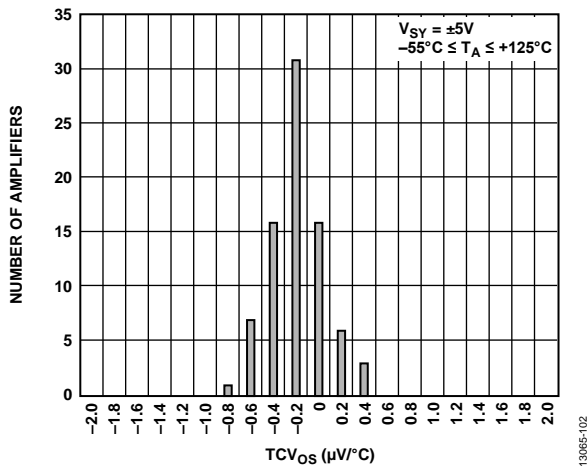


Figure 3. Input Offset Voltage Drift (TCV_{OS}) Distribution, $V_{SY} = \pm 5 V$

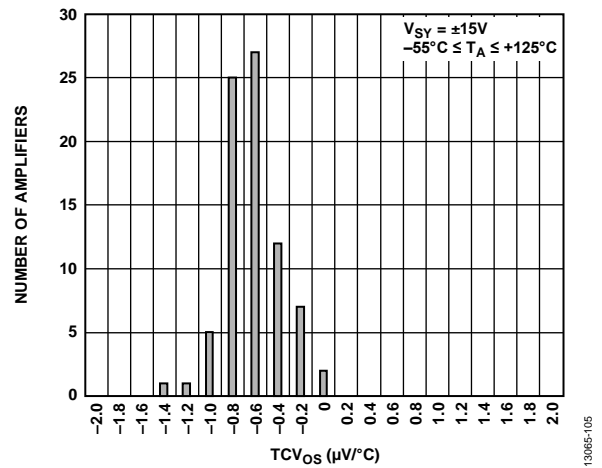


Figure 6. Input Offset Voltage Drift (TCV_{OS}) Distribution, $V_{SY} = \pm 15 V$

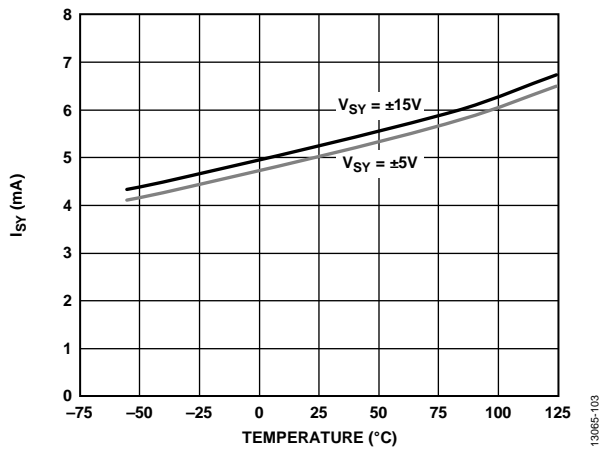


Figure 4. Supply Current (I_{SY}) vs. Temperature

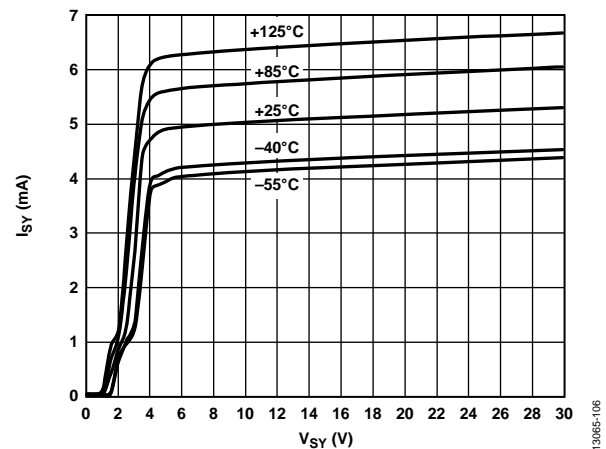


Figure 7. Supply Current (I_{SY}) vs. Supply Voltage (V_{SY})

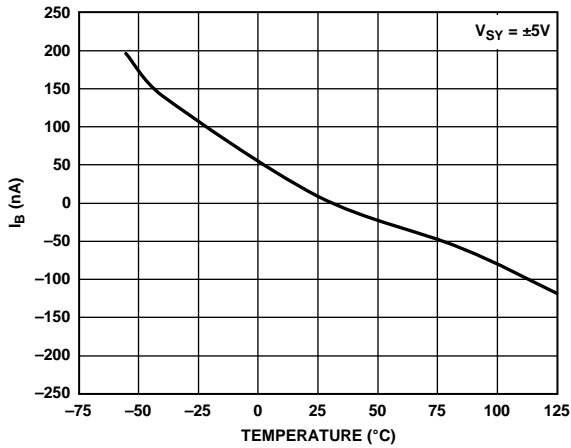


Figure 8. Input Bias Current (I_b) vs. Temperature, $V_{SY} = \pm 5 V$

13085-107

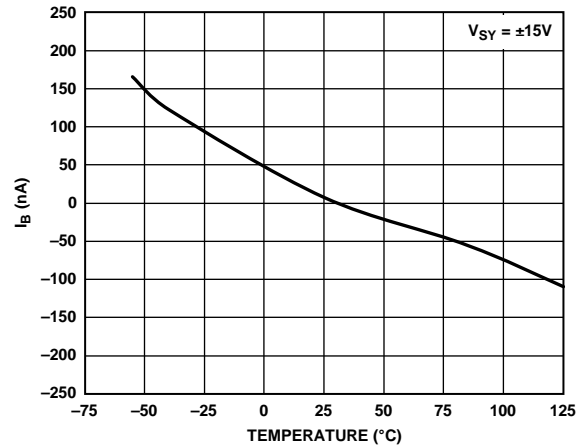


Figure 11. Input Bias Current (I_b) vs. Temperature, $V_{SY} = \pm 15 V$

13085-110

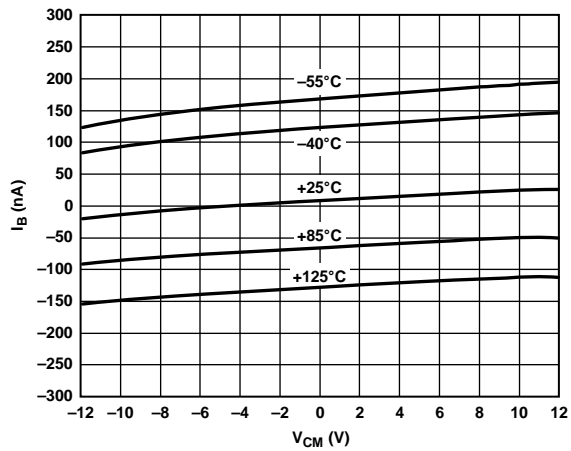


Figure 9. Input Bias Current (I_b) vs. Common-Mode Voltage (V_{CM})

13085-108

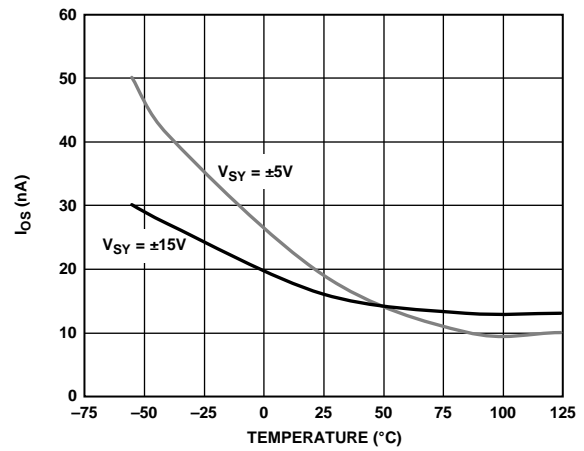


Figure 12. Input Offset Current (I_{os}) vs. Temperature

13085-111

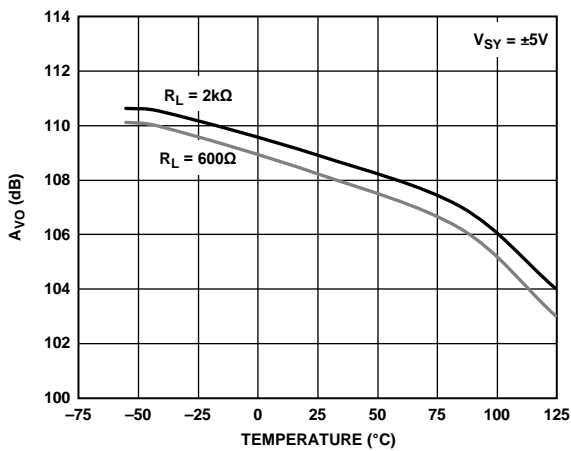


Figure 10. Large Signal Voltage Gain (A_{VO}) vs. Temperature, $V_{SY} = \pm 5 V$

13085-109

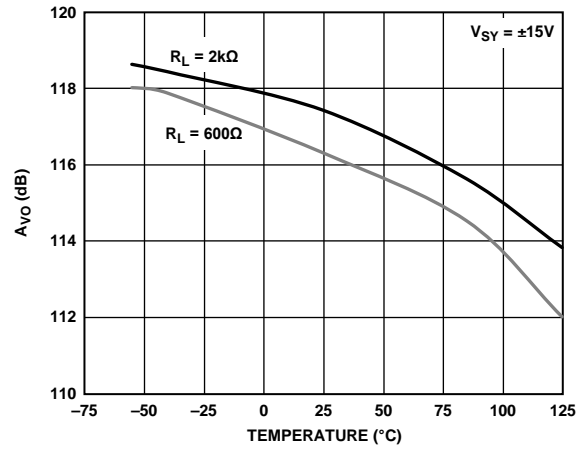


Figure 13. Large Signal Voltage Gain (A_{VO}) vs. Temperature

13085-112

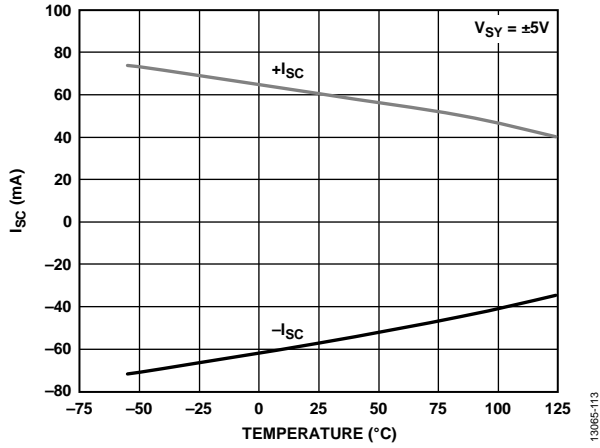


Figure 14. Output Short-Circuit Current (I_{SC}) vs. Temperature, $V_{SY} = \pm 5 V$

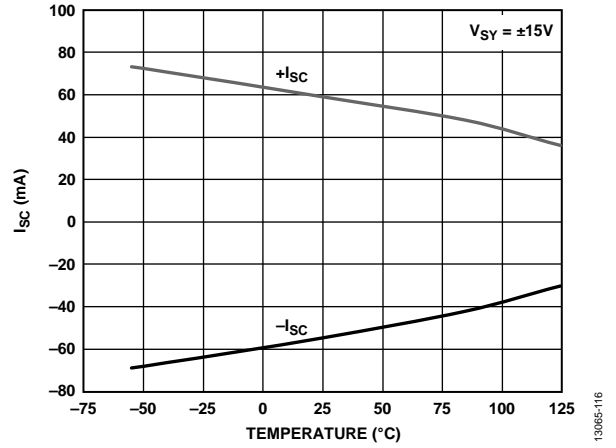


Figure 17. Output Short-Circuit Current (I_{SC}) vs. Temperature, $V_{SY} = \pm 15 V$

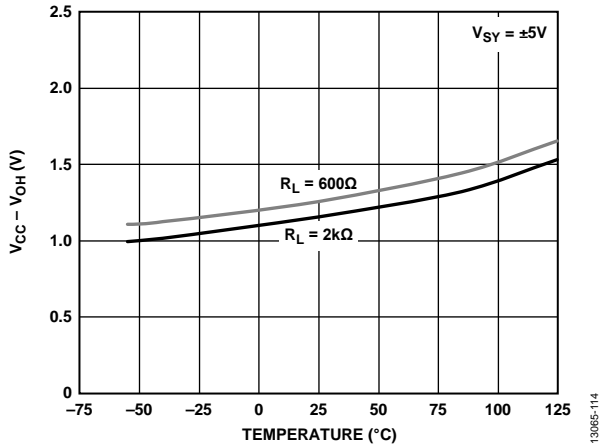


Figure 15. Output Saturation Voltage ($V_{CC} - V_{OH}$) vs. Temperature, $V_{SY} = \pm 5 V$

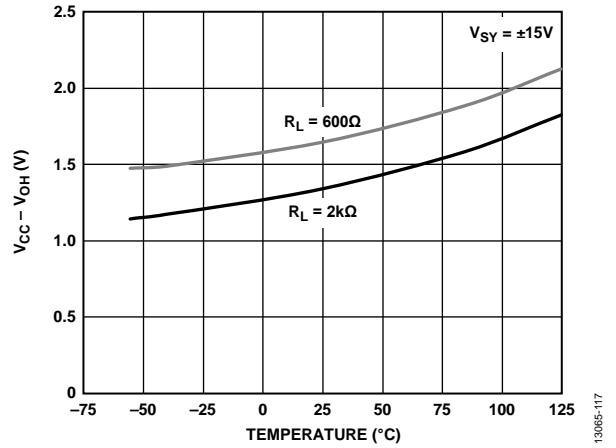


Figure 18. Output Saturation Voltage ($V_{CC} - V_{OH}$) vs. Temperature, $V_{SY} = \pm 15 V$

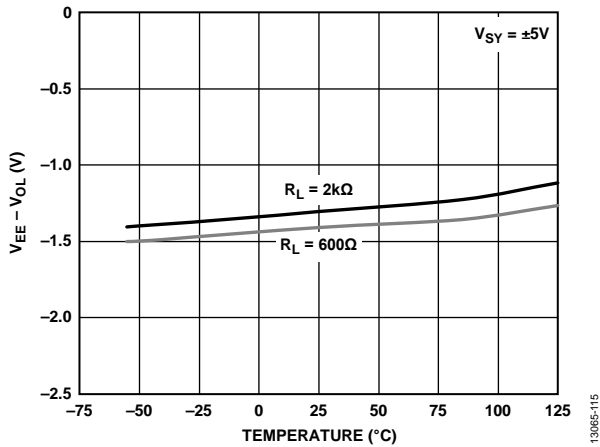


Figure 16. Output Saturation Voltage ($V_{EE} - V_{OL}$) vs. Temperature, $V_{SY} = \pm 5 V$

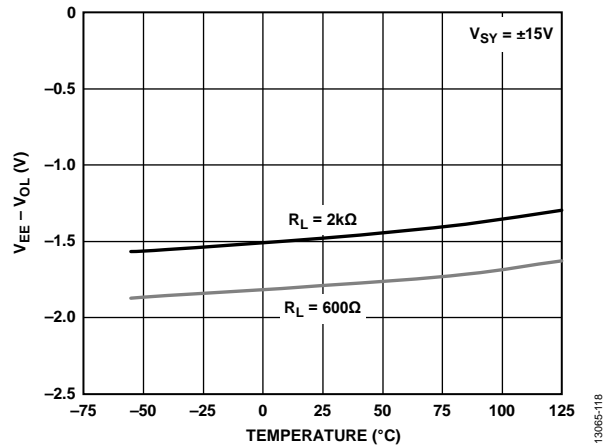
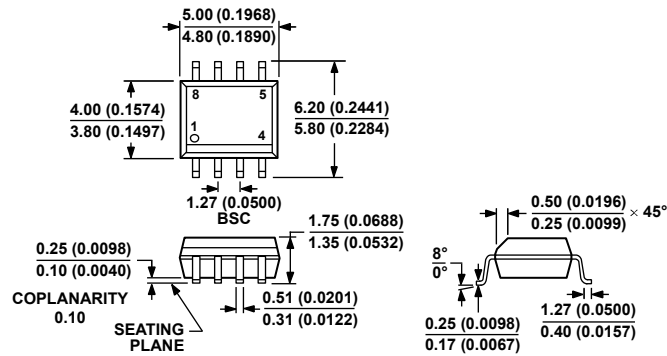


Figure 19. Output Saturation Voltage ($V_{EE} - V_{OL}$) vs. Temperature, $V_{SY} = \pm 15 V$

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 20. 8-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body
 (R-8)

Dimensions shown in millimeters and (inches)

012407-A

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|--|----------------|
| AD8599TRZ-EP | -55°C to +125°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 |
| AD8599TRZ-EP-R7 | -55°C to +125°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 |

¹ Z = RoHS Compliant Part.

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[LTC1050CN8#PBF](#) [LT1112ACN8#PBF](#) [LT1996AIDD#PBF](#) [LT1112CN8#PBF](#) [LTC6087CDD#PBF](#) [LT1078S8#PBF](#) [LT1079ACN#PBF](#)
[LTC6242HVCDHC#PBF](#)