16-Channel, 125 MHz Bandwidth, JESD204B Analog-to-Digital Converter

Data Sheet **AD9083**

FEATURES

1.0 V and 1.8 V supply operation
125 MHz usable analog input bandwidth
Sample rate up to 2 GSPS
Noise spectral density in 100 MHz bandwidth = −145 dBFS/Hz, 2.0 GSPS encode
SNR = 66 dBFS in 100 MHz bandwidth, 2.0 GSPS encode
SNR = 82 dBFS in 15.625 MHz bandwidth, 2.0 GSPS encode
SFDR = 60 dBc in 100 MHz bandwidth, 2.0 GSPS encode
SFDR = 80 dBc in 15.625 MHz bandwidth, 2.0 GSPS encode
90 mW total power per channel at 2.0 GSPS (default settings)
Flexible input range: 0.5 V p-p to 2 V p-p differential
90 dB channel crosstalk, 2.0 GSPS encode
Digital processor
- **CIC decimation filter**
- **Programmable DDC**
- **Data gating**

JESD204B Subclass 1 encoded outputs
- **Supports up to 16 Gbps/lane**
- **Flexible sample data processing**
- **Flexible JESD204B lane configurations**

Large signal dither
Serial port control

APPLICATIONS

Millimeter wave imaging
Electronic beam forming and phased arrays
Multichannel wideband receivers
Electronic support measures

PRODUCT HIGHLIGHTS

1. Continuous time, Σ-Δ analog-to-digital converters (ADCs) support signal bandwidths of up to 125 MHz with low power and minimal filtering.
2. Integrated digital processing blocks reduce data payload and lower overall system cost.
3. Configurable JESD204B interface reduces printed circuit board (PCB) complexity.
4. Flexible power-down options.
5. SPI interface controls various product features and functions to meet specific system requirements.
6. Small, 9 mm × 9 mm, 100-ball CSP_BGA package, simple interface, and integrated digital processing save PCB space.

FUNCTIONAL BLOCK DIAGRAM

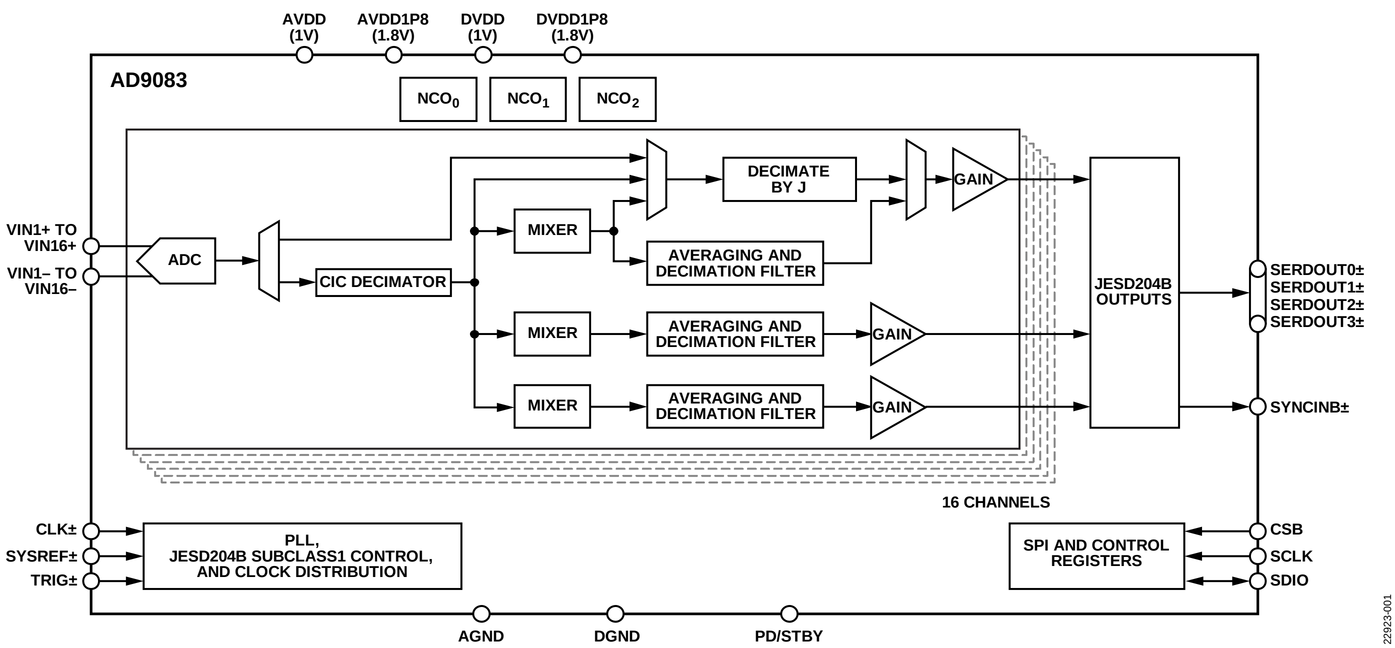

Figure 1.

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REVISION HISTORY

1/2021—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9083 is a 16-channel, 125 MHz bandwidth, continuous time Σ-Δ (CTSD) ADC. The device features an on-chip, programmable, single-pole antialiasing filter and termination resistor that is designed for low power, small size, and ease of use.

The 16 ADC cores features a first-order, CTSD modulator architecture with integrated, background nonlinearity correction logic and self cancelling dither. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The analog input and clock signals are differential inputs. Each ADC has a signal processing tile to filter out of band shaped noise from the Σ-Δ ADC and reduce the sample rate. Each tile contains a cascaded integrator comb (CIC) filter, a quadrature digital downconverter (DDC) with multiple finite input response (FIR) decimation filters (decimate by J block), or up to three quadrature DDC channels with averaging decimation filters for data gating applications.

Users can configure the Subclass 1 JESD204B based, high speed serialized output in a variety of lane configurations (up to four), depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multiple device synchronization is supported through the SYSREF±, TRIG±, and SYNCINB± input pins.

The AD9083 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 1.8 V capable 3-wire serial port interface (SPI).

The AD9083 is available in a Pb-free, 100-ball CSP_BGA and is specified over the −40°C to +85°C industrial temperature range. This product is protected by a U.S. patent.

SPECIFICATIONS

Table 1 shows the AD9083 wide bandwidth real output setups used to obtain the specifications. The AD9083 is a highly programmable device and supports many use cases. Refer to the Setting Up the AD9083 Digital Interface section and the Programming Guide section for more details.

Table 1.

f_{SAMPLE} (GSPS)	CIC Decimation	J Decimation	Output Data Rate (MSPS)	JESD204B Link Setup Parameters					
				Number of Lanes (L)	Number of Converters (M)	Number of Octets per Frame (F)	Number of Samples (S)	N'	K
2	1	8	250	4	16	6	1	12	32
1	1	4	250	4	16	6	1	12	32

DC SPECIFICATIONS

AVDD = 1.0 V, AVDD1P8 = 1.8 V, DVDD = 1.0 V, DVDD1P8 = 1.8 V, programmable maximum ADC input voltage range (V_{MAX}) = 1.8 V, analog input (A_{IN}) = −2.0 dBFS, −40°C ≤ T_J ≤ +115°C[1], mode details as shown in Table 1[2], backoff = 0[3], EN_HP = 0[4], unless otherwise noted. Typical specifications represent performance at T_J = 45°C (T_A = 25°C).

Table 2.

Parameter[5]	1.0 GSPS Min	1.0 GSPS Typ	1.0 GSPS Max	2.0 GSPS Min	2.0 GSPS Typ	2.0 GSPS Max	Unit
RESOLUTION	12		16	12		16	Bits
ACCURACY							
Offset Error		0.33		−0.86	+0.33	+1.55	%FS
Offset Matching		0.75			+0.75	+1.66	%FS
Gain Error		5.2		−10	+5.2	+20	%FS
Gain Matching		1.1			+1.1	+3.7	%FS
TEMPERATURE DRIFT							
Offset Stability Error		14.1			14.1		ppm/°C
Gain Stability Error		0.2			0.2		ppm/°C
Voltage Reference		0.1			0.1		ppm/°C
ANALOG INPUTS							
Differential Input Voltage Range	0.5	1.0	2.0	0.5	1.0	2.0	V p-p
Common-Mode Voltage (V_{CM})	0.5	0.7	1.0	0.5	0.7	1.0	V
Common-Mode Input Series Resistance (R_{IN}[6])		R_{IN}			R_{IN}		Ω
Differential Input Termination Resistance (R_{TERM})	100	200	2 × R_{IN}	100	200	2 × R_{IN}	Ω
Differential Input Capacitance		0.35			0.35		pF
Analog Full-Power Bandwidth		125			125		MHz
POWER SUPPLY							
AVDD	0.95	1.0	1.05	0.95	1.0	1.05	V
AVDD1P8	1.7	1.8	1.9	1.7	1.8	1.9	V
DVDD	0.95	1.0	1.05	0.95	1.0	1.05	V
DVDD1P8	1.7	1.8	1.9	1.7	1.8	1.9	V
AVDD Current (I_{AVDD})		208			397	471	mA
AVDD1P8 Current ($I_{AVDD1P8}$)		65			95	102	mA
DVDD Current (I_{DVDD})		592			797	971	mA
DVDD1P8 ($I_{DVDD1P8}$)		40			41	48	mA

Parameter[5]	Min	1.0 GSPS Typ	Max	Min	2.0 GSPS Typ	Max	Unit
POWER CONSUMPTION							
Total Power Dissipation (Including Output Drivers)[7]		1.0			1.4		W
Power-Down Dissipation		56			86		mW
Standby[8]		676			802		mW
Power per Channel		63			90		mW

[1] The-T_J range of −40°C to +115°C translates to an T_A range of −40°C to +85°C.
[2] 16-channel, 125 MSPS real output mode.
[3] Backoff is the reduction in front-end gain for increased linearity.
[4] EN_HP increases the SNR by 2.5 dB at an increased power dissipation.
[5] See the AN-835 for definitions and for details on how these tests were completed.
[6] R_{IN} = 8 kΩ/Kvti, where Kvti is proportional to the ADC front-end gain factor, R_{IN} = 1000 Ω for f_S = 1 GSPS, and R_{IN} = 381 for f_S = 2 GSPS.
[7] See Table 1 for setup details. Note that power consumption varies as a function of sample rate, the decimation options selected, and the JESD204B setup.
[8] Can be controlled by SPI, ADC in low power mode.

AC SPECIFICATIONS

AVDD = 1.0 V, AVDD1P8 = 1.8 V, DVDD = 1.0 V, DVDD1P8 = 1.8 V, V_{MAX} = 1.8 V, −40°C ≤ T_J ≤ +115°C T_J range of −40°C to +115°C translates to a T_A range of −65°C to +85°C. The mode details are as shown in Table 1 (16-channel, 125 MSPS, real output mode), unless otherwise noted. Typical specifications represent performance at T_J = 45°C (T_A = 25°C).

Table 3.

Parameter[1]	Test Conditions/Comments	1.0 GSPS Min	Typ	Max	2.0 GSPS Min	Typ	Max	Unit
NOISE SPECTRAL DENSITY (NSD)								
Flicker Noise Corner			1			1		MHz
NSD at 22 MHz	Backoff = 0, EN_HP = 0		−141			−146	−144	dBFS/Hz
A_{IN} = −3.0 dBFS, frequency (f) = 22 MHz	Backoff = 3, EN_HP = 0		−138			−145		dBFS/Hz
	Backoff = 6, EN_HP = 0		−136			−142		dBFS/Hz
	Backoff = 0, EN_HP = 1		−144			−149	−146	dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)								
SNR at 22 MHz	Backoff = 0, EN_HP = 0		60		62	65		dBFS
A_{IN} = −3.0 dBFS, f = 22 MHz	Backoff = 3, EN_HP = 0		57			64		dBFS
	Backoff = 6, EN_HP = 0		55			61		dBFS
	Backoff = 0, EN_HP = 1		63		65	67		dBFS
SPURIOUS-FREE DYNAMIC RANGE (SFDR)/ THIRD-ORDER HARMONIC DISTORTION (HD3)								
HD3 at 22 MHz	Backoff = 0, EN_HP = 0		−68			−69	−64	dBc
A_{IN} = −3.0 dBFS, f = 22 MHz	Backoff = 3, EN_HP = 0		−76			−71		dBc
	Backoff = 6, EN_HP = 0		−74			−75		dBc
	Backoff = 0, EN_HP = 1		−66			−69	−63	dBc
THIRD-ORDER INTERMODULATION DISTORTION (IMD3)								
SFDR/HD3 at 22 MHz	Backoff = 0, EN_HP = 0		−83			−85		dBFS
A_{IN} = −9.0 dBFS, f = 22 MHz	Backoff = 3, EN_HP = 0		−86			−86		dBFS
	Backoff = 6, EN_HP = 0		−93			−86		dBFS
	Backoff = 0, EN_HP = 1		−87			−85		dBFS
Delete blank line								
In-Band Gain Flatness[2]	25°C		0.3			0.5		dB
CROSSTALK[3]	25°C		90			90		dB
ANALOG INPUT BANDWIDTH, FULL POWER[4]	25°C		62.5			125		MHz

[1] See AN-835 for definitions and for details on how these tests were completed.
[2] The gain flatness may vary depending on the digital filter selection in the datapath.
[3] Crosstalk is measured at 30.3 MHz with a −2.0 dBFS analog input on one channel, and no input on the adjacent channel.
[4] Full power bandwidth of f_S/16 is achieved only when CIC decimation = 4 is used.

AC Specifications for Different Variable Settings

See the AN-835 for definitions and for details on how the tests shown in this section were completed. f_S is the sample clock of the converter core. Backoff is the reduction in front-end gain for increased linearity. EN_HP increases the SNR by 2.5 dB at an increased power dissipation.

Table 4. Variable Settings: f_S = 2.0 GSPS, Backoff = 0, and EN_HP = 0

Parameters	Test Conditions/Comments	Min	Typ	Max	Unit
NSD					
Flicker Noise Corner			1		MHz
At 15.625 MHz (f_S/128)	A_{IN} = −2.0 dBFS		−155		dBFS/Hz
At 31.25 MHz (f_S/64)	A_{IN} = −2.0 dBFS		−153		dBFS/Hz
At 100 MHz (f_S/20)	A_{IN} = −2.0 dBFS		−145		dBFS/Hz
SNR	A_{IN} = −2.0 dBFS				
7.8 MHz to 23.4 MHz (15.625 MHz Bandwidth)			82		dBFS
23.4 MHz to 39 MHz (15.625 MHz Bandwidth)			80		dBFS
92.2 MHz to 107.8 MHz (15.625 MHz Bandwidth)			71		dBFS
DC to 15.625 MHz			82		dBFS
DC to 31.25 MHz			76		dBFS
DC to 100 MHz			66		dBFS
SFDR/HD3	A_{IN} = −2.0 dBFS				
At f_S/128			−80		dBc
At f_S/64			−75		dBc
At f_S/20			−60		dBc
IMD3	A_{IN} = −8.0 dBFS				
At f_S/128			−80		dBc
At f_S/64			−75		dBc
At f_S/20			−60		dBc

Table 5. Variable Settings: f_S = 2.0 GSPS, Backoff = 3, and EN_HP = 0

Parameters	Test Conditions/Comments	Min	Typ	Max	Unit
NSD					
Flicker Noise Corner			1		MHz
At 15.625 MHz (f_S/128)	A_{IN} = −2.0 dBFS		−153		dBFS/Hz
At 31.25 MHz (f_S/64)	A_{IN} = −2.0 dBFS		−151		dBFS/Hz
At 100 MHz (f_S/20)	A_{IN} = −2.0 dBFS		−143		dBFS/Hz
SNR	A_{IN} = −2.0 dBFS				
7.8 MHz to 23.4 MHz (15.625 MHz Bandwidth)			80		dBFS
23.4 MHz to 39 MHz (15.625 MHz Bandwidth)			74		dBFS
92.2 MHz to 107.8 MHz (15.625 MHz Bandwidth)			64		dBFS
DC to 15.625 MHz			80		dBFS
DC to 31.25 MHz			74		dBFS
DC to 100 MHz			64		dBFS
SFDR/HD3	A_{IN} = −2.0 dBFS				
At f_S/128			−81		dBc
At f_S/64			−78		dBc
At f_S/20			−63		dBc
IMD3	A_{IN} = −8.0 dBFS				
At f_S/128			−81		dBc
At f_S/64			−77		dBc
At f_S/20			−63		dBc

Table 6. Variable Settings: f_S = 2.0 GSPS, Backoff = 6, and EN_HP = 0

Parameters	Test Conditions/Comments	Min	Typ	Max	Unit
NSD					
Flicker Noise Corner			1		MHz
At 15.625 MHz (f_S/128)	A_{IN} = −2.0 dBFS		−150		dBFS/Hz
At 31.25 MHz (f_S/64)	A_{IN} = −2.0 dBFS		−148		dBFS/Hz
At 100 MHz (f_S/20)	A_{IN} = −2.0 dBFS		−140		dBFS/Hz
SNR	A_{IN} = −2.0 dBFS				
7.8 MHz to 23.4 MHz (15.625 MHz Bandwidth)			77		dBFS
23.4 MHz to 39 MHz (15.625 MHz Bandwidth)			71		dBFS
92.2 MHz to 107.8 MHz (15.625 MHz Bandwidth)			61		dBFS
DC to 15.625 MHz			77		dBFS
DC to 31.25 MHz			71		dBFS
DC to 100 MHz			61		dBFS
SFDR/HD3	A_{IN} = −2.0 dBFS				
At f_S/128			−82		dBc
At f_S/64			−81		dBc
At f_S/20			−66		dBc
IMD3	A_{IN} = −8.0 dBFS				
At f_S/128			−82		dBc
At f_S/64			−80		dBc
At f_S/20			−66		dBc

Table 7. Variable Settings: f_S = 2.0 GSPS, Backoff = 0, and EN_HP = 1

Parameters	Test Conditions/Comments	Min	Typ	Max	Unit
NSD					
Flicker Noise Corner			1		MHz
At 15.625 MHz (f_S/128)	A_{IN} = −2.0 dBFS		−157		dBFS/Hz
At 31.25 MHz (f_S/64)	A_{IN} = −2.0 dBFS		−155		dBFS/Hz
At 100 MHz (f_S/20)	A_{IN} = −2.0 dBFS		−147		dBFS/Hz
SNR	A_{IN} = −2.0 dBFS				
7.8 MHz to 23.4 MHz (15.625 MHz Bandwidth)			85		dBFS
23.4 MHz to 39 MHz (15.625 MHz Bandwidth)			79		dBFS
92.2 MHz to 107.8 MHz (15.625 MHz Bandwidth)			69		dBFS
DC to 15.625 MHz			85		dBFS
DC to 31.25 MHz			79		dBFS
DC to 100 MHz			69		dBFS
SFDR/HD3	A_{IN} = −2.0 dBFS				
At f_S/128			−80		dBc
At f_S/64			−75		dBc
At f_S/20			−60		dBc
IMD3	A_{IN} = −8.0 dBFS				
At f_S/128			−80		dBc
At f_S/64			−75		dBc
At f_S/20			−60		dBc

Table 8. Variable Settings: f_S = 1.0 GSPS, Backoff = 0, and EN_HP = 0

Parameters	Test Conditions/Comments	Min	Typ	Max	Unit
NSD					
Flicker Noise Corner			1		MHz
At 7.8125 MHz (f_S/128)	A_{IN} = −2.0 dBFS		−152		dBFS/Hz
At 15.625 MHz (f_S/64)	A_{IN} = −2.0 dBFS		−151		dBFS/Hz
At 50 MHz (f_S/20)	A_{IN} = −2.0 dBFS		−144		dBFS/Hz
SNR	A_{IN} = −2.0 dBFS				
3.9 MHz to 11.7 MHz (7.8125 MHz Bandwidth)			82		dBFS
11.7 MHz to 19.5 MHz (7.8125 MHz Bandwidth)			80		dBFS
46.1 MHz to 53.9 MHz (7.8125 MHz Bandwidth)			71		dBFS
DC to 7.8125 MHz			82		dBFS
DC to 15.625 MHz			76		dBFS
DC to 50 MHz			66		dBFS
SFDR/HD3					
At f_S/128	A_{IN} = −2.0 dBFS		−80		dBc
HD3 at f_S/64	A_{IN} = −2.0 dBFS		−75		dBc
HD3 at f_S/20	A_{IN} = −2.0 dBFS		−60		dBc
SFDR/IMD3					
At f_S/128	A_{IN} = −8.0 dBFS		−80		dBc
At f_S/64	A_{IN} = −8.0 dBFS		−75		dBc
At f_S/20	A_{IN} = −8.0 dBFS		−60		dBc

Table 9. Variable Settings: f_S = 1.0 GSPS, Backoff = 3, and EN_HP = 0

Parameters	Test Conditions/Comments	Min	Typ	Max	Unit
NSD					
Flicker Noise Corner			1		MHz
At 7.8125 MHz (f_S/128)	A_{IN} = −2.0 dBFS		−150		dBFS/Hz
At 15.625 MHz (f_S/64)	A_{IN} = −2.0 dBFS		−149		dBFS/Hz
At 50 MHz (f_S/20)	A_{IN} = −2.0 dBFS		−142		dBFS/Hz
SNR	A_{IN} = −2.0 dBFS				
3.9 MHz to 11.7 MHz (7.8125 MHz Bandwidth)			80		dBFS
11.7 MHz to 19.5 MHz (7.8125 MHz Bandwidth)			74		dBFS
46.1 MHz to 53.9 MHz (7.8125 MHz Bandwidth)			64		dBFS
DC to 7.8125 MHz			80		dBFS
DC to 15.625 MHz			74		dBFS
DC to 50 MHz			64		dBFS
SFDR/HD3					
At f_S/128	A_{IN} = −2.0 dBFS		−81		dBc
HD3 at f_S/64	A_{IN} = −2.0 dBFS		−78		dBc
HD3 at f_S/20	A_{IN} = −2.0 dBFS		−63		dBc
SFDR/IMD3					
At f_S/128	A_{IN} = −8.0 dBFS		−81		dBc
At f_S/64	A_{IN} = −8.0 dBFS		−77		dBc
At f_S/20	A_{IN} = −8.0 dBFS		−63		dBc

Table 10. Variable Settings: f_S = 1.0 GSPS, Backoff = 6, and EN_HP = 0

Parameters	Test Conditions/Comments	Min	Typ	Max	Unit
NSD					
Flicker Noise Corner			1		MHz
At 7.8125 MHz (f_S/128)	A_{IN} = −2.0 dBFS		−147		dBFS/Hz
At 15.625 MHz (f_S/64)	A_{IN} = −2.0 dBFS		−146		dBFS/Hz
At 50 MHz (f_S/20)	A_{IN} = −2.0 dBFS		−139		dBFS/Hz
SNR	A_{IN} = −2.0 dBFS				
3.9 MHz to 11.7 MHz (7.8125 MHz Bandwidth)			77		dBFS
11.7 MHz to 19.5 MHz (7.8125 MHz Bandwidth)			71		dBFS
46.1 MHz to 53.9 MHz (7.8125 MHz Bandwidth)			61		dBFS
DC to 7.8125 MHz			77		dBFS
DC to 15.625 MHz			71		dBFS
DC to 50 MHz			61		dBFS
SFDR/HD3					
At f_S/128	A_{IN} = −2.0 dBFS		−82		dBc
HD3 at f_S/64	A_{IN} = −2.0 dBFS		−81		dBc
HD3 at f_S/20	A_{IN} = −2.0 dBFS		−66		dBc
SFDR/IMD3					
At f_S/128	A_{IN} = −8.0 dBFS		−82		dBc
At f_S/64	A_{IN} = −8.0 dBFS		−80		dBc
At f_S/20	A_{IN} = −8.0 dBFS		−66		dBc

Table 11. Variable Settings: f_S = 1.0 GSPS, Backoff = 0, and EN_HP = 1

Parameters	Test Conditions/Comments	Min	Typ	Max	Unit
NSD					
Flicker Noise Corner			1		MHz
At 7.8125 MHz (f_S/128)	A_{IN} = −2.0 dBFS		−154		dBFS/Hz
At 15.625 MHz (f_S/64)	A_{IN} = −2.0 dBFS		−153		dBFS/Hz
At 50 MHz (f_S/20)	A_{IN} = −2.0 dBFS		−146		dBFS/Hz
SNR	A_{IN} = −2.0 dBFS				
3.9 MHz to 11.7 MHz (7.8125 MHz Bandwidth)			85		dBFS
11.7 MHz to 19.5 MHz (7.8125 MHz Bandwidth)			79		dBFS
46.1 MHz to 53.9 MHz (7.8125 MHz Bandwidth)			69		dBFS
DC to 7.8125 MHz			85		dBFS
DC to 15.625 MHz			70		dBFS
DC to 50 MHz			69		dBFS
SFDR/HD3					
At f_S/128	A_{IN} = −2.0 dBFS		−80		dBc
HD3 at f_S/64	A_{IN} = −2.0 dBFS		−75		dBc
HD3 at f_S/20	A_{IN} = −2.0 dBFS		−60		dBc
SFDR/IMD3					
At f_S/128	A_{IN} = −8.0 dBFS		−80		dBc
At f_S/64	A_{IN} = −8.0 dBFS		−75		dBc
At f_S/20	A_{IN} = −8.0 dBFS		−60		dBc

DIGITAL SPECIFICATIONS

AVDD = 1.0 V, AVDD1P8= 1.8 V, DVDD = 1.0 V, DVDD1P8 = 1.8 V, V_{MAX} = 1.8 V[1], A_{IN} = −2.0 dBFS, −40°C ≤ T_J ≤ +115°C[2], mode details as shown in Table 1[3], unless otherwise noted. Typical specifications represent performance at T_J = 45°C (T_A = 25°C).

Table 12.

Parameter	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)				
Differential Input Voltage	300	800	1800	mV p-p
Input Common-Mode Voltage		0.5		V
Input Resistance (Differential)		100		Ω
Input Capacitance		1		pF
SYSREF and TRIG INPUTS (SYSREF+, SYSREF−, TRIG+, AND TRIG−)				
Logic Compliance		LVDS		
Differential Input Voltage		700	1100	mV p-p
Input Common-Mode Voltage		0.5		V
Input Resistance (Differential)		100		Ω
Input Capacitance (Differential)		1		pF
LOGIC INPUT (SDIO, SCLK, CSB, PD/STBY, AND RSTB)				
Logic Compliance		CMOS		
Logic 1 Voltage	0.7 × DVDD1P8			V
Logic 0 Voltage			0.3 × DVDD1P8	V
Input Resistance		High impedance		
LOGIC OUTPUT (SDIO)				
Logic Compliance		CMOS		
Logic 1 Voltage (High Output Current (I_{OH}) = 800 μA)	DVDD1P8 − 0.45			V
Logic 0 Voltage (Low Output Current (I_{OL}) = 50 μA)			0.45	V
SYNCINB INPUT (SYNCINB+/SYNCINB−)				
Logic Compliance		LVDS		
Differential Input Voltage		700	1900	mV p-p
Input Common-Mode Voltage		0.45		V
Input Resistance (Differential)		100		kΩ
Input Capacitance		1		pF
SYNCINB+ INPUT				
Logic Compliance		CMOS		
Logic 1 Voltage	0.7 × DVDD1P8			V
Logic 0 Voltage			0.3 × DVDD1P8	V
Input Resistance		High impedance		
DIGITAL OUTPUTS (SERDOUTx±, x = 0 TO 3)				
Standards Compliance		JESD204B		
Differential Output Voltage		675		mV p-p
Differential Termination Impedance	80	108	120	Ω

[1] V_{MAX} is the programmable maximum ADC input voltage range.
[2] The T_J range of −40°C to +115°C translates to an T_A range of −65°C to +85°C.
[3] 16-channel 125 MSPS real output mode.

SWITCHING SPECIFICATIONS

AVDD = 1.0 V, AVDD1P8 = 1.8 V, DVDD = 1.0 V, DVDD1P8 = 1.8 V, V_{MAX} = 1.8 V[1], −40°C ≤ T_J ≤ +115°C[2], mode details as shown in Table 1[3], unless otherwise noted. Typical specifications represent performance at T_J = 45°C (T_A = 25°C).

Table 13.

Parameter	Min	Typ	Max	Unit
CLOCK				
Clock Rate (at CLK+/CLK− Pins)[4]	50	250	500	MHz
ADC Sample Rate[5]	1		2	GSPS
Clock Pulse Width	1		10	ns
OUTPUT PARAMETERS				
Unit Interval (UI)[6]	62.5		4000	ps
Rise Time (t_R) (20% to 80% into 100 Ω Load)		30		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)		30		ps
Phase-Locked Loop (PLL) Lock Time[7]		5		ms
Data Rate per Channel (NRZ)[8]	0.25		16	Gbps

[1] V_{MAX} is the programmable maximum ADC input voltage range.
[2] The T_J range of −40°C to +115°C translates to an T_A range of −65°C to +85°C.
[3] 16-channel 125 MSPS real output mode.
[4] Input clock to the on-chip PLL (Pin K3 and Pin J3).
[5] ADC sample clock of the converter core.
[6] Baud rate = 1/UI. A subset of this range can be supported.
[7] Lock times may vary depending on the JESD204B link setup.
[8] Default L = 4. This number can be changed based on the sample rate and decimation ratio.

TIMING SPECIFICATIONS

Table 14.

Parameter	Description	Min	Typ	Max	Unit
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	4			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	4			ns
t_{CLK}	Period of the SCLK	10			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK must be in a logic high state	4			ns
t_{LOW}	Minimum period that SCLK must be in a logic low state	4			ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		2	4	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	6			ns

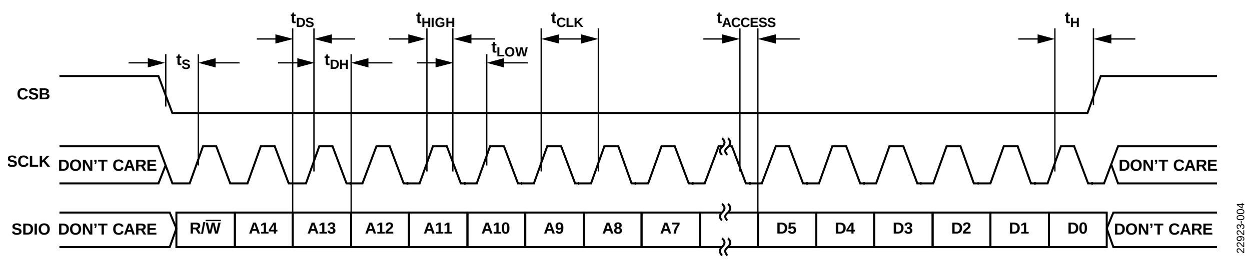

Figure 2. Serial Port Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 15.

Parameter	Rating
Electrical	
AVDD to AGND	1.05 V
AVDD1P8 to AGND	2.0 V
DVDD to DGND	1.05 V
DVDD1P8 to DGND	2.0 V
AGND to DGND	−0.3 V to +0.3 V
VINx± to AGND	AGND − 0.3 V to AVDD1P8 + 0.3 V
CLK± to AGND	AGND − 0.3 V to AVDD + 0.3 V
SCLK, SDIO, CSB, RSTB, PD/STBY to DGND	DGND − 0.3 V to DVDD1P8 + 0.3 V
SYSREF±, TRIG± to AGND	AGND − 0.3 V to AVDD + 0.3 V
SYNCINB± to DGND	DGND − 0.3 V to DVDD1P8 + 0.3 V
Temperature	
Junction Range	−40°C to +125°C
Storage Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 16. Thermal Resistance

Package Type	θ_{JA}	θ_{JC_TOP}	θ_{JB}	Ψ_{JB}	Ψ_{JT}	Unit
BC-100-8[1]	23.4	10.3	8.9	9.0	1.2	°C/W

[1] Test Condition 1: Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with 190 thermal vias. See JEDEC JESD-51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

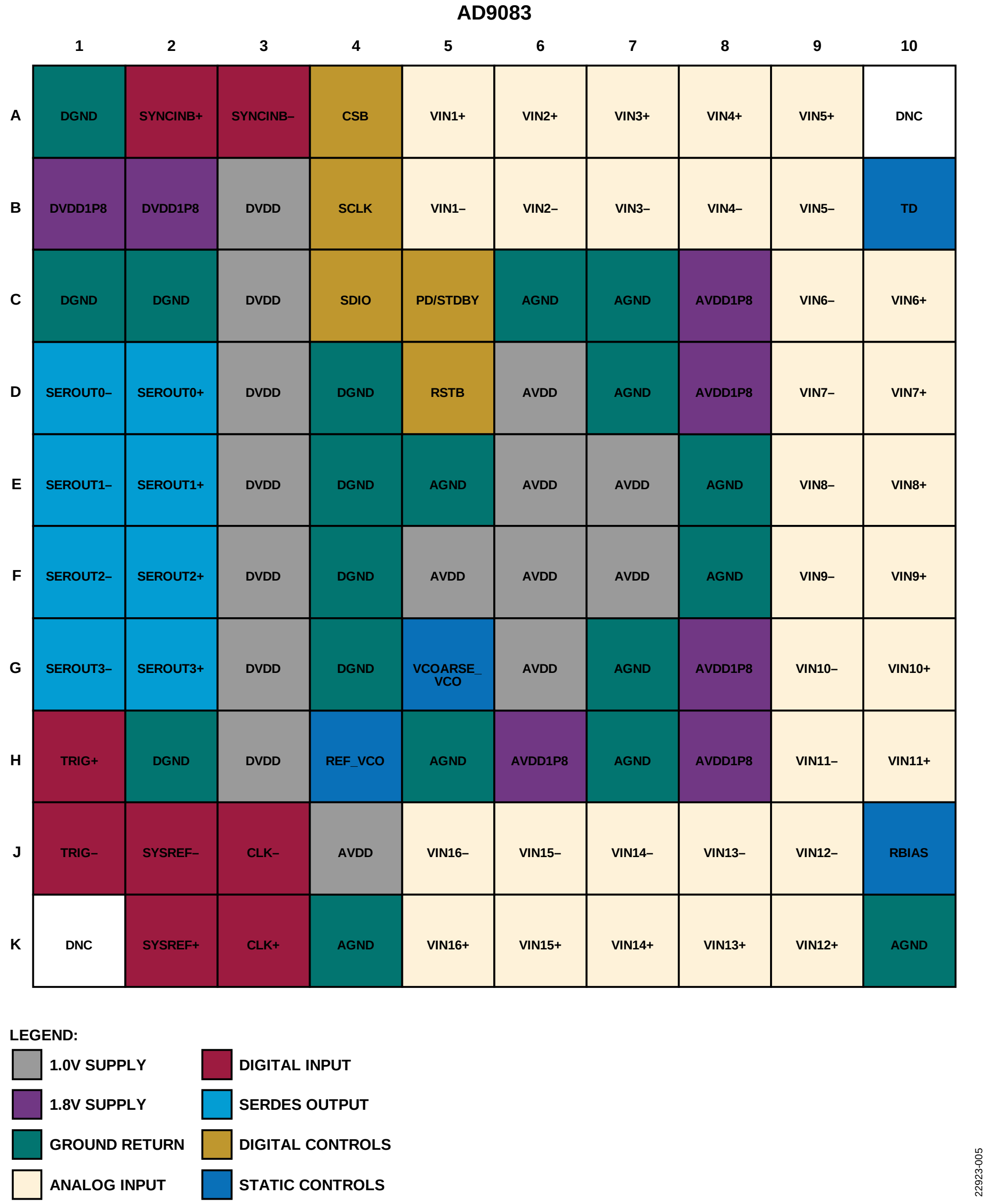

Figure 3. Pin Configuration

Table 17. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
Power Supplies			
D6, E6, E7, F6, F7, G6	AVDD	Power	Analog Power Supply (1.0 V Nominal).
F5	AVDD	Power	Analog Power Supply for Clock (1.0 V Nominal).
J4	AVDD	Power	Analog Power Supply for Internal PLL (1.0 V Nominal).
C8, D8, G8, H6, H8	AVDD1P8	Power	Analog Power Supply (1.8 V Nominal).
D3, E3, F3, G3	DVDD	Power	Digital Power Supply (1.0 V Nominal).
B3, C3, H3	DVDD	Power	Digital Driver Power Supply (1.0 V Nominal).
B1	DVDD1P8	Power	Digital Driver Power Supply (1.8 V Nominal).
B2	DVDD1P8	Power	Digital Power Supply for I/O and SPI (1.8 V Nominal).

Pin No.	Mnemonic	Type	Description
C6, C7, D7, E8, F8, G7, H5, H7, K10	AGND	Ground	Analog Ground. These AGND pins connect to the analog ground plane.
E5	AGND	Ground	Ground Reference for AVDD.
K4	AGND	Ground	Ground Reference for AVDD.
D4, E4, F4, G4	DGND	Ground	Digital Ground. These DGND pins connect to the digital ground plane.
A1, C1, C2, H2	DGND	Ground	Digital Driver Ground. These DGND pins connect to the digital driver ground plane.
Analog			
A5, B5	VIN1+, VIN1−	Input	ADC 1 Analog Input True/Complement.
A6, B6	VIN2+, VIN2−	Input	ADC 2 Analog Input True/Complement.
A7, B7	VIN3+, VIN3−	Input	ADC 3 Analog Input True/Complement.
A8, B8	VIN4+, VIN4−	Input	ADC 4 Analog Input True/Complement.
A9, B9	VIN5+, VIN5−	Input	ADC 5 Analog Input True/Complement.
C9, C10	VIN6−, VIN6+	Input	ADC 6 Analog Input Complement/True.
D9, D10	VIN7−, VIN7+	Input	ADC 7 Analog Input Complement/True.
E9, E10	VIN8−, VIN8+	Input	ADC 8 Analog Input Complement/True.
F9, F10	VIN9−, VIN9+	Input	ADC 9 Analog Input Complement/True.
G9, G10	VIN10−, VIN10+	Input	ADC 10 Analog Input Complement/True.
H9, H10	VIN11−, VIN11+	Input	ADC 11 Analog Input Complement/True.
J9, K9	VIN12−, VIN12+	Input	ADC 12 Analog Input Complement/True.
J8, K8	VIN13−, VIN13+	Input	ADC 13 Analog Input Complement/True.
J7, K7	VIN14−, VIN14+	Input	ADC 14 Analog Input Complement/True.
J6, K6	VIN15−, VIN15+	Input	ADC 15 Analog Input Complement/True.
J5, K5	VIN16−, VIN16+	Input	ADC 16 Analog Input Complement/True.
J3, K3	CLK−, CLK+	Input	Clock Input Complement/True.
Digital Inputs			
J2, K2	SYSREF−, SYSREF+	Input	Active High JESD204B LVDS/CML System Reference Input Complement/True.
A2, A3	SYNCINB+, SYNCINB-	Input	Active Low JESD204B LVDS Sync Input True/Complement.
H1, J1	TRIG+, TRIG−	Input	Trigger Input LVDS. These TRIG± pins can be left floating if disabled.
Data Outputs			
D1, D2	SERDOUT0−, SERDOUT0+	Output	Lane 0 Output Data Complement/True.
E1, E2	SERDOUT1−, SERDOUT1+	Output	Lane 1 Output Data Complement/True.
F1, F2	SERDOUT2−, SERDOUT2+	Output	Lane 2 Output Data Complement/True.
G1, G2	SERDOUT3−, SERDOUT3+	Output	Lane 3 Output Data Complement/True.
Digital Controls			
C5	PD/STBY	Input	Power-Down Input (Active High). The operation of the PD/STBY pin depends on the SPI mode and can be configured as power-down or standby.
D5	RSTB	Input	Active Low Input for Device Reset.
A4	CSB	Input	SPI Chip Select (Active Low).
B4	SCLK	Input	SPI Serial Clock.
C4	SDIO	Input/output	SPI Serial Data Input/Output.

Pin No.	Mnemonic	Type	Description
Static Control			
B10	TD		Temperature Diode Pin.
J10	RBIAS		Current Reference Resistor, 5 kΩ to AGND.
H4	REG_VCO		Clock Multiplier PLL Voltage Regulator Bypass Capacitor. Low effective series resistance (ESR), low effective series inductance (ESL), 2.2 μF capacitor to AGND. Inductance between package and capacitor < 1 nH.
G5	VCOARSE_VCO		Clock Multiplier PLL Coarse Tuning Loop Filter, 33 nF Capacitor to AGND.
A10, K1	DNC		Do Not Connect. Leave the DNC pins floating.

TYPICAL PERFORMANCE CHARACTERISTICS

Nominal supply voltages, A_{IN} = −2.0 dBFS, T_J = 45°C, and 128k FFT, unless otherwise noted.

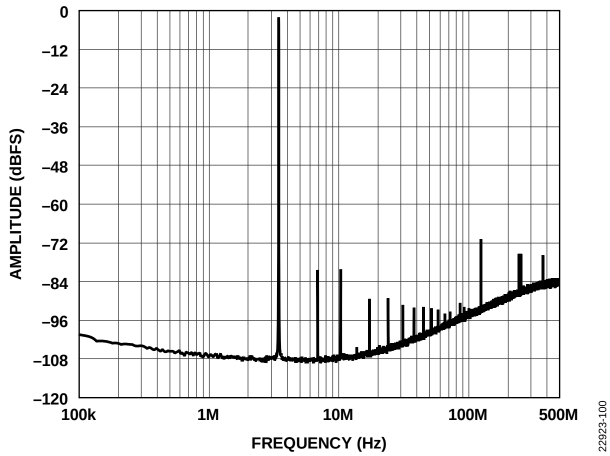

Figure 4. ADC Noise Floor at Backoff = 3 dB, 1 GSPS

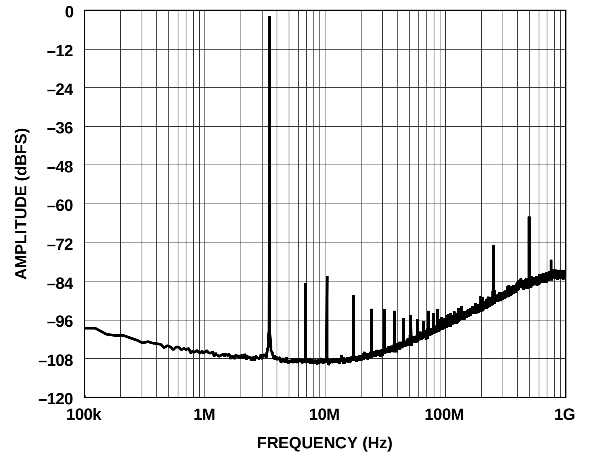

Figure 7. ADC Noise Floor at Backoff = 3 dB, 2 GSPS

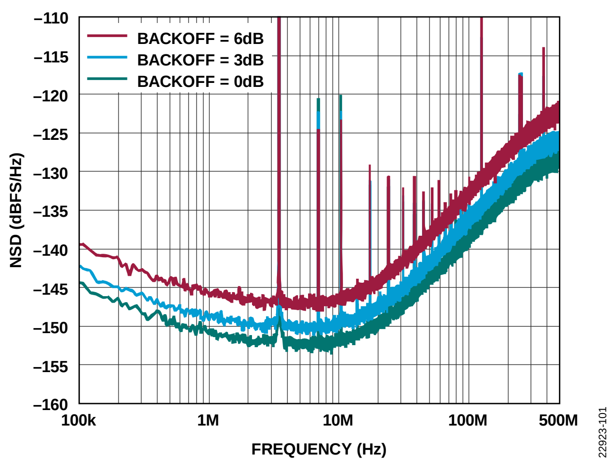

Figure 5. ADC NSD at Various Backoff Values, 1 GSPS

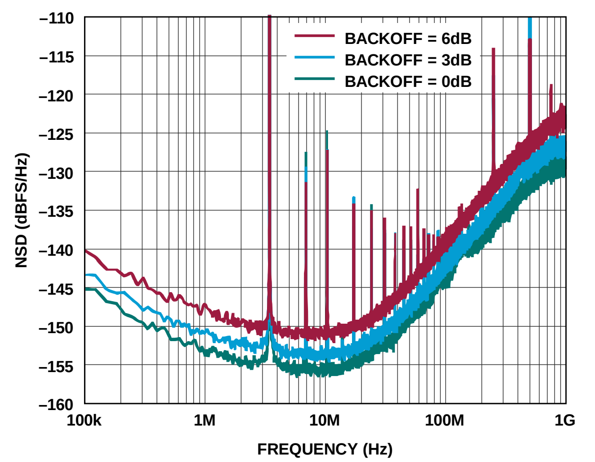

Figure 8. ADC NSD at Various Backoff Values, 2 GSPS

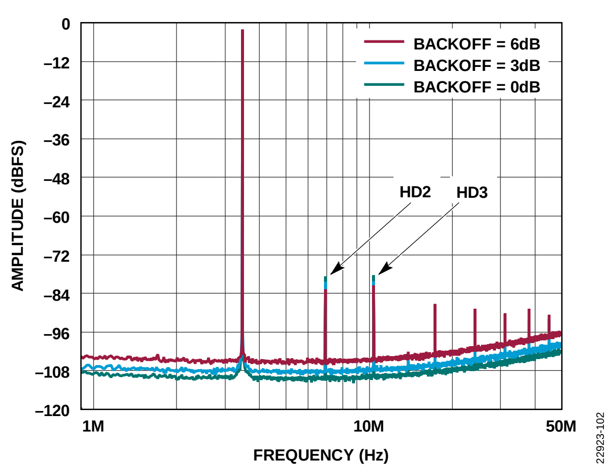

Figure 6. Harmonic Distortion 2 (HD2) and Harmonic Distortion 3 (HD3) at Various Backoff Values, 1 GSPS

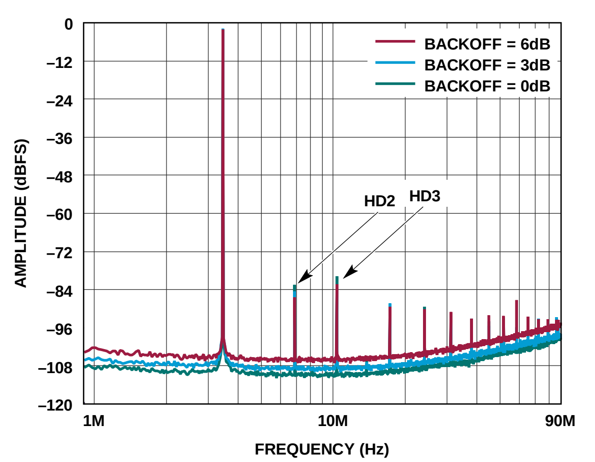

Figure 9. HD2 and HD3 at Various Backoff Values, 2 GSPS

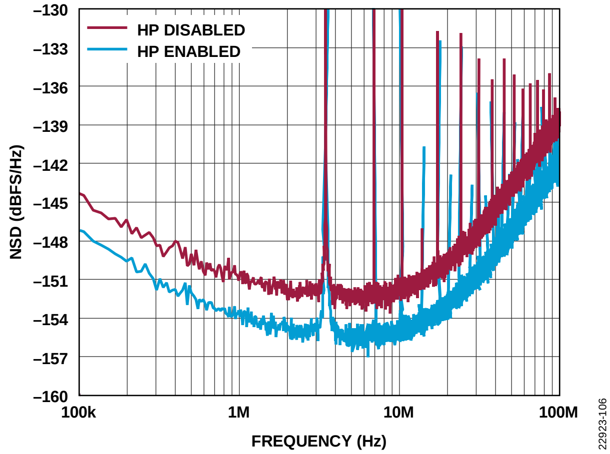

Figure 10. ADC NSD with and Without EN_HP, 1 GSPS

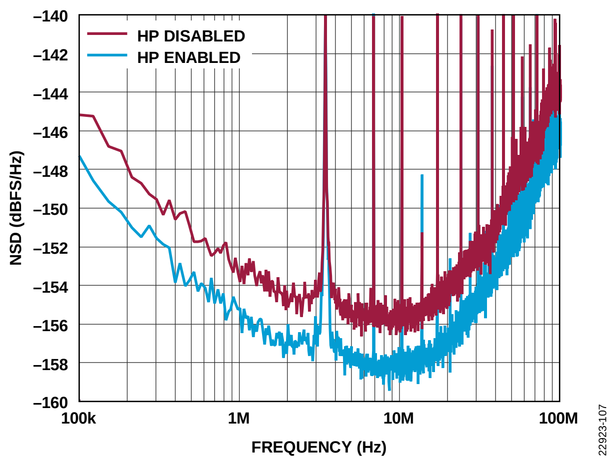

Figure 11. ADC NSD with and Without EN_HP, 2 GSPS

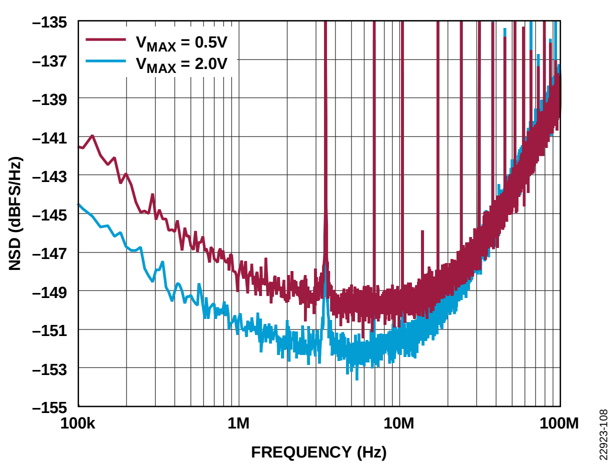

Figure 12. ADC NSD at Minimum and Maximum V_{MAX} Values, 1 GSPS

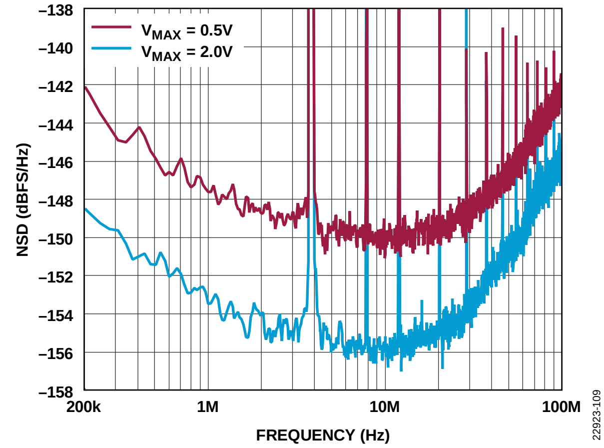

Figure 13. ADC NSD at Minimum and Maximum V_{MAX} Values, 2 GSPS

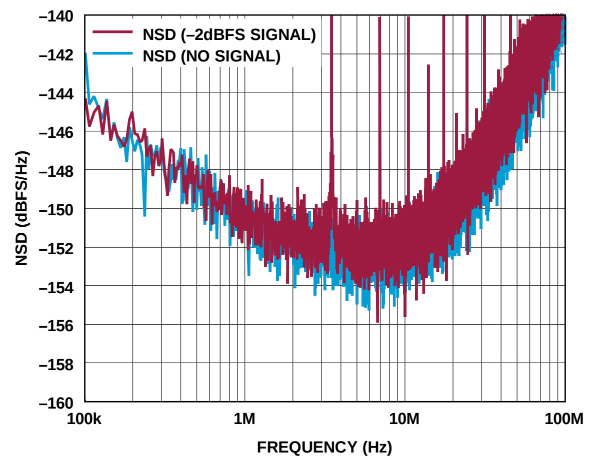

Figure 14. ADC NSD with and Without Full-Scale Input Signal, 1 GSPS

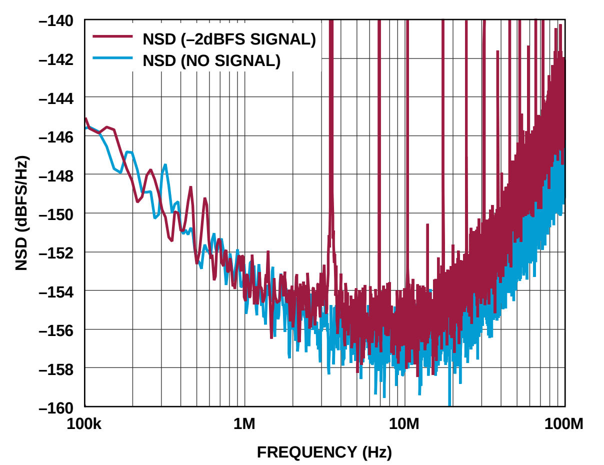

Figure 15. ADC NSD with and Without Full-Scale Input Signal, 2 GSPS

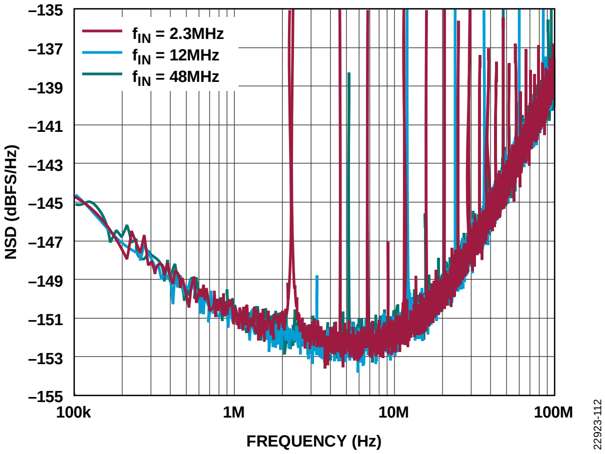

Figure 16. ADC NSD at Different Input Frequencies, 1 GSPS

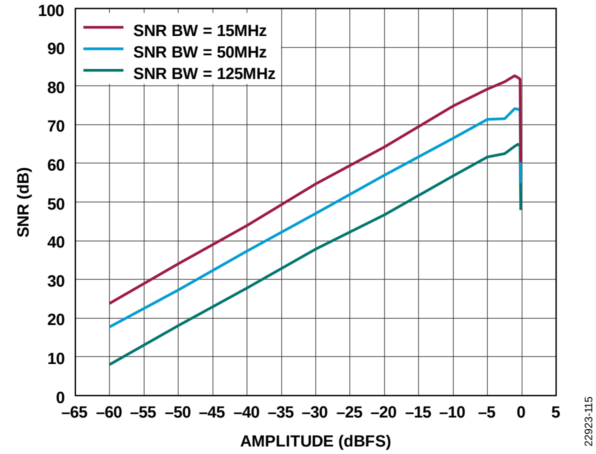

Figure 19. ADC SNR vs. Input Amplitude, 2 GSPS

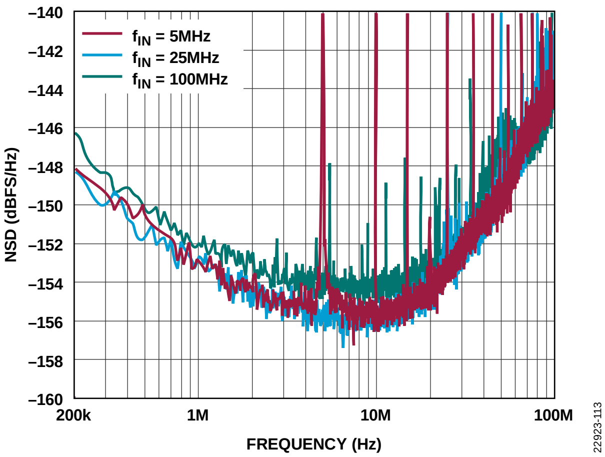

Figure 17. ADC NSD at Different Input Frequencies, 2 GSPS

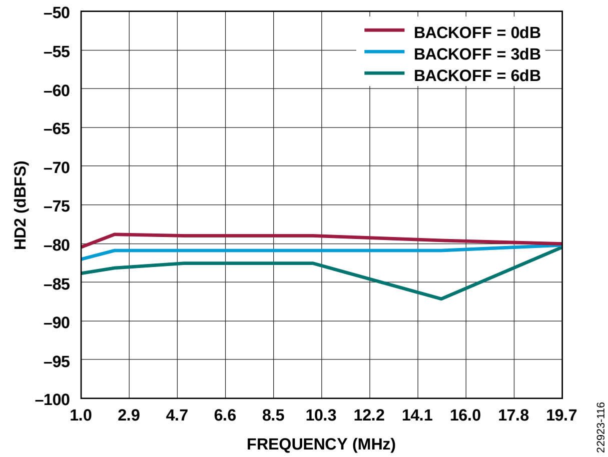

Figure 20. ADC HD2 vs. Frequency at Various Backoff Values and A_{IN} = −2 dB, 1 GSPS

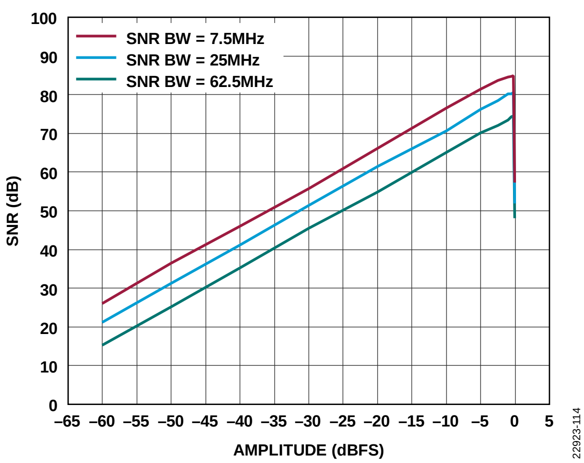

Figure 18. ADC SNR vs. Input Amplitude, 1 GSPS

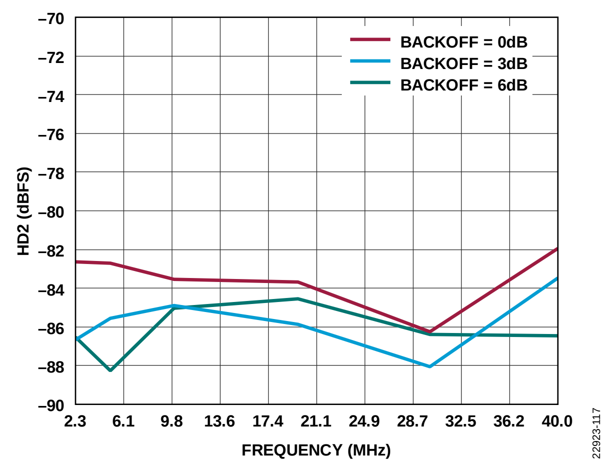

Figure 21. ADC HD2 vs. Frequency at Various Backoff Values and A_{IN} = −2 dB, 2 GSPS

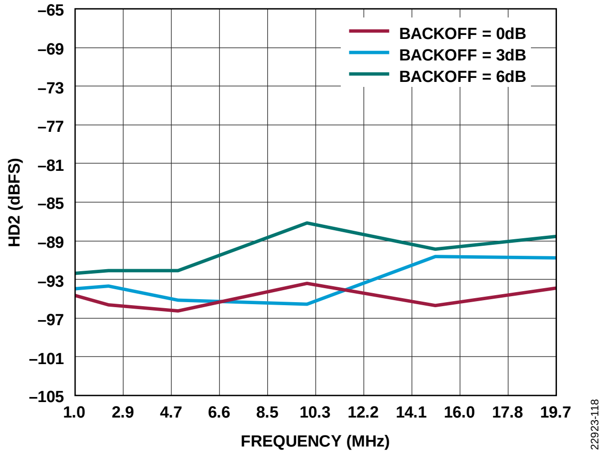

Figure 22. ADC HD2 vs. Frequency at Various Backoff Values and A_{IN} = −10 dB, 1 GSPS

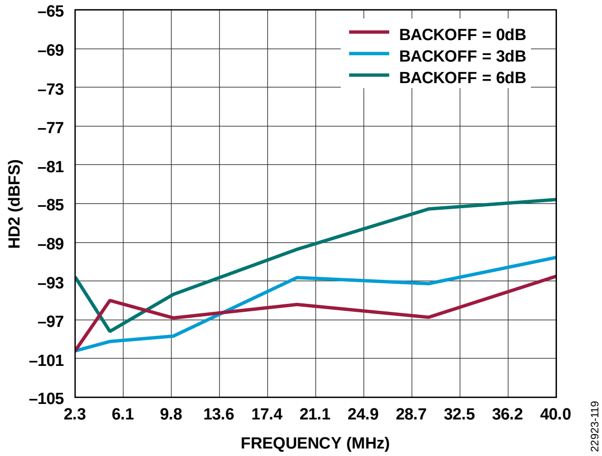

Figure 23. ADC HD2 vs. Frequency at Various Backoff Values and A_{IN} = −10 dB, 2 GSPS

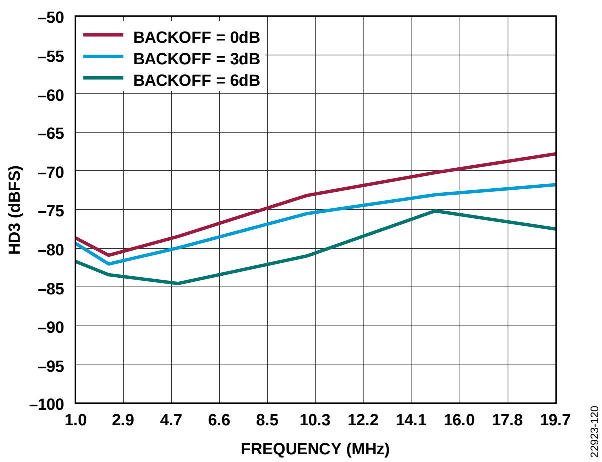

Figure 24. ADC HD3 vs. Frequency at Various Backoff Values and A_{IN} = −2 dB, 1 GSPS

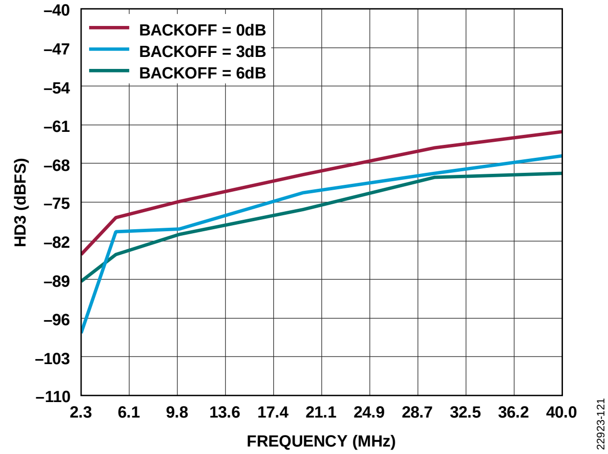

Figure 25. ADC HD3 vs. Frequency at Various Backoff Values and A_{IN} = −2 dB, 2 GSPS

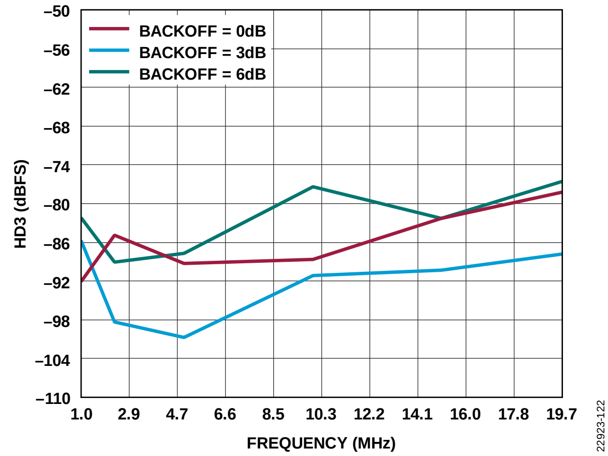

Figure 26. ADC HD3 vs. Frequency at Various Backoff Values and A_{IN} = −10 dB, 1 GSPS

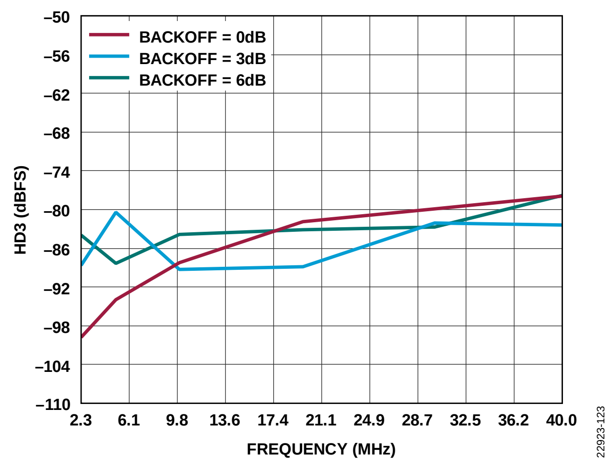

Figure 27. ADC HD3 vs. Frequency at Various Backoff Values and A_{IN} = −10 dB, 2 GSPS

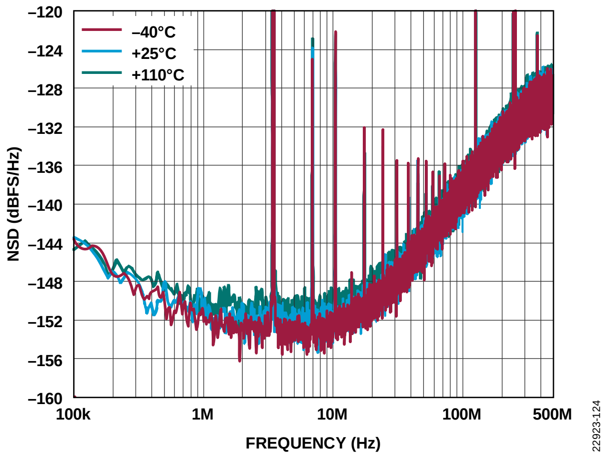

Figure 28. ADC NSD vs. Junction Temperature, 1 GSPS

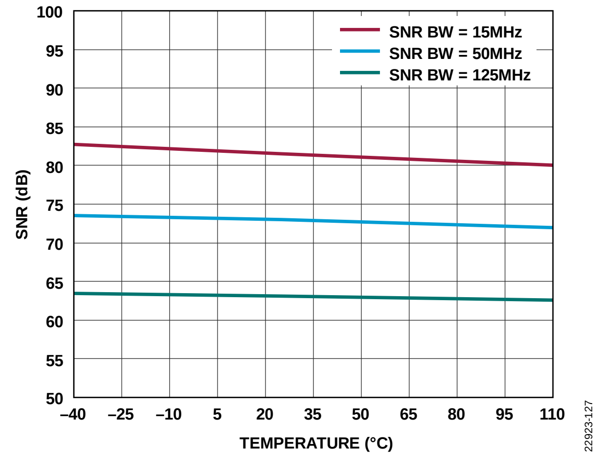

Figure 31. ADC SNR vs. Junction Temperature, 2 GSPS

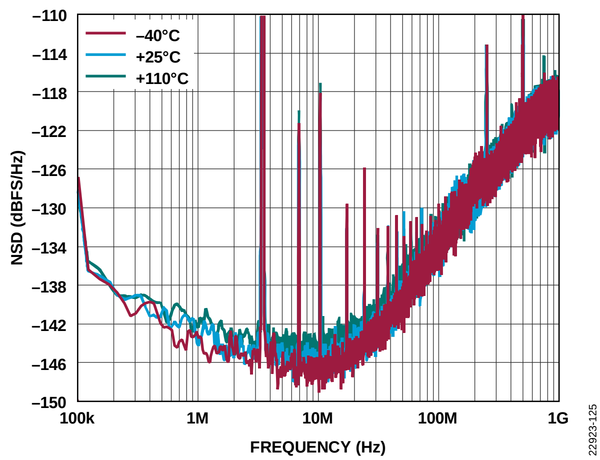

Figure 29. ADC NSD vs. Junction Temperature, 2 GSPS

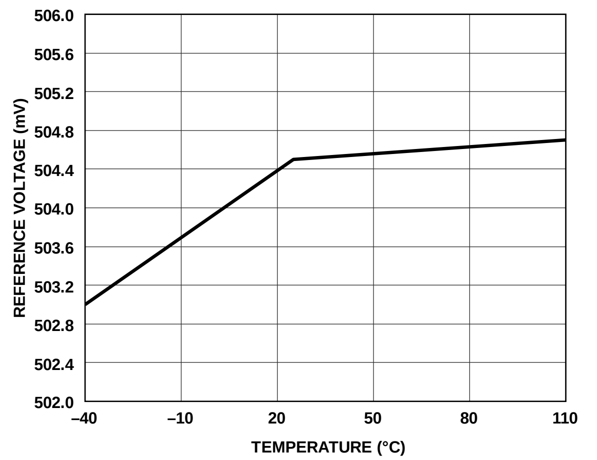

Figure 32. Reference Voltage vs. Junction Temperature

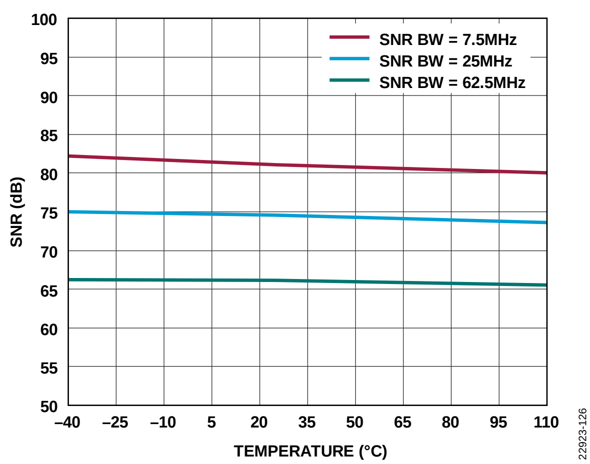

Figure 30. ADC SNR vs. Junction Temperature, 1 GSPS

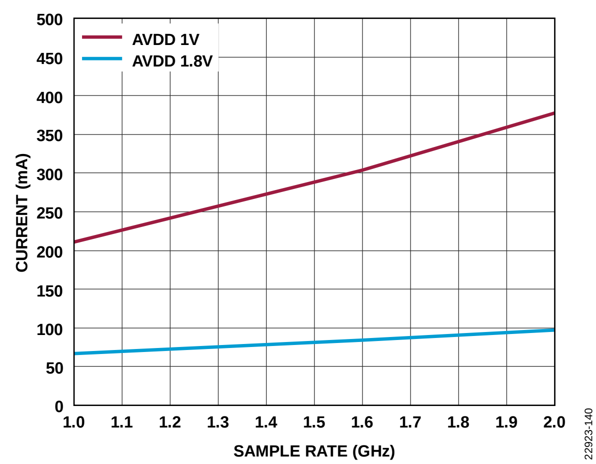

Figure 33. Supply Current vs. Sample Rate (Digital Domain Currents Vary with the DSP and JESD204B Setup)

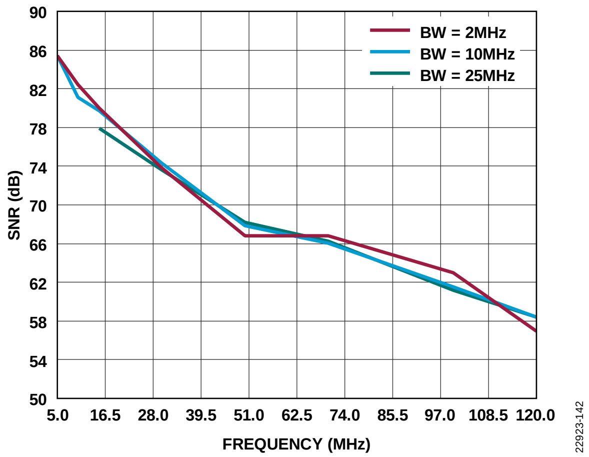

Figure 34. SNR vs. Sliding IF

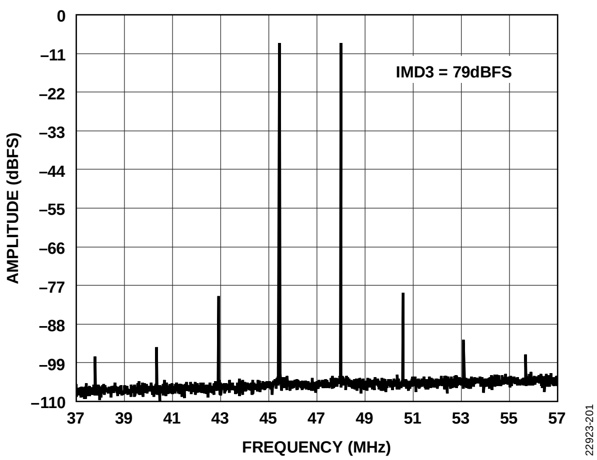

Figure 35. Two-Tone FFT, Backoff = 0, f_{IN1} = 45.4 MHz, f_{IN2} = 48 MHz, AIN1 and AIN2 = −8 dBFS, 1 GSPS

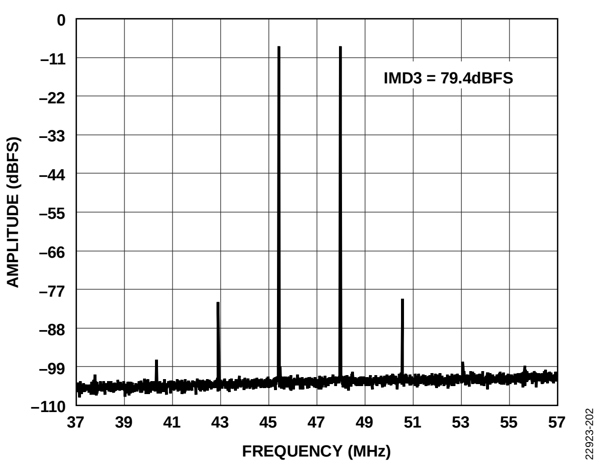

Figure 36. Two-Tone FFT, Backoff = 3, f_{IN1} = 45.4 MHz, f_{IN2} = 48 MHz, AIN1 and AIN2 = −8 dBFS, 1 GSPS

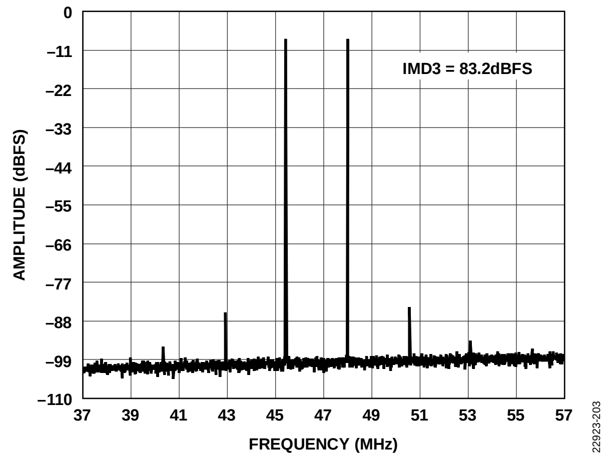

Figure 37. Two-Tone FFT, Backoff = 6, f_{IN1} = 45.4 MHz, f_{IN2} = 48 MHz, AIN1 and AIN2 = −8 dBFS, 1 GSPS

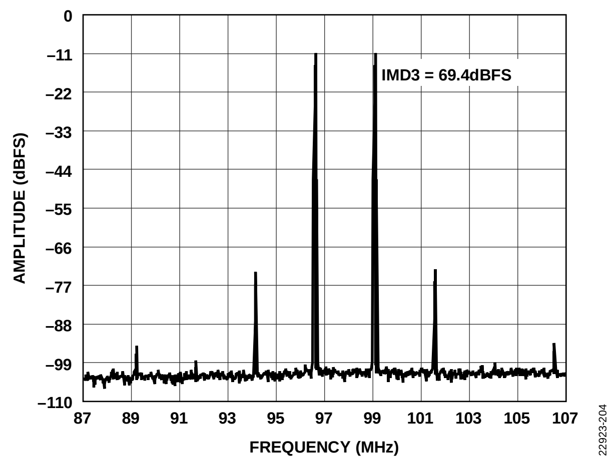

Figure 38. Two-Tone FFT, Backoff = 0, f_{IN1} = 96.6 MHz, f_{IN2} = 99 MHz, AIN1 and AIN2 = −8 dBFS, 2 GSPS

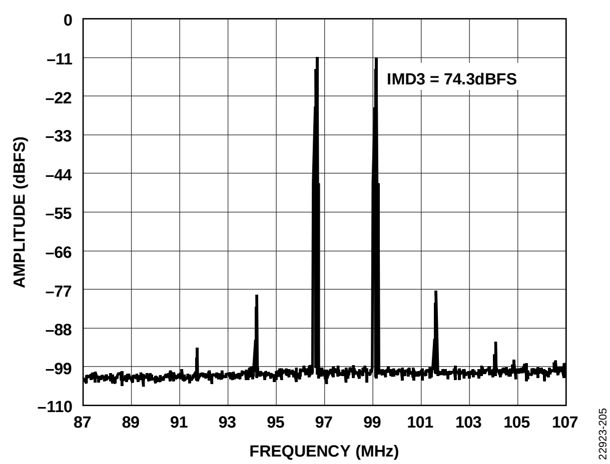

Figure 39. Two-Tone FFT, Backoff = 3, f_{IN1} = 96.6 MHz, f_{IN2} = 99 MHz, AIN1 and AIN2 = −8 dBFS, 2 GSPS

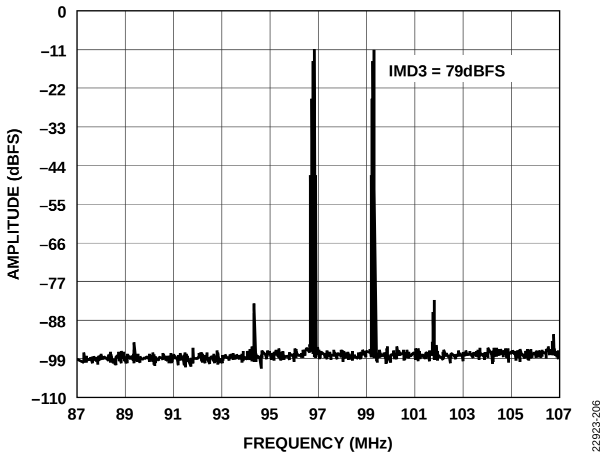

Figure 40. Two-Tone FFT, Backoff = 6, f_{IN1} = 96.6 MHz, f_{IN2} = 99 MHz, AIN1 and AIN2 = −8 dBFS, 2 GSPS

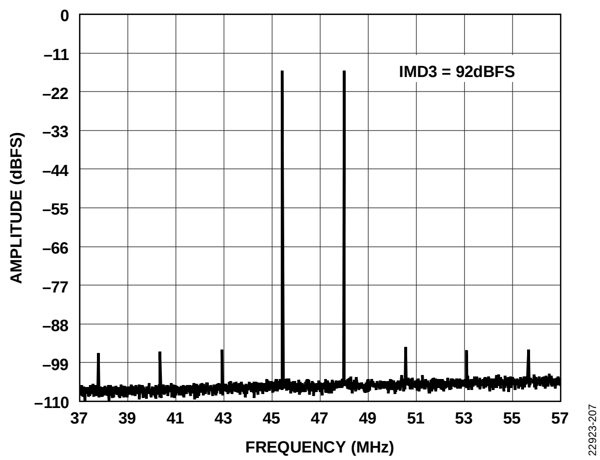

Figure 41. Two-Tone FFT, Backoff = 0, f_{IN1} = 45.4 MHz, f_{IN2} = 48 MHz, AIN1 and AIN2 = −16 dBFS, 1 GSPS

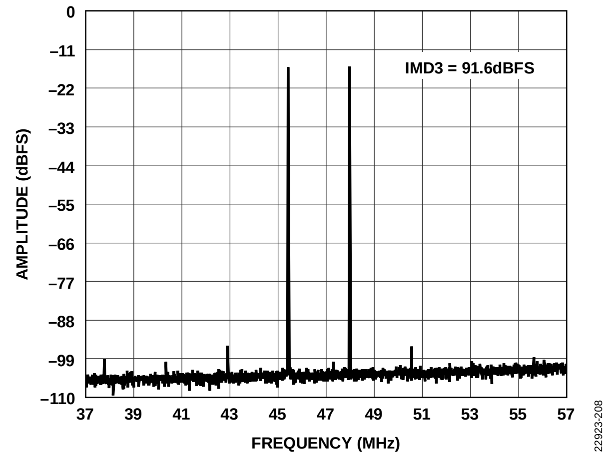

Figure 42. Two-Tone FFT, Backoff = 3, f_{IN1} = 45.4 MHz, f_{IN2} = 48 MHz, AIN1 and AIN2 = −16 dBFS, 1 GSPS

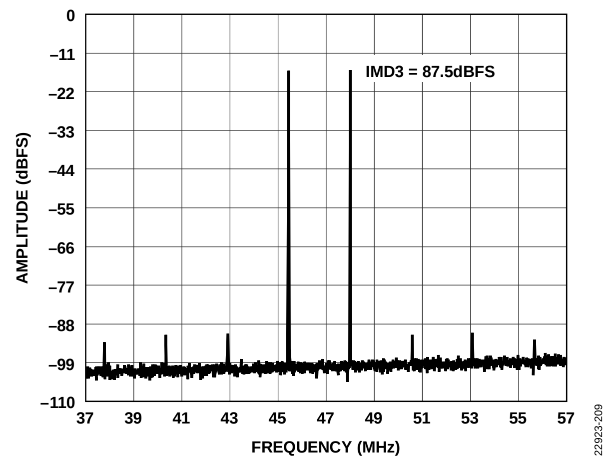

Figure 43. Two-Tone FFT, Backoff = 6, f_{IN1} = 45.4 MHz, f_{IN2} = 48 MHz, AIN1 and AIN2 = −16 dBFS, 1 GSPS

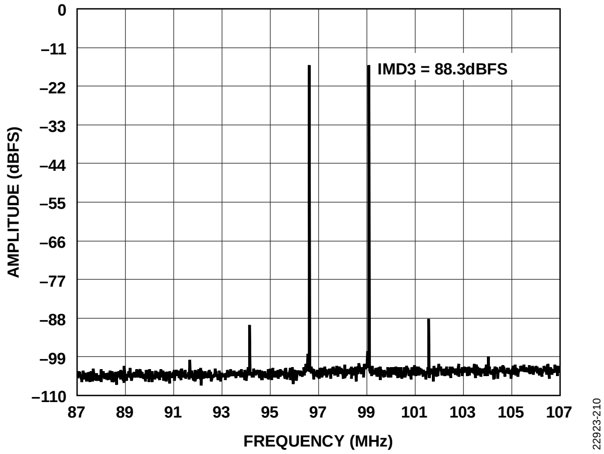

Figure 44. Two-Tone FFT, Backoff = 0, f_{IN1} = 96.6 MHz, f_{IN2} = 99 MHz, AIN1 and AIN2 = −16 dBFS, 2 GSPS

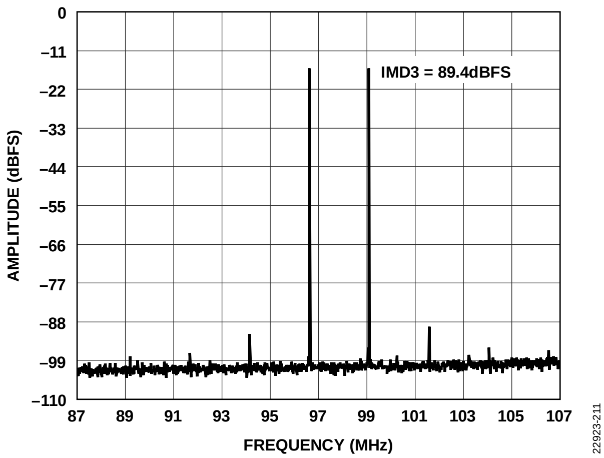

Figure 45. Two-Tone FFT, Backoff = 3, f_{IN1} = 96.6 MHz, f_{IN2} = 99 MHz, AIN1 and AIN2 = −16 dBFS, 2 GSPS

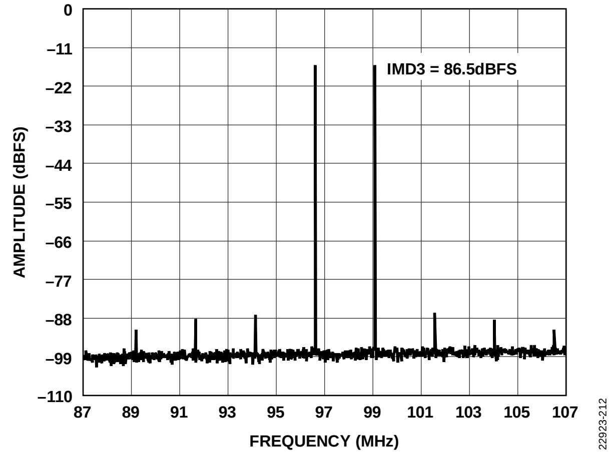

Figure 46. Two-Tone FFT, Backoff = 6, f_{IN1} = 96.6 MHz, f_{IN2} = 99 MHz, AIN1 and AIN2 = −16 dBFS, 2 GSPS

EQUIVALENT CIRCUITS

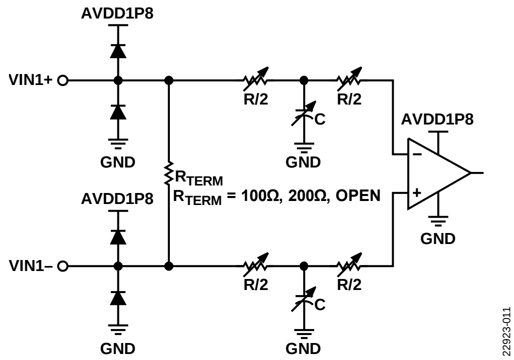

Figure 47. Analog Inputs

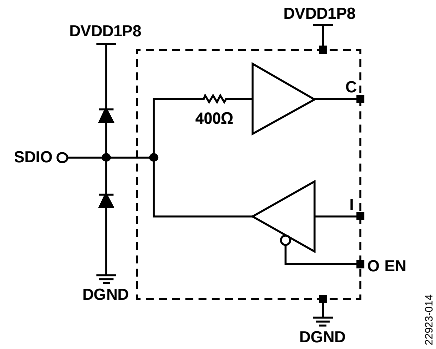

Figure 50. SDIO Input/Output

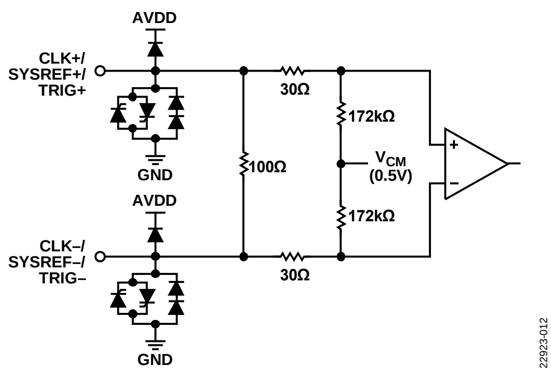

Figure 48. CLK±, SYSREF±, and TRIG± Inputs

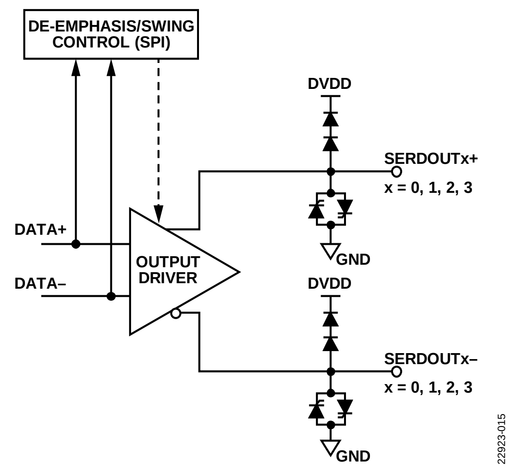

Figure 51. Digital Outputs

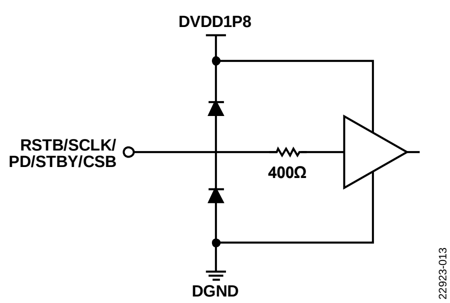

Figure 49. RSTB, SCLK, PD/STBY, and CSB Inputs

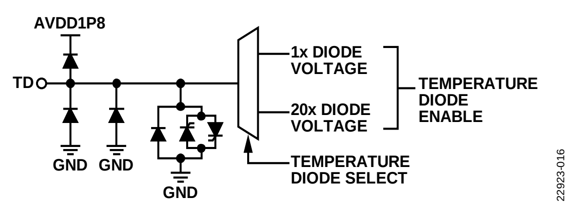

Figure 52. TD (Temperature Diode) Pin

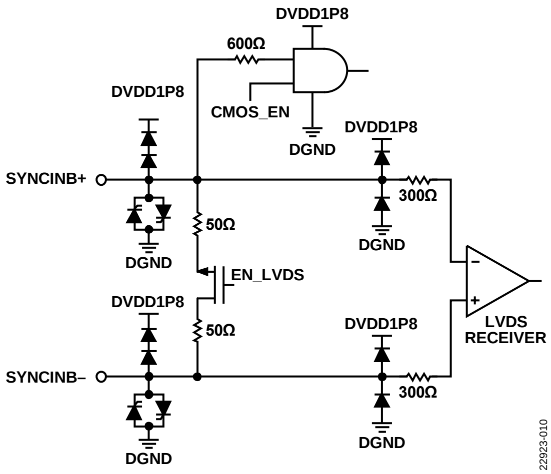

Figure 53. SYNCINB± Input

TERMINOLOGY

Noise Spectral Density (NSD)

The NSD is the noise power normalized to 1 Hz bandwidth (at a particular frequency) relative to the full-scale of the ADC (dBFS). NSD is given in units of dBFS/Hz. Unlike a descrete-time flash type ADC, a Σ-Δ ADC displays uneven NSD across the spectrum from dc up to f_S. Typical NSD at various inflection points are reported in the specifications. The total SNR is not always a straightforward calculation and it is often useful to think in terms of noise density instead of SNR. Achieving a good SNR is dependent on filtering out the wideband CTSD ADC quantization noise.

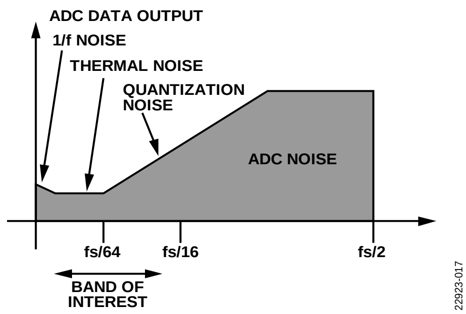

Figure 54. Noise Regions of a Σ-Δ ADC

In-Band Noise

In-band noise is the integrated noise power measured over a user defined bandwidth relative to the full-scale of the ADC (in dBFS). This bandwidth is typically equal to an intermediate frequency (IF) pass-band.

Third-Order Intermodulation Distortion (IMD3)

IMD3 is a figure of merit used to quantify the linearity of a component or system. Two equal amplitude, unmodulated carriers at specified frequencies (f_1 and f_2) injected in a nonlinear system exhibiting third-order nonlinearities produce IMD components at $2f_1 − f_2$ and $2f_2 − f1$. Note that the IMD3 performance of an ADC does not necessarily follow the 3:1 rule that is typical of RF/IF linear devices. IMD3 performance is dependent on dual tone frequencies, signal input levels, and the ADC clock rate.

Harmonic Distortion (HD2, HD3 and SFDR)

A harmonic tone that falls within the IF band of interest when a single tone is swept across the user defined frequency range.

Signal Transfer Function (STF)

STF is the frequency response of the ADC output signal relative to a swept single tone at the ADC input. The Typical Performance Characteristics section shows the STF over the IF pass-band to highlight pass-band flatness. The STF also affects aliasing of undesired signal near f_S.

THEORY OF OPERATION

ADC ARCHITECTURE

The AD9083 is a 16-channel, highly integrated and programmable front-end digitizer for a wide range of applications.

The AD9083 ADC uses a first-order, CTSD modulator architecture that provides first-order quantization noise shaping and inherent first-order, sinc shaped, antialias filtering. This oversampling, combined with the inherent antialias filtering, eliminates thermal noise folding into the band of interest. This feature enables a fast signal settling time when compared to the settling time of Nyquist rate converters, which require highly selective antialias filters to eliminate noise folding. The first-order Σ-Δ modulator is superior to a higher order modulator because the former requires only a second-order CIC decimation filter to eliminate quantization noise before decimation. This low order decimation filter features better signal settling time compared to a higher order filter. Built into the ADC front end is a programmable termination resistor, programmable gain adjust, and a programmable, single-pole, low-pass filter (LPF).

Background calibration digitally calibrates signal path gain error and nonlinearity. The ADC noise density is shaped, not flat, and is better at lower bandwidths. The worst case ADC noise density at a 2 GHz sample rate and 100 MHz offset is −147 dBFS/Hz. For a 2 GSPS sample rate and at 100 MHz bandwidth, the input referred noise figure is only 0.1 dB with 40 dB of front-end gain.

Flicker noise may be higher for this architecture, lending itself to better performance for IF applications instead of zero IF. Similarly, input referred offset has no effect on an IF application, except when using the full dynamic range of the signal converter. A low power mode is available with a noise density increase of 3 dB for half the converter power.

The ADC in the AD9083 must be initialized and set up based on the particular use case. Figure 55 shows the block diagram of the ADC used in the AD9083. The ADC in the AD9083 requires a set of user-defined variables that set up the ADC in the use case specified by the application. These variables are as follows:

- f_S, the sample clock of the converter core (1.0 GSPS to 2.0 GSPS).
- V_{MAX}, the differential peak-to-peak input full scale (0.5 V p-p, differential, to 2.0 V p-p, differential).
- f_C, the cutoff frequency of the LPF (125 MHz to 800 MHz).
- R_{TERM}, the differential input termination resistance.
- f_{INMAX}, the maximum input signal frequency.
- Backoff, the reduction in front-end gain for increased linearity.
- EN_HP, which increases the SNR by 2.5 dB by doubling the ADC power dissipation.

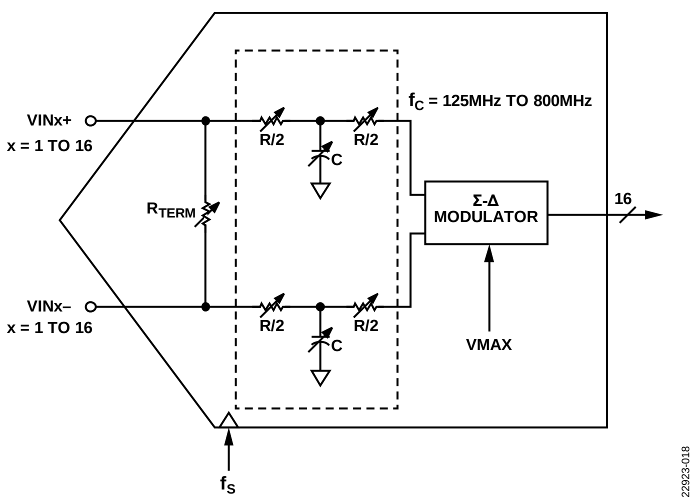

Figure 55. AD9083 ADC Block Diagram

LOW-PASS, CTSD ADC OVERVIEW

The AD9083 uses a voltage control oscillator (VCO)-based CTSD modulator ADC to convert the analog input to a digital word. The digital word can then be processed by a digital backend that provides decimation filtering, rate adjustment, DDC frequency shifting, and FIR filtering. The ADC samples at a rate (f_S) between 1 GSPS and 2 GSPS. The typical maximum oversampling ratio (OSR) is 8 for a usable bandwidth up to $f_S/16$.

LOW-PASS Σ-Δ ADC

Figure 56 shows a simplified, single-ended representation of the low power Σ-Δ ADC modulator. The ADC is a first-order, single-stage modulator. The NTF is first order. Therefore, a relatively high OSR is required to reduce noise in the signal band of interest. For a more detailed description of the modulator, see IEEE JSSC 2010 and IEEE JSSC 2013.

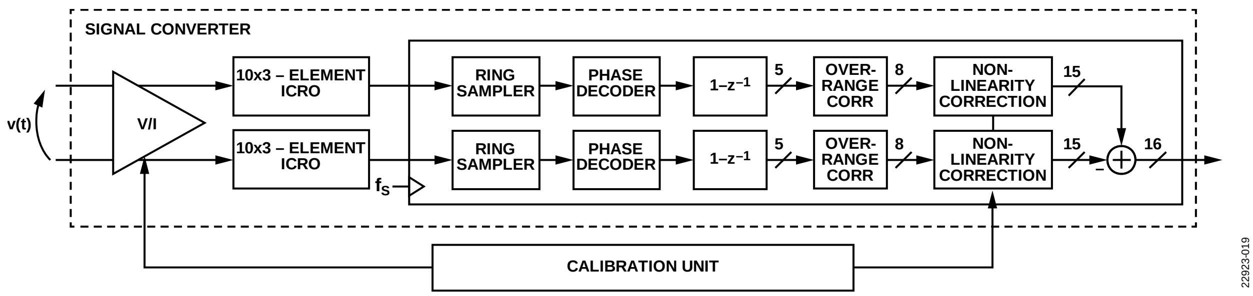

Figure 56. Simplified, Single-Ended, Low Power, Σ-Δ ADC Modulator

At signal frequencies below $f_S/64$, the dominant noise source is white thermal noise. Above this frequency, the noise is dominated by shaped quantization noise rising at 6 dB/octave. At the maximum signal bandwidth of $f_S/16$, quantization noise is the dominant noise source (see Figure 54). The ac performance tables give measurements of the NSD at various frequencies and ADC settings.

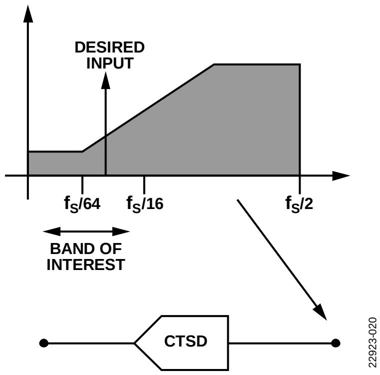

Figure 57. Noise Shaping Characterisctic of a Σ-Δ ADC

A digital decimation filter that follows the modulator removes the large out-of-band quantization noise (see Figure 57) while also reducing the data rate.

ANALOG INPUTS

The analog input to the AD9083 is a differential buffer. The internal common-mode voltage of the buffer is 1.1 V when ac coupling. When dc coupling, the allowable level is 0.5 V to 1.0 V. The nominal V_{MAX} level of the ADC is 1.8 V p-p, differential. This V_{MAX} level is programmable from 0.5 V p-p to 2.0 V p-p.

The inputs of the AD9083 are terminated using a programmable differential resistor. This differential resistor can be programmed to 100 Ω, 200 Ω, or can be left open. Following the termination resistor is a programmable single-pole, LPF. The maximum signal bandwidth of the AD9083 is 125 MHz ($f_S/16$) for a 2 GHz ADC f_S. The f_C of the LPF can be programmed to be between 125 MHz to 800 MHz to reduce input noise to the ADC. In particular, this noise includes unwanted signals near f_S that can alias down to the band of interest.

For applications where unwanted signals are not present, increasing the cutoff frequency of this filter improves the signal flatness out to the required signal bandwidth of the ADC. For best ADC noise performance, place the IF below $f_S/20$, where f_S is the ADC sample rate.

Differential Input Considerations

The AD9083 ADC uses a first-order, CTSD modulator architecture that provides first-order quantization noise shaping and inherent first-order, sinc shaped, antialias filtering. This oversampling, combined with the inherent antialias filtering, eliminates thermal noise folding into the band of interest. Therefore, there is no need for an antialiasing filter in the front end. The inputs can be differentially coupled using a balun/transformer or an amplifier. The inputs can also be ac- or dc-coupled. Moreover, the AD9083 inputs are resistively terminated, which makes it easier for amplifiers to drive the AD9083 analog inputs. Figure 58, Figure 59, Figure 60, and Figure 61 show some commonly applicable ways to provide an input to the AD9083.

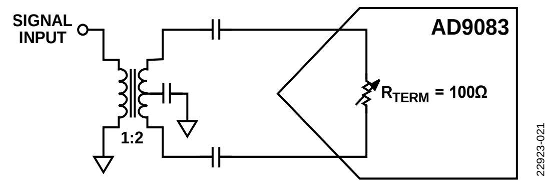

Figure 58. AC-Coupled Inputs to the AD9083 Using a Transformer

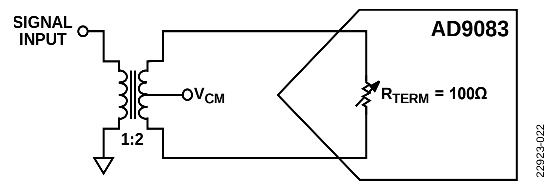

Figure 59. DC-Coupled Inputs to the AD9083 Using a Transformer (Note the Center Tap Connection Providing the Common-Mode Voltage)

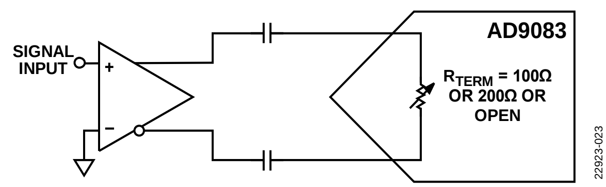

Figure 60. AC-Coupled Inputs to the AD9083 Using an Amplifier

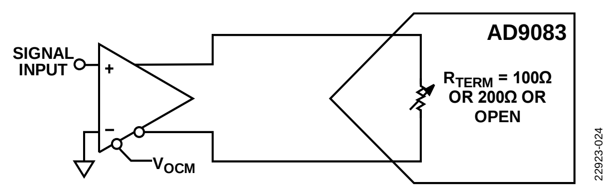

Figure 61. DC-Coupled Inputs to the AD9083 Using an Amplifier (Note the V_{OCM} Pin Providing the Common-Mode Voltage)

Σ-Δ Analog Input Considerations

A discrete time ADC aliases signals around the sample clock frequency and the corresponding multiples to the band of interest (see Figure 62). Therefore, an external antialias filter is needed to reject these signals.

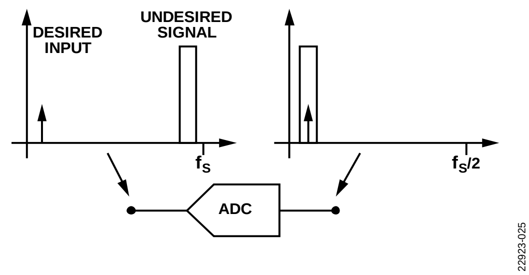

Figure 62. Aliasing in a Discrete Time ADC

In contrast, the CTSD modulator used in the AD9083 has some inherent antialiasing that lessens the antialias filtering requirements. The antialiasing property results from the signal processing inherent to the ADC architecture. The intrinsic STF of the ADC is that of a first-order sinc filter.

Additionally, a single-pole, first-order, programmable LPF is integrated in front of the ADC. This filter is SPI programmable between the 125 MHz to 800 MHz bandwidth.

The STF + LPF filtering at the front end reduces aliasing of undesired signals near the sample rate, f_S (see Figure 63).

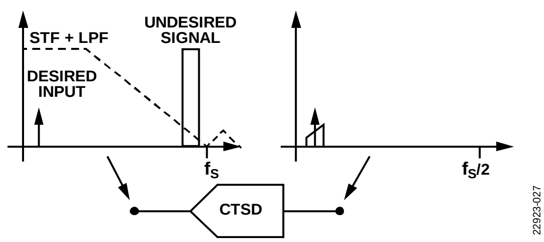

Figure 63. Alias Rejection of Σ-Δ ADC

Input Common Mode

The analog inputs of the AD9083 are programmable resistors internally dc biased to 1.1 V. The device typically expects a common-mode input of 0.5 V to 1.0 V with a nominal voltage of 0.7 V. An internal reference loop automatically senses the input common mode and sources a current across the input resistor network to generate the appropriate common-mode level shift across each R_{IN} (see Figure 64). The circuit driving the AD9083 must be able to sink this common-mode current. To set the value of the current use the following equation:

$$I_{SINK} = (1.1\text{ V} - V_{CM})/(R_{IN})$$

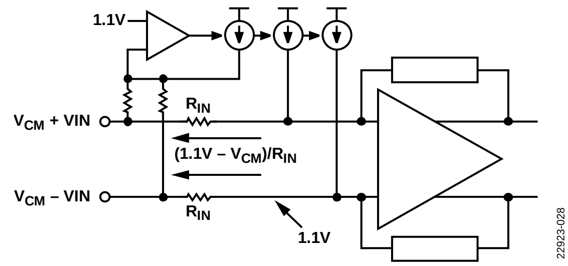

Figure 64. Input Stage of the AD9083 Showing the Common Mode Voltage Generation

The AD9083 can also be configured for ac-coupled applications. In this case, the output of the ac-coupling capacitor is biased to 1.1 V by the input circuit (see Figure 65).

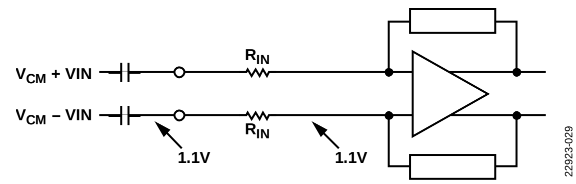

Figure 65. AC-Coupled Application Using the AD9083

Setting the device so that V_{CM} = 0.7 V is recommended for optimum performance. However, the device can function over a wider range with reasonable performance.

Input Termination

A differential input termination can be enabled via the SPI register. This termination value can be either 100 Ω, 200 Ω, or high impedance. On-chip foreground calibration is performed after startup to reduce the device to device variation of resistor and capacitor values due to tolerances associated with the device process. This calibration improves the termination value tolerances, as well as the LPF tolerances discussed previously

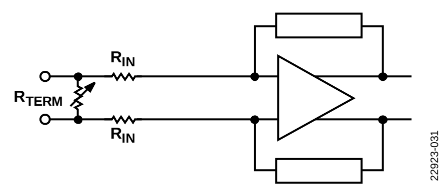

Figure 66. Programmable Input Termination of the AD9083

Input Signal Overload

Unlike a traditional CTSD ADC, the AD9083 ADC saturates much like a flash converter. The ADC does not become unstable (as with a traditional CTSD ADC), and the recovery time is one clock cycle.

CLOCK INPUTS

The AD9083 ADC sample clock is generated by using the on-chip, integrated, integer PLL VCO by providing a reference clock signal to the CLK± differential inputs (Pin K3 and Pin J3). Clock multiplying employs the on-chip ADC PLL that accepts a reference clock operating at a submultiple of the desired ADC sample rate. The operating range of the clock multiplier reference input is 50 MHz to 500 MHz. The PLL then multiplies the reference clock up to the desired ADC sample clock frequency, which generates all the clocks within the AD9083. The block diagram of the on-chip PLL is shown in Figure 68.

The AD9083 contains a low jitter, differential clock receiver that is capable of interfacing directly to a differential clock source. The input is self biased with a nominal impedance of 100 Ω. It is recommended that the clock source be ac-coupled to the CLK± input pins. Improved phase noise performance can be achieved with a higher clock input level. The quality of the clock source, as well as its interface to the AD9083 clock input, directly impacts ac performance. Select the phase noise and spur characteristics of the clock source to meet the target application requirements. The typical phase noise performance of the on-chip PLL when clocking the AD9083 at a 2 GHz sample rate is shown in Figure 67.

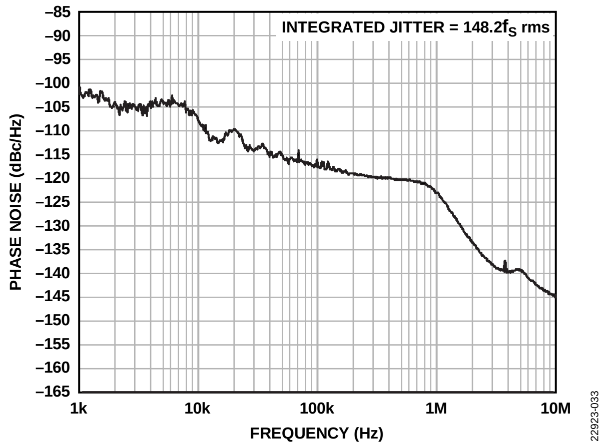

Figure 67. AD9083 On-Chip PLL Phase Noise vs. Frequency Offset, 2 GHz ADC Sample Rate, On-Chip DDC Enabled

For optimal performance of the on-chip PLL, connect a low ESR, low ESL, X7R dielectric, 2.2 μF capacitor between the REG_VCO pin and GND. Additionally, connect a C0G or NP0 dielectric, 33 nF capacitor between the VCOARSE_VCO pin and GND. Place these capacitors as close to the AD9083 chip as possible to avoid any external noise coupling.

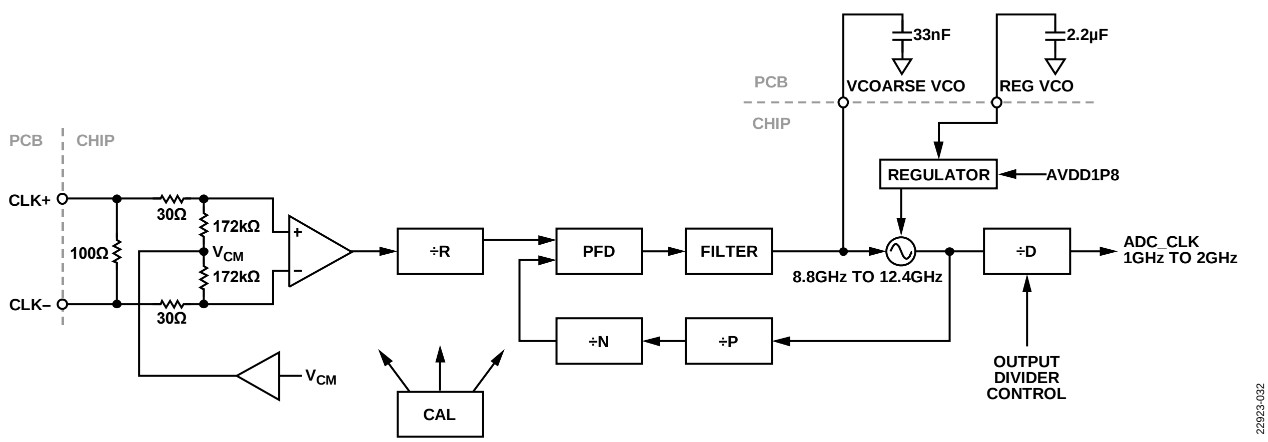

Figure 68. AD9083 Clock Path Block Diagram

POWER MODES

The AD9083 features low power modes that enable powering down certain blocks of the AD9083, or the entire chip, based on trade-offs between power saving achieved and wake-up time to full power on. These sections discuss the power-down modes available within the AD9083. All modes are controlled via the SPI.

Full Power-Down Mode

In full power-down mode, almost all of the blocks within the AD9083 are held in low power mode, resulting in the highest power saving. However, this power saving results in slow wake-up times. The ADC internal reference, on-chip clock PLL, and the JESD204B PLL are powered on. On release of this mode, the ADC must undergo recalibration. The on-chip clock PLL and the JESD204B PLL must undergo relocking to achieve normal performance.

Standby Mode

In standby mode, some of the blocks are kept running while others are held in a clock gated mode, resulting in medium power saving, but faster wake-up time compared to full power-down mode. The ADC cores, on-chip clock PLL, JESD204B PLL, and digital outputs are kept powered on. The digital and JESD204B framer blocks are clock gated. The JESD204B link must be reinitialized on release of this mode.

Power-On Mode

Power-on mode is the normal operation mode for the AD9083. All blocks within the AD9083 are powered up and running at rated frequency. However, to further reduce power during normal operation, digital portions that do not need to be running can be selectively clock gated. For example, if the application only requires one numerically controlled oscillator (NCO)/mixer, the other two NCOs/mixers can be disabled. The same principle applies to the JESD204B lanes. The unused lanes can be powered down.

TEMPERATURE DIODE

The AD9083 contains diode-based temperature sensors. The output voltages of these diodes correspond to the temperature of the silicon. There is a pair of diodes, one of which is 20× the size of the other. It is recommended to use both diodes to obtain an accurate estimate of the die temperature. For more information, see the AN-1432 Application Note, *Practical Thermal Modeling and Measurements in High Power ICs.* The temperature diode voltages can be exported to the TD pin using the SPI (see Figure 69).

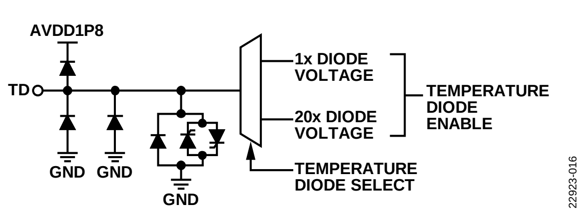

Figure 69. TD Pin Using the SPI

DIGITAL SIGNAL PROCESSING OVERVIEW

The CTSD ADC includes a digital processing block between the CTSD ADC output and the JESD204 transmitter core. The digital signal processing block can filter and translate IF to zero IF signals suitable for post processing by the host without any loss of dynamic range. This block includes a programmable CIC decimation filter, a mixer with NCO, and a highly programmable, multistage decimation FIR filter. Figure 70 shows a simplified diagram of the digital functional block. For clarity, Figure 70 does not show the digital datapath routing options, which are described in the Signal Processing Tile section.

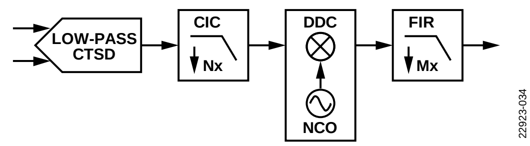

Figure 70. Simplified Diagram of the Digital Functional Block

The CTSD ADC provides a highly oversampled digital output representing the desired IF signal pass band and the out-of-band shaped noise. Figure 71 shows the spectrum of the raw ADC output.

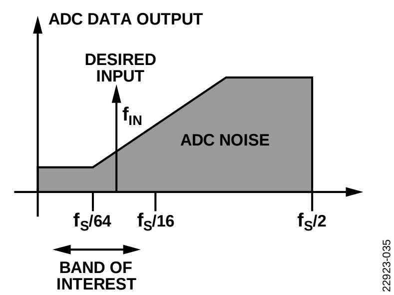

Figure 71. Spectrum of the Raw ADC Output

The digital signal path first filters and decimates the ADC output data by Nx. It is necessary to remove the majority of the out of band quantization noise before any clock rate reduction or frequency translation. Figure 72 shows the decimator output frequency spectrum.

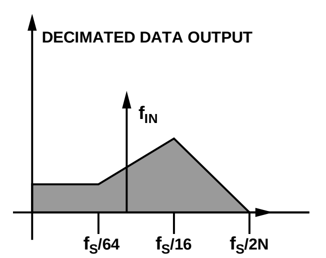

Figure 72. Frequency Spectrum of the Decimator Output

Next, the DDC can be enabled to perform a frequency translation. Typically, this frequency translation is from a middle IF down to zero IF or very low IF. Figure 73 shows a representative of the output spectrum of the DDC output.

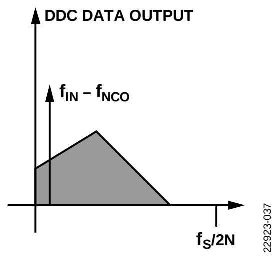

Figure 73. Output Spectrum of the DDC Output

Finally, the FIR can filter and downsample the baseband signal to a much lower data rate suitable for transfer via the JESD204B interface. Figure 74 shows a representative of the output spectrum of the FIR filter output of a baseband signal.

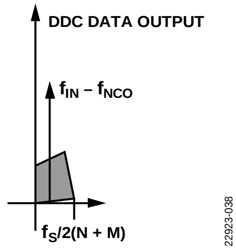

Figure 74. Output Spectrum of the FIR Filter Output of a Baseband Signal

Care must be taken when selecting the JESD204B output data format. Both 12- and 16-bit data modes are available, and the user must be careful to select a word length that does not add significant truncation noise to the baseband signal. Very narrow-band baseband applications may see high SNR values in the FIR output data. In all cases, the truncation noise density is well below the baseband NSD.

The following equation shows the quantization noise density for truncation errors:

$$NSD_{TRUNCATION} = 20\log_{10}(2^{BITS}) + 10\log_{10}(BW_{BASEBAND})$$

For example, with 12-bit JESD204B data and a 2 MHz baseband bandwidth, the truncation error NSD is only −135 dBFS, which is well above the ADC noise floor. In this narrow-band example, 16 bits are required to reduce the truncation error to −159 dBFS, which is well below the ADC noise level under all IF conditions.

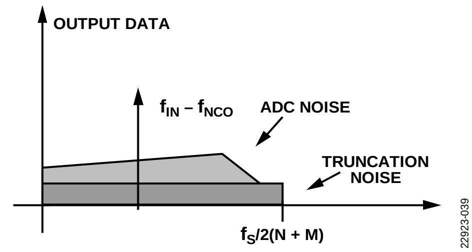

Figure 75. Example Showing ADC Noise Unaffected by Truncation Error

Truncation error that is well above the ADC noise floor may not only add to the noise floor but may also add spurious content when the truncation noise is correlated with the input signal.

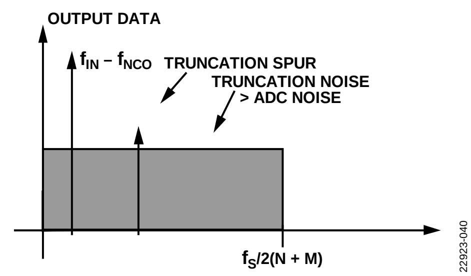

Figure 76. Example Showing ADC Noise Affected by Truncation Error

SIGNAL PROCESSING TILE

Each ADC has a signal processing tile to filter out of band shaped noise from the Σ-Δ ADC and to reduce the sample rate, resulting in 16 total tiles (see Figure 77).

Each tile contains a CIC filter and a DDC with multiple FIR decimation filters, known as the decimate by J filter block. The decimate by J filter block can be used with or without the quadrature mixer/NCO. For data gating applications, there are up to three quadrature DDC channels using an averaging filter, G, that selects and decimates the data.

Each processing block has control lines that allow the block to be independently enabled and disabled to provide the desired processing function. Multiplexers are enabled within the processing tile to send the data appropriate to the application use case. The register bits responsible for datapath selection by the multiplexors are shown in Figure 67.

There are three NCOs (NCO_0 to NCO_2) available for the signal processing tile, one for each mixer. NCO_2 and NCO_3 are only used when the device is configured for data gating. The same three NCOs are used for all 16 signal processing tiles.

The signal processing tile can be configured to output either real data or complex output data. The output is complex when using the mixer. The signal processing tile outputs a 16-bit stream. To enable this operation, the converter number of bits, N, is set to a default value of 16.

For typical high performance RF applications, the ADC can provide either a real output for zero IF inputs, or a quadrature output for low IF inputs. The datapath through the signal processing tile uses the multiple FIR decimate by J filters with optional frequency translation using the mixer/NCO_0 block. This datapath is referred to as the nonburst mode datapath.

For applications using stepped frequency modulation bursts (SFCW), time must be allowed for settling. Data gating is used to select the number valid samples (G) of the pulse burst for averaging prior to decimation. Decimation reduces the data samples by 1/H. This datapath is referred to as the burst mode. In burst mode, each input channel is provided with three quadrature DDCs. All channels are programmed the same, but the individual DDCs and averaging FIR filters within a channel can be configured for a different frequency.

Due to the JESD204B output line rate limitation (16 Gbps/lane) and the number of lanes available (four), care must be taken to ensure that the total throughput from all 16 signal processing tiles does not exceed the maximum allowable line rate. Therefore, not all combinations of CIC filter decimation, J decimation, or averaging (H) decimation are supported.

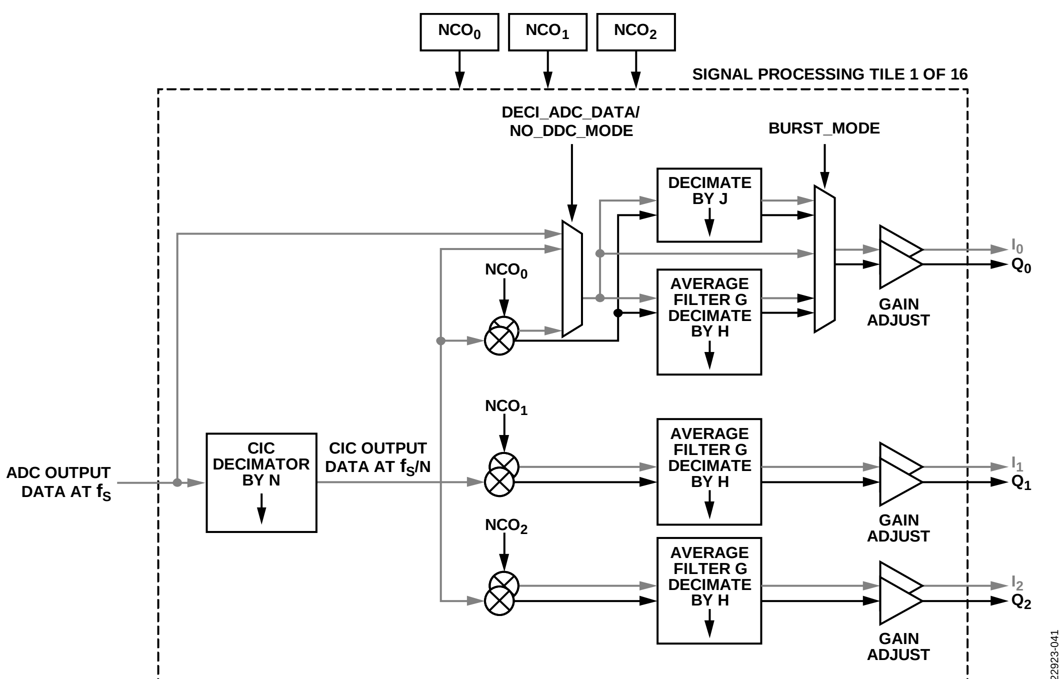

Figure 77. Signal Processing Tile Following Each ADC Channel (1 of 16)

CASCADED INTEGRATOR COMB (CIC) FILTER

Data from each ADC is sent to the CIC filter. The CIC filter can be bypassed, and the ADC data sent to the DDCs to decimate the data. This is enabled by writing a 1 to the DECI_ADC_DATA bit (Bit DB4) in the DP_CTRL register. In this mode, the mixer is bypassed. Therefore, there is no frequency shifting available.

The frequency response of the CIC filter built in to the AD9083 is identical to that of a second-order moving average filter of Length N, where N is the decimation rate. The decimation rates allowed are 4×, 8×, or 16×, based on the setting. The output of the CIC filter is a single 16-bit data sample at a rate of f_S/N where f_S is the ADC sample rate and N is the CIC decimation ratio setting.

The response of the CIC filter under different decimation settings is shown in Figure 78. The response is normalized to the ADC sample frequency (f_S). This normalization helps the end user with frequency planning. For example, if the ADC f_S is 2 GSPS, a fundamental frequency placed at 100 MHz incurs CIC losses of 1.09 dB, 4.77 dB, and 25.17 dB for CIC decimation ratios of 4×, 8×, and 16×, respectively. Therefore, for this application use case, it is best to select a CIC decimation ratio of 4× and rely on the DDC decimation to further decimate the data.

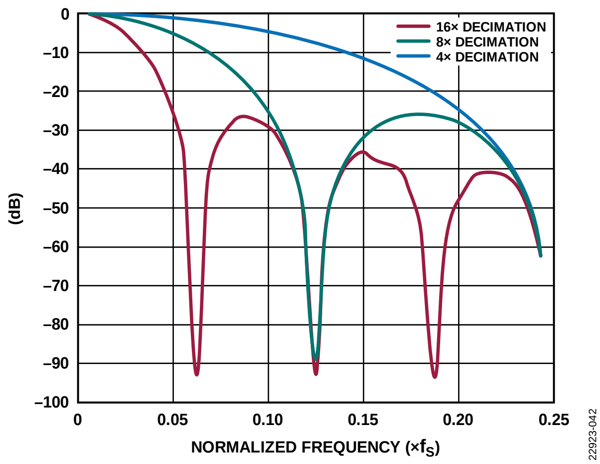

Figure 78. CIC Filter Response for Decimation Ratio = 4×, 8×, and 16×; Normalized to f_S

Adjust the CIC droop with a programmable gain adjustment. For each sample frequency, the tones are at different frequency values and the value of droop correction required is different. Figure 79 shows the droop characteristics to a finer detail.

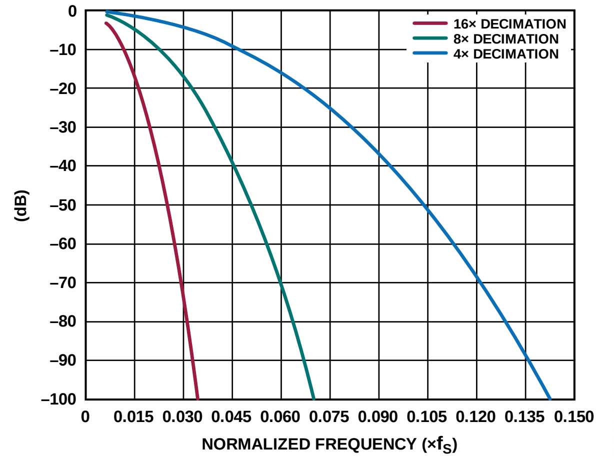

Figure 79. Zoomed in Image of the CIC Filter Response Shown in Figure 78; Normalized to f_S

The AD9083 digital datapath has a block that can be used to program the gain to compensate for the droop. Based on the application and the input frequency, the user can program the appropriate gain to compensate for the loss through the CIC filter. The gain setting to compensate for the loss is calculated as follows

$$\textit{Fractional Bit Calculation} \geq \text{frac}(10^{(-\text{Droop}/20)}) \times 2^{10}$$

For example, if the input frequency is 25 MHz, Table 18 shows the gain setting needed to compensate for the droop for the various CIC decimation ratios for various frequencies. As shown in Figure 79, the CIC roll-off must be considered when designing the AD9083 in a system. As a general rule, keep the IF to within 20% of the output data rate. For example, if the highest frequency in the system is 100 MHz, then a CIC decimation of 4× is recommended. Conversely, if a CIC decimation of 16× is chosen, keep the IF below 25 MHz.

The CIC gain is programmed as an unsigned 4.10 word. The first four bits represent the integer portion of the gain, and the following 10 bits represent the fraction portion of the gain.

Table 18. Example Gain Compensation Settings for various CIC filter Roll-Off Values; f_S = 2 GHz

Frequency (MHz)	4× Decimation		8× Decimation	
	CIC Droop (dB)	Gain Compensation (Unsigned 4.10)	CIC Droop (dB)	Gain Compensation (Unsigned 4.10)
25	−0.0669177	0001_00_0000_1000	−0.28	0001_00_0010_0010
50	−0.2687053	0001_00_0010_0000	−1.14	0001_00_1001_0000

NONBURST MODE DATAPATH

Figure 80 shows the signal processing configuration in the nonburst mode datapath. The input data can be direct from the ADC or via the output of the CIC filter. The datapath uses multiplexers configurable by the DP_CTRL register (Register 0x116) to appropriately route the data. The multiplexer control bits are shown in Figure 80.

- The NO_DDC_MODE bit (Register 0x0116, Bit 1) of the DP_CTRL register bypasses the NCO/mixer where frequency translation is not required.
- The BURST_MODE bit (Register 0x0116, Bit 2]) of the DP_CTRL register) selects the decimate by J filter block.

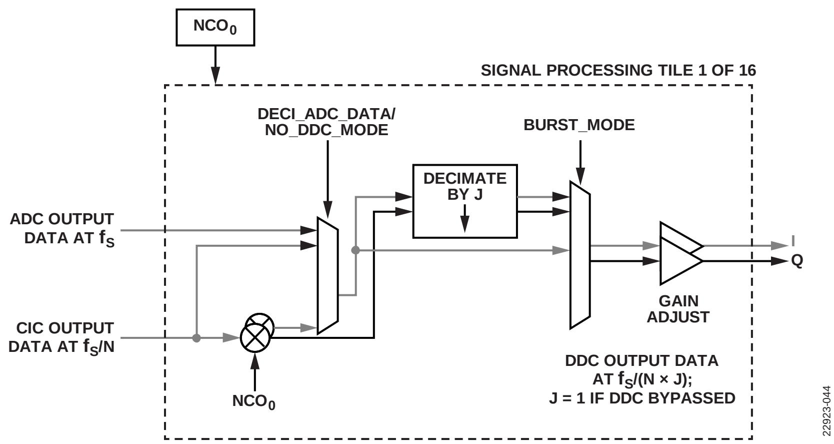

Figure 80. Nonburst Mode Datapath Within the Signal Processing Tile Following Each ADC Channel (1 of 16)

Decimate by J Filters

After the frequency translation stage, there are multiple decimation filter stages that reduce the output data rate. After the carrier of interest is tuned down to dc (carrier frequency = 0 Hz), these filters efficiently lower the sample rate, while providing sufficient alias rejection from unwanted adjacent carriers around the bandwidth of interest.

When the decimate by J block is supplied with direct data from the ADC, there is no mixing option. Only decimation occurs. The valid J decimation options are determined by the path before the decimate by J block. Table 19 lists the available J decimation options determined by the input data path.

The decimate by J block supports decimation ratios of 1, 4, 8, 10, 12, 16, 20, 24, 30, 40, and 60, as shown in Table 19.

Decimation rates of 1, 4, 10, and 30 are valid only when CIC is not bypassed (for example, DECI_ADC_DATA is equal to 0).

Figure 81 shows the detailed block diagram of the Decimate by J filters.

Table 12 describes the filter characteristics of the different FIR filter blocks.

Table 21 shows the different filter configurations selectable by including different filters. In all cases, the decimate by J filtering stage provides 81.4% of the available output bandwidth, <±0.005 dB of pass-band ripple, and >100 dB of stop band alias rejection. Table 22 shows the coefficients for the various finite impulse response (FIR) filters used in the AD9083.

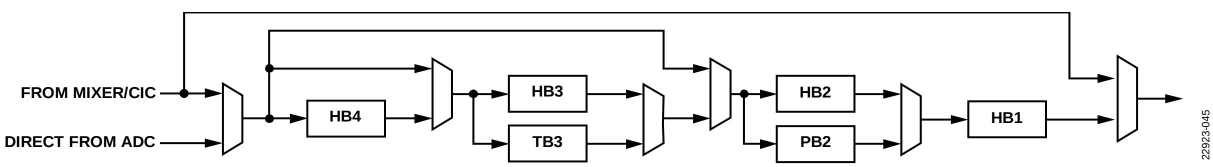

Figure 81. Decimate by J Filters Block Diagram

Table 19. J Decimation Rate

CIC Filter and NCO0/Mixer Bypassed (DECI_ADC_DATA = 1 and NO_DDC_MODE = 1)	CIC Filter Enabled and NCO0/Mixer Bypassed (DECI_ADC_DATA = 0 and NO_DDC_MODE = 1)	CIC Filter and NCO0/Mixer Enabled (DECI_ADC_DATA = 0 and NO_DDC_MODE = 0)
Invalid	1 (bypass mode)	1 (bypass mode)
Invalid	4	4
8	8	8
Invalid	10	Invalid
12	12	Invalid
16	16	16
20	20	Invalid
24	24	Invalid
40	40	Invalid
Invalid	30	Invalid
60	60	Invalid

Table 20. Decimation Filter Characteristics

Filter Name	Decimation Ratio	Pass Band (rad/sec)	Stop Band (rad/sec)	Pass-Band Ripple (dB)	Stop Band Rejection (dB)
HB4	2	0.1 × π/2	π/2 × 1.9	<±0.001	>100
HB3	2	0.2 × π/2	π/2 × 1.8	<±0.001	>100
HB2	2	0.4 × π/2	π/2 × 1.6	<±0.001	>100
HB1	2	0.8 × π/2	π/2 × 1.2	<±0.001	>100
TB3	3	0.3 × π/3	π/3 × 1.8	<±0.001	>100
PB2	5	0.4 × π/5	π/5 × 1.6	<±0.001	>100

Table 21. DDC Filter Configurations

DDC Input Sample Rate[1]	DDC Filter Configuration	Decimation Ratio	Output Bandwidth
f_{IN}	Not applicable	1	$-f_{IN}$ to $+f_{IN}$
	HB1 + HB2	4	0.814 × ($-f_{IN}$/4 to $+f_{IN}$/4)
	HB1 + HB2 + HB3	8	0.814 × ($-f_{IN}$/8 to $+f_{IN}$/8)
	HB1 + PB2	10	0.814 × ($-f_{IN}$/10 to $+f_{IN}$/10)
	HB1 + HB2 + TB3	12	0.814 × ($-f_{IN}$/12 to $+f_{IN}$/12)
	HB1 + HB2 + HB3 + HB4	16	0.814 × ($-f_{IN}$/16 to $+f_{IN}$/16)
	HB1 + PB2 + HB3	20	0.814 × ($-f_{IN}$/20 to $+f_{IN}$/20)
	HB1 + HB2 + TB3 + HB4	24	0.814 × ($-f_{IN}$/24 to $+f_{IN}$/24)
	HB1 + PB2 + TB3	30	0.814 × ($-f_{IN}$/30 to $+f_{IN}$/30)
	HB1 + PB2 + HB3 + HB4	40	0.814 × ($-f_{IN}$/40 to $+f_{IN}$/40)
	HB1 + PB2 + TB3 + HB4	60	0.814 × ($-f_{IN}$/60 to $+f_{IN}$/60)

[1] $f_{IN} = f_S$/CIC_DEC_RATIO, where f_S is the ADC sample rate.

Table 22. DDC Filter Coefficients for Various FIR Filters in the AD9083

Coefficient Number	HB1	HB2	HB3	HB4	TB3	PB2
1	21'h1FFFF4	19'h000B4	17'h1FF91	19'h006D2	17'h00000	20'h00000
2	21'h00000	19'h00000	17'h00000	19'h00000	17'h00000	20'hFFFF9
3	21'h00002C	19'h7FA7E	17'h0039C	19'h7CBA8	17'h1FFE4	20'hFFFEE
4	21'h00000	19'h00000	17'h00000	19'h00000	17'h1FFA8	20'hFFFE6
5	21'h1FFF8C	19'h01766	17'h1EFC4	19'h12D86	17'h00000	20'h00000
6	21'h00000	19'h00000	17'h00000	19'h20000	17'h001F8	20'h0005A
7	21'h000102	19'h7B3EB	17'h04D0F	19'h12D86	17'h003F0	20'h000F6
8	21'h00000	19'h00000	17'h08000	19'h00000	17'h00000	20'h0018A
9	21'h1FFDFC	19'h1397E	17'h04D0F	19'h7CBA8	17'h1F352	20'h00178
10	21'h00000	19'h20000	17'h00000	19'h00000	17'h1EAB6	20'h00000
11	21'h0003B4	19'h1397E	17'h1EFC4	19'h006D2	17'h00000	20'hFFCD0
12	21'h00000	19'h00000	17'h00000		17'h03E55	20'hFF8B0
13	21'h1FF9A0	19'h7B3EB	17'h0039C		17'h088D8	20'hFF5DC
14	21'h00000	19'h00000	17'h00000		17'h0AAAA	20'hFF77C
15	21'h000A6E	19'h01766	17'h1FF91		17'h088D8	20'h00000
16	21'h00000	19'h00000			17'h03E55	20'h00F00
17	21'h1FEFA7	19'h7FA7E			17'h00000	20'h01F90
18	21'h00000	19'h00000			17'h1EAB6	20'h02894
19	21'h0018C0	19'h000B4			17'h1F352	20'h01FF2
20	21'h00000				17'h00000	20'h00000
21	21'h1FDB90				17'h003F0	20'hFCD26
22	21'h00000				17'h001F8	20'hF98A4
23	21'h003492				17'h00000	20'hF7DEE
24	21'h00000				17'h1FFA8	20'hF9A1E
25	21'h1FB50C				17'h1FFE4	20'h00000
26	21'h00000				17'h00000	20'h0AD60
27	21'h006AD4				17'h00000	20'h186CA
28	21'h00000					20'h25CC0
29	21'h1F64EC					20'h2F99B
30	21'h00000					20'h33330
31	21'h00ED96					20'h2F99B
32	21'h00000					20'h25CC0
33	21'h1E5BAE					20'h186CA
34	21'h00000					20'h0AD60
35	21'h0512F9					20'h00000

Coefficient Number	HB1	HB2	HB3	HB4	TB3	PB2
36	21'h080000					20'hF9A1E
37	21'h0512F9					20'hF7DEE
38	21'h00000					20'hF98A4
39	21'h1E5BAE					20'hFCD26
40	21'h00000					20'h00000
41	21'h00ED96					20'h01FF2
42	21'h00000					20'h02894
43	21'h1F64EC					20'h01F90
44	21'h00000					20'h00F00
45	21'h006AD4					20'h00000
46	21'h00000					20'hFF77C
47	21'h1FB50C					20'hFF5DC
48	21'h00000					20'hFF8B0
49	21'h003492					20'hFFCD0
50	21'h00000					20'h00000
51	21'h1FDB90					20'h00178
52	21'h00000					20'h0018A
53	21'h0018C0					20'h000F6
54	21'h00000					20'h0005A
55	21'h1FEFA7					20'h00000
56	21'h00000					20'hFFFE6
57	21'h000A6E					20'hFFFEE
58	21'h00000					20'hFFFF9
59	21'h1FF9A0					20'h00000
60	21'h00000					
61	21'h0003B4					
62	21'h00000					
63	21'h1FFDFC					
64	21'h00000					
65	21'h000102					
66	21'h00000					
67	21'h1FFF8C					
68	21'h00000					
69	21'h00002C					
70	21'h00000					
71	21'h1FFFF4					

BURST MODE DATAPATH

Figure 82 shows the block diagram for the burst mode datapath of one signal processing tile of the AD9083. The data from the CIC filter can be sent to three DDCs channels simultaneously at a rate of f_S/N (N = 4, 8, 16). Each DDC has a mixer fed with a 7-bit NCO that can be used to tune the outputs to dc. The number of DDCs used is programmable. The NCOs can be programmed to different frequencies, enabling frequency translations for up to three tones. The number of tones is defined in the NUM_TONES bits (Bits[DB6:5]) in the DP_CTRL register (Register 0x116). The averaging filter uses a programmable number of last valid samples of the pulse burst equal to G and a programmable decimation value equal to H. The timing of the burst is derived from either the TRIG input or the SYSREF.

In burst mode, the decimate by J filter block is bypassed. This bypass is enabled by the BURST_MODE bit (Bit DB2) in the DP_CTRL register.

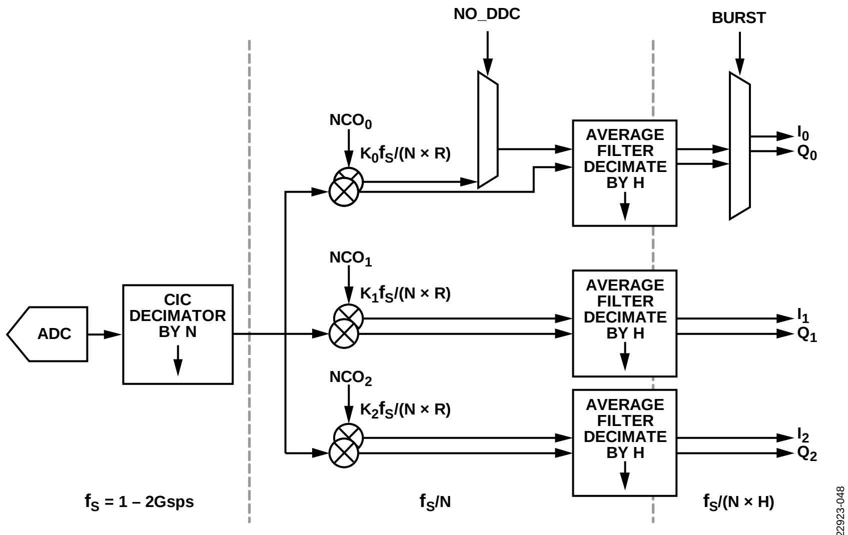

Figure 82. Averaging Filter Example Showing the Datapath

AVERAGING FILTERS

The averaging filters are used in the burst mode datapath. In contrast to traditional decimation filters, the averaging filters are designed for determining the phase and amplitude of a single continuous wave (CW) tone of a known frequency. The filters average G samples when the data is stable within every H window.

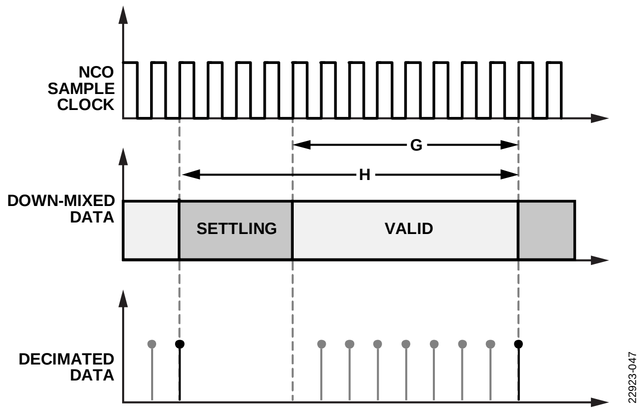

Figure 83. Averaging Filter

With the averaging filters, the user has the option to provide up to three different CW tones. The filters in each signal processing tile can use up to three NCOs. The three NCOs are shared by each of the channels. For example, Channel 15 must use the same three frequencies as Channel 2.

When using the burst mode datapath along with multiple CW tones, the frequencies of the tones (f_K) must be calculated per the following equation:

$$f_K = K \times \frac{f_S}{N \times G}$$

where:
f_S is the sample frequency.
N is the CIC N decimation.
G is the G value.
K = 1, 2, or 3 for Frequency 1, Frequency 2, or Frequency 3, respectively.

The supported values for G are 8 and 16. If G is 8, the supported H values are 12, 14, 16, 18. For a G value of 16, the supported H values are 24, 28, 32, 36.

Averaging Filter Example

In this example, the sample rate is 1.6 GSPS, N decimation = 4, and G = 16:

- f_{NCO1} = 1 × (1.6e9 / (4 × 16)) = 25 MHz.
- f_{NCO2} = 2 × (1.6e9 / (4 × 16)) = 50 MHz.
- f_{NCO3} = 3 × (1.6e9 / (4 × 16)) = 75 MHz.

Placing the frequencies like this is necessary to ensure that the two unwanted frequencies are located at the filter nulls of the selected NCO frequency and are removed. In the example shown, NCO_0 only allows the 25 MHz tone through, while nulling out the 50 MHz and 75 MHz tones. Similarly, NCO_1 only allows the 50 MHz tone through, while nulling out the 25 MHz and 75 MHz tones. See Figure 84 for the averaging filter frequency response at each stage of the datapath.

- f_S = 1.6 GSPS, CIC decimation = 8, G = 16, H decimation = 24.

In each case, the input frequency being observed must be identical to the NCO frequency, meaning that the output of the ADC appears to be dc. By looking at the dc values of the I and Q outputs, the phase and amplitude of the original CW tone can be determined.

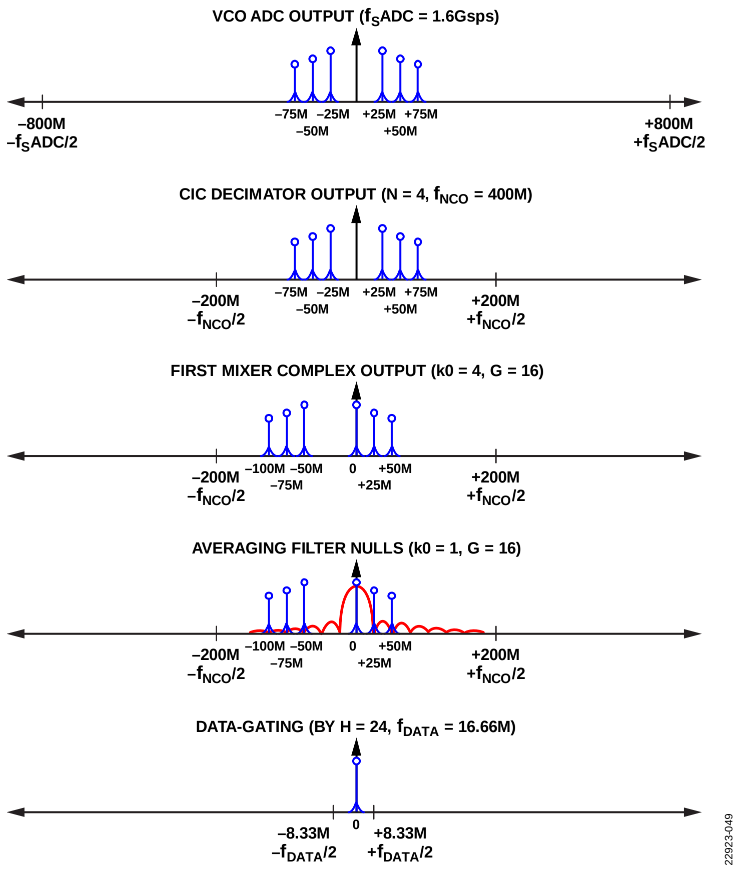

Figure 84. Averaging Filter Example Frequency Response

MIXERS

For nonburst mode RF applications, DDC_0 using NCO_0/mixer for frequency translation can be selected. In applications where real data outputs are required, the mixer can be bypassed.

For data gating applications using burst mode, there are three mixers available. These mixers are supplied by NCOs that can be set to three different frequencies, enabling multiple frequency translations (see the Averaging Filters section).

NCO FTW DESCRIPTION

There are three identical NCOs in the AD9083: NCO_0 to NCO_2. Each NCO enables the frequency translation process by creating a complex exponential frequency ($e^{-j\omega t}$), which can be mixed with the input spectrum to translate the desired frequency band of interest to dc, where it can be filtered by the subsequent LPF blocks to prevent aliasing. The NCO frequency tuning word (FTW) is 7-bits wide. The NCO output is 12-bits. All 16 signal processing tiles use the outputs from the same three NCOs (NCO_0 to NCO_2).

The NCO FTW can be calculated by the following equation:

$$NCO\_FTW = floor\left(2^7 \frac{\text{mod}(f_C, f_{IN})}{f_{IN}}\right)$$

where:
NCO_FTW is the 7-bit twos complement number representing the NCO FTW.
f_C is the desired carrier frequency.
f_{IN} is the input frequency to the DDC.

$$f_{IN} = \frac{f_S}{CIC\_DEC\_RATIO}$$

where *CIC_DEC_RATIO* is the CIC decimation ratio and can be 1, 4, 8, or 16.

mod(x) is a remainder function. For example mod(110,100) = 10 and for negative numbers, mod(−32,10) = −2.

floor(x) is defined as the largest integer less than or equal to x. For example, floor(3.6) = 3.

Example FTW Calculation

In this example, the ADC sample rate (f_S) is 2 GHz. CIC_DEC_RATIO is set to 4. The desired f_C is 100 MHz. Plugging in the following values to the equation above yields an NCO_FTW value of 26.

f_C Calculation from FTW

The actual f_C from the example above can be calculated as follows:

$$Actual\_f_C = \frac{NCO\_FTW \times f_{IN}}{2^7}$$

For the example listed above, the actual tuning frequency is

$$Actual\_f_C = \frac{26 \times \left(\frac{2\text{ GHz}}{4}\right)}{2^7} = 101.5625\text{ MHz}$$

The example in this section shows that, even though the requested frequency is 100 MHz, the actual tuning frequency is about 1.5% off the actual value. It is important that the system designer be aware of this phenomenon and adjust the frequency plan of the logic device. One way to increase this resolution is to increase the CIC decimation ratio. In the previous example, if the CIC decimation ratio is increased to 8 (instead of 4), the NCO_FTW results in a value of 51, which calculates to 99.6094 MHz. This frequency only varies from the actual requested frequency of 100 MHz by ~0.4%. However, choosing this frequency plan results in an increased CIC filter droop, as shown in Figure 78. Therefore, care must be taken to choose the appropriate ADC sample rates, CIC decimation ratio, and the NCO frequency tuning word.

DIGITAL OUTPUTS

The AD9083 digital outputs are designed to the JEDEC standard JESD204B, serial interface for data converters. JESD204B is a protocol to link the AD9083 to a digital processing device over a serial interface with lane rates of up to 16 Gbps. The benefits of the JESD204B interface over LVDS include a reduction in required board area for data interface routing, and an ability to enable smaller packages for converter and logic devices.

JESD204B OVERVIEW

The JESD204B data transmit block assembles the parallel data from the ADC into frames and uses 8-bit/10-bit encoding as well as optional scrambling to form serial output data. Lane synchronization is supported through the use of special control characters during the initial establishment of the link. Additional control characters are embedded in the data stream to maintain synchronization thereafter. A JESD204B receiver is required to complete the serial link. For additional details on the JESD204B interface, refer to the JESD204B standard.

The AD9083 JESD204B data transmit block maps up to sixteen physical ADCs or up to 96 virtual converters (when all the DDCs are enabled) over a link. A link can be configured to use one, two, or four JESD204B lanes. The JESD204B specification refers to a number of parameters to define the link, and these parameters must match between the JESD204B transmitter (the AD9083 output) and the JESD204B receiver (the logic device input).

The JESD204B link is described according to the following parameters:

- L is the number of lanes per converter device (lanes per link); (AD9083 value = 1, 2, 3, or 4)
- M is the number of converters per converter device (virtual converters per link) (AD9083 value = 16, 32, 96)
- F is the octets/frame (AD9083 value = 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, 64, 72 or 96)
- N′ is the number of bits per sample (JESD204B word size) (AD9083 value = 12 or 16)
- N is the converter resolution
- CS is the number of control bits/sample (AD9083 value = 0, 1, 2, or 3)
- K is the number of frames per multiframe (AD9083 value = 8, 16, or 32)
- S is the samples transmitted/single converter/frame cycle (AD9083 value = set automatically based on L, M, F, and N′)
- HD is the high density mode (AD9083 = set automatically based on L, M, F, and N′)
- CF is the number of control words/frame clock cycle/converter device (AD9083 value = 0)

Figure 85 shows a simplified block diagram of the AD9083 JESD204B link. The AD9083 can be configured to use sixteen converters and four lanes. Data from all sixteen converters is output to SERDOUT0±, SERDOUT1±, SERDOUT2± and SERDOUT3±. The AD9083 allows other configurations, such as combining the outputs of all converters onto a single lane. These modes are customizable, and can be set up via the SPI.

In the AD9083, if N’ = 16, the N-bit converter word from each converter is broken into two octets (eight bits of data). Bit N − 1 (MSB) through Bit N-8 are in the first octet. The second octet contains Bit N − 9 through Bit 0 (LSB), CS control bits (the CS parameter defines the number of control bits), and tail bits, if necessary, are appended to the LSB’s to achieve N’ number of bits in the JESD word. If tail bits are needed, they can be configured as zeros or a pseudorandom number sequence. Control bits can be used to indicate overrange, SYSREF±, or fast detect output.

For modes where N’ = 12, each of the M/L samples on a lane are concatenated starting with sample 0 on lane 0 to create the F octets in each lane. If control bits are required, then N must equal N’ – CS.

The resulting octets can be scrambled. Scrambling is optional; however, it is recommended to avoid spectral peaks when transmitting similar digital data patterns. The scrambler uses a self-synchronizing, polynomial-based algorithm defined by the equation $1 + x^{14} + x^{15}$. The descrambler in the receiver is a self-synchronizing version of the scrambler polynomial.

The octets are then encoded with an 8-bit/10-bit encoder. The 8-bit/10-bit encoder works by taking eight bits of data (an octet) and encoding them into a 10-bit symbol.

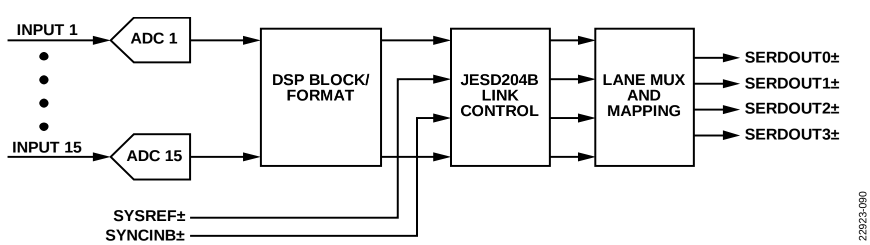

Figure 85. Transmit Link Simplified Block Diagram

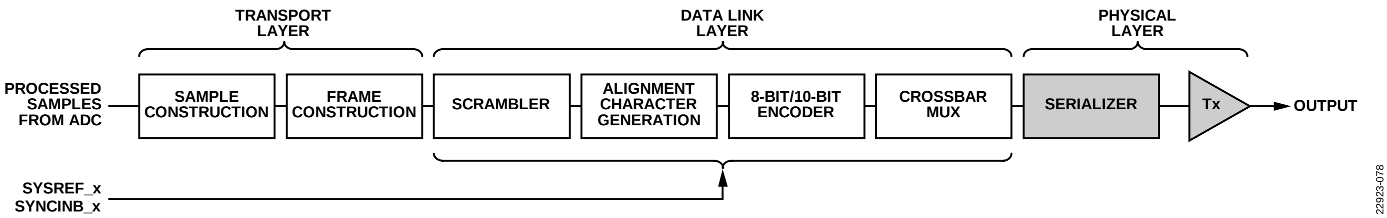

Figure 86. Data Flow

FUNCTIONAL OVERVIEW

The block diagram in Figure 86 shows the flow of data through the JESD204B hardware from the sample input to the physical output. The processing can be divided into layers that are derived from the open source initiative (OSI) model, widely used to describe the abstraction layers of communications systems. These layers are the transport layer, data link layer, and physical layer (serializer and output driver).

Transport Layer

The transport layer handles packing the data (consisting of samples and optional control bits) into JESD204B frames that are mapped to 8-bit octets. The packing of samples into frames are determined by the JESD204B configuration parameters for number of lanes (L), number of converters (M), the number of octets per lane per frame (F), the number of samples per converter per frame (S), and the number of bits in a nibble group (sometimes called the JESD204 word size – N').

Samples are mapped in order starting from Converter 0, then Converter 1, and so on until Converter M − 1. If S > 1, each sample from the converter is mapped before mapping the samples from the next converter. Each sample is mapped into words formed by appending converter control bits, if enabled, to the LSBs of each sample. The words are then padded with tail bits, if necessary, to form nibble groups (NGs) of the appropriate size as determined by the N' parameter. The following equation can be used to determine the number of tail bits within a nibble group (JESD204B word):

$$T = N' - N - CS$$

Data Link Layer

The data link layer is responsible for the low level functions of passing data across the link. These include optionally scrambling the data, inserting control characters during the initial lane alignment sequence (ILAS) and for frame and multiframe synchronization monitoring, and encoding 8-bit octets into 10-bit symbols. The data link layer is also responsible for sending the ILAS, which contains the link configuration data used by the receiver to verify the settings in the transport layer.

The implementation of the data link layer is discussed in the JESD204B Link Establishment section.

Physical Layer

The physical layer consists of the high speed circuitry clocked at the serial clock rate. In this layer, parallel data is converted into one, two, or four lanes of high speed differential serial data. The implementation of the Physical Layer is covered in the Physical Layer (Driver) Outputs section.

JESD204B LINK ESTABLISHMENT

The AD9083 JESD204B transmitter (Tx) interface operates in Subclass 0 or Subclass 1 as defined in the JEDEC Standard JESD204B (July 2011 specification). The link establishment process is divided into the following steps: code group synchronization, initial lane alignment sequence, and user data and error correction.

Code Group Synchronization (CGS)

CGS is the process by which the JESD204B receiver finds the boundaries between the 10-bit symbols in the stream of data. During the CGS phase, the JESD204B transmit block transmits /K/ characters (/K28.5/ symbols). The receiver must locate the /K/ characters in its input data stream using clock and data recovery (CDR) techniques.

The receiver issues a synchronization request by asserting the SYNCINB± pin of the AD9083 low. The JESD204B Tx then begins sending /K/ characters. After the receiver has synchronized, it waits for the correct reception of at least four consecutive /K/ symbols. It then de-asserts SYNCINB±. The AD9083 then transmits an ILAS on the following local multiframe clock (LMFC) boundary.

For more information on the code group synchronization phase, refer to the JEDEC Standard JESD204B, July 2011, Section 5.3.3.1.

The SYNCINB± pin operation can also be controlled by the SPI. The SYNCINB± signal is a differential dc-coupled LVDS mode signal by default, but it can also be driven single-ended.

The SYNCINB± pins can also be configured to run in CMOS (single-ended) mode by setting Bit 0 in Register 0x447. When running SYNCINB± in CMOS mode, connect the CMOS SYNCINB signal to Pin 21 (SYNCINB+) and leave Pin 20 (SYNCINB−) disconnected.

Initial Lane Alignment Sequence (ILAS)

The ILAS phase follows the CGS phase and begins on the next LMFC boundary after SYNCINB± deassertion. The ILAS consists of four mulitframes, with an /R/ character marking the beginning and an /A/ character marking the end. The ILAS begins by sending an /R/ character followed by 0 to 255 ramp data for one multiframe. On the second multiframe, the link configuration data is sent, starting with the third character. The second character is a /Q/ character to confirm that the link configuration data follows. All undefined data slots are filled with ramp data. The ILAS sequence is never scrambled.

The ILAS sequence construction is shown in Figure 87. The four multiframes include the following:

- Multiframe 1 begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 2 begins with an /R/ character followed by a /Q/ character (/K28.4/), followed by link configuration parameters over 14 configuration octets (see Table 23) and ends with an /A/ character. Many of the parameter values are of the value – 1 notation.
- Multiframe 3 begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 4 begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).

User Data and Error Detection

After the initial lane alignment sequence is complete, the user data (ADC samples) is sent. During transmission of the user data, a mechanism called character replacement monitors the frame clock and multiframe clock alignment. This mechanism replaces the last octet of a frame or multiframe with an /F/ or /A/ alignment characters when the data meets certain conditions.

These conditions are different for unscrambled and scrambled data. The scrambling operation is enabled by default, but it can be disabled using the SPI.

For scrambled data, any 0xFC character at the end of a frame is replaced by an /F/, and any 0x7C character at the end of a multiframe is replaced with an /A/. The JESD204B receiver (Rx) checks for /F/ and /A/ characters in the received data stream and verifies that they only occur in the expected locations. If an unexpected /F/ or /A/ character is found, the receiver handles the situation by using dynamic realignment or asserting the SYNCINB± signal for more than four frames to initiate a resynchronization. For unscrambled data, if the final octet of two subsequent frames are equal, the second octet is replaced with an /F/ symbol if it is at the end of a frame, and an /A/ symbol if it is at the end of a multiframe.

Insertion of alignment characters can be modified using SPI. The frame alignment character insertion (FACI) is enabled by default.

8-Bit/10-Bit Encoder

The 8-bit/10-bit encoder converts 8-bit octets into 10-bit symbols and inserts control characters into the stream when needed. The control characters used in JESD204B are shown in Table 23. The 8-bit/10-bit encoding ensures that the signal is dc balanced by using the same number of ones and zeros across multiple symbols.

The 8-bit/10-bit interface has options that can be controlled via the SPI. These operations include bypass and invert. These options are troubleshooting tools for the verification of the digital front end (DFE). Refer to the Memory Map section, Register 0x2A3 (JTX_DL_204B_CONFIG0) for information on configuring the 8-bit/10-bit encoder.

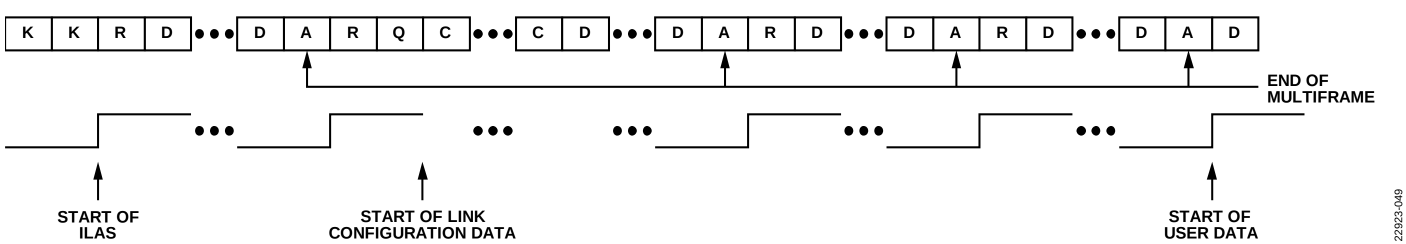

Figure 87. Initial Lane Alignment Sequence

Table 23. AD9083 Control Characters Used in JESD204B

Abbreviation	Control Symbol	8-Bit Value	10-Bit Value, RD[1] = −1	10-Bit Value, RD[1] = +1	Description
/R/	/K28.0/	000 11100	001111 0100	110000 1011	Start of multiframe
/A/	/K28.3/	011 11100	001111 0011	110000 1100	Lane alignment
/Q/	/K28.4/	100 11100	001111 0100	110000 1101	Start of link configuration data
/K/	/K28.5/	101 11100	001111 1010	110000 0101	Group synchronization
/F/	/K28.7/	111 11100	001111 1000	110000 0111	Frame alignment

[1] RD means running disparity.

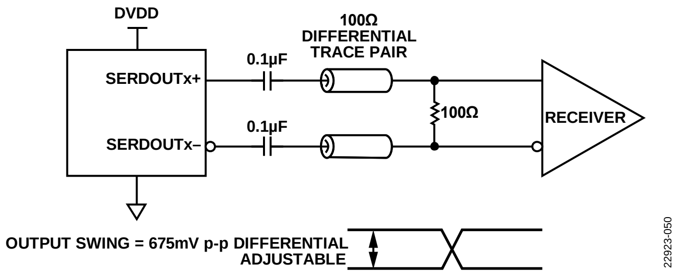

Figure 88. AC-Coupled Digital Output Termination Example

PHYSICAL LAYER (DRIVER) OUTPUTS

Digital Outputs, Timing, and Controls

The AD9083 physical layer consists of drivers that are defined in the JEDEC Standard JESD204B, July 2011. The differential digital outputs are powered up by default. The drivers use a dynamic 100 Ω internal termination to reduce unwanted reflections.

Place a 100 Ω differential termination resistor at each receiver input to result in a nominal 0.85 × DVDD V p-p swing at the receiver (see Figure 88). The swing is adjustable through the SPI registers. AC coupling is recommended to connect to the receiver. See the Memory Map section (Register 0x402 to Register 0x409) for more details.

The AD9083 digital outputs can interface with custom ASICs and field programmable gate array (FPGA) receivers, providing superior switching performance in noisy environments. Single point-to-point network topologies are recommended with a single differential 100 Ω termination resistor placed as close to the receiver inputs as possible.

If there is no far end receiver termination, or if there is poor differential trace routing, timing errors can result. To avoid such timing errors, it is recommended that the trace length be less than six inches, and that the differential output traces be close together and at equal lengths.

The format of the output data is twos complement by default. To change the output data format, see the Memory Map section Register 0x18A (OUT_FORMAT_SEL).

Deemphasis

Deemphasis enables the receiver eye diagram mask to be met in conditions where the interconnect insertion loss does not meet the JESD204B specification. Use the deemphasis feature only when the receiver is unable to recover the clock due to excessive insertion loss. Under normal conditions, it is disabled to conserve power. Additionally, enabling and setting too high a deemphasis value on a short link can cause the receiver eye diagram to fail. Use the deemphasis setting with caution because it can increase electromagnetic interference (EMI). See the Memory Map section (Register 0x413 to Register 0x422 in Memory Map) for more details.

JTX PLL

The JTX PLL generates the serializer clock (f_{LR}), which operates at the JESD204B lane rate. The status of the PLL lock can be checked in the PLL_STATUS register (Register 0x301), Bit 7 (JTX_PLL_LOCKED). This read only bit lets the user know if the PLL has achieved lock for the specific setup.

SETTING UP THE AD9083 DIGITAL INTERFACE

The AD9083 has one JESD204B link. The serial outputs (SERDOUT0± to SERDOUT3±) or lanes are considered to be part of one JESD204B link. The maximum lane rate allowed by the AD9083 is 16 Gbps.

The basic parameters that determine the link setup are

- AD9083 datapath (nonburst or burst mode)
- Number of converters per link (M).
- Number of lanes per link (L).
- N′ is the number of bits per sample (JESD204B word size), (AD9083 value = 12 or 16).

The lane line rate is related to the JESD204B parameters using the following equation:

$$Lane\ Rate = \frac{M \times N' \times \left(\frac{10}{8}\right) \times f_{OUT}}{L}$$

where:
$f_{OUT} = f_S/DECTOTAL$.
f_S is the ADC sample rate.
DECTOTAL is the total decimation rate of the signal processing tile.

Table 24 shows the JESD204B output configurations supported for the non-burst mode data path. Table 25 shows the JESD204B output configurations supported for burst mode data path. Take care to ensure that the serial line rate for a given configuration is within the supported range of 0.25 Gbps to 16 Gbps.

JESD204B TRANSPORT LAYER SETTINGS

See the JESD204B Overview section for details regarding the transport layer information listed in Table 24 and Table 25.

Table 24. JESD2048 Output Configuration in Nonburst Mode Data

No. of Virtual Converters Supported (Same Value as M)	JESD2048 Serial Lane Rate	CIC N	NCO/Mixer	Decimate by J	L	M	F	S	N'	K
8	160 × f_{OUT}	4	Bypassed	4, 8, 16	1	8	16	1	16	32
		8		4, 8, 16						
		16		1, 4, 8, 16						
	120 × f_{OUT}	4,	Bypassed	4, 8, 16	1	8	12	1	12	32
		8		4, 8, 16						
		16		1, 4, 8, 16						
	80 × f_{OUT}	4	Bypassed	4	2	8	8	1	16	32
		8		1						
		16		1						
	60 × f_{OUT}	4	Bypassed	4	2	8	6	1	12	32
		8		1						
		16		1						
	40 × f_{OUT}	4	Bypassed	1	4	8	4	1	16	32
		8		1						
	30 × f_{OUT}	4		1	4	8	3	1	12	32
		8		1						
16	320 × f_{OUT}	4	Bypassed	8, 12, 16, 20, 24, 30, 40, 60	1	16	32	1	16	32
		8		4, 8, 10, 12, 16, 20, 24, 30, 40, 60						
		16		4, 8, 10, 12, 16, 20, 24, 30, 40, 60						
		1		20, 40, 60						
	240 × f_{OUT}	4	Bypassed	10, 12, 20, 24, 30, 40, 60	1	16	24	1	12	32
		8		10, 12, 16, 20, 24, 30, 40, 60						
		16		8, 10, 12, 16, 20, 24, 30, 40, 60						
		1		16, 20, 40, 60						
	160 × f_{OUT}	4	Bypassed	4, 8,	2	16	16	1	16	32
		8		4						
		16		1						

No. of Virtual Converters Supported (Same Value as M)	JESD2048 Serial Lane Rate	CIC N	NCO/Mixer	Decimate by J	L	M	F	S	N'	K
		1		20						
	120 × f_{OUT}	1	Bypassed	16, 20	2	16	12	1	12	32
	80 × f_{OUT}	4	Bypassed	4	3	16	8	1	12	32
		8		1						
		16		1						
		1		8, 12, 16, 24						
	80 × f_{OUT}	4	Bypassed	4	4	16	8	1	16	32
		8		1						
		16		1						
		1		8, 12, 16, 24						
	60 × f_{OUT}	8	Bypassed	1	4	16	6	1	12	32
		1		4, 8, 12, 16, 24						
32	640 × f_{OUT}	4	Enabled	16	1	32	64	1	16	16
		8		8, 16						
		16		4, 8, 16,						
	480 × f_{OUT}	16	Enabled	16	1	32	48	1	12	16
	320 × f_{OUT}	4	Enabled	8, 16	2	32	32	1	16	32
		8		4, 8						
		16		4						
	160 × f_{OUT}	4	Enabled	4, 8, 16,	3	32	16	1	12	32
		8		4, 8, 16,						
		16		1, 4, 8, 16						
	160 × f_{OUT}	4	Enabled	4, 8	4	32	16	1	16	32
		8		4						
		16		1						
	120 × f_{OUT}	4	Enabled	4	4	32	12	1	12	32
		16		1						

Table 25. JESD2048 Output Configuration Burst Mode Datapath .

No. of Virtual Converters Supported (Same Value as M)	JESD2048 Lane Rate	CIC N	NCO/Mixer	Dec H	L	M	F	S	N′	K
32	640 × f_{OUT}	4	Enabled	24, 28, 32, 36	1	32	64	1	16	16
	640 × f_{OUT}	8	Enabled	12, 14, 16, 18	1	32	64	1	16	16
	480 × f_{OUT}	4	Enabled	24	1	32	48	1	12	16
	480 × f_{OUT}	8	Enabled	12, 16	1	32	48	1	12	16
64	640 × f_{OUT}	4	Enabled	24, 28, 32	2	64	64	1	16	16
	640 × f_{OUT}	8	Enabled	12, 14, 16	2	64	64	1	16	16
	480 × f_{OUT}	4	Enabled	24	2	64	48	1	12	16
	480 × f_{OUT}	8	Enabled	12	2	64	48	1	12	16
96	640 × f_{OUT}	4	Enabled	32, 36	3	96	64	1	16	16
	640 × f_{OUT}	8	Enabled	18	3	96	64	1	16	16
	480 × f_{OUT}	4	Enabled	24, 28, 32, 36	3	96	48	1	12	16
	480 × f_{OUT}	8	Enabled	14, 18	3	96	48	1	12	16
	480 × f_{OUT}	4	Enabled	24, 28	4	96	48	1	16	16
	480	8	Enabled	12, 14	4	96	48	1	16	16

DETERMINISTIC LATENCY

Both ends of the JESD204B link contain various clock domains distributed throughout each system. Data traversing from one clock domain to a different clock domain can lead to ambiguous delays in the JESD204B link. These ambiguities lead to non-repeatable latencies across the link from one power cycle or link reset to the next. The AD9083 supports JESD204B Subclass 0 and Subclass 1 operation. If deterministic latency is not a system requirement, Subclass 0 operation is recommended and the SYSREF signal may not be required. Even in Subclass 0 mode, the SYSREF signal can required in an application where multiple AD9083 devices must be synchronized with each other.

Subclass 0

If there is no requirement for multichip synchronization while operating in Subclass 0 mode, the SYSREF input can be left disconnected. In this mode, the relationship of the JESD204B clocks between the JESD204B transmitter and receiver are arbitrary but does not affect the ability of the receiver to capture and align the lanes within the link

Subclass 1

The JESD204B protocol organizes data samples into octets, frames, and multiframes, as described in the Transport Layer section of this data sheet. The LMFC is synchronous with the beginnings of these multiframes. In Subclass 1 operation, the SYSREF signal is used to synchronize the LMFCs for each device in a link or across multiple links (within the AD9083, SYSREF signal also synchronizes the internal sample dividers). The JESD204B receiver uses the multiframe boundaries and buffering to achieve consistent latency across lanes (or even multiple devices), and also to achieve a fixed latency between power cycles and link reset conditions. The AD9083 features sampled SYSREF modes for JESD204B Subclass 1 operation. See the Multichip Synchronization (MCS) section for details.

MULTICHIP SYNCHRONIZATION

The AD9083 has a JESD204B Subclass 1 compatible SYSREF input, which provides flexible options for synchronizing the internal blocks of the AD9083. The SYSREF input is a source synchronous system reference signal used to align the AD9083 LMFCs that enables multichip synchronization between multiple AD9083s. The input clock divider, the signal processing tile, signal monitor block, and JESD204B link can be synchronized using the SYSREF input.

SAMPLED SYSREF MODE

In sampled SYSREF mode, SYSREF operates as a standard JESD204B Subclass 1 signal.

The following are some characteristics of sampled SYSREF synchronization:

- Synchronous sampling of SYSREF.
- Must meet setup/hold time requirements for reliable synchronization. This is increasingly difficult to achieve as the sample rate increases.
- SYSREF jitter must be much less than one sample clock period. A SYSREF coming from an ASIC or an FPGA may have significant jitter.

SYSREF Related Functionality

The AD9083 supports resynchronization of internal clocks and NCOs, as well as across multiple AD9083 devices. The SYSREF and trigger signal inputs to the AD9083 are used to provide a synchronization triggering mechanism that supports

- Deterministic latency in JESD Subclass 1 mode.
- Multichip synchronization for NCO reset.

In resynchronization mode with the SYSREF_RESYNC_ MODE bit (Register 0x1C0, Bit 2 =1), the AD9083 aligns all internal clocks to the SYSREF signal (for Subclass 1 synchronization and deterministic latency). In the case of periodic SYSREF, after alignment is achieved, further periodic SYSREF inputs are automatically aligned to the internal clocks. A change in the SYSREF input phase initiates a re-alignment of the datapath clocks to the new SYSREF input phase.

The NCORESET_ALL_SYSREF bit field set to 0 (default) in Register 0x1C0, Bit 3 ensures that the NCOs only receive a reset pulse in response to a SYSREF pulse that has resynchronized the clocks. Program the NCOs to continuous synchronization mode by programming DDC_SYNC_NEXT = 0 and DDC_SYNC_EN = 1 in Register 0x1C4, Bits[1:0].

The DDCs are programmed to reset the NCOs in response to the periodic SYSREF pulse or the Nth SYSREF pulse received using Register 0x284 (JTX_TPL_SYSREF_N_SHOT).

Multichip Synchronization and NCO Reset Options

There are two aspects of multichip synchronization:

- Aligning the clocks across multiple devices.
- Aligning the NCOs across multiple devices.

Aligning Clocks Across Multiple Devices

Aligning the clocks across multiple devices is provided by the SYSREF signal in resynchronization mode. The SYSREF signal is used to align all the clocks in the AD9083. When SYSREF is deterministically sampled by multiple devices, it implies that the clocks are aligned across multiple devices.

Aligning NCOs Across Multiple Devices

NCO reset is handled by the reset of the NCO accumulators in the AD9083 signal processing tiles. To ensure that the NCOs are reset deterministically across devices, it is important to use resynchronization mode.

An external controller (for example, a clock generator chip) generates periodic SYSREF pulses or a one-shot SYSREF pulse to the SYSREF input.

Key Features and Notes Regarding Resynchronization Mode

In SYSREF resynchronization mode, all clocks shut down and restart in-phase to the SYSREF pulse.

The JESD LMFC aligns at a deterministic phase/delay from the SYSREF pulse.

The NCOs reset at a deterministic time after the SYSREF pulse is received. The NCO reset occurs after the datapath clocks are aligned to the new SYSREF.

The latency numbers, such as SYSREF LMFC delay, SYSREF to NCO reset delay, and so on, depend on the configuration used.

The latency of the NCO reset from SYSREF is constant for all periodic SYSREF pulses. If the SYSREF period is altered, a resynchronization followed by an NCO reset is triggered.

The SYSREF period for any mode must be a multiple of the multiframe clock period. Additional restriction may be required due to decimation modes.

An LMFC settling period of 8 LMFCs is expected for the internal LMFC to stabilize after a SYSREF input initiates realignment.

SERIAL PORT INTERFACE (SPI)

The AD9083 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the Serial Control Interface Standard (Rev. 1.0).

CONFIGURATION USING THE SPI

Three pins define the SPI of the AD9083 ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 26). The SCLK (serial clock) pin is used to synchronize the read and write data presented to and from the ADC. The SDIO (serial data input/ output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles. The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 2 and Table 14.

Other modes involving the CSB pin are available. The CSB pin can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB can stall high between bytes to allow additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued, which allows the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the Serial Control Interface Standard (Rev. 1.0).

HARDWARE INTERFACE

The pins described in Table 26 comprise the physical interface between the user programming device and the serial port of the AD9083. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9083 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

Table 26. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input that is used to synchronize serial interface, reads, and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that gates the read and write cycles.

PROGRAMMING GUIDE

The AD9083 is highly reconfigurable and programmable via the SPI interface.

The AD9083 product page contains instructions in the Software and Systems Requirements section to request device application programming interface (API) C code drivers. These drivers are reference code that allows the user to quickly configure the AD90803 using high level function calls, known as application APIs. Analog Devices provides the full source code for these high level function calls.

PROGRAMMING SEQUENCE

When powered on, the various blocks inside AD9083 power up in a disabled state. To set up the AD9083 in a specific mode, a set of SPI operations are required. Before beginning the full programming of the device, ensure that the following sequence is completed:

1. Ramp up the supplies. There is no requirement for any power supply sequencing. The POR circuitry holds the AD9083 in reset until all the supplies reach the correct threshold.
2. Issue a soft reset through SPI Register 0x000 = 81h, or by toggling the RSTB pin.
3. Delay = minimum 200 µs. Otherwise, wait for POR circuit to deassert. The PORB_STAT register (Register 0x0020) can be read back to verify the state of the PORb signals. Register 0x0020 = 7Fh means the AD9083 is ready to be programmed and the power supplies are at the optimal level.
4. Configure any supporting circuitry to the AD9083. For example, set up any necessary clock components so that the reference clock to the AD9083 on-chip PLL is stable before beginning to set up the AD9083.
5. Configure any necessary setup for the FPGA in the system to receive the JESD204B data after the AD9083 is fully configured.

After the platform and system-dependent setup is complete and stable, the AD9083 can be programmed to a desired configuration. To simplify the programming details needed to configure the AD9083, a short list of high level API function calls are provided. These high level API calls completely configure the device in any desired supported state. The programming sequence for proper AD9083 setup is shown in Table 27.

Table 27. Programming Sequence to Set Up the AD9083

Step No.	API Function	Input Parameters	Description
1	adi_ad9083_device_reset()	&ad9083_dev: (device structure pointer) ad9083_soft_reset	Performs a soft reset of the AD9083.
2	adi_ad9083_device_init()	&ad9083_dev: (device structure pointer)	Prints the API revision, retrieves the host CPU endian mode, retrieves the host CPU type, configures the SPI mode, executes a SPI read/write test, and checks the power status.
3	adi_ad9083_device_ clock_config_set()	&ad9083_dev: (device structure pointer) adc_clk_hz: ADC Sample Rate ref_clk_hz: PLL Reference Clock	Configures the on-chip PLL with the correct settings based on the user input of the desired ADC sample rate and the PLL reference clock that is provided to the CLK± pins.
4	adi_ad9083_rx_ adc_config_set()	&ad9083_dev (device structure pointer) fc: -3dB LPF cutoff frequency vmax: differential peak-to-peak input full-scale rterm: termination resistance en_hp: enable high performance mode backoff: dB backoff in terms of noise (dB value × 100) finmax: maximum input frequency, should be set to fADC/20	Configures the VCO ADC settings according to the desired input settings for each parameter.

Step No.	API Function	Input Parameters	Description
5	adi_ad9083_rx_ datapath_config_set()	&ad9083_dev: (device structure pointer) mode: determines datapath flow, refer to enumeration adi_ad9083_datapath_mode_e for exact details dec: array of decimation value choices including CIC decimation, J decimation, G averaging value and H decimation nco_freq_hz: NCO shift frequency desired	Configures the digital datapath of the ADC based on the desired signal path flow (determined by the mode input parameter), the decimation rates chosen, and the NCO frequency shift (if used). The valid adi_ad9083_datapath_ mode_e enumeration values are as follows: AD9083_DATAPATH_ADC_CIC: ADC → CIC → JESD204B Output AD9083_DATAPATH_ADC_CIC_NCO_J: ADC → CIC → NCO → J Decimation → JESD204B Output AD9083_DATAPATH_ADC_CIC_J: ADC → CIC → NCO → J Decimation → JESD204B Output AD9083_DATAPATH_ADC_J: ADC → J Decimation → JESD204B Output AD9083_DATAPATH_ADC_CIC_NCO_G: ADC → CIC → NCO → G average samples → JESD204B Output AD9083_DATAPATH_ADC_CIC_NCO_G_H: ADC → CIC → NCO → G average samples → H Decimation → JESD204B Output
6	adi_ad9083_jtx_startup()	&ad9083_dev: (device structure pointer) &jtx_param: pointer to array of JESD204B parameter settings for desired mode operation	Configures the JESD204B interface with the SERDES parameters for the desired configuration. Array inputs are: {L, F, M, S, HD, K, N, NP, CF, CS, DID, BID, LID, SC, SCR}, where SC = subclass

These API function calls are all that are needed to set up the device. All lower level SPI writes are handled by the API function calls underneath these high level calls and are abstracted to make configuration easier for the user. More detailed information about each of these API function calls and the lower level SPI configuration included in the source code can be found in the AD9083 API specification document, which is provided with the API source code. This source code package can be requested through the instructions provided at the AD9083 product page.

Example 1: Wide Bandwidth Real Output Mode

After powering up the device, execute the API sequence according to the target application requirements listed in this section. This sequence configures the AD9083 to operate in wide bandwidth mode without frequency translation in the datapath. The total power consumption in this mode is about 1.42 W. This is the mode of operation used to measure the data sheet parameters listed in the specification tables. (see Table 1).

- Sample rate = 2 GSPS.
- On-chip PLL reference = 250 MHz.
- f_{INMAX} = 100 MHz (sample rate/20).
- Low pass filter cut-off frequency (f_C) = 800 MHz.
- V_{MAX} = 2.0 V.
- R_{TERM} = 100 Ω.
- EN_HP = 0.
- Backoff = 0 dB.
- Mixer bypassed (real data).
- CIC decimator bypassed.
- Decimate by J = 8.
- Output bandwidth = 100 MHz.
- Transport parameters L, M, F, S, N’, K = 4, 16, 6, 1, 12, 32.
- Each lane = 15 Gbps.

The following API sequence with specific input parameters is needed to fully configure the device in the wide bandwidth mode of operation:

```
// Define device structure and instantiate
adi_ad9083_device_t ad9083_dev;

// Perform soft reset
adi_ad9083_device_reset(&ad9083_dev, 0);
// Get API revision, CPU info etc
adi_ad9083_device_init(&ad9083_dev);

// Set up clocking configuration, lock on-chip PLL
//ADC Sample Rate = 2GSPS (adc_clk_hz in units of Hz)
//PLL Reference Clock = 250MHz (ref_clk_hz in units of Hz)
adi_ad9083_device_clock_config_set(&ad9083_dev, adc_clk_hz = 2000000000, ref_clk_hz =
250000000);

// Setup VCO ADC settings
//LPF bandwidth Fc = 800MHz (fc in units of Hz), Vmax = 2.0V (vmax in mV units)
//Rterm = 100 ohm (rterm bitfield = 2 for 100 ohm), Enhp = 0
//Backoff = 0dB (backoff in terms of noise, dB * 100)
//Finmax = 100MHz (finmax in units of Hz)
adi_ad9083_adc_term_res_e rterm = AD9083_ADC_TERM_RES_100; // (enum value = 2)
adi_ad9083_rx_adc_config_set(&ad9083_dev, fc = 800000000, vmax = 2000, rterm = term, en_hp
= 0, backoff = 0, finmax = 100000000);

// Setup Datapath
//Datapath: ADC -> J -> JESD204B output
//Decimation: CIC bypassed (/1), J Decimation = 8, G value bypassed, H value bypassed
//NCO frequency shifts: NCO0, NCO1 & NCO2 bypassed
adi_ad9083_datapath_mode_e datapath_mode = AD9083_DATAPATH_ADC_J;
uint8_t dec[] = {0, AD9083_J_DEC_8, 0, 0};
uint64_t nco_freq_hz = { 0, 0, 0};
adi_ad9083_rx_datapath_config_set(&ad9083_dev, datapath_mode, dec, nco_freq_hz);
```

```
// Setup JESD204B
// L, M, F, S, N', K = 4,16,6,1,12,32
adi_cms_jesd_param_t jtx_param[] =
   /*L   F   M   S   HD   K    N   '   CF  CS  DID  BID  LID  SC  SCR */
    { 4, 6, 16,  1,   1,  32,  12,  12,   0,  0,  0,   0,   0,   0,  1 };
adi_ad9083_jtx_startup(&ad9083_dev, &jtx_param);
```

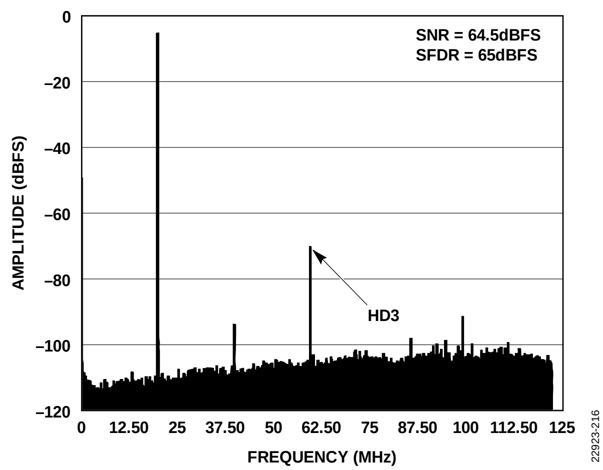

Figure 89. FFT Wide Bandwidth Real Output Mode

Table 28. Power Consumption Wide Bandwidth

Domain	Voltage (V)	Current (A)	Power (W)
AVDD	1	0.397	0.397
AVDD1P8	1.8	0.096	0.1728
DVDD	1	0.774	0.774
DVDD1P8	1.8	0.041	0.0738
		Total	1.4176
Power per Channel (W)			0.089

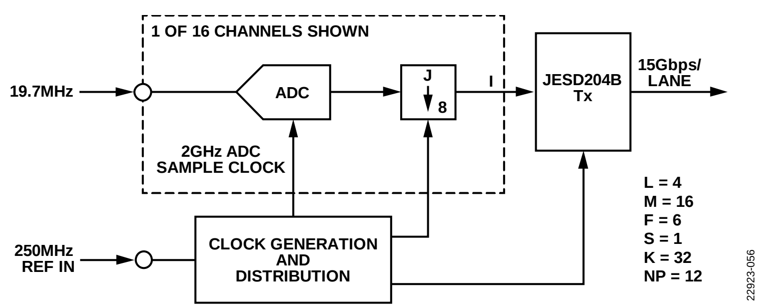

Figure 90. Wide Bandwidth Real Output Mode Block Diagram, See Table 1

Example 2 : Narrow Bandwidth Complex Output Mode

After powering up the device, execute the API sequence according to the target application requirements listed in this section. This sequence configures the AD9083 to operate in narrow bandwidth mode using frequency translation in the datapath. The total power consumption in this mode is about1.17 W.

- Sample rate = 2 GSPS.
- On-chip PLL reference = 250 MHz.
- f_{INMAX} = 100 MHz (sample rate/20).
- f_C = 800 MHz.
- V_{MAX} = 2.0 V.
- R_{TERM} = 100 Ω.
- EN_HP = 0
- Backoff = 0
- NCO_0/mixer (complex data), FTW = 70.3125 MHz.
- CIC decimator = 4.
- Decimate by J = 16.
- Output bandwidth = ±12.7187 MHz.
- Transport parameters L, M, F, S, N', K = 2, 32, 32, 1, 16, 32.
- Each lane = 10 Gbps.

The following API sequence with specific input parameters is needed to fully configure the part in the wide bandwidth mode of operation:

```
// Define device structure and instantiate
adi_ad9083_device_t ad9083_dev;

// Perform soft reset
adi_ad9083_device_reset(&ad9083_dev, 0);
// Get API revision, CPU info etc
adi_ad9083_device_init(&ad9083_dev);

// Set up clocking configuration, lock on-chip PLL
//ADC Sample Rate = 2GSPS (adc_clk_hz in units of Hz)
//PLL Reference Clock = 250MHz (ref_clk_hz in units of Hz)
adi_ad9083_device_clock_config_set(&ad9083_dev, adc_clk_hz = 2000000000, ref_clk_hz =
250000000);

// Setup VCO ADC settings
//LPF bandwidth Fc = 800MHz (fc in units of Hz), Vmax = 2.0V (vmax in mV units)
//Rterm = 100 ohm (rterm bitfield = 2 for 100 ohm), Enhp = 0
//Backoff = 0dB (backoff in terms of noise, dB * 100)
//Finmax = 100MHz (finmax in units of Hz)
adi_ad9083_adc_term_res_e rterm = AD9083_ADC_TERM_RES_100; // (enum value = 2)
adi_ad9083_rx_adc_config_set(&ad9083_dev, fc = 800000000, vmax = 2000, rterm = term, en_hp
= 0, backoff = 0, finmax = 100000000);

// Setup Datapath
//Datapath: ADC -> CIC -> NCO -> J -> JESD204B output
//Decimation: CIC =4, J Decimation = 16, G value bypassed, H value bypassed
//NCO frequency shifts: NCO0 = 70.3125MHz, NCO1 & NCO2 bypassed
adi_ad9083_datapath_mode_e datapath_mode = AD9083_DATAPATH_ADC_CIC_NCO_J;
uint8_t dec[] = {AD9083_CIC_DEC_4, AD9083_J_DEC_16, 0, 0};
uint64_t nco_freq_hz = { 70312500, 0, 0};
adi_ad9083_rx_datapath_config_set(&ad9083_dev, datapath_mode, dec, nco_freq_hz);
```

```
// Setup JESD204B
// L, M, F, S, N’, K = 2,32,32,1,16,32
adi_cms_jesd_param_t jtx_param[] =
   /*L   F   M   S   HD   K    N   '   CF  CS  DID  BID  LID  SC  SCR */
    { 2, 32, 32,  1,   1, 32,  16,  16,   0,  0,  0,   0,   0,   0,  1 };
adi_ad9083_jtx_startup(&ad9083_dev, &jtx_param);
```

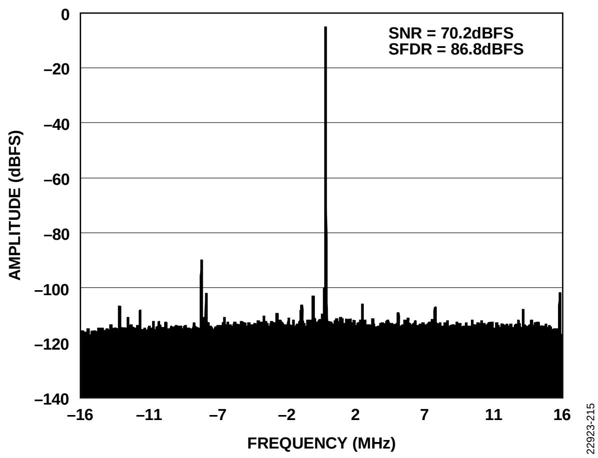

Figure 91. FFT Narrow Bandwidth Complex Output Mode

Table 29. Power Consumption Narrow Bandwidth

Domain	Voltage (V)	Current (A)	Power (W)
AVDD	1	0.396	0.396
AVDD1P8	1.8	0.096	0.1728
DVDD	1	0.532	0.532
DVDD1P8	1.8	0.041	0.0738
		Total	1.1746
Power per Channel (W)			0.073

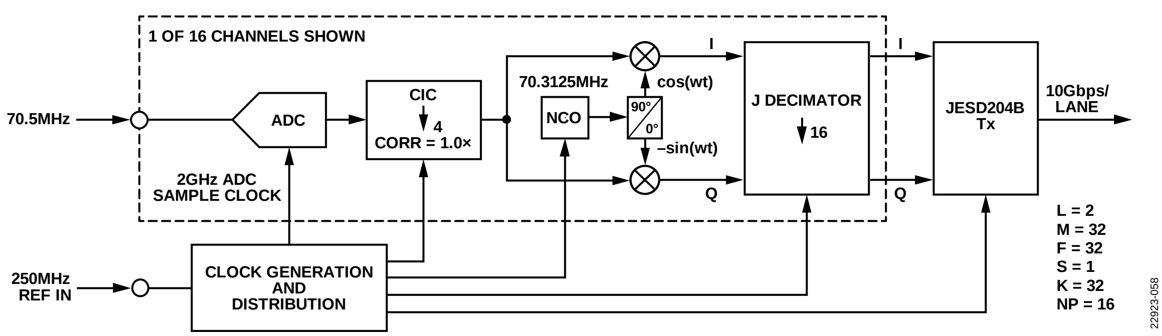

Figure 92. Narrow Bandwidth Complex Output Mode Block Diagram

MEMORY MAP

All address locations that are not included in the memory map are not currently supported for this device and must not be written.

LOGIC LEVELS

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."
- X denotes a don't care bit.

MEMORY MAP REGISTER DETAILS

Table 30. AD9083 Memory Map Register Details

Addr.	Name	Bits	Bit Name	Description	Reset	Access
Analog Devices SPI Registers						
0x000	SPI_INTERFACE_ CONFIG_A	7	SOFT_RESET_7	Initiates a Reset Equivalent to a Hard Reset. Whenever a soft reset is issued, the user must wait at least 200 μs before writing to any other register, to provide sufficient time for the device reset to complete. 0: Do nothing. 1: Reset the SPI and registers (self clearing).	0x0	R/W
		6	LSB_FIRST_6	LSB/MSB Bit Shift First. 1: Least significant bit shifted first for all SPI operations. 0: Most significant bit shifted first for all SPI operations.	0x0	R/W
		5	ADDR_ASCENSION_5	Multibyte SPI Operations Address Increment. 0: Multibyte SPI operations cause addresses to auto-decrement. 1: Multibyte SPI operations cause addresses to auto-increment.	0x0	R/W
		[4:3]	RESERVED	Reserved.	0x0	R/W
		2	ADDR_ASCENSION_2	Mirror of 0x000[5]. 0: Multibyte SPI operations cause addresses to auto-decrement. 1: Multibyte SPI operations cause addresses to auto-increment.	0x0	R/W
		1	LSB_FIRST_1	Mirror of 0x000[6]. 1: Least significant bit shifted first for all SPI operations. 0: Most significant bit shifted first for all SPI operations.	0x0	R/W
		0	SOFT_RESET_0	Mirror of 0x000[7]. 0: Do nothing. 1: Reset the SPI and registers (self clearing).	0x0	R/W
0x01	SPI_INTERFACE_ CONFIG_B	7	SINGLE_INSTRUCTION	SPI Streaming Mode. 0: Streaming is enabled. 1: Streaming is disabled. Only one read or write operation is performed regardless of the state of the CSB line.	0x0	R/W
		[6:0]	RESERVED	Reserved.	0x0	R/W
0x02	DEVICE_CONFIG	[7:2]	RESERVED	Reserved.	0x0	R
		[1:0]	OP_MODE	Operating Mode. 00: Normal Operation. 01: Normal Operation with Reduced Power. 10: Standby. 11: Sleep.	0x0	R/W
0x03	CHIP_TYPE	[7:0]	CHIP_TYPE	High Speed ADCs.	0x3	R
0x04	PROD_ID_LSB	[7:0]	PROD_ID[7:0]	Chip ID. AD9083	0xEA	R
0x05	PROD_ID_MSB	[7:0]	PROD_ID[15:8]	Chip ID. AD9083	0x0	R
0x06	CHIP_GRADE	[7:4]	CHIP_SPEED_GRADE	Chip Speed Grade.	0x0	R
		[3:0]	RESERVED	Reserved.	0x0	R
0x08	DEVICE_INDEX1	[7:0]	DEV_INDEX1	Offset Pointer or LSB of the Device Index Register.	0x0	R/W
0x09	DEVICE_INDEX2	[7:0]	DEV_INDEX2	Offset Pointer or LSB of the Device Index Register.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x0A	CHIP_SCRATCH	[7:0]	CHIP_SCRATCH	Chip Scratchpad Register. This register is used to provide a consistent memory location for software debug.	0x0	R/W
0x0C	VENDOR_ID_LSB	[7:0]	CHIP_VENDOR_ID[7:0]	Vendor ID.	0x56	R
0x0D	VENDOR_ID_MSB	[7:0]	CHIP_VENDOR_ID[15:8]	Vendor ID.	0x4	R
0x20	PORB_STAT	7	RESERVED	Reserved.	0x0	R
		6	PORB_VDDSYNTH_JTX_PLL_1P0	PORb Status of JESD PLL 1.0 V V_{DD}.	0x0	R
		5	PORB_VDDPHY_SER_1P0	PORb Status of JESD SER PHY 1.0 V V_{DD}.	0x0	R
		4	PORB_VDDLDO_JTX_PLL_1P8	PORb Status of JESD PLL (LDO) 1.8 V V_{DD}.	0x0	R
		3	PORB_VDDCP_JTX_PLL_1P0	PORb Status of JESD PLL 1.0 V V_{DD}.	0x0	R
		2	PORB_VDD_SYNCRX_1P8	PORb Status for SYNCRX I/O V_{DD} 1.8V.	0x0	R
		1	PORB_VDD_DIG_1P0	PORb Status of Digital 1.0 V V_{DD} and Digital I/O 1.8 V V_{DD}.	0x0	R
		0	PORB_VDD_ANA	Status of V_{DD} Domains in ADC, CLKTOP, on-chip PLL, and TOPREF.	0x0	R
0x21	PORB_MASK_RESET	[7:1]	RESERVED	Reserved.	0x0	R
		0	PORB_IGNORE	Controls Whether or Not to Gate Internal Resets with PORb.	0x0	R/W
0x24	BLOCK_RESET	[7:6]	RESERVED	Reserved.	0x0	R
		5	DIG_DP_JTX_RESET	Resets the DIG Datapath and JTX. 1: Assert Reset. 0: De-Assert Reset	0x0	R/W
		4	JTX_PLL_RESET	Reset the JTX_PLL. 1: Assert Reset. 0: De-Assert Reset.	0x0	R/W
		3	JTXPHY_RESET	Reset the SER PHY. 1: Assert Reset. 0: De-Assert Reset.	0x0	R/W
		2	TOPREF_RESET	Reset the TOP REF. 1: Assert Reset. 0: De-Assert Reset.	0x0	R/W
		1	CLKTOP_RESET	Reset the CLK TOP. 1: Assert Reset. 0: De-Assert Reset.	0x0	R/W
		0	ADC_RESET	Reset the ADCs. 1: Assert Reset. 0: De-Assert Reset.	0x0	R/W
0x30	LOW_PWR_PIN_CTRL	[7:6]	RESERVED	Reserved.	0x0	R
		5	JTXPHY_PIN_CTRL	For JTXPHY. 1: PD Pin and MASK Bit Control 0: CONFIG Bit Programming Control	0x0	R/W
		4	JTX_PIN_CTRL	For JTX. 1: PD Pin and MASK Bit Control 0: CONFIG Bit Programming Control	0x0	R/W
		3	DIG_DP_PIN_CTRL	For DIG DP. 1: PD Pin and MASK Bit Control 0: CONFIG Bit Programming Control	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
		2	TOPREF_PIN_CTRL	For TOP REF. 1: PD Pin and MASK Bit Control 0: CONFIG Bit Programming Control	0x0	R/W
		1	CLKTOP_PIN_CTRL	Power Down for CLKTOP. 1: PD Pin and MASK Bit Control 0: CONFIG Bit Programming Control	0x0	R/W
		0	ADC_PIN_CTRL	For All 16 ADCs. 1: PD Pin and MASK Bit Control 0: CONFIG Bit Programming Control	0x0	R/W
0x31	LOW_PWR_PIN_ POLARITY	[7:2]	RESERVED	Reserved.	0x0	R
		[1:0]	POL	Polarity of PD Pin. 0: Active High. 1: Active Low.	0x0	R/W
0x32	LOW_PWR_CONFIG	[7:6]	RESERVED	Reserved.	0x0	R
		5	JTXPHY_LP_MODE	Low Power Mode for JTXPHY. 0 : Normal Mode. 1 : Low Power Mode.	0x0	R/W
		4	JTX_LP_MODE	Low Power Mode for JTX. 0: Normal Mode 1: Low Power Mode	0x0	R/W
		3	DIG_DP_LP_MODE	Low Power Mode for Digital Datapath. 0: Normal Mode 1: Low Power Mode	0x0	R/W
		2	TOPREF_LP_MODE	Low Power Mode for Top Ref. If 1 then bias currents to on-chip PLL, ADC, clock buffer and monitor mux from master bias are disabled. BG is still active. 0: Normal Mode 1: Low Power Mode	0x0	R/W
		1	CLKTOP_LP_MODE	Low Power Mode for Clock Top. 0: Normal Mode 1: Low Power Mode	0x0	R/W
		0	ADC_LP_MODE	Low Power Mode for All 16 ADCs. 0: Normal Mode 1: Low Power Mode	0x0	R/W
0x33	LOW_PWR_PIN_MASK	[7:6]	RESERVED	Reserved.	0x0	R
		5	JTXPHY_LP_PIN_MASK	Mask the PD to JTXPHY. 0: Mask 1: Unmask	0x0	R/W
		4	JTX_LP_PIN_MASK	Mask the PD to JTX. 0: Mask 1: Unmask	0x0	R/W
		3	DIG_DP_LP_PIN_MASK	Mask the PD to DIG_DP. 0: Mask 1: Unmask	0x0	R/W
		2	TOPREF_LP_PIN_MASK	Mask the PD to TOP REF. 0: Mask 1: Unmask	0x0	R/W
		1	CLKTOP_LP_PIN_MASK	Mask the PD to CLKTOP. 0: Mask 1: Unmask	0x0	R/W
		0	ADC_LP_PIN_MASK	Mask the PD to ADC 0: Mask 1: Unmask.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
Digital Datapath Setup Registers						
0x100	NCO0_CONTROL	[7:1]	RESERVED	Reserved.	0x0	R
		0	ADITHER_EN0	Amplitude Dither Enable for NCO0. 1: Enables amplitude dither. 0: Disables amplitude dither.	0x1	R/W
0x105	NCO0_FTW	7	RESERVED	Reserved.	0x0	R
		[6:0]	NCO0_FTW	NCO Frequency Tuning Word for NCO0. Specifies the frequency tuning word for NCO0. Only Bits[6:0] are valid.	0x0	R/W
0x106	NCO0_PHOFF	7	RESERVED	Reserved.	0x0	R
		[6:0]	NCO0_PHOFF	NCO Phase Offset for NCO0. Specifies the phase offset for NCO0. Only Bits[6:0] are valid	0x0	R/W
0x107	NCO1_CONTROL	[7:1]	RESERVED	Reserved.	0x0	R
		0	ADITHER_EN1	Amplitude Dither Enable for NCO1. 1: Enables amplitude dither. 0: Disables amplitude dither.	0x1	R/W
0x10C	NCO1_FTW	7	RESERVED	Reserved.	0x0	R
		[6:0]	NCO1_FTW	NCO Frequency Tuning Word for NCO1. Specifies the frequency tuning word for NCO0. Only Bits[6:0] are valid	0x0	R/W
0x10D	NCO1_PHOFF	7	RESERVED	Reserved.	0x0	R
		[6:0]	NCO1_PHOFF	NCO Phase Offset for NCO1. Specifies the phase offset for NCO0. Only Bits[6:0] are valid	0x0	R/W
0x10E	NCO2_CONTROL	[7:1]	RESERVED	Reserved.	0x0	R
		0	ADITHER_EN2	Amplitude Dither Enable for NCO2. 1: Enables amplitude dither. 0: Disables amplitude dither.	0x1	R/W
0x113	NCO2_FTW	7	RESERVED	Reserved.	0x0	R
		[6:0]	NCO2_FTW	NCO Frequency Tuning Word for NCO2. Specifies the frequency tuning word for NCO0. Only Bits[6:0] are valid	0x0	R/W
0x114	NCO2_PHOFF	7	RESERVED	Reserved.	0x0	R
		[6:0]	NCO2_PHOFF	NCO Phase Offset for NCO2. Specifies the phase offset for NCO0. Only Bits[6:0] are valid	0x0	R/W
0x115	MIXER_CTRL	[7:2]	RESERVED	Reserved.	0x0	R
		[1:0]	MIXER_MODE	Mixer Mode. 00: Normal Mode: Output is input multiplied by NCO data. 01: NCO Bypass Mode: Output is same as input. 10: Reserved. 11: NCO Test Mode : Output is constant times NCO Data.	0x0	R/W
0x116	DP_CTRL	7	RESERVED	Reserved.	0x0	R
		[6:5]	NUM_TONES	Number of Tones. Defines number of Tones per ADC in Burst mode. This field is valid only for BURST_MODE = 1 case. 00: Invalid. 01: 1 Tone. 10: 2 Tone. 11: 3 Tones.	0x3	R/W
		4	DECI_ADC_DATA	ADC Output as input to J decimator. 1: ADC output to J decimator. 0: CIC output to J decimator.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
		3	NCO_6DB_GAIN	Enable Gain 6 db. 1: Enables the 6 dB gain when NCO is used in datapath 0: Disables 6 dB gain for all modes	0x0	R/W
		2	BURST_MODE	Burst Mode. 1: Burst mode is selected. Selects the G/H path. 0: Non-burst Mode. Selects the Decimate by J path.	0x1	R/W
		1	NO_DDC_MODE	NCO Bypass. Note that this bit is valid only for non-burst mode. 1: Bypasses the NCO/MIXER(Real Data). 0: NCO/MIXER Enabled.	0x0	R/W
		0	DATAPATH_EN	Datapath Enable. 1: Enables all the 16 datapaths. 0: Disables all the 16 datapaths.	0x0	R/W
0x117	CIC_CTRL	[7:3]	RESERVED	Reserved.	0x0	R
		2	CIC_ACC_CLR	CIC Accumulator Clear. 1: Clears the CIC accumulators in all the 16 datapaths 0: No Action	0x0	R/W
		[1:0]	CIC_DEC_RATE	CIC Decimation Rate. 00-Decimate by 4 01: Decimate by 8 10: Decimate by 16 This is common for all the 16 datapaths 00: Decimate by 4. 01: Decimate by 8. 10: Decimate by 16.	0x0	R/W
0x118	DECIMATE_H	[7:0]	H_VALUE	"H" Value. Specifies the "H" value for decimation in burst mode. (G/H) Eg: 'h04 ==> Decimate by 4 000001: 1. 001100: 12. 001110: 14. 010000: 16. 010010: 18. 011000: 24. 011100: 28. 100000: 32. 100100: 36.	0x10	R/W
0x119	DECIMATE_G	[7:0]	G_VALUE	"G" Value. Specifies the "G" value in burst mode. (G/H) It is for these many samples averaging has to be done. 00000: N/A. 01000: 8. 10000: 16.	0x8	R/W
0x11A	DECIMATE_J	[7:4]	RESERVED	Reserved.	0x0	R
		[3:0]	DEC_J	Bits for J Decimator. 0000: Bypass (No Decimation). 0001: Decimate by 4. 0010: Decimate by 8. 0011: Decimate by 16. 0100: Not Valid. 0101: Not Valid. 0110: Decimate by 12.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
				0111: Decimate by 24. 1000: Not Valid. 1001: Decimate By 10 (Valid only for CIC Data Not valid for Decimation of ADC Data). 1010: Decimate by 20. 1011: Decimate by 40. 1100: Not Valid. 1101: Not Valid. 1110: Not Valid. 1111: Decimate by 60.		
0x11B	DECIMATE_H_EFF	[7:0]	H_EFF_VALUE	"H_EFF" Value. Specifies the "H" value for decimation in burst mode. (G/H) Eg: 'h04 ==> Decimate by 4	0x10	R
0x152	CIC_GAIN_ADJ_VALUE_0	[7:0]	CIC_GAIN_ADJ_VAL_0[7:0]	CIC Gain Adj 0. integer-4. fraction-10	0x7	R/W
0x153	CIC_GAIN_ADJ_VALUE_1	[7:2]	RESERVED	Reserved.	0x0	R
		[1:0]	CIC_GAIN_ADJ_VAL_0[9:8]	CIC Gain Adj 0. integer-4. fraction-10	0x0	R/W
0x154	CIC_GAIN_ADJ_VALUE_2	[7:4]	RESERVED	Reserved.	0x0	R
		[3:0]	CIC_GAIN_ADJ_VAL_0[13:10]	CIC Gain Adj 0. integer-4. fraction-10	0x1	R/W
0x155	CIC_GAIN_ADJ_VALUE_3	[7:0]	CIC_GAIN_ADJ_VAL_1[7:0]	CIC Gain Adj 1. integer-4. fraction-10	0x20	R/W
0x156	CIC_GAIN_ADJ_VALUE_4	[7:2]	RESERVED	Reserved.	0x0	R
		[1:0]	CIC_GAIN_ADJ_VAL_1[9:8]	CIC Gain Adj 1. integer-4. fraction-10	0x0	R/W
0x157	CIC_GAIN_ADJ_VALUE_5	[7:4]	RESERVED	Reserved.	0x0	R
		[3:0]	CIC_GAIN_ADJ_VAL_1[13:10]	CIC Gain Adj 1. integer-4. fraction-10	0x1	R/W
0x158	CIC_GAIN_ADJ_VALUE_6	[7:0]	CIC_GAIN_ADJ_VAL_2[7:0]	CIC Gain Adj 2. integer-4. fraction-10	0x4A	R/W
0x159	CIC_GAIN_ADJ_VALUE_7	[7:2]	RESERVED	Reserved.	0x0	R
		[1:0]	CIC_GAIN_ADJ_VAL_2[9:8]	CIC Gain Adj 2. integer-4. fraction-10	0x0	R/W
0x170	CIC_GAIN_ADJ_VALUE_8	[7:4]	RESERVED	Reserved.	0x0	R
		[3:0]	CIC_GAIN_ADJ_VAL_2[13:10]	CIC Gain Adj 2. integer-4. fraction-10	0x1	R/W
0x189	OUT_RES	[7:6]	RESERVED	Reserved.	0x0	R
		5	DFORMAT_DDC_DITHER_EN	0: Disable 1: Enable	0x0	R/W
		4	RESERVED	Reserved.	0x0	R/W
		[3:0]	DFORMAT_RES	Data Output Resolution. 0000: 16-bit resolution. 0001: 15-bit resolution. 0010: 14-bit resolution. 0011: 13-bit resolution. 0100: 12-bit resolution. 0101: 11-bit resolution. 0110: 10-bit resolution. 0111: 9-bit resolution. 1000: 8-bit resolution.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x18A	OUT_FORMAT_SEL	[7:3]	RESERVED	Reserved.	0x0	R
		2	DFORMAT_INV	Output Data Inversion Enable. Digital ADC Sample Invert 0: ADC sample data is NOT inverted 1: ADC sample data is inverted	0x0	R/W
		[1:0]	DFORMAT_SEL	Output Data Format Selection. 00: 2'Complement. 01: Offset Binary. 10: Gray Code.	0x0	R/W
0x18B	CTRL_0_1_SEL	[7:4]	DFORMAT_CTRL_BIT_1_SEL	Control Bit 1 Mux Selection. 00: Overrange Bit. 01: SYSREF.	0x0	R/W
		[3:0]	DFORMAT_CTRL_BIT_0_SEL	Control Bit 0 Mux Selection. 00: Overrange Bit. 01: SYSREF.	0x0	R/W
0x18C	CTRL_2_SEL	[7:4]	RESERVED	Reserved.	0x0	R
		[3:0]	DFORMAT_CTRL_BIT_2_SEL	Control Bit 2 Mux Selection. 00: Overrange Bit. 01: SYSREF.	0x0	R/W
0x18D	OVR_CLR_0	[7:0]	DFORMAT_OVR_CLR[7:0]	Overrange Status Clear. Converter overrange clear bit (active high). After an overrange sticky bit is set, it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLR bit. The DFORMAT_OVR_CLEAR[95:0] bits must be cleared for further overrange to be reported . [0] = Overrange sticky bit clear for Converter 0 [1] = Overrange sticky bit clear for Converter 1 [2] = Overrange sticky bit clear for Converter 2 and so on.	0x0	R/W
0x18E	OVR_CLR_1	[7:0]	DFORMAT_OVR_CLR[15:8]	Overrange Status Clear. Converter overrange clear bit (active high). After an overrange sticky bit is set, it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLR bit. The DFORMAT_OVR_CLEAR[95:0] bits must be cleared for further overrange to be reported . [0] = Overrange sticky bit clear for Converter 0 [1] = Overrange sticky bit clear for Converter 1 [2] = Overrange sticky bit clear for Converter 2 and so on.	0x0	R/W
0x18F	OVR_CLR_2	[7:0]	DFORMAT_OVR_CLR[23:16]	Overrange Status Clear. Converter overrange clear bit (active high). After an overrange sticky bit is set, it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLR bit. The DFORMAT_OVR_CLEAR[95:0] bits must be cleared for further overrange to be reported . [0] = Overrange sticky bit clear for Converter 0 [1] = Overrange sticky bit clear for Converter 1 [2] = Overrange sticky bit clear for Converter 2 and so on.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x190	OVR_CLR_3	[7:0]	DFORMAT_OVR_CLR[31:24]	Overrange Status Clear. Converter overrange clear bit (active high). After an overrange sticky bit is set, it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLR bit. The DFORMAT_OVR_CLEAR[95:0] bits must be cleared for further overrange to be reported . [0] = Overrange sticky bit clear for Converter 0 [1] = Overrange sticky bit clear for Converter 1 [2] = Overrange sticky bit clear for Converter 2 and so on.	0x0	R/W
0x191	OVR_CLR_4	[7:0]	DFORMAT_OVR_CLR[39:32]	Overrange Status Clear. Converter overrange clear bit (active high). After an overrange sticky bit is set, it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLR bit. The DFORMAT_OVR_CLEAR[95:0] bits must be cleared for further overrange to be reported . [0] = Overrange sticky bit clear for Converter 0 [1] = Overrange sticky bit clear for Converter 1 [2] = Overrange sticky bit clear for Converter 2 and so on.	0x0	R/W
0x192	OVR_CLR_5	[7:0]	DFORMAT_OVR_CLR[47:40]	Overrange Status Clear. Converter overrange clear bit (active high). After an overrange sticky bit is set, it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLR bit. The DFORMAT_OVR_CLEAR[95:0] bits must be cleared for further overrange to be reported . [0] = Overrange sticky bit clear for Converter 0 [1] = Overrange sticky bit clear for Converter 1 [2] = Overrange sticky bit clear for Converter 2 and so on.	0x0	R/W
0x193	OVR_CLR_6	[7:0]	DFORMAT_OVR_CLR[55:48]	Overrange Status Clear. Converter overrange clear bit (active high). After an overrange sticky bit is set, it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLR bit. The DFORMAT_OVR_CLEAR[95:0] bits must be cleared for further overrange to be reported . [0] = Overrange sticky bit clear for Converter 0 [1] = Overrange sticky bit clear for Converter 1 [2] = Overrange sticky bit clear for Converter 2 and so on.	0x0	R/W
0x194	OVR_CLR_7	[7:0]	DFORMAT_OVR_CLR[63:56]	Overrange Status Clear. Converter overrange clear bit (active high). After an overrange sticky bit is set, it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLR bit. The DFORMAT_OVR_CLEAR[95:0] bits must be cleared for further overrange to be reported . [0] = Overrange sticky bit clear for Converter 0 [1] = Overrange sticky bit clear for Converter 1 [2] = Overrange sticky bit clear for Converter 2 and so on.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x195	OVR_CLR_8	[7:0]	DFORMAT_OVR_CLR[71:64]	Overrange Status Clear. Converter overrange clear bit (active high). After an overrange sticky bit is set, it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLR bit. The DFORMAT_OVR_CLEAR[95:0] bits must be cleared for further overrange to be reported . [0] = Overrange sticky bit clear for Converter 0 [1] = Overrange sticky bit clear for Converter 1 [2] = Overrange sticky bit clear for Converter 2 and so on.	0x0	R/W
0x196	OVR_CLR_9	[7:0]	DFORMAT_OVR_CLR[79:72]	Overrange Status Clear. Converter overrange clear bit (active high). After an overrange sticky bit is set, it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLR bit. The DFORMAT_OVR_CLEAR[95:0] bits must be cleared for further overrange to be reported . [0] = Overrange sticky bit clear for Converter 0 [1] = Overrange sticky bit clear for Converter 1 [2] = Overrange sticky bit clear for Converter 2 and so on.	0x0	R/W
0x197	OVR_CLR_10	[7:0]	DFORMAT_OVR_CLR[87:80]	Overrange Status Clear. Converter overrange clear bit (active high). After an overrange sticky bit is set, it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLR bit. The DFORMAT_OVR_CLEAR[95:0] bits must be cleared for further overrange to be reported . [0] = Overrange sticky bit clear for Converter 0 [1] = Overrange sticky bit clear for Converter 1 [2] = Overrange sticky bit clear for Converter 2 and so on.	0x0	R/W
0x198	OVR_CLR_11	[7:0]	DFORMAT_OVR_CLR[95:88]	Overrange Status Clear. Converter overrange clear bit (active high). After an overrange sticky bit is set, it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLR bit. The DFORMAT_OVR_CLEAR[95:0] bits must be cleared for further overrange to be reported . [0] = Overrange sticky bit clear for Converter 0 [1] = Overrange sticky bit clear for Converter 1 [2] = Overrange sticky bit clear for Converter 2 and so on.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x199	OVR_STATUS_0	[7:0]	DFORMAT_OVR_STATUS[7:0]	Output Overrange Status Indicator. Converter overrange indication sticky bits (active high). One bit for each virtual converter 0: No overrange occurred. 1: Overrange occurred. This bit is set to 1 if converter is driven beyond the specified input range. It is sticky, meaning it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLEAR[15:0] bits. The corresponding DFORMAT_OVR_CLEAR[15:0] bits must be cleared for further overflows to be reported. [0] = Overrange sticky bit for Converter 0 [1] = Overrange sticky bit for Converter 1 [2] = Overrange sticky bit for Converter 2 and so on.	0x0	R
0x19A	OVR_STATUS_1	[7:0]	DFORMAT_OVR_STATUS[15:8]	Output Overrange Status Indicator. Converter overrange indication sticky bits (active high). One bit for each virtual converter 0: No overrange occurred. 1: Overrange occurred. This bit is set to 1 if converter is driven beyond the specified input range. It is sticky, meaning it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLEAR[15:0] bits. The corresponding DFORMAT_OVR_CLEAR[15:0] bits must be cleared for further overflows to be reported. [0] = Overrange sticky bit for Converter 0 [1] = Overrange sticky bit for Converter 1 [2] = Overrange sticky bit for Converter 2 and so on.	0x0	R
0x19B	OVR_STATUS_2	[7:0]	DFORMAT_OVR_STATUS[23:16]	Output Overrange Status Indicator. Converter overrange indication sticky bits (active high). One bit for each virtual converter 0: No overrange occurred. 1: Overrange occurred. This bit is set to 1 if converter is driven beyond the specified input range. It is sticky, meaning it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLEAR[15:0] bits. The corresponding DFORMAT_OVR_CLEAR[15:0] bits must be cleared for further overflows to be reported. [0] = Overrange sticky bit for Converter 0 [1] = Overrange sticky bit for Converter 1 [2] = Overrange sticky bit for Converter 2 and so on.	0x0	R

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x19C	OVR_STATUS_3	[7:0]	DFORMAT_OVR_ STATUS[31:24]	Output Overrange Status Indicator. Converter overrange indication sticky bits (active high). One bit for each virtual converter 0: No overrange occurred. 1: Overrange occurred. This bit is set to 1 if converter is driven beyond the specified input range. It is sticky, meaning it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLEAR[15:0] bits. The corresponding DFORMAT_OVR_CLEAR[15:0] bits must be cleared for further overflows to be reported. [0] = Overrange sticky bit for Converter 0 [1] = Overrange sticky bit for Converter 1 [2] = Overrange sticky bit for Converter 2 and so on.	0x0	R
0x19D	OVR_STATUS_4	[7:0]	DFORMAT_OVR_ STATUS[39:32]	Output Overrange Status Indicator. Converter overrange indication sticky bits (active high). One bit for each virtual converter 0: No overrange occurred. 1: Overrange occurred. This bit is set to 1 if converter is driven beyond the specified input range. It is sticky, meaning it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLEAR[15:0] bits. The corresponding DFORMAT_OVR_CLEAR[15:0] bits must be cleared for further overflows to be reported. [0] = Overrange sticky bit for Converter 0 [1] = Overrange sticky bit for Converter 1 [2] = Overrange sticky bit for Converter 2 and so on.	0x0	R
0x19E	OVR_STATUS_5	[7:0]	DFORMAT_OVR_ STATUS[47:40]	Output Overrange Status Indicator. Converter overrange indication sticky bits (active high). One bit for each virtual converter 0: No overrange occurred. 1: Overrange occurred. This bit is set to 1 if converter is driven beyond the specified input range. It is sticky, meaning it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLEAR[15:0] bits. The corresponding DFORMAT_OVR_CLEAR[15:0] bits must be cleared for further overflows to be reported. [0] = Overrange sticky bit for Converter 0 [1] = Overrange sticky bit for Converter 1 [2] = Overrange sticky bit for Converter 2 and so on.	0x0	R

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x19F	OVR_STATUS_6	[7:0]	DFORMAT_OVR_ STATUS[55:48]	Output Overrange Status Indicator. Converter overrange indication sticky bits (active high). One bit for each virtual converter 0: No overrange occurred. 1: Overrange occurred. This bit is set to 1 if converter is driven beyond the specified input range. It is sticky, meaning it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLEAR[15:0] bits. The corresponding DFORMAT_OVR_CLEAR[15:0] bits must be cleared for further overflows to be reported. [0] = Overrange sticky bit for Converter 0 [1] = Overrange sticky bit for Converter 1 [2] = Overrange sticky bit for Converter 2 and so on.	0x0	R
0x1A0	OVR_STATUS_7	[7:0]	DFORMAT_OVR_ STATUS[63:56]	Output Overrange Status Indicator. Converter overrange indication sticky bits (active high). One bit for each virtual converter 0: No overrange occurred. 1: Overrange occurred. This bit is set to 1 if converter is driven beyond the specified input range. It is sticky, meaning it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLEAR[15:0] bits. The corresponding DFORMAT_OVR_CLEAR[15:0] bits must be cleared for further overflows to be reported. [0] = Overrange sticky bit for Converter 0 [1] = Overrange sticky bit for Converter 1 [2] = Overrange sticky bit for Converter 2 and so on.	0x0	R
0x1A1	OVR_STATUS_8	[7:0]	DFORMAT_OVR_ STATUS[71:64]	Output Overrange Status Indicator. Converter overrange indication sticky bits (active high) . One bit for each virtual converter 0: No overrange occurred. 1: Overrange occurred. This bit is set to 1 if converter is driven beyond the specified input range. It is sticky, meaning it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLEAR[15:0] bits . The corresponding DFORMAT_OVR_CLEAR[15:0] bits must be cleared for further overflows to be reported. [0] = Overrange sticky bit for Converter 0 [1] = Overrange sticky bit for Converter 1 [2] = Overrange sticky bit for Converter 2 and so on.	0x0	R

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x1A2	OVR_STATUS_9	[7:0]	DFORMAT_OVR_ STATUS[79:72]	Output Overrange Status Indicator. Converter overrange indication sticky bits (active high) . One bit for each virtual converter 0: No overrange occurred. 1: Overrange occurred. This bit is set to 1 if converter is driven beyond the specified input range. It is sticky, meaning it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLEAR[15:0] bits . The corresponding DFORMAT_OVR_CLEAR[15:0] bits must be cleared for further overflows to be reported. [0] = Overrange sticky bit for Converter 0 [1] = Overrange sticky bit for Converter 1 [2] = Overrange sticky bit for Converter 2 and so on.	0x0	R
0x1A3	OVR_STATUS_10	[7:0]	DFORMAT_OVR_ STATUS[87:80]	Output Overrange Status Indicator. Converter overrange indication sticky bits (active high) . One bit for each virtual converter 0: No overrange occurred. 1: Overrange occurred. This bit is set to 1 if converter is driven beyond the specified input range. It is sticky, meaning it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLEAR[15:0] bits . The corresponding DFORMAT_OVR_CLEAR[15:0] bits must be cleared for further overflows to be reported. [0] = Overrange sticky bit for Converter 0 [1] = Overrange sticky bit for Converter 1 [2] = Overrange sticky bit for Converter 2 and so on.	0x0	R
0x1A4	OVR_STATUS_11	[7:0]	DFORMAT_OVR_ STATUS[95:88]	Output Overrange Status Indicator. Converter overrange indication sticky bits (active high) . One bit for each virtual converter 0: No overrange occurred. 1: Overrange occurred. This bit is set to 1 if converter is driven beyond the specified input range. It is sticky, meaning it remains set until explicitly cleared by writing a 1 to the corresponding DFORMAT_OVR_CLEAR[15:0] bits . The corresponding DFORMAT_OVR_CLEAR[15:0] bits must be cleared for further overflows to be reported. [0] = Overrange sticky bit for Converter 0 [1] = Overrange sticky bit for Converter 1 [2] = Overrange sticky bit for Converter 2 and so on.	0x0	R
0x1B0	DATA_PATTERN_OVERRIDE	[7:4]	RESERVED	Reserved.	0x0	R
		[3:2]	RESERVED	Reserved.	0x0	R
		1	DATA_PATTERN_OVERRIDE	This Bit Overrides the Dformat_tmode_sel[*] in the Dformat. 0: Don't override data-pattern (Default). 1: Override data-pattern.	0x0	R/W
		0	RESERVED	Reserved.	0x0	R

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x1C0	SYNC_CTRL1	[7:4]	RESERVED	Reserved.	0x1	R
		3	NCORESET_ALL_SYSREF	NCO Reset Control by SYSREF. Applicable only in resynchronization mode. 0: NCO reset happens only with a SYSREF which caused resynchronization of clocks. 1: NCO reset happens with all SYSREF pulses (not recommended unless SYSREF period is much greater LMFC periods).	0x1	R/W
		2	SYSREF_RESYNC_MODE	SYSREF Resync Mode. 0: SYSREF is not used for resync 1: SYSREF is used for resync	0x0	R/W
		1	RISEDGE_SYSREF	Risedge SYSREF. 0: No rise edge detection on SYSREF pin. Input SYSREF used as such 1: Rise edge detection done on input SYSREF and used.	0x0	R/W
		0	DP_CLK_FORCEN	Reserved.	0x0	R/W
0x1C1	TRIG_PROG_DELAY	[7:0]	TRIG_PROG_DELAY	Programmable delay for input trig in terms of $f_S/4$ clock cycles.	0x0	R/W
0x1C2	SYSREF_PROG_DELAY	[7:0]	SYSREF_PROG_DELAY	Programmable delay for input SYSREF terms of $f_S/2$ clock cycles.	0x0	R/W
0x1C3	TRIG_CTRL	[7:6]	TRIG_EDGE_CTRL	Control for Trig Edge Detection. 00: No Edge Detection. 01: Positive Edge. 10: Negative Edge.	0x0	R/W
		[5:0]	RESERVED	Reserved.	0x10	R/W
0x1C4	DDC_SYNC_CTRL	[7:5]	RESERVED	Reserved.	0x0	R/W
		4	DDC_SOFT_RESET	Digital Down Converter Soft Reset. Digital Down Converter Soft Reset 0: Normal Operation 1: DDC Held in Reset. Note: this bit can be used to synchronize all the NCOs inside the DDC blocks.	0x0	R/W
		[3:2]	RESERVED	Reserved.	0x0	R
		1	DDC_SYNC_NEXT	DDC Next Synchronization Mode. DDC Next Synchronization Mode 0: Continuous mode 1: Next Synchronization mode - only the next valid edge of SYSREF pin will be used to synchronize the NCO in the DDC block. Subsequent edges of the SYSREF pin will be ignored. Note: The SYSREF pin must an integer multiple of the NCO frequency in order for this function to operate correctly in continuous mode.	0x1	R/W
		0	DDC_SYNC_EN	DDC Synchronization Enable. DDC Synchronization Enable 0: Synchronization Disabled 1: Synchronization Enabled. If DDC_SYNC_ NEXT = 1, only the next valid edge of the SYSREF pin will be used to synchronize the NCO in the DDC block. Subsequent edges of the SYSREF pin are ignored. After the next SYSREF is received, this must be cleared for any subsequent use of next SYSREF. Note: the SYSREF input pin must be enabled in order to synchronize the DDCs.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x1C5	DDC_SYNC_STATUS	[7:1]	RESERVED	Reserved.	0x0	R
		0	DDC_SYNC_EN_CLEAR	DDC Sync Enable Clear Status. DDC Sync Enable Clear Status	0x0	R
JESD204B Transmitter (JTX) Control Registers						
0x200 to 0x25F by 1	JTX_CORE_SAMPLE_ XBARn	7	JTX_CONV_DISABLE	Converter sample mask to 0.	0x0	R/W
		[6:0]	JTX_CONV_SEL	Converter sample crossbar selection.	0x0	R/W
0x260	JTX_CORE_CONFIG	7	JTX_SYSREF_FOR_RELINK	Will mask lane data to 0 until another SYSREF pulse is received if SYNC~ is asserted. Applies to JESD204B operation only.	0x0	R/W
		6	JTX_SYSREF_FOR_STARTUP	Will mask lane data to 0 until the first SYSREF pulse is received after reset.	0x0	R/W
		[5:4]	RESERVED	Reserved.	0x0	R
		3	JTX_CHKSUM_LSB_ALG	0: Sum whole octets of L0 config for checksum 1: Sum individual fields for checksum.	0x0	R/W
		2	JTX_CHKSUM_DISABLE	Checksum is always 0.	0x0	R/W
		[1:0]	JTX_LINK_TYPE	Link layer type selection: 0: 204B 1: 204C 2: 204H.	0x0	R/W
0x261 to 0x264 by 1	JTX_CORE_LANE_ XBARn	7	JTX_LANE_PD	Physical lane in use based on link and crossbar configuration.	0x0	R
		6	JTX_FORCE_LANE_PD	Send 0s and activate jtx_lane_pd.	0x0	R/W
		5	JTX_LANE_INV	Invert logical lane data (before crossbar).	0x0	R/W
		[4:0]	JTX_LANE_SEL	Lane crossbar selection. Setting here selects which logical lane should feed the physical lane.	0x0	R/W
0x271	JTX_CORE_TEST_ CONFIG	7	JTX_TEST_USER_GO	Activate USER_SINGLE test mode.	0x0	R/W
		6	JTX_TEST_MIRROR	Reverse bit order of test data.	0x0	R/W
		[5:4]	JTX_TEST_GEN_SEL	Test insertion point.	0x0	R/W
		[3:0]	JTX_TEST_GEN_MODE	Test mode selection. 0: Disabled for TEST_GEN_SEL = 0, lane loopback for TEST_GEN_SEL = 1. 1: CHECKER_BOARD 2: WORD_TOGGLE 3: PN31 5: PN15 7: PN7 8: RAMP 14: USER_REPEAT 15: USER_SINGLE.	0x0	R/W
0x272	JTX_TEST_USER_DATA0	[7:0]	JTX_TEST_USER_DATA[7:0]	User defined test data in LSBs.	0x0	R/W
0x273	JTX_TEST_USER_DATA1	[7:0]	JTX_TEST_USER_DATA[15:8]	User defined test data in LSBs.	0x0	R/W
0x274	JTX_TEST_USER_DATA2	[7:0]	JTX_TEST_USER_DATA[23:16]	User defined test data in LSBs.	0x0	R/W
0x275	JTX_TEST_USER_DATA3	[7:0]	JTX_TEST_USER_DATA[31:24]	User defined test data in LSBs.	0x0	R/W
0x276	JTX_TEST_USER_DATA4	[7:0]	JTX_TEST_USER_DATA[39:32]	User defined test data in LSBs.	0x0	R/W
0x277	JTX_TEST_USER_DATA5	[7:0]	JTX_TEST_USER_DATA[47:40]	User defined test data in LSBs.	0x0	R/W
0x278	JTX_TEST_USER_DATA6	[7:0]	JTX_TEST_USER_DATA[55:48]	User defined test data in LSBs.	0x0	R/W
0x279	JTX_TEST_USER_DATA7	[7:0]	JTX_TEST_USER_DATA[63:56]	User defined test data in LSBs.	0x0	R/W
0x27A	JTX_TEST_USER_DATA8	[7:2]	RESERVED	Reserved.	0x0	R
		[1:0]	JTX_TEST_USER_DATA[65:64]	User defined test data in LSBs.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x27B	JTX_CORE_SYNC_N_SEL	[7:3]	RESERVED	Reserved.	0x0	R
		[2:0]	JTX_SYNC_N_SEL	Decimal value to select the physical sync_n source pin. Ignored when JTX_NUM_LINKS = 1.	0x0	R/W
0x27C	JTX_CORE_13	[7:1]	RESERVED	Reserved.	0x0	R
		0	JTX_LINK_EN	See JTX documentation.	0x0	R/W
0x27D	JTX_TPL_CONFIG0	[7:3]	JTX_NS_CFG	Number of unique samples per converter in conv_sample.	0x0	R/W
		2	JTX_TPL_CONV_ASYNCHRONOUS	Expect link_pclk asynchronous to conv_clk. This will increase the delay for the domain handoff buffer in fixed latency mode. The increased delay may require setting the JTX_TPL_ASYNC_SUPPORT parameter.	0x0	R/W
		1	JTX_TPL_TEST_ENABLE	Enable long transport layer test.	0x0	R/W
		0	JTX_TPL_ADAPTIVE_LATENCY	Enable adaptive latency mode. Default should be 0.	0x0	R/W
0x27E	JTX_TPL_CONFIG1	7	JTX_TPL_SYSREF_IGNORE_WHEN_LINKED	Mask incoming SYSREF when SYNC~ is de-asserted. Applies to 204B operation only.	0x0	R/W
		6	JTX_TPL_SYSREF_CLR_PHASE_ERR	Clear jtx_tpl_SYSREF_phase_err.	0x0	R/W
		5	JTX_TPL_SYSREF_MASK	Mask any incoming SYSREF to 0.	0x0	R/W
		[4:3]	RESERVED	Reserved.	0x0	R
		2	JTX_TPL_SYSREF_PHASE_ERR	Incoming SYSREF has been registered at an unexpected time from the previously established SYSREF phase.	0x0	R
		1	JTX_TPL_SYSREF_RCVD	SYSREF phase has been established.	0x0	R
		0	RESERVED	Reserved	0x0	R
0x27F	JTX_TPL_LATENCY_ADJUST	[7:0]	JTX_TPL_LATENCY_ADJUST	Add additional conv_clk cycles of latency (for both latency modes). Useful in adaptive latency mode to get a wider adaptable range.	0x0	R/W
0x280	JTX_TPL_PHASE_ADJUST0	[7:0]	JTX_TPL_PHASE_ADJUST[7:0]	Output LMFC phase adjustment in conv_clk cycles. Maximum value is k*s/ns-1.	0x0	R/W
0x281	JTX_TPL_PHASE_ADJUST1	[7:0]	JTX_TPL_PHASE_ADJUST[15:8]	Output LMFC phase adjustment in conv_clk cycles. Maximum value is k*s/ns-1.	0x0	R/W
0x282	JTX_TPL_TEST_NUM_FRAMES0	[7:0]	JTX_TPL_TEST_NUM_FRAMES_M1[7:0]	Number of frames (minus 1) in the long transport layer test pattern.	0x0	R/W
0x283	JTX_TPL_TEST_NUM_FRAMES1	[7:0]	JTX_TPL_TEST_NUM_FRAMES_M1[15:8]	Number of frames (minus 1) in the long transport layer test pattern.	0x0	R/W
0x284	JTX_TPL_SYSREF_N_SHOT	[7:5]	RESERVED	Reserved.	0x0	R
		4	JTX_TPL_SYSREF_N_SHOT_ENABLE	Mask all incoming SYSREF pulses except the Nth pulse specified by the n_shot_count. Disabling this will cause all SYSREF pulses to be sampled (continuous mode) and reset the n_shot counter.	0x0	R/W
		[3:0]	JTX_TPL_SYSREF_N_SHOT_COUNT	Mask all incoming SYSREF pulses except the Nth pulse where N is the value programmed + 1. Only used when n_shot_enable is high.	0x0	R/W
0x285	JTX_TPL_BUF_FRAMES	[7:0]	JTX_TPL_BUF_FRAMES	Frame delay through transport layer buffer.	0x0	R
0x286	JTX_L0_DID	[7:0]	JTX_DID_CFG	Device (= link) identification no.	0x0	R/W
0x287	JTX_L0_ADJCNT_BID	[7:4]	JTX_ADJCNT_CFG	Number of adjustment resolution steps to adjust DAC LMFC. Applies to Subclass 2 operation only.	0x0	R/W
		[3:0]	JTX_BID_CFG	Bank ID Extension to DID.	0x0	R/W
		[4:0]	RESERVED	Reserved.	0x0	R

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x289	JTX_L0_SCR_L	7	JTX_SCR_CFG	JTx Scrambler 0 = Disabled 1 = Enabled	0x0	R/W
		[6:5]	RESERVED	Reserved.	0x0	R
		[4:0]	JTX_L_CFG	Number of lanes per converter device (link). 0 : L = 1 1 : L = 2 2 : L = 3 3 : L = 4 Values > 3 are not supported	0x0	R/W
0x28A	JTX_L0_F	[7:0]	JTX_F_CFG	Number of octets per frame per lane. F = N/16 × M × N / L.	0x0	R/W
0x28B	JTX_L0_K	[7:0]	JTX_K_CFG	Number of frames in a multi-frame/block.	0x0	R/W
0x28C	JTX_L0_M	[7:0]	JTX_M_CFG	Number of converters per device. JTx number of virtual converters per link (M=JTX M configuration + 1). 0 = 1 virtual converter 1 = 2 virtual converters 2 = 3 virtual converters 3 = 4 virtual converters 5 = 6 virtual converters 7 = 8 virtual converters 11 = 12 virtual converters 15 = 16 virtual converters All other values are invalid.	0x0	R/W
0x28D	JTX_L0_CS_N	[7:6]	JTX_CS_CFG	Number of control bits per sample.	0x0	R/W
		5	RESERVED	Reserved.	0x0	R
		[4:0]	JTX_N_CFG	Converter resolution.	0x0	R/W
0x28E	JTX_L0_SUBCLASSV_NP	[7:5]	JTX_SUBCLASSV_CFG	Device Subclass Version 2: align transmission and LMFC boundaries to SYNC~ 1: align transmission and LMFC boundaries to SYSREF 0: transmission and LMFC boundaries are arbitrary.	0x0	R/W
		[4:0]	JTX_NP_CFG	Total number of bits per sample.	0x0	R/W
0x28F	JTX_L0_JESDV_S	[7:5]	JTX_JESDV_CFG	JESD204 version 001: JESD204B	0x0	R/W
		[4:0]	JTX_S_CFG	Samples per converter per frame.	0x0	R/W
0x290	JTX_L0_HD	7	JTX_HD_CFG	High Density format enabled.	0x0	R/W
		[6:0]	RESERVED	Reserved.	0x0	R
0x293 to 0x296 by 1	JTX_L0_CHKSUMn	[7:0]	JTX_CHKSUM_CFG	Checksum calculation output (per lane).	0x0	R
0x297 to 0x29A by 1	JTX_L0_LIDn	[7:5]	RESERVED	Reserved.	0x0	R
		[4:0]	JTX_LID_CFG	Lane identification number (within link).	0x0	R/W
0x2A3	JTX_DL_204B_CONFIG0	[7:4]	JTX_DL_204B_ILAS_DELAY_CFG	Delays ILAS Start by 0 to 15 LMFC Periods.	0x0	R/W
		3	JTX_DL_204B_BYP_ILAS_CFG	bypass initial lane alignment sequence.	0x0	R/W
		2	JTX_DL_204B_ILAS_TEST_EN_CFG	Enable ilas test mode that sends repeated ILAS pattern. If sync_n not active then 16 Kchars sent followed by repeated ILAS.	0x0	R/W
		1	JTX_DL_204B_BYP_8B10B_CFG	Bypass 8-bit/10-bit encoder.	0x0	R/W
		0	JTX_DL_204B_BYP_ACG_CFG	bypass alignment character generation.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x2A4	JTX_DL_204B_CONFIG1	[7:3]	RESERVED	Reserved.	0x0	R
		2	JTX_DL_204B_LSYNC_EN_CFG	Lane sync on both sides enabled.	0x0	R/W
		1	JTX_DL_204B_DEL_SCR_CFG	Alternative scrambler enable (see JESD204B section 5.2.4) 1 = scrambling begins at octet 2 of user data 0 = scrambling begins at octet 0 of user data This is the common usage.	0x0	R/W
		0	JTX_DL_204B_10B_MIRROR	Reverse order of 10 bit symbols from 204B link layer data.	0x0	R/W
0x2A5	JTX_DL_204B_CONFIG2	[7:6]	RESERVED	Reserved.	0x0	R
		5	JTX_DL_204B_TESTMODE_IGNORE_SYNCN_CFG	ignore sync_n input during D21.5 and RPAT modes.	0x0	R/W
		4	JTX_DL_204B_TPL_TEST_EN_CFG	Turn on JESD Pattern Sequence test mode.	0x0	R/W
		3	RESERVED	Reserved.	0x0	R
		[2:1]	JTX_DL_204B_RJSPAT_SEL_CFG	High Frequency Patterns Test Modes 11 = Unused 10 = JTSPAT Sequence 01 = JSPAT Sequence 00 = RPAT Sequence.	0x0	R/W
		0	JTX_DL_204B_RJSPAT_EN_CFG	Enable RPAT/JSPAT/JTSPAT Generator 1 = on (Note: Must also set phy_data_sel[n] = 1) 0 = off.	0x0	R/W
0x2A6	JTX_DL_204B_KF_ILAS	[7:0]	JTX_DL_204B_KF_ILAS_CFG	Number of multiframes to transmit during initialization sequence = 4*(kf_ilas_cfg+1).	0x0	R/W
0x2A8	JTX_DL_204B_SYNC_N	7	JTX_DL_204B_SYNC_N	JESD204 Frame Sync. Active low. Synchronous upon rising edge pclk. 0=transmit code group sync (K characters). Subclass 1: Internal LMFC reset for 1-pclk by falling edge sync_n Subclass 0: Internal lmfc held in reset by sync_n=0.	0x0	R
		[6:2]	RESERVED	Reserved.	0x0	R
		1	JTX_DL_204B_SYNC_N_FORCE_EN	Force SYNC~ signal to value specified.	0x0	R/W
		0	JTX_DL_204B_SYNC_N_FORCE_VAL	Value to force SYNC~ if force enabled.	0x0	R/W
0x2A9	JTX_DL_204B_CLEAR_SYNC_NE_COUNT	[7:1]	RESERVED	Reserved.	0x0	R
		0	JTX_DL_204B_CLEAR_SYNC_NE_COUNT	Clear counter of SYNC~ falling edges.	0x0	R/W
0x2AA	JTX_DL_204B_SYNC_NE_COUNT	[7:0]	JTX_DL_204B_SYNC_NE_COUNT	Count of falling SYNC~ edges.	0x0	R
0x2AB to 0x2AE by 1	JTX_DL_204B_LANE_CONFIGn	[7:5]	RESERVED	Reserved.	0x0	R
		4	JTX_DL_204B_SCR_IN_CTRL_CFG	connect test_data[39:0] to scrambler input for lane n.	0x0	R/W
		3	JTX_DL_204B_SCR_DATA_SEL_CFG	Scrambler Input JESD Data on Lane Boundary scr_data_sel_cfg [n]: 1 = Continuous D21.5 Data for Lane [n] scr_data_sel_cfg [n]: 0 = JESD Frame Memory or ILAS Data for Lane[n].	0x0	R/W
		2	JTX_DL_204B_PHY_DATA_SEL_CFG	JESD Data to PHY on a Lane Boundary [n]: 1 = RPAT/JSPAT/JTSPAT Generator Data [n]: 0 = 8-bit/10-bit Encoder Output Data.	0x0	R/W
		1	RESERVED	Reserved.	0x0	R
		0	RESERVED	Reserved	0x0	R/W
0x2C9 to 0x2CC by 1	JTX_PHY_IFX_LANE_CONFIGn	[7:4]	JTX_LANE_FIFO_WR_ENTRIES	Number of entries in the FIFO synchronized to the write pointer.	0x0	R
		[3:0]	JTX_BR_LOG2_RATIO	Log(bit repeat ratio)/Log(2), per lane.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x301	PLL_STATUS	7	JTX_PLL_LOCKED	PLL Locked Status Bit.	0x0	R
		[6:0]	RESERVED	Reserved.	0x0	R
0x309	SYSREF_DELAY_REG	7	SYSREF_PULSE_DELAY_ ENABLE	Force link reset from Regmap.	0x0	R/W
		[6:0]	SYSREF_PULSE_DELAY_CYCLES	Force link reset from Regmap.	0x0	R/W
0x30A	RESET_CTRL_REG	7	FORCE_JTX_PLL_RST_ RELEASE_EN	Enable Force JTX_PLL Reset Release.	0x0	R/W
		6	FORCE_JTX_PLL_RST_ RELEASE	Force JTX_PLL reset release.	0x0	R/W
		5	RESERVED	Reserved.	0x0	R
		4	FORCE_JTX_DIGITAL_RESET_ ON_SYSREF	Enable SYSREF to Force link reset.	0x0	R/W
		[3:1]	RESERVED	Reserved.	0x0	R
		0	FORCE_JTX_DIGITAL_RESET_ ON_RSTEN_FORCE_EN	Enable Early Detection of SYSREF to Force link reset.	0x0	R/W
0x30B	SER_PARITY_RESET_EN1	[7:0]	SER_PARITY_RESET_EN	parity reset enable.	0x0	R/W
0x30C	LCM_DIV_FORCE_EN	[7:1]	RESERVED	Reserved.	0x0	R
		0	LCM_DIV_FORCE_EN	LCM Divider Value Force Enable.	0x0	R/W
0x30D	LCM_DIV1	[7:0]	LCM_DIV[7:0]	LCM Divider Value.	0x0	R/W
0x30E	LCM_DIV2	[7:0]	LCM_DIV[15:8]	LCM Divider Value.	0x0	R/W
0x30F	LMFC_CTL	7	LMFC_OUT_SEL	To select the lmfc or divided lmfc'.	0x0	R/W
		[6:5]	RESERVED	Reserved.	0x0	R
		4	LMFC_DIV_EDGE	which edge of LMFC. which edge of LMFC is used for division before sending out of GPIO. 0for posedge	0x0	R/W
		3	RESERVED	Reserved.	0x0	R
		[2:0]	LMFC_OUT_DIV	Divider value before passing LMFC out of GPIO.	0x0	R/W
0x310	FORCE_LINK_RESET_REG	[7:5]	RESERVED	Reserved.	0x0	R
		4	FORCE_LINK_DIGITAL_RESET	Force link reset from Regmap.	0x0	R/W
		[3:1]	RESERVED	Reserved.	0x0	R
		0	FORCE_LINK_RESET	Force link reset from Regmap.	0x1	R/W
0x313	PHASE_ESTABLISH_ STATUS	[7:1]	RESERVED	Reserved.	0x0	R
		0	JTX_PHASE_ESTABLISHED	phase established readback.	0x0	R
0x315	CLKGEN_ALIGN_FALL_R ST_DEASSERT	[7:1]	RESERVED	Reserved.	0x0	R
		0	CLKGEN_ALIGN_FALL_FOR_R ST_DEASSERT	To use clkgen_align for rst de-assert.	0x0	R/W
0x317	PLL_REF_CLK_DIV1_REG	[7:4]	RESERVED	Reserved.	0x0	R
		[3:0]	DIVM_JTX_PLL_RC_RX	Selects output division rate;. Selects output division rate; 0: pd 1: no divider 2: divide by 2 3: divide by 4	0x2	R/W
0x319	PCLK_SYNC_DIV_REG1	[7:0]	PCLK_SYNC_DIV_VAL[7:0]	JESD Synchronous PCLK Divider Value.	0x4	R/W
0x31A	PCLK_SYNC_DIV_REG2	[7:1]	RESERVED	Reserved.	0x0	R
		0	PCLK_SYNC_DIV_VAL[8]	JESD Synchronous PCLK Divider Value.	0x0	R/W
0x31B	PCLK_ASYNC_DIV_REG1	[7:0]	PCLK_ASYNC_DIV_VAL[7:0]	JESD Asynchronous PCLK Divider Value.	0x4	R/W
0x31C	PCLK_ASYNC_DIV_REG2	[7:1]	RESERVED	Reserved.	0x0	R
		0	PCLK_ASYNC_DIV_VAL[8]	JESD Asynchronous PCLK Divider Value.	0x0	R/W
0x31D	CONV_CLK_DIV_REG1	[7:0]	CONV_CLK_DIV_VAL[7:0]	JESD Conv Clock Divider Value.	0x4	R/W
0x31E	CONV_CLK_DIV_REG2	[7:2]	RESERVED	Reserved.	0x0	R
		[1:0]	CONV_CLK_DIV_VAL[9:8]	JESD Conv Clock Divider Value.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x31F	JTX_CLK_CTRL_REG	[7:4]	RESERVED	Reserved.	0x0	R
		3	JTX_ASYNC_PCLK_EN	Enable to the Async Conv Clk Divider.	0x1	R/W
		2	JTX_IFX_CLK_EN	Enable to the IFX Clock Divider.	0x1	R/W
		1	JTX_CONV_CLK_EN	Enable to the Conv Clk Divider.	0x1	R/W
		0	JTX_SYNC_PCLK_EN	Enable to the Sync PCLK Divider.	0x1	R/W
0x320	JTX_CLK_CTRL_REG2	[7:4]	RESERVED	Reserved.	0x0	R
		3	JTX_CONV_CLK_DIV_ OVERRIDE	Override the Async Conv Clk Div Val with the Regmap Val.	0x0	R/W
		2	JTX_IFX_CLK_DIV_OVERRIDE	Override the Async Conv Clk Div Val with the Regmap Val.	0x0	R/W
		1	JTX_SYNC_PCLK_DIV_ OVERRIDE	Override the Async Conv Clk Div Val with the Regmap Val.	0x0	R/W
		0	JTX_ASYNC_PCLK_DIV_ OVERRIDE	Override the Async Conv Clk DivVal with the Regmap Val.	0x0	R/W
0x321	IFX_CLK_DIV_REG1	[7:0]	IFX_CLK_DIV_VAL[7:0]	JESD IFX Clock Divider Value.	0x4	R/W
0x322	IFX_CLK_DIV_REG2	[7:1]	RESERVED	Reserved.	0x0	R
		0	IFX_CLK_DIV_VAL[8]	JESD IFX Clock Divider Value.	0x0	R/W
0x323	ASYNC_PCLK_CTRL	7	TESTMUX_CLK_SEL	Select Testmux_clk[0] as the asynchronous clock.	0x0	R/W
		6	TESTMUX_CLK_EN	Enable Testmux_clk[0] Select.	0x0	R/W
		[5:4]	RESERVED	Reserved.	0x0	R
		3	ASYNC_LANE_DOUT_SEL	Select Asynchronous Lane Data.	0x0	R/W
		2	ASYNC_LINK_PCLK_SEL	Select Asynchronous Link PCLK.	0x0	R/W
		1	ASYNC_LANE_CLK_SEL	Select Asynchronous Lane Clock.	0x0	R/W
		0	ASYNC_IFX_PCLK_SEL	Select Asynchronous IFX PCLK.	0x0	R/W
0x325	JTX_PCLK_DIV_ INTEGER1	[7:0]	JTX_PCLK_DIV_INTEGER[7:0]	Integer Part for PCLK Divider.	0x0	R/W
0x326	JTX_PCLK_DIV_ INTEGER2	[7:1]	RESERVED	Reserved.	0x0	R
		0	JTX_PCLK_DIV_INTEGER[8]	Integer Part for PCLK Divider.	0x0	R/W
0x327	JTX_PCLK_DIV_FRAC_ NUM	[7:5]	RESERVED	Reserved.	0x0	R
		[4:0]	JTX_PCLK_DIV_FRAC_NUM	Fractional Numerator for PCLK Divider.	0x0	R/W
0x328	JTX_PCLK_DIV_FRAC_ DEN	[7:5]	RESERVED	Reserved.	0x0	R
		[4:0]	JTX_PCLK_DIV_FRAC_DEN	Fractional Denominator for PCLK Divider.	0x0	R/W
0x329	JTX_IFX_PCLK_DIV_ INTEGER1	[7:0]	JTX_IFX_PCLK_DIV_ INTEGER[7:0]	Integer Part for PCLK Divider.	0x0	R/W
0x32A	JTX_IFX_PCLK_DIV_ INTEGER2	[7:1]	RESERVED	Reserved.	0x0	R
		0	JTX_IFX_PCLK_DIV_ INTEGER[8]	Integer Part for PCLK Divider.	0x0	R/W
0x32B	JTX_IFX_PCLK_DIV_ FRAC_NUM	[7:5]	RESERVED	Reserved.	0x0	R
		[4:0]	JTX_IFX_PCLK_DIV_FRAC_ NUM	Fractional Numerator for PCLK Divider.	0x0	R/W
0x32C	JTX_IFX_PCLK_DIV_ FRAC_DEN	[7:5]	RESERVED	Reserved.	0x0	R
		[4:0]	JTX_IFX_PCLK_DIV_FRAC_ DEN	Fractional Denominator for PCLK Divider.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x402	JTX_SWING	7	RESERVED	Reserved.	0x0	R
		[6:4]	DRVSWING_CH1_SER_RC	SERDOUT1 output swing level. 0 = 1.00 × DVDD 1 = 0.85 × DVDD 2 = 0.75 × DVDD 3 = 0.50 × DVDD	0x1	R/W
		3	RESERVED	Reserved.	0x0	R
		[2:0]	DRVSWING_CH0_SER_RC	SERDOUT0 output swing level. 0 = 1.00 × DVDD 1 = 0.85 × DVDD 2 = 0.75 × DVDD 3 = 0.50 × DVDD	0x1	R/W
0x403	JTX_SWING2	7	RESERVED	Reserved.	0x0	R
		[6:4]	DRVSWING_CH3_SER_RC	SERDOUT3 output swing level. 0 = 1.00 × DVDD 1 = 0.85 × DVDD 2 = 0.75 × DVDD 3 = 0.50 × DVDD	0x1	R/W
		3	RESERVED	Reserved.	0x0	R
		[2:0]	DRVSWING_CH2_SER_RC	SERDOUT2 output swing level. 0 = 1.00 × DVDD 1 = 0.85 × DVDD 2 = 0.75 × DVDD 3 = 0.50 × DVDD	0x1	R/W
0x40A	POST_TAP_LEVEL1	7	RESERVED	Reserved.	0x0	R
		[6:4]	DRVPOSTEM_CH1_SER_RC	Sets Post Tap Level for SERDOUT1. 0 = 0 dB. 1 = 3 dB. 2 = 6 dB. 3 = 9 dB. 4 = 12 dB. 5 to 7 = not applicable.	0x0	R/W
		3	RESERVED	Reserved.	0x0	R
		[2:0]	DRVPOSTEM_CH0_SER_RC	Sets Post Tap Level for SERDOUT0. 0 = 0 dB. 1 = 3 dB. 2 = 6 dB. 3 = 9 dB. 4 = 12 dB. 5 to 7 = not applicable.	0x0	R/W
0x40B	POST_TAP_LEVEL2	7	RESERVED	Reserved.	0x0	R
		[6:4]	DRVPOSTEM_CH3_SER_RC	Sets Post Tap Level for SERDOUT3. 0 = 0 dB. 1 = 3 dB. 2 = 6 dB. 3 = 9 dB. 4 = 12 dB. 5 to 7 = not applicable.	0x0	R/W
		3	RESERVED	Reserved.	0x0	R
		[2:0]	DRVPOSTEM_CH2_SER_RC	Sets Post Tap Level for SERDOUT2. 0 = 0 dB. 1 = 3 dB. 2 = 6 dB. 3 = 9 dB. 4 = 12 dB. 5 to 7 = not applicable.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x413	PRE_TAP_LEVEL_CH0	[7:0]	DRVPREEM_CH0_SER_RC	Sets Pre Tap Level for SERDOUT0. 0 = 0 dB. 1 = 3 dB. 2 = 6 dB. 3 = not applicable.	0x0	R/W
0x414	PRE_TAP_LEVEL_CH1	[7:0]	DRVPREEM_CH1_SER_RC	Sets Pre Tap Level for SERDOUT1. 0 = 0 dB. 1 = 3 dB. 2 = 6 dB. 3 = not applicable.	0x0	R/W
0x415	PRE_TAP_LEVEL_CH2	[7:0]	DRVPREEM_CH2_SER_RC	Sets Pre Tap Level for SERDOUT2. 0 = 0 dB. 1 = 3 dB. 2 = 6 dB. 3 = not applicable.	0x0	R/W
0x416	PRE_TAP_LEVEL_CH3	[7:0]	DRVPREEM_CH3_SER_RC	Sets Pre Tap Level for SERDOUT3. 0 = 0 dB. 1 = 3 dB. 2 = 6 dB. 3 = not applicable.	0x0	R/W
0x425	PARITY_ERROR	[7:0]	PARITY_ERROR_SER[7:0]	JTx Parity Output Error flag, <0>=ch0, <1>=ch1	0x0	R
0x426	PARITY_ERROR2	[7:0]	PARITY_ERROR_SER[15:8]	JTx Parity Output Error flag, <0>=ch0, <1>=ch1	0x0	R
0x427	PARITY_RST_N	[7:0]	SER_PARITY_RST_N[7:0]	JTx Parity Clear bit each bit is a channel. JTx Parity Clear bit each bit is a channel ==> <3> = chan_3, <2> = chan_2	0x0	R/W
0x428	PARITY_RST_N2	[7:0]	SER_PARITY_RST_N[15:8]	JTx Parity Clear bit each bit is a channel. JTx Parity Clear bit each bit is a channel ==> <3> = chan_3, <2> = chan_2	0x0	R/W
0x439	MAIN_DATA_INV	[7:4]	RESERVED	Reserved	0x0	R/W
		3	OUTPUTDATAINVERT_CH3	JTx, Invert SERDOUT3 data. 0 = normal. 1 = invert.	0x0	R/W
		2	OUTPUTDATAINVERT_CH2	JTx, Invert SERDOUT2 data. 0 = normal. 1 = invert.	0x0	R/W
		1	OUTPUTDATAINVERT_CH1	JTx, Invert SERDOUT1 data. 0 = normal. 1 = invert.	0x0	R/W
		0	OUTPUTDATAINVERT_CH0	JTx, Invert SERDOUT0 data. 0 = normal. 1 = invert.	0x0	R/W
0x447	SYNCINB_CTRL	[7:4]	RESERVED	Reserved.	0x0	R
		3	PD_SYNCINB_RX_RC	SYNCINB receiver power control bit. 0 = Normal Operation 1 = Power Down	0x1	R/W
		2	SYNCINB_RX_PN_INV_RC	SYNCINB Polarity control bit. 0 = Normal polarity 1 = Invert polarity	0x0	R/W
		1	SYNCINB_RX_ONCHIP_TERM_RC	SYNCINB onchip termination control bit. 0 = Disabled (Use if 0x447[0] = 0) 1 = Enabled (100Ω differential)	0x0	R/W
		0	SYNCINB_RX_MODE_RC	SYNCINB Mode control bit. 0 = CMOS mode (Single Ended) 1 = LVDS mode (Differential)	0x0	R/W
0x449	JTX_CTRL	[7:1]	RESERVED	Reserved.	0x0	R
		0	JTAG_EN_SER_TESTMODE_RC	SYNC control bit.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x500	JTX_PLL_RST	[7:1]	RESERVED	Reserved.	0x0	R
		0	RSTB_JTX_PLL_RC	Force link reset from REGMAP.	0x0	R/W
0x501	PLL_ENABLE_CTRL	7	PLL_LOCKED_BYPASS_VAL	Bypass value for PLL_LOCKED output when PLL_LOCKED_BYPASS is 1. Select between PLL lock signal and timer based lock signal generation	0x0	R/W
		6	PLL_LOCKED_BYPASS	Bypass control for PLL_LOCKED output. 0: use state machine value 1: use PLL_LOCKED_BYPASS_VAL). Select between PLL lock signal and timer based lock signal generation	0x0	R/W
		5	JTX_PLL_BYPASS_LOCK	Bypass PLL lock input.	0x0	R/W
		4	RESERVED	Reserved.	0x0	R
		3	LOLSTICKYCLEAR_FORCE_ JTX_PLL_RC	Clears out loss of lock bit.	0x0	R/W
		2	RESERVED	Reserved.	0x0	R
		1	LDSYNTH_FORCE_JTX_PLL_A DC	to start calibration. A short "1" pulse starts VCO calibration, the pulse width should be at least 1 reference clock period. Allows for user to do a calibration at will.	0x0	R/W
		0	PWRUP_JTX_PLL	Power up PLL. Power up PLL, starts LDO, Starts Calibration, sends out PLL locked when done . "Big green button", forces power up, will not read back correctly if PLL is powered up internally	0x0	R/W
0x502	PLL_STATUS	[7:5]	RESERVED	Reserved.	0x0	R
		4	LOSSLOCK_JTX_PLL_RS	PLL went out-of-lock. Bit to indicate PLL went out-of-lock at any time between frequency acquisitions.	0x0	R
		3	RFPLLLOCK_JTX_PLL_RS	PLL is locked when this bit is HIGH.	0x0	R
		2	VCOCALINPROG_JTX_PLL_RS	0: when the last ALC is done (VCO cal. state machine is in ALC_CAL_LSB state). 1: when init_cal_redge=1 initiated by ld_synth	0x0	R
		1	REGULATORRDY_JTX_PLL_RS	High = indicates regulator voltage is above threshold for at least cnt conversions	0x0	R
		0	JTX_PLLLOCK_JTX_PLL_RS	PLL is locked when this bit is high.	0x0	R
0x506	PLL_ENCAL	[7:5]	RESERVED	Reserved.	0x0	R
		4	PD_TXCLK_DIST_RC	txclk dist rc. Enable output clocks to serializer1 SER	0x0	R/W
		3	PD_RXCLK_DIST_RC	rxclk dist rc. Enable output clocks to serializer1 SER	0x0	R/W
		2	RESERVED	Reserved.	0x0	R
		1	EN_TX_ONLY_JTX_PLL_RC	Enable output clocks to serializer 1 SER only	0x0	R/W
		0	EN_OCTAVECAL_JTX_PLL_RC	Determines whether to enable PLL octave calibration.	0x0	R/W
0x507	JTX_PLL_REF_CLK_ DIV1_REG	7	REFCK_DIV40BDIV120_JTX_PLL	Ref clock output (1/40 or 1/120).	0x0	R/W
		6	DIVP_JTX_PLL_RC	Selects whether B is multiplied by 6 or 8. Selects output division rate; 0->pd, 1->no divider, 2->divide by 2, 3->divide by 4	0x0	R/W
		[5:4]	DIVM_JTX_PLL_RC	Selects output division rate;. Selects output division rate; 0->/1, 1->/2. Bit [1] is not used.	0x2	R/W
		3	RESERVED	Reserved.	0x0	R
		[2:0]	REFINDIV_JTX_PLL_RC	Sets division rate on input:. Sets division rate on input: 0->1, 1->2, 2->4, 3->8, 4 and above div 16	0x2	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x508	PLL_DIV2	[7:0]	B_JTX_PLL_RC	Selects PLL feedback divider. Sets integer division rate as N=8*B, where B=5 is its minimum value. (divb)	0x5	R/W
0x50A	PLL_DIVOVD	[7:4]	RESERVED	Reserved.	0x0	R
		3	RXDIVRATEOVD_JTX_PLL_RC	Override rxdivrate.	0x0	R/W
		2	REFINDIVOVD_JTX_PLL_RC	Override refindiv.	0x1	R/W
		1	DIVMOVD_JTX_PLL_RC	Override divm control.	0x1	R/W
		0	BOVD_JTX_PLL_RC	Bypass from octave cal (use b_JTX_PLL_rc).	0x1	R/W
0x50B	PLL_RXDIVRATE	[7:4]	RESERVED	Reserved.	0x0	R
		[3:0]	RXDIVRATE_JTX_PLL_RC	When refindivovd is 1, sets value for rx_divrate.	0x8	R/W
0x50C	PLL_VCO_TRIM	[7:6]	RESERVED	Reserved.	0x0	R
		[5:0]	VCORTRIM_JTX_PLL_RC	Trim code slaved to 6-bits in the bandgap.	0x0	R/W
0x50D	PLL_REFCLK_CPL	[7:2]	RESERVED	Reserved.	0x0	R
		1	SEL_REFINDIV3_JTX_PLL_RC	Enables additional /3 on input reference clock to PLL.	0x0	R/W
		0	SEL_REFCKDCACB_JTX_PLL_RC	Determines whether the reference clock input should be DC-coupled (1) or AC coupled (0)	0x1	R/W
0x50E	CBUS_REN_JTX_PLL	[7:1]	RESERVED	Reserved.	0x0	R
		0	CBUS_REN_JTX_PLL_RC	Read enable for JTX_PLL registers.	0x0	R/W
0x50F	CBUS_WSTROBE_JTX_PLL	[7:1]	RESERVED	Reserved.	0x0	R
		0	CBUS_WSTROBE_JTX_PLL_RC	Write Strobe for JTX_PLL registers.	0x0	R/W
0x510	CKDIST_PD	[7:2]	RESERVED	Reserved.	0x0	R
		1	IDIST_PD_RC	Enable output clocks to serializer. 1 : Enable	0x0	R/W
		0	PD_PPF_DES_RC	Enable output clocks to serializer 1 : Enable	0x0	R/W
0x511	POLYPHASE_CTRL	[7:0]	TRIM_POLYPHASE_DES_RC	DESIGNER DEBUG: Polyphase control. DESIGNER DEBUG: Polyphase control: <6:5>: ppf_divm_od<1:0>, <4>: en_ppf_divm_od, <3:1>: inv_str_od<2:0>, <0>: en_inv_str_od.	0x2F	R/W
0x512	PLL_READ_FREQ4	[7:0]	VCOFREQBAND_JTX_PLL_RS[7:0]	VCO frequency control word that sets VCO frequency, 00: max. VCO frequency, 7FF: min. VCO frequency	0x0	R
0x513	PLL_READ_FREQ5	[7:3]	RESERVED	Reserved.	0x0	R
		[2:0]	VCOFREQBAND_JTX_PLL_RS[10:8]	VCO frequency control word that sets VCO frequency, 00: max. VCO frequency, 7FF: min. VCO frequency	0x0	R
0x514	PLL_PTAT_STARTUP	[7:0]	PTAT_STARTUP_JTX_PLL_RC	PTAT startup control.	0x0	R/W
0x515	PLL_PTAT_STARTUP_STATUS1	[7:1]	RESERVED	Reserved.	0x0	R
		0	PTAT_STARTUP_STATUS_RS1	PTAT startup status.	0x0	R
0x516	PLL_PTAT_STARTUP_STATUS2	[7:1]	RESERVED	Reserved.	0x0	R
		0	PTAT_STARTUP_STATUS_RS2	PTAT startup status.	0x0	R
0x517	PLL_TEMP	[7:1]	RESERVED	Reserved.	0x0	R
		0	TDEGCINIT_JTX_PLL_RC	Low-to-High transition activates on-chip temperature measurement.	0x0	R/W
0x51E	PLL_LOCK_CTL1	[7:4]	JTX_PLL_LOCK_DIVIDER[3:0]	PLL Lock counter.	0x0	R/W
		[3:1]	RESERVED	Reserved.	0x0	R
		0	JTX_PLL_LOCK_SEL	PLL lock and timer based lock select. Select between PLL lock signal and timer based lock signal generation	0x0	R/W
0x51F	PLL_LOCK_CTL2	[7:6]	RESERVED	Reserved.	0x0	R
		[5:0]	JTX_PLL_LOCK_DIVIDER[9:4]	PLL Lock counter.	0x0	R/W
0x520	CBUS_ADDR	[7:0]	CBUS_ADDR_JTX_PLL_RC	Control bus address select.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0x521	CBUS_WDATA	[7:0]	CBUS_WDATA_JTX_PLL_RC	Control Bus data,. Control Bus data, channel selected with cbus_wstrobe_ser signal	0x0	R/W
0x522	CBUS_RDATA	[7:0]	CBUS_RDATA_JTX_PLL_RS	Read back bus, channel selected bwith cbus_ren_ser.	0x0	R
0x523	REFCLK_CTRL	7	RESERVED	Reserved.	0x0	R
		[6:3]	SEL_REFCLK_RCVR_CM_CTRL	Synca for refclk.	0x0	R/W
		2	SEL_REFCLK_RCVR_LP_MODE_RC	Synca for refclk.	0x0	R/W
		1	SEL_SYNCA_FOR_REFCLK_RC	Synca for refclk.	0x0	R/W
		0	EN_REFCLK_RCVR_RC	Synca for refclk.	0x1	R/W
0x524	JTX_PLL_REV_ID_RS	[7:0]	JTX_PLL_REV_ID_RS	Read back bus, channel selected bwith cbus_ren_ser.	0x0	R
0xB90	POWER_DOWN_REG	7	EN_CAL_ANA	Enable Calibration Analog Blocks, Set to 0 for Power-down.	0x0	R/W
		6	EN_CAL_CLK	Enable Calibration Clock and Digital Blocks, Set to 0 for Power-down.	0x0	R/W
		5	EN_34	Enable Additional Two Signal Channels for 3dB Noise Improvement.	0x0	R/W
		[4:3]	PIN_PD_MODE	Power down mode. 00: power down pin disabled. 01: power down pin disables clock path only. 10: power down pin disables adc clock and vti bias. 11: power down pin disables adc clock, vti bias and adc masterbias block.	0x0	R/W
		2	EN_BIAS	Enable for Adc Bias Block, Set to 0 for Power-down.	0x0	R/W
		1	EN_ADCCLK	Enable Channel I Adc Clock, Set to 0 for Power-down.	0x0	R/W
		0	EN_VTI	Enable Channel I Analog Front End, Set to 0 for Power-down.	0x0	R/W
0xB91	ENABLE_CH7_0_REG	7	EN_ADC7	Enable for Channel 7 Adc Clock.	0x0	R/W
		6	EN_ADC6	Enable for Channel 6 Adc Clock.	0x0	R/W
		5	EN_ADC5	Enable for Channel 5 Adc Clock.	0x0	R/W
		4	EN_ADC4	Enable for Channel 4 Adc Clock.	0x0	R/W
		3	EN_ADC3	Enable for Channel 3 Adc Clock.	0x0	R/W
		2	EN_ADC2	Enable for Channel 2 Adc Clock.	0x0	R/W
		1	EN_ADC1	Enable for Channel 1 Adc Clock.	0x0	R/W
		0	EN_ADC0	Enable for Channel 0 Adc Clock.	0x0	R/W
0xB92	ENABLE_CH15_8_REG	7	EN_ADC15	Enable for Channel 15 Adc Clock.	0x0	R/W
		6	EN_ADC14	Enable for Channel 14 Adc Clock.	0x0	R/W
		5	EN_ADC13	Enable for Channel 13 Adc Clock.	0x0	R/W
		4	EN_ADC12	Enable for Channel 12 Adc Clock.	0x0	R/W
		3	EN_ADC11	Enable for Channel 11 Adc Clock.	0x0	R/W
		2	EN_ADC10	Enable for Channel 10 Adc Clock.	0x0	R/W
		1	EN_ADC9	Enable for Channel 9 Adc Clock.	0x0	R/W
		0	EN_ADC8	Enable for Channel 8 Adc Clock.	0x0	R/W
0xB94	VTI_GAIN_REG	[7:6]	RESERVED	Reserved	0x0	R
		[5:0]	BGAIN	Bgain Adjustment.	0x0	R/W
0xB95	VTI_LPF_CAP_REG	[7:6]	RESERVED	Reserved	0x0	R
		[5:0]	BCAP	Bcap Adjustment.	0x0	R/W
0xB99	DITHER_DAC_CURRENT1_REG	[7:0]	BDITHDAC1	Bdither DAC1.	0x0	R/W
0xB9A	DITHER_DAC_CURRENT2_REG	[7:0]	BDITHDAC2	Bdither DAC2.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0xBA2	VTI_SHIFT_CURRENT_ MSB_REG	7	SPARE_REG_12_7	(vti_force_cm): 0 = vti normal mode, 1= vti input common-mode is forced by input.	0x0	R/W
		6	SPARE_REG_12_6	(vti_high_imp): 0 = vti normal mode, 1= vti input common-mode is high impedance.	0x0	R/W
		[5:4]	RTERM	Termination Resistance. 00: Open. 01: 200 Ohm. 10: 100 Ohm.	0x0	R/W
		[3:0]	RESERVED	Reserved.	0x0	R/W
0xBB3	CAL_EN	7	ENABLE_CLOCK	Clock Enable for the VCO ADC Digital.	0x0	R/W
		[6:0]	RESERVED	Reserved.	0x0	R/W
0xBBA	KGAIN_VAL0	[7:0]	KGAIN_VAL[7:0]	floor(kgain) – (2^8)*Kgain1 – (2^16)*Kgain2	0x0	R/W
0xBBB	KGAIN_VAL1	[7:0]	KGAIN_VAL[15:8]	floor(kgain/2^8) – (2^8)*Kgain2	0x0	R/W
0xBBC	KGAIN_VAL2	[7:6]	RESERVED	Reserved.	0x0	R
		[5:0]	KGAIN_VAL[21:16]	floor(kgain/2^16)	0x0	R/W
0xBC3	BCENTER_1	[7:2]	BCENTER_OFFSET	Offset Value for Bcenter.	0x0	R/W
		[1:0]	RESERVED[9:8]	Reserved.	0x0	R
0xBC8	DIVM_RC	[7:0]	DIVM_RC	Wait Time for C Measurement. Valid range is 125-255. This multiplied by the fs/8 clock period determines the time between falling edge of C_RESET to falling edge of C_CLK for C ramp.	0x0	R/W
Temperature Diode Control Registers						
0xC01	TRM_TEMP_DIODE	[7:0]	TRM_TEMP_DIODE	00: Default. 11: Temp sensor: Enable sense 1x and 20x diode voltages.	0x0	R/W
0xC04	TOP_REF_MONITOR	[7:4]	RESERVED	Reserved.	0x0	R
		[3:2]	SPI_SEL_MON_TEMP	00: Default. 01: Temp Sensor: measure 1x diode (also set trm_temp_diode[7:0] = 3). 10: Temp sensor: measure 20x diode (also set trm_temp_diode[7:0] = 3). 11: Temp sensor: measure GND.	0x0	R/W
		[1:0]	RESERVED	Reserved.	0x0	R/W
On-Chip PLL Configuration Registers						
0xD02	RESET_REG	[7:2]	RESERVED	Reserved.	0x0	R
		1	D_CAL_RESET	Resets Vco Calibration. Rising edge starts VCO momcap calibration.	0x0	R/W
		0	RESERVED	Reserved.	0x0	R/W
0xD03	INPUT_MISC_REG	[7:2]	RESERVED	Reserved.	0x4	R
		[1:0]	D_REFIN_DIV	Programmable Predivider Value (1,2,3,4) (Also called /R in some documentation). 00: /1. 01: /2. 10: /3. 11: /4.	0x0	R/W
0xD04	CHARGEPUMP_REG_0	[7:6]	RESERVED	Reserved.	0x0	R/W
		[5:0]	D_CP_CURRENT	Charge Pump Current	0x13	R/W
0xD09	DIVIDER_REG	[7:6]	RESERVED	Reserved.	0x0	R/W
		[5:0]	D_DIVIDE_CONTROL	Programmable Divide by N Value (2-50)	0x6	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
0xD0C	VCO_CAL_LOCK_REG	[7:6]	RESERVED	Reserved.	0x0	R
		[5:4]	D_CONTROL_HS_FB_DIV	Hs Feedback Divider (/P) 00: /5. 01: /7. 10: /8. 11: /11.	0x2	R/W
		[3:0]	RESERVED	Reserved.	0x6	R
0xD21	FILT_MAIN_0	[7:6]	RESERVED	Reserved.	0x0	R
		[5:0]	D_FILT_CBIG	the large capacitor in filter: .5pF + 9.5pF*N (0<N<63).	0x20	R/W
0xD22	FILT_MAIN_1	[7:0]	D_FILT_R	the resistor control for filter: nonlinear. R = 31k ohm/(1+!<0>+2*!<1>+4*!<2>+8*!<3>+16*!<4>+32*!<5>+64*!<6>+128*!<7>, or Resistor_code = 256 - 31k/R (123 < R <31k).	0xFA	R/W
0xD23	FILT_MAIN_2	[7:6]	RESERVED	Reserved.	0x0	R
		[5:0]	D_FILT_CSMALL	the small capacitor in filter. .83pF+.87pF*M (0<M<63).	0x22	R/W
0xD40	CLOCK_PD	[7:4]	RESERVED	Reserved.	0x0	R
		3	SPI_PLL_BYP	Bypass On-chip PLL.	0x0	R/W
		[2:0]	RESERVED	Reserved.	0x0	R/W
0xD41	CLOCK_DIVIDER_CNTRL	[7:5]	RESERVED	Reserved.	0x0	R
		[4:3]	SPI_CNTRL_HS_DIV	Select Divider for Vco Outputs. 00: /6. 01: /8. 10: /10. 11: Not supported.	0x0	R/W
		[2:0]	RESERVED	Reserved.	0x7	R/W
0xD44	Clock_PLL_READY_CNTRL	[7:5]	RESERVED	Reserved.	0x0	R
		4	SPI_OUTOFLOCK_RST	Reset F/F for Slow Lock Coming Out of Lock.	0x0	R/W
		3	SPI_LOCK_VALID_RST	Reset F/F for Slow Lock Valid Signal.	0x0	R/W
		2	PLL_OUTOFLOCK	1: Lock Slow Transitioned Low (PLL Out of Lock); Once the PLL is in lock, if the PLL goes out of lock (output "pll_lock_slow" transitions low), pll_outoflock will transition high and stay high until spi_outoflock_rst is set high then low.	0x0	R
		1	PLL_LOCK_VALID	1: Lock Slow Transitioned High (PLL in Lock); Once the PLL achieves lock (output "pll_lock_slow" transitions high), pll_lock_valid will transition high and stay high until spi_lock_valid_rst is set high then low.	0x0	R
		0	RESERVED	Reserved.	0x0	R
0xD4A	JTX_PLL_REFCLK_DIV	[7:6]	RESERVED	Reserved.	0x0	R
		[5:0]	SPI_DIV_JTX_PLL	Adjust Divider for Refclk to JTX_PLL. 00000: NC. 00001: NC. 00010: /2. 00011: /3. 00100: /4. 00101: /5. 00110: /6. 00111: /7. 01000: /8. 01001: /9.	0x2	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
				01010: /10. 01011: /11. 01100: /12. 01101: /13. 01110: /14. 01111: /15. 10000: /16. 10001: /17. 10010: /18. 10011: /19. 10100: /20. 10101: /21. 10110: /22. 10111: /23. 11000: /24. 11001: /25. 11010: /26. 11011: /27. 11100: /28. 11101: /29. 11110: /30. 11111: /31.		
0xD4D	SYSREF_IGNORE	7	RESERVED	Reserved.	0x0	R
		6	SPI_SYSREF_IGNORE_START	Start ignoring sysrefs. This bit will self clear once count expires. The first posedge of sysref after the start is passed through, thereafter they are masked until ignore count expires. The bit will self-clear once masking is over.	0x0	R/W
		5	SPI_SYSREF_IGNORE_ENABLE	Master enable for sysref_ignore block. This also acts as a clock gating signal for the FFs in the block.	0x0	R/W
		[4:1]	SPI_SYSREF_IGNORE_COUNT	Number of sysrefs to ignore. Value to be programmed is N-1, e.g. 0 will ignore 1 sysref, 0xF will ignore 16 sysrefs.	0x0	R/W
		0	SPI_SYSREF_DISABLE	Master disable for sysref, asynchronous – can affect duty cycle of sysref edge closest to bit transition.	0x0	R/W
G/H Sync Mode Control Registers						
0xE20	TRIGGER_DELAY_VAL_0	[7:0]	TRIGGER_DELAY	Delay in Trigger Pulse in terms of cic_clk cycles. This delay is a common delay for all path.	0x0	R/W
0xE21	TRIGGER_DELAY_VAL_1	[7:0]	I_TRIGGER_DELAY	Hardware computed value of Delay in Trigger Pulse in terms of cic_clk cycles. This delay is a common delay for all path.	0x0	R
0xE24	G_H_SYNC_MODE_VAL	[7:5]	RESERVED	Reserved.	0x0	R
		4	TRIG_NCO_RESET_EN	Enable/Disable for NCO Reset Based on G/H Trig. 1-Enables periodic reset of NCO based on G/H Trig. Upon the arrival of G/H Trig NCO resets are periodically generated at the period of "H". 0-Disables NCO reset based on G/H Trig.	0x0	R/W
		3	RESERVED	Reserved.	0x0	R
		2	DELAY_AUTO_INCR	Auto Increment Trigger Delay after each trigger out for calibration purpose.	0x0	R/W

Addr.	Name	Bits	Bit Name	Description	Reset	Access
		[1:0]	G_H_SYNC_MODE	Mode Selection for G H Sync. 00: Sysref Based Synchronization. 01: Trigger Based Synchronization with exclusive trigger. 10: Trigger Based Synchronization with sysref repurposed. 11: Direct Pulse Mode.	0x0	R/W
0xE25	G_H_SYNC_SYSREF_ FUNC_VAL	[7:1]	RESERVED	Reserved.	0x0	R
		0	SYSREF_FUNC	Flag for Sysref Function for Mode 2 with sysref repurposed.	0x0	R/W
0xE26	TRIG_AVG_DELAY_VAL	[7:0]	AVERAGER_DELAY	Moving Averager Strobe Delay in terms of number of clock cycles of cic_clk. Indicates the amount of delay to be incurred on the strobe for moving averager. Strobe is initiated by G/H trig, and this register indicates the amount of delay on that strobe.	0xE	R/W
0xE27	TRIG_AVG_DELAY_G_V AL	[7:0]	AVERAGER_G_DELAY	Moving Averager Strobe Delay to account for G value in terms of cic_clk cycles.	0x0	R/W
0xE28	TRIG_NCO_DELAY_VAL	[7:0]	NCO_DELAY	NCO Strobe/Reset Delay in terms of cic_clk cycles. Indicates the amount of delay to be incurred on the strobe/Reset for NCO. Strobe is initiated by G/H trig, and this register indicates the amount of delay on that strobe for NCO.	0x0	R/W
0xE30	TRIG_DELAY_OVERWRI TE	[7:4]	RESERVED	Reserved.	0x0	R
		3	OVERWRITE_TRIGGER_DELAY	1: Overwrite the TRIGGER delay 0 : Don't overwrite the delay value.	0x0	R/W
		2	OVERWRITE_NCO_DELAY	1: Overwrite the NCO delay 0 : Don't overwrite the delay value.	0x0	R/W
		1	OVERWRITE_AVERAGER_ DELAY	1: Overwrite the Averager delay 0 : Don't overwrite the delay value.	0x0	R/W
		0	OVERWRITE_AVERAGER_G_ DELAY	1: Overwrite the Averager G delay 0 : Don't overwrite the delay value.	0x0	R/W

APPLICATIONS INFORMATION

EVALUATION BOARD INFORMATION

For information regarding the AD9083 evaluation board, visit https://wiki.analog.com/resources/eval/ad9083.

POWER DELIVERY NETWORK

The power supplies needed to power the AD9083 are shown in Table 31.

Table 31. Typical Power Supplies for AD9083

Domain	Voltage (V)	Tolerance (%)
AVDD	1.0	±5
AVDD1P8	1.8	±5
DVDD	1.0	±5
DVDD1P8	1.8	±5

The evaluation board uses the power delivery network shown in Figure 93. Ferrite beads are used to isolate each of the supply domains. The ferrite beads are sized to limit the IR drop across it such that the ±5% regulation specification can still be maintained. The DVDD supply does not use a ferrite due to its high current draw.

The AD9083 can be driven directly from the dc-to-dc converter. Note that this approach has risks in that more power supply noise could be injected into the power supply domains of the ADC. To minimize noise, follow the layout guidelines of the dc-to-dc converter.

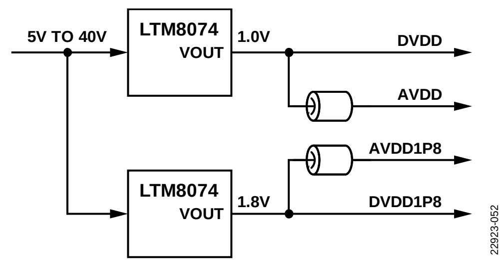

Figure 93. Simplified Power Solution for the AD9083

The user can employ several different decoupling capacitors to cover both high and low frequencies. These capacitors must be located close to the point of entry at the PCB level and close to the devices, with minimal trace lengths.

LAYOUT GUIDELINES

The ADC evaluation board can be used as a guide to follow good layout practices. The evaluation board layout is done in such a way as to

- Minimize coupling between the analog inputs.
- Minimize clock coupling to the analog inputs.
- Provide enough power and ground planes for the various supply domains while reducing cross coupling.
- Provide adequate thermal relief to the ADC.

Figure 94 shows the overall layout scheme used for the AD9083 evaluation board.

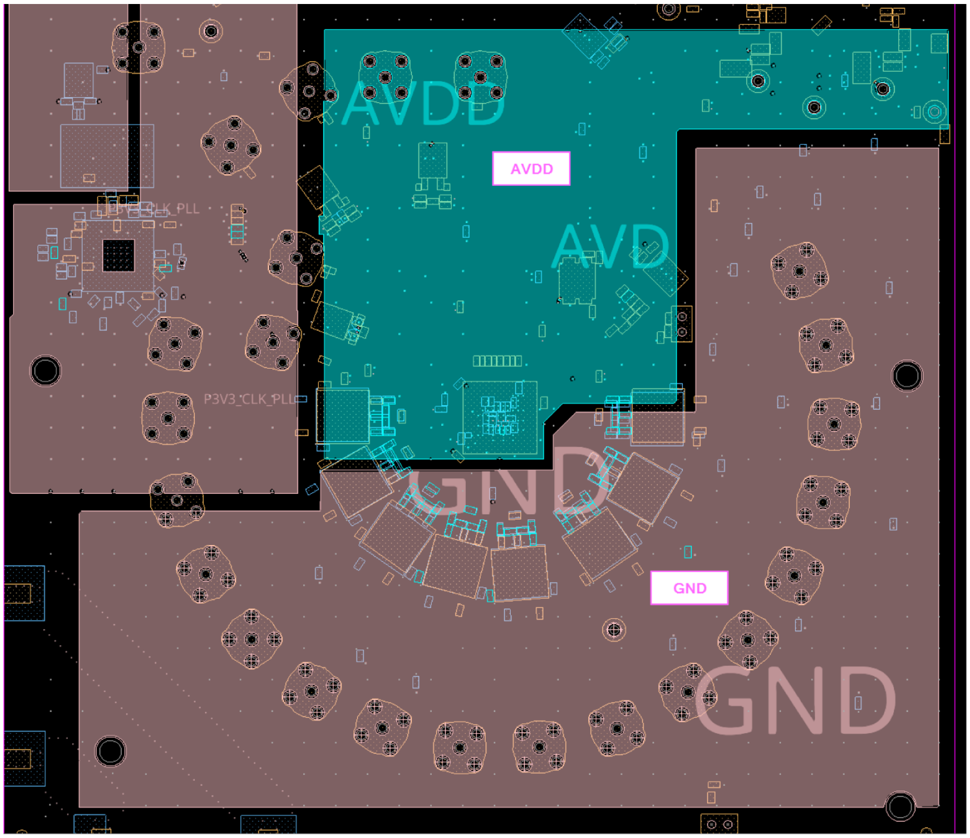

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Figure 94. AD9083EBZ Layout Showing AVDD Plane (Layer 3)

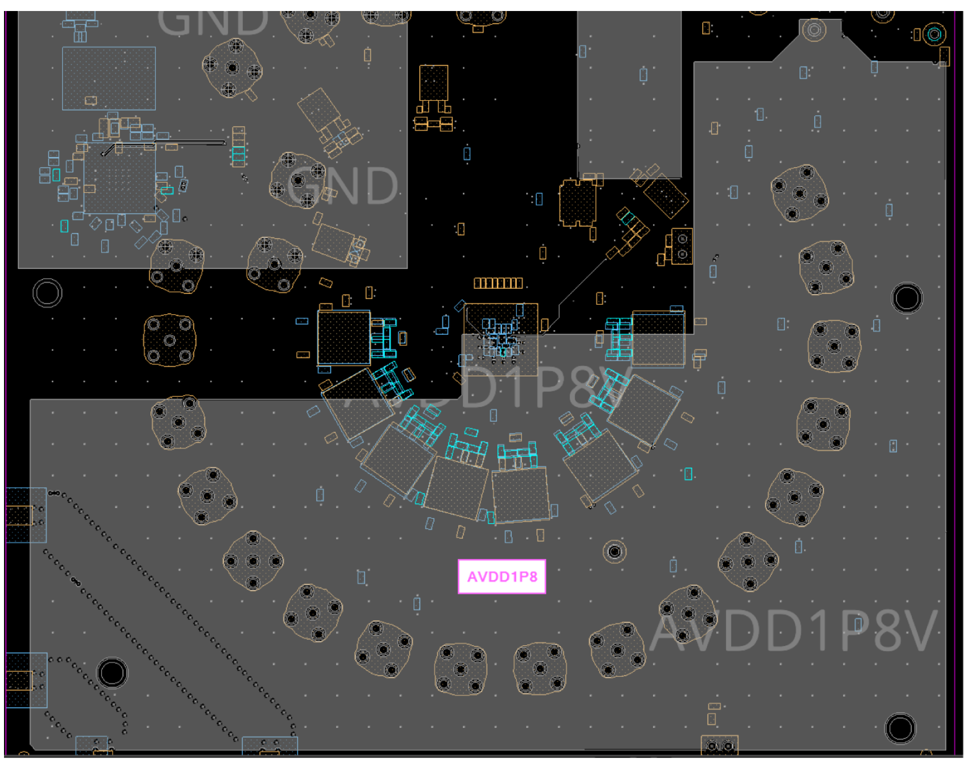

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Figure 95. AD9083EBZ Layout Showing AVDD1P8 Plane (Layer 4)

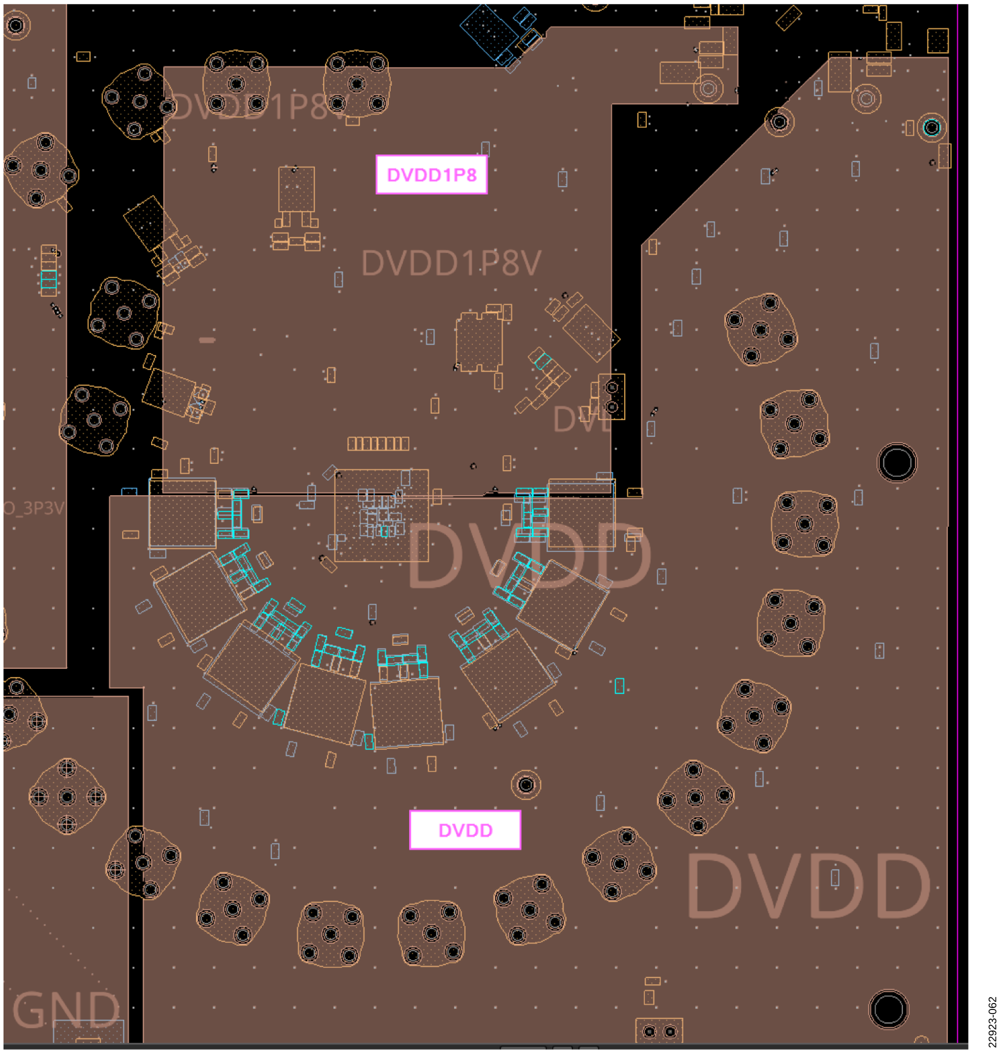

Figure 96. AD9083EBZ Layout Showing DVDD and DVDD1P8 Planes (Layer 6)

OUTLINE DIMENSIONS

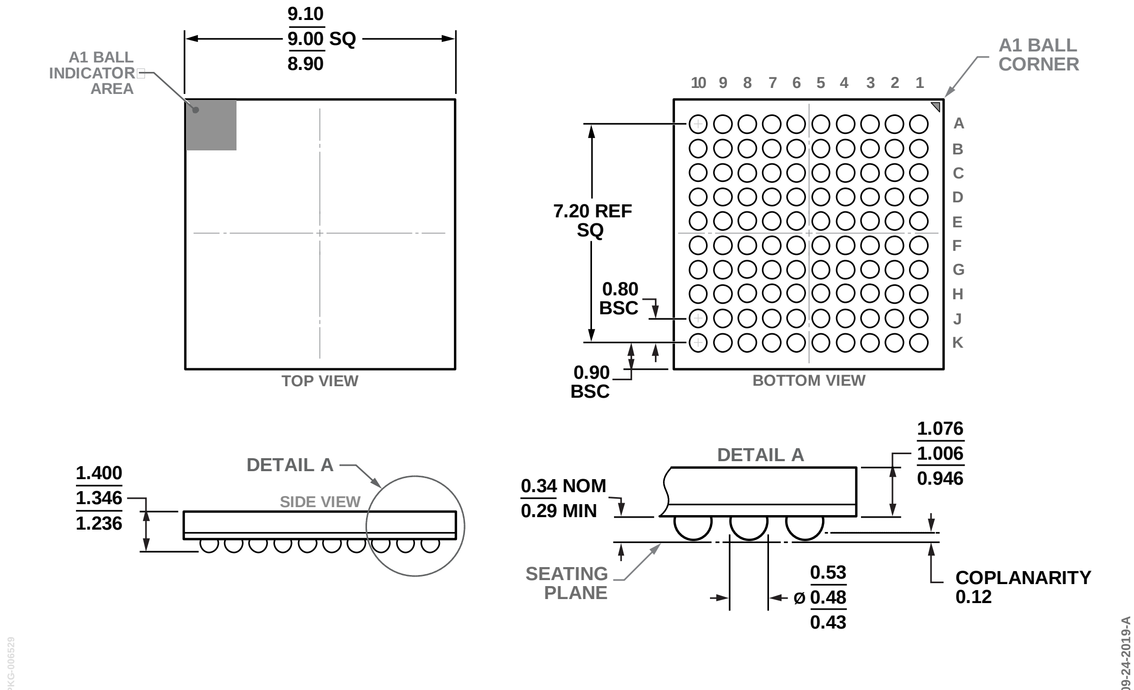

Figure 97. 100-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-100-8) Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range[2]	Package Description	Package Option
AD9083BBCZ	−40°C to +115°C	100-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC−100−8
AD9083BBCZ-RL7	−40°C to +115°C	100-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC−100−8
AD9083EBZ		Evaluation board for AD9083	

[1] Z = RoHS Compliant Part
[2] Specified T_J start-up at T_J = 40°C is guaranteed.