Dual, 11-/16-Bit, 2.8 GSPS, TxDAC+® Digital-to-Analog Converters

Data Sheet **AD9135/AD9136**

FEATURES

- Support input data rate >2 GSPS
- Proprietary low spurious and distortion design
  - SFDR = 82 dBc at dc IF, −9 dBFS
  - Flexible 8-lane JESD204B interface
- Multiple chip synchronization
  - Fixed latency
  - Data generator latency compensation
- Selectable 1×, 2×, 4×, or 8× interpolation filter
  - Low power architecture
- Transmit enable function allows extra power saving and instant control of the output status
- High performance, low noise phase-locked loop (PLL) clock multiplier
- Digital inverse sinc filter
- Low power: 1.42 W at 1.6 GSPS full operating conditions
- 88-lead LFCSP with exposed pad

APPLICATIONS

- Wireless communications
  - 3G/4G W-CDMA base stations
  - Wideband repeaters
  - Software defined radios
- Wideband communications
  - Point to point
  - Local multipoint distribution service (LMDS) and multichannel multipoint distribution service (MMDS)
- Transmit diversity, multiple input/multiple output (MIMO)
- Instrumentation
- Automated test equipment

TYPICAL APPLICATION CIRCUIT

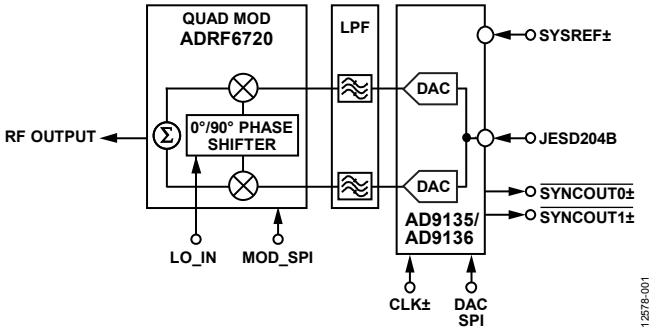

Figure 1.

GENERAL DESCRIPTION

The AD9135/AD9136 are dual, 11-/16-bit, high dynamic range digital-to-analog converters (DACs) that provide a maximum sample rate of 2800 MSPS, permitting a multicarrier generation over a very wide bandwidth. The DAC outputs are optimized to interface seamlessly with the ADRF6720, as well as other analog quadrature modulators (AQMs) from Analog Devices, Inc. An optional 3-wire or 4-wire serial port interface (SPI) provides for programming/readback of many internal parameters. The full-scale output current can be programmed over a typical range of 13.9 mA to 27.0 mA. The AD9135/AD9136 are available in an 88-lead LFCSP.

PRODUCT HIGHLIGHTS

1. Greater than 2 GHz, ultrawide complex signal bandwidth enables emerging wideband and multiband wireless applications.
2. Advanced low spurious and distortion design techniques provide high quality synthesis of wideband signals from baseband to high intermediate frequencies.
3. JESD204B Subclass 1 support simplifies multichip synchronization in software and hardware design.
4. Fewer pins for data interface width with a serializer/deserializer (SERDES) JESD204B eight-lane interface.
5. Programmable transmit enable function allows easy design balance between power consumption and wake-up time.
6. Small package size with 12 mm × 12 mm footprint.

Rev. D
Document Feedback

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FUNCTIONAL BLOCK DIAGRAM

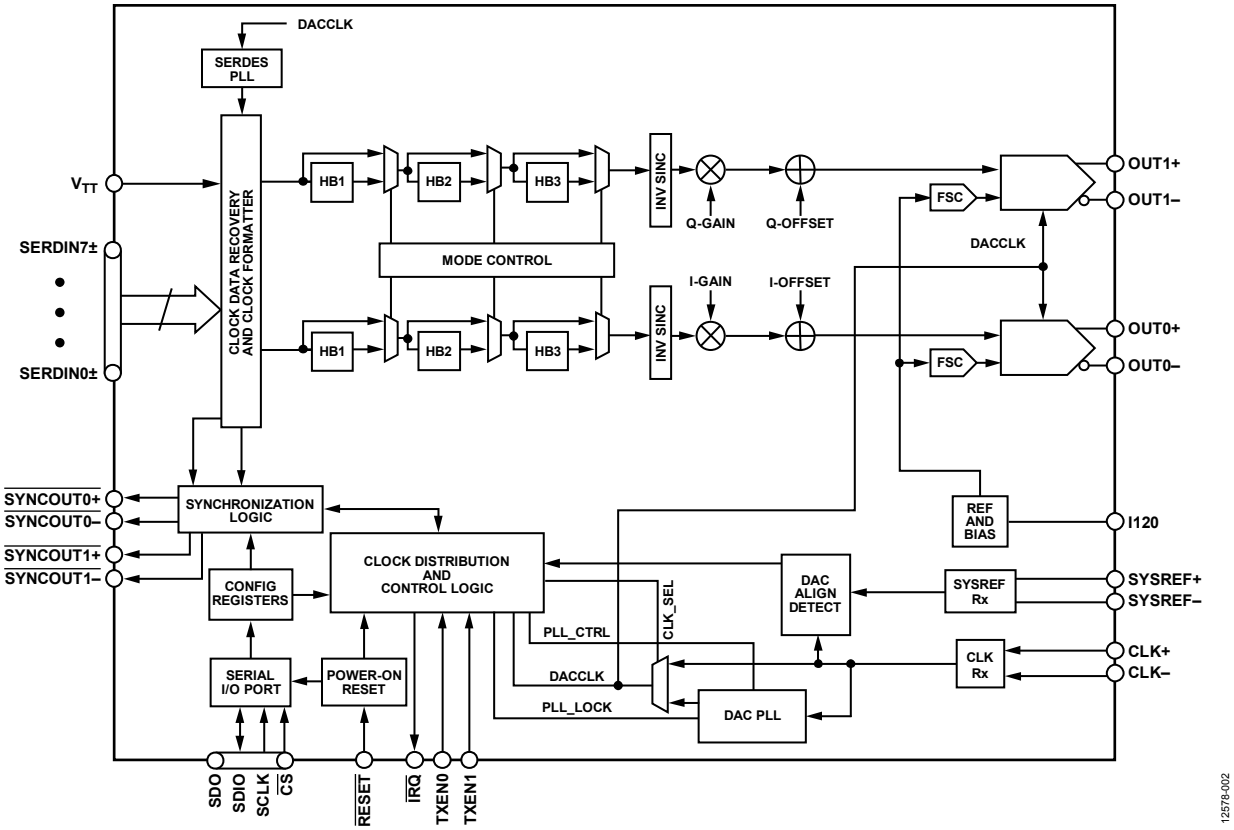


Figure 2.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 1.

		AD9135			AD9136			
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION			11			16		Bits
ACCURACY	With calibration							
Differential Nonlinearity (DNL)			±0.175			±1.0		LSB
Integral Nonlinearity (INL)			±0.35			±2.0		LSB
MAIN DAC OUTPUTS								
Gain Error	With internal reference	−2.5	+2	+5.5	−2.5	+2	+5.5	% FSR
I/Q Gain Mismatch		−0.6		+0.6	−0.6		+0.6	% FSR
Full-Scale Output Current (I_{OUTFS})	Based on a 4 kΩ external resistor between I120 and GND							
Maximum Setting		25.5	27.0	28.6	25.5	27.0	28.6	mA
Minimum Setting		13.1	13.9	14.8	13.1	13.9	14.8	mA
Output Compliance Range		−250		+750	−250		+750	mV
Output Resistance			0.2			0.2		MΩ
Output Capacitance			3.0			3.0		pF
Gain DAC Monotonicity			Guaranteed			Guaranteed		
Settling Time	To within ±0.5 LSB		20			20		ns
MAIN DAC TEMPERATURE DRIFT								
Offset			0.04			0.04		ppm
Gain			32			32		ppm/°C
REFERENCE								
Internal Reference Voltage			1.2			1.2		V
ANALOG SUPPLY VOLTAGES								
AVDD33		3.13	3.3	3.47	3.13	3.3	3.47	V
PVDD12		1.14	1.2	1.26	1.14	1.2	1.26	V
CVDD12		1.14	1.2	1.26	1.14	1.2	1.26	V
DIGITAL SUPPLY VOLTAGES								
SIOVDD33		3.13	3.3	3.47	3.13	3.3	3.47	V
V_{TT}		1.1	1.2	1.37	1.1	1.2	1.37	V
DVDD12	1.2 V nominal supply voltage	1.14	1.2	1.26	1.14	1.2	1.26	V
	1.3 V nominal supply voltage	1.274	1.3	1.326	1.274	1.3	1.326	V
SVDD12	1.2 V nominal supply voltage	1.14	1.2	1.26	1.14	1.2	1.26	V
	1.3 V nominal supply voltage	1.274	1.3	1.326	1.274	1.3	1.326	V
IOVDD		1.71	1.8	3.47	1.71	1.8	3.47	V
POWER CONSUMPTION								
1× Interpolation Mode, JESD Mode 8, 8 SERDES Lanes	f_{DAC} = 1.6 GSPS, IF = 40 MHz, PLL on, digital gain on, inverse sinc on, DAC full-scale current (I_{OUTFS}) = 20 mA		1.42	1.74		1.42	1.74	W
AVDD33			68	73		68	73	mA
PVDD12			100	113.4		100	113.4	mA
CVDD12			101	112		101	112	mA
SVDD12	Includes V_{TT}		554	665		554	665	mA
DVDD12			196	224		196	224	mA
SIOVDD33			11	12		11	12	mA
IOVDD			36	50		36	50	µA

DIGITAL SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS INPUT LOGIC LEVEL						
Input Voltage (V_{IN}) Logic						
High		1.8 V ≤ IOVDD ≤ 3.3 V	0.7 × IOVDD			V
Low		1.8 V ≤ IOVDD ≤ 3.3 V			0.3 × IOVDD	V
CMOS OUTPUT LOGIC LEVEL						
Output Voltage (V_{OUT}) Logic						
High		1.8 V ≤ IOVDD ≤ 3.3 V	0.75 × IOVDD			V
Low		1.8 V ≤ IOVDD ≤ 3.3 V			0.25 × IOVDD	V
MAXIMUM DAC UPDATE RATE[1]						
		1× interpolation[2] (see Table 4)	2120			MSPS
		2× interpolation[2]	2120			MSPS
		4× interpolation[3]	2800			MSPS
		8× interpolation[3]	2800			MSPS
ADJUSTED DAC UPDATE RATE						
		1× interpolation	2120			MSPS
		2× interpolation	1060			MSPS
		4× interpolation	700			MSPS
		8× interpolation	350			MSPS
INTERFACE[4]						
Number of JESD204B Lanes				8		Lanes
JESD204B Serial Interface Speed						
Minimum		Per lane			1.44	Gbps
Maximum		Per lane, SVDD12 = 1.3 V ± 2%	12.4			Gbps
DAC CLOCK INPUT (CLK+, CLK−)						
Differential Peak-to-Peak Voltage			400	1000	2000	mV
Common-Mode Voltage		Self biased input, ac-coupled		600		mV
Maximum Clock Rate			2800			MHz
REFCLK[5] Frequency (PLL Mode)		6.0 GHz ≤ f_{VCO} ≤ 12.0 GHz	35		1000	MHz
SYSTEM REFERENCE INPUT (SYSREF+, SYSREF−)						
Differential Peak-to-Peak Voltage			400	1000	2000	mV
Common-Mode Voltage			0		2000	mV
SYSREF± Frequency[6]					$f_{DATA}/(K \times S)$	Hz
SYSREF SIGNAL TO DAC CLOCK[7]		SYSREF differential swing = 0.4 V, slew rate = 1.3 V/ns, common modes tested: ac-coupled, 0 V, 0.6 V, 1.25 V, 2.0 V				
Setup Time	t_{SSD}		131			ps
Hold Time	t_{HSD}		119			ps
Keep Out Window	KOW			20		ps
SPI						
Maximum Clock Rate	SCLK	IOVDD = 1.8 V	10			MHz
Minimum SCLK Pulse Width						
High	t_{PWH}				8	ns
Low	t_{PWL}				12	ns
SDIO to SCLK						
Setup Time	t_{DS}		5			ns
Hold Time	t_{DH}		2			ns

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SDO to SCLK						
Data Valid Window	t_{DV}		25			ns
$\overline{CS}$ to SCLK						
Setup Time	$t_{S\overline{CS}}$		5			ns
Hold Time	$t_{H\overline{CS}}$		2			ns

[1] See Table 3 for detailed specifications for DAC update rate conditions.
[2] The maximum speed for 1× and 2× interpolation is limited by the JESD204B interface with increased supply levels. See Table 4 for details.
[3] The maximum speed for 4× and 8× interpolation is limited by the DAC core. See Table 4 for details.
[4] See Table 4 for detailed specifications for JESD204B speed conditions.
[5] REFCLK is the reference clock.
[6] K, F, and S are JESD204B transport layer parameters. See Table 43 for the full definitions.
[7] See Table 5 for detailed specifications for SYSREF signal to DAC clock timing conditions.

MAXIMUM DAC UPDATE RATE SPEED SPECIFICATIONS BY SUPPLY

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
MAXIMUM DAC UPDATE RATE					
2×, 4×, and 8× Interpolation					
	DVDD12, CVDD12 = 1.2 V ± 5%	2.23			GSPS
	DVDD12, CVDD12 = 1.2 V ± 2%	2.41			GSPS
	DVDD12, CVDD12 = 1.3 V ± 2%	2.80			GSPS
1× Interpolation					
	DVDD12, CVDD12 = 1.2 V ± 5%	1.81			GSPS
	DVDD12, CVDD12 = 1.2 V ± 2%	1.93			GSPS
	DVDD12, CVDD12 = 1.3 V ± 2%	2.21			GSPS

JESD204B SERIAL INTERFACE SPEED SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
HALF RATE	SVDD12 = 1.2 V ± 5%	5.75		11.4	Gbps
	SVDD12 = 1.2 V ± 2%	5.75		12.0	Gbps
	SVDD12 = 1.3 V ± 2%	5.75		12.4	Gbps
FULL RATE	SVDD12 = 1.2 V ± 5%	2.88		5.98	Gbps
	SVDD12 = 1.2 V ± 2%	2.88		6.06	Gbps
	SVDD12 = 1.3 V ± 2%	2.88		6.2	Gbps
OVERSAMPLING	SVDD12 = 1.2 V ± 5%	1.44		3.0	Gbps
	SVDD12 = 1.2 V ± 2%	1.44		3.04	Gbps
	SVDD12 = 1.3 V ± 2%	1.44		3.1	Gbps

SYSREF SIGNAL TO DAC CLOCK TIMING SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, SYSREF± common-mode voltages = 0.0 V, 0.6 V, 1.25 V, and 2.0 V, unless otherwise noted.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYSREF DIFFERENTIAL SWING = 0.4 V, SLEW RATE = 1.3 V/ns					
Setup Time	AC-coupled		126		ps
	DC-coupled		131		ps
Hold Time	AC-coupled		92		ps
	DC-coupled		119		ps
SYSREF DIFFERENTIAL SWING = 0.7 V, SLEW RATE = 2.28 V/ns					
Setup Time	AC-coupled		96		ps
	DC-coupled		104		ps
Hold Time	AC-coupled		77		ps
	DC-coupled		95		ps
SYSREF SWING = 1.0 V, SLEW RATE = 3.26 V/ns					
Setup Time	AC-coupled		83		ps
	DC-coupled		90		ps
Hold Time	AC-coupled		68		ps
	DC-coupled		84		ps

DIGITAL INPUT DATA TIMING SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = 25°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 6.

Parameter	Min	Typ	Max	Unit
LATENCY				
Interface		17		PClock[1] cycles
Interpolation				
1×		66		DAC clock cycles
2×		137		DAC clock cycles
4×		251		DAC clock cycles
8×		484		DAC clock cycles
Inverse Sinc		17		DAC clock cycles
Digital Gain Adjust		12		DAC clock cycles
POWER-UP TIME		60		µs

[1] PClock is the AD9135/AD9136 internal processing clock and equals the lane rate ÷ 40.

LATENCY VARIATION SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = 25°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 7.

Parameter	Min	Typ	Max	Unit
DAC LATENCY VARIATION				
SYNC On				
PLL Off		0	1	DAC clock cycles
PLL On	−1		+1	DAC clock cycles

JESD204B INTERFACE ELECTRICAL SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V, V_{TT} = 1.2 V, T_A = −40°C to +85°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 8.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
JESD204B DATA INPUTS						
Input Leakage Current		T_A = 25°C				
Logic High		Input level = 1.2 V ± 0.25 V, V_{TT} = 1.2 V		10		µA
Logic Low		Input level = 0 V		−4		µA
Unit Interval	UI		94		714	ps
Common-Mode Voltage	V_{RCM}	AC-coupled, V_{TT} = SVDD12[1]	−0.05		+1.85	V
Differential Voltage	R_V_{DIFF}		110		1050	mV
V_{TT} Source Impedance	Z_{TT}	At dc			30	Ω
Differential Impedance	Z_{RDIFF}	At dc	80	100	120	Ω
Differential Return Loss	RL_{RDIF}			8		dB
Common-Mode Return Loss	RL_{RCM}			6		dB
DIFFERENTIAL OUTPUTS ($\overline{SYNCOUTx\pm}$)[2]						
Output Differential Voltage	V_{OD}					
Normal Swing Mode		Register 0x2A5[0] = 0	192		235	mV
High Swing Mode		Register 0x2A5[0] = 1	341		394	mV
Output Offset Voltage	V_{OS}		1.19		1.27	V
DETERMINISTIC LATENCY						
Fixed					17	PClock[3] cycles
Variable					2	PClock[3] cycles
SYSREF± to LOCAL MULTIFRAME COUNTER (LMFC) DELAY				4		DAC clock cycles

[1] As measured on the input side of the ac coupling capacitor.
[2] IEEE Standard 1596.3 LVDS compatible.
[3] PClock is an AD9135/AD9136 internal processing clock and equals the lane rate ÷ 40.

AC SPECIFICATIONS

AVDD33 = 3.3 V, SIOVDD33 = 3.3 V, IOVDD = 1.8 V, DVDD12 = 1.2 V, CVDD12 = 1.2 V, PVDD12 = 1.2 V, SVDD12 = 1.2 V,[1] V_{TT} = 1.2 V, T_A = 25°C, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 9.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)	−9 dBFS single-tone				
f_{DAC} = 983.04 MSPS	f_{OUT} = 20 MHz		82		dBc
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		76		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 20 MHz		81		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 170 MHz		69		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)	−9 dBFS				
f_{DAC} =983.04 MSPS	f_{OUT} = 20 MHz		90		dBc
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		82		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 20 MHz		90		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 170 MHz		81		dBc
NOISE SPECTRAL DENSITY (NSD), SINGLE-TONE	0 dBFS				
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		−162		dBm/Hz
f_{DAC} = 1966.08 MSPS	f_{OUT} = 150 MHz		−163		dBm/Hz
W-CDMA FIRST ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE-CARRIER	0 dBFS				
f_{DAC} = 983.04 MSPS	f_{OUT} = 30 MHz		82		dBc
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		80		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 150 MHz		80		dBc
W-CDMA SECOND ACLR, SINGLE-CARRIER	0 dBFS				
f_{DAC} = 983.04 MSPS	f_{OUT} = 30 MHz		84		dBc
f_{DAC} = 983.04 MSPS	f_{OUT} = 150 MHz		85		dBc
f_{DAC} = 1966.08 MSPS	f_{OUT} = 150 MHz		85		dBc

[1] SVDD12 = 1.3 V for all f_{DAC} = 1966.08 MSPS conditions in Table 9.

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
I120 to Ground	−0.3 V to AVDD33 + 0.3 V
SERDINx±, V_{TT}, $\overline{SYNCOUT1}$±/ $\overline{SYNCOUT0}$±, TXENx	−0.3 V to SIOVDD33 + 0.3 V
OUTx±	−0.3 V to AVDD33 + 0.3 V
SYSREF±	GND − 0.5 V to +2.5 V
CLK± to Ground	−0.3 V to PVDD12 + 0.3 V
$\overline{RESET}$, $\overline{IRQ}$, $\overline{CS}$, SCLK, SDIO, SDO to Ground	−0.3 V to IOVDD + 0.3 V
LDO_BYP1	−0.3 V to SVDD12 + 0.3 V
LDO_BYP2	−0.3 V to PVDD12 + 0.3 V
LDO24	−0.3 V to AVDD33 + 0.3 V
Ambient Operating Temperature (T_A)	−40°C to +85°C
Operating Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

The exposed pad (EPAD) must be soldered to the ground plane for the 88-lead LFCSP. The EPAD provides an electrical, thermal, and mechanical connection to the board.

Typical θ_{JA}, θ_{JB}, and θ_{JC} values are specified for a 4-layer JESD51-7 high effective thermal conductivity test board for leaded surface-mount packages. θ_{JA} is obtained in still air conditions (JESD51-2). Airflow increases heat dissipation, effectively reducing θ_{JA}. θ_{JB} is obtained following double-ring cold plate test conditions (JESD51-8). θ_{JC} is obtained with the test case temperature monitored at the bottom of the exposed pad.

Ψ_{JT} and Ψ_{JB} are thermal characteristic parameters obtained with θ_{JA} in still air test conditions.

Junction temperature (T_J) can be estimated using the following equations:

$$T_J = T_T + (\Psi_{JT} \times P)$$

or

$$T_J = T_B + (\Psi_{JB} \times P)$$

where:
T_T is the temperature measured at the top of the package.
P is the total device power dissipation.
T_B is the temperature measured at the board.

Table 11. Thermal Resistance

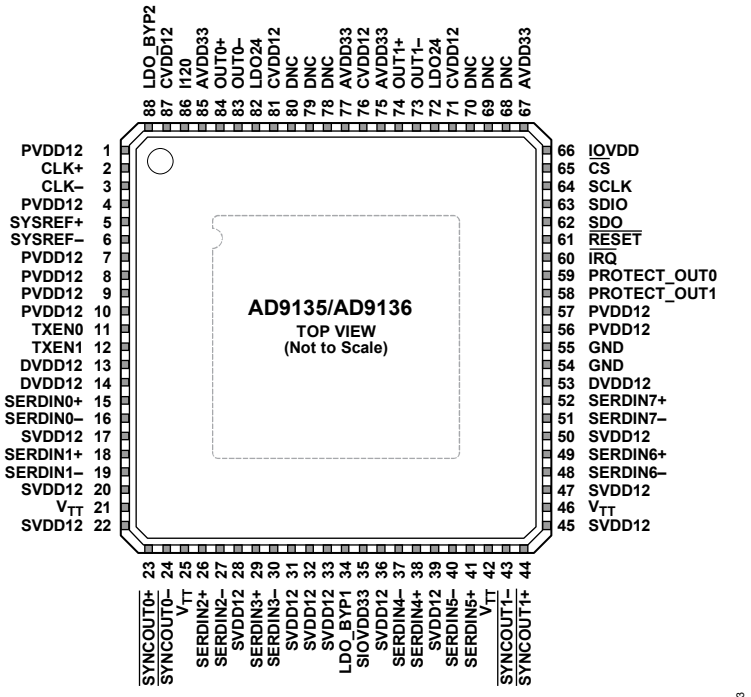
Package	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}	Unit
88-Lead LFCSP[1]	22.6	5.59	1.17	0.1	5.22	°C/W

[1] The exposed pad must be securely connected to the ground plane.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED PAD MUST BE SECURELY CONNECTED TO THE GROUND PLANE.

Figure 3. Pin Configuration

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
2	CLK+	PLL Reference/Clock Input, Positive. When the PLL is used, this pin is the positive reference clock input. When the PLL is not used, this pin is the positive device clock input. This pin is self biased and must be ac-coupled.
3	CLK–	PLL Reference/Clock Input, Negative. When the PLL is used, this pin is the negative reference clock input. When the PLL is not used, this pin is the negative device clock input. This pin is self biased and must be ac-coupled.
4	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
5	SYSREF+	Positive Reference Clock for Deterministic Latency. This pin is self biased for ac coupling. It can be ac-coupled or dc-coupled.
6	SYSREF–	Negative Reference Clock for Deterministic Latency. This pin is self biased for ac coupling. It can be ac-coupled or dc-coupled.
7	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
8	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
9	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
10	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
11	TXEN0	Transmit Enable for DAC0. CMOS levels are determined with respect to IOVDD.
12	TXEN1	Transmit Enable for DAC1. CMOS levels are determined with respect to IOVDD.
13	DVDD12	1.2 V Digital Supply.
14	DVDD12	1.2 V Digital Supply.
15	SERDIN0+	Serial Channel Input 0, Positive. CML compliant. SERDIN0+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
16	SERDIN0–	Serial Channel Input 0, Negative. CML compliant. SERDIN0– is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
17	SVDD12	1.2 V JESD204B Receiver Supply.
18	SERDIN1+	Serial Channel Input 1, Positive. CML compliant. SERDIN1+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.

Pin No.	Mnemonic	Description
19	SERDIN1−	Serial Channel Input 1, Negative. CML compliant. SERDIN1− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
20	SVDD12	1.2 V JESD204B Receiver Supply.
21	V_{TT}	1.2 V Termination Voltage. Connect V_{TT} to the SVDD12 supply pins.
22	SVDD12	1.2 V JESD204B Receiver Supply.
23	$\overline{\text{SYNCOUT0+}}$	Positive LVDS Sync (Active Low) Output Signal Channel Link 0.
24	$\overline{\text{SYNCOUT0−}}$	Negative LVDS Sync (Active Low) Output Signal Channel Link 0.
25	V_{TT}	1.2 V Termination Voltage. Connect V_{TT} to the SVDD12 supply pins.
26	SERDIN2+	Serial Channel Input 2, Positive. CML compliant. SERDIN2+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
27	SERDIN2−	Serial Channel Input 2, Negative. CML compliant. SERDIN2− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
28	SVDD12	1.2 V JESD204B Receiver Supply.
29	SERDIN3+	Serial Channel Input 3, Positive. CML compliant. SERDIN3+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
30	SERDIN3−	Serial Channel Input 3, Negative. CML compliant. SERDIN3− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
31	SVDD12	1.2 V JESD204B Receiver Supply.
32	SVDD12	1.2 V JESD204B Receiver Supply.
33	SVDD12	1.2 V JESD204B Receiver Supply.
34	LDO_BYP1	LDO SERDES Bypass. This pin requires a 1 Ω resistor in series with a 1 µF capacitor to ground.
35	SIOVDD33	3.3 V Supply for SERDES.
36	SVDD12	1.2 V JESD204B Receiver Supply.
37	SERDIN4−	Serial Channel Input 4, Negative. CML compliant. SERDIN4− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
38	SERDIN4+	Serial Channel Input 4, Positive. CML compliant. SERDIN4+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
39	SVDD12	1.2 V JESD204B Receiver Supply.
40	SERDIN5−	Serial Channel Input 5, Negative. CML compliant. SERDIN5− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
41	SERDIN5+	Serial Channel Input 5, Positive. CML compliant. SERDIN5+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
42	V_{TT}	1.2 V Termination Voltage. Connect V_{TT} to the SVDD12 supply pins.
43	$\overline{\text{SYNCOUT1−}}$	Negative LVDS Sync (Active Low) Output Signal Channel Link 1.
44	$\overline{\text{SYNCOUT1+}}$	Positive LVDS Sync (Active Low) Output Signal Channel Link 1.
45	SVDD12	1.2 V JESD204B Receiver Supply.
46	V_{TT}	1.2 V Termination Voltage. Connect V_{TT} to the SVDD12 supply pins.
47	SVDD12	1.2 V JESD204B Receiver Supply.
48	SERDIN6−	Serial Channel Input 6, Negative. CML compliant. SERDIN6− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
49	SERDIN6+	Serial Channel Input 6, Positive. CML compliant. SERDIN6+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
50	SVDD12	1.2 V JESD204B Receiver Supply.
51	SERDIN7−	Serial Channel Input 7, Negative. CML compliant. SERDIN7− is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
52	SERDIN7+	Serial Channel Input 7, Positive. CML compliant. SERDIN7+ is internally terminated to the V_{TT} pin voltage using a calibrated 50 Ω resistor. This pin is ac-coupled only.
53	DVDD12	1.2 V Digital Supply.
54	GND	Ground. Connect GND to the ground plane.
55	GND	Ground. Connect GND to the ground plane.
56	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
57	PVDD12	1.2 V Supply. PVDD12 provides a clean supply.
58	PROTECT_OUT1	Power Detection and Protection Pin Output for DAC1. Pin 58 is high when power protection is in process.
59	PROTECT_OUT0	Power Detection and Protection Pin Output for DAC0. Pin 59 is high when power protection is in process.
60	$\overline{\text{IRQ}}$	Interrupt Request (Active Low, Open Drain).

Pin No.	Mnemonic	Description
61	$\overline{\text{RESET}}$	Reset. This pin is active low. CMOS levels are determined with respect to IOVDD.
62	SDO	Serial Port Data Output. CMOS levels are determined with respect to IOVDD.
63	SDIO	Serial Port Data Input/Output. CMOS levels are determined with respect to IOVDD.
64	SCLK	Serial Port Clock Input. CMOS levels are determined with respect to IOVDD.
65	$\overline{\text{CS}}$	Serial Port Chip Select. This pin is active low. CMOS levels are determined with respect to IOVDD.
66	IOVDD	IOVDD Supply for CMOS Input/Output and SPI. Operational for 1.8 V ≤ IOVDD ≤ 3.3 V.
67	AVDD33	3.3 V Analog Supply for DAC Cores.
68	DNC	Do not connect to this pin.
69	DNC	Do not connect to this pin.
70	DNC	Do not connect to this pin.
71	CVDD12	1.2 V Clock Supply. Place bypass capacitors as near as possible to Pin 71.
72	LDO24	2.4 V LDO. Requires a 1 µF capacitor to ground.
73	OUT1−	DAC1 Negative Current Output.
74	OUT1+	DAC1 Positive Current Output.
75	AVDD33	3.3 V Analog Supply for DAC Cores.
76	CVDD12	1.2 V Clock Supply. Place bypass capacitors as near as possible to Pin 76.
77	AVDD33	3.3 V Analog Supply for DAC Cores.
78	DNC	Do not connect to this pin.
79	DNC	Do not connect to this pin.
80	DNC	Do not connect to this pin.
81	CVDD12	1.2 V Clock Supply. Place bypass capacitors as near as possible to Pin 81.
82	LDO24	2.4 V LDO. Requires a 1 µF capacitor to ground.
83	OUT0−	DAC0 Negative Current Output.
84	OUT0+	DAC0 Positive Current Output.
85	AVDD33	3.3 V Analog Supply for DAC Cores.
86	I120	Output Current Generation Pin for DAC Full-Scale Current. Tie a 4 kΩ resistor from the I120 pin to ground.
87	CVDD12	1.2 V Clock Supply. Place bypass capacitors as near as possible to Pin 87.
88	LDO_BYP2	LDO Clock Bypass for DAC PLL. This pin requires a 1 Ω resistor in series with a 1 µF capacitor to ground.
	EPAD	Exposed Pad. The exposed pad must be securely connected to the ground plane.

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Offset Error
Offset error is the deviation of the output current from the ideal of 0 mA. For OUTx+, 0 mA output is expected when all inputs are set to 0. For OUTx−, 0 mA output is expected when all inputs are set to 1.

Gain Error
Gain error is the difference between the actual and ideal output span. The actual span is determined by the difference between the output when the input is at its minimum code and the output when the input is at its maximum code.

Output Compliance Range
The output compliance range is the range of allowable voltages at the output of a current output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Offset drift is a measure of how far from full-scale range (FSR) the DAC output current is at 25°C (in ppm). Gain drift is a measure of the slope of the DAC output current across its full ambient operating temperature range, T_A (in ppm/°C).

Power Supply Rejection (PSR)
PSR is the maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the peak amplitude of the output signal and the peak spurious signal within the dc to Nyquist frequency of the DAC. Typically, energy in this band is rejected by the interpolation filters. This specification, therefore, defines how well the interpolation filters work and the effect of other parasitic coupling paths on the DAC output.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Interpolation Filter
If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed that has a sharp transition band near $f_{DATA}/2$. Images that typically appear around f_{DAC} (output data rate) can be greatly suppressed.

Adjacent Channel Leakage Ratio (ACLR)
ACLR is the ratio in decibels relative to the carrier (dBc) between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection
In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

Adjusted DAC Update Rate
The adjusted DAC update rate is defined as the DAC update rate divided by the smallest interpolating factor. For clarity on DACs with multiple interpolating factors, the adjusted DAC update rate for each interpolating factor may be given.

Physical Lane
Physical Lane x refers to SERDINx±.

Logical Lane
Logical Lane x refers to physical lanes after optionally being remapped by the crossbar block (Register 0x308 to Register 0x30B).

Link Lane
Link Lane x refers to logical lanes considered per link. When paging Link 0 (Register 0x300[2] = 0), Link Lane x = Logical Lane x. When paging Link 1 (Register 0x300[2] = 1, dual link only), Link Lane x = Logical Lane x + 4.

TYPICAL PERFORMANCE CHARACTERISTICS

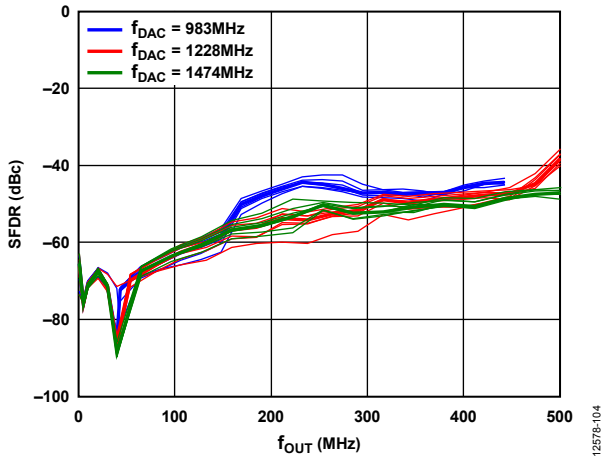


Figure 4. Single-Tone SFDR vs. f_{OUT} in the First Nyquist Zone, f_{DAC} = 983 MHz, 1228 MHz, and 1474 MHz

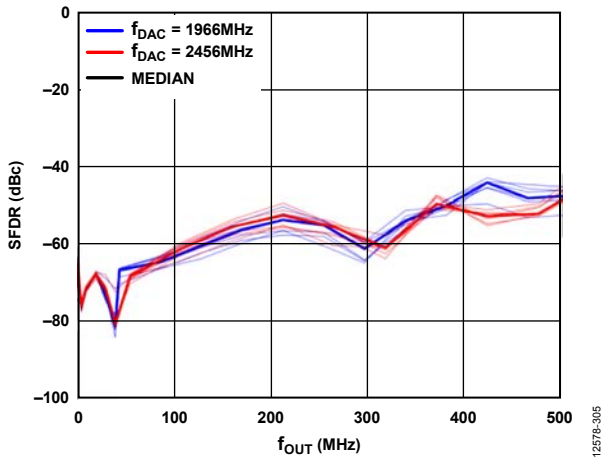


Figure 5. Single-Tone SFDR vs. f_{OUT} in the First Nyquist Zone, f_{DAC} = 1966 MHz and 2456 MHz

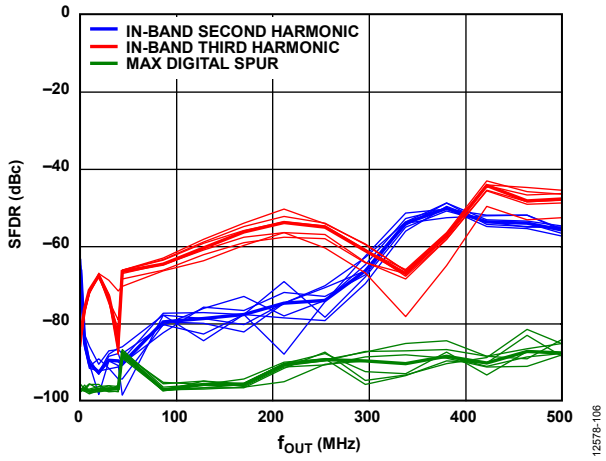


Figure 6. Single-Tone Second and Third Harmonics and Maximum Digital Spur in the First Nyquist Zone, f_{DAC} = 1966 MHz, 0 dB Back Off

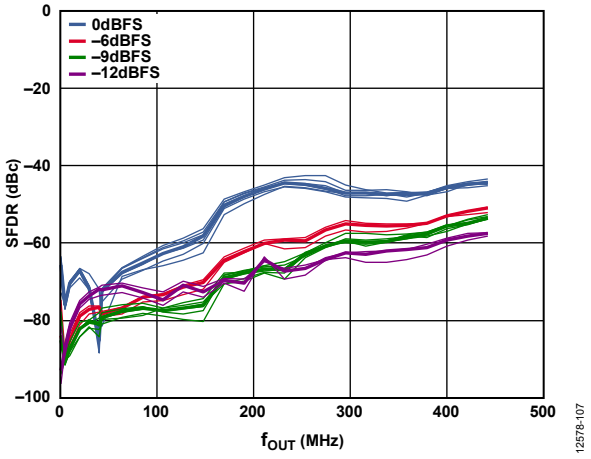


Figure 7. Single-Tone SFDR vs. f_{OUT} in the First Nyquist Zone over Digital Back Off, f_{DAC} = 983 MHz

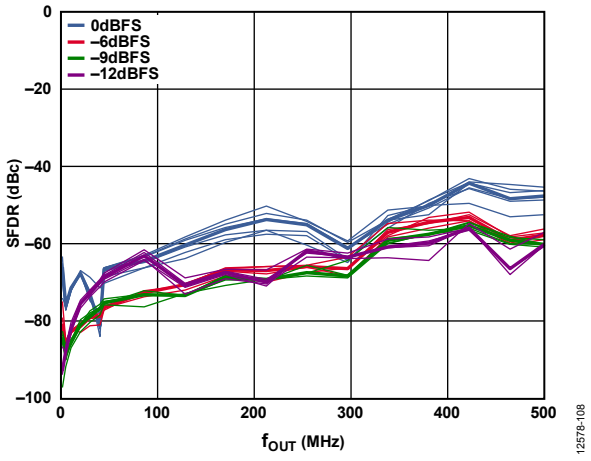


Figure 8. Single-Tone SFDR vs. f_{OUT} in the First Nyquist Zone over Digital Back Off, f_{DAC} = 1966 MHz

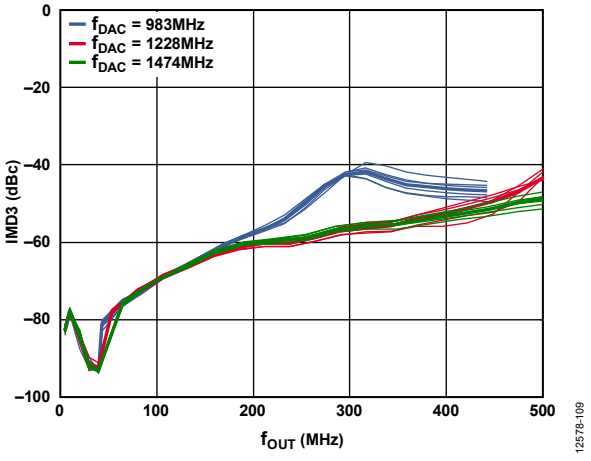


Figure 9. Two-Tone Third IMD (IMD3) vs. f_{OUT}, f_{DAC} = 983 MHz, 1228 MHz, and 1474 MHz

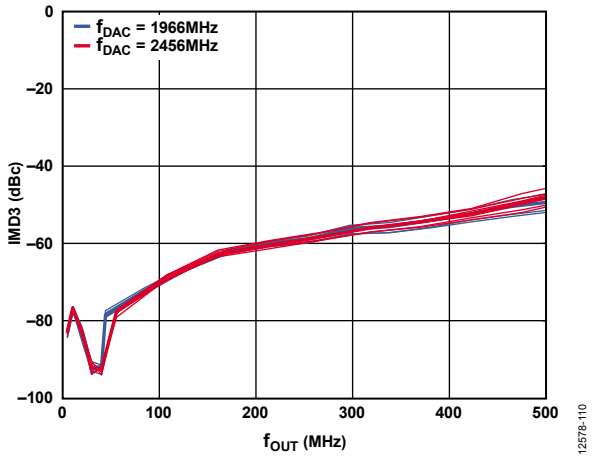


Figure 10. Two-Tone Third IMD (IMD3) vs. f_{OUT}, f_{DAC} = 1966 MHz and 2456 MHz

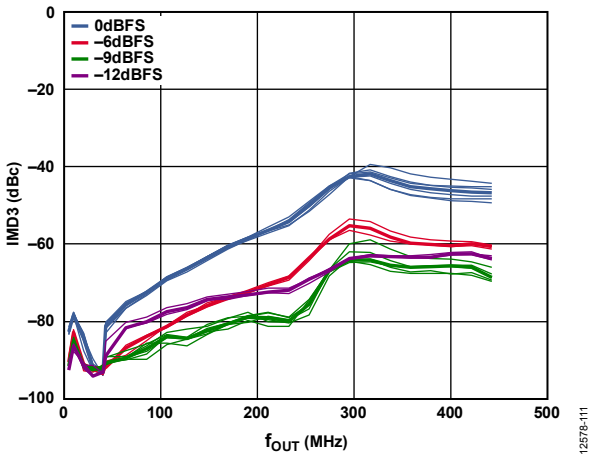


Figure 11. Two-Tone Third IMD (IMD3) vs. f_{OUT} over Digital Back Off, f_{DAC} = 983 MHz, Each Tone Is at –6 dBFS

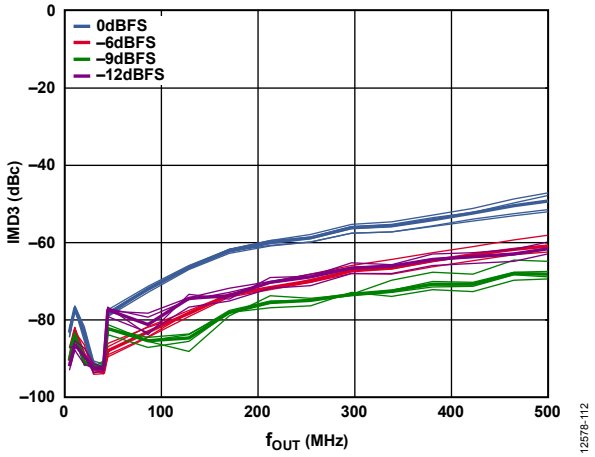


Figure 12. Two-Tone Third IMD (IMD3) vs. f_{OUT} over Digital Back Off, f_{DAC} = 1966 MHz, Each Tone Is at –6 dBFS

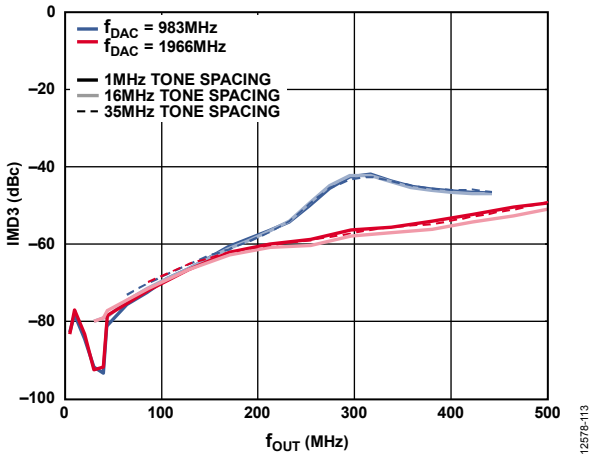


Figure 13. Two-Tone Third IMD (IMD3) vs. f_{OUT} over Tone Spacing at 0 dB Back Off, f_{DAC} = 983 MHz and 1966 MHz

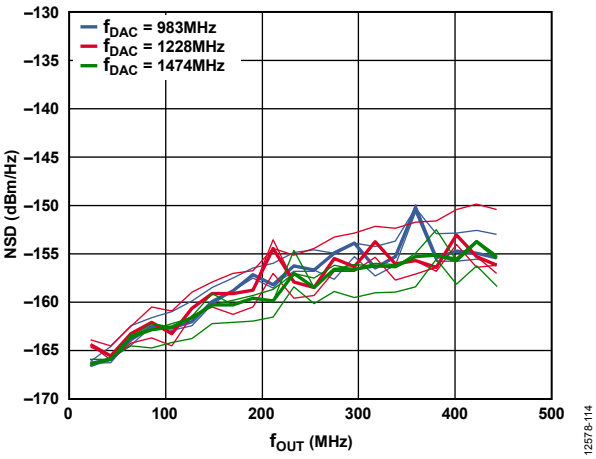


Figure 14. AD9136 Single-Tone (0 dBFS) NSD vs. f_{OUT}, f_{DAC} = 983 MHz, 1228 MHz, and 1474 MHz

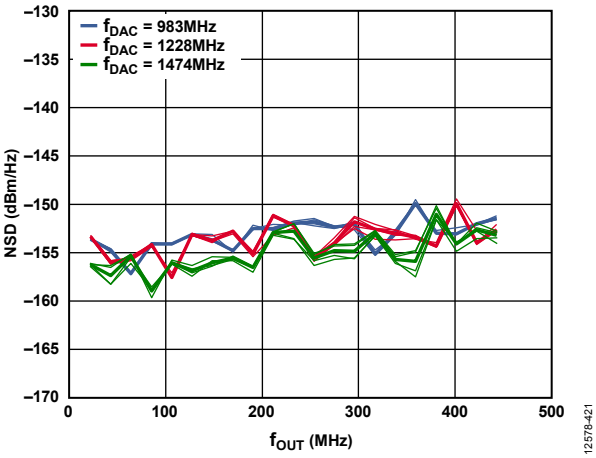


Figure 15. AD9135 Single-Tone (0 dBFS) NSD vs. f_{OUT}, f_{DAC} = 983 MHz, 1228 MHz, and 1474 MHz

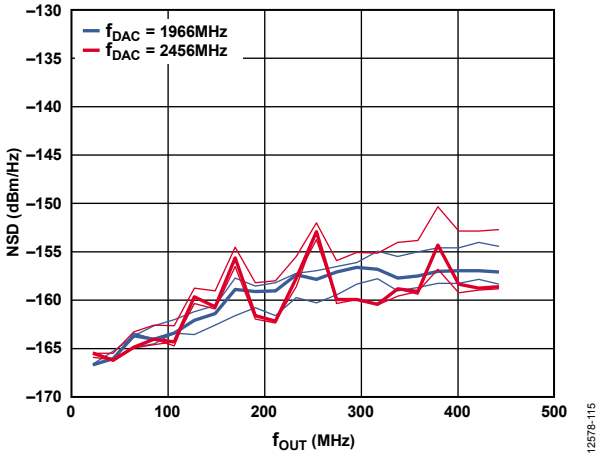


Figure 16. AD9136 Single-Tone (0 dBFS) NSD vs. f_{OUT}, f_{DAC} = 1966 MHz and 2456 MHz

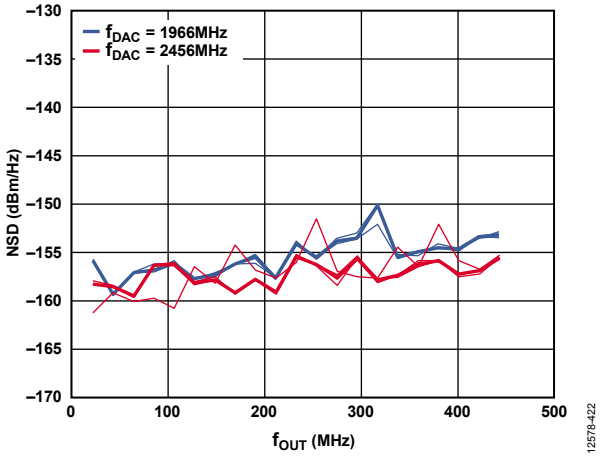


Figure 17. AD9135 Single-Tone (0 dBFS) NSD vs. f_{OUT}, f_{DAC} = 1966 MHz and 2456 MHz

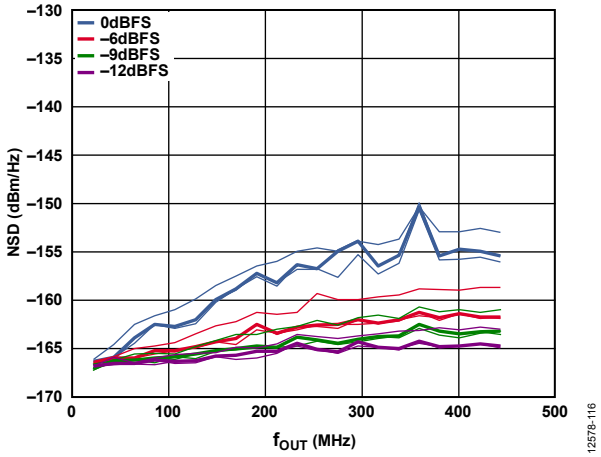


Figure 18. AD9136 Single-Tone NSD vs. f_{OUT} over Digital Back Off, f_{DAC} = 983 MHz

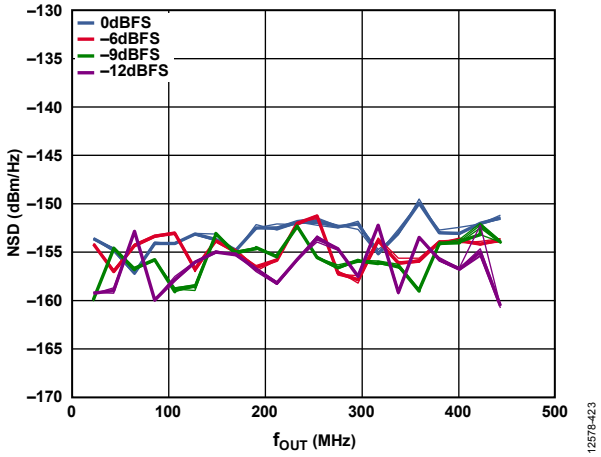


Figure 19. AD9135 Single-Tone NSD vs. f_{OUT} over Digital Back Off, f_{DAC} = 983 MHz

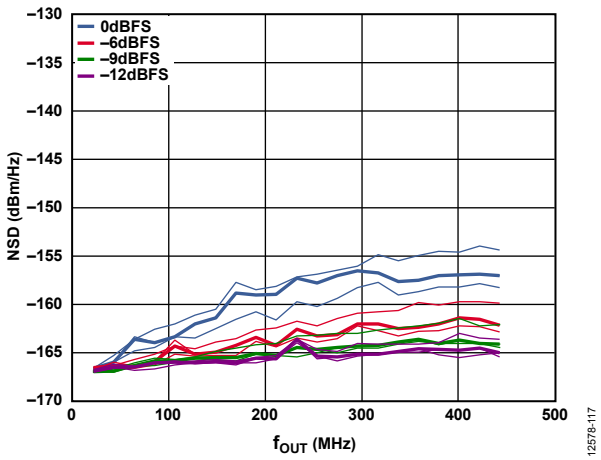


Figure 20. AD9136 Single-Tone NSD vs. f_{OUT} over Digital Back Off, f_{DAC} = 1966 MHz

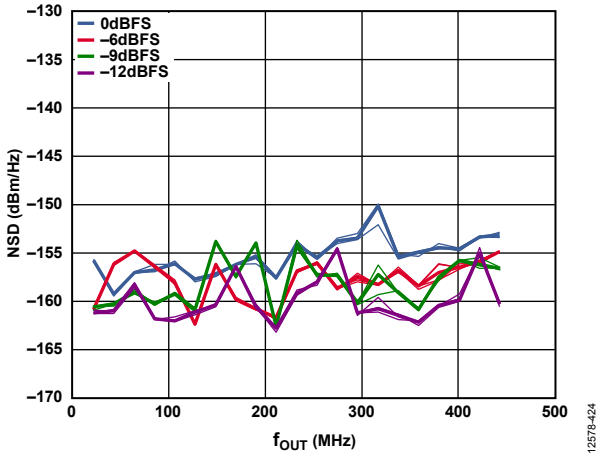


Figure 21. AD9135 Single-Tone NSD vs. f_{OUT} over Digital Back Off, f_{DAC} = 1966 MHz

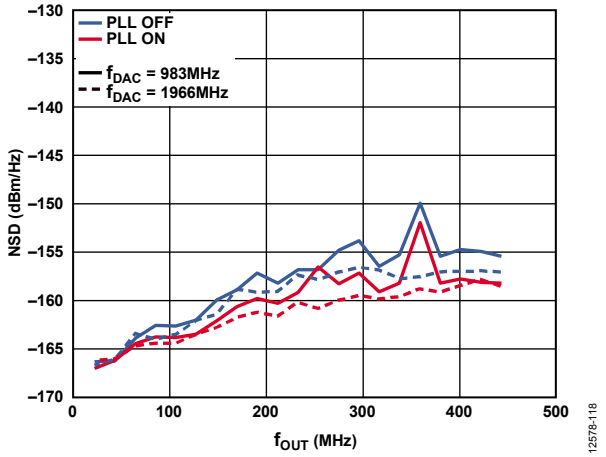


Figure 22. AD9136 Single-Tone NSD (0 dBFS) vs. f_{OUT}, f_{DAC} = 983 MHz and 1966 MHz, PLL On and Off

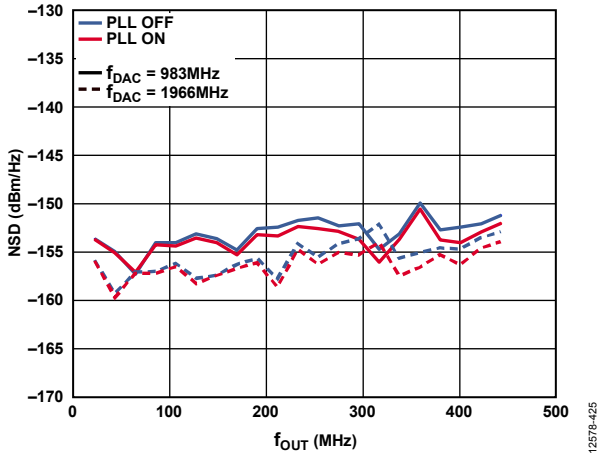


Figure 23. AD9135 Single-Tone NSD (0 dBFS) vs. f_{OUT}, f_{DAC} = 983 MHz and 1966 MHz, PLL On and Off

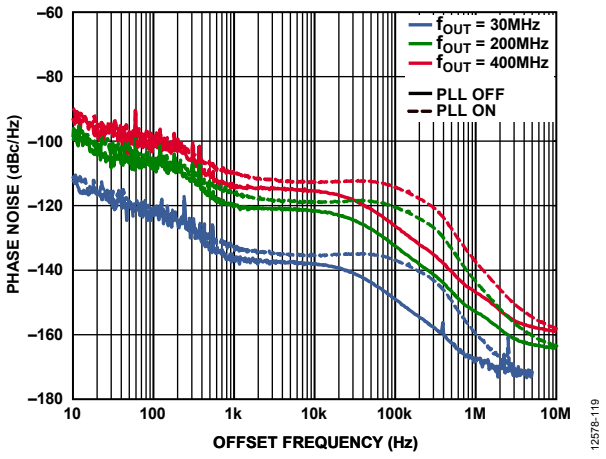


Figure 24. AD9136 Single-Tone Phase Noise vs. Offset Frequency over f_{OUT}, f_{DAC} = 2.0 GHz, PLL On and Off

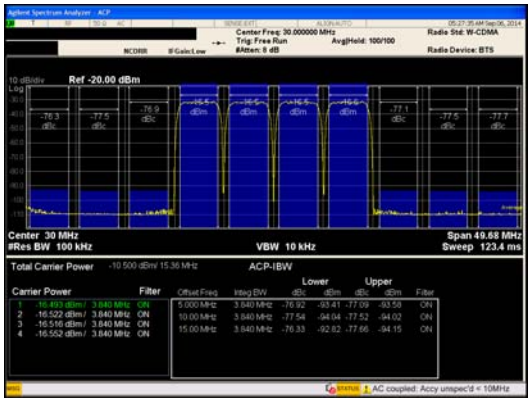


Figure 25. AD9136 Four-Carrier W-CDMA ACLR, f_{OUT} = 30 MHz, f_{DAC} = 983 MHz, 2× Interpolation, PLL Frequency = 122 MHz

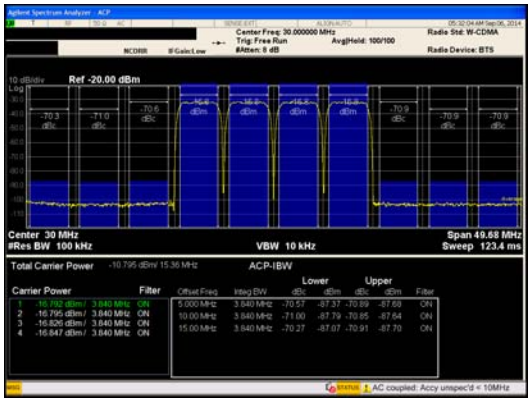


Figure 26. AD9135 Four-Carrier W-CDMA ACLR, f_{OUT} = 30 MHz, f_{DAC} = 983 MHz, 2× Interpolation, PLL Frequency = 122 MHz

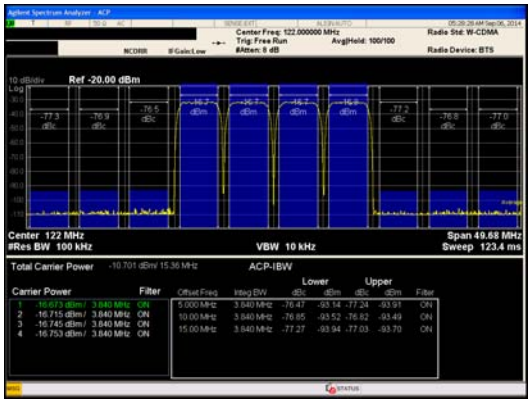


Figure 27. AD9136 Four-Carrier W-CDMA ACLR, f_{OUT} = 122 MHz, f_{DAC} = 983 MHz, 2× Interpolation, PLL Frequency = 122 MHz

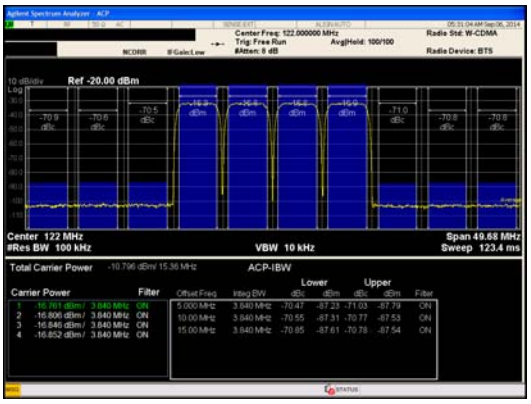


Figure 28. AD9135 Four-Carrier W-CDMA ACLR, f_{OUT} = 122 MHz, f_{DAC} = 983 MHz, 2× Interpolation, PLL Frequency = 122 MHz

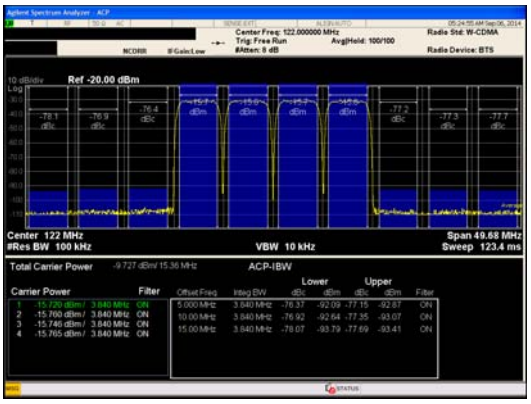


Figure 31. AD9136 Four-Carrier W-CDMA ACLR, f_{OUT} = 122 MHz, f_{DAC} = 1966 MHz, 4× Interpolation, PLL Frequency = 122 MHz

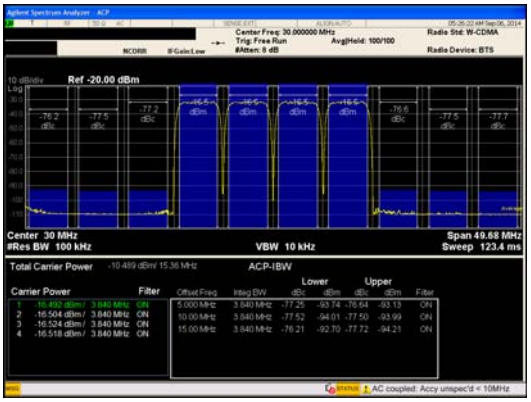


Figure 29. AD9136 Four-Carrier W-CDMA ACLR, f_{OUT} = 30 MHz, f_{DAC} = 1966 MHz, 4× Interpolation, PLL Frequency = 245 MHz

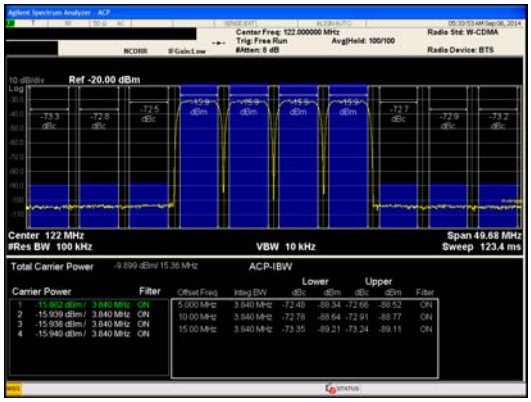


Figure 32. AD9135 Four-Carrier W-CDMA ACLR, f_{OUT} = 122 MHz, f_{DAC} = 1966 MHz, 4× Interpolation, PLL Frequency = 122 MHz

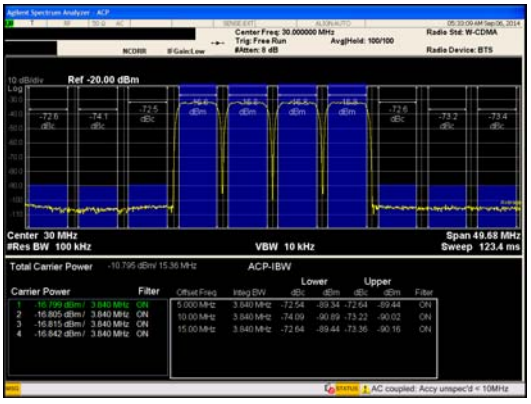


Figure 30. AD9135 Four-Carrier W-CDMA ACLR, f_{OUT} = 30 MHz, f_{DAC} = 1966 MHz, 4× Interpolation, PLL Frequency = 245 MHz

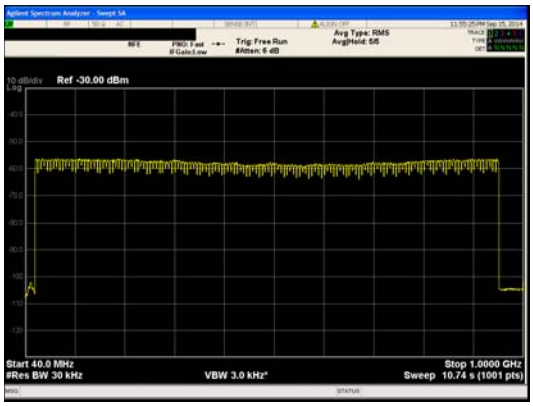


Figure 33. AD9136 Output Performance of an Ultra Wideband (900 MHz) QAM Signal, f_{DAC} = 2 GHz, 1× Interpolation, Inverse sinc On, JESD204B Mode 11

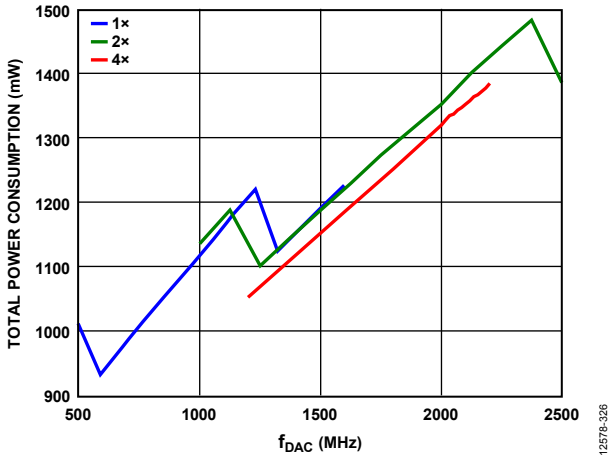


Figure 34. Total Power Consumption vs. f_{DAC} over Interpolation, 8 SERDES Lanes Enabled, 2 DACs Enabled, Digital Gain, Inverse Sinc and DAC PLL Disabled

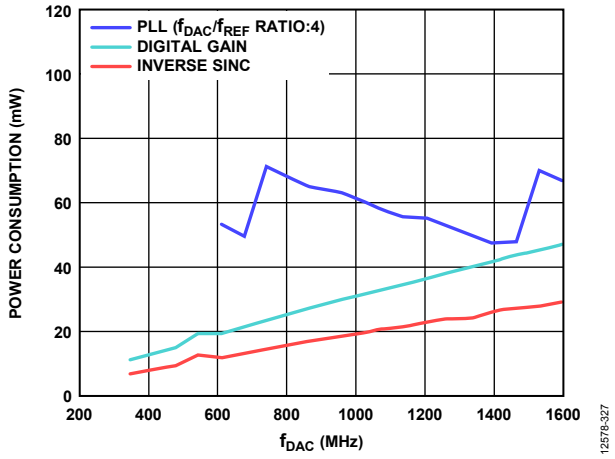


Figure 35. Power Consumption vs. f_{DAC} over Digital Functions

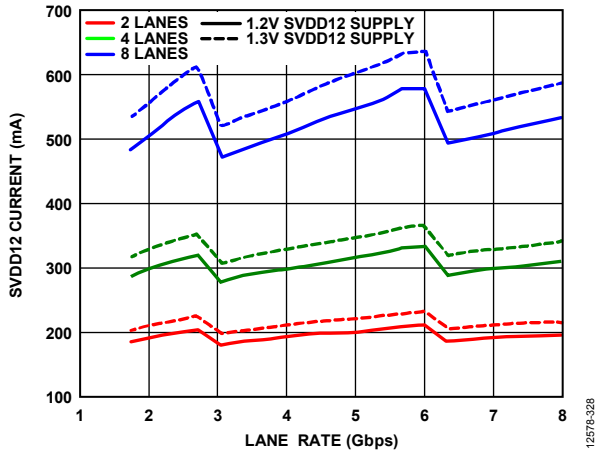


Figure 36. SVDD12 Current vs. Lane Rate over Number of SERDES Lanes and Supply Voltage Setting

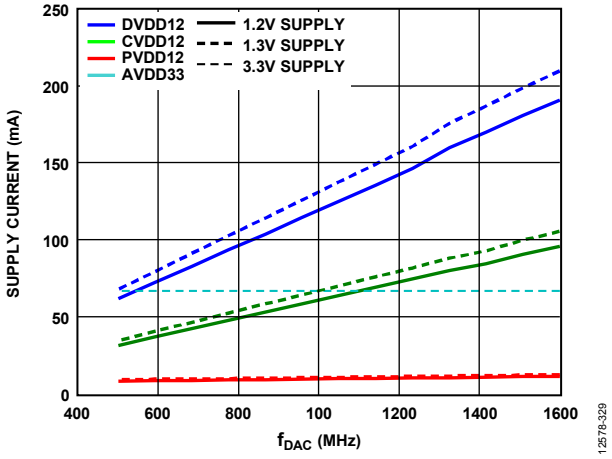


Figure 37. DVDD12, CVDD12, PVDD12, and AVDD33 Supply Currents vs. f_{DAC} over Supply Voltage Setting, 2 DACs Enabled

THEORY OF OPERATION

The AD9135/AD9136 are 11-/16-bit, dual DACs with a SERDES interface. Figure 2 shows a detailed functional block diagram of the AD9135/AD9136. Eight high speed serial lanes carry data at a maximum speed of 12.4 Gbps, and a 2120 MSPS input data rate to each DAC. Compared to either LVDS or CMOS interfaces, the SERDES interface simplifies pin count, board layout, and input clock requirements to the device.

The clock for the input data is derived from the device clock (required by the JESD204B specification). This device clock can be sourced with a PLL reference clock used by the on-chip PLL to generate a DAC clock or a high fidelity direct external DAC sampling clock. The device can be configured to operate in one-, two-, four-, or eight-lane modes, depending on the required input data rate.

The digital datapath of the AD9135/AD9136 offers four interpolation modes (1×, 2×, 4×, and 8×) through three half-band filters with a maximum DAC sample rate of 2.8 GSPS. An inverse sinc filter is provided to compensate for sinc related roll-off.

The AD9135/AD9136 DAC cores provide a fully differential current output with a nominal full-scale current of 20 mA. The full-scale current, I_{OUTFS}, is user adjustable to between 13.9 mA and 27.0 mA, typically. The differential current outputs are complementary and are optimized for easy integration with the Analog Devices the ADRF6720 AQM. The AD9135/AD9136 are capable of multichip synchronization that can both synchronize multiple DACs and establish a constant and deterministic latency (latency locking) path for the DACs. The latency for each of the DACs remains constant from link establishment to link establishment. An external alignment (SYSREF±) signal makes the AD9135/AD9136 Subclass 1 compliant. Several modes of SYSREF± signal handling are available for use in the system.

An SPI configures the various functional blocks and monitors their statuses. The various functional blocks and the data interface must be set up in a specific sequence for proper operation (see the Device Setup Guide section). Simple SPI initialization routines set up the JESD204B link and are included in the evaluation board package. The following sections describe the various blocks of the AD9135/AD9136 in greater detail. Descriptions of the JESD204B interface, control parameters, and various registers to set up and monitor the device are provided. The recommended start-up routine reliably sets up the data link.

SERIAL PORT OPERATION

The serial port is a flexible, synchronous serial communications port that allows easy interfacing with many industry-standard microcontrollers and microprocessors. The serial input/output (I/O) is compatible with most synchronous transfer formats, including both the Motorola SPI and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9135/AD9136. MSB first or LSB first transfer formats are supported. The serial port interface can be configured as a 4-wire interface or a 3-wire interface in which the input and output share a single-pin I/O (SDIO).

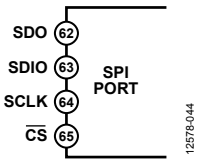


Figure 38. Serial Port Interface Pins

There are two phases to a communication cycle with the AD9135/AD9136. Phase 1 is the instruction cycle (the writing of an instruction byte into the device), coincident with the first 16 SCLK rising edges. The instruction word provides the serial port controller with information regarding the data transfer cycle, Phase 2 of the communication cycle. The Phase 1 instruction word defines whether the upcoming data transfer is a read or write, along with the starting register address for the following data transfer.

A logic high on the $\overline{CS}$ pin followed by a logic low resets the serial port timing to the initial state of the instruction cycle. From this state, the next 16 rising SCLK edges represent the instruction bits of the current I/O operation.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the device and the system controller. Phase 2 of the communication cycle is a transfer of one or more data bytes. Eight × N SCLK cycles are needed to transfer N bytes during the transfer cycle. Registers change immediately upon writing to the last bit of each transfer byte.

DATA FORMAT

The instruction byte contains the information shown in Table 13.

Table 13. Serial Port Instruction Word

I[15] (MSB)	I[14:0]
R/$\overline{W}$	A[14:0]

R/$\overline{W}$, Bit 15 of the instruction word, determines whether a read or a write data transfer occurs after the instruction word write. Logic 1 indicates a read operation, and Logic 0 indicates a write operation.

A14 to A0, Bit 14 to Bit 0 of the instruction word, determine the register that is accessed during the data transfer portion of the communication cycle. For multibyte transfers, A[14:0] is the starting address. The remaining register addresses are generated by the device based on the address increment bits. If the address increment bits are set high (Register 0x000, Bit 5 and Bit 2), multibyte SPI writes start at A[14:0] and increment by 1 every 8 bits sent/received. If the address increment bits are set to 0, the address decrements by 1 every 8 bits.

SERIAL PORT PIN DESCRIPTIONS

Serial Clock (SCLK)

The serial clock pin synchronizes data to and from the device and runs the internal state machines. The maximum frequency of SCLK is 10 MHz. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

Chip Select ($\overline{CS}$)

An active low input starts and gates a communication cycle. $\overline{CS}$ allows more than one device to be used on the same serial communications lines. The SDIO pin goes to a high impedance state when this input is high. During the communication cycle, chip select must stay low.

Serial Data I/O (SDIO)

This pin is a bidirectional data line. In 4-wire mode, this pin acts as the data input, and SDO acts as the data output.

SERIAL PORT OPTIONS

The serial port can support both MSB first and LSB first data formats. This functionality is controlled by the LSB first bits (Register 0x000, Bit 6 and Bit 1). The default is MSB first (LSBFIRST/LSBFIRST_M = 0).

When the LSB first bits = 0 (MSB first), the instruction and data bits must be written from MSB to LSB. R/$\overline{W}$ is followed by A[14:0] as the instruction word, and D[7:0] is the data-word. When the LSB first bits = 1 (LSB first), the opposite is true. A[0:14] is followed by R/$\overline{W}$, which is subsequently followed by D[0:7].

The serial port supports a 3-wire or 4-wire interface. When the SDO active bits = 1 (Register 0x000, Bit 4 and Bit 3), a 4-wire interface with a separate input pin (SDIO) and output pin (SDO) is used. When the SDO active bits = 0, the SDO pin is unused and the SDIO pin is used for both input and output.

Multibyte data transfers can be performed as well. This is done by holding the $\overline{CS}$ pin low for multiple data transfer cycles (eight SCLKs) after the first data transfer word following the instruction cycle. The first eight SCLKs following the instruction cycle read from or write to the register provided in the instruction cycle. For each additional eight SCLK cycles, the address is either incremented or decremented and the read/write occurs on the new register. The direction of the address can be set using the address increment bits (Register 0x000, Bit 5 and Bit 2). When the address increment bits is 1, the multicycle addresses are incremented. When the address increment bits is 0, the addresses are decremented. A new write cycle can always be initiated by bringing $\overline{CS}$ high and then low again.

To prevent confusion and to ensure consistency between devices, the chip tests the first nibble following the address phase, ignoring the second nibble. This test is completed independently from the LSB first bit and ensures that there are extra clock cycles following the soft reset bits (Register 0x000, Bit 0 and Bit 7). This only applies when writing to Register 0x000.

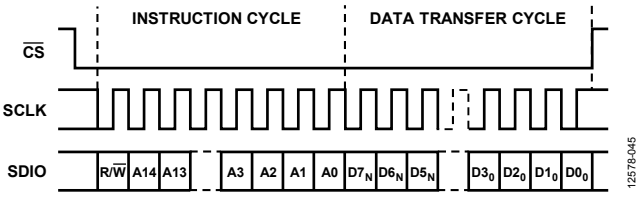


Figure 39. Serial Register Interface Timing, MSB First, ADDRINC = 0

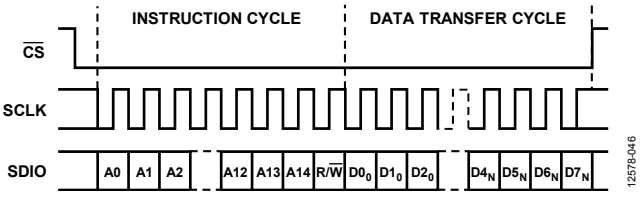


Figure 40. Serial Register Interface Timing, LSB First, ADDRINC = 1

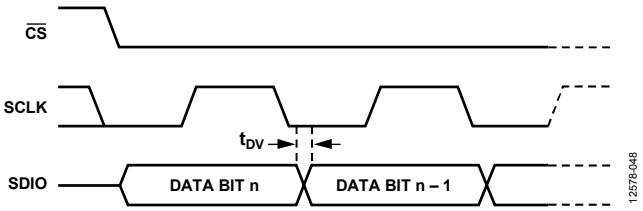


Figure 41. Timing Diagram for Serial Port Register Read

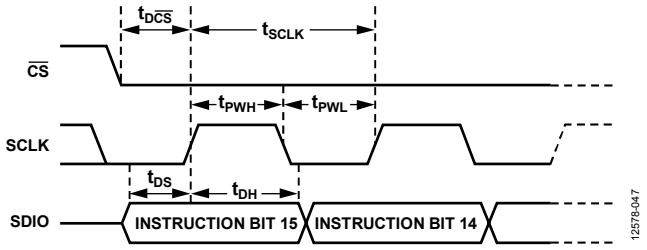


Figure 42. Timing Diagram for Serial Port Register Write

CHIP INFORMATION

Register 0x003 to Register 0x006 contain chip information, as shown in Table 14.

Table 14. Chip Information

Information	Description
Chip Type	The product type is high speed DAC, which is represented by a code of 0x04 in Register 0x003.
Product ID	Eight MSBs in Register 0x005 and eight LSBs in Register 0x004. The product ID is 0x9144.
Product Grade	Register 0x006[7:4]. The product grade is 0x6 for the AD9136 and 0x4 for the AD9135.
Device Revision	Register 0x006[3:0]. The device revision is 0x08.

DEVICE SETUP GUIDE

OVERVIEW

The sequence of steps to properly set up the AD9135/AD9136 is as follows:

1. Set up the SPI interface, power up necessary circuit blocks, make the required writes to the configuration registers, and set up the DAC clocks (see the Step 1: Start Up the DAC section).
2. Set the digital features of the AD9135/AD9136 (see the Step 2: Digital Datapath section).
3. Set up the JESD204B links (see the Step 3: Transport Layer section).
4. Set up the physical layer of the SERDES interface (see the Step 4: Physical Layer section).
5. Set up the data link layer of the SERDES interface (see the Step 5: Data Link Layer section).
6. Check for errors (see the Step 6: Optional Error Monitoring section).
7. Optionally, enable any needed features as described in the Step 7: Optional Features section.

The register writes listed in Table 15 to Table 21 give the register writes necessary to set up the AD9135/AD9136. Consider printing this setup guide and filling in the Value column with the appropriate variable values for the conditions of the desired application.

The notation 0x, shaded in gray, indicates register settings that must be filled in by the user. To fill in the unknown register values, select the correct settings for each variable listed in the Variable column of Table 15 to Table 21. The Description column describes how to set variables or provides a link to a section where this is described. A variable is noted by concatenating multiple terms. For example, PdDACs is a variable corresponding to the value that is determined for Register 0x011[6:3] in the Device Setup Guide section.

STEP 1: START UP THE DAC

This section describes how to set up the SPI interface, power up necessary circuit blocks, write to the required configuration registers, and set up the DAC clocks, listed in Table 15.

Table 15. Power-Up and DAC Initialization Settings

Addr.	Bit No.	Value[1]	Variable	Description
0x000		0xBD		Soft reset.
0x000		0x3C		Deassert reset, set 4-wire SPI.
0x011		0x		
	7	0		Power up band gap.
	[6:3]		PdDACs	PdDACs = 0x05 to power up DAC0/DAC1. PdDACs = 0x07 if only using DAC0.
	2	0		Power up master DAC.
0x080		0x	PdClocks	PdClocks = 0 if DAC0/DAC1 are being used. PdClocks = 0x40 if only using DAC0.
0x081		0x	PdSysref	PdSysref = 0x00 for Subclass 1. PdSysref = 0x10 for Subclass 0. See the Subclass Setup section for details on subclass.

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.

The registers in Table 16 must be written from their default values to be the values listed in the table for the device to work correctly. These registers must be written after any soft reset, hard reset, or power-up occurs.

Table 16. Required Device Configurations

Addr.	Value	Description
0x12D	0x8B	Digital datapath configuration
0x146	0x01	Digital datapath configuration
0x2A4	0xFF	Clock configuration
0x232	0xFF	SERDES interface configuration
0x333	0x01	SERDES interface configuration

If using the optional DAC PLL, also set the registers in Table 17.

Table 17. Optional DAC PLL Configuration Procedure

Addr.	Value[1]	Variable	Description
0x087	0x62		Optimal DAC PLL loop filter settings
0x088	0xC9		Optimal DAC PLL loop filter settings
0x089	0x0E		Optimal DAC PLL loop filter settings
0x08A	0x12		Optimal DAC PLL charge pump settings
0x08D	0x7B		Optimal DAC LDO settings for DAC PLL
0x1B0	0x00		Power DAC PLL blocks when power machine disabled
0x1B9	0x24		Optimal DAC PLL charge pump settings
0x1BC	0x0D		Optimal DAC PLL VCO control settings
0x1BE	0x02		Optimal DAC PLL VCO power control settings
0x1BF	0x8E		Optimal DAC PLL VCO calibration settings
0x1C0	0x2A		Optimal DAC PLL lock counter length setting
0x1C1	0x2A		Optimal DAC PLL charge pump setting
0x1C4	0x7E		Optimal DAC PLL varactor settings
0x08B	0x	LODivMode	See the DAC PLL Setup section
0x08C	0x	RefDivMode	See the DAC PLL Setup section
0x085	0x	BCount	See the DAC PLL Setup section
Various	0x	LookUpVals	See Table 25 in the DAC PLL Setup section for the list of register addresses and values for each.
0x083	0x10		Enable the DAC PLL[2]

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.

[2] Verify that Register 0x084[1] reads back 1 after enabling the DAC PLL to indicate that the DAC PLL has locked.

STEP 2: DIGITAL DATAPATH

This section describes which interpolation filters to use and how to set the data format being used. Additional digital features are available, including digital gain scaling and an inverse sinc filter used to improve pass-band flatness. Table 22 provides further details on the feature blocks available.

Table 18. Digital Datapath Settings

Addr.	Bit No.	Value[1]	Variable	Description
0x112		0x	InterpMode	Select interpolation mode; see the Interpolation section.
0x110		0x		
	7		DataFmt	DataFmt = 0 if twos complement; DataFmt = 1 if unsigned binary.

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.

STEP 3: TRANSPORT LAYER

This section describes how to set up the JESD204B links. The parameters are determined by the desired JESD204B operating mode. See the JESD204B Setup section for details.

Table 19 shows the register settings for the transport layer. If using dual-link mode, perform writes from Register 0x300 to Register 0x47D with CurrentLink = 0 and then repeat the same set of register writes with CurrentLink = 1 (Register 0x200 and Register 0x201 need only be written once).

Table 19. Transport Layer Settings

Addr.	Bit No.	Value[1]	Variable	Description
0x200		0x00		Power up the interface.
0x201		0x	UnusedLanes	See the JESD204B Setup section.
0x300		0x		
	6		CheckSumMode	See the JESD204B Setup section.
	3		DualLink	See the JESD204B Setup section.
	2		CurrentLink	See the JESD204B Setup section.
0x450		0x	DID	Set DID to match the device ID sent by the transmitter.
0x451		0x	BID	Set BID to match the bank ID sent by the transmitter.
0x452		0x	LID	Set LID to match the lane ID sent by the transmitter.
0x453		0x		
	7		Scrambling	See the JESD204B Setup section.
	[4:0]		L – 1[2]	See the JESD204B Setup section.
0x454		0x	F – 1[2]	See the JESD204B Setup section.
0x455		0x	K – 1[2]	See the JESD204B Setup section.
0x456		0x	M – 1[2]	See the JESD204B Setup section.
0x457		0x	N – 1[2]	N = 16.
0x458		0x		
	[7:5]		Subclass	See the JESD204B Setup section.
	[4:0]		NP – 1[2]	NP = 16.
0x459		0x		
	[7:5]		JESDVer	JESDVer = 1 for JESD204B, JESDVer = 0 for JESD204A.
	[4:0]		S – 1[2]	See the JESD204B Setup section.
0x45A		0x		
	7		HD	See the JESD204B Setup section.
	[4:0]	0	CF	CF must equal 0.
0x45D		0x	Lane0Checksum	See the JESD204B Setup section.
0x46C		0x	Lanes	Deskew lanes. See the JESD204B Setup section.
0x476		0x	F	See the JESD204B Setup section.
0x47D		0x	Lanes	Enable lanes. See the JESD204B Setup section.

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the correct register value.
[2] This JESD204B link parameter is programmed in n – 1 notation as noted. For example, if the setup requires L = 8 (8 lanes per link), program L – 1 or 7 into Register 0x453[4:0].

STEP 4: PHYSICAL LAYER

This section describes how to set up the physical layer of the SERDES interface. In this section, the input termination settings are configured along with the CDR sampling and SERDES PLL.

Table 20. Device Configurations and Physical Layer Settings

Addr.	Bit No.	Value[1]	Variable	Description
0x2AA		0xB7		SERDES interface termination setting
0x2AB		0x87		
0x2B1		0xB7		SERDES interface termination setting
0x2B2		0x87		
0x2A7		0x01		Autotune PHY setting
0x2AE		0x01		Autotune PHY setting
0x314		0x01		SERDES SPI configuration
0x230		0x		
	5		Halfrate	Set up the CDR; see the SERDES Clocks Setup section
	[4:2]	0x2		SERDES PLL default configuration
	1		OvSmp	Set up the CDR; see the SERDES Clocks Setup section
0x206		0x00		Reset the CDR
0x206		0x01		Release the CDR reset
0x289		0x		
	2	1		SERDES PLL configuration
	[1:0]		PLLDiv	Set the CDR oversampling for PLL; see the SERDES Clocks Setup section
0x284		0x62		Optimal SERDES PLL loop filter
0x285		0xC9		Optimal SERDES PLL loop filter
0x286		0x0E		Optimal SERDES PLL loop filter
0x287		0x12		Optimal SERDES PLL charge pump
0x28A		0x7B		Optimal SERDES PLL VCO LDO
0x28B		0x00		Optimal SERDES PLL configuration
0x290		0x89		Optimal SERDES PLL VCO varactor
0x294		0x24		Optimal SERDES PLL charge pump
0x296		0x03		Optimal SERDES PLL VCO
0x297		0x0D		Optimal SERDES PLL VCO
0x299		0x02		Optimal SERDES PLL configuration
0x29A		0x8E		Optimal SERDES PLL VCO varactor
0x29C		0x2A		Optimal SERDES PLL charge pump
0x29F		0x78		Optimal SERDES PLL VCO varactor
0x2A0		0x06		Optimal SERDES PLL VCO varactor
0x280		0x01		Enable the SERDES PLL[2]
0x268		0x		
	[7:6]		EqMode	See the Equalization Mode Setup section
	[5:0]	0x22		Required value (default)

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the correct register value.
[2] Verify that Register 0x281[0] reads back 1 after enabling the SERDES PLL to indicate that the SERDES PLL has locked.

STEP 5: DATA LINK LAYER

This section describes how to set up the data link layer of the SERDES interface. This section deals with SYSREF signal processing, setting deterministic latency, and establishing the link.

Table 21. Data Link Layer Settings

Addr.	Bit No.	Value[1]	Variable	Description
0x301		0x	Subclass	See the JESD204B Setup section.
0x304		0x	LMFCDel	See the Link Latency Setup section.
0x305		0x	LMFCDel	See the Link Latency section.
0x306		0x	LMFCVar	See the Link Latency Setup section.
0x307		0x	LMFCVar	See the Link Latency Setup section.
0x03A		0x01		Set sync mode = one-shot sync; see the Syncing LMFC Signals section for other sync options.
0x03A		0x81		Enable the sync machine.
0x03A		0xC1		Arm the sync machine.
SYSREF± Signal				If Subclass = 1, ensure that at least one SYSREF± edge is sent to the device.[2]
0x308 to 0x30B		0x	XBarVals	If remapping lanes, set up crossbar; see the Crossbar Setup section.
0x334		0x	InvLanes	Invert the polarity of the desired logical lanes. Bit x of InvLanes must be a 1 for each Logical Lane x to invert.
0x300		0x		Enable the links.
	6		CheckSumMode	See the JESD204B Setup section.
	3		DualLink	
	2		CurrentLink	Set to 0 to access Link 0 status or 1 for Link 1 status readbacks. See the JESD204B Setup section.
	[1:0]		EnLinks	EnLinks = 3 if DualLink = 1 (enables Link 0 and Link 1); EnLinks = 1 if DualLink = 0 (enables Link 0 only).

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the correct register value.
[2] Verify that Register 0x03B[3] reads back 1 after sending at least one SYSREF± edge to the device to indicate that the LMFC sync machine has properly locked.

STEP 6: OPTIONAL ERROR MONITORING

For JESD204B error monitoring, see the JESD204B Error Monitoring section. For other error checks, see the Interrupt Request Operation section.

STEP 7: OPTIONAL FEATURES

There are a number of optional features that can be enabled. Table 22 provides links to the sections describing each feature. These features can be enabled during the Digital Datapath configuration step, or after the link is set up, because it is not required to configure them for the link to be established, unlike interpolation. Unless otherwise noted, these features are paged as described in the DAC Paging section. Paging is particularly important for DAC specific settings like digital gain and dc offset.

Table 22. Optional Features

Feature	Default	Description
Inverse Sinc	On	Improves pass-band flatness. See the Inverse Sinc section.
Digital Gain	2.7 dB	Multiplies data by a factor. Can compensate inverse sinc usage or balance I/Q amplitude. See the Digital Gain section.
DC Offset	Off	Used to cancel LO leakage. See the DC Offset section.
Group Delay	0	Used to control overall latency. See the Group Delay section.
Downstream Protection	Off	Used to protect downstream components. See the Downstream Protection section.
Self Calibration	Off	Used to improve DAC linearity. Not paged by the dual paging register. See the Self Calibration section.

DAC PLL SETUP

This section explains how to select appropriate values for LODivMode, RefDivMode, and BCount in the Step 1: Start Up the DAC section. These parameters depend on the desired DAC clock frequency (f_{DAC}) and DAC reference clock frequency (f_{REF}). When using the DAC PLL, the reference clock signal is applied to the CLK± differential pins (Pin 2 and Pin 3).

Table 23. DAC PLL LODivMode Settings

DAC Frequency Range (MHz)	LO_DIV_MODE, Register 0x08B[1:0]
1500 to 2800	1
750 to 1500	2
420 to 750	3

Table 24. DAC PLL RefDivMode Settings

DAC PLL Reference Frequency (f_{REF}) (MHz)	Divide by (RefDivFactor)	REF_DIV_MODE, Register 0x08C[2:0]
35 to 80	1	0
80 to 160	2	1
160 to 320	4	2
320 to 640	8	3
640 to 1000	16	4

The VCO frequency (f_{VCO}) is related to the DAC clock frequency according to the following equation:

$$f_{VCO} = f_{DAC} \times 2^{LODivMode + 1}$$

where 6 GHz ≤ f_{VCO} ≤ 12 GHz.

BCount must be between 6 and 127 and is calculated based on f_{DAC} and f_{REF} as follows:

$$BCount = \text{floor}((f_{DAC})/(2 \times f_{REF}/RefDivFactor))$$

where $RefDivFactor = 2^{RefDivMode}$ (see Table 24).

Finally, to finish configuring the DAC PLL, set the VCO control registers up as described in Table 25 based on the VCO frequency (f_{VCO}). Write the registers listed in the table with the corresponding LookUpVals.

Table 25. VCO Control Lookup Table Reference

VCO Frequency Range (GHz)	Register 0x1B5 Setting	Register 0x1BB Setting	Register 0x1C5 Setting
f_{VCO} < 6.3	0x08	0x03	0x07
6.3 ≤ f_{VCO} < 7.25	0x09	0x03	0x06
f_{VCO} ≥ 7.25	0x09	0x13	0x06

For more information on the DAC PLL, see the DAC Input Clock Configurations section.

INTERPOLATION

The transmit path can use zero to three cascaded interpolation filters, which each provides a 2× increase in output data rate and a low-pass function. Table 26 shows the different interpolation modes and the respective usable bandwidth along with the maximum f_{DATA} rate attainable.

Table 26. Interpolation Modes and Their Usable Bandwidth

Interpolation Mode	InterpMode	Usable Bandwidth	Maximum f_{DATA} (MSPS)
1× (bypass)	0x00	0.5 × f_{DATA}	2120 (SERDES limited)
2×	0x01	0.4 × f_{DATA}	1060 (SERDES limited)
4×	0x03	0.4 × f_{DATA}	700
8×	0x04	0.4 × f_{DATA}	350

The usable bandwidth is defined for 1×, 2×, 4×, and 8× modes as the frequency band over which the filters have a pass-band ripple of less than ±0.001 dB and an image rejection of greater than 85 dB. For more information, see the Interpolation Filters section.

JESD204B SETUP

This section explains how to select a JESD204B operating mode for a desired application. This section in turn defines appropriate values for CheckSumMode, UnusedLanes, DualLink, CurrentLink, Scrambling, L, F, K, M, N, NP, Subclass, S, HD, Lane0Checksum, and Lanes needed for the Step 3: Transport Layer section.

Note that DualLink, Scrambling, F, K, N, NP, S, HD, and Subclass must be set the same on the transmit side. For Mode 8, Mode 9, and Mode 10, the number of converters (M) and the lane count (L) on the transmit side must also match the receive side. For Mode 11, Mode 12, and Mode 13, M and L on the transmit side do not match the receive side. See Table 28 for details.

For a summary of how a JESD204B system works and what each parameter means, see the JESD204B Serial Data Interface section.

Available Operating Modes

Table 27. JESD204B Operating Modes (Single- or Dual-Link) (Applies to Both JESD204B Tx and Rx)

	Mode		
Parameter	8[1]	9	10
M (Converter Count)	1	1	1
L (Lane Count)	4	2	1
S ((Samples per Converter) per Frame)	2	1	1
F ((Octets per Frame) per Lane)	1	1	2

[1] Mode 8 can only be used with 1× interpolation. Other interpolation options are not available in this mode.

Table 28. JESD204B Operating Modes (Single-Link Only)

	Mode		
Parameter	**11[2]**	**12**	**13**
M (Converter Count) (Tx Setting)	2	2	2
AD9135 and AD9136 M Setting[1] (Rx Setting)	1	1	1
L (Lane Count) (Tx Setting)	8	4	2
AD9135 and AD9136 L Setting[1] (Rx Setting)	4	2	1
S ((Samples per Converter) per Frame)	2	1	1
F ((Octets per Frame) per Lane)	1	1	2

[1] Note that for Mode 11 to Mode 13, the M and L parameters programmed on the receive side do not match the parameters on the transmit side. The parameters on the transmit side reflect the true number of converters and lanes per link.
[2] Mode 11 can only be used with 1× interpolation. Other interpolation options are not available in this mode.

For a particular application, the number of converters to use per link (M) and the f_{DATA} (DataRate) are known. The LaneRate and number of lanes (L) can be traded off as follows:

$$DataRate = (DACRate)/(InterpolationFactor)$$
$$LaneRate = (20 \times DataRate \times M)/L$$

where *LaneRate* is between 1.44 Gbps and 12.4 Gbps.

Octets per frame per lane (F) and samples per convertor per frame (S) define how the data is packed. If F = 1, the high density setting must be set to one (HD = 1). Otherwise, set HD = 0.

Converter resolution and bits per sample (N and NP) must both be set to 16. Frames per multiframe (K) must be set to 32 for Mode 8, Mode 9, Mode 11, and Mode 12. Other modes can use either K = 16 or K = 32.

DualLink

DualLink sets up two independent JESD204B links, which allows each link to be reset independently. If this functionality is desired, set DualLink to 1; if a single link is desired, set DualLink to 0. Note that Link 0 and Link 1 must have identical parameters. The operating modes available when using dual- or single-link mode are shown in Table 27. Additional single-link modes that are available are shown in Table 28.

Scrambling

Scrambling is a feature that makes the spectrum of the link data independent. This avoids spectral peaking and provides some protection against data dependent errors caused by frequency selective effects in the electrical interface. Set this variable to 1 if scrambling is being used, or to 0 if it is not.

Subclass

Subclass determines whether the latency of the device is deterministic, meaning it requires an external synchronization signal. See the Subclass Setup section for more information.

CurrentLink

Set CurrentLink to either 0 or 1 depending on whether Link 0 or Link 1, respectively, needs to be configured.

Lanes

Lanes is used to enable and deskew particular lanes in two thermometer coded registers. The lanes setting for each of the modes is given in Table 29.

Table 29. Lanes Setting per JESD Operating Mode

JESD Mode ID	8	9	10	11	12	13
Lanes	0x0F	0x03	0x01	0xFF	0x33	0x11

UnusedLanes

UnusedLanes is used to turn off unused circuit blocks to save power. Each physical lane that is not being used (SERDINx±) must be powered off by writing a 1 to the corresponding bit of Register 0x201.

For example, if using Mode 9 in dual-link mode and sending data on SERDIN0±, SERDIN1±, SERDIN4±, and SERDIN5±, set UnusedLanes = 0xCC to power off Physical Lane 2, Lane 3, Lane 6, and Lane 7.

CheckSumMode

CheckSumMode must match the checksum mode used on the transmit side. If the checksum used is the sum of fields in the link configuration table, CheckSumMode = 0. If summing the registers containing the packed link configuration fields, CheckSumMode = 1. For more information on the how to calculate the two checksum modes, see the Lane0Checksum section.

Lane0Checksum

Lane0Checksum can be used for error checking purposes to ensure that the transmitter is set up as expected.

If CheckSumMode = 0, the checksum is the lower eight bits of the sum of the L − 1, M − 1, K − 1, N − 1, NP − 1, S − 1, Scrambling, HD, Subclass, and JESDVer variables.

If CheckSumMode = 1, Lane0Checksum is the lower eight bits of the sum of Register 0x450 to Register 0x45A. Select whether to sum by fields or by registers, matching the setting on the transmitter.

DAC Power-Down Setup

As described in the Step 1: Start Up the DAC section, PdDACs must be set to 5 if both converters are being used either in a single- or dual-link mode. If only one DAC is being used (M = 1 and in single-link mode), PdDACs must be set to 7.

SERDES CLOCKS SETUP

This section describes how to select the appropriate Halfrate, OvSmp, and PLLDiv settings in the Step 4: Physical Layer section. These parameters depend solely on the lane rate (the lane rate is established in the JESD204B Setup section).

Table 30. SERDES Lane Rate Configuration Settings

Lane Rate (Gbps)	Halfrate	OvSmp	PLLDiv
1.44 to 3.1	0	1	2
2.88 to 6.2	0	0	1
5.75 to 12.4	1	0	0

Halfrate and OvSmp set how the clock detect and recover (CDR) circuit samples. See the SERDES PLL section for an explanation of how that circuit blocks works and the role of PLLDiv in the block.

EQUALIZATION MODE SETUP

Set EqMode = 1 for a low power setting. Select this mode if the insertion loss in the printed circuit board (PCB) is less than 12 dB. For insertion losses greater than 12 dB but less than 17.5 dB, set EqMode = 0. More details can be found in the Equalization section.

LINK LATENCY SETUP

This section describes the steps necessary to guarantee multichip deterministic latency in Subclass 1 and to guarantee synchronization of links within a device in Subclass 0. Use this section to fill in LMFCDel, LMFCVar, and Subclass in the Step 5: Data Link Layer section. For more information, see the Syncing LMFC Signals section.

Subclass Setup

The AD9135/AD9136 support JESD204B Subclass 0 and Subclass 1 operation.

Subclass 1

This mode gives deterministic latency and allows links to be synced to within ½ DAC clock periods. It requires an external SYSREF± signal that is accurately phase aligned to the DAC clock.

Subclass 0

This mode does not require any signal on the SYSREF± pins, which can be left disconnected.

Subclass 0 still requires that all lanes arrive within the same LMFC cycle and that the two DACs must be synchronized to each other; they are synchronized to an internal clock instead of to the SYSREF± signal.

Set Subclass to 0 or 1 as desired.

Link Delay Setup

LMFCVar and LMFCDel are used to impose delays such that all lanes in a system arrive in the same LMFC cycle.

The unit used internally for delays is the period of the internal processing clock (PClock), whose rate is 1/40th the lane rate. Delays that are not in PClock cycles must be converted before they are used.

Some useful internal relationships are defined by

$$PClockPeriod = 40/LaneRate$$

PClockPeriod can be used to convert from time to PClock cycles when needed.

$$PClockFactor = 4/F \text{ (frames per PClock)}$$

PClockFactor is used to convert from units of PClock cycles to FrameClock cycles, which is needed to set LMFCDel in Subclass 1.

$$PClocksPerMF = K/PClockFactor \text{ (PClocks per LMFC cycle)}$$

where *PClocksPerMF* is the number or PClock cycles in a multiframe cycle.

The values for PClockFactor and PClockPerMF are given per JESD mode in Table 31.

Table 31. PClockFactor and PClockPerMF

JESD Mode ID	8	9	10	11	12	13
PClockFactor	4	4	2	4	4	2
PClockPerMF (K = 32)	8	8	16	8	8	16
PClockPerMF (K = 16)	N/A[1]	N/A[1]	8	N/A[1]	N/A[1]	8

[1] N/A means not applicable.

With Known Delays

With information about all the system delays, LMFCVar and LMFCDel can be calculated directly.

RxFixed (the fixed receiver delay in PClock cycles) and RxVar (the variable receiver delay in PClock cycles) can be found in Table 8. TxFixed (the fixed transmitter delay in PClock cycles) and TxVar (the variable receiver delay in PClock cycles) can be found in the data sheet of the transmitter used. PCBFixed (the fixed PCB trace delay in PClock cycles) can be extracted from software; because this is generally much smaller than a PClock cycle, it can also be omitted. For both the PCB and transmitter delays, convert the delays into PClock cycles.

For each lane,

$$MinDelayLane = \text{floor}(RxFixed + TxFixed + PCBFixed)$$

$$MaxDelayLane = \text{ceiling}(RxFixed + RxVar + TxFixed + TxVar + PCBFixed))$$

For safety, add a guard band of 1 PClock cycle to each end of the link delay as in the following equations:

$$LMFCVar = (MaxDelay + 1) - (MinDelay - 1)$$

where:
MinDelay is the minimum of all *MinDelayLane* values across lanes, links, and devices.
MaxDelay is the maximum of all *MaxDelayLane* values across lanes, links, and devices.

Note that if LMFCVar must be more than 10, the AD9135/AD9136 cannot tolerate the variable delay in the system.

For Subclass 1

$$LMFCDel = ((MinDelay - 1) \times PClockFactor) \% K$$

For Subclass 0

$$LMFCDel = (MinDelay - 1) \% PClockPerMF$$

Program the same LMFCDel and LMFCVar across all links and devices.

See the Link Delay Setup Example, with Known Delays section for an example calculation.

Without Known Delays

If comprehensive delay information is not available or known, the AD9135/AD9136 can read back the link latency between the local LMFC for each link ($LMFC_{RX}$) and the last arriving LMFC boundary in PClock cycles. This information is then used to calculate LMFCVar and LMFCDel.

For each link (on each device),

1. Power up the board.
2. Follow the steps in Table 15 through Table 21 of the Device Setup Guide.
3. Set the subclass and perform a sync. For one-shot sync, perform the writes in Table 32. See the Syncing LMFC Signals section for alternate sync modes.
4. Record DYN_LINK_LATENCY_0 (Register 0x302) as a value of Delay for that link and power cycle.
5. Record DYN_LINK_LATENCY_1 (Register 0x303) as a value of Delay for that link and power cycle the system.

Repeat Step 1 to Step 5 twenty times for each device in the system. Keep a single list of the Delay values across all runs and devices.

Table 32. Register Configuration and Procedure for One-Shot Sync

Addr.	Bit. No.	Value[1]	Variable	Description
0x301		0x	Subclass	Set subclass
0x03A		0x01		Set sync mode to one-shot sync
0x03A		0x81		Enable the sync machine
0x03A		0xC1		Arm the sync machine
SYSREF± Signal				If Subclass = 1, ensure that at least one SYSREF± edge is sent to the device
0x300		0x		Enable the links
	6		CheckSumMode	See the JESD204B Setup section
	3		DualLink	See the JESD204B Setup section
	2		CurrentLink	Set to 0 to access Link 0 status or 1 for Link 1 status readbacks. See the JESD204B Setup section.
	[1:0]		EnLinks	EnLinks = 3 if in DualLink mode to enable Link 0 and Link 1; EnLinks = 1 if not in DualLink mode to enable Link 0

[1] 0x denotes a register value that the user must fill in. See the Variable and Description columns for information on selecting the appropriate register value.

The list of Delay values is used to calculate LMFCDel and LMFCVar, however, first some of the Delay values may need to be remapped.

The maximum possible value for DYN_LINK_LATENCY_x is one less than the number of PClocks in a multiframe (PClocksPerMF). It is possible that a rollover condition may be encountered; that is, the set of recorded Delay values may roll over the edge of a multiframe. If so, Delay values may be near both 0 and PClocksPerMF. If this occurs, add PClocksPerMF to the set of values near 0.

For example, for Delay value readbacks of 6, 7, 0, and 1, the 0 and 1 Delay values must be remapped to 8 and 9, making the new set of Delay values 6, 7, 8, and 9.

Across power cycles, links, and devices,

- MinDelay is the minimum of all Delay measurements
- MaxDelay is the maximum of all Delay measurements

For safety, a guard band of 1 PClock cycle is added to each end of the link delay and calculate LMFCVar and LMFCDel with the following equation:

$$LMFCVar = (MaxDelay + 1) - (MinDelay - 1)$$

Note that if LMFCVar must be more than 10, the AD9135/AD9136 cannot tolerate the variable delay in the system.

For Subclass 1

$$LMFCDel = ((MinDelay - 1) \times PClockFactor)$$

For Subclass 0

$$LMFCDel = (MinDelay - 1) \% PClockPerMF$$

Program the same LMFCDel and LMFCVar across all links and devices.

See the Link Delay Setup Example, Without Known Delay section for an example calculation.

CROSSBAR SETUP

Register 0x308 to Register 0x30B allow arbitrary mapping of physical lanes (SERDINx±) to logical lanes used by the SERDES deframers.

Table 33. Crossbar Registers

Address	Bits	Logical Lane
0x308	[2:0]	LOGICAL_LANE0_SRC
0x308	[5:3]	LOGICAL_LANE1_SRC
0x309	[2:0]	LOGICAL_LANE2_SRC
0x309	[5:3]	LOGICAL_LANE3_SRC
0x30A	[2:0]	LOGICAL_LANE4_SRC
0x30A	[5:3]	LOGICAL_LANE5_SRC
0x30B	[2:0]	LOGICAL_LANE6_SRC
0x30B	[5:3]	LOGICAL_LANE7_SRC

Write each LOGICAL_LANEy_SRC with the number (x) of the desired physical lane (SERDINx±) from which to receive data. By default, all logical lanes use the corresponding physical lane as their data source. For example, by default LOGICAL_LANE0_SRC = 0, meaning that Logical Lane 0 receives data from Physical Lane 0 (SERDIN0±). To use SERDIN4± as the source for Logical Lane 0, write LOGICAL_LANE0_SRC = 4.

JESD204B SERIAL DATA INTERFACE

JESD204B OVERVIEW

The AD9135/AD9136 have eight JESD204B data ports that receive data. The eight JESD204B ports can be configured as part of a single JESD204B link or as part of two separate JESD204B links (dual-link mode) that share a single system reference (SYSREF±) and device clock (CLK±).

The JESD204B serial interface hardware consists of three layers: the physical layer, the data link layer, and the transport layer. These sections of the hardware are described in subsequent sections, including information for configuring every aspect of the interface. Figure 43 shows the communication layers implemented in the AD9135/AD9136 serial data interface to recover the clock and deserialize, descramble, and deframe the data before it is sent to the digital signal processing section of the device.

The physical layer establishes a reliable channel between the transmitter and the receiver, the data link layer unpacks the data into octets and descrambles the data, and the transport layer receives the descrambled JESD204B frames and converts them to DAC samples.

A number of JESD204B parameters (L, F, K, M, N, NP, S, HD, and Scrambling) defines how the data is packed and instruct the device how to turn the serial data into samples. These parameters are defined in detail in the Transport Layer section.

Only certain combinations of parameters are supported. Each supported combination is called a mode. In total, six modes are supported by the AD9135/AD9136. There are three supported single-link modes, as described in Table 35, and three modes that can operate in either single- or dual-link mode, as described in Table 34. These tables show the associated clock rates when the lane rate is 10 Gbps.

For a particular application, the number of converters to use (M) and DataRate are known. Calculate LaneRate and number of lanes (L) as follows:

$$DataRate = (DACRate)/(InterpolationFactor)$$
$$LaneRate = (20 \times DataRate \times M)/L$$

where *LaneRate* must be between 1.44 Gbps and 12.4 Gbps.

Achieving and recovering synchronization of the lanes is very important. To simplify the interface to the transmitter, the AD9135/AD9136 designate a master synchronization signal for each JESD204B link. In single-link mode, $\overline{\text{SYNCOUT0}}$± is used as the master signal for all lanes; in dual-link mode, $\overline{\text{SYNCOUT0}}$± is used as the master signal for Link 0, and $\overline{\text{SYNCOUT1}}$± is used as the master signal for Link 1. If any lane in a link loses synchronization, a resynchronization request is sent to the transmitter via the synchronization signal of the link. The transmitter stops sending data and instead sends synchronization characters to all lanes in that link until resynchronization is achieved.

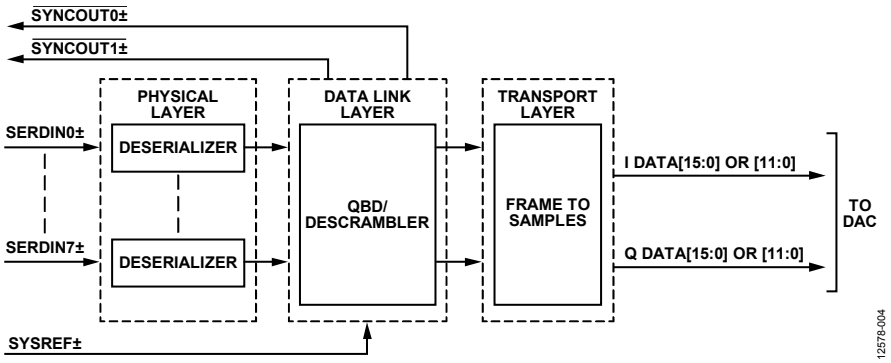


Figure 43. Functional Block Diagram of Serial Link Receiver

Table 34. Single-Link and Dual-Link JESD204B Operating Modes

	Mode		
Parameter	**8**	**9**	**10**
M (Converter Counts)	1	1	1
L (Lane Counts)	4	2	1
S ((Samples per Converter) per Frame)	2	1	1
F ((Octets per Frame) per Lane)	1	1	2
Example Clocks for 10 Gbps Lane Rate			
PClock Rate (MHz)	250	250	250
Frame Rate (MHz)	1000	1000	500
Data Rate (MHz)	2000	1000	500

Table 35. Single-Link JESD204B Operating Modes

	Mode		
Parameter	**11**	**12**	**13**
M (Converter Count) (Tx setting)	2	2	2
AD9135 and AD9136 M Setting[1] (Rx Setting)	1	1	1
L (Lane Count) (Tx setting)	8	4	2
AD9135 and AD9136 L Setting[1] (Rx Setting)	4	2	1
S ((Samples per Converter) per Frame)	2	1	1
F ((Octets per Frame) per Lane)	1	1	2
Example Clocks for 10 Gbps Lane Rate			
PClock Rate (MHz)	250	250	250
Frame Rate (MHz)	1000	1000	500
Data Rate (MHz)	2000	1000	500

[1] Note that for Mode 11 to Mode 13, the M and L parameters programmed on the receive side do not match the parameters on the transmit side. The parameters on the transmit side reflect the true number of converters and lanes per link.

PHYSICAL LAYER

The physical layer of the JESD204B interface, hereafter referred to as the deserializer, has eight identical channels. Each channel consists of the terminators, an equalizer, a clock and data recovery (CDR) circuit, and the 1:40 demux function (see Figure 45).

JESD204B data is input to the AD9135/AD9136 via the SERDINx± 1.2 V differential input pins as per the JESD204B specification.

Interface Power-Up and Input Termination

Before using the JESD204B interface, it must be powered up by setting Register 0x200[0] = 0. In addition, each physical lane that is not being used (SERDINx±) must be powered down. To do so, set the corresponding Bit x for Physical Lane x in Register 0x201 to 0 if the physical lane is being used, and to 1 if it is not being used.

The AD9135/AD9136 autocalibrate the input termination to 50 Ω. Before running the termination calibration, write to Register 0x2AA, Register 0x2AB, Register 0x2B1, and Register 0x2B2 as described in Table 36 to guarantee proper calibration. The termination calibration begins when Register 0x2A7[0] and Register 0x2AE[0] transition from low to high. Register 0x2A7 controls autocalibration for PHY 0, PHY 1, PHY 6, and PHY 7. Register 0x2AE controls autocalibration for PHY 2, PHY 3, PHY 4, and PHY 5.

The PHY termination autocalibration routine is shown in Table 36.

Table 36. PHY Termination Autocalibration Routine

Address	Value	Description
0x2AA	0xB7	SERDES interface termination configuration
0x2AB	0x87	SERDES interface termination configuration
0x2B1	0xB7	SERDES interface termination configuration
0x2B2	0x87	SERDES interface termination configuration
0x2A7	0x01	Autotune PHY terminations
0x2AE	0x01	Autotune PHY terminations

The input termination voltage of the DAC is sourced externally via the V_{TT} pins (Pin 21, Pin 25, Pin 42, and Pin 46). Set V_{TT} by connecting it to SVDD12. It is recommended that the JESD204B inputs be ac-coupled to the JESD204B transmit device using 100 nF capacitors.

Receiver Eye Mask

The AD9135/AD9136 comply with the JESD204B specification regarding the receiver eye mask and are capable of capturing data that complies with this mask. Figure 44 shows the receiver eye mask normalized to the data rate interval with a V_{TT} swing of 600 mV. See the JESD204B specification for more information regarding the eye mask and permitted receiver eye opening.

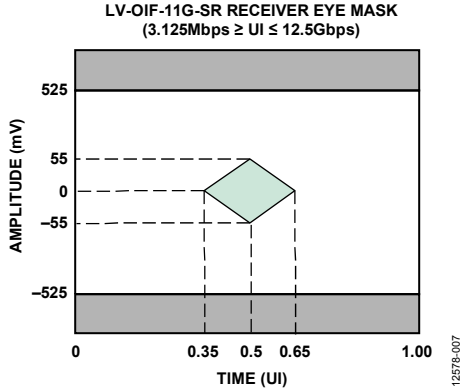


Figure 44. Receiver Eye Mask

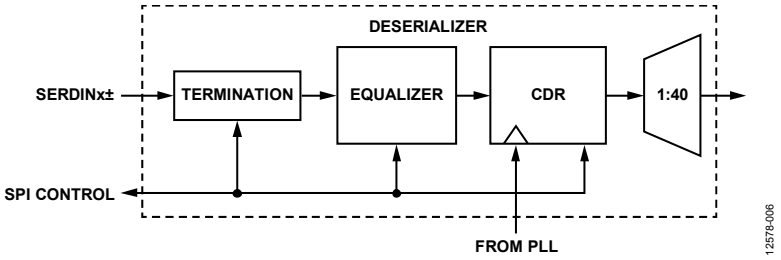


Figure 45. Deserializer Block Diagram

Clock Relationships

The following clocks rates are used throughout the rest of the JESD204B section. The relationship between any of the clocks can be derived from the following equations:

$$DataRate = (DACRate)/(InterpolationFactor)$$

$$LaneRate = (20 \times DataRate \times M)/L$$

$$ByteRate = LaneRate/10$$

where:
M is the JESD204B parameter for converters per link.
L is the JESD204B parameter for lanes per link.

This relationship comes from 8-bit/10-bit encoding, where each byte is represented by 10 bits.

$$PClockRate = ByteRate/4$$

The processing clock is used for a quad-byte decoder.

$$FrameRate = ByteRate/F$$

where *F* is defined as bytes per frame per lane.

$$PClockFactor = FrameRate/PClockRate = 4/F$$

where *F* is the JESD204B parameter for octets per frame per lane.

SERDES PLL

Functional Overview of the SERDES PLL

The independent SERDES PLL uses integer-N techniques to achieve clock synthesis. The entire SERDES PLL is integrated on-chip, including the VCO and the loop filter. The SERDES PLL VCO operates over the range of 5.65 GHz to 12.04 GHz.

In the SERDES PLL, a VCO divider block divides the VCO clock by 2 to generate a 2.825 GHz to 6.2 GHz quadrature clock for the deserializer cores. This clock is the input to the clock and data recovery block that is described in the Clock and Data Recovery section.

The reference clock to the SERDES PLL is always running at a frequency, f_{REF}, that is equal to 1/40 of the lane rate (PClockRate). This clock is divided by the DivFactor value to deliver a clock to the PFD block that is between 35 MHz and 80 MHz. Table 37 includes the respective SERDES_PLL_DIV_MODE register settings for each of the desired DivFactor options available.

Table 37. SERDES PLL Divider Settings

LaneRate (Gbps)	Divide by (DivFactor)	SERDES_PLL_DIV_MODE, Register 0x289[1:0]
1.44 to 3.1	1	2
2.88 to 6.2	2	1
5.75 to 12.4	4	0

Register 0x280 controls the synthesizer enable and recalibration.

To enable the SERDES PLL, first set the PLL divider register according to Table 37, and then enable the SERDES PLL by writing 1 to Register 0x280[0].

Confirm that the SERDES PLL is working by reading Register 0x281. If Register 0x281[0] = 1, the SERDES PLL has locked. If Register 0x281[3] = 1, the SERDES PLL was successfully calibrated. If Register 0x281[4] or Register 0x281[5] are high, the PLL has reached the upper or lower end of its calibration band and must be recalibrated by writing 0 and then 1 to Register 0x280[2].

SERDES PLL Fixed Register Writes

To optimize the SERDES PLL across all operating conditions, the register writes in Table 38 are recommended.

Table 38. SERDES PLL Fixed Register Writes

Address	Value	Description
0x284	0x62	Optimal SERDES PLL loop filter
0x285	0xC9	Optimal SERDES PLL loop filter
0x286	0x0E	Optimal SERDES PLL loop filter
0x287	0x12	Optimal SERDES PLL charge pump
0x28A	0x7B	Optimal SERDES PLL VCO LDO
0x28B	0x00	Optimal SERDES PLL configuration
0x290	0x89	Optimal SERDES PLL VCO varactor
0x294	0x24	Optimal SERDES PLL charge pump
0x296	0x03	Optimal SERDES PLL VCO
0x297	0x0D	Optimal SERDES PLL VCO
0x299	0x02	Optimal SERDES PLL configuration
0x29A	0x8E	Optimal SERDES PLL VCO varactor
0x29C	0x2A	Optimal SERDES PLL charge pump
0x29F	0x78	Optimal SERDES PLL VCO varactor
0x2A0	0x06	Optimal SERDES PLL VCO varactor

SERDES PLL IRQ

SERDES PLL lock and lost signals are available as IRQ events. Use Register 0x01F[3:2] to enable these signals, and then use Register 0x023[3:2] to read back their statuses and reset the IRQ signals. See the Interrupt Request Operation section for more information.

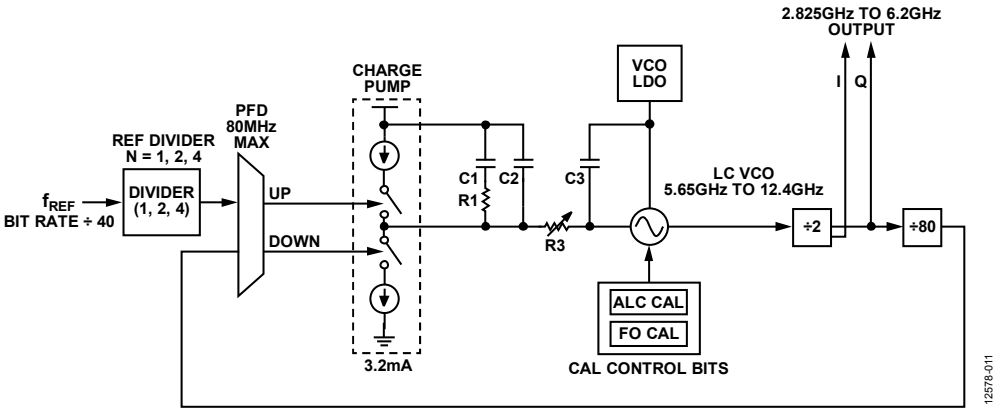


Figure 46. SERDES PLL Synthesizer Block Diagram Including VCO Divider Block

Clock and Data Recovery

The deserializer is equipped with a CDR circuit. Instead of recovering the clock from the JESD204B serial lanes, the CDR recovers the clocks from the SERDES PLL. The 2.825 GHz to 6.2 GHz output from the SERDES PLL, shown in Figure 46, is the input to the CDR.

A CDR sampling mode must be selected to generate the lane rate clock inside the device. If the desired lane rate is greater than 5.65 GHz, half rate CDR operation must be used. If the desired lane rate is less than 5.65 GHz, disable half rate operation. If the lane rate is less than 2.825 GHz, disable half rate operation and enable 2× oversampling to recover the appropriate lane rate clock. Table 39 gives a breakdown of CDR sampling settings that must be set dependent on the LaneRate.

Table 39. CDR Operating Modes

LaneRate (Gbps)	ENHALFRATE, Register 0x230[5]	CDR_OVERSAMP, Register 0x230[1]
1.44 to 3.1	0	1
2.88 to 6.2	0	0
5.75 to 12.4	1	0

The CDR circuit synchronizes the phase used to sample the data on each serial lane independently. This independent phase adjustment per serial interface ensures accurate data sampling and eases the implementation of multiple serial interfaces on a PCB.

After configuring the CDR circuit, reset it and then release the reset by writing 1 and then 0 to Register 0x206[0].

Power-Down Unused PHYs

Note that any unused and enabled lanes consume extra power unnecessarily. Each lane that is not being used (SERDINx±) must be powered off by writing a 1 to the corresponding bit of PHY_PD (Register 0x201).

Equalization

To compensate for signal integrity distortions for each PHY channel due to PCB trace length and impedance, the AD9135/AD9136 employ an easy to use, low power equalizer on each JESD204B channel. The AD9135/AD9136 equalizers can compensate for insertion losses far greater than required by the JESD204B specification. The equalizers have two modes of operation that are determined by the EQ_POWER_MODE register setting in Register 0x268[7:6]. In low power mode (Register 0x268[7:6] = 2b'01) and operating at the maximum lane rate of 10 Gbps, the equalizer can compensate for up to 12 dB of insertion loss. In normal mode (Register 0x268[7:6] = 2b'00), the equalizer can compensate for up to 17.5 dB of insertion loss. This performance is shown in Figure 47 as an overlay to the JESD204B specification for insertion loss. Figure 47 shows the equalization performance at 10.0 Gbps, near the maximum baud rate for the AD9135/AD9136.

Figure 48 and Figure 49 are provided as points of reference for hardware designers and show the insertion loss for various lengths of well laid out stripline and microstrip transmission lines. See the Hardware Considerations section for specific layout recommendations for the JESD204B channel.

Low power mode is recommended if the insertion loss of the JESD204B PCB channels is less than that of the most lossy supported channel for low power mode (shown in Figure 47). If the insertion loss is greater than that, but still less than that of the most lossy supported channel for normal mode (shown in Figure 47), use normal mode. At 10 Gbps operation, the equalizer in normal mode consumes about 4 mW more power per lane used than in low power equalizer mode. Note that either mode can be used in conjunction with transmitter preemphasis to ensure functionality and/or to optimize for power.

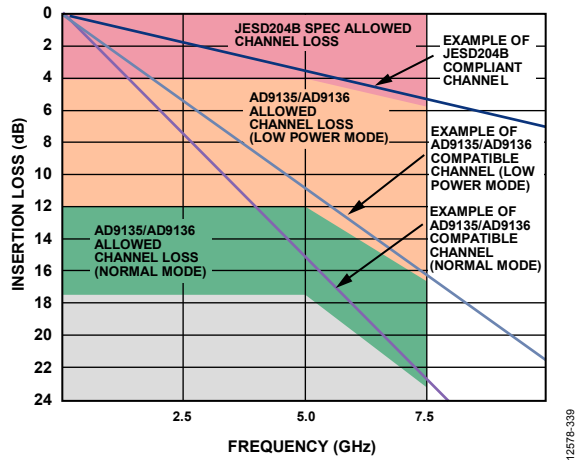


Figure 47. Insertion Loss Allowed

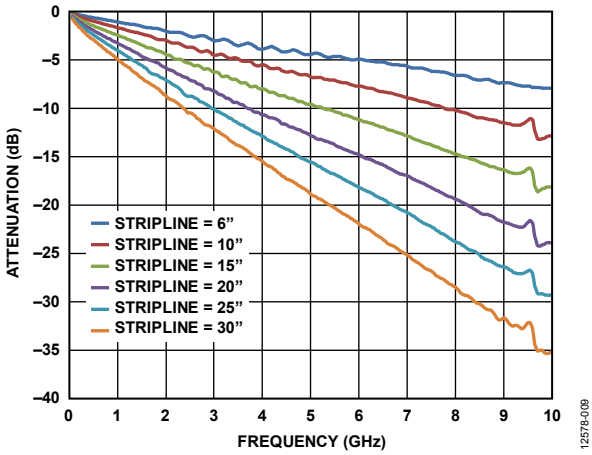


Figure 48. Insertion Loss of 50 Ω Striplines on FR4

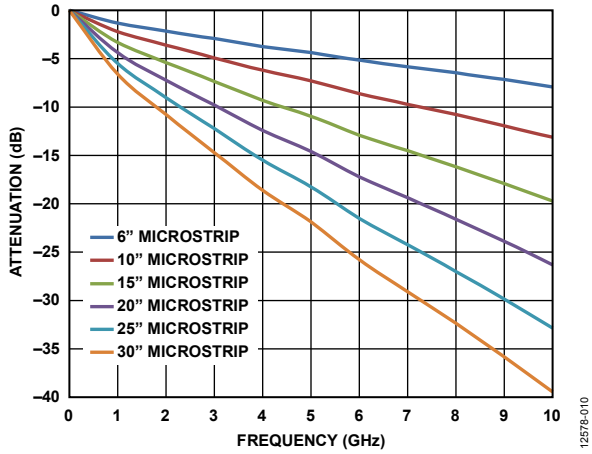


Figure 49. Insertion Loss of 50 Ω Microstrips on FR4

DATA LINK LAYER

The data link layer of the AD9135/AD9136 JESD204B interface accepts the deserialized data from the PHYs and deframes and descrambles them so that data octets are presented to the transport layer to be put into DAC samples. Figure 50 shows the link mode block diagrams for single-link and dual-link configurations and the interaction between the physical layer and logical layer. The DACs can only be configured in sequential order; for example, in Mode 10, when in single-link mode, the AD9135/AD9136 only uses Logical Lane 0 and DAC0. Logical lanes must be set according to Table 29 for the desired mode. See the Mode Configuration Maps section for further details on each of the mode configurations supported. The architecture of the data link layer is shown in Figure 51. The data link layer consists of a synchronization FIFO for each lane, a crossbar switch, a deframer, and descrambler.

The AD9135/AD9136 can operate as a single-link or dual-link high speed JESD204B serial data interface. When operating in dual-link mode, configure both links with the same JESD204B parameters because they share a common device clock and system reference. All eight lanes of the JESD204B interface handle link layer communications such as code group synchronization, frame alignment, and frame synchronization.

The AD9135/AD9136 decode 8-bit/10-bit control characters, allowing marking of the start and end of the frame and alignment between serial lanes. Each AD9135/AD9136 serial interface link can issue a synchronization request by setting its $\overline{\text{SYNCOUT0±}}$/ $\overline{\text{SYNCOUT1±}}$ signal low. The synchronization protocol follows Section 4.9 of the JESD204B standard. When a stream of four consecutive /K/ symbols is received, the AD9135/AD9136 deactivate the synchronization request by setting the $\overline{\text{SYNCOUT0±}}$/ $\overline{\text{SYNCOUT1±}}$ signal high at the next internal LMFC rising edge. Then, the AD9135/AD9136 wait for the transmitter to issue an ILAS. During the ILAS sequence, all lanes are aligned using the /A/ to /R/ character transition as described in the JESD204B Serial Link Establishment section. Elastic buffers hold early arriving lane data until the alignment character of the latest lane arrives. At this point, the buffers for all lanes are released and all lanes are aligned (see Figure 52).

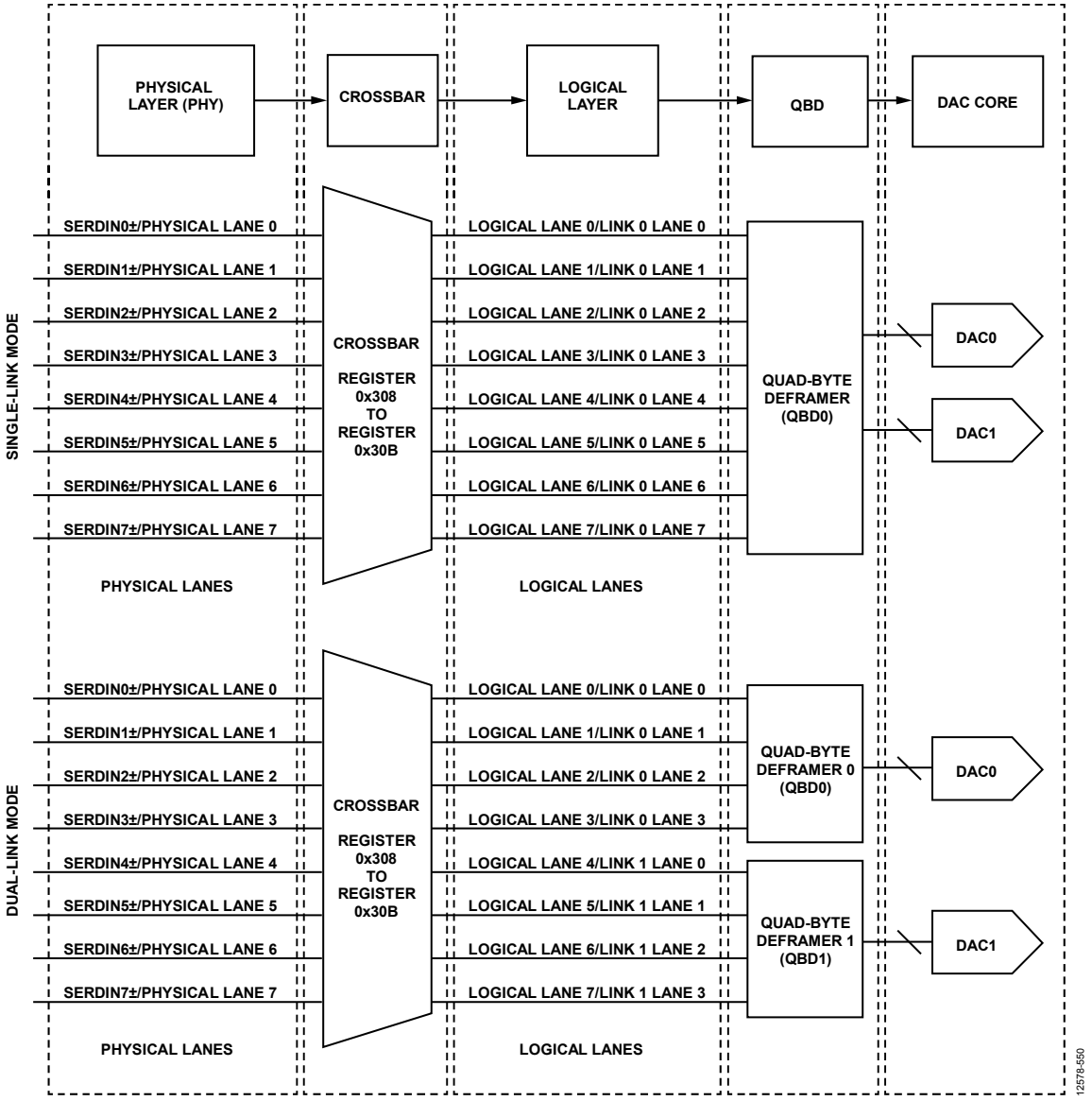


Figure 50. Link Mode Functional Diagram

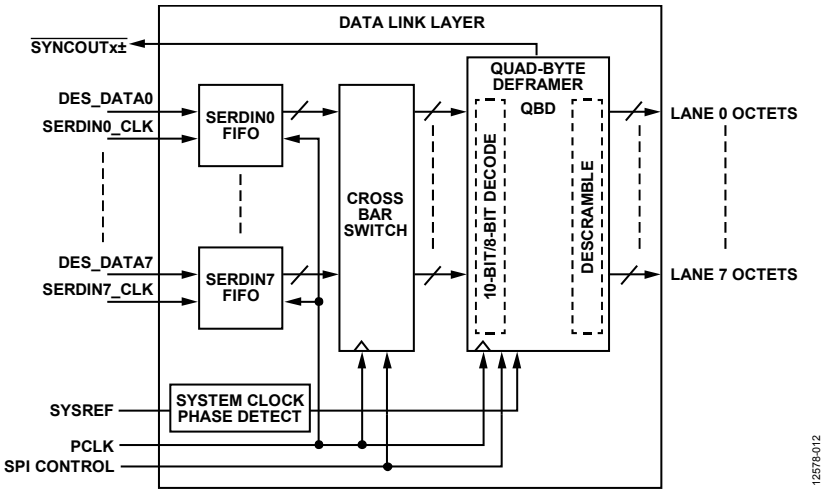


Figure 51. Data Link Layer Block Diagram

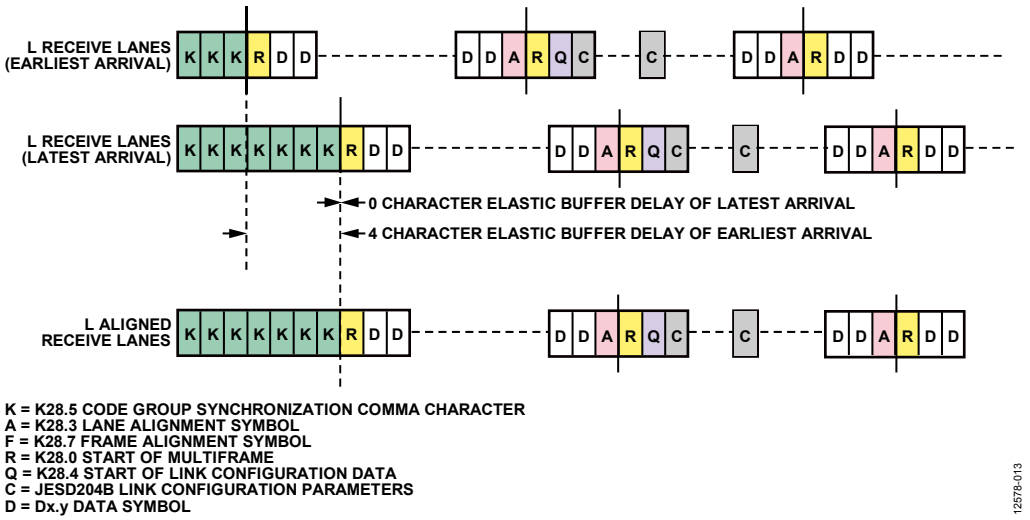


Figure 52. Lane Alignment During ILAS

JESD204B Serial Link Establishment

A brief summary of the high speed serial link establishment process for Subclass 1 is provided. See Section 5.3.3 of the JESD204B specifications document for complete details.

Step 1: Code Group Synchronization

Each receiver must locate K (K28.5) characters in its input data stream. After four consecutive K characters are detected on all link lanes, the receiver block deasserts the $\overline{\text{SYNCOUTx±}}$ signal to the transmitter block at the receiver LMFC edge.

The transmitter captures the change in the $\overline{\text{SYNCOUTx±}}$ signal, and at a future transmitter LMFC rising edge, starts the initial lane alignment sequence (ILAS).

Step 2: Initial Lane Alignment Sequence

The main purposes of this phase are to align all the lanes of the link and to verify the parameters of the link.

Before the link is established, write each of the link parameters to the receiver device to designate how data is sent to the receiver block.

The ILAS consists of four or more multiframes. The last character of each multiframe is a multiframe alignment character, /A/. The first, third, and fourth multiframes are populated with predetermined data values. Note that Section 8.2 of the JESD204B specifications document describes the data ramp that is expected during ILAS. By default, the AD9135/AD9136 do not require this ramp. Register 0x47E[0] can be set high to require the data ramp. The deframer uses the final /A/ of each lane to align the ends of the multiframes within the receiver. The second multiframe contains an R (K28.0), Q (K28.4), and then data corresponding to the link parameters. Additional multiframes can be added to the ILAS if needed by the receiver. By default, the AD9135/AD9136 use four multiframes in the ILAS (this can be changed in Register 0x478). If using Subclass 1, exactly four multiframes must be used.

After the last /A/ character of the last ILAS, multiframe data begins streaming. The receiver adjusts the position of the /A/ character such that it aligns with the internal LMFC of the receiver at this point.

Step 3: Data Streaming

In this phase, data is streamed from the transmitter block to the receiver block.

Optionally, data can be scrambled. Scrambling does not start until the very first octet following the ILAS.

The receiver block processes and monitors the data it receives for errors, including

- Bad running disparity (8-bit/10-bit error)
- Not in table (8-bit/10-bit error)
- Unexpected control character
- Bad ILAS
- Interlane skew error (through character replacement)

If any of these errors exist, they are reported back to the transmitter in one of a few ways (see the JESD204B Error Monitoring section for details).

- $\overline{\text{SYNCOUTx±}}$ signal assertion: resynchronization ($\overline{\text{SYNCOUTx±}}$ signal pulled low) is requested at each error for the last two errors. For the first three errors, an optional resynchronization request can be asserted when the error counter reaches a set error threshold.
- For the first three errors, each multiframe with an error in it causes a small pulse on $\overline{\text{SYNCOUTx±}}$.
- Errors can optionally trigger an IRQ event, which can be sent to the transmitter.

Various test modes for verifying the link integrity can be found in the JESD204B Test Modes section.

Lane FIFO

The FIFOs in front of the crossbar switch and deframer synchronize the samples sent on the high speed serial data interface with the deframer clock by adjusting the phase of the incoming data. The FIFO absorbs timing variations between the data source and the deframer; this allows up to two PClock cycles of drift from the transmitter. The FIFO_STATUS_REG_0 register and FIFO_STATUS_REG_1 register (Register 0x30C and Register 0x30D, respectively) can be monitored to identify whether the FIFOs are full or empty.

Lane FIFO IRQ

An aggregate lane FIFO error bit is also available as an IRQ event. Use Register 0x01F[1] to enable the FIFO error bit, and then use Register 0x023[1] to read back its status and reset the IRQ signal. See the Interrupt Request Operation section for more information.

Crossbar Switch

Register 0x308 to Register 0x30B allow arbitrary mapping of physical lanes (SERDINx±) to logical lanes used by the SERDES deframers.

Table 40. Crossbar Registers

Address	Bits	Logical Lane
0x308	[2:0]	LOGICAL_LANE0_SRC
0x308	[5:3]	LOGICAL_LANE1_SRC
0x309	[2:0]	LOGICAL_LANE2_SRC
0x309	[5:3]	LOGICAL_LANE3_SRC
0x30A	[2:0]	LOGICAL_LANE4_SRC
0x30A	[5:3]	LOGICAL_LANE5_SRC
0x30B	[2:0]	LOGICAL_LANE6_SRC
0x30B	[5:3]	LOGICAL_LANE7_SRC

Write each LOGICAL_LANEy_SRC with the number (x) of the desired physical lane (SERDINx±) from which to receive data. By default, all logical lanes use the corresponding physical lane as their data source. For example, by default LOGICAL_LANE0_SRC = 0; thus, Logical Lane 0 receives data from Physical Lane 0 (SERDIN0±). If instead the user wants to use SERDIN4± as the source for Logical Lane 0, the user must write LOGICAL_LANE0_SRC = 4.

Lane Inversion

Register 0x334 allows inversion of desired logical lanes, which can be used to ease routing of the SERDINx± signals. For each Logical Lane x, set Bit x of Register 0x334 to 1 to invert it.

Deframers

The AD9135/AD9136 consist of two quad-byte deframers (QBDs). Each deframer receives the 8-bit/10-bit encoded data from the deserializer (via the crossbar switch), decodes it, and descrambles it into JESD204B frames before passing it to the transport layer to be converted to DAC samples. The deframer processes four symbols (or octets) per processing clock (PClock) cycle.

In single-link mode, Deframer 0 is used exclusively and Deframer 1 remains inactive. In dual-link mode, both QBDs are active and must be configured separately using the LINK_PAGE bit (Register 0x300[2]) to select which link to configure. The LINK_MODE bit (Register 0x300[3]) is 1 for dual-link, or 0 for single-link.

Each deframer uses the JESD204B parameters that the user has programmed into the register map to identify how the data has been packed and how to unpack it. The JESD204B parameters are described in detail in the Transport Layer section; many of the parameters are also needed in the transport layer to convert JESD204B frames into samples.

Descrambler

The AD9135/AD9136 provide an optional descrambler block using a self synchronous descrambler with a polynomial: $1 + x^{14} + x^{15}$.

Enabling data scrambling reduces spectral peaks that are produced when the same data octets repeat from frame to frame. It also makes the spectrum data independent so that possible frequency selective effects on the electrical interface do not cause data dependent errors. Descrambling of the data is enabled by setting the SCR bit (Register 0x453[7]) to 1.

Syncing LMFC Signals

The first step in guaranteeing synchronization across links and devices begins with syncing the LMFC signals. Each DAC has its own LMFC signal. In Subclass 0, the LMFC signals for each of the two DACs are synchronized to an internal processing clock. In Subclass 1, all LMFC signals (for all DACs and devices) are synchronized to an external SYSREF signal. All LMFC sync registers are paged as described in the DAC Paging section.

SYSREF Signal

The SYSREF signal is a differential source synchronous input that synchronizes the LMFC signals in both the transmitter and receiver in a JESD204B Subclass 1 system to achieve deterministic latency.

The SYSREF signal is an active high signal that is sampled by the device clock rising edge. It is best practice that the device clock and SYSREF signals be generated by the same source, such as the AD9516-1 clock generator, so that the phase alignment between the signals is fixed. When designing for optimum deterministic latency operation, consider the timing distribution skew of the SYSREF signal in a multipoint link system (multichip).

The AD9135/AD9136 support a single pulse or step, or a periodic SYSREF± signal. The periodicity can be continuous, strobed, or gapped periodic. The SYSREF± signal can always be dc-coupled (with a common-mode voltage of 0 V to 2 V). When dc-coupled, a small amount of common-mode current (<500 µA) is drawn from the SYSREF± pins. See Figure 53 for the SYSREF± internal circuit.

To avoid this common-mode current draw, a 50% duty-cycle periodic SYSREF± signal can be used with ac coupling capacitors. If ac-coupled, the ac coupling capacitors combine with the resistors shown in Figure 53 to make a high-pass filter with a RC time constant, $\tau = RC$. Select C such that $\tau > 4/\text{SYSREF}$ frequency. In addition, the edge rate must be sufficiently fast—at least 1.3 V/ns is recommended per Table 5—to meet the SYSREF± vs. DAC clock keepout window (KOW) requirements.

It is possible to use ac-coupled mode without meeting the frequency to time-constant constraint by using SYSREF± hysteresis (Register 0x081 and Register 0x082). However, this increases the DAC clock KOW (Table 5 does not apply) by an amount depending on SYSREF± frequency, level of hysteresis, capacitor choice, and edge rate.

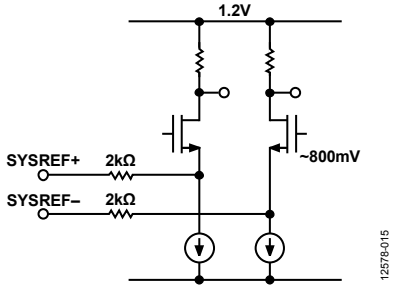


Figure 53. SYSREF± Input Circuit

Sync Processing Modes Overview

The AD9135/AD9136 support various LMFC sync processing modes. These modes are one-shot, continuous, windowed continuous, and monitor modes. All sync processing modes perform a phase check to see that the LMFC is phase aligned to an alignment edge. In Subclass 1, the SYSREF pulse acts as the alignment edge; in Subclass 0, an internal processing clock acts as the alignment edge. If the signals are not in phase, a clock rotation occurs to align the signals. The sync modes are described in the following sections. See the Sync Procedure section for details on the procedure for syncing the LMFC signals.

One-Shot Sync Mode (SYNCMODE = 0x1)

In one-shot sync mode, a phase check occurs on only the first alignment edge that is received after the sync machine is armed. If the phase error is larger than a specified window error tolerance, a phase adjustment occurs. Though an LMFC synchronization occurs only once, the SYSREF signal can still be continuous.

Continuous Sync Mode (SYNCMODE = 0x2)

Continuous mode can only be used in Subclass 1 with a periodic SYSREF signal. In continuous mode, a phase check/alignment occurs on every alignment edge.

Continuous mode differs from one-shot mode in two ways. First, no SPI cycle is required to arm the device; the alignment edge seen after continuous mode is enabled results in a phase check. Second, a phase check (and when necessary, clock rotation) occurs on every alignment edge in continuous mode. The one caveat to the previous statement is that when a phase rotation cycle is underway, subsequent alignment edges are ignored until the logic lane is ready again.

The maximum acceptable phase error (in DAC clock cycles) between the alignment edge and the LMFC edge is set in the error window tolerance register. If continuous sync mode is used with a nonzero error window tolerance, a phase check occurs on every SYSREF± pulse, but an alignment occurs only if the phase error is greater than the specified error window tolerance. If the jitter of the SYSREF signal violates the KOW specification given in Table 5 and therefore causes phase error uncertainty, the error tolerance can be increased to avoid constant clock rotations. Note that this means the latency is less deterministic by the size of the window.

For debug purposes, SYNCARM (Register 0x03A[6]) can be used to inform the user that alignment edges are being received in continuous mode. Because the SYNCARM bit is self cleared after an alignment edge is received, the user can arm the sync (SYNCARM (Register 0x03A[6]) = 1), and then read back SYNCARM. If SYNCARM = 0, the alignment edges are being received and phase checks are occurring. Arming the sync machine in this mode does not affect the operation of the device.

One-Shot Then Monitor Sync Mode (SYNCMODE = 0x9)

In one-shot then monitor mode, the user can monitor the phase error in real time. Use this sync mode with a periodic SYSREF signal. A phase check and alignment occurs on the first alignment edge received after the sync machine is armed. On all subsequent alignment edges, the phase is monitored and reported, but no clock phase adjustment occurs.

The phase error can be monitored on the SYNC_CURRERR_L register (Register 0x03C[3:0]). Immediately after an alignment occurs, CURRERROR = 0 indicates that there is no difference between the alignment edge and the LMFC edge. On every subsequent alignment edge, the phase is checked. If the alignment is lost, the phase error is reported in the SYNC_CURRERR_L register in DAC clock cycles. If the phase error is beyond the selected window tolerance (Register 0x034[2:0]), one bit of Register 0x03D[7:6] is set high depending on whether the phase error is on the low or high side.

When an alignment occurs, snapshots of the last phase error (Register 0x03C[3:0]) and the corresponding error flags (Register 0x03D[7:6]) are placed into readable registers for reference (Register 0x038 and Register 0x039, respectively).

Sync Procedure

The procedure for enabling the sync is as follows:

1. Set Register 0x008 to 0x03 to sync the LMFC for both DAC0 and DAC1.
2. Set the desired sync processing mode. The sync processing mode settings are listed in Table 41.
3. For Subclass 1, set the error window according to the uncertainty of the SYSREF signal relative to the DAC clock and the tolerance of the application for deterministic latency uncertainty. Sync window tolerance settings are given in Table 42.
4. Enable sync by writing 1 to SYNCENABLE (Register 0x03A[7]).
5. If in one-shot mode, arm the sync machine by writing 1 to SYNCARM (Register 0x03A[6]).
6. If in Subclass 1, ensure that at least one SYSREF± pulse is sent to the device.
7. Check the status by reading the following bit fields:
   a) SYNC_BUSY (Register 0x03B[7]) = 0 to indicate that the sync logic is no longer busy.
   b) SYNC_LOCK (Register 0x03B[3]) = 1 to indicate that the signals are aligned. This bit updates on every phase check.
   c) SYNC_WLIM (Register 0x03B[1]) = 0 to indicate that the phase error is not beyond the specified error window. This bit updates on every phase check.
   d) SYNC_ROTATE (Register 0x03B[2]) = 1. If the phases were not aligned before the sync and an alignment occurred, this bit indicates that a clock alignment occurred. This bit is sticky and can be cleared only by writing to the SYNCCLRSTKY control bit (Register 0x03A[5]).
   e) SYNC_TRIP (Register 0x03B[0]) = 1 to indicate that the alignment edge was received and a phase check occurred. This bit is sticky and can be cleared only by writing to the SYNCCLRSTKY control bit (Register 0x03A[5]).

Table 41. Sync Processing Modes

Sync Processing Mode	SYNCMODE (Register 0x03A[3:0])
One-shot	0x01
Continuous	0x02
One-shot then monitor	0x09

Table 42. Sync Window Tolerance

Sync Error Window Tolerance	ERRWINDOW (Register 0x034[2:0])
±½ DAC clock cycles	0x00
±1 DAC clock cycles	0x01
±2 DAC clock cycles	0x02
±3 DAC clock cycles	0x03

LMFC Sync IRQ

The sync status bits (SYNC_LOCK, SYNC_ROTATE, SYNC_TRIP, and SYNC_WLIM) are available as IRQ events.

Use Register 0x021[3:0] to enable the sync status bits for DAC0 and then use Register 0x025[3:0] to read back their statuses and to reset the IRQ signals.

Use Register 0x022[3:0] to enable the sync status bits for DAC1 and then use Register 0x026[3:0] to read back their statuses and to reset the IRQ signals.

See the Interrupt Request Operation section for more information.

Deterministic Latency

JESD204B systems contain various clock domains distributed throughout each system. Data traversing from one clock domain to a different clock domain can lead to ambiguous delays in the JESD204B link. These ambiguities lead to nonrepeatable latencies across the link from power cycle to power cycle with each new link establishment. Section 6 of the JESD204B specification addresses the issue of deterministic latency with mechanisms defined as Subclass 1 and Subclass 2.

The AD9135/AD9136 support JESD204B Subclass 0 and Subclass 1 operation, but not Subclass 2. Write the subclass to Register 0x301[2:0] and once per link to Register 0x458[7:5].

Subclass 0

This mode does not require any signal on the SYSREF± pins, which can be left disconnected.

Subclass 0 still requires that all lanes arrive within the same LMFC cycle and that the two DACs be synchronized to each other.

Minor Subclass 0 Caveats

Because the AD9135/AD9136 require an ILAS, the nonmultiple converter device alignment single lane (NMCDA-SL) case from the JESD204A specification is supported only when using the optional ILAS.

Error reporting using $\overline{\text{SYNCOUTx±}}$ is not supported when using Subclass 0 with F = 1.

Subclass 1

This mode gives deterministic latency and allows links to be synced to within ½ of a DAC clock period. It requires an external SYSREF± signal that is accurately phase aligned to the DAC clock.

DETERMINISTIC LATENCY REQUIREMENTS

Several key factors are required for achieving deterministic latency in a JESD204B Subclass 1 system.

- SYSREF± signal distribution skew within the system must be less than the desired uncertainty.
- SYSREF± setup and hold time requirements must be met for each device in the system.
- The total latency variation across all lanes, links, and devices must be ≤10 PClock periods. This includes both variable delays and the variation in fixed delays from lane to lane, link to link, and device to device in the system.

Link Delay

The link delay of a JESD204B system is the sum of fixed and variable delays from the transmitter, channel, and receiver as shown in Figure 56.

For proper functioning, all lanes on a link must be read during the same LMFC period. Section 6.1 of the JESD204B specification states that the LMFC period must be larger than the maximum link delay. For the AD9135/AD9136, this is not necessarily the case; instead, the AD9135/AD9136 use a local LMFC for each link ($LMFC_{Rx}$) that can be delayed from the SYSREF aligned LMFC. Because the LMFC is periodic, this can account for any amount of fixed delay. As a result, the LMFC period must only be larger than the variation in the link delays, and the AD9135/AD9136 can achieve proper performance with a smaller total latency. Figure 54 and Figure 55 show a case where the link delay is larger than an LMFC period. Note that it can be accommodated by delaying $LMFC_{Rx}$.

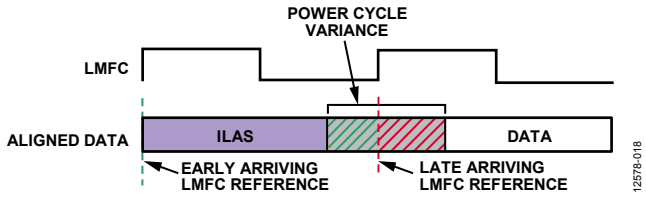


Figure 54. Link Delay > LMFC Period Example

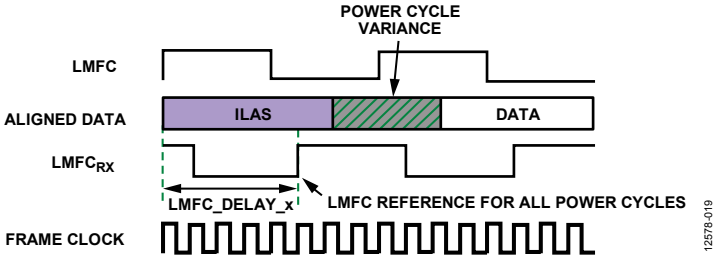


Figure 55. LMFC_DELAY_x, to Compensate for Link Delay > LMFC

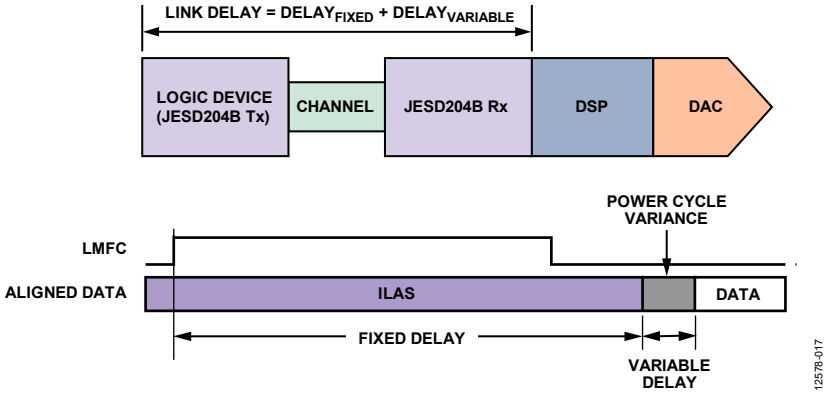


Figure 56. JESD204B Link Delay = Fixed Delay + Variable Delay

The method to set the LMFCDel and LMFCVar values is described in the Link Delay Setup section.

Setting LMFCDel appropriately ensures that all the corresponding data samples arrive in the same LMFC period. Then LMFCVar is written into the receive buffer delay (RBD) to absorb all link delay variation. This ensures that all data samples have arrived before reading. By setting these to fixed values across runs and devices, deterministic latency is achieved.

The RBD described in the JESD204B specification takes values from 1 frame clock cycle to K frame clock cycles, whereas the RBD of the AD9135/AD9136 take values from 0 PClock cycles to 10 PClock cycles. As a result, up to 10 PClock cycles of total delay variation can be absorbed. Because LMFCVar is in PClock cycles, and LMFCDel is in frame clock cycles, a conversion between these two units is needed. The PClockFactor, or number of frame clock cycles per PClock cycle, is equal to 4/F. For more information on this relationship, see the Clock Relationships section.

Two examples follow that show how to determine LMFCVar and LMFCDel. After they are calculated, write LMFCDel into both Register 0x304 and Register 0x305 for all devices in the system, and write LMFCVar to both Register 0x306 and Register 0x307 for all devices in the system.

Link Delay Setup Example, with Known Delays

All the known system delays can be used to calculate LMFCVar and LMFCDel as described in the Link Delay Setup section.

The example shown in Figure 57 is demonstrated in the following steps according to the procedure outlined in the Link Delay Setup section. Note that this example is in Subclass 1 to achieve deterministic latency, which has a PClockFactor (4/F) of two frame clock cycles per PClock Cycle, and uses K = 32 (frames/multiframe). Because PCBFixed << PClockPeriod, PCBFixed is negligible in this example and not included in the calculations.

1. Find the receiver delays using Table 8.
   RxFixed = 17 PClock cycles
   RxVar = 2 PClock cycles
2. Find the transmitter delays. The equivalent table in the example JESD204B core (implemented on a GTH or GTX transceiver on a Virtex-6 FPGA) states that the delay is 56 ± 2 byte clock cycles.
   Because the PClockRate = ByteRate/4 as described in the Clock Relationships section, the transmitter delays in PClock cycles are as follows:
   TxFixed = 54/4 = 13.5 PClock cycles
   TxVar = 4/4 = 1 PClock cycle
3. Calculate MinDelayLane as follows:
   MinDelayLane = floor(*RxFixed* + *TxFixed* + *PCBFixed*)
   = floor(17 + 13.5 + 0)
   = floor(30.5)
   MinDelayLane = 30
4. Calculate MaxDelayLane as follows:
   MaxDelayLane = ceiling(*RxFixed* + *RxVar* + *TxFixed* + *TxVar* + *PCBFixed*))
   = ceiling(17 + 2 + 13.5 + 1 + 0)
   = ceiling(33.5)
   MaxDelayLane = 34
5. Calculate LMFCVar as follows:
   LMFCVar = (*MaxDelay* + 1) − (*MinDelay* − 1)
   = (34 + 1) − (30 − 1) = 35 − 29
   LMFCVar = 6 PClock cycles
6. Calculate LMFCDel as follows:
   LMFCDel = ((*MinDelay* − 1) × *PClockFactor*) % K
   = ((30 − 1) × 2) % 32 = (29 × 2) % 32
   = 58 % 32
   LMFCDel = 26 frame clock cycles
7. Write LMFCDel to both Register 0x304 and Register 0x305 for all devices in the system. Write LMFCVar to both Register 0x306 and Register 0x307 for all devices in the system.

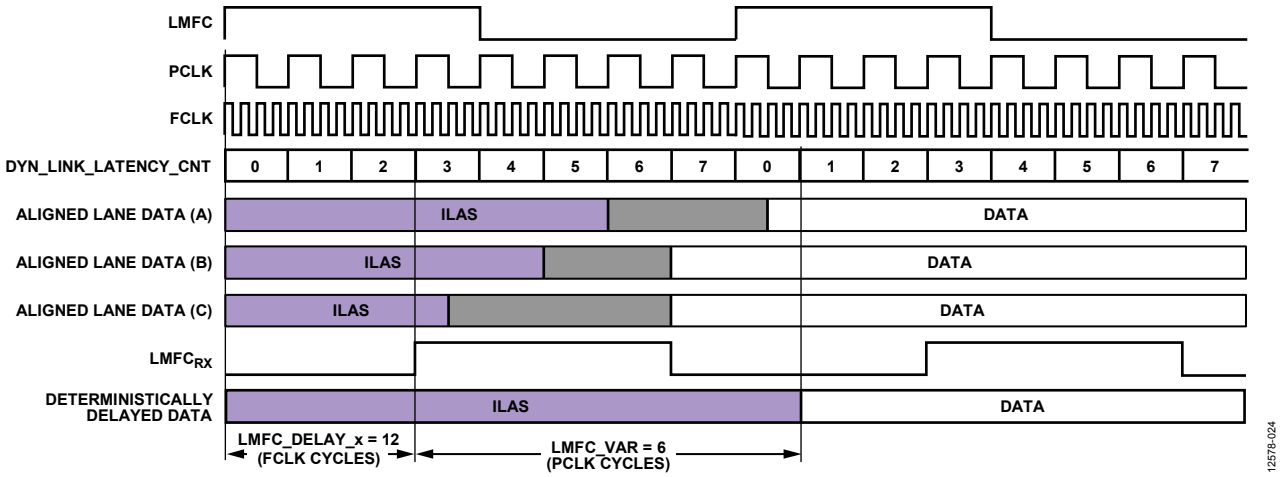


Figure 57. LMFC_DELAY_x Calculation Example

Link Delay Setup Example, Without Known Delay

If the system delays are not known, the AD9135/AD9136 can read back the link latency between $LMFC_{RX}$ for each link and the SYSREF± aligned LMFC. This information is then used to calculate LMFCVar and LMFCDel, as shown in the Without Known Delays section.

Figure 59 shows how DYN_LINK_LATENCY_x (Register 0x302 and Register 0x303) provides a readback showing the delay (in PClock cycles) between $LMFC_{RX}$ and the transition from ILAS to the first data sample. By repeatedly power cycling and taking this measurement, the minimum and maximum delays across power cycles can be determined and used to calculate LMFCVar and LMFCDel.

The example shown in Figure 59 is demonstrated in the following steps according to the procedure outlined in the Without Known Delays section. Note that this example is in Subclass 1 to achieve deterministic latency, which has a PClockFactor (frame clock rate/PClockRate) of 2 and uses K = 16; therefore, PClocksPerMF = 8.

1. In Figure 59, for Link A, Link B, and Link C, the system containing the AD9135/AD9136 (including the transmitter) is power cycled and configured 20 times. The AD9135/AD9136 are configured as described in the Device Setup Guide. Because the point of this exercise is to determine LMFCDel and LMFCVar, the LMFCDel is programmed to 0 and DYN_LINK_LATENCY_x is read from Register 0x302 and Register 0x303 for Link 0 and Link 1, respectively. The variation in the link latency over the 20 runs is shown in Figure 59 in gray.
   Link A gives readbacks of 6, 7, 0, and 1. Note that the set of recorded delay values rolls over the edge of a multiframe at the boundary K/PClockFactor = 8. Add PClocksPerMF = 8 to low set. Delay values range from 6 to 9.
   Link B gives Delay values from 5 to 7.
   Link C gives Delay values from 4 to 7.
2. Calculate the minimum of all Delay measurements across all power cycles, links, and devices:
   MinDelay = min(all *Delay* values) = 4
3. Calculate the maximum of all Delay measurements across all power cycles, links, and devices:
   MaxDelay = max(all *Delay* values) = 9
4. Calculate the total Delay variation (with guard band) across all power cycles, links, and devices:
   LMFCVar = (*MaxDelay* + 1) − (*MinDelay* − 1)
   = (9 + 1) − (4 − 1) = 10 − 3 = 7 PClock cycles
5. Calculate the minimum delay in frame clock cycles (with guard band) across all power cycles, links, and devices:
   LMFCDel = ((*MinDelay* − 1) × *PClockFactor*) % K
   = ((4 − 1) × 2) % 16 = (3 × 2) % 16
   = 6 % 16 = 6 frame clock cycles
6. Write LMFCDel to both Register 0x304 and Register 0x305 for all devices in the system. Write LMFCVar to both Register 0x306 and Register 0x307 for all devices in the system.

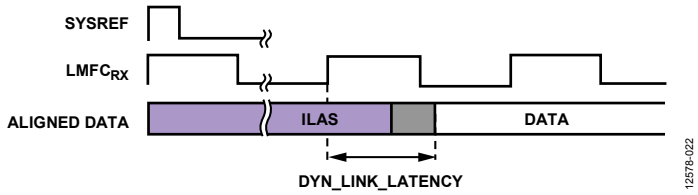


Figure 58. DYN_LINK_LATENCY Illustration

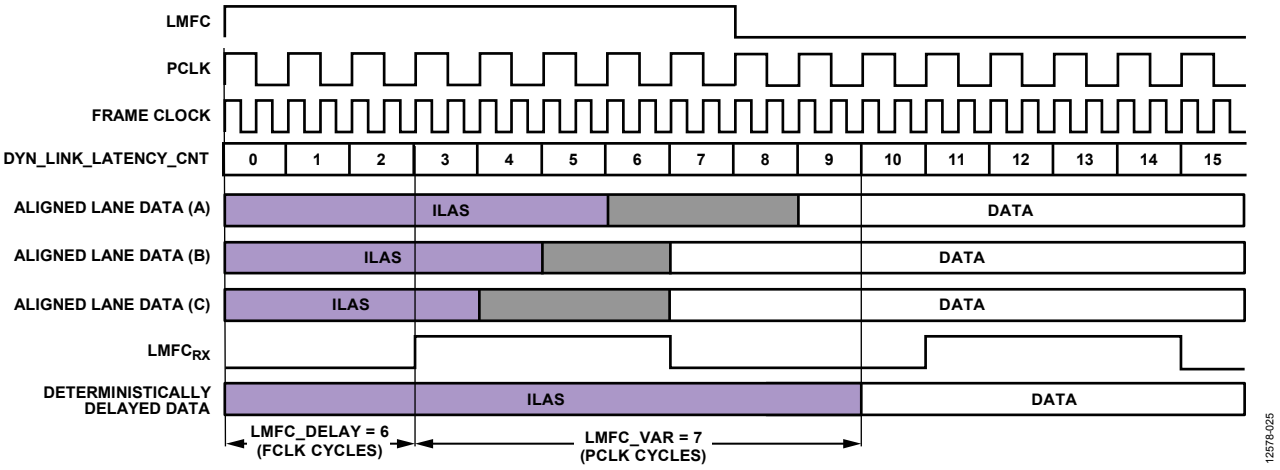


Figure 59. Multilink Synchronization Settings, Derived Method Example

TRANSPORT LAYER

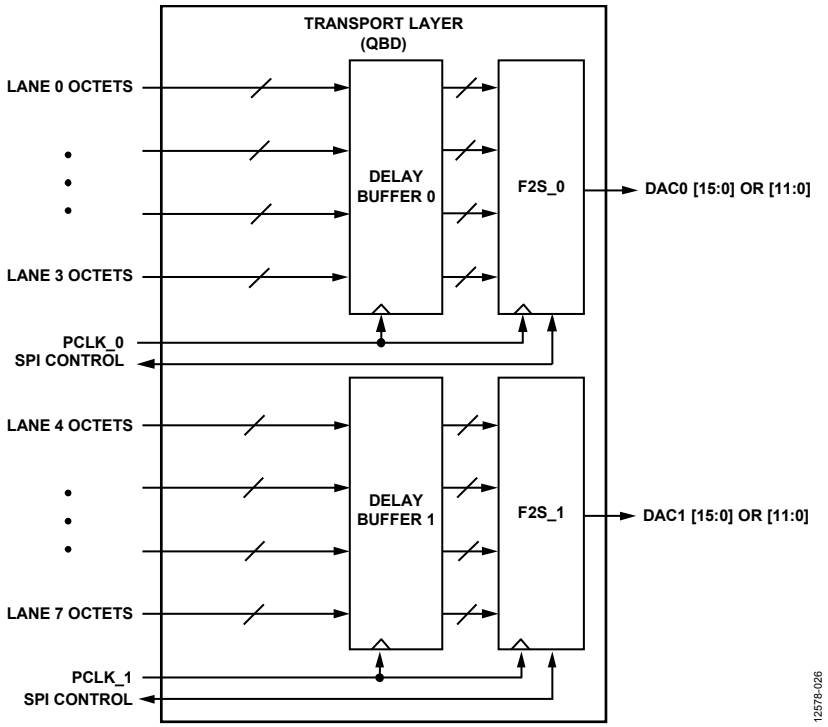


Figure 60. Transport Layer Block Diagram

The transport layer receives the descrambled JESD204B frames and converts them to DAC samples based on the programmed JESD204B parameters shown in Table 43. A number of device parameters are defined in Table 44.

Table 43. JESD204B Transport Layer Parameters

Parameter	Description
F	Number of octets per frame per lane: 1, 2, or 4.
K	Number of frames per multiframe. K = 32 if F = 1, K = 16 or 32 otherwise.
L	Number of lanes per converter device (per link), as follows: 1, 2, 4, or 8 (single-link mode). 1, 2, or 4 (dual-link mode).
M	Number of converters per device (per link), as follows: 1 or 2 (single-link mode). 1 (dual-link mode).
S	Number of samples per converter, per frame: 1 or 2.

Table 44. JESD204B Device Parameters

Parameter	Description
CF	Number of control words per device clock per link. Not supported, must be 0.
CS	Number of control bits per conversion sample. Not supported, must be 0.
HD	High density user data format. Used when samples must be split across lanes. Set to 1 when F = 1, otherwise 0.
N	Converter resolution = 16.
N' (or NP)	Total number of bits per sample = 16.

Certain combinations of these parameters, called JESD204B operating modes, are supported by the AD9135/AD9136. See Table 45 and Table 46 for a list of supported modes, along with their associated clock relationships.

Table 45. Single-Link and Dual-Link JESD204B Operating Modes

	Mode		
Parameter	**8[1]**	**9**	**10**
M (Converter Count)	1	1	1
L (Lane Count)	4	2	1
S (Samples per Converter per Frame)	2	1	1
F (Octets per Frame per Lane)	1	1	2
K[2] (Frames per Multiframe)	32	32	16 or 32
HD (High Density)	1	1	0
N (Converter Resolution)	16	16	16
NP (Bits per Sample)	16	16	16
Example Clocks for 10 Gbps Lane Rate			
PClock Rate (MHz)	250	250	250
Frame Clock Rate (MHz)	250	1000	500
Data Rate (MHz)	250	1000	500

[1] Mode 8 can only be used with 1× interpolation. Other interpolation options are not available in this mode.
[2] K must be 32 in Mode 8 and Mode 9. It can be 16 or 32 in Mode 10.

Table 46. Single-Link JESD204B Operating Modes

	Mode		
Parameter	**11[1]**	**12**	**13**
M (Converter Count)	2	2	2
AD9135/AD9136 M Setting[2]	1	1	1
L (Lane Count)	8	4	2
AD9135/AD9136 L Setting[2]	4	2	1
S (Samples per Converter per Frame)	2	1	1
F (Octets per Frame, per Lane)	1	1	2
K[3] (Frames per Multiframe)	32	32	16 or 32
HD (High Density)	1	1	0
N (Converter Resolution)	16	16	16
NP (Bits per Sample)	16	16	16
Example Clocks for 10 Gbps Lane Rate			
PClock Rate (MHz)	250	250	250
Frame Clock Rate (MHz)	250	250	1000
Data Rate (MHz)	250	250	1000

[1] Mode 11 can only be used with 1× interpolation. Other interpolation options are not available in this mode.
[2] Note that for Mode 11 through Mode 13, the M and L parameters programmed on the receive side do not match the parameters on the transmit side. The parameters on the transmit side reflect the true number of converters and lanes per link.
[3] K must be 32 in Mode 11 and Mode 12. It can be 16 or 32 in Mode 13.

Configuration Parameters

The AD9135/AD9136 modes refer to the link configuration parameters for L, K, M, N, NP, S, and F. Table 47 provides the description and addresses for these settings.

Table 47. Configuration Parameters

JESD204B Setting	Description	Address
L – 1	Number of lanes – 1.	0x453[4:0]
F – 1[1]	Number of ((octets per frame) per lane) – 1.	0x454[7:0]
K – 1	Number of frames per multiframe – 1.	0x455[4:0]
M – 1	Number of converters – 1.	0x456[7:0]
N – 1	Converter bit resolution – 1.	0x457[4:0]
NP – 1	Bit packing per sample – 1.	0x458[4:0]
S – 1	Number of ((samples per converter) per frame) – 1.	0x459[4:0]
HD	High density format. Set to 1 if F = 1. Leave at 0 if F ≠ 1.	0x45A[7]
F[1]	F parameter, in ((octets per frame) per lane).	0x476[7:0]
DID	Device ID. Match the device ID sent by the transmitter.	0x450[7:0]
BID	Bank ID. Match the bank ID sent by the transmitter.	0x451[3:0]
LID0	Lane ID for Lane 0. Match the lane ID sent by the transmitter on Logical Lane 0.	0x452[4:0]
JESDV	JESD204x version. Match the version sent by the transmitter (0x0 = JESD204A, 0x1 = JESD204B).	0x459[7:5]

[1] The values that need to be written in Register 0x454 and Register 0x476 are different, F – 1 and F, respectively.

Data Flow Through the JESD204B Receiver

The link configuration parameters determine how the serial bits on the JESD204B receiver interface are deframed and passed on to the DACs as data samples. Figure 61 shows a detailed flow of the data through the various hardware blocks for Mode 11 (L = 8, M = 2, S = 2, F = 1). Simplified flow diagrams for all other modes are shown in Figure 62 through Figure 66.

Single- and Dual-Link Configuration

The AD9135/AD9136 use the settings contained in Table 45 and Table 46. Mode 8 to Mode 13 can be used for single-link operation. Mode 8 to Mode 10 can also be used for dual-link operation.

To use dual-link mode, set LINK_MODE (Register 0x300[3]) to 1. In dual-link mode, Link 1 must be programmed with identical parameters to Link 0. To write to Link 1, set LINK_PAGE (Register 0x300[2]) to 1.

If single-link mode is being used, a small amount of power can be saved by powering down the output buffer for SYNCOUT1±, which can be done by setting Register 0x203[0] = 1.

Checking Proper Configuration

As a convenience, the AD9135/AD9136 provide some quick configuration checks. Register 0x030[5] is high if an illegal LMFC_DELAY value is used. Register 0x030[3] is high if an unsupported combination of L, M, F, or S is used. Register 0x030[2] is high if an illegal K is used. Register 0x030[1] is high if an illegal SUBCLASSV is used.

Deskewing and Enabling Logical Lanes

After proper configuration, the logical lanes must be deskewed and enabled to capture data.

Set Bit x in Register 0x46C to 1 to deskew Logical Lane x and to 0 if that logical lane is not being used. Then, set Bit x in Register 0x47D to 1 to enable Logical Lane x and to 0 if that logical lane is not being used.

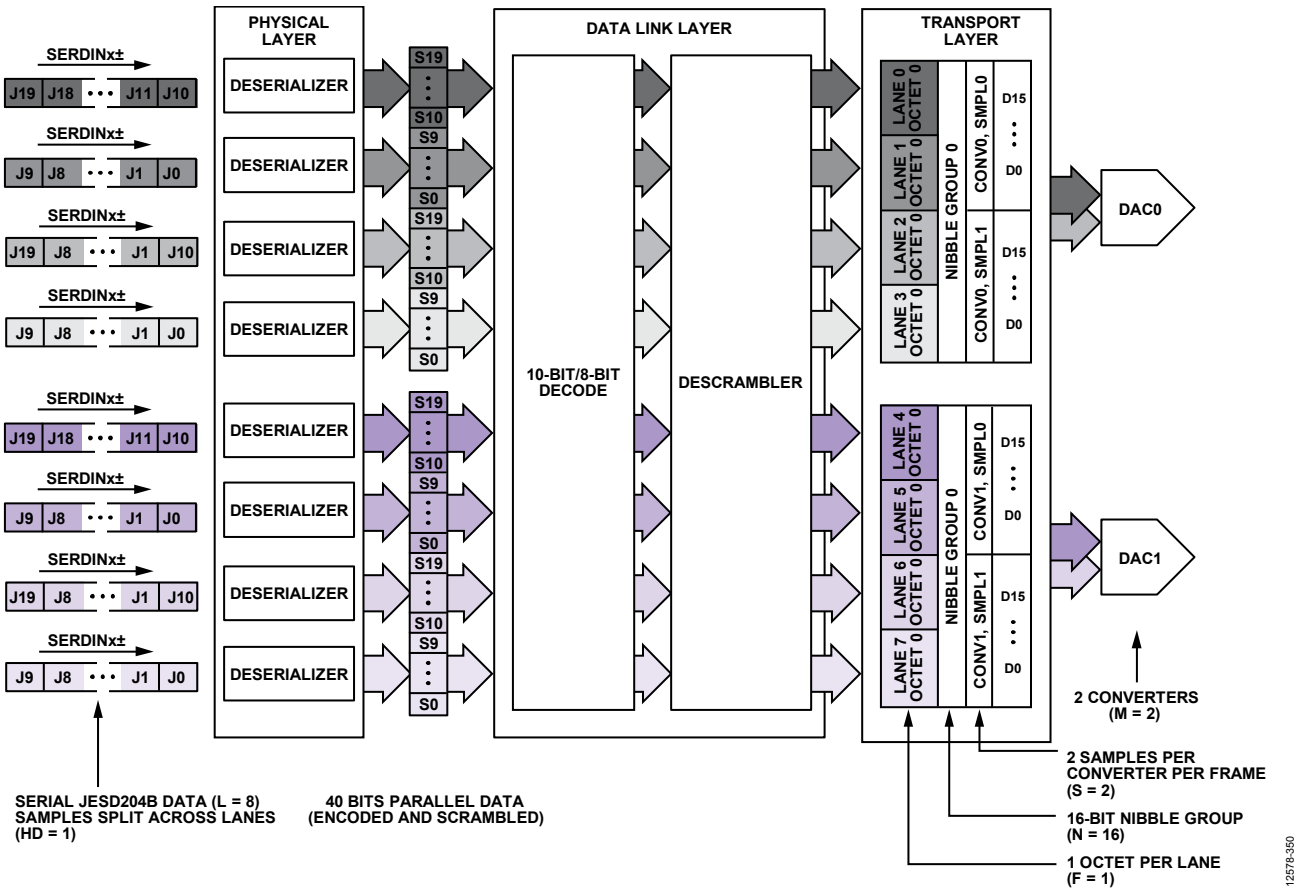


Figure 61. JESD204B Mode 11 Data Deframing

Mode Configuration Maps

Table 48 to Table 53 contain the SPI configuration map for each mode shown in Figure 61 through Figure 66. Figure 61 through Figure 66 show the associated data flow through the deframing process of the JESD204B receiver for each of the modes.

Mode 8 to Mode 13 apply to single-link operation. Mode 8 to Mode 10 also apply to dual-link operation. Register 0x300 must be set accordingly for single- or dual-link operation.

For additional details regarding all the SPI registers, see the Register Maps and Descriptions section.

Table 48. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 8

Address	Setting	Description
0x453	0x03 or 0x83	Register 0x453[7] = 0 or 1: scrambling disabled or enabled, Register 0x453[4:0] = 0x3: L = 4 lanes per link
0x454	0x00	Register 0x454[7:0] = 0x00: F = 1 octet per frame
0x455	0x1F	Register 0x455[4:0] = 0x1F: K = 32 frames per multiframe
0x456	0x00	Register 0x456[7:0] = 0x00: M = 1 converter per link
0x457	0x0F	Register 0x457[7:6] = 0x0: always set CS = 0; Register 0x457[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1; Register 0x458[4:0] = 0xF: NP = 16 bits per sample
0x459	0x21	Register 0x459[7:5] = 0x1: set to JESD204B version; Register 0x459[4:0] = 0x1: S = 2 (samples per converter) per frame
0x45A	0x80	Register 0x45A[7] = 1: HD = 1; Register 0x45A[4:0] = 0x00: always set CF = 0
0x46C	0x0F	Register 0x46C[7:0] = 0x0F: deskew Link Lane 0 to Link Lane 3
0x476	0x01	Register 0x476[7:0] = 0x01: F = 1 octet per frame
0x47D	0x0F	Register 0x47D[7:0] = 0x0F: enable Link Lane 0 to Link Lane 3

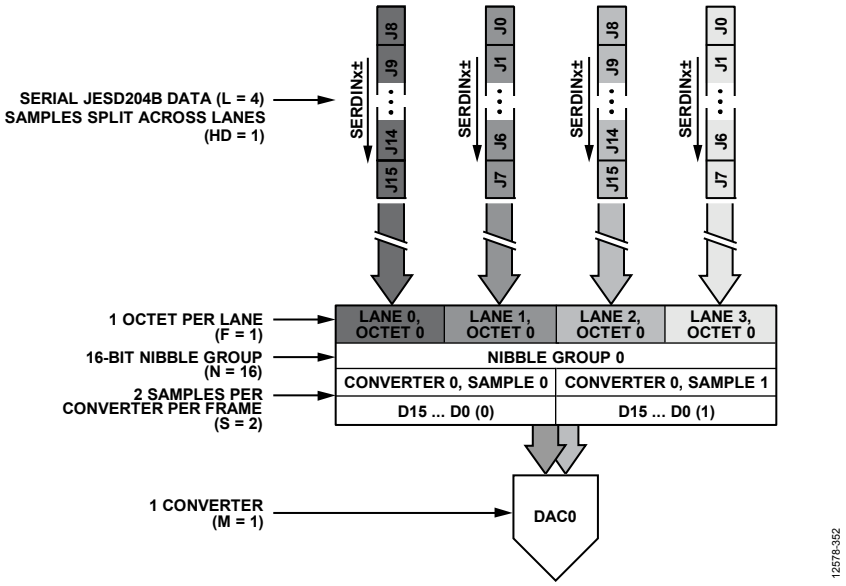


Figure 62. JESD204B Mode 8 Data Deframing

Table 49. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 9

Address	Setting	Description
0x453	0x01 or 0x81	Register 0x453[7] = 0 or 1: scrambling disabled or enabled, Register 0x453[4:0] = 0x1: L = 2 lanes per link
0x454	0x00	Register 0x454[7:0] = 0x00: F = 1 octet per frame
0x455	0x1F	Register 0x455[4:0] = 0x1F: K = 32 frames per multiframe
0x456	0x00	Register 0x456[7:0] = 0x00: M = 1 converter per link
0x457	0x0F	Register 0x457[7:6] = 0x0: always set CS = 0; Register 0x457[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1; Register 0x458[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459[7:5] = 0x1: set to JESD204B version; Register 0x459[4:0] = 0x0: S = 1 (sample per converter) per frame
0x45A	0x80	Register 0x45A[7] = 1: HD = 1; Register 0x45A[4:0] = 0x00: always set CF = 0
0x46C	0x03	Register 0x46C[7:0] = 0x0F: deskew Link Lane 0 and Link Lane 1
0x476	0x01	Register 0x476[7:0] = 0x01: F = 1 octet per frame
0x47D	0x03	Register 0x47D[7:0] = 0x03: enable Link Lane 0 and Link Lane 1

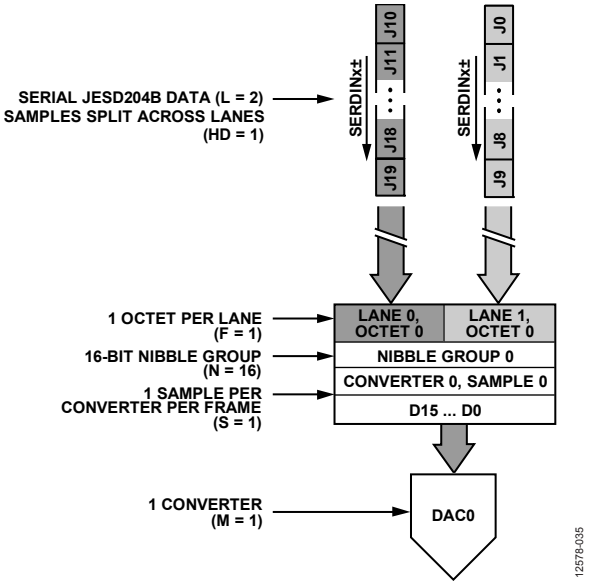


Figure 63. JESD204B Mode 9 Data Deframing

Table 50. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 10

Address	Setting	Description
0x453	0x00 or 0x80	Register 0x453[7] = 0 or 1: scrambling disabled or enabled, Register 0x453[4:0] = 0x0: L = 1 lane per link
0x454	0x01	Register 0x454[7:0] = 0x01: F = 2 octets per frame
0x455	0x0F or 0x1F	Register 0x455[4:0] = 0x0F or 0x1F: K = 16 or 32 frames per multiframe
0x456	0x00	Register 0x456[7:0] = 0x00: M = 1 converter per link
0x457	0x0F	Register 0x457[7:6] = 0x0: always set CS = 0; Register 0x457[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1; Register 0x458[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459[7:5] = 0x1: set to JESD204B version; Register 0x459[4:0] = 0x0: S = 1 (sample per converter) per frame
0x45A	0x00	Register 0x45A[7] = 0: HD = 0; Register 0x45A[4:0] = 0x00: always set CF = 0
0x46C	0x01	Register 0x46C[7:0] = 0x0F: deskew Link Lane 0
0x476	0x02	Register 0x476[7:0] = 0x02: F = 2 octets per frame
0x47D	0x01	Register 0x47D[7:0] = 0x01: enable Link Lane 0

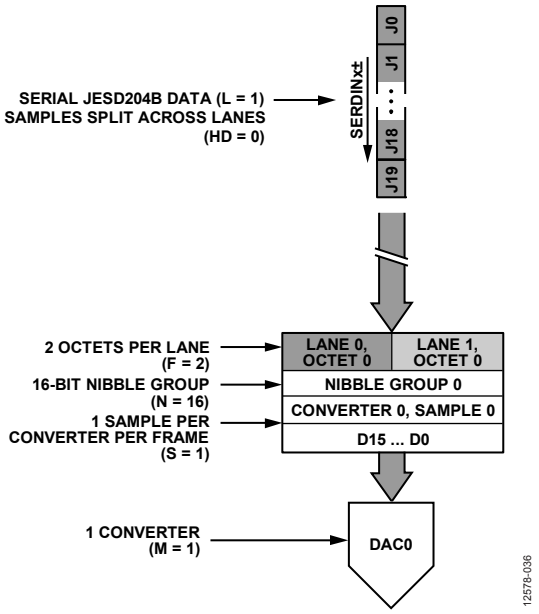


Figure 64. JESD204B Mode 10 Data Deframing

Table 51. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 11

Address	Setting	Description
0x453	0x03 or 0x83	Register 0x453[7] = 0 or 1: scrambling disabled or enabled, Register 0x453[4:0] = 0x3: L = 4 lanes per link (L = 8 on transmit side)[1]
0x454	0x00	Register 0x454[7:0] = 0x00: F = 1 octet per frame
0x455	0x1F	Register 0x455[4:0] = 0x1F: K = 32 frames per multiframe
0x456	0x00	Register 0x456[7:0] = 0x00: M = 1 converter per link (M = 2 on transmit side)[1]
0x457	0x0F	Register 0x457[7:6] = 0x0: always set CS = 0; Register 0x457[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1; Register 0x458[4:0] = 0xF: NP = 16 bits per sample
0x459	0x21	Register 0x459[7:5] = 0x1: set to JESD204B version; Register 0x459[4:0] = 0x1: S = 2 (samples per converter) per frame
0x45A	0x80	Register 0x45A[7] = 1: HD = 1; Register 0x45A[4:0] = 0x00: always set CF = 0
0x46C	0xFF	Register 0x46C[7:0] = 0x0F: deskew Link Lane 0 to Link Lane 7
0x476	0x01	Register 0x476[7:0] = 0x01: F = 1 octet per frame
0x47D	0xFF	Register 0x47D[7:0] = 0x0F: enable Link Lane 0 to Link Lane 7

[1] Note that for Mode 11 through Mode 13, the M and L parameters programmed on the receive side do not match the parameters on the transmit side. The parameters on the transmit side reflect the true number of converters and lanes per link.

See Figure 61 for an illustration of the AD9135/AD9136 JESD204B Mode 11 data deframing process.

Table 52. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 12

Address	Setting	Description
0x453	0x01 or 0x81	Register 0x453[7] = 0 or 1: scrambling disabled or enabled, Register 0x453[4:0] = 0x1: L = 2 lanes per link (L = 4 on transmit side)[1]
0x454	0x00	Register 0x454[7:0] = 0x00: F = 1 octet per frame
0x455	0x1F	Register 0x455[4:0] = 0x1F: K = 32 frames per multiframe
0x456	0x00	Register 0x456[7:0] = 0x00: M = 1 converter per link (M = 2 on transmit side)[1]
0x457	0x0F	Register 0x457[7:6] = 0x0: always set CS = 0; Register 0x457[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1; Register 0x458[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459[7:5] = 0x1: set to JESD204B version; Register 0x459[4:0] = 0x0: S = 1 (sample per converter) per frame
0x45A	0x80	Register 0x45A[7] = 1: HD = 1; Register 0x45A[4:0] = 0x00: always set CF = 0
0x46C	0x33	Register 0x46C[7:0] = 0x0F: deskew Link Lane 0, Link Lane 1, Link Lane 4, and Link Lane 5
0x476	0x01	Register 0x476[7:0] = 0x01: F = 1 octet per frame
0x47D	0x33	Register 0x47D[7:0] = 0x03: enable Link Lane 0, Link Lane 1, Link Lane 4, and Link Lane 5

[1] Note that for Mode 11 through Mode 13, the M and L parameters programmed on the receive side do not match the parameters on the transmit side. The parameters on the transmit side reflect the true number of converters and lanes per link.

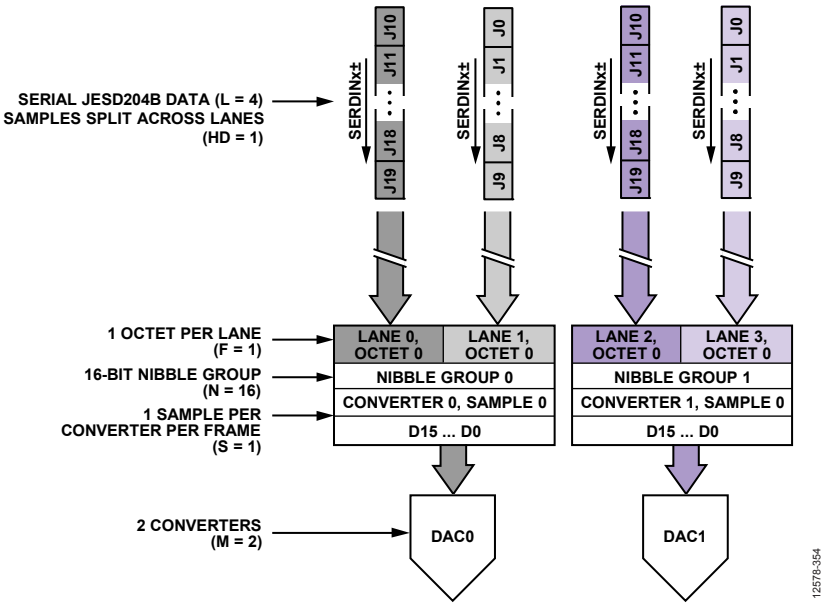


Figure 65. JESD204B Mode 12 Data Deframing

Table 53. SPI Configuration Map—Register Settings for JESD204B Parameters for Mode 13

Address	Setting	Description
0x453	0x00 or 0x80	Register 0x453[7] = 0 or 1: scrambling disabled or enabled, Register 0x453[4:0] = 0x0: L = 1 lane per link (L = 2 on transmit side)[1]
0x454	0x01	Register 0x454[7:0] = 0x01: F = 2 octets per frame
0x455	0x0F or 0x1F	Register 0x455[4:0] = 0x0F or 0x1F: K = 16 or 32 frames per multiframe
0x456	0x00	Register 0x456[7:0] = 0x00: M = 1 converter per link (M = 2 on transmit side)[1]
0x457	0x0F	Register 0x457[7:6] = 0x0: always set CS = 0; Register 0x457[4:0] = 0x0F: N = 16, always set to 16-bit resolution
0x458	0x0F or 0x2F	Register 0x458[7:5] = 0x0 or 0x1: Subclass 0 or Subclass 1; Register 0x458[4:0] = 0xF: NP = 16 bits per sample
0x459	0x20	Register 0x459[7:5] = 0x1: set to JESD204B version; Register 0x459[4:0] = 0x0: S = 1 (sample per converter) per frame
0x45A	0x00	Register 0x45A[7] = 0: HD = 0; Register 0x45A[4:0] = 0x00: always set CF = 0
0x46C	0x11	Register 0x46C[7:0] = 0x0F: deskew Link Lane 0 and Link Lane 4
0x476	0x02	Register 0x476[7:0] = 0x02: F = 2 octets per frame
0x47D	0x11	Register 0x47D[7:0] = 0x01: enable Link Lane 0 and Link Lane 4

[1] Note that for Mode 11 through Mode 13, the M and L parameters programmed on the receive side do not match the parameters on the transmit side. The parameters on the transmit side reflect the true number of converters and lanes per link.

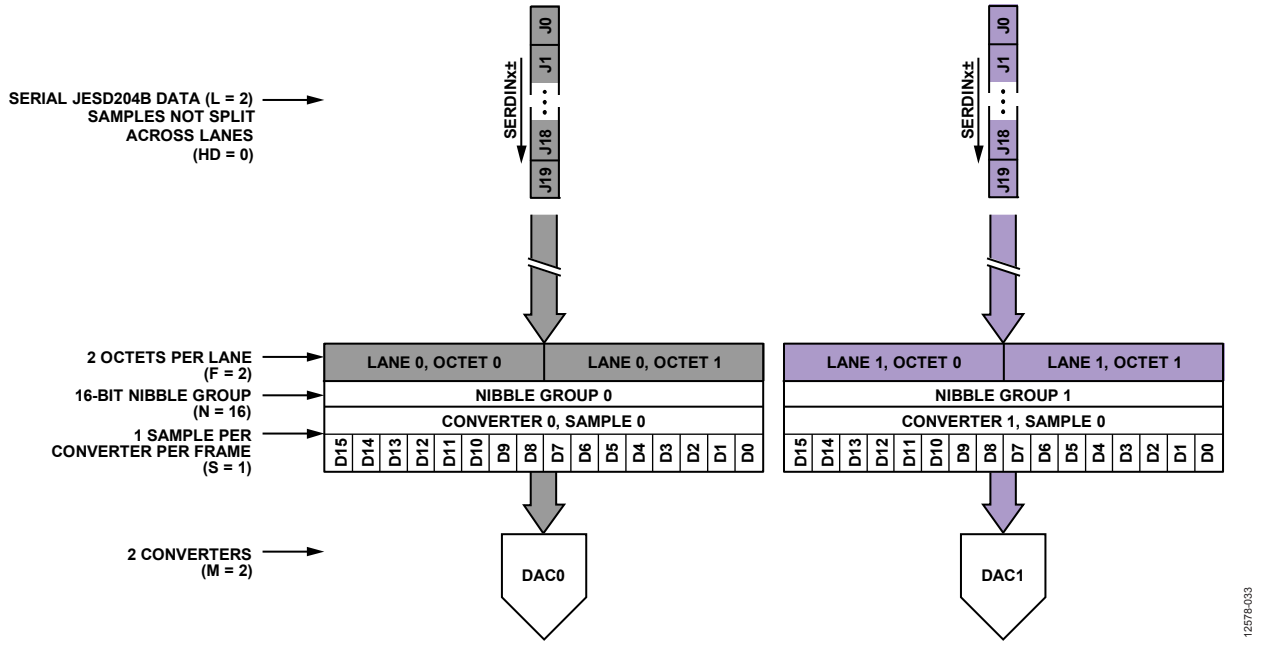


Figure 66. JESD204B Mode 13 Data Deframing

JESD204B TEST MODES

PHY PRBS Testing

The JESD204B receiver on the AD9135/AD9136 includes a PRBS pattern checker on the back end of its physical layer. This functionality enables bit error rate (BER) testing of each physical lane of the JESD204B link. The PHY PRBS pattern checker does not require that the JESD204B link be established. The pattern checker can synchronize with a PRBS7, PRBS15, or PRBS31 data pattern. PRBS pattern verification can be performed on multiple lanes at once. The error counts for failing lanes are reported for one JESD204B lane at a time. The process for performing PRBS testing on the AD9135/AD9136 is as follows:

1. Start sending a PRBS7, PRBS15, or PRBS31 pattern from the JESD204B transmitter.
2. Select and write the appropriate PRBS pattern to Register 0x316[3:2], as shown in Table 54.
3. Enable the PHY test for all lanes being tested by writing to PHY_TEST_EN (Register 0x315). Each bit of Register 0x315 enables the PRBS test for the corresponding lane. For example, writing a 1 to Bit 0 enables the PRBS test for Physical Lane 0.
4. Toggle PHY_TEST_RESET (Register 0x316[0]) from 0 to 1 then back to 0.
5. Set PHY_PRBS_ERROR_THRESHOLD (Register 0x317 to Register 0x319) as desired.
6. Write a 0 and then a 1 to PHY_TEST_START (Register 0x316[1]). The rising edge of PHY_TEST_START starts the test.
7. Wait 500 ms.
8. Stop the test by writing PHY_TEST_START (Register 0x316[1]) = 0.
9. Read the PRBS test results.
   a. Each bit of PHY_PRBS_PASS (Register 0x31D) corresponds to one SERDES lane: 0 is fail, 1 is pass.
   b. The number of PRBS errors seen on each failing lane can be read by writing the lane number to check (0 to 7) in the PHY_SRC_ERR_CNT (Register 0x316[6:4]) and reading the PHY_PRBS_ERR_CNT (Register 0x31A to Register 0x31C). The maximum error count is 2^{24-1}. If all bits of Register 0x31A to Register 0x31C are high, the maximum error count on the selected lane has been exceeded.

Table 54. PHY PRBS Pattern Selection

PHY_PRBS_PAT_SEL Setting, (Register 0x316[3:2])	PRBS Pattern
0b00 (default)	PRBS7
0b01	PRBS15
0b10	PRBS31

Transport Layer Testing

The JESD204B receiver in the AD9135/AD9136 supports the short transport layer (STPL) test as described in the JESD204B standard. This test can be used to verify the data mapping between the JESD204B transmitter and receiver. To perform this test, this function must be implemented in the logic device and enabled there. Before running the test on the receiver side, the link must be established and running without errors (see the Device Setup Guide).

The STPL test ensures that each sample from each converter is mapped appropriately according to the number of converters (M) and the number of samples per converter (S). As specified in the JESD204B standard, the converter manufacturer specifies what test samples are transmitted. Each sample must have a unique value. For example, if M = 2 and S = 2, there are 4 unique samples transmitted repeatedly until the test is stopped. The expected sample must be programmed into the device and the expected sample is compared to the received sample one sample at a time until all have been tested. The process to perform this test on the AD9135/AD9136 is described as follows:

1. Synchronize JESD204B link.
2. Enable the STPL test at the JESD204B transmitter.
3. Select Converter 0 Sample 0 for testing. Write SHORT_TPL_DAC_SEL (Register 0x32C[3:2]) = 0 and SHORT_TPL_SP_SEL (Register 0x32C[5:4]) = 0.
4. Set the expected test sample for Converter 0, Sample 0. Program the expected 11-/16-bit test sample into the SHORT_TPL_REF_SP_x registers (Register 0x32E and Register 0x32D).
5. Enable the STPL test. Write SHORT_TPL_TEST_EN (Register 0x32C[0]) = 1.
6. Toggle the STPL reset. SHORT_TPL_TEST_RESET (Register 0x32C[1]) from 0 to 1 then back to 0.
7. Check for failures. Read SHORT_TPL_FAIL (Register 0x32F[0]): 0 is pass, 1 is fail.
8. Repeat Step 3 to Step 7 for each sample of each converter, $Conv_0Sample_0$ through $Conv_{M-1}Sample_{S-1}$.

Repeated CGS and ILAS Test

As per Section 5.3.3.8.2 of the JESD204B specification, the AD9135/AD9136 can check that a constant stream of /K28.5/ characters is being received, or that CGS followed by a constant stream of ILAS is being received.

To run a repeated CGS test, send a constant stream of /K28.5/ characters to the AD9135/AD9136 SERDES inputs. Next, set up the device and enable the links as described in the Device Setup Guide section. Ensure that the /K28.5/ characters are being received by verifying that the $\overline{\text{SYNCOUTx}\pm}$ has been deasserted and that CGS has passed for all enabled link lanes by reading Register 0x470. Program Register 0x300[2] = 0 to monitor the status of lanes on Link 0, and Register 0x300[2] = 1 to monitor the status of lanes on Link 1 for dual-link mode.

To run the CGS followed by a repeated ILAS sequence test, follow the Device Setup Guide section; however, before performing the last write (enabling the links), enable the ILAS test mode by writing a 1 to Register 0x477[7]. Then, enable the links. When the device recognizes four CGS characters on each lane, it deasserts $\overline{\text{SYNCOUTx±}}$. At this point, the transmitter starts sending a repeated ILAS sequence.

Read Register 0x473 to verify that initial lane synchronization has passed for all enabled link lanes. Program Register 0x300[2] = 0 to monitor the status of lanes on Link 0, and Register 0x300[2] = 1 to monitor the status of lanes on Link 1 for dual-link mode.

JESD204B ERROR MONITORING

Disparity, Not in Table, and Unexpected Control Character Errors

As per Section 7.6 of the JESD204B specification, the AD9135/AD9136 can detect disparity errors, not in table errors, and unexpected control character errors, and can optionally issue a sync request and reinitialize the link when errors occur.

Note that the disparity error counter counts all characters with invalid disparity, regardless of whether they are in the 8-bit/10-bit decoding table. This is a minor deviation from the JESD204B specification, which only counts disparity errors when they are in the 8-bit/10-bit decoding table.

Checking Error Counts

The error count can be checked for disparity errors, not in table errors, and unexpected control character errors. The error counts are on a per lane and per error type basis. Note that the lane select and counter select are programmed into Register 0x46B and the error count is read back from the same address. To check the error count, complete the following steps:

1. Select the desired link lane and error type of the counter to view. Write these to Register 0x46B according to Table 55.
   To select a link lane, first select a link (Register 0x300[2] = 0 to select Link 0 or Register 0x300[2] = 1 to select Link 1 (dual link only)).
   Note that when using Link 1, Link Lane x refers to Logical Lane x + 4.
2. Read the error count from Register 0x46B. Note the maximum error count is equal to the error threshold set in Register 0x47C.

Table 55. Error Counters

Addr.	Bits	Variable	Description
0x46B	[6:4]	LaneSel	LaneSel = x to monitor the error count of Link Lane x. See the notes on link lane in Step 1 of the Checking Error Counts section.
	[1:0]	CntrSel	CntrSel = 0b00 for bad running disparity counter. CntrSel = 0b01 for not in table error counter. CntrSel = 0b10 for unexpected control character counter.

Check for Error Count Over Threshold

In addition to reading the error count per lane and error type as described in the Checking Error Counts section, the user can check a register to see if the error count for a given error type has reached a programmable threshold.

The same error threshold is used for the three error types (disparity, not in table, and unexpected control character). The error counters are on a per error type basis. To use this feature, complete the following steps:

1. Program the desired error count threshold into ERRORTHRES (Register 0x47C).
2. Read back the error status for each error type to see if the error count has reached the error threshold.
   Disparity errors are reported in Register 0x46D.
   Not in table errors are reported in Register 0x46E.
   Unexpected control character errors are reported in Register 0x46F.

Error Counter and IRQ Control

The user can write to Register 0x46D and Register 0x46F to reset or disable the error counts and to reset the IRQ for a given lane. Note that these are the same registers that are used to report error count over threshold (see the Check for Error Count Over Threshold section); therefore, the readback is not the value that was written. For each error type,

1. Select the link lane to access. To select a link lane, first select a link (Register 0x300[2] = 0 to select Link 0, Register 0x300[2] = 1 to select Link 1 (dual link only)). Note that when using Link 1, Link Lane x refers to Logical Lane x + 4.
2. Decide whether to reset the IRQ, disable the error count, and/or reset the error count for the given lane and error type.
3. Write the link lane and desired reset or disable action to Register 0x46D to Register 0x46F according to Table 56.

Table 56. Error Counter and IRQ Control: Disparity (Register 0x46D), Not In Table (Register 0x46E), Unexpected Control Character (Register 0x46F)

Bits	Variable	Description
7	RstIRQ	RstIRQ = 1 to reset IRQ for the lane selected in Bits[2:0].
6	Disable_ErrCnt	Disable_ErrCnt = 1 to disable the error count for the lane selected in Bits[2:0].
5	RstErrCntr	RsteErrCntr = 1 to reset the error count for the lane selected in Bits[2:0].
[2:0]	LaneAddr	LaneAddr = x to monitor the error count of Link Lane x. See the notes on link lane in Step 1 of the Checking Error Counts section.

Monitoring Errors via SYNCOUTx±

When one or more disparity, not in table, or unexpected control character error occurs, the error is reported on the SYNCOUTx± pins as per Section 7.6 of the JESD204B specification. The JESD204B specification states that the SYNCOUTx± signal is asserted for exactly two frame periods when an error occurs. For the AD9135/AD9136, the width of the SYNCOUTx± pulse can be programmed to ½, 1, or 2 PClock cycles. The settings to achieve a SYNCOUTx± pulse of 2 frame clock cycles are given in Table 57.

Table 57. Setting SYNCOUTx± Error Pulse Duration

JESD Mode IDs	PClockFactor (Frames/PClock)	SYNCB_ERR_DUR (Register 0x312[5:4]) Setting[1]
8, 9, 11, 12	4	0 (default)
10, 13	2	1

[1] These register settings assert the SYNCOUTx± signal for 2 frame clock cycle pulse widths.

Disparity, Not in Table, and Unexpected Control Character IRQs

For disparity, not in table, and unexpected control character errors, error count over the threshold events are available as IRQ events. Enable these events by writing to Register 0x47A[7:5]. The IRQ event status can be read at the same address (Register 0x47A[7:5]) after the IRQs are enabled.

See the Error Counter and IRQ Control section for information on resetting the IRQ. See the Interrupt Request Operation section for more information on IRQs.

Errors Requiring Reinitializing

A link reinitialization automatically occurs when four invalid disparity characters are received as per Section 7.1 of the JESD204B specification. When a link reinitialization occurs, the resync request is five frames and nine octets long.

The user can optionally reinitialize the link when the error count for disparity errors, not in table errors, or unexpected control characters reaches a programmable error threshold. The process to enable the reinitialization feature for certain error types is as follows:

1. Set THRESHOLD_MASK_EN (Register 0x477[3]) = 1. Note that when this bit is set, unmasked errors do not saturate at either threshold or maximum value.
2. Enable the sync assertion mask for each type of error by writing to the SYNCASSERTIONMASK register (Register 0x47B[7:5]) according to Table 58.
3. Program the desired error counter threshold into ERRORTHRES (Register 0x47C).
4. For each error type enabled in the SYNCASSERTIONMASK register, if the error counter on any lane reaches the programmed threshold, SYNCOUTx± falls, issuing a sync request. Note that all error counts are reset when a link reinitialization occurs. The IRQ does not reset and must be reset manually.

Table 58. Sync Assertion Mask

Addr.	Bit No.	Bit Name	Description
0x47B	7	BADDIS_S	Set to 1 to assert SYNCOUTx± if the disparity error count reaches the threshold
	6	NIT_S	Set to 1 to assert SYNCOUTx± if the not in table error count reaches the threshold
	5	UCC_S	Set to 1 to assert SYNCOUTx± if the unexpected control character count reaches the threshold

CGS, Frame Sync, Checksum, and ILAS Monitoring

Register 0x470 to Register 0x473 can be monitored to verify that each stage of the JESD204B link establishment has occurred. Program Register 0x300[2] = 0 to monitor the status of the lanes on Link 0, and Register 0x300[2] = 1 to monitor the status of the lanes on Link 1.

Bit x of CODEGRPSYNCFLAG (Register 0x470) is high if Link Lane x received at least four K28.5 characters and passed code group synchronization.

Bit x of FRAMESYNCFLAG (Register 0x471) is high if Link Lane x completed initial frame synchronization.

Bit x of GOODCHKSUMFLG (Register 0x472) is high if the checksum sent over the lane matches the sum of the JESD204B parameters sent over the lane during ILAS for Link Lane x. The parameters can be added either by summing the individual fields in registers or summing the packed register. If Register 0x300[6] = 0 (default), the calculated checksums are the lower eight bits of the sum of the following fields: DID, BID, LID, SCR, L − 1, F − 1, K − 1, M − 1, N − 1, SUBCLASSV, NP − 1, JESDV, S − 1, and HD. If Register 0x300[6] = 1, the calculated checksums are the lower eight bits of the sum of Register 0x400 to Register 0x40C and LID.

Bit x of INITLANESYNCFLG (Register 0x473) is high if Link Lane x passed the initial lane alignment sequence.

CGS, Frame Sync, Checksum, and ILAS IRQs

Fail signals for CGS, frame sync, checksum, and ILAS are available as IRQ events. Enable them by writing to Register 0x47A[3:0]. The IRQ event status can be read at the same address (Register 0x47A[3:0]) after the IRQs are enabled. Write a 1 to Register 0x470[7] to reset the CGS IRQ. Write a 1 to Register 0x471 to reset the frame sync IRQ. Write a 1 to Register 0x472 to reset the checksum IRQ. Write a 1 to Register 0x473 to reset the ILAS IRQ.

See the Interrupt Request Operation section for more information.

Configuration Mismatch IRQ

The AD9135/AD9136 have a configuration mismatch flag that is available as an IRQ event. Use Register 0x47B[3] to enable the mismatch flag (it is enabled by default), and then use Register 0x47B[4] to read back its status and reset the IRQ signal. See the Interrupt Request Operation section for more information.

The configuration mismatch event flag is high when the link configuration settings (in Register 0x450 to Register 0x45D) do not match the JESD204B transmitted settings (Register 0x400 to Register 0x40D). All these registers are paged per link (in Register 0x300). For Mode 11 through Mode 13, the configuration mismatch flag is high because the values for the M and L parameters sent over the link do not match the parameters programmed to Register 0x453 and Register 0x456.

Note that this function is different from the good checksum flags in Register 0x472. The good checksum flags ensure that the transmitted checksum matches a calculated checksum based on the transmitted settings. The configuration mismatch event ensures that the transmitted settings match the configured settings.

HARDWARE CONSIDERATIONS

Power Supply Recommendations

The power supply domains are described in Table 59. The power supplies can be grouped into separate PCB domains as show in Figure 67. All the AD9135/AD9136 supply domains must remain as noise free as possible for the best operation. Power supply noise has a frequency component that affects performance, and is specified in terms of V rms. Figure 68 shows the recommended power supply components.

An LC filter on the output of the power supply is recommended to attenuate the noise, and must be placed as close to the AD9135/AD9136 as possible. An effective filter is shown in Figure 67. This filter scheme reduces high frequency noise components. Each of the power supply pins of the AD9135/AD9136 must also have a 0.1 µF capacitor connected to the ground plane, as shown in Figure 67. Place the capacitor as close to the supply pin as possible. Adjacent power pins can share a bypass capacitor. Connect the ground pins of the AD9135/AD9136 to the ground plane using vias.

Power and Ground Planes

Solid ground planes are recommended to avoid ground loops and to provide a solid, uninterrupted ground reference for the high speed transmission lines that require controlled impedances. Do not use segmented power planes as a reference for controlled impedances unless the entire length of the controlled impedance trace traverses across only a single segmented plane. These and additional guidelines for the topology of high speed transmission lines are described in the JESD204B Serial Interface Inputs (SERDIN0± to SERDIN7±) section.

Table 59. Power Supplies

Supply Domain	Voltage (V)	Circuitry
DVDD12[1]	1.2	Digital core
PVDD12[2]	1.2	DAC PLL
SVDD12[3]	1.2	JESD204B receiver interface
CVDD12[1]	1.2	DAC clocking
IOVDD	1.8	SPI interface
V_{TT}[4]	1.2	V_{TT}
SIOVDD33	3.3	Sync LVDS transmit
AVDD33	3.3	DAC

[1] This supply requires a 1.3 V supply when operating at maximum DAC sample rates. See Table 3 for details.
[2] This supply can be combined with CVDD12 on the same regulator with a separate supply filter network and sufficient bypass capacitors near the pins.
[3] This supply requires a 1.3 V supply when operating at maximum interface rates. See Table 4 for details.
[4] This supply can be connected to SVDD12 and does not need separate circuitry.

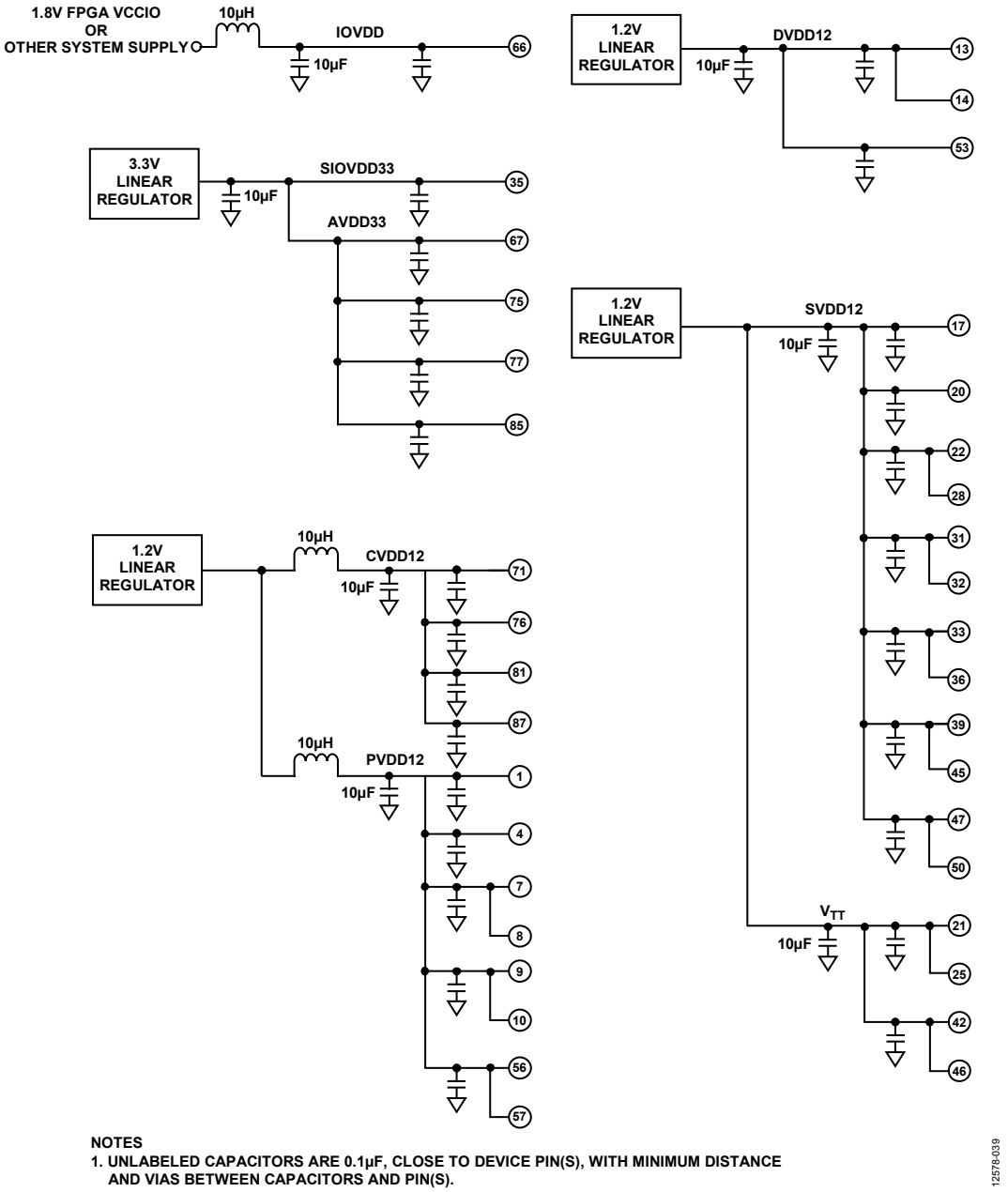


Figure 67. JESD204B Interface PCB Power Domain Recommendation

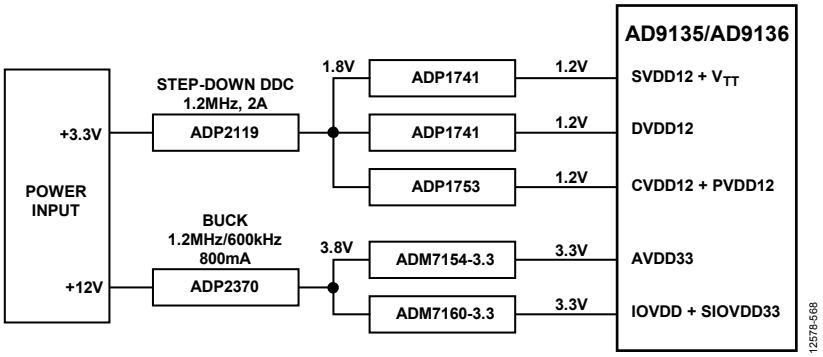


Figure 68. Power Supply Connections

JESD204B Serial Interface Inputs (SERDIN0± to SERDIN7±)

When considering the layout of the JESD204B serial interface transmission lines, there are many factors to consider to maintain optimal link performance. Among these factors are insertion loss, return loss, signal skew, and the topology of the differential traces.

Insertion Loss

The JESD204B specification limits the amount of insertion loss allowed in the transmission channel (see Figure 47). The AD9135/AD9136 equalization circuitry allows significantly more loss in the channel than is required by the JESD204B specification. It is still important that the designer of the PCB minimize the amount of insertion loss by adhering to the following guidelines:

- Keep the differential traces short by placing the AD9135/AD9136 as near to the transmitting logic device as possible and routing the trace as directly as possible between the devices.
- Route the differential pairs on a single plane using a solid ground plane as a reference.
- Use a PCB material with a low dielectric constant (<4) to minimize loss, if possible.

When choosing between the stripline and microstrip techniques, keep in mind the following considerations: stripline has less loss (see Figure 48 and Figure 49) and emits less EMI, but requires the use of vias that can add complexity to the task of controlling the impedance; whereas microstrip is easier to implement if the component placement and density allow routing on the top layer and eases the task of controlling the impedance.

If using the top layer of the PCB is problematic or the advantages of stripline are desirable, follow these recommendations:

- Minimize the number of vias.
- If possible, use blind vias to eliminate via stub effects and use micro vias to minimize via inductance.
- If using standard vias, use the maximum via length to minimize the stub size. For example, on an 8-layer board, use Layer 7 for the stripline pair (see Figure 69).
- For each via pair, place a pair of ground vias adjacent to them to minimize the impedance discontinuity (see Figure 69).

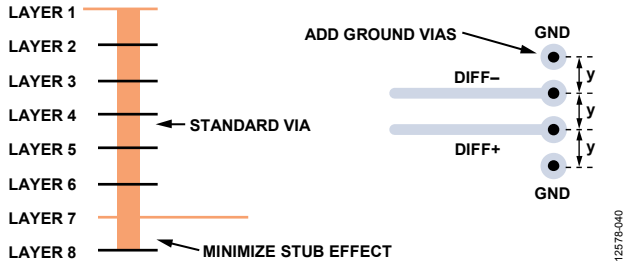


Figure 69. Minimizing Stub Effect and Adding Ground Vias for Differential Stripline Traces

Return Loss

The JESD204B specification limits the amount of return loss allowed in a converter device and a logic device, but does not specify return loss for the channel. However, every effort must be made to maintain a continuous impedance on the transmission line between the transmitting logic device and the AD9135/AD9136. As mentioned in the Insertion Loss section, minimizing the use of vias, or eliminating them altogether, reduces one of the primary sources for impedance mismatches on a transmission line. Maintain a solid reference beneath (for microstrip) or above and below (for stripline) the differential traces to ensure continuity in the impedance of the transmission line. If the stripline technique is used, follow the guidelines listed in the Insertion Loss section to minimize impedance mismatches and stub effects.

Another primary source for impedance mismatch is at either end of the transmission line, where care must be taken to match the impedance of the termination to that of the transmission line. The AD9135/AD9136 handle this internally with a calibrated termination scheme for the receiving end of the line. See the Interface Power-Up and Input Termination section for details on this circuit and the calibration routine.

Signal Skew

There are many sources for signal skew, but the two sources to consider when laying out a PCB are interconnect skew within a single JESD204B link and skew between multiple JESD204B links. In each case, keeping the channel lengths matched to within 15 mm is adequate for operating the JESD204B link at speeds of up to 12.4 Gbps. Managing the interconnect skew within a single link is fairly straightforward. Managing multiple links across multiple devices is more complex. However, follow the 15 mm guideline for length matching.

Topology

Structure the differential SERDINx± pairs to achieve 50 Ω to ground for each half of the pair. Stripline vs. microstrip trade-offs are described in the Insertion Loss section. In either case, it is important to keep these transmission lines separated from potential noise sources such as high speed digital signals and noisy supplies. If using stripline differential traces, route them using a coplanar method, with both traces on the same layer. Although this does not offer more noise immunity than the broadside routing method (traces routed on adjacent layers), it is easier to route and manufacture so that the impedance continuity is maintained. An illustration of broadside vs. coplanar differential routing techniques is shown in Figure 70.

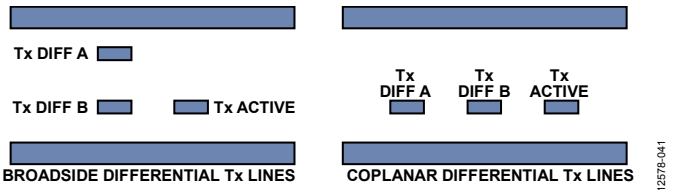


Figure 70. Broadside vs. Coplanar Differential Stripline Routing Techniques

When considering the trace width vs. copper weight and thickness, the speed of the interface must be considered. At multigigabit speeds, the skin effect of the conducting material confines the current flow to the surface. Maximize the surface area of the conductor by making the trace width made wider to reduce the losses. Additionally, loosely couple differential traces to accommodate the wider trace widths. This helps reduce the crosstalk and minimize the impedance mismatch when the traces must separate to accommodate components, vias, connectors, or other routing obstacles. Tightly coupled vs. loosely coupled differential traces are shown in Figure 71.

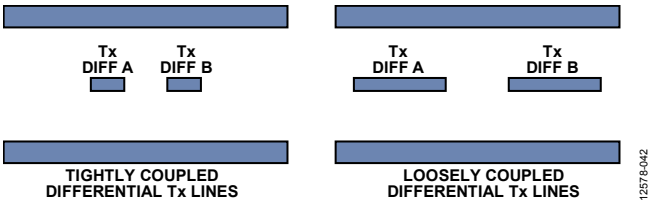


Figure 71. Tightly Coupled vs. Loosely Coupled Differential Traces

AC Coupling Capacitors

The AD9135/AD9136 require that the JESD204B input signals be ac-coupled to the source. These capacitors must be 100 nF and placed as close as possible to the transmitting logic device. To minimize the impedance mismatch at the pads, select the package size of the capacitor so that the pad size on the PCB matches the trace width as closely as possible.

$\overline{\text{SYNCOUTx}}$±, SYSREF±, and CLK± Signals

The $\overline{\text{SYNCOUTx}}$± and SYSREF± signals on the AD9135/AD9136 are low speed LVDS differential signals. Use controlled impedance traces routed with 100 Ω differential impedance and 50 Ω to ground when routing these signals. As with the SERDIN0± to SERDIN7± data pairs, it is important to keep these signals separated from potential noise sources such as high speed digital signals and noisy supplies.

Separate the $\overline{\text{SYNCOUTx}}$± signal from other noisy signals, because noise on the $\overline{\text{SYNCOUTx}}$± may be interpreted as a request for K characters. The $\overline{\text{SYNCOUTx}}$± signal has two modes of operation available for use. Register 0x2A5[0] defaults to 0, which sets the $\overline{\text{SYNCOUTx}}$± swing to normal swing mode. When this bit is set to 1, the $\overline{\text{SYNCOUTx}}$± swing is configured for high swing mode. For more details, see Table 8.

It is important to keep similar trace lengths for the CLK± and SYSREF± signals from the clock source to each of the devices on either end of the JESD204B links (see Figure 72). If using a clock chip that can tightly control the phase of CLK± and SYSREF±, the trace length matching requirements are greatly reduced.

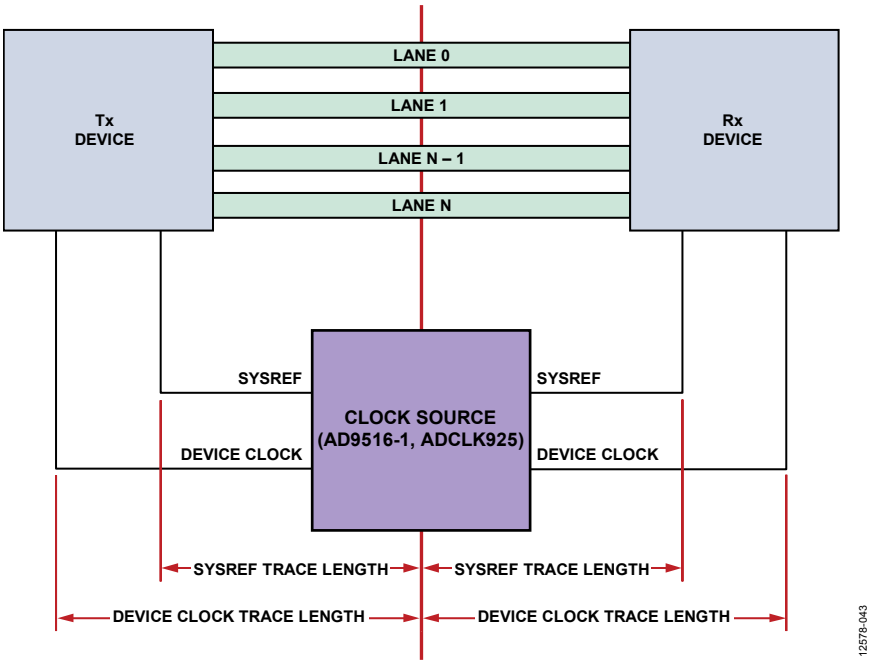


Figure 72. SYSREF Signal and Device Clock Trace Length

DIGITAL DATAPATH

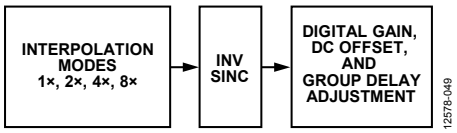


Figure 73. Block Diagram of Digital Datapath

The block diagram in Figure 73 shows the functionality of the digital datapath (all blocks can be bypassed). The digital processing includes three half-band interpolation filters, an inverse sinc filter, and gain, offset, and group delay adjustment blocks.

Note that the pipeline delay changes when digital datapath functions are enabled/disabled. If fixed DAC pipeline latency is desired, do not reconfigure these functions after initial configuration.

DAC PAGING

Digital datapath registers are paged to allow configuration of either DAC independently or both simultaneously. Table 60 shows how to use the DAC paging bits.

Table 60. Paging Modes

DAC_PAGE, Register 0x008[1:0]	DACs Paged
1	DAC0
2	DAC1
3 (default)	DAC0 and DAC1

Several functions are paged by DAC, such as input data format, downstream protection, interpolation, inverse sinc, digital gain, dc offset, group delay, datapath PRBS, and LMFC sync.

DATA FORMAT

BINARY_FORMAT (Register 0x110[7]), paged as described in the DAC Paging section) controls the expected input data format. By default it is 0, which means the input data must be in twos complement. It can also be set to 1, which means the input data is in offset binary. For the AD9136, 0x0000 is negative full scale and 0xFFFF is positive full scale. For the AD9135, 0x0000 is negative full scale and 0xFFE0 is positive full scale.

Though the AD9135 is an 11-bit resolution DAC at the output, the input to the part must still be 16-bits wide for proper 8-bit/10-bit decoding. The AD9135 uses a 16-bit datapath that is truncated to 11 bits before going into the DAC core. Either 11-bit zero-padded data or full 16-bit data can be sent into the device, with the latter having slightly better spectral performance by minimizing quantization error along the datapath.

INTERPOLATION FILTERS

The transmit path contains three half-band interpolation filters, which each provide a 2× increase in output data rate and a low-pass function. The filters can be cascaded to provide a 4× or 8× interpolation ratio. Table 61 shows how to select each available interpolation mode, their usable bandwidths, and their maximum data rates. Note that $f_{DATA} = f_{DAC}$/Interpolation Factor. Interpolation mode is paged as described in the DAC Paging section. Register 0x030[0] is high if an unsupported interpolation mode is selected.

Table 61. Interpolation Modes and Usable Bandwidth

Interpolation Mode	INTERP_MODE, Reg. 0x112[2:0]	Usable Bandwidth	Maximum f_{DATA} (MHz)
1× (bypass)[1]	0x00	0.5 × f_{DATA}	2120[2]
2×	0x01	0.4 × f_{DATA}	1060[2]
4×	0x03	0.4 × f_{DATA}	700
8×	0x04	0.4 × f_{DATA}	350

[1] Mode 8 and Mode 11 can only use 1× interpolation. 2×, 4×, and 8× interpolation are only available in Mode 9, Mode 10, Mode 12, and Mode 13.
[2] The maximum speed for 1× and 2× interpolation is limited by the JESD204B interface. See Table 4 for the appropriate supply levels.

Filter Performance

The interpolation filters interpolate between existing data in such a way that they minimize changes in the incoming data while suppressing the creation of interpolation images. This is shown for each filter in Figure 74.

The usable bandwidth (as shown in Table 61) is defined as the frequency band over which the filters have a pass-band ripple of less than ±0.001 dB and an image rejection of greater than 85 dB.

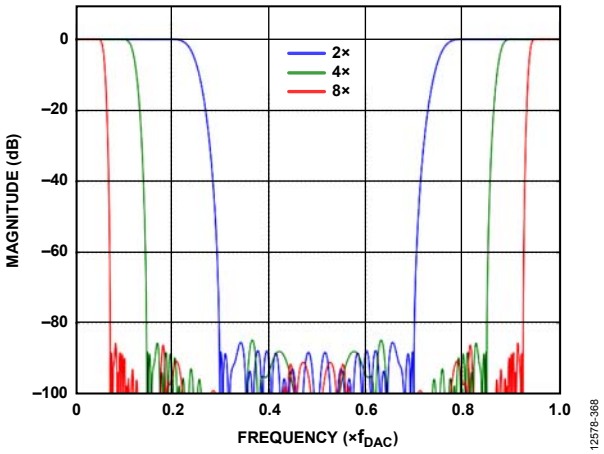


Figure 74. All Band Responses of Interpolation Filters

Filter Performance Beyond Specified Bandwidth

The interpolation filters are specified to 0.4 × f_{DATA} (with pass band). The filters can be used slightly beyond this ratio at the expense of increased pass-band ripple and decreased interpolation image rejection.

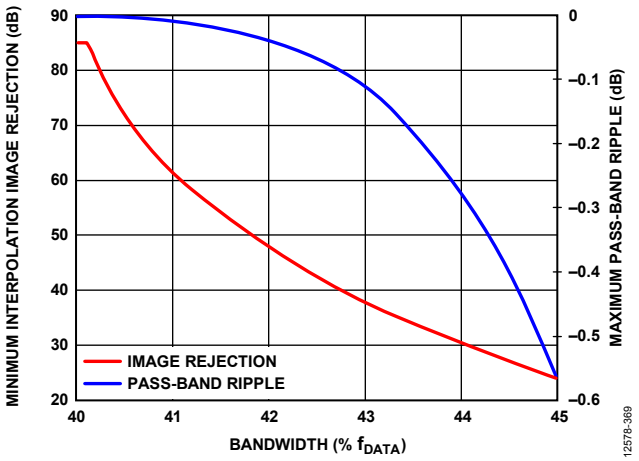


Figure 75. Interpolation Filter Performance Beyond Specified Bandwidth

Figure 75 shows the performance of the interpolation filters beyond 0.4 × f_{DATA}. Note that the ripple increases much slower than the image rejection decreases. This means that if the application can tolerate degraded image rejection from the interpolation filters, more bandwidth can be used.

INVERSE SINC

The AD9135/AD9136 provide a digital inverse sinc filter to compensate the DAC roll-off over frequency. The filter is enabled by setting the INVSINC_ENABLE bit (Register 0x111[7]; paged as described in the DAC Paging section) and is enabled by default.

The inverse sinc ($sinc^{-1}$) filter is a seven-tap FIR filter. Figure 76 shows the frequency response of sin(x)/x roll-off, the inverse sinc filter, and the composite response. The composite response has less than ±0.05 dB pass-band ripple up to a frequency of 0.4 × f_{DAC}. To provide the necessary peaking at the upper end of the pass band, the inverse sinc filter shown has an intrinsic insertion loss of about 3.8 dB; in many cases, this can be partially compensated as described in the Digital Gain section.

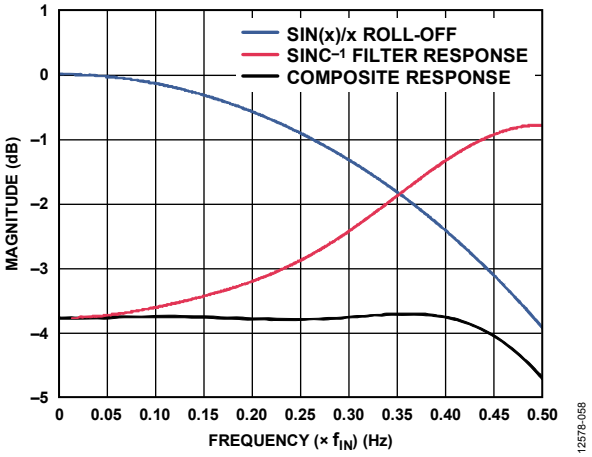


Figure 76. Responses of sin(x)/x Roll-Off, the Sinc⁻¹ Filter, and the Composite of the Two-Input Signal and Protection

DIGITAL GAIN, DC OFFSET, AND GROUP DELAY

Digital gain and dc offset (as described in the Digital Gain section and DC Offset section) allow compensation of imbalances in the I and Q paths due to analog mismatches between DAC I/Q outputs, quadrature modulator I/Q baseband inputs, and DAC/modulator interface I/Q paths. These imbalances can cause the two following issues:

- An unwanted sideband signal to appear at the quadrature modulator output with significant energy. Tuning the quadrature gain adjust values can optimize image rejection in single sideband radios or can optimize the error vector magnitude (EVM) in zero IF (ZIF) architectures.
- The I/Q mismatch can cause LO leakage through a modulator, which can be tuned out using dc offset.

Group delay allows adjustment of the delay through the DAC, which can be used to adjust digital predistortion (DPD) loop delay.

Digital Gain

Digital gain can be used to independently adjust the digital signal magnitude being fed into each DAC. This is useful to balance the gain between I and Q channels of a DAC or to cancel out the insertion loss of the inverse sinc filter. Digital gain must be enabled when using the blanking state machine (see the Downstream Protection section). If digital gain is disabled, TXENx must be tied high.

Digital gain is enabled by setting the DIG_GAIN_ENABLE bit (Register 0x111[5], paged as described in the DAC Paging section). In addition to enabling the function the amount of digital gain (GainCode) desired must be programmed. By default, digital gain is enabled and GainCode is 0xAEA.

$$0 \le Gain \le 4095/2048$$
$$-\infty \text{ dB} \le dBGain \le 6.018 \text{ dB}$$
$$Gain = GainCode \times (1/2048)$$
$$dBGain = 20 \times \log10(Gain)$$
$$GainCode = 2048 \times Gain = 2048 \times 10^{dBGain/20}$$

where *GainCode* is a 12-bit unsigned binary number.

The I/Q digital gain is set as shown in Table 62 and paged as described in the DAC Paging section.

The default GainCode value (0xAEA = 2.7 dB) is appropriate to counteract the insertion loss of the inverse sinc filter without causing digital clipping when using 2× interpolation. This value can be read from of Figure 76 at 0.25 × f_{DAC}, because that is the Nyquist rate when using a 2× interpolation. The recommended GainCode values for 4× and 8× interpolation are 0xBB3 (3.3 dB) and 0xBF8 (3.5 dB), respectively.

Table 62. Digital Gain Registers

Register	Bit Name	Description
0x111[5]	DIG_GAIN_ENABLE	Set to 1 to enable digital gain
0x13C[7:0]	DAC_DIG_GAIN[7:0]	LSB gain code
0x13D[3:0]	DAC_DIG_GAIN[11:8]	MSB gain code

DC Offset

The dc offset feature is used to individually offset the data into the I or Q DAC. This feature can be used to cancel LO leakage.

The offset is programmed as a 16-bit twos complement number in LSBs, plus a 5-bit twos complement number in 16ths of an LSB, as shown in Table 63. DC offset is paged as described in the DAC Paging section.

$$-2^{15} \leq LSBs\ Offset < 2^{15}$$
$$-16 \leq Sixteenths\ Offset \leq 15$$

where
LSBs Offset is the value of Register 0x136 and Register 0x137.
Sixteenths Offset is the value of Register 0x13A.

Table 63. DC Offset Registers

Register	Bit Name	Description
0x135[0]	DC_OFFSET_ON	Set to 1 to enable dc offset
0x136[7:0]	LSB_OFFSET[7:0]	LSB dc offset code
0x137[7:0]	LSB_OFFSET[15:8]	MSB dc offset code
0x13A[4:0]	SIXTEENTH_OFFSET	Sub-LSB dc offset code

Group Delay

Group delay can be used to delay the I or Q channels. This can be useful, for example, for DPD loop delay adjustment.

$$-4 \leq DAC\ Clock\ Cycles \leq 3.5$$
$$Group\ Delay = (DAC\ Clock\ Cycles \times 2) + 8$$

where *Group Delay* is a 4-bit twos complement number.

Write the GroupDelay to the GROUP_DLY register (Register 0x014[3:0]). This feature is paged as described in the DAC Paging section.

DOWNSTREAM PROTECTION

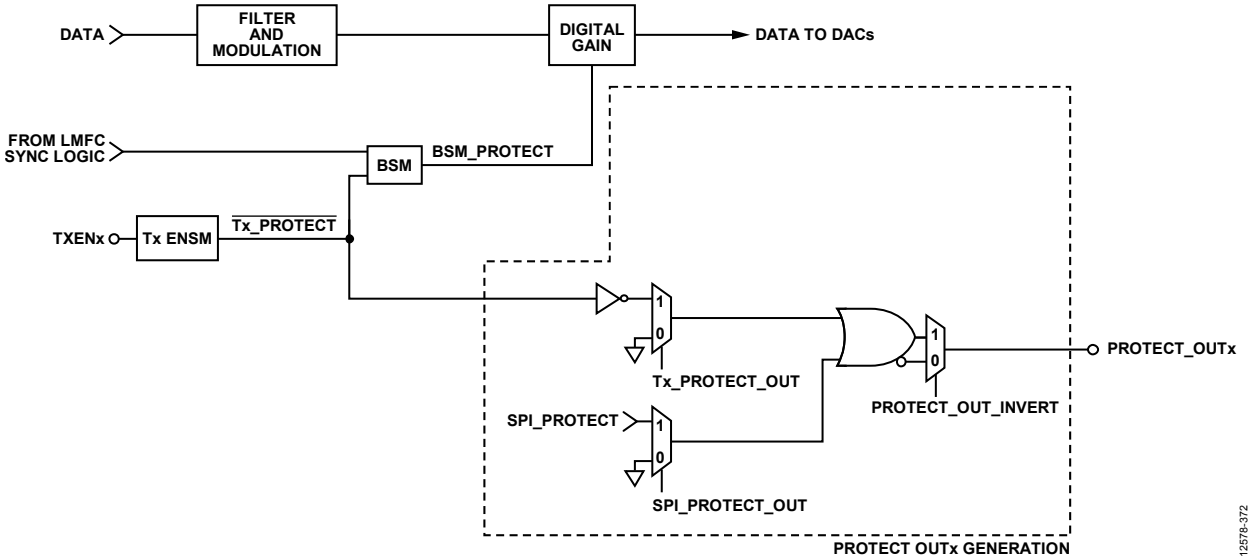


Figure 77. Downstream Protection Block Diagram

The AD9135/AD9136 have several blocks designed to protect the power amplifier (PA) of the system, as well as other downstream blocks. The AD9135/AD9136 consist of a blanking state machine (BSM) and a transmit enable state machine (Tx ENSM).

The Tx ENSM is a block that controls delay between TXENx and the $\overline{\text{Tx\_PROTECT}}$ signal. The $\overline{\text{Tx\_PROTECT}}$ signal is used as an input to the BSM and its inverse can optionally be routed externally. Optionally, the Tx ENSM can also power down its associated DAC.

The BSM gently ramps data entering the DAC and flushes the datapath. The BSM is activated by the $\overline{\text{Tx\_PROTECT}}$ signal or automatically by the LMFC sync logic during a rotation. For proper function, digital gain must be enabled; tie TXENx high if disabling digital gain.

Finally, some simple logic takes the outputs from each of those blocks and uses them to generate a desired PROTECT_OUTx signal on an external pin. This signal can be used to enable/disable downstream components, such as a PA.

Transmit Enable State Machine

The Tx ENSM is a simple block that controls the delay between the TXENx signal and the $\overline{\text{TX\_PROTECT}}$ signal. This signal is used as an input to the BSM and its inverse can be routed to an external pin (PROTECT_OUTx) to turn downstream components on or off as desired.

The TXENx signal can be used to power down the associated DAC. If DAC0_MASK (Register 0x012[0]) = 1, a falling edge of TXENx causes DAC0 to power down. If DAC1_MASK (Register 0x012[1]) = 1, a falling edge of TXENx causes DAC1 to power down.

On a rising edge of TXENx, without DAC0_MASK and DAC1_MASK enabled, the output is valid after the BSM settles (see the Blanking State Machine (BSM) section). If the masks are enabled, an additional delay is imposed; the output is not valid until the BSM settles and the DACs fully power on (nominally an additional ~35 µs).

The Tx ENSM is configured as shown in Table 64 and is paged as described in the DAC Paging section.

Table 64. Tx ENSM Registers

Addr.	Bit No.	Bit Name	Description
0x11F	[7:6]	FALL_COUNTERS	Number of fall counters to use (1 to 2).
	[5:4]	RISE_COUNTERS	Number of rise counters to use (0 to 2).
0x121	[7:0]	RISE_COUNT_0	Delay TX_PROTECT rise from TXENx rising edge by 32 × RISE_COUNT_0 DAC clock cycles.
0x122	[7:0]	RISE_COUNT_1	Delay TX_PROTECT rise from TXENx rising edge by 32 × RISE_COUNT_1 DAC clock cycles.
0x123	[7:0]	FALL_COUNT_0	Delay TX_PROTECT rise from TXENx rising edge by 32 × FALL_COUNT_0 DAC clock cycles. Must be at least 0x12.
0x124	[7:0]	FALL_COUNT_1	Delay TX_PROTECT rise from TXENx rising edge by 32 × FALL_COUNT_1 DAC clock cycles.

Blanking State Machine (BSM)

The BSM gently ramps data entering the DAC and flushes the datapath.

On a falling edge of $\overline{\text{TX\_PROTECT}}$ (the TXENx signal delayed by the Tx ENSM), the datapath holds the latest data value and the digital gain gently ramps from its set value to 0. At the same time, the datapath is flushed with zeros.

On a rising edge of $\overline{\text{TX\_PROTECT}}$, the TXENx signal is delayed by the Tx ENSM; data is allowed to flow through the datapath again and the digital gain gently ramps the data from 0 up to the set digital gain.

Both of these functions are also triggered automatically by the LMFC sync logic during a rotation to prevent glitching on the output.

Ramping

For proper ramping, digital gain must be enabled; tie TXENx high if disabling digital gain.

The step size to use when ramping gain to 0 or its assigned value can be controlled via the GAIN_RAMP_DOWN_STEP[11:0] registers (Register 0x142 and Register 0x143) and the GAIN_RAMP_UP_STEP[11:0] registers (Register 0x140 and Register 0x141). These registers are paged as described in the DAC Paging section.

The current BSM state can be read back as shown in Table 65.

Table 65. Blanking State Machine Ramping Readbacks

Register	Value	Description
0x147[7:6]	0b00	Data is being held at midscale.
	0b01	Ramping gain to 0. Data ramping to midscale.
	0b10	Ramping gain to assigned value. Data ramping to normal amplitude.
	0b11	Data at normal amplitude.

Blanking State Machine IRQ

Blanking completion is available as an IRQ event.

Use Register 0x021[5] to enable blanking completion for DAC0 and then use Register 0x025[5] to read back its status and reset the IRQ signal.

Use Register 0x022[5] to enable blanking completion for DAC1 and then use Register 0x026[5] to read back its status and reset the IRQ signal.

See the Interrupt Request Operation section for more information.

PROTECT_OUTx Generation

Register 0x013 controls which signals are ORed into the external PROTECT_OUTx signal. Register 0x11F[2] can be used to invert the PROTECT_OUTx signal. By default, PROTECT_OUTx is high when the output is valid. Register 0x013 and Register 0x11F are paged as described in the DAC Paging section.

Table 66. PROTECT_OUTx Registers

Reg.	Bit No.	Bit Name	Description
0x013	5	TX_PROTECT_OUT	1: Tx ENSM triggers PROTECT_OUT
	3	SPI_PROTECT_OUT	1: SPI_PROTECT triggers PROTECT_OUT
	2	SPI_PROTECT	Sets SPI_PROTECT
0x11F	2	PROTECT_OUT_INVERT	Inverts PROTECT_OUTx

DATAPATH PRBS

The datapath PRBS can be used to verify that the AD9135/AD9136 datapath is receiving and correctly decoding data. The datapath PRBS verifies that the JESD204B parameters of the transmitter and receiver match, that the lanes of the receiver are mapped appropriately, that the lanes have been appropriately inverted, if necessary, and in general that the start-up routine has been implemented correctly. The datapath PRBS test is designed to support input data rates of up to 1060 MHz.

The datapath PRBS is paged as described in the DAC Paging section. To run the datapath PRBS test, complete the following steps:

1. Set up the device in the desired operating mode. See the Device Setup Guide section for details on setting up the device.
2. Send the PRBS7 or PRBS15 data.
3. Write Register 0x14B[2] = 0 for PRBS7 or 1 for PRBS15.
4. Write Register 0x14B[1:0] = 0b11 to enable and reset the PRBS test.
5. Write Register 0x14B[1:0] = 0b01 to enable the PRBS test and release reset.
6. Wait 500 ms.
7. Check the status by checking the IRQ for DAC0 and DAC1 PRBS as described in the Datapath PRBS IRQ section.
8. If there are failures, set Register 0x008 = 0x01 to view the status of DAC0. Set Register 0x008 = 0x02 to view the status of DAC1.
9. Read Register 0x14B[6]. Bit 6 is 0 if the selected DAC has any errors. This must match the IRQ.
10. Read Register 0x14C to read the error count of the selected DAC.

Note that the PRBS processes 32 bits at a time, and compares the 32 new bits to the previous set of 32 bits. It detects (and reports) only 1 error in every group of 32 bits; therefore, the error count partly depends on when the errors are seen. For example,

- Bits: 32 good, 31 good, 1 bad; 32 good (2 errors)
- Bits: 32 good, 22 good, 10 bad; 32 good (2 errors)
- Bits: 32 good, 31 good, 1 bad; 31 good, 1 bad; 32 good (3 errors)

Datapath PRBS IRQ

The PRBS fail signals for each DAC are available as IRQ events. Use Register 0x020, Bit 2 and Bit 0, to enable the fail signals, and then use Register 0x024, Bit 2 and Bit 0, to read back their statuses and reset the IRQ signals. See the Interrupt Request Operation section for more information.

DC TEST MODE

As a convenience, the AD9135/AD9136 provide a dc test mode, which is enabled by setting Register 0x520[1] to 1 and clearing Register 0x146[0] to 0. When this mode is enabled, the datapath is given 0 (midscale) for its data. Register 0x146[0] must be set to 1 for all other modes of operation.

In conjunction with dc offset, this test mode can provide the desired dc data to the DACs.

INTERRUPT REQUEST OPERATION

The AD9135/AD9136 provide an interrupt request output signal on Pin 60 ($\overline{IRQ}$) that can be used to notify an external host processor of significant device events. On assertion of the interrupt, query the device to determine the precise event that occurred. The $\overline{IRQ}$ pin is an open-drain, active low output. Pull the $\overline{IRQ}$ pin high external to the device. This pin can be tied to the interrupt pins of other devices with open-drain outputs to wire; OR these pins together.

Figure 78 shows a simplified block diagram of how the IRQ blocks works. If IRQ_EN is low, the INTERRUPT_SOURCE signal is set to 0. If IRQ_EN is high, any rising edge of an event causes the INTERRUPT_SOURCE signal to be set high. If any INTERRUPT_SOURCE signal is high, the $\overline{IRQ}$ pin is pulled low. INTERRUPT_SOURCE can be reset to 0 by either an IRQ_RESET signal or a DEVICE_RESET.

Depending on the STATUS_MODE signal, the EVENT_STATUS bit reads back event or INTERRUPT_SOURCE. The AD9135/AD9136 have several IRQ register blocks, which can monitor up to 75 events (depending on device configuration). Certain details vary by IRQ register block as described in Table 67. Table 68 shows which registers the IRQ_EN, IRQ_RESET, and STATUS_MODE signals in Figure 78 originate from, as well as the address where EVENT_STATUS is read back.

Table 67. IRQ Register Block Details

Register Block	Event Reported	EVENT_STATUS
0x01F to 0x026	Per chip	INTERRUPT_SOURCE if IRQ is enabled, if not, it is EVENT
0x46D to 0x46F; 0x470 to 0x473; 0x47A	Per link and lane	INTERRUPT_SOURCE if IRQ is enabled, if not, 0
0x47B[4]	Per link	INTERRUPT_SOURCE if IRQ is enabled, if not, 0

INTERRUPT SERVICE ROUTINE

Interrupt request management begins by selecting the set of event flags that require host intervention or monitoring. Enable the events that require host action so that the host is notified when they occur. For events requiring host intervention upon $\overline{IRQ}$ activation, run the following routine to clear an interrupt request:

1. Read the status of the event flag bits that are being monitored.
2. Disable the interrupt by writing 0 to IRQ_EN.
3. Read the event source. For Register 0x01F to Register 0x026, EVENT_STATUS has a live readback. For other events, see their registers.
4. Perform any actions required to clear the cause of the EVENT. In many cases, no specific actions may be required.
5. Verify that the event source is functioning as expected.
6. Clear the interrupt by writing 1 to IRQ_RESET.
7. Enable the interrupt by writing 1 to IRQ_EN.

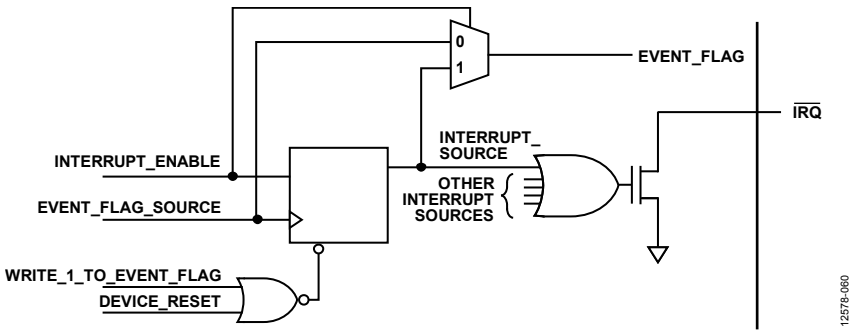


Figure 78. Simplified Schematic of $\overline{IRQ}$ Circuitry

Table 68. IRQ Register Block Address of IRQ Signal Details

	Address of IRQ Signals[1]			
Register Block	**IRQ_EN**	**IRQ_RESET**	**STATUS_MODE**	**EVENT_STATUS**
0x01F to 0x026	0x01F to 0x022; R/W per chip	0x023 to 0x026; W per chip	STATUS_MODE = IRQ_EN	0x023 to 0x026; R per chip
0x46D to 0x46F	0x47A; W per link	0x46D to 0x46F; W per link and lane	N/A, STATUS_MODE = 1	0x47A; R per link
0x470 to 0x473	0x47A; W per link	0x470 to 0x473; W per link	N/A, STATUS_MODE = 1	0x47A; R per link
0x47B[4]	0x47B[3]; R/W per link; 1 by default	0x47B[4]; W per link	N/A, STATUS_MODE = 1	0x47B[4]; R per link

[1] N/A means not applicable.

DAC INPUT CLOCK CONFIGURATIONS

The AD9135/AD9136 DAC sample clock (DACCLK) can be sourced directly through CLK± (Pin 2 and Pin 3) or by clock multiplication through the CLK± differential input. Clock multiplication employs the on-chip PLL that accepts a reference clock operating at a submultiple of the desired DACCLK rate. The PLL then multiplies the reference clock up to the desired DACCLK frequency, which is used to generate all the internal clocks required by the DAC. The clock multiplier provides a high quality clock that meets the performance requirements of most applications. Using the on-chip clock multiplier removes the burden of generating and distributing the high speed DACCLK.

The second mode bypasses the clock multiplier circuitry and allows DACCLK to be sourced directly to the DAC core. This mode allows the user to source a very high quality clock directly to the DAC core.

DRIVING THE CLK± INPUTS

The CLK± differential input circuitry is shown in Figure 79 as a simplified circuit diagram of the input. The on-chip clock receiver has a differential input impedance of 10 kΩ. It is self biased to a common-mode voltage of about 600 mV. The inputs can be driven by differential PECL or LVDS drivers with ac-coupling between the clock source and the receiver.

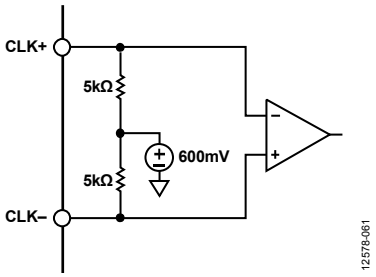


Figure 79. Clock Receiver Input Simplified Equivalent Circuit

The minimum input drive level to the differential clock input is 400 mV p-p differential. The optimal performance is achieved when the clock input signal is between 800 mV p-p differential and 1000 mV p-p differential. Whether using the on-chip clock multiplier or sourcing the DACCLK directly (the CLK± pins are used in both cases), the input clock signal to the device must have low jitter and fast edge rates to optimize the DAC noise performance. Direct clocking with a low noise clock produces the lowest noise spectral density at the DAC outputs.

The clocks and clock receiver are powered down by default. The clocks must be enabled by writing to Register 0x080. To enable all clocks on the device, write Register 0x080 = 0x00. Register 0x080, Bit 7 powers up the clocks for DAC0. Bit 6 powers up the clocks for DAC1. Bit 5 powers up the digital clocks; Bit 4 powers up the SERDES clocks; and Bit 3 powers up the clock receiver.

DAC PLL FIXED REGISTER WRITES

To optimize the PLL across all operating conditions, the register writes in Table 69 are recommended. These writes properly set up the DAC PLL, including the loop filter and the charge pump.

Table 69. DAC PLL Fixed Register Writes

Register Address	Register Value	Description
0x087	0x62	Optimal DAC PLL loop filter settings
0x088	0xC9	Optimal DAC PLL loop filter settings
0x089	0x0E	Optimal DAC PLL loop filter settings
0x08A	0x12	Optimal DAC PLL charge pump settings
0x08D	0x7B	Optimal DAC LDO settings for DAC PLL
0x1B0	0x00	Power DAC PLL blocks when power machine disabled
0x1B9	0x24	Optimal DAC PLL charge pump settings
0x1BC	0x0D	Optimal DAC PLL VCO control settings
0x1BE	0x02	Optimal DAC PLL VCO power control settings
0x1BF	0x8E	Optimal DAC PLL VCO calibration settings
0x1C0	0x2A	Optimal DAC PLL lock counter length setting
0x1C1	0x2A	Optimal DAC PLL charge pump setting
0x1C4	0x7E	Optimal DAC PLL varactor settings

CLOCK MULTIPLICATION

The on-chip PLL clock multiplier circuit can be used to generate the DAC sample rate clock from a lower frequency reference clock. The PLL is integrated on-chip, including the VCO and the loop filter. The VCO operates over the frequency range of 6 GHz to 12 GHz.

The PLL configuration parameters must be programmed before the PLL is enabled. Step by step instructions on how to program the PLL can be found in the Starting the PLL section. The functional block diagram of the clock multiplier is shown in Figure 82.

The clock multiplication circuit generates the DAC sampling clock from the REFCLK input, which is fed in on the CLK± differential pins (Pin 2 and Pin 3). The frequency of the REFCLK input is referred to as f_{REF}.

The REFCLK input is divided by the variable RefDivFactor. Select the RefDivFactor variable to ensure that the frequency into the phase frequency detector (PFD) block is between 35 MHz and 80 MHz. The valid values for RefDivFactor are 1, 2, 4, 8, 16, or 32. Each RefDivFactor value maps to the appropriate REF_DIV_MODE register control according to Table 70. The REF_DIV_MODE register is programmed through Register 0x08C[2:0].

Table 70. Mapping of RefDivFactor to REF_DIV_MODE

DAC Reference Frequency Range (MHz)	Divide by (RefDivFactor)	REF_DIV_MODE, Reg. 0x08C[2:0]
35 to 80	1	0
80 to 160	2	1
160 to 320	4	2
320 to 640	8	3
640 to 1000	16	4

The range of f_{REF} is 35 MHz to 1 GHz, and the output frequency of the PLL is 420 MHz to 2.8 GHz. Use the following equations to determine the RefDivFactor:

$$35\text{ MHz} < \frac{f_{REF}}{RefDivFactor} < 80\text{ MHz} \quad (1)$$

where:
f_{REF} is the reference frequency on the CLK± input pins.
RefDivFactor is the reference divider division ratio.

The BCount value is the divide ratio of the loop divider. It is set to divide the f_{DAC} to frequency match the f_{REF}/RefDivFactor. Select BCount so that the following equation is true:

$$\frac{f_{DACCLK}}{2 \times BCount} = \frac{f_{REF}}{RefDivFactor} \quad (2)$$

where:
f_{DAC} is the DAC sample clock.
BCount is the feedback loop divider ratio.

The BCount value is programmed with Bits[7:0] of Register 0x085. It is programmable from 6 to 127.

The PFD compares f_{REF}/RefDivRate to f_{DAC}/(2 × BCount) and pulses the charge pump up or down to control the frequency of the VCO. A low noise VCO is tunable over an octave with an oscillation range of 6 GHz to 12 GHz.

The clock multiplication circuit operates such that the VCO outputs a frequency, f_{VCO}.

$$f_{VCO} = f_{DAC} \times LODivFactor \quad (3)$$

and from Equation 2, the DAC sample clock frequency, f_{DAC}, is equal to

$$f_{DACCLK} = 2 \times BCount \times \frac{f_{REF}}{RefDivFactor} \quad (4)$$

The LODivFactor is chosen to keep f_{VCO} in the operating range between 6 GHz and 12 GHz. The valid values for LODivFactor are 4, 8, and 16. Each LODivFactor maps to a LO_DIV_MODE value. The LO_DIV_MODE (Register 0x08B[1:0]) is programmed as described in Table 71.

Table 71. DAC VCO Divider Selection

DAC Frequency Range (MHz)	Divide by (LODivFactor)	LO_DIV_MODE, Register 0x08B[1:0]
>1500	4	1
750 to 1500	8	2
420 to 750	16	3

Table 72 lists some common frequency examples for the RefDivFactor, LODivFactor, and BCount values that are needed to configure the PLL properly.

Table 72. Common Frequency Examples

Frequency (MHz)	f_{DAC} (MHz)	f_{VCO} (MHz)	RefDiv-Factor	LODiv-Factor	BCount
368.64	1474.56	11796.48	8	8	16
184.32	1474.56	11796.48	4	8	16
307.2	1228.88	9831.04	8	8	16
122.88	983.04	7864.35	2	8	8
61.44	983.04	7864.35	1	8	8
491.52	1966.08	7864.35	8	4	16
245.76	1966,08	7864.35	4	4	16

Loop Filter

The RF PLL filter is fully integrated on-chip and is a standard passive third-order filter with five 4-bit programmable components (see Figure 80). The C1, C2, C3, R1, and R3 filter components are programmed with Register 0x087 through Register 0x089, as described in the DAC PLL Fixed Register Writes section.

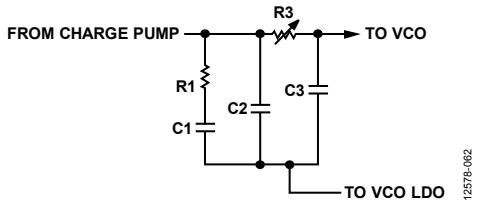


Figure 80. Loop Filter

Charge Pump

The charge pump current is 6-bit programmable and varies from 0.1 mA to 6.4 mA in 0.1 mA steps. The charge pump current is programmed into Register 0x08A for the DAC PLL as shown in the DAC PLL Fixed Register Writes section. The charge pump calibration must be run one time during chip initialization to reduce reference spurs. This calibration is on by default.

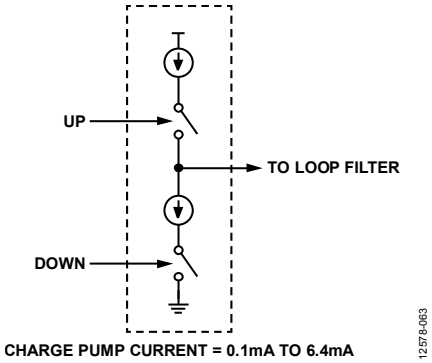


Figure 81. Charge Pump

Charge pump calibration is run during the first power-up of the PLL, and the coefficient of the calibration is held for all subsequent starts. The PLL is enabled by writing 0x10 into Register 0x083, but the configuration registers must be programmed before the PLL is enabled. The calibration tries to match the up and down current, which minimizes the spurs at the reference frequency that appears at the DAC output. The charge pump calibration takes 64 reference clock cycles. Bit 5 in Register 0x084 notifies the user that the charge pump calibration is completed and is valid.

Temperature Tracking

When properly configured, the device automatically selects one of the 512 VCO bands. The PLL settings selected by the device ensure that the PLL remains locked over the full −40°C to +85°C operating temperature range of the device without further adjustment. The PLL remains locked over the full temperature range, even if the temperature during initialization is at one of the temperature extremes. Confirm the PLL lock bit to ensure that the calibration completed properly. The PLL lock bit is Bit 1 of Register 0x084.

To properly configure temperature tracking, follow the settings in the DAC PLL Fixed Register Writes section and the f_{VCO} dependent SPI writes shown in Table 73.

Table 73. VCO Control Lookup Table Reference

VCO Frequency Range (GHz)	Register 0x1B5 Setting	Register 0x1BB Setting	Register 0x1C5 Setting
$f_{VCO} < 6.3$	0x08	0x03	0x07
$6.3 \le f_{VCO} < 7.25$	0x09	0x03	0x06
$f_{VCO} \ge 7.25$	0x09	0x13	0x06

STARTING THE PLL

The programming sequence for the DAC PLL is as follows:

1. Program the registers in the DAC PLL Fixed Register Writes section.
2. Determine the VCO frequency based on the DAC frequency requirements.
3. Determine the VCO divider ratio to achieve the desired DAC frequency. Program the VCO divider ratio in Register 0x08B[1:0].
4. Determine the BCount ratio to achieve the desired PLL reference frequency (35 MHz to 80 MHz). Program the BCount ratio in Register 0x085[7:0].
5. Determine the reference divider ratio to achieve the desired PLL reference frequency. Program the reference divider ratio in Register 0x08C[2:0].
6. Based on the f_{VCO} found in Step 2, write the temperature tracking registers as shown in Table 73.
7. Enable the DAC PLL synthesizer by setting Register 0x083[4] to 1.

Register 0x084[5] notifies the user that the DAC PLL calibration is completed and is valid.

Register 0x084[1] notifies the user that the PLL has locked.

Register 0x084[7] and Register 0x084[6] notify the user that the DAC PLL has reached the upper or lower edge of its operating band, respectively. If either of these bits are high, recalibrate the DAC PLL by setting Register 0x083[7] to 0 and then 1.

DAC PLL IRQ

The DAC PLL lock and lost signals are available as IRQ events. Use Register 0x01F[5:4] to enable these signals, and then use Register 0x023[5:4] to read back their statuses and reset the IRQ signals. See the Interrupt Request Operation section for more information.

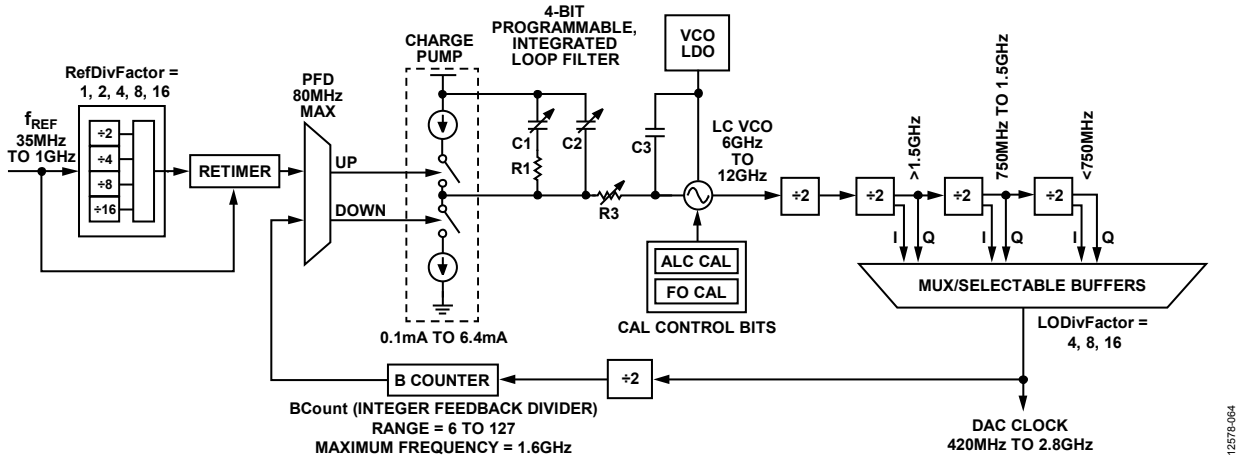


Figure 82. Device Clock PLL Block Diagram

ANALOG OUTPUTS

TRANSMIT DAC OPERATION

Figure 83 shows a simplified block diagram of the transmit path DACs. The DAC core consists of a current source array, a switch core, digital control logic, and full-scale output current control. The DAC full-scale output current (I_{OUTFS}) is nominally 20.48 mA. The output currents from the OUTx± pins are complementary, meaning that the sum of the two currents always equals the full-scale current of the DAC. The digital input code to the DAC determines the effective differential current delivered to the load.

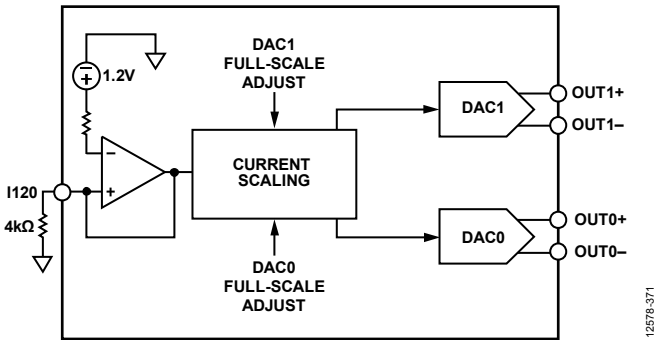


Figure 83. Simplified Block Diagram of DAC Core

The DAC has a 1.2 V band gap reference. A 4 kΩ external resistor, R_{SET}, must be connected from the I120 pin to the ground plane. This resistor, along with the reference control amplifier, sets up the correct internal bias currents for the DAC. Because the full-scale current is inversely proportional to this resistor, the tolerance of R_{SET} is reflected in the full-scale output amplitude.

DACFSC_x (where x is either 0 or 1, corresponding to DAC0 or DAC1) is a 10-bit twos complement value that controls the full-scale current of each of the four DAC outputs. These values are stored in Register 0x040 to Register 0x041 and Register 0x044 to Register 0x045 as shown in Table 74.

The typical full-scale current for each DAC is given by

$$I_{OUTFS} = 20.45 + (DACFSC\_x \times 6.55\ \text{mA})/2^{(10-1)}$$

For nominal values of V_{REF} (1.2 V), R_{SET} (4 kΩ), and DACFSC_x (0, which is midscale in twos complement), the full-scale current of the DAC is nominally 20.48 mA. The DAC full-scale current can be adjusted from 13.9 mA to 27.0 mA, by programming the appropriate DACFSC_x values in Register 0x040, Register 0x041, and Register 0x044, and Register 0x045. Analog output full-scale current vs. gain DAC code is shown in Figure 84.

Table 74. DAC Full-Scale Current Registers

Address	Value	Description
0x040[1:0]	DACFSC_0[9:8]	DAC0 MSB gain code
0x041[7:0]	DACFSC_0[7:0]	DAC0 LSB gain code
0x044[1:0]	DACFSC_1[9:8]	DAC1 MSB gain code
0x045[7:0]	DACFSC_1[7:0]	DAC1 LSB gain code

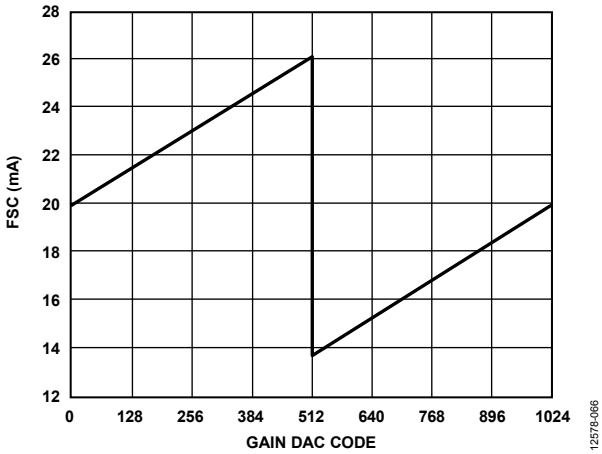


Figure 84. DAC Full-Scale Current (I_{OUTFS}) vs. Gain DAC Code

Transmit DAC Transfer Function

The output currents from the OUTx+ and OUTx− pins are complementary, meaning that the sum of the positive and negative currents always equals the full-scale current of the DAC. The digital input code to the DAC determines the effective differential current delivered to the load. OUTx± provides the maximum output current when all bits are high for binary data. The output currents vs. DACCODE for the DAC outputs using binary format are expressed as

$$I_{OUTP} = \frac{DACCODE_{BIN}}{2^N - 1} \times I_{OUTFS} \quad (5)$$

$$I_{OUTN} = I_{OUTFS} - I_{OUTP} \quad (6)$$

where $DACCODE_{BIN}$ is the 11-/16-bit input to the DAC in unsigned binary. $DACCODE_{BIN}$ has a range of 0 to $2^N - 1$.

If the data format is twos complement, the output currents are expressed as

$$I_{OUTP} = \frac{DACCODE_{TWOS} + 2^{N-1}}{2^N - 1} \times I_{OUTFS} \quad (7)$$

$$I_{OUTN} = I_{OUTFS} - I_{OUTP} \quad (8)$$

where $DACCODE_{TWOS}$ is the 11-/16-bit input to the DAC in twos complement. $DACCODE_{TWOS}$ has a range of -2^{N-1} to $2^{N-1} - 1$.

Powering Down Unused DACs

Power down any unused DAC outputs to avoid burning excess power. The DAC power downs are located in Register 0x011. Register 0x011, Bit 6 corresponds to DAC0, and Bit 4 to DAC1. Write a 1 to each bit to power down the appropriate DACs.

Register 0x011, Bit 7 and Bit 2, must stay low to enable the band gap and DAC master bias, respectively.

Self Calibration

The AD9135/AD9136 have a self calibration feature that improves the DAC dc and ac linearity in zero or low IF applications. The performance improvement includes the INL/DNL, second and fourth harmonic distortions (HD2 and HD4), and second-order intermodulation distortion (IMD2) of the device. Figure 85 and Figure 86 show the typical DAC INL and DNL before and after the calibration. Figure 87 and Figure 88 show the calibration effect on the HD2, HD4, and IMD2 performance. The improvement from calibration decreases with the DAC output frequency. For improvement in HD2 and HD4, it is recommended to run the calibration routine when the desired output frequency is below 100 MHz. For improvement in IMD2, it is recommended to run the routine when the desired output frequency is below 200 MHz. A single run of the routine is sufficient to obtain the desired performance for both ac and dc performance.

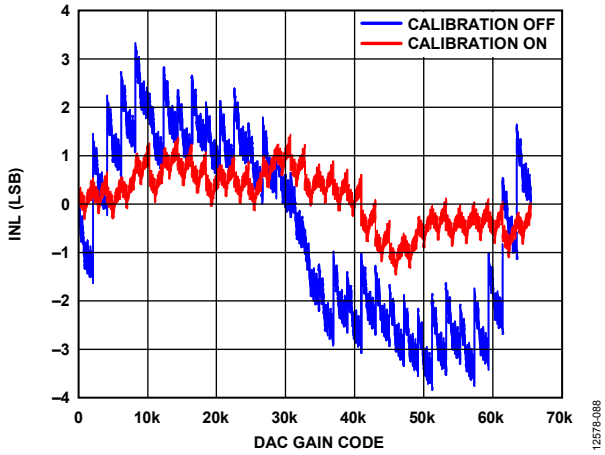


Figure 85. Pre-Calibration and Post-Calibration, INL

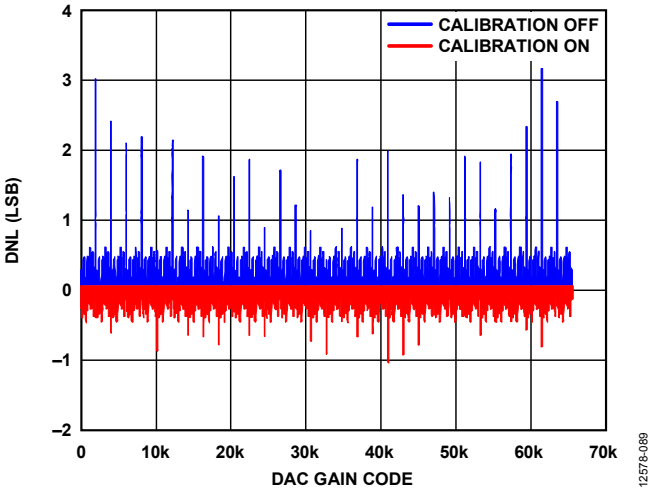


Figure 86. Pre-Calibration and Post-Calibration, DNL

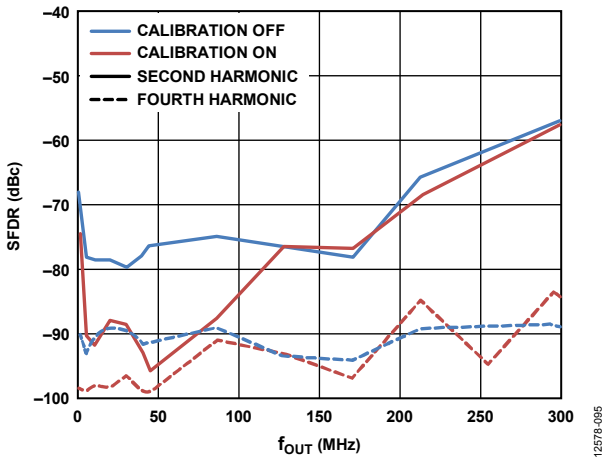


Figure 87. Pre-Calibration and Post-Calibration, HD2 and HD4

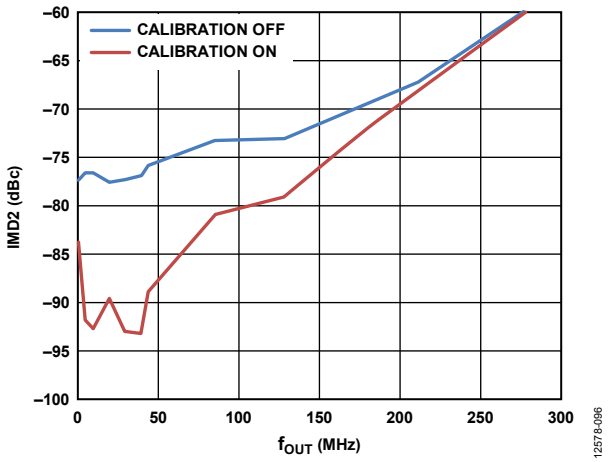


Figure 88. Pre-Calibration and Post-Calibration, IMD2

To calibrate, follow the routine in Table 75.

Table 75. Device Self Calibration Procedure

Addr.	Bit	SPI Data Byte	Description
0x0E7	[7:0]	0x38	Use highest comparator speed and set calibration clock divider
0x0E8			Select DACs to calibrate
	3	0	Set this bit to 0
	2	0b0 or 0b1	1 if DAC1 is enabled
	1	0	Set this bit to 0
	0	0b0 or 0b1	1 if DAC0 is enabled
0x0ED	[7:0]	0xA2	Configure initial value
0x0E9	[7:0]	0x01	Enable calibration
0x0E9	[7:0]	0x03	Start calibration
0x0E7	[7:0]	0x30	Disable calibration clock

For each DAC that is calibrated, verify the calibration status by writing a 1 in the corresponding bit of CAL_PAGE (Register 0x0E8) and reading Register 0x0E9. If the calibration completed correctly, CAL_FIN (Register 0x0E9[7]) = 1 to indicate that calibration is complete, and Register 0x0E9[6:4] = 0 to indicate that no errors have occurred.

The post-calibration result is a function of operating temperature. A set of calibration coefficients obtained at one temperature may not be the optimal setting for a different temperature. Figure 89 and Figure 90 show the typical temperature drift effect after a single run calibration.

For optimal performance, run the calibration again when the operating temperature changes significantly. Note that it is recommended to power down the DAC outputs when running the calibration routine. If continuous transmission is required in the system, running the calibration again during the operation may not be an option. In this case, it is recommended to perform a calibration at the average temperature of the operating temperature range and to use the same set of coefficients during the operation. This results in the best overall performance over temperature.

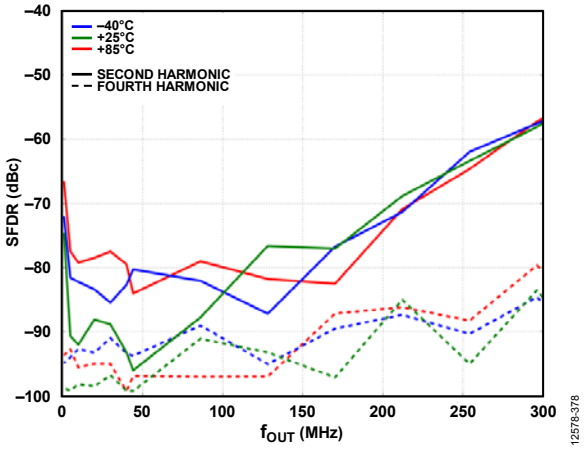


Figure 89. Post-Calibration HD2 and HD4 over Temperature, Calibrated at 25°C

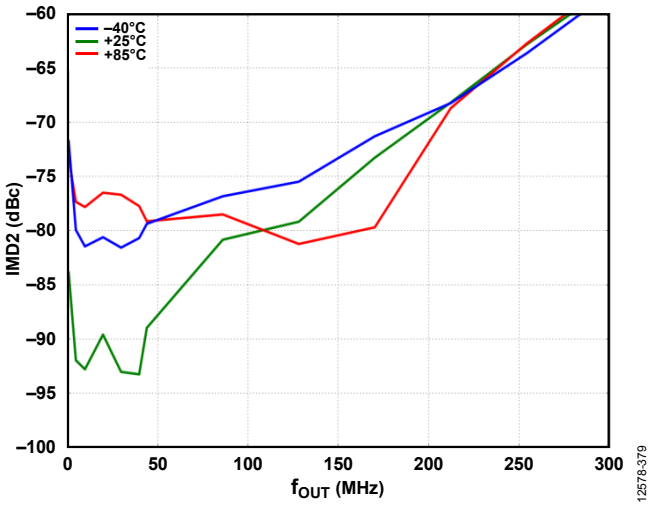


Figure 90. Post-Calibration IMD2 over Temperature, Calibrated at 25°C

DEVICE POWER DISSIPATION

The AD9135/AD9136 have eight supply rails, AVDD33, DVDD12, SVDD12, SIOVDD33, CVDD12, IOVDD, V_{TT}, and PVDD12, which can be driven from five regulators to achieve optimum performance, as shown in Figure 67.

The AVDD33 supply powers the DAC core circuitry. The power dissipation of the AVDD33 supply rail is independent of the digital operating mode and sample rate. The current drawn from the AVDD33 supply rail is typically 68 mA (225 mW) when the full-scale current of DAC0 and DAC1 are set to the nominal value of 20.48 mA.

PVDD12 powers the DAC PLLs and varies depending on the DAC sample rate. CVDD12 can be combined with the PVDD12 regulator, but requires proper bypass capacitor networks near the pins. CVDD12 powers the clock tree, and the current varies directly with the DAC sample rate. DVDD12 powers the DSP core, and the current draw depends on the number of DSP functions and the DAC sample rate used. SVDD12 supplies the SERDES lanes and associated circuitry including the equalizers, SERDES PLL, PHY, and up to the input of the DSP. The current depends on the number lanes and the lane bit rate. IOVDD powers the SPI circuit and draws a very small current.

SIOVDD33 powers the equalizers for the SERDES lanes. The V_{TT} termination voltage draws a very small current of <5 mA.

TEMPERATURE SENSOR

The AD9135/AD9136 have a band gap temperature sensor for monitoring the temperature changes of the AD9135/AD9136. The temperature must be calibrated against a known temperature to remove the device-to-device variation on the band gap circuit used to sense the temperature.

To monitor temperature change, the user must take a reading at a known ambient temperature for a single-point calibration of each AD9135/AD9136 device.

$$Tx = T_{REF} + 7.3 \times (CODE\_X - CODE\_REF)/1000$$

where:
CODE_X is the readback code at the unknown temperature, *Tx*.
CODE_REF is the readback code at the calibrated temperature, T_{REF}.

To use the temperature sensor, it must be enabled by setting Register 0x12F[0] to 1. The user must write a 1 to Register 0x134[0] before reading back the die temperature from Register 0x132 and Register 0x133.

START-UP SEQUENCE

Table 76 through Table 83 show the register writes needed to set up the AD9135/AD9136 with f_{DAC} = 1474.56 MHz, 1× interpolation, and the DAC PLL enabled with a 368.64 MHz reference clock. The JESD204B interface is configured in Mode 11, single-link mode, Subclass 1, and scrambling is enabled with all eight SERDES lanes running at 7.3728 Gbps, inputting twos complement formatted data. No remapping of lanes with the crossbar is used in this example.

The sequence of steps to properly start up the AD9135/AD9136 is as follows:

1. Set up the SPI interface, power up necessary circuit blocks, make required writes to the configuration register, and set up the DAC clocks (see the Step 1: Start Up the DAC section).
2. Set the digital features of the AD9135/AD9136 (see the Step 2: Digital Datapath section).
3. Set up the JESD204B links (see the Step 3: Transport Layer section).
4. Set up the physical layer of the SERDES interface (see the Step 4: Physical Layer section).
5. Set up the data link layer of the SERDES interface. This procedure is for quick startup or debug only and does not guarantee deterministic latency (see the Step 5: Data Link Layer section).
6. Check for errors on Link 0 and Link 1 (see the Step 6: Error Monitoring section).

These steps are outlined in detail in the following sections in tables that list the required register write and read commands.

STEP 1: START UP THE DAC

Power-Up and DAC Initialization

Table 76. Power-Up and DAC Initialization

Command	Address	Value	Description
W	0x000	0xBD	Soft reset
W	0x000	0x3C	Deassert reset, set 4-wire SPI
W	0x011	0x28	Enable reference, DAC channels, and master DAC
W	0x080	0x00	Power up all clocks
W	0x081	0x00	Power up SYSREF± receiver, disable hysteresis

Required Device Configurations

Table 77. Required Device Configurations

Command	Address	Value	Description
W	0x12D	0x8B	Digital datapath configuration
W	0x146	0x01	Digital datapath configuration
W	0x2A4	0xFF	Clock configuration
W	0x232	0xFF	SERDES interface configuration
W	0x333	0x01	SERDES interface configuration

Configure the DAC PLL

Table 78. Configure DAC PLL

Command	Address	Value	Description
W	0x087	0x62	Optimal DAC PLL loop filter settings
W	0x088	0xC9	Optimal DAC PLL loop filter settings
W	0x089	0x0E	Optimal DAC PLL loop filter settings
W	0x08A	0x12	Optimal DAC PLL charge pump settings
W	0x08D	0x7B	Optimal DAC LDO settings for DAC PLL
W	0x1B0	0x00	Power DAC PLL blocks when power machine disabled
W	0x1B9	0x24	Optimal DAC PLL charge pump settings
W	0x1BC	0x0D	Optimal DAC PLL VCO control settings
W	0x1BE	0x02	Optimal DAC PLL VCO power control settings
W	0x1BF	0x8E	Optimal DAC PLL VCO calibration settings
W	0x1C0	0x2A	Optimal DAC PLL lock counter length setting
W	0x1C1	0x2A	Optimal DAC PLL charge pump setting
W	0x1C4	0x7E	Optimal DAC PLL varactor settings
W	0x08B	0x02	Set the VCO LO divider to 8 so that 6 GHz ≤ $f_{VCO} = f_{DAC} \times 2^{(LODivMode+1)} \leq 12$ GHz
W	0x08C	0x03	Set the reference clock divider to 8 so that the reference clock into the PLL is less than 80 MHz
W	0x085	0x10	Set the B counter to 16 to divide the DAC clock down to 2× the reference clock
W	0x1B5	0x09	PLL lookup value from Table 25 for $f_{VCO} \geq 7.25$ GHz
W	0x1BB	0x13	PLL lookup value from Table 25 for $f_{VCO} \geq 7.25$ GHz
W	0x1C5	0x06	PLL lookup value from Table 25 for $f_{VCO} \geq 7.25$ GHz
W	0x083	0x10	Enable DAC PLL
R	0x084	0x01	Verify that Bit 1 reads back high for PLL locked

STEP 2: DIGITAL DATAPATH

Table 79. Digital Datapath

Command	Address	Value	Description
W	0x112	0x00	Set the interpolation to 1×
W	0x110	0x00	Set twos complement data format

STEP 3: TRANSPORT LAYER

Table 80. Link 0 Transport Layer

Command	Address	Value	Description
W	0x200	0x00	Power up the interface
W	0x201	0x00	Enable all lanes
W	0x300	0x08	Bit 3 = 0 for single link, Bit 2 = 0 to access Link 0 registers
W	0x450	0x00	Set the device ID to match Tx (0x00 in this example)
W	0x451	0x00	Set the bank ID to match Tx (0x00 in this example)
W	0x452	0x00	Set the lane ID to match Tx (0x00 in this example)
W	0x453	0x83	Set descrambling and L to 4 (in n − 1 notation) (L = 8 on transmit side)[1]
W	0x454	0x00	Set F = 1 (in n − 1 notation)
W	0x455	0x1F	Set K = 32 (in n − 1 notation)
W	0x456	0x00	Set M to 1 (in n − 1 notation) (M = 2 on transmit side)[1]
W	0x457	0x0F	Set N = 16 (in n − 1 notation)
W	0x458	0x2F	Set Subclass 1 and NP = 16 (in n − 1 notation)
W	0x459	0x21	Set JESD204B Version and S = 2 (in n − 1 notation)
W	0x45A	0x80	Set HD = 1
W	0x45D	0x45	Set checksum for Lane 0
W	0x46C	0xFF	Deskew Lane 0 to Lane 7
W	0x476	0x01	Set F (not in n − 1 notation)
W	0x47D	0xFF	Enable Lane 0 to Lane 7

[1] Note that for Mode 11 through Mode 13, the M and L the parameters programmed on the receive side do not match the parameters on the transmit side. The parameters on the transmit side reflect the true number of converters and lanes per link.

STEP 4: PHYSICAL LAYER

Table 81. Physical Layer

Command	Address	Value	Description
W	0x2AA	0xB7	SERDES interface termination setting
W	0x2AB	0x87	SERDES interface termination setting
W	0x2B1	0xB7	SERDES interface termination setting
W	0x2B2	0x87	SERDES interface termination setting
W	0x2A7	0x01	Autotune PHY setting
W	0x2AE	0x01	Autotune PHY setting
W	0x314	0x01	SERDES SPI configuration
W	0x230	0x28	Configure CDRs in half rate mode
W	0x206	0x00	Resets CDR logic
W	0x206	0x01	Release CDR logic reset
W	0x289	0x04	Configure PLL divider to 1 along with PLL required configuration
W	0x284	0x62	Optimal SERDES PLL loop filter
W	0x285	0xC9	Optimal SERDES PLL loop filter
W	0x286	0x0E	Optimal SERDES PLL loop filter
W	0x287	0x12	Optimal SERDES PLL charge pump
W	0x28A	0x7B	Optimal SERDES PLL VCO LDO
W	0x28B	0x00	Optimal SERDES PLL configuration
W	0x290	0x89	Optimal SERDES PLL VCO varactor
W	0x294	0x24	Optimal SERDES PLL charge pump
W	0x296	0x03	Optimal SERDES PLL VCO
W	0x297	0x0D	Optimal SERDES PLL VCO
W	0x299	0x02	Optimal SERDES PLL configuration
W	0x29A	0x8E	Optimal SERDES PLL VCO varactor
W	0x29C	0x2A	Optimal SERDES PLL charge pump
W	0x29F	0x78	Optimal SERDES PLL VCO varactor
W	0x2A0	0x06	Optimal SERDES PLL VCO varactor
W	0x280	0x01	Enable SERDES PLL
R	0x281	0x01	Verify that Bit 0 reads back high for SERDES PLL lock
W	0x268	0x62	Set EQ mode to low power

STEP 5: DATA LINK LAYER

Note that this procedure does not guarantee deterministic latency.

Table 82. Data Link Layer—Does Not Guarantee Deterministic Latency

Command	Address	Value	Description
W	0x301	0x01	Set subclass = 1
W	0x304	0x00	Set the LMFC delay setting to 0
W	0x305	0x00	Set the LMFC delay setting to 0
W	0x306	0x0A	Set the LMFC receive buffer delay to 10
W	0x307	0x0A	Set the LMFC receive buffer delay to 10
W	0x03A	0x01	Set sync mode to one-shot sync
W	0x03A	0x81	Enable the sync machine
W	0x03A	0xC1	Arm the sync machine
SYSREF± Signal			Ensure that at least one SYSREF± edge is sent to the device
W	0x300	0x01	Bit 0 = 1 to enable Link 0, Bit 2 = 0 to access Link 0

STEP 6: ERROR MONITORING

Link 0 Checks

Confirm that the registers in Table 83 read back as noted and that system tasks are completed as described.

Table 83. Link 0 Checks

Command	Address	Value	Description
R	0x470	0xFF	Acknowledge that four consecutive K28.5 characters have been detected on Lane 0 to Lane 3.
$\overline{\text{SYNCOUT0}}$± Signal			Confirm that $\overline{\text{SYNCOUT0}}$± is high.
SERDINx± Signals			Apply ILAS and data to SERDES input pins.
R	0x471	0xFF	Check for frame sync on all lanes.
R	0x472	0xFF	Check for good checksum.
R	0x473	0xFF	Check for ILAS.

REGISTER MAPS AND DESCRIPTIONS

In the following tables, register addresses (Reg. column) and reset (Reset column) values are hexadecimal and in the read/write (R/W) column, R means read only, W means write only, R/W means read/write, and N/A means not applicable. All values in the register address and reset columns are hexadecimal numbers.

DEVICE CONFIGURATION REGISTER MAP

Table 84. Device Configuration Register Map

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x000	SPI_INTFCONFA	SOFT RESET_M	LSBFIRST_ M	ADDRINC_M	SDOACTIVE_M	SDOACTIVE	ADDRINC	LSBFIRST	SOFTRESET	0x00	R/W
0x003	CHIPTYPE	CHIPTYPE								0x04	R
0x004	PRODIDL	PRODIDL								0x44	R
0x005	PRODIDH	PRODIDH								0x91	R
0x006	CHIPGRADE	PROD_GRADE				DEV_REVISION				0x48/ 0x68	R
0x008	SPI_PAGEINDX	RESERVED						DAC_PAGE		0x03	R/W
0x00A	SCRATCH_PAD	SCRATCHPAD								0x00	R/W
0x011	PWRCNTRL0	PD_BG	PD_DAC_0	RESERVED	PD_DAC_1	RESERVED	PD_DACM	RESERVED		0x7C	R/W
0x012	TXENMASK	RESERVED						DAC1_MASK	DAC0_MASK	0x00	R/W
0x013	PWRCNTRL3	RESERVED		TX_PROTECT_ OUT	RESERVED	SPI_PROTECT_OUT	SPI_PROTECT	RESERVED		0x20	R/W
0x014	GROUP_DLY	RESERVED				GROUP_DLY				0x88	R/W
0x01F	IRQEN_ STATUSMODE0	IRQEN_ SMODE_ CALPASS	IRQEN_ SMODE_ CALFAIL	IRQEN_ SMODE_ DACPLLLOST	IRQEN_SMODE_ DACPLLLOCK	IRQEN_SMODE_ SERPLLLOST	IRQEN_SMODE_ SERPLLLOCK	IRQEN_ SMODE_ LANEFIFOERR	RESERVED	0x00	R/W
0x020	IRQEN_ STATUSMODE1	RESERVED					IRQEN_SMODE_ PRBS1	RESERVED	IRQEN_ SMODE_ PRBS0	0x00	R/W
0x021	IRQEN_ STATUSMODE2	IRQEN_ SMODE_ PDPERR0	RESERVED	IRQEN_ SMODE_ BLNKDONE0	RESERVED	IRQEN_SMODE_ SYNC_LOCK0	IRQEN_SMODE_ SYNC_ROTATE0	IRQEN_ SMODE_ SYNC_ WLIM0	IRQEN_ SMODE_ SYNC_TRIP0	0x00	R/W
0x022	IRQEN_ STATUSMODE3	IRQEN_ SMODE_ PDPERR1	RESERVED	IRQEN_ SMODE_ BLNKDONE1	RESERVED	IRQEN_SMODE_ SYNC_LOCK1	IRQEN_SMODE_ SYNC_ROTATE1	IRQEN_ SMODE_ SYNC_ WLIM1	IRQEN_ SMODE_ SYNC_TRIP1	0x00	R/W
0x023	IRQ_STATUS0	CALPASS	CALFAIL	DACPLLLOST	DACPLLLOCK	SERPLLLOST	SERPLLLOCK	LANEFIFO-ERR	RESERVED	0x00	R
0x024	IRQ_STATUS1	RESERVED					PRBS1	RESERVED	PRBS0	0x00	R
0x025	IRQ_STATUS2	PDPERR0	RESERVED	BLNKDONE0	RESERVED	SYNC_LOCK0	SYNC_ROTATE0	SYNC_ WLIM0	SYNC_TRIP0	0x00	R
0x026	IRQ_STATUS3	PDPERR1	RESERVED	BLNKDONE1	RESERVED	SYNC_LOCK1	SYNC_ROTATE1	SYNC_ WLIM1	SYNC_TRIP1	0x00	R
0x030	JESD_CHECKS	RESERVED		ERR_DLYOVER	ERR_WINLIMIT	ERR_JESDBAD	ERR_KUNSUPP	ERR_ SUBCLASS	ERR_INTSUPP	0x00	R
0x034	SYNC_ ERRWINDOW	RESERVED						ERRWINDOW		0x00	R/W
0x038	SYNC_LASTERR_L	RESERVED				LASTERROR				0x00	R
0x039	SYNC_LASTERR_H	LASTUN-DER	LASTOVER	RESERVED						0x00	R
0x03A	SYNC_CONTROL	SYNC-ENABLE	SYNCARM	SYNCCLRSTKY	SYNCCLRLAST	SYNCMODE				0x00	R/W
0x03B	SYNC_STATUS	SYNC_ BUSY	RESERVED			SYNC_LOCK	SYNC_ ROTATE	SYNC_WLIM	SYNC_ TRIP	0x00	R
0x03C	SYNC_CURRERR_L	RESERVED				CURRERROR				0x00	R
0x03D	SYNC_CURRERR_H	CURRUN-DER	CURROVER	RESERVED						0x00	R

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x040	DACGAIN0_1	RESERVED						DACFSC_0[9:8]		0x00	R/W
0x041	DACGAIN0_0	DACFSC_0[7:0]								0x00	R/W
0x044	DACGAIN1_1	RESERVED						DACFSC_1[9:8]		0x00	R/W
0x045	DACGAIN1_0	DACFSC_1[7:0]								0x00	R/W
0x080	CLKCFG0	PD_CLK0	PD_CLK1	PD_CLK_DIG	PD_SERDES_PCLK	PD_CLK_REC	RESERVED			0xF8	R/W
0x081	SYSREF_ACTRL0	RESERVED			PD_SYSREF	HYS_ON	SYSREF_RISE	HYS_CNTRL1		0x10	R/W
0x082	SYSREF_ACTRL1	HYS_CNTRL0								0x00	R/W
0x083	DACPLLCNTRL	RECAL_DACPLL	RESERVED		ENABLE_DACPLL	RESERVED				0x00	R/W
0x084	DACPLLSTATUS	DACPLL_OVER-RANGE_H	DACPLL_OVER-RANGE_L	DACPLL_CAL_VALID	RESERVED			DACPLL_LOCK	RESERVED	0x00	R
0x085	DACINTEGER-WORD0	B_COUNT								0x08	R/W
0x087	DACLOOPFILT1	LF_C2_WORD				LF_C1_WORD				0x88	R/W
0x088	DACLOOPFILT2	LF_R1_WORD				LF_C3_WORD				0x88	R/W
0x089	DACLOOPFILT3	LF_BYPASS_R3	LF_BYPASS_R1	LF_BYPASS_C2	LF_BYPASS_C1	LF_R3_WORD				0x08	R/W
0x08A	DACCPCNTRL	RESERVED		CP_CURRENT						0x20	R/W
0x08B	DACLOGENCNTRL	RESERVED						LO_DIV_MODE		0x02	R/W
0x08C	DACLDOCNTRL1	RESERVED					REF_DIV_MODE			0x01	R/W
0x08D	DACLDOCNTRL2	DAC_LDO								0x2B	R/W
0x0E2	CAL_CTRL_GLOBAL	RESERVED						CAL_START_AVG	CAL_EN_AVG	0x00	R/W
0x0E7	CAL_CLKDIV	RESERVED				CAL_CLK_EN	RESERVED			0x30	R/W
0x0E8	CAL_PAGE	RESERVED				CAL_PAGE				0x0F	R/W
0x0E9	CAL_CTRL	CAL_FIN	CAL_ACTIVE	CAL_ERRHI	CAL_ERRLO	RESERVED		CAL_START	CAL_EN	0x00	R/W
0x0ED	CAL_INIT	CAL_INIT								A6	R/W
0x110	DATA_FORMAT	BINARY_FORMAT	RESERVED							00	R/W
0x111	DATAPATH_CTRL	INVSINC_ENABLE	RESERVED	DIG_GAIN_ENABLE	RESERVED					0xA0	R/W
0x112	INTERP_MODE	RESERVED					INTERP_MODE			0x01	R/W
0x11F	TXEN_SM_0	FALL_COUNTERS		RISE_COUNTERS		RESERVED	PROTECT_OUT_INVERT	RESERVED		0x83	R/W
0x121	TXEN_RISE_COUNT_0	RISE_COUNT_0								0x0F	R/W
0x122	TXEN_RISE_COUNT_1	RISE_COUNT_1								0x00	R/W
0x123	TXEN_FALL_COUNT_0	FALL_COUNT_0								0xFF	R/W
0x124	TXEN_FALL_COUNT_1	FALL_COUNT_1								0xFF	R/W
0x12D	DEVICE_CONFIG_REG_0	DEVICE_CONFIG_0								0x46	R/W
0x12F	DIE_TEMP_CTRL0	RESERVED							AUXADC_ENABLE	0x20	R/W
0x132	DIE_TEMP0	DIE_TEMP[7:0]								0x00	R
0x133	DIE_TEMP1	DIE_TEMP[15:8]								0x00	R
0x134	DIE_TEMP_UPDATE	RESERVED							DIE_TEMP_UPDATE	0x00	R/W

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x135	DC_OFFSET_CTRL	RESERVED							DC_OFFSET_ON	0x00	R/W
0x136	DAC_DC_OFFSET_1PART0	LSB_OFFSET[7:0]								0x00	R/W
0x137	DAC_DC_OFFSET_1PART1	LSB_OFFSET[15:8]								0x00	R/W
0x13A	DAC_DC_OFFSET_2PART	RESERVED			SIXTEENTH_OFFSET					0x00	R/W
0x13C	DAC_DIG_GAIN0	DAC_DIG_GAIN[7:0]								0xEA	R/W
0x13D	DAC_DIG_GAIN1	RESERVED				DAC_DIG_GAIN[11:8]				0x0A	R/W
0x140	GAIN_RAMP_UP_STEP0	GAIN_RAMP_UP_STEP[7:0]								0x04	R/W
0x141	GAIN_RAMP_UP_STEP1	RESERVED				GAIN_RAMP_UP_STEP[11:8]				0x00	R/W
0x142	GAIN_RAMP_DOWN_STEP0	GAIN_RAMP_DOWN_STEP[7:0]								0x09	R/W
0x143	GAIN_RAMP_DOWN_STEP1	RESERVED				GAIN_RAMP_DOWN_STEP[11:8]				0x00	R/W
0x146	DEVICE_CONFIG_REG_1	DEVICE_CONFIG_1								0x00	R/W
0x147	BSM_STAT	SOFTBLANKRB		RESERVED						0x00	R
0x14B	PRBS	RESERVED	PRBS_GOOD	RESERVED			PRBS_MODE	PRBS_RESET	PRBS_EN	0x10	R/W
0x14C	PRBS_ERROR	PRBS_COUNT								0x00	R
0x1B0	DACPLLT0	DAC_PLL_PWR								0xFA	R/W
0x1B5	DACPLLT5	RESERVED				VCO_VAR				0x83	R/W
0x1B9	DACPLLT9	DAC_PLL_CP1								0x34	R/W
0x1BB	DACPLLTB	RESERVED			VCO_BIAS_TCF		VCO_BIAS_REF			0x0C	R/W
0x1BC	DACPLLTC	DAC_PLL_VCO_CTRL								0x00	R/W
0x1BE	DACPLLTE	DAC_PLL_VCO_PWR								0x00	R/W
0x1BF	DACPLLTF	DAC_PLL_VCOCAL								0x8D	R/W
0x1C0	DACPLLT10	DAC_PLL_LOCK_CNTR								0x2E	R/W
0x1C1	DACPLLT11	DAC_PLL_CP2								0x24	R/W
0x1C4	DACPLLT17	DAC_PLL_VAR1								0x33	R/W
0x1C5	DACPLLT18	DAC_PLL_VAR2								0x08	R/W
0x200	MASTER_PD	RESERVED							SPI_PD_MASTER	0x01	R/W
0x201	PHY_PD	SPI_PD_PHY								0x00	R/W
0x203	GENERIC_PD	RESERVED						SPI_SYNC1_PD	SPI_SYNC2_PD	0x00	R/W
0x206	CDR_RESET	RESERVED							SPI_CDR_RESETN	0x01	R/W
0x230	CDR_OPERATING_MODE_REG_0	RESERVED		ENHALFRATE	RESERVED			CDR_OVERSAMP	RESERVED	0x28	R/W
0x232	DEVICE_CONFIG_REG_3	DEVICE_CONFIG_3								0x0	R/W
0x268	EQ_BIAS_REG	EQ_POWER_MODE		RESERVED						0x62	R/W
0x280	SERDESPLL_ENABLE_CNTRL	RESERVED					RECAL_SERDESPLL	RESERVED	ENABLE_SERDESPLL	0x00	R/W
0x281	PLL_STATUS	RESERVED		SERDES_PLL_OVERRANGE_H	SERDES_PLL_OVERRANGE_L	SERDES_PLL_CAL_VALID_RB	RESERVED		SERDES_PLL_LOCK_RB	0x00	R
0x284	LOOP_FILTER_1	LOOP_FILTER_1								0x77	R/W
0x285	LOOP_FILTER_2	LOOP_FILTER_2								0x87	R/W
0x286	LOOP_FILTER_3	LOOP_FILTER_3								0x08	R/W

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x287	SERDES_PLL_CP1	SERDES_PLL_CP1								0x3F	R/W
0x289	REF_CLK_ DIVIDER_LDO	RESERVED					DEVICE_ CONFIG_4	SERDES_PLL_DIV_MODE		0x00	R/W
0x28A	VCO_LDO	SERDES_PLL_VCO_LDO								0x2B	R/W
0x28B	SERDES_PLL_PD1	SERDES_PLL_PD1								0x7F	R/W
0x290	SERDESPLL_VAR1	SERDES_PLL_VAR1								0x83	R/W
0x294	SERDES_PLL_CP2	SERDES_PLL_CP2								0xB0	R/W
0x296	SERDESPLL_VCO1	SERDES_PLL_VCO1								0x0C	R/W
0x297	SERDESPLL_VCO2	SERDES_PLL_VCO2								0x00	R/W
0x299	SERDES_PLL_PD2	SERDES_PLL_PD2								0x00	R/W
0x29A	SERDESPLL_VAR2	SERDES_PLL_VAR2								0xFE	R/W
0x29C	SERDES_PLL_CP3	SERDES_PLL_CP3								0x17	R/W
0x29F	SERDESPLL_VAR3	SERDES_PLL_VAR3								0x33	R/W
0x2A0	SERDESPLL_VAR4	SERDES_PLL_VAR4								0x08	R/W
0x2A4	DEVICE_CONFIG_ REG_8	DEVICE_CONFIG_8								0x4B	R/W
0x2A5	SYNCOUTB_ SWING	RESERVED							SYNCOUTB_ SWING_MD	0x00	R/W
0x2A7	TERM_BLK1_ CTRLREG0	RESERVED							RCAL_ TERMBLK1	0x00	R/W
0x2AA	DEVICE_CONFIG_ REG_9	DEVICE_CONFIG_9								0xC3	R/W
0x2AB	DEVICE_CONFIG_ REG_10	DEVICE_CONFIG_10								0x93	R/W
0x2AE	TERM_BLK2_ CTRLREG0	RESERVED							RCAL_ TERMBLK2	0x00	R/W
0x2B1	DEVICE_CONFIG_ REG_11	DEVICE_CONFIG_11								0xC3	R/W
0x2B2	DEVICE_CONFIG_ REG_12	DEVICE_CONFIG_12								0x93	R/W
0x300	GENERAL_JRX_ CTRL_0	RESERVED	CHECKSUM _MODE	RESERVED		LINK_MODE	LINK_PAGE	LINK_EN		0x00	R/W
0x301	GENERAL_JRX_ CTRL_1	RESERVED					SUBCLASSV_LOCAL			0x01	R/W
0x302	DYN_LINK_ LATENCY_0	RESERVED			DYN_LINK_LATENCY_0					0x00	R
0x303	DYN_LINK_ LATENCY_1	RESERVED			DYN_LINK_LATENCY_1					0x00	R
0x304	LMFC_DELAY_0	RESERVED			LMFC_DELAY_0					0x00	R/W
0x305	LMFC_DELAY_1	RESERVED			LMFC_DELAY_1					0x00	R/W
0x306	LMFC_VAR_0	RESERVED			LMFC_VAR_0					0x06	R/W
0x307	LMFC_VAR_1	RESERVED			LMFC_VAR_1					0x06	R/W
0x308	XBAR_LN_0_1	RESERVED		LOGICAL_LANE1_SRC			LOGICAL_LANE0_SRC			0x08	R/W
0x309	XBAR_LN_2_3	RESERVED		LOGICAL_LANE3_SRC			LOGICAL_LANE2_SRC			0x1A	R/W
0x30A	XBAR_LN_4_5	RESERVED		LOGICAL_LANE5_SRC			LOGICAL_LANE4_SRC			0x2C	R/W
0x30B	XBAR_LN_6_7	RESERVED		LOGICAL_LANE7_SRC			LOGICAL_LANE6_SRC			0x3E	R/W
0x30C	FIFO_STATUS_ REG_0	LANE_FIFO_FULL								0x00	R
0x30D	FIFO_STATUS_ REG_1	LANE_FIFO_EMPTY								0x00	R
0x312	SYNCB_GEN_1	RESERVED		SYNCB_ERR_DUR		RESERVED				0x00	R/W
0x314	SERDES_SPI_REG	SERDES_SPI_CONFIG								0x00	R/W
0x315	PHY_PRBS_TEST_ EN	PHY_TEST_EN								0x00	R/W

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x316	PHY_PRBS_TEST_CTRL	RESERVED	PHY_SRC_ERR_CNT			PHY_PRBS_PAT_SEL		PHY_TEST_START	PHY_TEST_RESET	0x00	R/W
0x317	PHY_PRBS_TEST_THRESHOLD_LOBITS	PHY_PRBS_THRESHOLD[7:0]								0x00	R/W
0x318	PHY_PRBS_TEST_THRESHOLD_MIDBITS	PHY_PRBS_THRESHOLD[15:8]								0x00	R/W
0x319	PHY_PRBS_TEST_THRESHOLD_HIBITS	PHY_PRBS_THRESHOLD[23:16]								0x00	R/W
0x31A	PHY_PRBS_TEST_ERRCNT_LOBITS	PHY_PRBS_ERR_CNT[7:0]								0x00	R
0x31B	PHY_PRBS_TEST_ERRCNT_MIDBITS	PHY_PRBS_ERR_CNT[15:8]								0x00	R
0x31C	PHY_PRBS_TEST_ERRCNT_HIBITS	PHY_PRBS_ERR_CNT[23:16]								0x00	R
0x31D	PHY_PRBS_TEST_STATUS	PHY_PRBS_PASS								0xFF	R
0x32C	SHORT_TPL_TEST_0	RESERVED		SHORT_TPL_SP_SEL		SHORT_TPL_DAC_SEL		SHORT_TPL_TEST_RESET	SHORT_TPL_TEST_EN	0x00	R/W
0x32D	SHORT_TPL_TEST_1	SHORT_TPL_REF_SP_LSB								0x00	R/W
0x32E	SHORT_TPL_TEST_2	SHORT_TPL_REF_SP_MSB								0x00	R/W
0x32F	SHORT_TPL_TEST_3	RESERVED							SHORT_TPL_FAIL	0x00	R
0x333	DEVICE_CONFIG_REG_13	DEVICE_CONFIG_13								0x00	R/W
0x334	JESD_BIT_INVERSE_CTRL	JESD_BIT_INVERSE								0x00	R/W
0x400	DID_REG	DID_RD								0x00	R
0x401	BID_REG	ADJCNT_RD				BID_RD				0x00	R
0x402	LID0_REG	RESERVED	ADJDIR_RD	PHADJ_RD		LID0_RD				0x00	R
0x403	SCR_L_REG	SCR_RD	RESERVED			L-1_RD				0x00	R
0x404	F_REG	F-1_RD								0x00	R
0x405	K_REG	RESERVED				K-1_RD				0x00	R
0x406	M_REG	M-1_RD								0x00	R
0x407	CS_N_REG	CS_RD		RESERVED		N-1_RD				0x00	R
0x408	NP_REG	SUBCLASSV_RD				NP-1_RD				0x00	R
0x409	S_REG	JESDV_RD				S-1_RD				0x00	R
0x40A	HD_CF_REG	HD_RD	RESERVED			CF_RD				0x00	R
0x40B	RES1_REG	RES1_RD								0x00	R
0x40C	RES2_REG	RES2_RD								0x00	R
0x40D	CHECKSUM_REG	FCHK0_RD								0x00	R
0x40E	COMPSUM0_REG	FCMP0_RD								0x00	R
0x412	LID1_REG	RESERVED				LID1_RD				0x00	R
0x415	CHECKSUM1_REG	FCHK1_RD								0x00	R
0x416	COMPSUM1_REG	FCMP1_RD								0x00	R
0x41A	LID2_REG	RESERVED				LID2_RD				0x00	R
0x41D	CHECKSUM2_REG	FCHK2_RD								0x00	R
0x41E	COMPSUM2_REG	FCMP2_RD								0x00	R
0x422	LID3_REG	RESERVED				LID3_RD				0x00	R
0x425	CHECKSUM3_REG	FCHK3_RD								0x00	R

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x426	COMPSUM3_REG	FCMP3_RD								0x00	R
0x42A	LID4_REG	RESERVED				LID4_RD				0x00	R
0x42D	CHECKSUM4_REG	FCHK4_RD								0x00	R
0x42E	COMPSUM4_REG	FCMP4_RD								0x00	R
0x432	LID5_REG	RESERVED				LID5_RD				0x00	R
0x435	CHECKSUM5_REG	FCHK5_RD								0x00	R
0x436	COMPSUM5_REG	FCMP5_RD								0x00	R
0x43A	LID6_REG	RESERVED				LID6_RD				0x00	R
0x43D	CHECKSUM6_REG	FCHK6_RD								0x00	R
0x43E	COMPSUM6_REG	FCMP6_RD								0x00	R
0x442	LID7_REG	RESERVED				LID7_RD				0x00	R
0x445	CHECKSUM7_REG	FCHK7_RD								0x00	R
0x446	COMPSUM7_REG	FCMP7_RD								0x00	R
0x450	ILS_DID	DID								0x00	R/W
0x451	ILS_BID	ADJCNT				BID				0x00	R/W
0x452	ILS_LID0	RESERVED	ADJDIR	PHADJ		LID0				0x00	R/W
0x453	ILS_SCR_L	SCR	RESERVED			L-1				0x83	R/W
0x454	ILS_F	F-1								0x00	R/W
0x455	ILS_K	RESERVED				K-1				0x1F	R/W
0x456	ILS_M	M-1								0x01	R/W
0x457	ILS_CS_N	CS		RESERVED		N-1				0x0F	R/W
0x458	ILS_NP	SUBCLASSV				NP-1				0x2F	R/W
0x459	ILS_S	JESDV				S-1				0x20	R/W
0x45A	ILS_HD_CF	HD	RESERVED			CF				0x80	R/W
0x45B	ILS_RES1	RES1								0x00	R/W
0x45C	ILS_RES2	RES2								0x00	R/W
0x45D	ILS_CHECKSUM	FCHK0								0x45	R/W
0x46B	ERRCNTRMON_RB	READERRORCNTR								0x00	R
0x46B	ERRCNTRMON	RESERVED	LANESEL			RESERVED		CNTRSEL		0x00	R/W
0x46C	LANEDESKEW	LANEDESKEW								0x0F	R/W
0x46D	BADDISPARITY_RB	BADDIS								0x00	R
0x46D	BADDISPARITY	RST_IRQ_DIS	DISABLE_ERR_CNTR_DIS	RST_ERR_CNTR_DIS	RESERVED		LANE_ADDR_DIS			0x00	R/W
0x46E	NIT_RB	NIT								0x00	R
0x46E	NIT_W	RST_IRQ_NIT	DISABLE_ERR_CNTR_NIT	RST_ERR_CNTR_NIT	RESERVED		LANE_ADDR_NIT			0x00	R/W
0x46F	UNEXPECTED-CONTROL_RB	UCC								0x00	R
0x46F	UNEXPECTED-CONTROL_W	RST_IRQ_UCC	DISABLE_ERR_CNTR_UCC	RST_ERR_CNTR_UCC	RESERVED		LANE_ADDR_UCC			0x00	R/W
0x470	CODEGRPSYNCFLG	CODEGRPSYNC								0x00	R/W
0x471	FRAMESYNCFLG	FRAMESYNC								0x00	R/W
0x472	GOODCHKSUMFLG	GOODCHECKSUM								0x00	R/W
0x473	INITLANESYNCFLG	INITIALLANESYNC								0x00	R/W
0x476	CTRLREG1	F								0x01	R/W
0x477	CTRLREG2	ILAS_MODE	RESERVED			THRESHOLD_MASK_EN	RESERVED			0x00	R/W
0x478	KVAL	KSYNC								0x01	R/W

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x47A	IRQVECTOR_MASK	BADDIS_ MASK	NIT_MASK	UCC_ MASK	RESERVED	INITIALLANESYNC_ MASK	BADCHECKSUM _MASK	FRAMESYNC_ MASK	CODEGRP-SYNC_MASK	0x00	R/W
0x47A	IRQVECTOR_FLAG	BADDIS_ FLAG	NIT_FLAG	UCC_FLAG	RESERVED	INITIALLANESYNC_ FLAG	BADCHECKSUM _FLAG	FRAMESYNC_ FLAG	CODEGRP-SYNC_FLAG	0x00	R
0x47B	SYNCASSERTION-MASK	BADDIS_S	NIT_S	UCC_S	CMM	CMM_ENABLE	RESERVED			0x008	R/W
0x47C	ERRORTHRES	ETH								0xFF	R/W
0x47D	LANEENABLE	LANE_ENA								0x0F	R/W
0x47E	RAMP_ENA	RESERVED							ENA_RAMP_ CHECK	0x00	R/W
0x520	DIG_TEST0	RESERVED						DC_TEST_ MODE	RESERVED	0x1C	R/W
0x521	DC_TEST_VALUE0	DC_TEST_VALUE[7:0]								0x00	R/W
0x522	DC_TEST_VALUE1	DC_TEST_VALUE[15:8]								0x00	R/W

DEVICE CONFIGURATION REGISTER DESCRIPTIONS

Table 85. Device Configuration Register Descriptions

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x000	SPI_INTFCONFA	7	SOFTRESET_M		Soft Reset (Mirror).	0x0	R
		6	LSBFIRST_M		LSB First (Mirror).	0x0	R
		5	ADDRINC_M		Address Increment (Mirror).	0x0	R
		4	SDOACTIVE_M		SDO Active (Mirror).	0x0	R
		3	SDOACTIVE		SDO Active.	0x0	R/W
		2	ADDRINC		Address Increment. Controls whether addresses are incremented or decremented during multibyte data transfers.	0x0	R/W
				1	Addresses are incremented during multibyte data transfers		
				0	Addresses are decremented during multibyte data transfers		
		1	LSBFIRST		LSB First. Controls whether input and output data are oriented as LSB first or MSB first.	0x0	R/W
				1	Shift LSB in first		
				0	Shift MSB in first		
		0	SOFTRESET		Soft Reset. Setting this bit initiates a reset. This bit is autoclearing after the soft reset is complete.	0x0	R/W
				1	Assert soft reset		
0x003	CHIPTYPE	[7:0]	CHIPTYPE		The product type is "High Speed DAC", which is represented by a code of 0x04.	0x4	R
0x004	PRODIDL	[7:0]	PRODIDL		Product Identification Low.	0x44	R
0x005	PRODIDH	[7:0]	PRODIDH		Product Identification High.	0x91	R
0x006	CHIPGRADE	[7:4]	PROD_GRADE		Product Grade.		R
					AD9136	0x6	R
					AD9135	0x4	R
		[3:0]	DEV_REVISION		Device Revision.	0x8	R
0x008	SPI_PAGEINDX	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	DAC_PAGE		DAC Paging. Selects which DAC is accessed and written to when changing digital features, such as digital gain, dc offset. This paging affects Register 0x013 to Register 0x014, Register 0x034 to Register 0x03D, Register 0x110 to Register 0x124, and Register 0x135 to Register 0x14C.	0x3	R/W
				0b01	Read and write DAC0		
				0b10	Read and write DAC1		
				0b11	Write both DACs; read DAC0		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x00A	SCRATCH_PAD	[7:0]	SCRATCHPAD		This register does not affect any functions in the part and can be used for testing SPI communication with the part. Any value written to this register will be read back to reflect the change unless a reset or power-cycle occurs.	0x00	R/W
0x011	PWRCNTRL0	7	PD_BG		Reference Power-Down. Powers down the band gap reference for the entire chip. Circuits will not be provided with bias currents.	0x0	R/W
				1	Power down reference		
		6	PD_DAC_0		Powers Down DAC0. Powers down the I-channel DAC.	0x1	R/W
				1	Powers down DAC0		
		5	RESERVED		Reserved.	0x0	R
		4	PD_DAC_1		Powers Down DAC1. Powers down the Q-channel DAC.	0x1	R/W
				1	Powers down DAC1		
		3	RESERVED		Reserved.	0x0	R
		2	PD_DACM		Powers Down the DAC Master Bias. The master bias cell provides currents and DAC full-scale adjustments to the four DACs. With the DAC master bias powered down, the DACs are inoperative.	0x1	R/W
				1	Powers down the DAC master bias		
		[1:0]	RESERVED		Reserved.	0x0	R
0x012	TXENMASK	[7:2]	RESERVED		Reserved.	0x0	R
		1	DAC1_MASK		DAC1 TXEN1 Mask. Power down DAC1 on a falling edge of TXEN1.	0x0	R/W
				1	If TXEN1 is low, power down DAC1		
		0	DAC0_MASK		DAC0 TXEN0 Mask. Power down DAC0 on a falling edge of TXEN0.	0x0	R/W
				1	If TXEN0 is low, power down DAC0		
0x013	PWRCNTRL3	[7:6]	RESERVED		Reserved.	0x0	R
		5	TX_PROTECT_OUT	1	TX_PROTECT triggers PROTECT_OUTx.	0x1	R/W
		4	RESERVED		Reserved.	0x0	R
		3	SPI_PROTECT_OUT	1	SPI_PROTECT triggers PROTECT_OUTx.	0x0	R/W
		2	SPI_PROTECT		SPI_PROTECT	0x0	R/W
		[1:0]	RESERVED		Reserved.	0x0	R
0x014	GROUP_DLY	[7:4]	RESERVED		Reserved.	0x8	R
		[3:0]	GROUP_DLY		Group Delay Control. Delays the selected DAC channel output per the paging register. 0 = minimum delay. 15 = maximum delay. The range of the delay is −4 to +3.5 DAC clock periods, and the resolution is 1/2 DAC clock period.	0x8	R/W
0x01F	IRQEN_STATUSMODE0	7	IRQEN_SMODE_CALPASS		Calibration Pass Detection Status Mode.	0x0	R/W
				1	If CALPASS goes high, it latches and pulls $\overline{IRQ}$ low		
				0	CALPASS shows current status		
		6	IRQEN_SMODE_CALFAIL		Calibration Fail Detection Status Mode.	0x0	R/W
				1	If CALFAIL goes high, it latches and pulls $\overline{IRQ}$ low		
				0	CALFAIL shows current status		
		5	IRQEN_SMODE_DACPLLLOST		DAC PLL Lost Detection Status Mode.	0x0	R/W
				1	If DACPLLLOST goes high, it latches and pulls $\overline{IRQ}$ low		
				0	DACPLLLOST shows current status		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		4	IRQEN_SMODE_ DACPLLLOCK		DAC PLL Lock Detection Status Mode.	0x0	R/W
				1	If DACPLLLOCK goes high, it latches and pulls $\overline{IRQ}$ low		
				0	DACPLLLOCK shows current status		
		3	IRQEN_SMODE_ SERPLLLOST		SERDES PLL Lost Detection Status Mode.	0x0	R/W
				1	If SERPLLLOST goes high, it latches and pulls $\overline{IRQ}$ low		
				0	SERPLLLOST shows current status		
		2	IRQEN_SMODE_ SERPLLLOCK		SERDES PLL Lock Detection Status Mode.	0x0	R/W
				1	If SERPLLLOCK goes high, it latches and pulls $\overline{IRQ}$ low		
				0	SERPLLLOCK shows current status		
		1	IRQEN_SMODE_ LANEFIFOERR		Lane FIFO Error Detection Status Mode.	0x0	R/W
				1	If LANEFIFOERR goes high, latches and pulls $\overline{IRQ}$ low		
				0	LANEFIFOERR shows current status		
		0	RESERVED		Reserved.	0x0	R
0x020	IRQEN_ STATUSMODE1	[7:3]	RESERVED		Reserved.	0x0	R
		2	IRQEN_SMODE_ PRBS1		DAC1 PRBS Error Status Mode.	0x0	R/W
				1	If PRBS1 goes high, it latches and pulls $\overline{IRQ}$ low		
				0	PRBS1 shows current status		
		1	RESERVED			0x0	R/W
		0	IRQEN_SMODE_ PRBS0		DAC0 PRBS Error Status Mode.	0x0	R/W
				1	If PRBS0 goes high, it latches and pulls $\overline{IRQ}$ low		
				0	PRBS0 shows current status		
0x021	IRQEN_ STATUSMODE2	7	IRQEN_SMODE_ PDPERR0		DAC0 PDP Error.	0x0	R/W
				1	If PDPERR0 goes high, it latches and pulls $\overline{IRQ}$ low		
				0	PDPERR0 shows current status		
		6	RESERVED		Reserved.	0x0	R
		5	IRQEN_SMODE_ BLNKDONE0		DAC0 Blanking Done Status Mode.	0x0	R/W
				1	If BLNKDONE0 goes high, it latches and pulls $\overline{IRQ}$ low		
				0	BLNKDONE0 shows current status		
		4	RESERVED		Reserved.	0x0	R
		3	IRQEN_SMODE_ SYNC_LOCK0		DAC0 Alignment Locked Status Mode.	0x0	R/W
				1	If SYNC_LOCK0 goes high, it latches and pulls $\overline{IRQ}$ low		
				0	SYNC_LOCK0 shows current status		
		2	IRQEN_SMODE_ SYNC_ROTATE0		DAC0 Alignment Rotate Status Mode.	0x0	R/W
				1	If SYNC_ROTATE0 goes high, it latches and pulls $\overline{IRQ}$ low		
				0	SYNC_ROTATE0 shows current status		
		1	IRQEN_SMODE_ SYNC_WLIM0		DAC0 Outside Window Status Mode.	0x0	R/W
				1	If SYNC_WLIM0 goes high, it latches and pulls $\overline{IRQ}$ low		
				0	SYNC_WLIM0 shows current status		
		0	IRQEN_SMODE_ SYNC_TRIP0		DAC0 Alignment Tripped Status Mode.	0x0	R/W
				1	If SYNC_TRIP0 goes high, it latches and pulls $\overline{IRQ}$ low		
				0	SYNC_TRIP0 shows current status		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x022	IRQEN_ STATUSMODE3	7	IRQEN_SMODE_ PDPERR1		DAC1 PDP Error.	0x0	R/W
				1	If PDPERR1 goes high, it latches and pulls $\overline{IRQ}$ low		
				0	PDPERR1 shows current status		
		6	RESERVED		Reserved.	0x0	R
		5	IRQEN_SMODE_ BLNKDONE1		DAC1 Blanking Done Status Mode.	0x0	R/W
				1	If BLNKDONE1 goes high, it latches and pulls $\overline{IRQ}$ low		
				0	BLNKDONE1 shows current status		
		4	RESERVED		Reserved.	0x0	R
		3	IRQEN_SMODE_ SYNC_LOCK1		DAC1 Alignment Locked Status Mode.	0x0	R/W
				1	If SYNC_LOCK1 goes high, it latches and pulls $\overline{IRQ}$ low		
				0	SYNC_LOCK1 shows current status		
		2	IRQEN_SMODE_ SYNC_ROTATE1		DAC1 Alignment Rotate Status Mode.	0x0	R/W
				1	If SYNC_ROTATE1 goes high, it latches and pulls $\overline{IRQ}$ low		
				0	SYNC_ROTATE1 shows current status		
		1	IRQEN_SMODE_ SYNC_WLIM1		DAC1 Outside Window Status Mode.	0x0	R/W
				1	If SYNC_WLIM1 goes high, it latches and pulls $\overline{IRQ}$ low		
				0	SYNC_WLIM1 shows current status		
		0	IRQEN_SMODE_ SYNC_TRIP1		DAC1 Alignment Tripped Status Mode.	0x0	R/W
				1	If SYNC_TRIP1 goes high, it latches and pulls $\overline{IRQ}$ low		
				0	SYNC_TRIP1 shows current status		
0x023	IRQ_STATUS0	7	CALPASS		Calibration Pass Status. If IRQEN_SMODE_CALPASS is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Calibration passed		
		6	CALFAIL		Calibration Fail Detection Status. If IRQEN_SMODE_CALFAIL is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Calibration failed		
		5	DACPLLLOST		DAC PLL Lost Status. If IRQEN_SMODE_DACPLLLOST is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC PLL lock was lost		
		4	DACPLLLOCK		DAC PLL Lock Status. If IRQEN_SMODE_DACPLLLOCK is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC PLL locked		
		3	SERPLLLOST		SERDES PLL Lost Status. If IRQEN_SMODE_SERPLLLOST is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	SERDES PLL lock was lost		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		2	SERPLLLOCK		SERDES PLL Lock Status. If IRQEN_SMODE_SERPLLLOCK is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	SERDES PLL locked		
		1	LANEFIFOERR		Lane FIFO Error Status. If IRQEN_SMODE_LANEFIFOERR is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. A lane FIFO error occurs when there is a full or empty condition on any of the FIFOs between the deserializer block and the core digital. This error requires a link disable and reenable to remove it. The status of the lane FIFOs can be found in Register 0x30C (FIFO full), and Register 0x30D (FIFO empty).	0x0	R
				1	Lane FIFO error		
		0	RESERVED		Reserved.	0x0	R
0x024	IRQ_STATUS1	[7:3]	RESERVED		Reserved.	0x0	R
		2	PRBS1		DAC1 PRBS Error Status. If IRQEN_SMODE_PRBS1 is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC1 failed PRBS		
		1	RESERVED		Reserved.	0x0	R
		0	PRBS0		DAC0 PRBS Error Status. If IRQEN_SMODE_PRBS0 is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC0 failed PRBS		
0x025	IRQ_STATUS2	7	PDPERR0		DAC0 PDP Error. If IRQEN_SMODE_PAERR0 is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Data into DAC0 over power threshold		
		6	RESERVED		Reserved.	0x0	R
		5	BLNKDONE0		DAC0 Blanking Done Status. If IRQEN_SMODE_BLNKDONE0 is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC0 blanking done		
		4	RESERVED		Reserved	0x0	R
		3	SYNC_LOCK0		DAC0 LMFC Alignment Locked Status. If IRQEN_SMODE_SYNC_LOCK0 is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC0 LMFC alignment locked		
		2	SYNC_ROTATE0		DAC0 LMFC Alignment Rotate Status. If IRQEN_SMODE_SYNC_ROTATE0 is low, this bit shows current status. If not, this bit latches on a rising edge and pull IRQ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC0 LMFC alignment rotated		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		1	SYNC_WLIM0		DAC0 Outside Window Status. If IRQEN_SMODE_SYNC_WLIM0 is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC0 LMFC phase outside of window		
		0	SYNC_TRIP0		DAC0 LMFC Alignment Tripped Status. If IRQEN_SMODE_SYNC_TRIP0 is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC0 LMFC alignment tripped		
0x026	IRQ_STATUS3	7	PDPERR1		DAC1 PDP Error. If IRQ_SMODE_PDPERR1 is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	Data into DAC1 over power threshold		
		6	RESERVED		Reserved.	0x0	R
		5	BLNKDONE1		DAC1 Blanking Done Status. If IRQEN_SMODE_BLNKDONE1 is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC1 blanking done		
		4	RESERVED		Reserved.	0x0	R
		3	SYNC_LOCK1		DAC1 LMFC Alignment Locked Status. If IRQEN_SMODE_SYNC_LOCK1 is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC1 LMFC alignment locked		
		2	SYNC_ROTATE1		DAC1 LMFC Alignment Rotate Status. If IRQEN_SMODE_SYNC_ROTATE1 is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC1 LMFC alignment rotated		
		1	SYNC_WLIM1		DAC1 Outside Window Status. If IRQEN_SMODE_SYNC_WLIM1 is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC1 LMFC phase outside of window		
		0	SYNC_TRIP1		DAC1 LMFC Alignment Tripped Status. If IRQEN_SMODE_SYNC_TRIP1 is low, this bit shows current status. If not, this bit latches on a rising edge and pull $\overline{IRQ}$ low. When latched, write a 1 to clear this bit.	0x0	R
				1	DAC1 LMFC alignment tripped		
0x030	JESD_CHECKS	[7:6]	RESERVED		Reserved.	0x0	R
		5	ERR_DLYOVER		Error: LMFC_Delay > JESD_K Parameter.	0x0	R
				1	LMFC_Delay > JESD_K		
		4	ERR_WINLIMIT		Unsupported Window Limit.	0x0	R
				1	Unsupported SYSREF window limit		
		3	ERR_JESDBAD		Unsupported M/L/S/F Selection.	0x0	R
				1	This JESD combination is not supported		
		2	ERR_KUNSUPP		Unsupported K Values. 16 and 32 are supported.	0x0	R
				1	K value unsupported		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		1	ERR_SUBCLASS		Unsupported Subclass Value. 0 and 1 are supported.	0x0	R
				1	Unsupported subclass value		
		0	ERR_INTSUPP		Unsupported Interpolation Rate Factor. 1, 2, 4, 8 are supported.	0x0	R
				1	Unsupported interpolation rate factor		
0x034	SYNC_ERRWINDOW	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	ERRWINDOW		LMFC Sync Error Window. The error window allows the SYSREF sample phase to vary within the confines of the window without triggering a clock adjustment. This is useful if SYSREF cannot be guaranteed to always arrive in the same period of the device clock associated with the target phase. Error window tolerance = ± ERRWINDOW	0x0	R/W
0x038	SYNC_LASTERR_L	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	LASTERROR		LMFC Sync Last Alignment Error. 4-bit twos complement value that represents the phase error (in number of DAC clock cycles) when the clocks were last adjusted.		R
0x039	SYNC_LASTERR_H	7	LASTUNDER		LMFC Sync Last Error Under Flag.	0x0	R
				1	Last phase error was beyond lower window tolerance boundary		
		6	LASTOVER		LMFC Sync Last Error Over Flag.	0x0	R
				1	Last phase error was beyond upper window tolerance boundary		
		[5:0]	RESERVED		Reserved.	0x0	R
0x03A	SYNC_CONTROL	7	SYNCENABLE		LMFC Sync Logic Enable.	0x0	R/W
				1	Enable sync logic		
				0	Disable sync logic		
		6	SYNCARM		LMFC Sync Arming Strobe.	0x0	R/W
				1	Sync one-shot armed		
		5	SYNCCLRSTKY		LMFC Sync Sticky Bit Clear. On a rising edge, this bit clears SYNC_ROTATE and SYNC_TRIP.	0x0	R/W
		4	SYNCCLRLAST		LMFC Sync Clear Last Error. On a rising edge, this bit clears LASTERROR, LASTUNDER, LASTOVER.	0x0	R/W
		[3:0]	SYNCMODE		LMFC Sync Mode.	0x0	R/W
				0b0001	Sync one-shot mode		
				0b0010	Sync continuous mode		
				0b1000	Sync monitor only mode		
				0b1001	Sync one-shot, then monitor		
0x03B	SYNC_STATUS	7	SYNC_BUSY		LMFC Sync Machine Busy.	0x0	R
				1	Sync logic SM is busy		
		[6:4]	RESERVED		Reserved.	0x0	R
		3	SYNC_LOCK		LMFC Sync Alignment Locked.	0x0	R
				1	Sync logic aligned within window		
		2	SYNC_ROTATE		LMFC Sync Rotated.	0x0	R
				1	Sync logic rotated with SYSREF (sticky)		
		1	SYNC_WLIM		LMFC Sync Alignment Limit Range.	0x0	R
				1	Phase error outside window threshold		
		0	SYNC_TRIP		LMFC Sync Tripped After Arming.	0x0	R
				1	Sync received SYSREF pulse (sticky)		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x03C	SYNC_CURRERR_L	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	CURRERROR		LMFC Sync Alignment Error. 4-bit twos complement value that represents the phase error in number of DAC clock cycles (that is, number of DAC clocks between LMFC edge and SYSREF edge). When an adjustment of the clocks is made on any given SYSREF, the value of the phase error is placed into SYNC_ LASTERR, and SYNC_CURRERR is forced to 0.	0x0	R
0x03D	SYNC_CURRERR_H	7	CURRUNDER		LMFC Sync Current Error Under Flag.	0x0	R
				1	Current phase error is beyond lower window tolerance boundary		
		6	CURROVER		LMFC Sync Current Error Over Flag.	0x0	R
				1	Current phase error is beyond upper window tolerance boundary		
		[5:0]	RESERVED		Reserved.	0x0	R
0x040	DACGAIN0_1	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	DACFSC_0[9:8]		2 MSBs of I-Channel DAC Gain DAC0. A 10-bit twos complement value that is mapped to analog full-scale current for DAC0 as shown: 01111111111 = 27.0 mA 0000000000 = 20.48 mA 1000000000 = 13.9 mA	0x0	R/W
0x041	DACGAIN0_0	[7:0]	DACFSC_0[7:0]		8 LSBs of I-Channel DAC Gain DAC0.	0x0	R/W
0x044	DACGAIN1_1	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	DACFSC_1[9:8]		2 MSBs of Q-Channel DAC Gain DAC1. A 10-bit twos complement value that is mapped to analog full-scale current for DAC as shown in Register 0x040. 01111111111 = 27.0 mA 0000000000 = 20.48 mA 1000000000 = 13.9 mA	0x0	R/W
0x045	DACGAIN1_0	[7:0]	DACFSC_1[7:0]		8 LSBs of Q-Channel DAC Gain DAC1.	0x0	R/W
0x080	CLKCFG0	7	PD_CLK0		Power-Down Clock for DAC0. This bit disables the digital and analog clocks for DAC0.	0x1	R/W
		6	PD_CLK1		Power-Down Clock for DAC1. This bit disables the digital and analog clocks for DAC1.	0x1	R/W
		5	PD_CLK_DIG		Power-Down Clocks to all DACs. This bit disables the digital and analog clocks for both duals. This includes all reference clocks, PCLK, DAC clocks, and digital clocks.	0x1	R/W
		4	PD_SERDES_PCLK		Serdes PLL Clock Power-Down. This bit disables the reference clock to the SERDES PLL, which is needed to have an operational serial interface.	0x1	R/W
		3	PD_CLK_REC		Clock Receiver Power-Down. This bit powers down the analog DAC clock receiver block. With this bit set, clocks are not passed to internal nets.	0x1	R/W
		[2:0]	RESERVED		Reserved.	0x0	R

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x081	SYSREF_ACTRL0	[7:5]	RESERVED		Reserved.	0x0	R
		4	PD_SYSREF		Power-Down SYSREF Buffer. This bit powers down the SYSREF receiver. For Subclass 1 operation to work, this buffer must be enabled.	0x1	R/W
		3	HYS_ON		Hysteresis Enabled. This bit enables the programmable hysteresis control for the SYSREF receiver. Using hysteresis gives some noise resistance, but delays the SYSREF± edge an amount depending on HYS_CNTRL and the SYSREF± edge rate. The SYSREF± KOW is not guaranteed when using hysteresis.	0x0	R/W
		2	SYSREF_RISE		Select DAC Clock Edge to Sample SYSREF.	0x0	R/W
				0	Use falling edge of DAC clock to sample SYSREF for alignment		
				1	Use rising edge of DAC clock to sample SYSREF for alignment		
		[1:0]	HYS_CNTRL1		Hysteresis Control Bits[9:8]. HYS_CNTRL is a 10-bit thermometer-coded number. Each bit set adds 10 mV of differential hysteresis to the SYSREF receiver.	0x0	R/W
0x082	SYSREF_ACTRL1	[7:0]	HYS_CNTRL0		Hysteresis Control Bits[7:0].	0x0	R/W
0x083	DACPLLCNTRL	7	RECAL_DACPLL		Recalibrate DAC PLL. On a rising edge of this bit, recalibrate the DAC PLL.	0x0	R/W
		[6:5]	RESERVED		Reserved.	0x0	R
		4	ENABLE_DACPLL		Synthesizer Enable. This bit enables and calibrates the DAC PLL.	0x0	R/W
		[3:0]	RESERVED		Reserved.	0x0	R
0x084	DACPLLSTATUS	7	DACPLL_ OVERRANGE_H		DAC PLL High Overrange. This bit indicates that the DAC PLL hit the upper edge of its operating band. Recalibrate.	0x0	R
		6	DACPLL_ OVERRANGE_L		DAC PLL Low Overrange. This bit indicates that the DAC PLL hit the lower edge of its operating band. Recalibrate.	0x0	R
		5	DACPLL_CAL_ VALID		DAC PLL Calibration Valid. This bit indicates that the DAC PLL has been successfully calibrated.	0x0	R
		[4:2]	RESERVED		Reserved.	0x0	R
		1	DACPLL_LOCK		DAC PLL Lock Bit. This bit is set high by the PLL when it has achieved lock.	0x0	R
		0	RESERVED		Reserved.	0x0	R
0x085	DACINTEGERWORD0	[7:0]	B_COUNT		Integer Division Word. This bit controls the integer feedback divider for the DAC PLL. Determine the frequency of the DAC clock by the following equations (see the Clock Multiplication section for more details): $f_{DAC} = f_{REF}/(REF\_DIVRATE) \times 2 \times B\_COUNT$ $f_{VCO} = f_{REF}/(REF\_DIVRATE) \times 2 \times B\_COUNT \times LO\_DIV\_MODE$ Minimum value is 6.	0x8	R/W
0x087	DACLOOPFILT1	[7:4]	LF_C2_WORD		C2 Control Word. Set this control to 0x6 for optimal performance.	0x8	R/W
		[3:0]	LF_C1_WORD		C1 Control Word. Set this control to 0x2 for optimal performance.	0x8	R/W
0x088	DACLOOPFILT2	[7:4]	LF_R1_WORD		R1 Control Word. Set this control to 0xC for optimal performance.	0x8	R/W
		[3:0]	LF_C3_WORD		C3 Control Word. Set this control to 0x9 for optimal performance.	0x8	R/W

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x089	DACLOOPFILT3	7	LF_BYPASS_R3		Bypass R3 Resistor. When this bit is set, bypass the R3 capacitor (set to 0 pF) when R3_WORD is set to 0. Set this control to 0x0 for optimal performance.	0x0	R/W
		6	LF_BYPASS_R1		Bypass R1 Resistor. When this bit is set, bypass the R1 capacitor (set to 0 pF) when R1_WORD is set to 0. Set this control to 0x0 for optimal performance.	0x0	R/W
		5	LF_BYPASS_C2		Bypass C2 Capacitor. When this bit is set, bypass the C2 capacitor (set to 0 pF) when C2_WORD is set to 0. Set this control to 0x0 for optimal performance.	0x0	R/W
		4	LF_BYPASS_C1		Bypass C1 Capacitor. When this bit is set, bypass the C1 capacitor (set to 0 pF) when C1_WORD is set to 0. Set this control to 0x0 for optimal performance.	0x0	R/W
		[3:0]	LF_R3_WORD		R3 Control Word. Set this control to 0xE for optimal performance.	0x8	R/W
0x08A	DACCPCNTRL	[7:6]	RESERVED		Reserved.	0x0	R
		[5:0]	CP_CURRENT		Charge Pump Current Control. Set this control to 0x12 for optimal performance.	0x20	R/W
0x08B	DACLOGENCNTRL	[7:2]	RESERVED		Reserved.	0x0	R
		[1:0]	LO_DIV_MODE		This range controls the RF clock divider between the VCO and DAC clock rates. The options are 4×, 8×, or 16× division. Choose the LO_DIV_MODE so that 6 GHz < f_{VCO} < 12 GHz (see the Clock Multiplication section for more details):	0x2	R/W
				01	DAC clock = VCO/4		
				10	DAC clock = VCO/8		
				11	DAC clock = VCO/16		
0x08C	DACLDOCNTRL1	[7:3]	RESERVED		Reserved.	0x0	R
		[2:0]	REF_DIV_MODE		Reference Clock Division Ratio. This field controls the amount of division that is done to the input clock at the CLK+/CLK– pins before it is presented to the PLL as a reference clock. The reference clock frequency must be between 35 MHz and 80 MHz, but the CLK+/CLK– input frequency can range from 35 MHz to 1 GHz. The user sets this division to achieve a 35 MHz to 80 MHz PLL reference frequency. For more details see the Clock Multiplication section.	0x1	R/W
				000	1		
				001	2		
				010	4		
				011	8		
				100	16		
0x08D	DACLDOCNTRL2	[7:0]	DAC_LDO		DAC PLL LDO setting. This register must be written to 0x7B for optimal performance.	0x2B	R/W
0x0E2	CAL_CTRL_GLOBAL	[7:2]	RESERVED		Reserved.	0x0	R
		1	CAL_START_AVG		Averaged Calibration Start. On rising edge, calibrate the DACs. Only use if calibrating all DACs.	0x0	R/W
		0	CAL_EN_AVG		Averaged Calibration Enable. Set prior to starting calibration with CAL_START_AVG. While this bit is set, calibration can be performed, and the results are applied.	0x0	R/W
				1	Enable averaged calibration		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x0E7	CAL_CLKDIV	[7:4]	RESERVED		Must write the default value for proper operation.	0x3	R/W
		3	CAL_CLK_EN		Enable Self Calibration Clock.	0x0	R/W
				1	Enable calibration clock		
				0	Disable calibration clock		
		[2:0]	RESERVED		Reserved.	0x0	R
0x0E8	CAL_PAGE	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	CAL_PAGE		DAC Calibration Paging. Selects which of the DACs are being accessed for calibration or calibration readback. This paging affects Register 0x0E9 and Register 0x0ED. Calibration: any number of DACs can be accessed simultaneously to write and calibrate. Write a 1 to Bit 0 to include DAC0. Write a 1 to Bit 2 to include DAC1. Readback: only one DAC at a time can be accessed when reading back CAL_CTRL (Register 0x0E9). Write a 1 to Bit 0 to read from DAC0 or write a 1 to Bit 2 to read from DAC1 (the other bits must be 0).	0xF	R/W
0x0E9	CAL_CTRL	7	CAL_FIN		Calibration finished. This bit is high when the calibration has completed. If the calibration completes and either CAL_ERRHI or CAL_ERRLO is high, then the calibration cannot be considered valid and are considered a timeout event.	0x0	R
				1	Calibration ran and is finished		
		6	CAL_ACTIVE		Calibration Active. This bit is high while the calibration is in progress.	0x0	R
				1	Calibration is running		
		5	CAL_ERRHI		SAR Data Error: Too High. This bit is set at the end of a calibration cycle if any of the calibration DACs has overranged to the high side. This typically means that the algorithm adjusts the calibration preset of the calibration DACs and runs another cycle.	0x0	R
				1	Data saturated high		
		4	CAL_ERRLO		SAR Data Error: Too Low. This bit is set at the end of a calibration cycle if any of the calibration DACs has overranged to the low side. This typically means that the algorithm adjusts the calibration preset of the calibration DACs and runs another cycle.	0x0	R
				1	Data saturated low		
		[3:2]	RESERVED		Reserved.	0x0	R
		1	CAL_START		Calibration Start. The rising edge of this bit kicks off a calibration sequence for the DACs that have been selected in the CAL_INDX register.	0x0	R/W
				0	Normal operation		
				1	Start calibration state machine		
		0	CAL_EN		Calibration Enable. Enable the calibration DAC of the converter. Enable to calibration engine and machines. Prepare for a calibration start. For calibration coefficients to be applied to the calibrated DACs, this bit must be high.	0x0	R/W
				0	Do not use calibration DACs		
				1	Use calibration DACs		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x0ED	CAL_INIT	[7:0]	CAL_INIT		Initialize Calibration. Must be written to 0xA2 before starting calibration or averaged calibration.	0xA6	R/W
0x110	DATA_FORMAT	7	BINARY_FORMAT		Binary or Twos Complementary Format on the Data Bus.	0x0	R/W
				0	Input data is twos complement		
				1	Input data is offset binary		
		[6:0]	RESERVED		Reserved.	0x0	R
0x111	DATAPATH_CTRL	7	INVSINC_ENABLE		Enable Inverse Sinc Filter.	0x1	R/W
				1	Enable inverse sinc filter		
				0	Disable inverse sinc filter		
		6	RESERVED		Reserved.	0x0	R
		5	DIG_GAIN_ENABLE		Enable Digital Gain.	0x1	R/W
				1	Enable digital gain function		
				0	Disable digital gain function		
		[4:0]	RESERVED		Reserved	0x0	R
0x112	INTERP_MODE	[7:3]	RESERVED		Reserved.	0x0	R
		[2:0]	INTERP_MODE		Interpolation Mode.	0x1	R/W
				000	1× mode		
				001	2× mode		
				011	4× mode		
				100	8× mode		
0x11F	TXEN_SM_0	[7:6]	FALL_COUNTERS		Fall Counters. The number of counters to use to delay TX_PROTECT fall from TXENx falling edge. Must be set to 1 or 2.	0x2	R/W
		[5:4]	RISE_COUNTERS		Rise Counters. The number of counters to use to delay TX_PROTECT rise from TXENx rising edge.	0x0	R/W
		3	RESERVED		Reserved.	0x0	R
		2	PROTECT_OUT_ INVERT		PROTECT_OUTx Invert.	0x0	R/W
				0	PROTECT_OUTx is high when output is valid. Suitable for enabling downstream components during transmission		
				1	PROTECT_OUTx is high when output is invalid. Suitable for disabling downstream components when not transmitting		
		[1:0]	RESERVED		Must write the default value for proper operation.	0x3	R/W
0x121	TXEN_RISE_COUNT_0	[7:0]	RISE_COUNT_0		First counter used to delay TX_PROTECT rise from TXENx rising edge. Delays by 32 × RISE_COUNT_0 DAC clock cycles.	0xF	R/W
0x122	TXEN_RISE_COUNT_1	[7:0]	RISE_COUNT_1		Second counter used to delay TX_PROTECT rise from TXENx rising edge. Delays by 32 × RISE_COUNT_1 DAC clock cycles.	0x0	R/W
0x123	TXEN_FALL_ COUNT_0	[7:0]	FALL_COUNT_0		First counter used to delay TX_PROTECT fall from TXENx falling edge. Delays by 32 × FALL_COUNT_0 DAC clock cycles. Must be set to a minimum of 0x12.	0xFF	R/W
0x124	TXEN_FALL_ COUNT_1	[7:0]	FALL_COUNT_1		Second counter used to delay TX_PROTECT fall from TXENx falling edge. Delays by 32 × FALL_COUNT_1 DAC clock cycles.	0xFF	R/W
0x12D	DEVICE_CONFIG_ REG_0	[7:0]	DEVICE_CONFIG_0		Must be set to 0x8B for proper digital datapath configuration.	0x46	R/W
0x12F	DIE_TEMP_CTRL0	[7:1]	RESERVED		Must write the default value for proper operation.	0x10	R/W
		0	AUXADC_ENABLE		Enables the AUX ADC Block.	0x0	R/W
				0	AUX ADC disable		
				1	AUX ADC enable		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x132	DIE_TEMP0	[7:0]	DIE_TEMP[7:0]		Aux ADC Readback Value.	0x0	R
0x133	DIE_TEMP1	[7:0]	DIE_TEMP[15:8]		Aux ADC Readback Value.	0x0	R
0x134	DIE_TEMP_UPDATE	[7:1]	RESERVED		Reserved.	0x0	R
		0	DIE_TEMP_ UPDATE		Die Temperature Update. On a rising edge, a new temperature code is generated.	0x0	R/W
0x135	DC_OFFSET_CTRL	[7:1]	RESERVED		Reserved.	0x0	R
		0	DC_OFFSET_ON		DC Offset On.	0x0	R/W
				1	Enables dc offset module		
0x136	DAC_DC_OFFSET_1 PART0	[7:0]	LSB_OFFSET[7:0]		8 LSBs of DC Offset. LSB_OFFSET is a 16-bit twos complement number that is added to incoming data. Applies to the DAC selected by DAC_PAGE (Register 0x008 [1:0]).	0x0	R/W
0x137	DAC_DC_OFFSET_ 1PART1	[7:0]	LSB_OFFSET[15:8]		8 MSBs of DC Offset. LSB_OFFSET is a 16-bit twos complement number that is added to incoming data. Applies to the DAC selected by DAC_PAGE (Register 0x008 [1:0]).	0x0	R/W
0x13A	DAC_DC_OFFSET_ 2PART	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	SIXTEENTH_ OFFSET		SIXTEENTH_OFFSET is a 5-bit twos complement number in 16ths of an LSB that is added to incoming I data.	0x0	R/W
				x	x/16 LSB DC offset		
0x13C	DAC_DIG_GAIN0	[7:0]	DAC_DIG_ GAIN[7:0]		8 LSBs of DAC Digital Gain. DAC_DIG_GAIN is the digital gain of the DAC selected by DAC_PAGE (Register 0x008 [1:0]). The digital gain is a multiplier from 0 to 4095/2048 in steps of 1/2048.	0xEA	R/W
0x13D	DAC_DIG_GAIN1	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	DAC_DIG_ GAIN[11:8]		4 MSBs of DAC Digital Gain	0xA	R/W
0x140	GAIN_RAMP_UP_ STEP0	[7:0]	GAIN_RAMP_UP_ STEP[7:0]		8 LSBs of Gain Ramp Up Step. GAIN_RAMP_UP_STEP controls the amplitude step size of the BSM's ramping feature when the gain is being ramped to its assigned value.	0x4	R/W
				0x0	Smallest ramp up step size		
				0xFFF	Largest ramp up step size		
0x141	GAIN_RAMP_UP_ STEP1	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	GAIN_RAMP_UP_ STEP[11:8]		4 MSBs of Gain Ramp Up Step. See Register 0x140 for description.	0x0	R/W
0x142	GAIN_RAMP_DOWN_ STEP0	[7:0]	GAIN_RAMP_ DOWN_STEP[7:0]		8 LSBs of Gain Ramp Down Step. GAIN_RAMP_DOWN_STEP controls the amplitude step size of the BSM's ramping feature when the gain is being ramped to zero.	0x9	R/W
				0	Smallest ramp down step size		
				0xFFF	Largest ramp down step size		
0x143	GAIN_RAMP_ DOWN_STEP1	[7:4]	RESERVED		Reserved.	0x0	R
		[3:0]	GAIN_RAMP_ DOWN_STEP[11:8]		4 MSBs of Gain Ramp Down Step. See Register 0x142 for description.	0x0	R/W
0x146	DEVICE_CONFIG_ REG_1	[7:0]	DEVICE_CONFIG_1		Must be set to 0x01 for proper digital datapath configuration.	0x0	R/W
0x147	BSM_STAT	[7:6]	SOFTBLANKRB		Blanking State.	0x0	R
				00	Data is fully blanked		
				01	Ramping from data process to full blanking		
				10	Ramping from fully blanked to data process		
				11	Data is being processed		
		[5:0]	RESERVED		Reserved.	0x0	R

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x14B	PRBS	7	RESERVED		Reserved.	0x0	R
		6	PRBS_GOOD		Good Data Indicator.	0x0	R
				0	Incorrect sequence detected		
				1	Correct PRBS sequence detected		
		[5:3]	RESERVED		Reserved.	0x0	R
		2	PRBS_MODE		Polynomial Select	0x0	R/W
				0	7-bit: $x^7 + x^6 + 1$		
				1	15-bit: $x^{15} + x^{14} + 1$		
		1	PRBS_RESET		Reset Error Counters.	0x0	R/W
				0	Normal operation		
				1	Reset counters		
		0	PRBS_EN		Enable PRBS Checker.	0x0	R/W
				0	Disable		
				1	Enable		
0x14C	PRBS_ERROR	[7:0]	PRBS_COUNT		Error Count Value.	0x0	R
0x1B0	DACPLLT0	[7:0]	DAC_PLL_PWR		DAC PLL PD settings. This register must be written to 0x00 for optimal performance.	0xFA	R/W
0x1B5	DACPLLT5	[7:4]	RESERVED		Must write the default value for proper operation.	0x8	R/W
		[3:0]	VCO_VAR		Varactor KVO Setting. See Table 73 for optimal settings based on the f_{VCO} being used.	0x3	R/W
0x1B9	DACPLLT9	[7:0]	DAC_PLL_CP1		DAC PLL Charge Pump settings. This register must be written to 0x24 for optimal performance.	0x34	R/W
0x1BB	DACPLLTB	[7:5]	RESERVED		Reserved.	0x0	R
		[4:3]	VCO_BIAS_TCF		Temperature Coefficient for VCO Bias. See Table 73 for optimal settings based on the f_{VCO} being used.	0x1	R/W
		[2:0]	VCO_BIAS_REF		VCO Bias Control. See Table 73 for optimal settings based on the f_{VCO} being used.	0x4	R/W
0x1BC	DACPLLTC	[7:0]	DAC_PLL_VCO_ CTRL		DAC PLL VCO control settings. This register must be written to 0x0D for optimal performance.	0x00	R/W
0x1BE	DACPLLTE	[7:0]	DAC_PLL_VCO_ PWR		DAC PLL VCO power control settings. This register must be written to 0x02 for optimal performance.	0x00	R/W
0x1BF	DACPLLTF	[7:0]	DAC_PLL_VCOCAL		DAC PLL VCO calibration settings. This register must be written to 0x8E for optimal performance.	0x8D	R/W
0x1C0	DACPLLT10	[7:0]	DAC_PLL_LOCK_ CNTR		This register must be written to 0x2A for optimal performance.	0x2E	R/W
0x1C1	DACPLLT11	[7:0]	DAC_PLL_CP2		This register must be written to0x2A for optimal performance.	0x24	R/W
0x1C4	DACPLLT17	[7:0]	DAC_PLL_VAR1		DAC PLL Varactor setting. Must be set to 0x7E for proper DAC PLL configuration.	0x33	R/W
0x1C5	DACPLLT18	[7:0]	DAC_PLL_VAR2		DAC PLL Varactor setting. See Table 73 for optimal settings based on the f_{VCO} being used.	0x08	R/W
0x200	MASTER_PD	[7:1]	RESERVED		Reserved.	0x0	R
		0	SPI_PD_MASTER		Power Down the Entire JESD Receiver Analog (All Eight Channels Plus Bias).	0x1	R/W
0x201	PHY_PD	[7:0]	SPI_PD_PHY		SPI Override to Power Down the Individual PHYs. Set Bit x to power down the corresponding SERDINx± PHY	0x0	R/W

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x203	GENERIC_PD	[7:2]	RESERVED		Reserved.	0x0	R
		1	SPI_SYNC1_PD		Power down LVDS buffer for $\overline{\text{SYNCOUT0}}$±.	0x0	R/W
		0	SPI_SYNC2_PD		Power down LVDS buffer for $\overline{\text{SYNCOUT1}}$±.	0x0	R/W
0x206	CDR_RESET	[7:1]	RESERVED		Reserved.	0x0	R
		0	SPI_CDR_RESETN		Resets the Digital Control Logic for All PHYs.	0x1	R/W
				0	Hold CDR in reset		
				1	Enable CDR		
0x230	CDR_OPERATING_ MODE_REG_0	[7:6]	RESERVED		Reserved.	0x0	R
		5	ENHALFRATE		Enables Half-Rate CDR Operation. Set to 1 when 5.75 Gbps ≤ lane rate ≤ 12.4 Gbps.	0x1	R/W
		[4:2]	RESERVED		Must write the default value for proper operation.	0x2	R/W
		1	CDR_OVERSAMP		Enables Oversampling of the Input Data. Set to 1 when 1.44 Gbps ≤ lane rate ≤ 3.1 Gbps.	0x0	R/W
		0	RESERVED		Reserved.	0x0	R
0x232	DEVICE_CONFIG_ REG_3	[7:0]	DEVICE_CONFIG_3		Must be set to 0xFF for proper JESD interface configuration.	0x0	R/W
0x268	EQ_BIAS_REG	[7:6]	EQ_POWER_ MODE		Control the Equalizer Power/Insertion Loss Capability.	0x1	R/W
				00	Normal mode		
				01	Low power mode		
		[5:0]	RESERVED		Must write the default value for proper operation.	0x22	R/W
0x280	SERDESPLL_ ENABLE_CNTRL	[7:3]	RESERVED		Reserved.	0x0	R
		2	RECAL_SERDESPLL		Recalibrate SERDES PLL. On a rising edge, recalibrate the SERDES PLL.	0x0	R/W
		1	RESERVED		Reserved.	0x0	R
		0	ENABLE_ SERDESPLL		Enable the SERDES PLL. Setting this bit enables and calibrates the SERDES PLL.	0x0	R/W
0x281	PLL_STATUS	[7:6]	RESERVED		Reserved.	0x0	R
		5	SERDES_PLL_ OVERRANGE_H		SERDES PLL High Overrange. This bit indicates that the SERDES PLL hit the lower edge of its operating band. Recalibrate.	0x0	R
		4	SERDES_PLL_ OVERRANGE_L		SERDES PLL Low Overrange. This bit indicates that the SERDES PLL hit the lower edge of its operating band. Recalibrate.	0x0	R
		3	SERDES_PLL_CAL_ VALID_RB		SERDES PLL Calibration Valid. This bit indicates that the SERDES PLL has been successfully calibrated.	0x0	R
		[2:1]	RESERVED		Reserved.	0x0	R
		0	SERDES_PLL_ LOCK_RB		SERDES PLL Lock. This bit is set high by the PLL when it has achieved lock.	0x0	R
0x284	LOOP_FILTER_1	[7:0]	LOOP_FILTER_1		SERDES PLL loop filter setting. This register must be written to 0x62 for optimal performance.	0x77	R/W
0x285	LOOP_FILTER_2	[7:0]	LOOP_FILTER_2		SERDES PLL loop filter setting. This register must be written to 0xC9 for optimal performance.	0x87	R/W
0x286	LOOP_FILTER_3	[7:0]	LOOP_FILTER_3		SERDES PLL loop filter setting. This register must be written to 0x0E for optimal performance.	0x08	R/W
0x287	SERDES_PLL_CP1	[7:0]	SERDES_PLL_CP1		SERDES PLL charge pump setting. This register must be written to 0x12 for optimal performance.	0x3F	R/W

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x289	REF_CLK_DIVIDER_LDO	[7:3]	RESERVED		Reserved.	0x0	R
		2	DEVICE_CONFIG_4		Must be set to 1 for proper SERDES PLL configuration.	0x0	R/W
		[1:0]	SERDES_PLL_DIV_MODE		SERDES PLL Reference Clock Division Factor. This field controls the division of the SERDES PLL reference clock before it is fed into the SERDES PLL Phase Frequency Detector (PFD). It must be set so f_{REF}/DivFactor is between 35 MHz and 80 MHz.	0x0	R/W
				00	Divide by 4 for 5.75 Gbps to 12.4 Gbps lane rate		
				01	Divide by 2 for 2.88 Gbps to 6.2 Gbps lane rate		
				10	Divide by 1 for 1.44 Gbps to 3.1 Gbps lane rate		
0x28A	VCO_LDO	[7:0]	SERDES_PLL_VCO_LDO		SERDES PLL VCO LDO setting. This register must be written to 0x7B for optimal performance.	0x2B	R/W
0x28B	SERDES_PLL_PD1	[7:0]	SERDES_PLL_PD1		SERDES PLL PD setting. This register must be written to 0x00 for optimal performance.	0x7F	R/W
0x290	SERDESPLL_VAR1	[7:0]	SERDES_PLL_VAR1		SERDES PLL Varactor setting. This register must be written to 0x89 for optimal performance.	0x83	R/W
0x294	SERDES_PLL_CP2	[7:0]	SERDES_PLL_CP2		SERDES PLL Charge Pump setting. This register must be set to 0x24 for optimal performance.	0xB0	R/W
0x296	SERDESPLL_VCO1	[7:0]	SERDES_PLL_VCO1		SERDES PLL VCO setting. This register must be set to 0x03 for optimal performance.	0x0C	R/W
0x297	SERDESPLL_VCO2	[7:0]	SERDES_PLL_VCO2		SERDES PLL VCO setting. This register must be set to 0x0D for optimal performance.	0x00	R/W
0x299	SERDES_PLL_PD2	[7:0]	SERDES_PLL_PD2		SERDES PLL PD setting. This register must be set to 0x02 for optimal performance.	0x00	R/W
0x29A	SERDESPLL_VAR2	[7:0]	SERDES_PLL_VAR2		SERDES PLL Varactor setting. This register must be set to 0x8E for optimal performance.	0xFE	R/W
0x29C	SERDES_PLL_CP3	[7:0]	SERDES_PLL_CP3		SERDES PLL Charge Pump setting. Must be set to 0x2A for proper SERDES PLL configuration.	0x17	R/W
0x29F	SERDESPLL_VAR3	[7:0]	SERDES_PLL_VAR3		SERDES PLL Varactor setting. Must be set to 0x78 for proper SERDES PLL configuration.	0x33	R/W
0x2A0	SERDESPLL_VAR4	[7:0]	SERDES_PLL_VAR4		SERDES PLL Varactor setting. This register must be set to 0x06 for optimal performance.	0x08	R/W
0x2A4	DEVICE_CONFIG_REG_8	[7:0]	DEVICE_CONFIG_8		Must be set to 0xFF for proper clock configuration.	0x4B	R/W
0x2A5	SYNCOUTB_SWING	[7:1]	RESERVED		Reserved.	0x0	R
		0	SYNCOUTB_SWING_MD		$\overline{\text{SYNCOUTx}}\pm$ Swing Mode. Sets the output differential swing mode for the $\overline{\text{SYNCOUTx}}\pm$ pins. See Table 8 for details.	0x0	R/W
				0	Normal Swing Mode		
				1	High Swing Mode		
0x2A7	TERM_BLK1_CTRLREG0	[7:1]	RESERVED		Reserved.	0x0	R
		0	RCAL_TERMBLK1		Termination Calibration. The rising edge of this bit calibrates PHY0, PHY1, PHY6, and PHY7 terminations to 50 Ω.	0x0	R/W
0x2AA	DEVICE_CONFIG_REG_9	[7:0]	DEVICE_CONFIG_9		Must be set to 0xB7 for proper JESD interface termination configuration.	0xC3	R/W
0x2AB	DEVICE_CONFIG_REG_10	[7:0]	DEVICE_CONFIG_10		Must be set to 0x87 for proper JESD interface termination configuration.	0x93	R/W

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x2AE	TERM_BLK2_ CTRLREG0	[7:1]	RESERVED		Reserved.	0x0	R
		0	RCAL_TERMBLK2		Terminal Calibration. The rising edge of this bit calibrates PHY2, PHY3, PHY4 and PHY5 terminations to 50 Ω.	0x0	R/W
0x2B1	DEVICE_CONFIG_ REG_11	[7:0]	DEVICE_CONFIG_ 11		Must be set to 0xB7 for proper JESD interface termination configuration.	0xC3	R/W
0x2B2	DEVICE_CONFIG_ REG_12	[7:0]	DEVICE_CONFIG_ 12		Must be set to 0x87 for proper JESD interface termination configuration.	0x93	R/W
0x300	GENERAL_JRX_ CTRL_0	7	RESERVED		Reserved.	0x0	R
		6	CHECKSUM_MODE		Checksum Mode. This bit controls the locally generated JESD204B link parameter checksum method. The value is stored in the FCMP registers (Register 0x40E, Register 0x416, Register 0x41E, Register 0x426, Register 0x42E, Register 0x436, Register 0x43E, and Register 0x446).	0x0	R/W
				0	Checksum is calculated by summing the individual fields in the link configuration table as defined in Section 8.3, Table 20 of the JESD204B standard		
				1	Checksum is calculated by summing the registers containing the packed link configuration fields (Σ[0x400:0x40A] modulo 256).		
		[5:4]	RESERVED		Reserved.	0x0	R
		3	LINK_MODE		Link Mode. This register selects either single-link or dual-link mode.	0x0	R/W
				0	Single-link mode		
				1	Dual-link mode		
		2	LINK_PAGE		Link Paging. Selects which link's register map is used. This paging affects Registers 0x401 to 0x47E.	0x0	R/W
				0	Use Link 0 register map		
				1	Use Link 1 register map		
		[1:0]	LINK_EN		Link Enable. These bits bring up the JESD204B receiver digital circuitry: Bit 0 for Link 0 and Bit 1 for Link 1. Enable the link only after the following has occurred: all JESD204B parameters are set, the DAC PLL is enabled and locked (Register 0x084[1] = 1), and the JESD204B PHY is enabled (Register 0x200 = 0x00) and calibrated (Register 0x281[2] = 0).	0x0	R/W
				0b00	Disable both JESD Link 1 and JESD Link 0		
				0b01	Disable JESD Link 1, enable JESD Link 0		
				0b10	Enable JESD Link 1, disable JESD Link 0		
				0b11	Enable both JESD Link 1 and JESD Link 0		
0x301	GENERAL_JRX_CTRL_1	[7:3]	RESERVED		Reserved.	0x0	R
		[2:0]	SUBCLASSV_ LOCAL		JESD204B Subclass.	0x1	R/W
				000	Subclass 0		
				001	Subclass 1		
0x302	DYN_LINK_LATENCY_0	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	DYN_LINK_ LATENCY_0		Dynamic Link Latency: Link 0. Latency between the $LMFC_{Rx}$ for Link 0 and the last arriving LMFC boundary in units of PCLK cycles. See the Deterministic Latency section.	0x0	R
0x303	DYN_LINK_LATENCY_1	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	DYN_LINK_ LATENCY_1		Dynamic Link Latency: Link 1. Latency between the $LMFC_{Rx}$ for Link 1 and the last arriving LMFC boundary in units of PCLK cycles. See the Deterministic Latency section.	0x0	R

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x304	LMFC_DELAY_0	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LMFC_DELAY_0		LMFC Delay: Link 0 Delay from the LMFC to $LMFC_{Rx}$ for Link 0. In units of frame clock cycles for subclass 1 and PCLK cycles for subclass 0. See the Deterministic Latency section.	0x0	R/W
0x305	LMFC_DELAY_1	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LMFC_DELAY_1		LMFC Delay: Link 1. Delay from the LMFC to $LMFC_{Rx}$ for Link 1. In units of frame clock cycles for subclass 1 and PCLK cycles for subclass 0. See the Deterministic Latency section.	0x0	R/W
0x306	LMFC_VAR_0	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LMFC_VAR_0		Variable Delay Buffer: Link 0. Sets when data is read from a buffer to be consistent across links and power cycles. In units of PCLK cycles. See the Deterministic Latency section. This setting must not be more than 10.	0x6	R/W
0x307	LMFC_VAR_1	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LMFC_VAR_1		Variable Delay Buffer: Link 1. Sets when data is read from a buffer to be consistent across links and power cycles. In units of PCLK cycles. See the Deterministic Latency section. This setting must not be more than 10.	0x6	R/W
0x308	XBAR_LN_0_1	[7:6]	RESERVED		Reserved.	0x0	R
		[5:3]	LOGICAL_LANE1_SRC		Logical Lane 1 Source. Selects a physical lane to be mapped onto Logical Lane 1.	0x1	R/W
				x	Data is from SERDINx		
		[2:0]	LOGICAL_LANE0_SRC		Logical Lane 0 Source. Selects a physical lane to be mapped onto Logical Lane 0.	0x0	R/W
				x	Data is from SERDINx		
0x309	XBAR_LN_2_3	[7:6]	RESERVED		Reserved.	0x0	R
		[5:3]	LOGICAL_LANE3_SRC		Logical Lane 3 Source. Selects a physical lane to be mapped onto Logical Lane 3.	0x3	R/W
				x	Data is from SERDINx		
		[2:0]	LOGICAL_LANE2_SRC		Logical Lane 2 source. Selects a physical lane to be mapped onto Logical Lane 2.	0x2	R/W
				x	Data is from SERDINx		
0x30A	XBAR_LN_4_5	[7:6]	RESERVED		Reserved.	0x0	R
		[5:3]	LOGICAL_LANE5_SRC		Logical Lane 5 Source. Selects a physical lane to be mapped onto Logical Lane 5.	0x5	R/W
				x	Data is from SERDINx		
		[2:0]	LOGICAL_LANE4_SRC		Logical Lane 4 Source. Selects a physical lane to be mapped onto Logical Lane 4.	0x4	R/W
				x	Data is from SERDINx		
0x30B	XBAR_LN_6_7	[7:6]	RESERVED		Reserved.	0x0	R
		[5:3]	LOGICAL_LANE7_SRC		Logical Lane 7 Source. Selects a physical lane to be mapped onto Logical Lane 7.	0x7	R/W
				x	Data is from SERDINx		
		[2:0]	LOGICAL_LANE6_SRC		Logical Lane 6 Source. Selects a physical lane to be mapped onto Logical Lane 6.	0x6	R/W
				x	Data is from SERDINx		
0x30C	FIFO_STATUS_REG_0	[7:0]	LANE_FIFO_FULL		FIFO Full Flags for Each Logical Lane. A full FIFO indicates an error in the JESD204B configuration or with a system clock. If the FIFO for Lane x is full, Bit x in this register will be high.	0x0	R

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x30D	FIFO_STATUS_REG_1	[7:0]	LANE_FIFO_EMPTY		FIFO Empty Flags for Each Logical Lane. An empty FIFO indicates an error in the JESD204B configuration or with a system clock. If the FIFO for Logical Lane x is empty, Bit x in this register will be high.	0x0	R
0x312	SYNCB_GEN_1	[7:6]	RESERVED		Reserved.	0x0	R/W
		[5:4]	SYNCB_ERR_DUR		Duration of $\overline{\text{SYNCOUTx}}$± Low for Error. The duration applies to both $\overline{\text{SYNCOUT0}}$ and $\overline{\text{SYNCOUT1}}$. A sync error is asserted at the end of a multiframe whenever one or more disparity, not in table or unexpected control character errors are encountered.		
				0	½ PCLK cycle		
				1	1 PCLK cycle		
				2	2 PCLK cycles		
		[3:0]	RESERVED		Reserved.	0x0	R/W
0x314	SERDES_SPI_REG	[7:0]	SERDES_SPI_ CONFIG		SERDES SPI Configuration. Must be written to 0x01 as part of the Physical Layer setup step.	0x0	R/W
0x315	PHY_PRBS_TEST_EN	[7:0]	PHY_TEST_EN		PHY Test Enable. Enables the PHY BER test. Set Bit x to enable the PHY test for Lane x.	0x0	R/W
0x316	PHY_PRBS_TEST_CTRL	7	RESERVED		Reserved.	0x0	R
		[6:4]	PHY_SRC_ERR_CNT		PHY Error Count Source. Selects which PHY errors are being reported in Register 0x31A to Register 0x31C.	0x0	R/W
				x	Report Lane x error count		
		[3:2]	PHY_PRBS_PAT_SEL		PHY PRBS Pattern Select. Selects the PRBS pattern for PHY BER test.	0x0	R/W
				00	PRBS7		
				01	PRBS15		
				10	PRBS31		
		1	PHY_TEST_START		PHY PRBS Test Start. Starts and stops the PHY PRBS test.	0x0	R/W
				0	Test stopped		
				1	Test in progress		
		0	PHY_TEST_RESET		PHY PRBS Test Reset. Resets the PHY PRBS test state machine and error counters.	0x0	R/W
				0	Enable PHY PRBS test state machine		
				1	Hold PHY PRBS test state machine in reset		
0x317	PHY_PRBS_TEST_ THRESHOLD_LOBITS	[7:0]	PHY_PRBS_ THRESHOLD[7:0]		8 LSBs of PHY PRBS Error Threshold.	0x0	R/W
0x318	PHY_PRBS_TEST_ THRESHOLD_ MIDBITS	[7:0]	PHY_PRBS_ THRESHOLD[15:8]		8 ISBs of PHY PRBS Error Threshold.	0x0	R/W
0x319	PHY_PRBS_TEST_ THRESHOLD_HIBITS	[7:0]	PHY_PRBS_ THRESHOLD[23:16]		8 MSBs of PHY PRBS Error Threshold.	0x0	R/W
0x31A	PHY_PRBS_TEST_ ERRCNT_LOBITS	[7:0]	PHY_PRBS_ERR_ CNT[7:0]		8 LSBs of PHY PRBS Error Count. Reported PHY BERT error count from lane selected using Register 0x316[6:4].	0x0	R
0x31B	PHY_PRBS_TEST_ ERRCNT_MIDBITS	[7:0]	PHY_PRBS_ERR_ CNT[15:8]		8 ISBs of PHY PRBS Error Count.	0x0	R
0x31C	PHY_PRBS_TEST_ ERRCNT_HIBITS	[7:0]	PHY_PRBS_ERR_ CNT[23:16]		8 MSBs of PHY PRBS Error Count.	0x0	R
0x31D	PHY_PRBS_TEST_ STATUS	[7:0]	PHY_PRBS_PASS		PHY PRBS Test Pass/Fail. Bit x corresponds to PHY PRBS pass/fail for Physical Lane x. The bit is set to 1 while the error count for Physical Lane x is less than PHY_PRBS_THRESHOLD.	0xFF	R

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x32C	SHORT_TPL_TEST_0	[7:6]	RESERVED		Reserved.	0x0	R
		[5:4]	SHORT_TPL_SP_SEL		Short Transport Layer Sample Select. Selects which sample to check from the DAC selected via Bits[3:2].	0x0	R/W
				x	Sample x		
		[3:2]	SHORT_TPL_DAC_SEL		Short Transport Layer Test DAC Select. Selects which DAC to sample.	0x0	R/W
				0	Sample from DAC0		
				2	Sample from DAC1		
		1	SHORT_TPL_TEST_RESET		Short Transport Layer Test Reset. Resets the result of short transport layer test.	0x0	R/W
				0	Not reset		
				1	Reset		
		0	SHORT_TPL_TEST_EN		Short Transport Layer Test Enable. See the Subclass 0 section for details on how to perform this test.	0x0	R/W
				0	Disable		
				1	Enable		
0x32D	SHORT_TPL_TEST_1	[7:0]	SHORT_TPL_REF_SP_LSB		Short Transport Layer Test Reference, Sample LSB. This is the lower eight bits of the expected DAC sample. It is used to compare with the received DAC sample at the output of the JESD204B receiver.	0x0	R/W
0x32E	SHORT_TPL_TEST_2	[7:0]	SHORT_TPL_REF_SP_MSB		Short Transport Layer Test Reference, Sample MSB. This is the upper eight bits of the expected DAC sample. It is used to compare with the received DAC sample at the output of the JESD204B receiver.	0x0	R/W
0x32F	SHORT_TPL_TEST_3	[7:1]	RESERVED		Reserved.	0x0	R
		0	SHORT_TPL_FAIL		Short Transport Layer Test Fail. This bit shows whether the selected DAC sample matches the reference sample. If they match, it is a test pass, otherwise it is a test fail.	0x0	R
				0	Test pass		
				1	Test fail		
0x333	DEVICE_CONFIG_REG_13	[7:0]	DEVICE_CONFIG_13		Must be set to 0x01 for proper JESD interface configuration.	00	R/W
0x334	JESD_BIT_INVERSE_CTRL	[7:0]	JESD_BIT_INVERSE		Logical Lane Invert. Set Bit x high to invert the JESD deserialized data on Logical Lane x.	0x0	R/W
0x400	DID_REG	[7:0]	DID_RD		Device Identification Number. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x401	BID_REG	[7:4]	ADJCNT_RD		Adjustment Resolution to DAC LMFC. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B. Must be 0.	0x0	R
		[3:0]	BID_RD		Bank Identification: Extension to DID. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x402	LID0_REG	7	RESERVED		Reserved.	0x0	R
		6	ADJDIR_RD		Direction to Adjust DAC LMFC. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B. Must be 0.	0x0	R
		5	PHADJ_RD		Phase Adjustment Request to DAC Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B. Must be 0.	0x0	R
		[4:0]	LID0_RD		Lane Identification for Lane 0. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x403	SCR_L_REG	7	SCR_RD		Transmit Scrambling Status. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
				0	Scrambling is disabled		
				1	Scrambling is enabled		
		[6:5]	RESERVED		Reserved.	0x0	R
		[4:0]	L-1_RD		Number of Lanes per Converter Device. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
				0	One lane per converter		
				1	Two lanes per converter		
				3	Four lanes per converter		
				7	Eight lanes per converter (single link only)		
0x404	F_REG	[7:0]	F-1_RD		Number of Octets per Frame. Settings of 1, 2 and 4 octets per frame are valid. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
				0	(One octet per frame) per lane		
				1	(Two octets per frame) per lane		
				3	(Four octets per frame) per lane		
0x405	K_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	K-1_RD		Number of Frames per Multiframe. Settings of 16 or 32 are valid. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
				0x0F	16 frames per multiframe		
				0x1F	32 frames per multiframe		
0x406	M_REG	[7:0]	M-1_RD		Number of converters per device. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B. Must be 0 or 1.	0x0	R
				0	One converter per device		
				1	Two converters per device		
0x407	CS_N_REG	[7:6]	CS_RD		Number of Control Bits per Sample. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B. CS must be 0.	0x0	R
		5	RESERVED		Reserved.	0x0	R
		[4:0]	N-1_RD		Converter Resolution. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B. Converter resolution must be 16.	0x0	R
				0x0F	Converter resolution of 16		
0x408	NP_REG	[7:5]	SUBCLASSV_RD		Device Subclass Version. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
		[4:0]	NP-1_RD		Total Number of Bits per Sample. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B. Must be 16 bits per sample.	0x0	R
				0x0F	16 bits per sample.		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x409	S_REG	[7:5]	JESDV_RD		JESD204 Version. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
				000	JESD204A		
				001	JESD204B		
		[4:0]	S-1_RD		Number of Samples per Converter per Frame Cycle. Settings of one and two are valid. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
				0	One sample per converter per frame		
				1	Two samples per converter per frame		
0x40A	HD_CF_REG	7	HD_RD		High Density Format. See Section 5.1.3 of the JESD294B standard. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
				0	Low density mode		
				1	High density mode: link information received on Lane 0 as specified in Section 8.3 of JESD204B		
		[6:5]	RESERVED		Reserved.	0x0	R
		[4:0]	CF_RD		Number of Control Words per Frame Clock Period per Link. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B. Bits[4:0] must be 0.	0x0	R
0x40B	RES1_REG	[7:0]	RES1_RD		Reserved Field 1. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x40C	RES2_REG	[7:0]	RES2_RD		Reserved Field 2. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x40D	CHECKSUM_REG	[7:0]	FCHK0_RD		Checksum for Link Lane 0. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x40E	COMPSUM0_REG	[7:0]	FCMP0_RD		Computed Checksum for Link Lane 0. The JESD204B receiver computes the checksum of the link information received on Lane 0 as specified in Section 8.3 of JESD204B. The computation method is set by the CHECKSUM_MODE bit (Address 0x300[6]) and must match the likewise calculated checksum in Register 0x40D.	0x0	R
0x412	LID1_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID1_RD		Lane Identification for Link Lane 1.Link information received on Lane 0 as specified in section 8.3 of JESD204B.	0x0	R
0x415	CHECKSUM1_REG	[7:0]	FCHK1_RD		Checksum for Link Lane 1. Link information received on Lane 0 as specified in Section 8.3 of JESD204B.	0x0	R
0x416	COMPSUM1_REG	[7:0]	FCMP1_RD		Computed Checksum for Link Lane 1. See the description for Register 0x40E.	0x0	R
0x41A	LID2_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID2_RD		Lane Identification for Link Lane 2.	0x0	R
0x41D	CHECKSUM2_REG	[7:0]	FCHK2_RD		Checksum for Link Lane 2.	0x0	R
0x41E	COMPSUM2_REG	[7:0]	FCMP2_RD		Computed Checksum for Link Lane 2 (see the description for Register 0x40E).	0x0	R
0x422	LID3_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID3_RD		Lane Identification for Link Lane 3.	0x0	R
0x425	CHECKSUM3_REG	[7:0]	FCHK3_RD		Checksum for Link Lane 3.	0x0	R
0x426	COMPSUM3_REG	[7:0]	FCMP3_RD		Computed Checksum for Link Lane 3 (see the description for Register 0x40E).	0x0	R

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x42A	LID4_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID4_RD		Lane Identification for Link Lane 4.	0x0	R
0x42D	CHECKSUM4_REG	[7:0]	FCHK4_RD		Checksum for Link Lane 4.	0x0	R
0x42E	COMPSUM4_REG	[7:0]	FCMP4_RD		Computed Checksum for Link Lane 4 (see the description for Register 0x40E).	0x0	R
0x432	LID5_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID5_RD		Lane Identification for Link Lane 5.	0x0	R
0x435	CHECKSUM5_REG	[7:0]	FCHK5_RD		Checksum for Link Lane 5.	0x0	R
0x436	COMPSUM5_REG	[7:0]	FCMP5_RD		Computed Checksum for Link Lane 5 (see the description for Register 0x40E).	0x0	R
0x43A	LID6_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID6_RD		Lane Identification for Link Lane 6.	0x0	R
0x43D	CHECKSUM6_REG	[7:0]	FCHK6_RD		Checksum for Link Lane 6.	0x0	R
0x43E	COMPSUM6_REG	[7:0]	FCMP6_RD		Computed Checksum for Link Lane 6 (see the description for Register 0x40E).	0x0	R
0x442	LID7_REG	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	LID7_RD		Lane Identification for Link Lane 7.	0x0	R
0x445	CHECKSUM7_REG	[7:0]	FCHK7_RD		Checksum for Link Lane 7.	0x0	R
0x446	COMPSUM7_REG	[7:0]	FCMP7_RD		Computed Checksum for Link Lane 7 (see the description for Register 0x40E).	0x0	R
0x450	ILS_DID	[7:0]	DID		Device Identification Number. Link information received on Link Lane 0 as specified in Section 8.3 of JESD204B. Must be set to value read in Register 0x400.	0x0	R/W
0x451	ILS_BID	[7:4]	ADJCNT		Adjustment Resolution to DAC LMFC Must be set to 0.	0x0	R/W
		[3:0]	BID		Bank Identification: Extension to DID Must be set to value read in Register 0x401[3:0].	0x0	R/W
0x452	ILS_LID0	7	RESERVED		Reserved.	0x0	R
		6	ADJDIR		Direction to Adjust DAC LMFC. Must be set to 0.	0x0	R/W
		5	PHADJ		Phase Adjustment Request to DAC. Must be set to 0.	0x0	R/W
		[4:0]	LID0		Lane Identification for Link Lane 0. Must be set to the value read in Register 0x402[4:0].	0x0	R/W
0x453	ILS_SCR_L	7	SCR		Receiver Descrambling Enable.	0x1	R/W
				0	Descrambling is disabled		
				1	Descrambling is enabled		
		[6:5]	RESERVED		Reserved.	0x0	R
		[4:0]	L-1		Number of Lanes per Converter Device. See Table 34 and Table 35.	0x3	R/W
				0	One lane per converter		
				1	Two lanes per converter		
				3	Four lanes per converter		
				7	Eight lanes per converter (single link only)		
0x454	ILS_F	[7:0]	F-1		Number of Octets per Lane per Frame. Settings of 1, 2, and 4 (octets per lane) per frame are valid. See Table 34 and Table 35.	0x0	R/W
				0	(One octet per lane) per frame		
				1	(Two octets per lane) per frame		
				3	(Four octets per lane) per frame		
0x455	ILS_K	[7:5]	RESERVED		Reserved.	0x0	R
		[4:0]	K-1		Number of Frames per Multiframe. Settings of 16 or 32 are valid. Must be set to 32 when F = 1 (Register 0x476).	0x1F	R/W
				0x0F	16 frames per multiframe		
				0x1F	32 frames per multiframe		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x456	ILS_M	[7:0]	M-1		Number of Converters per Device. See Table 34 and Table 35.	0x1	R/W
				0	One converter per link		
				1	Two converters per link		
0x457	ILS_CS_N	[7:6]	CS		Number of Control Bits per Sample. Must be set to 0. Control bits are not supported.	0x0	R/W
				0	Zero control bits per sample		
		5	RESERVED		Reserved.	0x0	R
		[4:0]	N-1		Converter Resolution. Must be set to 16 bits of resolution.	0xF	R/W
				0x0F	Converter resolution of 16.		
0x458	ILS_NP	[7:5]	SUBCLASSV		Device Subclass Version.	0x1	R/W
				0	Subclass 0		
				1	Subclass 1		
		[4:0]	NP-1		Total Number of Bits per Sample. Must be set to 16 bits per sample.	0xF	R/W
				0xF	16 bits per sample.		
0x459	ILS_S	[7:5]	JESDV		JESD204 Version.	0x1	R/W
				000	JESD204A		
				001	JESD204B		
		[4:0]	S-1		Number of Samples per Converter per Frame Cycle. Settings of one and two are valid.	0x0	R/W
				0	One sample per converter per frame		
				1	Two samples per converter per frame		
0x45A	ILS_HD_CF	7	HD		High Density Format. If F = 1, HD must be set to 1. Otherwise, HD must be set to 0. See Section 5.1.3 of JESD204B standard.	0x1	R/W
				0	Low density mode		
				1	High density mode		
		[6:5]	RESERVED		Reserved.	0x0	R
		[4:0]	CF		Number of Control Words per Frame Clock Period per Link. Must be set to 0. Control bits are not supported.	0x0	R/W
0x45B	ILS_RES1	[7:0]	RES1		Reserved Field 1.	0x0	R/W
0x45C	ILS_RES2	[7:0]	RES2		Reserved Field 2.	0x0	R/W
0x45D	ILS_CHECKSUM	[7:0]	FCHK0		Checksum for Link Lane 0. Calculated checksum. Calculation depends on 0x300[6].	0x45	R/W
0x46B	ERRCNTRMON_RB	[7:0]	READERRORCNTR		Read JESD204B Error Counter. After selecting the lane and error counter by writing to LANESEL and CNTRSEL (both in this same register), the selected error counter is read back here.	0x0	R
0x46B	ERRCNTRMON	7	RESERVED		Reserved.	0x0	R
		[6:4]	LANESEL		Link Lane select for JESD204B error counter. Selects the lane whose errors are read back in this register.	0x0	W
				x	Selects Link Lane x		
		[3:2]	RESERVED		Reserved.	0x0	R
		[1:0]	CNTRSEL		JESD204B Error Counter Select. Selects the type of error that are read back in this register.	0x0	W
				00	BADDISCNTR: bad running disparity counter		
				01	NITCNTR: not in table error counter		
				10	UCCCNTR: Unexpected control character counter		
0x46C	LANEDESKEW	[7:0]	LANEDESKEW		Lane Deskew. Setting Bit x deskews Link Lane x	0xF	R/W
0x46D	BADDISPARITY_RB	[7:0]	BADDIS		Bad Disparity Character Error (BADDIS). Bit x is set when the bad disparity error count for Link Lane x reaches the threshold in Register 0x47C.	0x0	R

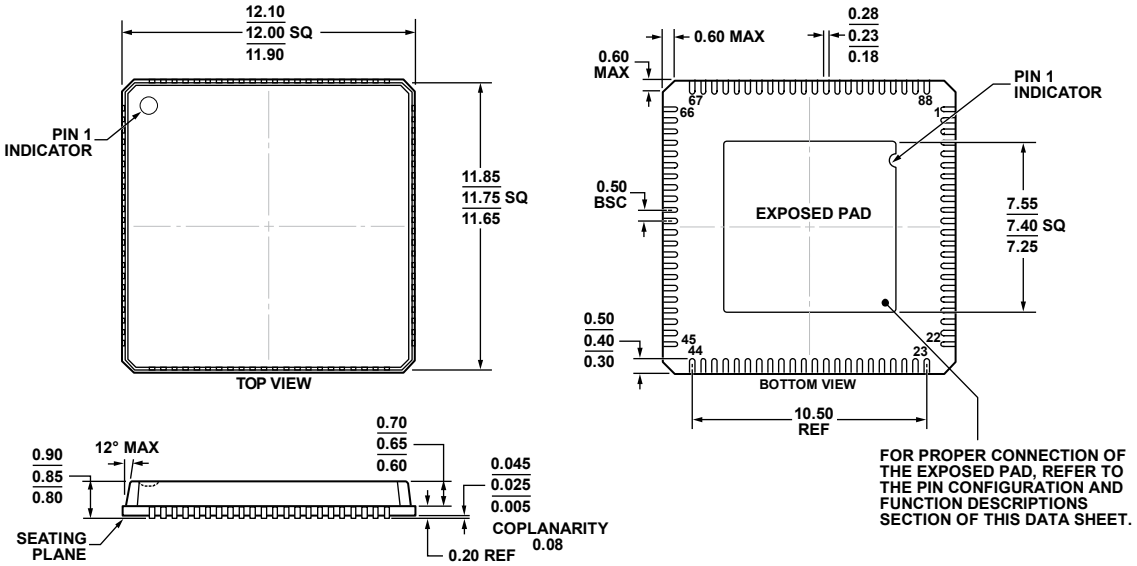
Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x46D	BADDISPARITY	7	RST_IRQ_DIS		BADDIS IRQ Reset. Reset BADDIS IRQ for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		6	DISABLE_ERR_ CNTR_DIS		BADDIS Error Counter Disable. Disable the BADDIS error counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		5	RST_ERR_CNTR_DIS		BADDIS Error Counter Reset. Reset BADDIS error counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		[4:3]	RESERVED		Reserved.	0x0	R
		[2:0]	LANE_ADDR_DIS		Link Lane Address for Functions Described in Bits[7:5].	0x0	W
0x46E	NIT_RB	[7:0]	NIT		Not in table Character Error (NIT). Bit x is set when Link Lane x's NIT error count reaches the threshold in Register 0x47C.	0x0	R
0x46E	NIT_W	7	RST_IRQ_NIT		IRQ Reset. Reset IRQ for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		6	DISABLE_ERR_ CNTR_NIT		Disable Error Counter. Disable the error counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		5	RST_ERR_CNTR_NIT		Reset Error Counter. Reset error counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		[4:3]	RESERVED		Reserved.	0x0	R
		[2:0]	LANE_ADDR_NIT		Link Lane Address for Functions Described in Bits[7:5].	0x0	W
0x46F	UNEXPECTED-CONTROL_RB	[7:0]	UCC		Unexpected Control Character Error (UCC). Bit x is set when Link Lane x's UCC error count reaches the threshold in Register 0x47C.	0x0	R
0x46F	UNEXPECTED-CONTROL_W	7	RST_IRQ_UCC		IRQ Reset. Reset IRQ for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		6	DISABLE_ERR_ CNTR_UCC		Disable Error Counter. Disable the error counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		5	RST_ERR_CNTR_ UCC		Reset Error Counter. Reset error counter for lane selected via Bits[2:0] by writing 1 to this bit.	0x0	W
		[4:3]	RESERVED		Reserved.	0x0	R
		[2:0]	LANE_ADDR_UCC		Link Lane Address for Functions Described in Bits[7:5].	0x0	W
0x470	CODEGRPSYNCFLG	[7:0]	CODEGRPSYNC		Code Group Sync Flag (from Each Instantiated Lane). Writing 1 to Bit 7 resets the IRQ. The associated IRQ flag is located in Register 0x47A[0]. A loss of CODEGRPSYNC triggers sync request assertion. See the SYNCOUTx±, SYSREF±, and CLK± Signals section and the Deterministic Latency section.	0x0	R/W
				0	Synchronization is lost		
				1	Synchronization is achieved		
0x471	FRAMESYNCFLG	[7:0]	FRAMESYNC		Frame Sync Flag (from Each Instantiated Lane). This register indicates the live status for each lane. Writing 1 to Bit 7 resets the IRQ. A loss of frame sync automatically initiates a synchronization sequence.	0x0	R/W
				0	Synchronization is lost		
				1	Synchronization is achieved		
0x472	GOODCHKSUMFLG	[7:0]	GOODCHECKSUM		Good Checksum Flag (from Each Instantiated Lane). Writing 1 to Bit 7 resets the IRQ. The associated IRQ flag is located in Register 0x47A[2].	0x0	R/W
				0	Last computed checksum is not correct		
				1	Last computed checksum is correct		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x473	INITLANESYNCFLG	[7:0]	INITIALLANESYNC		Initial Lane Sync Flag (from Each Instantiated Lane). Writing 1 to Bit 7 resets the IRQ. The associated IRQ flag is located in Register 0x47A[3]. Loss of synchronization is also reported on SYNCOUT1± or SYNCOUT0±. See the SYNCOUTx±, SYSREF±, and CLK± Signals section and the Deterministic Latency section.	0x0	R/W
0x476	CTRLREG1	[7:0]	F		Number of Octets per Frame. Settings of 1, 2, and 4 are valid. See Table 34 and Table 35.	0x1	R/W
				1	One octet per frame		
				2	Two octets per frame		
				4	Four octets per frame		
0x477	CTRLREG2	7	ILAS_MODE		ILAS Test Mode. Defined in Section 5.3.3.8 of JESD204B specification.	0x0	R/W
				1	JESD204B receiver is constantly receiving ILAS frames		
				0	Normal link operation		
		[6:4]	RESERVED		Reserved.	0x0	R
		3	THRESHOLD_ MASK_EN		Threshold Mask Enable. Set this bit if using SYNC_ASSERTION_MASK (Register 0x47B[7:5]).	0x0	R/W
		[2:0]	RESERVED		Reserved.	0x0	R
0x478	KVAL	[7:0]	KSYNC		Number of K Multiframes During ILAS (Divided by Four). Sets the number of multiframes to send initial lane alignment sequence. Cannot be set to 0.	0x1	R/W
				x	4× multiframes during ILAS		
0x47A	IRQVECTOR_MASK	7	BADDIS_MASK		Bad Disparity Mask.	0x0	W
				1	If the bad disparity count reaches ERRORTHRESH on any lane, IRQ is pulled low.		
		6	NIT_MASK		Not in table Mask.	0x0	W
				1	If the not in table character count reaches ERRORTHRESH on any lane, IRQ is pulled low.		
		5	UCC_MASK		Unexpected Control Character Mask.	0x0	W
				1	If the unexpected control character count reaches ERRORTHRESH on any lane, IRQ is pulled low.		
		4	RESERVED		Reserved.	0x0	R
		3	INITIALLANESYNC_ MASK		Initial Lane Sync Mask.	0x0	W
				1	If initial lane sync (0x473) fails on any lane, IRQ is pulled low.		
		2	BADCHECKSUM_ MASK		Bad Checksum Mask.	0x0	W
				1	If there is a bad checksum (0x472) on any lane, IRQ is pulled low.		
		1	FRAMESYNC_ MASK		Frame Sync Mask	0x0	W
				1	If frame sync (0x471) fails on any lane, IRQ is pulled low.		
		0	CODEGRPSYNC_ MASK		Code Group Sync Machine Mask.	0x0	W
				1	If code group sync (0x470) fails on any lane, IRQ is pulled low.		
0x47A	IRQVECTOR_FLAG	7	BADDIS_FLAG		Bad Disparity Error Count.	0x0	R
				1	Bad disparity character count reached ERRORTHRESH (0x47C) on at least one lane. Read Register 0x46D to determine which lanes are in error.		
		6	NIT_FLAG		Not in table Error Count	0x0	R
				1	Not in table character count reached ERRORTHRESH (0x47C) on at least one lane. Read Register 0x46E to determine which lanes are in error.		

Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
		5	UCC_FLAG		Unexpected Control Character Error Count	0x0	R
				1	Unexpected control character count reached ERRORTHRESH (0x47C) on at least one lane. Read Register 0x46F to determine which lanes are in error.		
		4	RESERVED		Reserved.	0x0	R
		3	INITIALLANESYNC_ FLAG		Initial Lane Sync Flag.	0x0	R
				1	Initial lane sync failed on at least one lane. Read Register 0x473 to determine which lanes are in error		
		2	BADCHECKSUM_ FLAG		Bad Checksum Flag.	0x0	R
				1	Bad checksum on at least one lane. Read Register 0x472 to determine which lanes are in error.		
		1	FRAMESYNC_ FLAG		Frame Sync Flag.	0x0	R
				1	Frame sync failed on at least one lane. Read Register 0x471 to determine which lanes are in error.		
		0	CODEGRPSYNC_ FLAG		Code Group Sync Flag.	0x0	R
				1	Code group sync failed on at least one lane. Read Register 0x470 to determine which lanes are in error		
0x47B	SYNCASSERTIONMASK	7	BADDIS_S		Bad Disparity Error on Sync.	0x0	R/W
				1	Asserts a sync request on $\overline{\text{SYNCOUTx±}}$ when the bad disparity character count reaches the threshold in Register 0x47C		
		6	NIT_S		Not in table Error on Sync.	0x0	R/W
				1	Asserts a sync request on $\overline{\text{SYNCOUTx±}}$ when the not in table character count reaches the threshold in Register 0x47C		
		5	UCC_S		Unexpected Control Character Error on Sync.	0x0	R/W
				1	Asserts a sync request on $\overline{\text{SYNCOUTx±}}$ when the unexpected control character count reaches the threshold in Register 0x47C		
		4	CMM		Configuration Mismatch IRQ. If CMM_ENABLE is high, this bit latches on a rising edge and pull $\overline{\text{IRQ}}$ low. When latched, write a 1 to clear this bit. If CMM_ENABLE is low, this bit is non-functional.	0x0	R/W
				1	Link Lane 0 configuration registers (Register 0x450 to Register 0x45D) do not match the JESD204B transmit settings (Register 0x400 to Register 0x40D)		
		3	CMM_ENABLE		Configuration Mismatch IRQ Enable.	0x1	R/W
				1	Enables IRQ generation if a configuration mismatch is detected		
				0	Configuration mismatch IRQ disabled		
		[2:0]	RESERVED		Reserved.	0x0	R
0x47C	ERRORTHRES	[7:0]	ETH		Error Threshold. Bad disparity, not in table, and unexpected control character errors are counted and compared to the error threshold value. When the count reaches the threshold, either an IRQ is generated or the $\overline{\text{SYNCOUTx±}}$ signal is asserted per the mask register settings, or both. Function is performed in all lanes.	0xFF	R/W
0x47D	LANEENABLE	[7:0]	LANE_ENA		Lane Enable. Setting Bit x enables Link Lane x. This register must be programmed before receiving the code group pattern for proper operation.	0xF	R/W

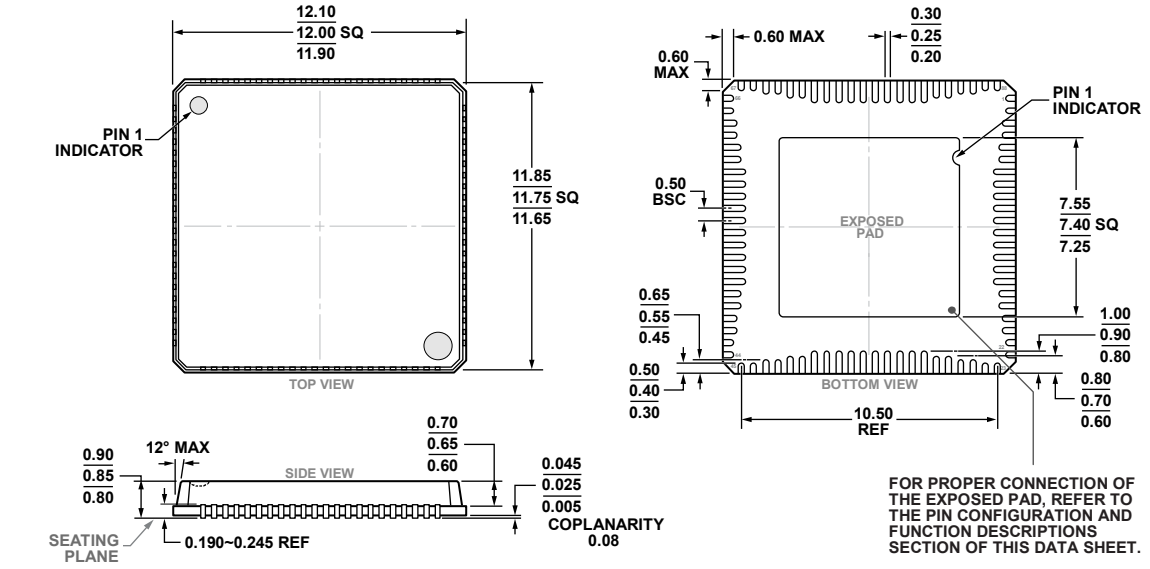
Address	Name	Bit No.	Bit Name	Settings	Description	Reset	Access
0x47E	RAMP_ENA	[7:1]	RESERVED		Reserved.	0x0	R
		0	ENA_RAMP_ CHECK		Enable Ramp Checking at the Beginning of ILAS.	0x0	W
				0	Disable ramp checking at beginning of ILAS; ILAS data need not be a ramp		
				1	Enable ramp checking; ILAS data needs to be a ramp starting at 00-01-02; otherwise, the ramp ILAS fails and the device does not start up		
0x520	DIG_TEST0	[7:2]	RESERVED		Must write default value for proper operation.	0x7	R/W
		1	DC_TEST_MODE		DC Test Mode	0x0	R/W
		0	RESERVED		Reserved.	0x0	R/W
0x521	DC_TEST_VALUE0	[7:0]	DC_TEST_ VALUE[7:0]		DC Value LSB of DC Test Mode for DAC0 and DAC1.	0x0	R/W
0x522	DC_TEST_VALUE1	[7:0]	DC_TEST_ VALUE[15:8]		DC value MSB of DC Test Mode for DAC0 and DAC1.	0x0	R/W

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VRRD

Figure 91. 88-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
12 mm × 12 mm Body, Very Thin Quad
(CP-88-6)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220

Figure 92. 88-Lead Lead Frame Chip Scale Package [LFCSP_VQ] (Variable Lead Length)
12 mm × 12 mm Body, Very Thin Quad
(CP-88-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9135BCPZ	−40°C to +85°C	88-Lead LFCSP_VQ	CP-88-6
AD9135BCPZRL	−40°C to +85°C	88-Lead LFCSP_VQ	CP-88-6
AD9135BCPAZ	−40°C to +85°C	88-Lead LFCSP_VQ (Variable Lead Length)	CP-88-9
AD9135BCPAZRL	−40°C to +85°C	88-Lead LFCSP_VQ (Variable Lead Length)	CP-88-9
AD9136BCPZ	−40°C to +85°C	88-Lead LFCSP_VQ	CP-88-6
AD9136BCPZRL	−40°C to +85°C	88-Lead LFCSP_VQ	CP-88-6
AD9136BCPAZ	−40°C to +85°C	88-Lead LFCSP_VQ (Variable Lead Length)	CP-88-9
AD9136BCPAZRL	−40°C to +85°C	88-Lead LFCSP_VQ (Variable Lead Length)	CP-88-9
AD9136-FMC-EBZ		FMC Evaluation Board	
AD9135-FMC-EBZ		FMC Evaluation Board	

[1] Z = RoHS Compliant Part.

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