Data Sheet

AD9177

Quad, 16-Bit, 12 GSPS RF DAC with Wideband Channelizers

FEATURES

- Flexible, reconfigurable common platform design
  - 4 DAC cores connected to various DSP and bypass datapaths
  - Supports single, dual, and quad band
  - Datapaths and DSP blocks are fully bypassable
  - On-chip PLL with multichip synchronization
    - External RFCLK input option for off-chip PLL
- Maximum DAC sample rate up to 12 GSPS
  - Maximum data rate up to 12 GSPS using JESD204C
  - Useable analog bandwidth to 8 GHz
- DAC ac performance at 12 GSPS
  - Full-scale output current range: 6.43 mA to 37.75 mA
  - Two-tone IMD3 (−7 dBFS per tone): −78.9 dBc
  - NSD, single-tone at 3.7 GHz: −155.1 dBc/Hz
  - SFDR, single-tone at 3.7 GHz: −70 dBc
- Versatile digital features
  - Selectable interpolation filters
  - Configurable or bypassable DUCs
    - 8 fine complex DUCs and 4 coarse complex DUCs
    - 48-bit NCO per DUC
    - Option to bypass fine and coarse DUC
  - Programmable delay per datapath
  - Transmit DPD support
    - Fine DUC channel gain control and delay adjust
- Auxiliary features
  - Direct digital synthesis and fast frequency hopping
  - Low latency loopback mode (receive datapath NCO outputs can be routed to the transmit datapaths)
  - Power amplifier downstream protection circuitry
  - On-chip temperature monitoring unit
  - Flexible GPIO pins
  - TDD power savings option
- SERDES JESD204B/JESD204C interface
  - 8-lane JESD204B/C receiver (JRx)
  - JESD204B compliance with the maximum 15.5 Gbps
  - JESD204C compliance with the maximum 24.75 Gbps
  - Supports real or complex digital data (8-, 12-, 16-, or 24-bit)
- 15 mm × 15 mm, 324-ball BGA with 0.8 mm pitch

APPLICATIONS

- Wireless communications infrastructure
- Microwave point to point, E-band and 5G mmWave
- Broadband communications systems
- DOCSIS 3.1 and 4.0 CMTS
- Phased array radar and electronic warfare
- Electronic test and measurement systems

GENERAL DESCRIPTION

The AD9177 is a highly integrated device with four 16-bit, 12 GSPS maximum sample rate, RF digital-to-analog converter (DAC) cores supporting up to eight baseband channels. The device is well suited for applications requiring wideband DACs to process signals of wide instantaneous bandwidth. The device features an 8-lane, 24.75 Gbps JESD204C or 15.5 Gbps JESD204B data receiver (JRx) port, an on-chip clock multiplier, and digital signal processing (DSP) datapaths capable of processing complex signals for wideband or multiband direct to RF applications, phase array radar systems, and electronic warfare applications. The DSP datapaths can be bypassed to allow a direct connection between the data receiver port and the DAC cores.

For direct digital synthesis (DDS) applications, the AD9177 can be operated without a data receiver port to generate multiple sine wave tones of varying frequencies. The main numerically controlled oscillator (NCO) block inside each of the four course digital upconverters (DUCs) contains one 48-bit NCO and a bank of thirty one 32-bit NCOs, each with an independent phase accumulator. Similarly, the main NCO block inside each of the course and fine digital downconverters (DDCs) in the receive datapath contains a bank of sixteen 48-bit NCOs that can be looped into the transmit datapath for processing ahead of the course DUCs and DAC outputs. Combined with general-purpose input/output (GPIO) controls for frequency hopping, preconfigurable profile selection, and the ability to synchronize the NCOs to a common trigger using the SYSREF input port, this bank allows phase coherent fast frequency hopping (FFH) for applications where multiple devices are synchronized or where NCO frequencies are continuously adjusted during operation.

Rev. A

TABLE OF CONTENTS

REVISION HISTORY

7/2021—Rev. 0 to Rev. A

Changes to Data Sheet Title and Features Section ... 1

6/2021—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

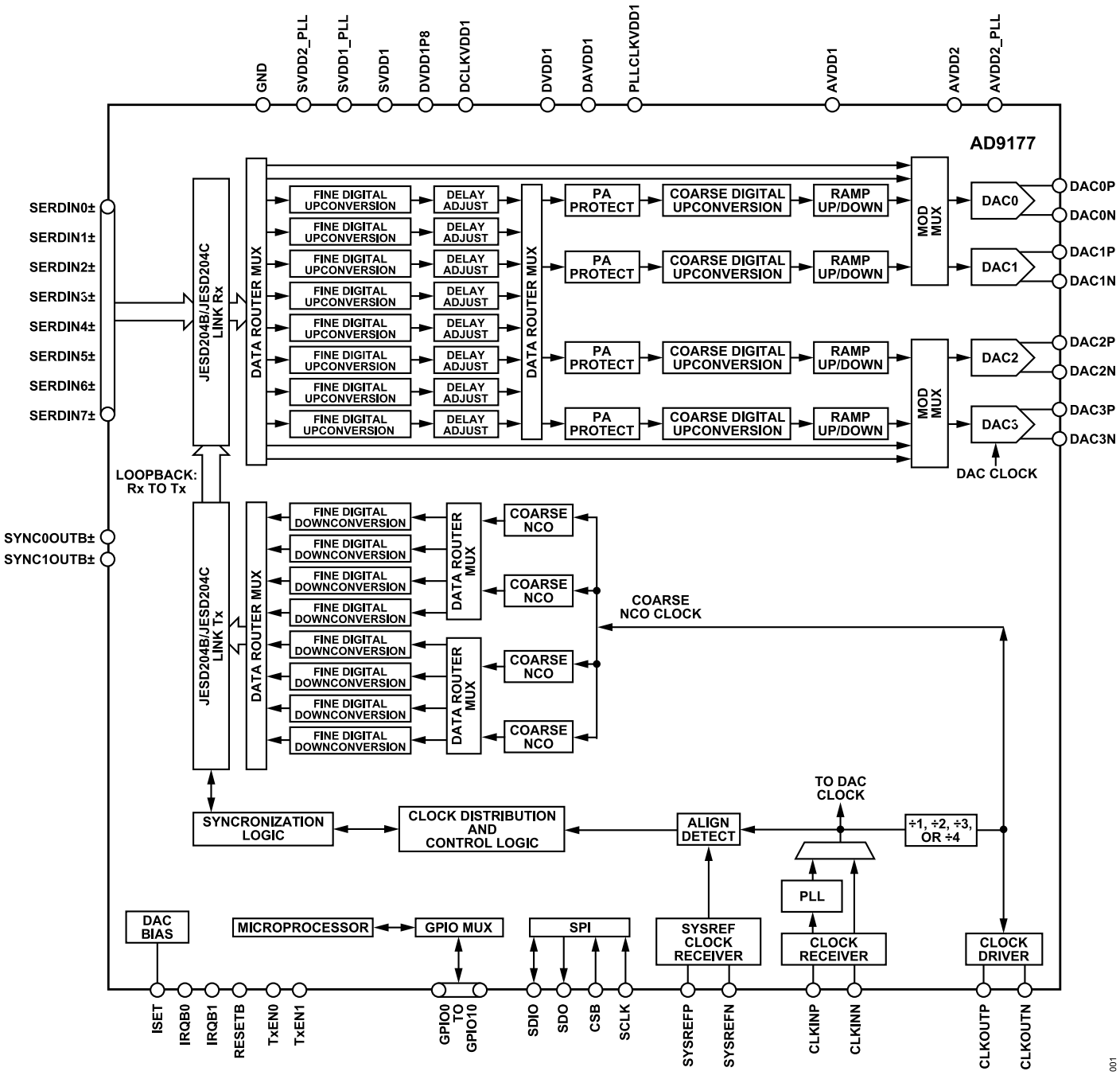

Figure 1.

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Successful DAC calibration is required during the device initialization phase that occurs shortly after power-up to ensure long-term reliability of the DAC core circuitry. Refer to the UG-1578 user guide for more information on device initialization.

Table 1.

Parameter	Min	Typ	Max	Unit
OPERATING JUNCTION TEMPERATURE (T_J)	−40		+120	°C
ANALOG SUPPLY VOLTAGE RANGE				
AVDD2, AVDD2_PLL	1.9	2.0	2.1	V
AVDD1, PLLCLKVDD1	0.95	1.0	1.05	V
DIGITAL SUPPLY VOLTAGE RANGE				
DVDD1, DCLKVDD1, DAVDD1	0.95	1.0	1.05	V
DVDD1P8	1.7	1.8	2.1	V
SERIALIZER/DESERIALIZER (SERDES) SUPPLY VOLTAGE RANGE				
SVDD2_PLL	1.9	2.0	2.1	V
SVDD1, SVDD1_PLL	0.95	1.0	1.05	V

POWER CONSUMPTION

Typical at nominal supplies and maximum at 5% supplies. For the minimum and maximum values, T_J varies between −40°C and +120°C. For the typical values, T_A = 25°C, which corresponds to T_J = 80°C, unless otherwise noted.

DAC datapath with a complex I/Q data rate frequency (f_{IQ_DATA}) = 2 GSPS, interpolation of 6×, and DAC frequency (f_{DAC}) of 12 GSPS. JESD204C mode of 24C (L = 8, M = 8, F = 3, S = 2, K = 256, E = 3, N = 12, NP = 12).

See the UG-1578 user guide for further information on the JESD204B and JESD204C mode configurations and a detailed description of the settings referenced throughout this data sheet. A table showing other operational modes and the corresponding typical and maximum power consumption numbers is included.

Table 2. Power Consumption

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENTS					
AVDD2 (I_{AVDD2})	2.0 V supply		273	301	mA
AVDD2_PLL (I_{AVDD2_PLL}) +SVDD2_PLL (I_{SVDD2_PLL})	2.0 V supply		45	56	mA
Power Dissipation for 2 V Supplies	2.0 V supply total power dissipation		0.63	0.7	W
PLLCLKVDD1 ($I_{PLLCLKVDD1}$)	1.0 V supply		15	25	mA
AVDD1 (I_{AVDD1})	1.0 V supply		1770	2338	mA
DAVDD1 (I_{DAVDD1})	1.0 V supply		1140	1484	mA
DVDD1 (I_{DVDD1})	1.0 V supply		1823	2973	mA
SVDD1 (I_{SVDD1}) + SVDD1_PLL (I_{SVDD1_PLL})	1.0 V supply		1046	1600	mA
Power Dissipation for 1 V Supplies	1.0 V supply total power dissipation		5.7	8.4	W
DVDD1P8 ($I_{DVDD1P8}$)	1.8 V supply		7	10	mA
Total Power Dissipation	Total power dissipation of 2 V and 1 V supplies		6.4	9.1	W

SPECIFICATIONS

DAC DC SPECIFICATIONS

Nominal supplies with DAC full-scale output current (I_{OUTFS}) = 26 mA, unless otherwise noted. ADC setup in 4 GSPS, full bandwidth mode (all digital downconverters bypassed). For the minimum and maximum values, T_J = −40°C to +120°C, and for the typical values, T_A = 25°C, which corresponds to T_J = 80°C, unless otherwise noted.

Table 3. DAC DC Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DAC RESOLUTION		16			Bit
DAC ACCURACY					
Gain Error			1.5		% FSR
Gain Matching			0.7		% FSR
Integral Nonlinearity (INL)	Shuffling disabled		8.0		LSB
Differential Nonlinearity (DNL)	Shuffling disabled		3.5		LSB
DAC ANALOG OUTPUTS	DACxP and DACxN				
Full-Scale Output Current Range	AC coupling, setting resistance (R_{SET}) = 5 kΩ				
AC Coupling	Output common-mode voltage (V_{CM}) = 0 V	6.43	26.5	37.75	mA
DC Coupling	50 Ω shunt to a negative supply, forcing V_{CM} = 0 V	6.43		37.75	mA
	50 Ω shunt to GND, forcing V_{CM} = 0.3 V	6.43		20[1]	mA
Full-Scale Sine Wave Output Power with AC Coupling[2]	Ideal 2:1 balun interface to 50 Ω				
I_{OUTFS} = 26.5 mA			3.3		dBm
I_{OUTFS} = 37.75 mA			7		dBm
Common-Mode Output Voltage (VCM_{OUT})			0		V
AC Coupling	Bias each output to GND across a shunt inductor		0		V
DC Coupling	Bias each output to a negative voltage rail across a 25 Ω to 200 Ω resistor, selected such that VCM_{OUT} = 0 V, VCM_{OUT} = 0.3 V is with a 25 Ω resistor to GND and I_{OUTFS} = 20 mA		0	0.3	V
Differential Resistance			100		Ω

[1] For dc-coupled applications, the maximum full-scale output current is limited by the maximum VCM_{OUT} specification.

[2] The actual measured full-scale power is frequency dependent due to DAC sinc response, impedance mismatch loss, and balun insertion loss.

SPECIFICATIONS

CLOCK INPUTS AND OUTPUTS

For the minimum and maximum values, T_J = −40°C to +120°C and ±5% of nominal supply, unless otherwise noted.

Table 4. Clock Inputs and Outputs

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK INPUTS	CLKINP and CLKINN				
Differential Input Power	Direct RF clock				
Minimum				0	dBm
Maximum				6	dBm
Common-Mode Voltage	AC-coupled			0.5	V
Differential Input Resistance				100	Ω
Differential Input Capacitance				0.3	pF
CLOCK OUTPUTS (ADC CLOCK DRIVER)	ADCDRVP and ADCDRVN				
Differential Output Voltage Magnitude[1]	1.5 GHz			740	mV p-p
	2.0 GHz			690	mV p-p
	3.0 GHz			640	mV p-p
	6.0 GHz			490	mV p-p
Differential Output Resistance				100	Ω
Common-Mode Voltage	AC-coupled			0.5	V

[1] Measured with differential 100 Ω load and less than 2 mm of printed circuit board (PCB) trace from package ball.

CLOCK INPUT AND PHASE-LOCKED LOOP (PLL) FREQUENCY SPECIFICATIONS

For the minimum and maximum values, T_J = −40°C to +120°C and ±5% of nominal supply, unless otherwise noted.

Table 5. Clock Input and PLL Frequency Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK INPUTS (CLKINP, CLKINN) FREQUENCY RANGES		25		12000	MHz
PHASE FREQUENCY DETECTOR (PFD) INPUT FREQUENCY RANGES		25		750	MHz
FREQUENCY RANGES ACCORDING TO CLOCK PATH CONFIGURATION					
Direct Clock (PLL Off)		2900[1]		12000	MHz
PLL Reference Clock (PLL On)	M divider set to divide by 1	25		750	MHz
	M divider set to divide by 2	50		1500	MHz
	M divider set to divide by 3	75		2250	MHz
	M divider set to divide by 4	100		3000	MHz
PLL VOLTAGE CONTROLLED OSCILLATOR (VCO) FREQUENCY RANGES					
VCO Output					
Divide by 1	D divider set to divide by 1	5.8		12	GHz
Divide by 2	D divider set to divide by 2	2.9		6	GHz
Divide by 3	D divider set to divide by 3	1.93333		4	GHz
Divide by 4	D divider set to divide by 4	1.45		3	GHz

[1] The minimum direct clock frequency is limited by the minimum DAC (core) sample rate, as specified in Table 6. The clock receiver can accommodate the full range between the minimum PLL reference clock frequency and the maximum direct clock frequency.

SPECIFICATIONS

DAC SAMPLE RATE SPECIFICATIONS

Nominal supplies. For the minimum and maximum values, T_J = −40°C to +120°C and ±5% of nominal supply. For the typical values, T_A = 25°C, which corresponds to T_J = 80°C, unless otherwise noted.

Table 6. DAC Sample Rate Specifications

Parameter	Min	Typ	Max	Unit
DAC SAMPLE RATE[1]				
Minimum			2.9	GSPS
Maximum	12			GSPS

[1] Pertains to the update rate of the DAC core, independent of the datapath and JESD204 mode configuration.

INPUT DATA RATE SPECIFICATIONS

For the minimum and maximum values, T_J = −40°C to +120°C and ±5% of nominal supply, unless otherwise noted.

Table 7. Input Data Rate Specifications

Parameter[1, 2]	Test Conditions/Comments	Min	Typ	Max	Unit
MAXIMUM DATA RATE PER NUMBER OF ACTIVE DAC OUTPUTS					
	Single DAC, fine digital upconverter (FDUC) and coarse digital upconverter (CDUC) bypassed (1× interpolation), 16-bit resolution, limited by the maximum DAC clock rate			12000	MSPS
	Quad DAC, FDUC and CDUC bypassed (1× interpolation), 12-bit resolution, limited by the maximum JESD204C link throughput (M = 4, L = 8)			4000	MSPS
MAXIMUM COMPLEX (I/Q) DATA RATE PER NUMBER OF ACTIVE INPUT DATA CHANNELS					
	1 channel: FDUC bypassed, 1 CDUC enabled, 12-bit or 16-bit resolution, limited by the maximum CDUC NCO clock rate			6000	MSPS
	2 channels: FDUC bypassed, 2 CDUCs enabled, 12-bit resolution, limited by the maximum JESD204C link throughput (M = 4, L = 8)			4000	MSPS
	4 channels: FDUC bypassed, 4 CDUCs enabled, 12-bit resolution, limited by the maximum JESD204C link throughput (M = 8, L = 8)			2000	MSPS
	8 channels: 8 FDUCs enabled, one or more CDUC enabled, 12-bit or 16-bit resolution, limited by the maximum FDUC NCO clock rate divided by the minimum 2× interpolation rate required to enable the FDUC			750	MSPS

[1] The values listed for these parameters are the maximum possible when considering all JESD204 modes of operation. Some modes are more limiting, based on other parameters.

[2] The interpolation filters in the Tx datapath have a total complex filter bandwidth of 80% of the data rate, combining the 40% bandwidth in the I path and 40% bandwidth in the Q path. Similarly, the decimation stages inside the Rx datapath use filters with a total complex filter bandwidth of 81.4%. Therefore, the maximum allowed instantaneous complex signal bandwidth (iBW) per channel is calculated as iBW = (complex I/Q data rate per channel) × (total complex filter bandwidth).

SPECIFICATIONS

NCO FREQUENCY SPECIFICATIONS

For the minimum and maximum values, T_J = −40°C to +120°C and ±5% of nominal supply, unless otherwise noted.

Table 8. NCO Frequency Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
MAXIMUM NCO CLOCK RATE					
FDUC NCO				1.5	GHz
CDUC NCO				12	GHz
MAXIMUM NCO SHIFT FREQUENCY RANGE					
FDUC NCO	Channel interpolation rate must be > 1×	−750		+750	MHz
CDUC NCO	f_{DAC} = 12 GHz, main interpolation rate must be > 1×	−6		+6	GHz
MAXIMUM FREQUENCY SPACING BETWEEN CHANNELIZER CHANNELS					
Tx FDUC Channels	Maximum FDUC NCO clock rate × 0.8[1]			1200	MHz

[1] The 0.8 factor is because the total complex pass-band of the first interpolation filter is 80% of the filter input data rate.

JESD204B AND JESD204C INTERFACE ELECTRICAL AND SPEED SPECIFICATIONS

Nominal supplies. For the minimum and maximum values, T_J = −40°C to +120°C and ±5% of nominal supply, and for the typical values, T_A = 25°C, which corresponds to T_J = 80°C, unless otherwise noted.

Table 9. Serial Interface Rate Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
JESD204B SERIAL INTERFACE RATE	Serial lane rate	1.0		15.5	Gbps
Unit Interval		64.5		1000.0	ps
JESD204C SERIAL INTERFACE RATE	Serial lane rate	6.0		24.75	Gbps
Unit Interval		40.4		166.67	ps

Table 10. JESD204 Receiver (JRx) Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
JESD204 DATA INPUTS	SERDINx±, where x = 0 to 7				
Standards Compliance			JESD204B and JESD204C		
Differential Voltage, R_{VDIFF}			800		mV p-p
Differential Impedance, Z_{RDIFF}	At dc		98		Ω
Termination Voltage, V_{TT}	AC-coupled		0.97		V
SYNCxOUTB± OUTPUTS[1]	Where x = 0 or 1				
Output Differential Voltage, V_{OD}	Driving 100 Ω differential load		400		mV
Output Offset Voltage, V_{OS}			DVDD1P8/2 + 0.2		V
SYNCxOUTB+ AND SYNCxOUTB−	CMOS output option		Refer to the CMOS Pin Specifications section		

[1] IEEE 1596.3 standard LVDS compatible.

Table 11. SYSREF Electrical Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYSREFP AND SYSREFN INPUTS					
Logic Compliance			LVDS/LVPECL[1]		
Differential Input Voltage			0.7	1.9	V p-p
Input Common-Mode Voltage Range	DC-coupled		0.675	2	V
Input Resistance, R_{IN} (Differential)			100		Ω
Input Capacitance (Differential)			1		pF

[1] LVDS means low voltage differential signaling and LVPECL means low voltage positive/pseudo emitter-coupled logic.

SPECIFICATIONS

CMOS PIN SPECIFICATIONS

For the minimum and maximum values, T_J = −40°C to +120°C, 1.7 V ≤ DVDD1P8 ≤ 2.1 V, other supplies nominal, unless otherwise noted.

Table 12. CMOS Pin Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUTS		SDIO, SCLK, CSB, RESETB, RXEN0, RXEN1, TXEN0, TXEN1, SYNC0INB±, SYNC1INB±, and GPIOx				
Logic 1 Voltage	V_{IH}		0.70 × DVDD1P8			V
Logic 0 Voltage	V_{IL}				0.3 × DVDD1P8	V
Input Resistance			40			kΩ
OUTPUTS		SDIO, SDO, GPIOx, SYNC0OUTB±, and SYNC1OUTB±, 4 mA load				
Logic 1 Voltage	V_{OH}		DVDD1P8 − 0.45			V
Logic 0 Voltage	V_{OL}				0.45	V
INTERRUPT OUTPUTS		IRQB_0 and IRQB_1, pull-up resistor of 5 kΩ to DVDD1P8				
Logic 1 Voltage	V_{OH}		1.35			V
Logic 0 Voltage	V_{OL}				0.48	V

DAC AC SPECIFICATIONS

Nominal supplies with T_A = 25°C. Specifications represent the average of all four DAC channels with the DAC I_{OUTFS} = 26 mA, unless otherwise noted.

Table 13. DAC AC Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
Single-Tone, f_{DAC} = 12 GSPS	−7 dBFS digital backoff, shuffle enabled, 15C mode				
Output Frequency (f_{OUT}) = 70 MHz		63	80		dBc
f_{OUT} = 100 MHz			77		dBc
f_{OUT} = 500 MHz			76		dBc
f_{OUT} = 900 MHz			77		dBc
f_{OUT} = 1900 MHz		61	79		dBc
f_{OUT} = 2600 MHz			75		dBc
f_{OUT} = 3700 MHz			69		dBc
f_{OUT} = 4500 MHz			68		dBc
Single-Tone, f_{DAC} = 9 GSPS	−7 dBFS digital backoff, shuffle enabled, 15C mode				
f_{OUT} = 100 MHz			78		dBc
f_{OUT} = 500 MHz			78		dBc
f_{OUT} = 900 MHz			77		dBc
f_{OUT} = 1900 MHz			80		dBc
f_{OUT} = 2600 MHz			80		dBc
f_{OUT} = 3700 MHz			72		dBc
Single-Tone, f_{DAC} = 6 GSPS	−7 dBFS digital backoff, shuffle enabled, 15C mode				
f_{OUT} = 100 MHz			84		dBc
f_{OUT} = 500 MHz			81		dBc
f_{OUT} = 900 MHz			82		dBc
f_{OUT} = 1900 MHz			81		dBc
ADJACENT CHANNEL LEAKAGE RATIO					
Single Carrier 20 MHz LTE Downlink Test Vector	−1 dBFS digital backoff, 256 QAM				

SPECIFICATIONS

Table 13. DAC AC Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
f_{DAC} = 12 GSPS	f_{OUT} = 1840 MHz		77		dBc
	f_{OUT} = 2650 MHz		76		dBc
	f_{OUT} = 3500 MHz		73		dBc
f_{DAC} = 9 GSPS	f_{OUT} = 1900 MHz		77		dBc
	f_{OUT} = 2650 MHz		77		dBc
f_{DAC} = 6 GSPS	f_{OUT} = 750 MHz		79		dBc
	f_{OUT} = 1840 MHz		77		dBc
THIRD-ORDER INTERMODULATION DISTORTION (IMD3)	Two tone test, 1 MHz spacing, 0 dBFS digital backoff, −6 dBFS per tone				
f_{DAC} = 12 GSPS	f_{OUT} = 1900 MHz		−69	−62	dBc
	f_{OUT} = 2600 MHz		−72		dBc
	f_{OUT} = 3700 MHz		−72		dBc
f_{DAC} = 9 GSPS	f_{OUT} = 1900 MHz		−79		dBc
	f_{OUT} = 2600 MHz		−76		dBc
f_{DAC} = 6 GSPS	f_{OUT} = 900 MHz		−79		dBc
	f_{OUT} = 1900 MHz		−90		dBc
NOISE SPECTRAL DENSITY (NSD)	0 dBFS, NSD measurement taken at 10% away from f_{OUT}, shuffle off				
Single-Tone, f_{DAC} = 12 GSPS					
f_{OUT} = 150 MHz			−168		dBc/Hz
f_{OUT} = 500 MHz			−167		dBc/Hz
f_{OUT} = 950 MHz			−165		dBc/Hz
f_{OUT} = 1840 MHz			−162		dBc/Hz
f_{OUT} = 2650 MHz			−160		dBc/Hz
f_{OUT} = 3700 MHz			−155		dBc/Hz
f_{OUT} = 4500 MHz			−154		dBc/Hz
Single-Tone, f_{DAC} = 9 GSPS					
f_{OUT} = 150 MHz			−168		dBc/Hz
f_{OUT} = 500 MHz			−166		dBc/Hz
f_{OUT} = 950 MHz			−164		dBc/Hz
f_{OUT} = 1840 MHz			−160		dBc/Hz
f_{OUT} = 2650 MHz			−158		dBc/Hz
f_{OUT} = 3700 MHz			−154		dBc/Hz
Single-Tone, f_{DAC} = 6 GSPS					
f_{OUT} = 150 MHz			−168		dBc/Hz
f_{OUT} = 500 MHz			−165		dBc/Hz
f_{OUT} = 950 MHz			−163		dBc/Hz
f_{OUT} = 1840 MHz			−159		dBc/Hz
f_{OUT} = 2650 MHz			−157		dBc/Hz
SINGLE SIDEBAND PHASE NOISE OFFSET (PLL DISABLED)	Direct device clock input at 6 dBm				
f_{OUT} = 3.6 GHz, f_{DAC} = 12 GSPS, CLKINx Frequency (f_{CLKIN}) = 12 GHz	Rohde & Schwarz SMA100B B711 option				
1 kHz			−118		dBc/Hz
10 kHz			−129		dBc/Hz
100 kHz			−137		dBc/Hz
600 kHz			−144		dBc/Hz
1.2 MHz			−148		dBc/Hz
1.8 MHz			−149		dBc/Hz
6 MHz			−153		dBc/Hz

SPECIFICATIONS

Table 13. DAC AC Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SINGLE SIDEBAND PHASE NOISE OFFSET (PLL ENABLED)	Loop filter component values include C1 = 22 nF, R1 = 226 Ω, C2 = 2.2 nF, C3 = 33 nF, and PFD = 500 MHz[1]				
f_{OUT} = 1.8 GHz, f_{DAC} = 12 GSPS, f_{CLKIN} = 0.5 GHz					
1 kHz			−106		dBc/Hz
10 kHz			−113		dBc/Hz
100 kHz			−120		dBc/Hz
600 kHz			−127		dBc/Hz
1.2 MHz			−134		dBc/Hz
1.8 MHz			−138		dBc/Hz
6 MHz			−150		dBc/Hz

[1] See UG-1578 for details on the loop filter components.

SPECIFICATIONS

TIMING SPECIFICATIONS

For the minimum and maximum values, T_J = −40°C to +120°C and ±5% of nominal supply, unless otherwise noted.

Table 14. Timing Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SERIAL PORT INTERFACE (SPI) WRITE OPERATION						
Maximum SCLK Clock Rate	f_{SCLK}, $1/t_{SCLK}$		33			MHz
SCLK Clock High	t_{PWH}	SCLK = 33 MHz	8			ns
SCLK Clock Low	t_{PWL}	SCLK = 33 MHz	8			ns
SDIO to SCLK Setup Time	t_{DS}		4			ns
SCLK to SDIO Hold Time	t_{DH}		4			ns
CSB to SCLK Setup Time	t_S		4			ns
CLK to CSB Hold Time	t_H		4			ns
SPI READ OPERATION						
LSB First Data Format						
Maximum SCLK Clock Rate	f_{SCLK}, $1/t_{SCLK}$		33			MHz
SCLK Clock High	t_{PWH}		8			ns
SCLK Clock Low	t_{PWL}		8			ns
MSB First Data Format						
Maximum SCLK Clock Rate	f_{SCLK}, $1/t_{SCLK}$		15			MHz
SCLK Clock High	t_{PWH}		30			ns
SCLK Clock Low	t_{PWL}		30			ns
SDIO to SCLK Setup Time	t_{DS}		4			ns
SCLK to SDIO Hold Time	t_{DH}		4			ns
CSB to SCLK Setup Time	t_S		4			ns
SCLK to SDIO Data Valid Time	t_{DV}		20			ns
SCLK to SDO Data Valid Time	t_{DV_SDO}		20			ns
CSB to SDIO Output Valid to High-Z	t_Z		20			ns
CSB to SDO Output Valid to High-Z	t_{Z_SDO}		20			ns
RESETB		Minimum hold time to trigger a device reset	40			ns

Timing Diagrams

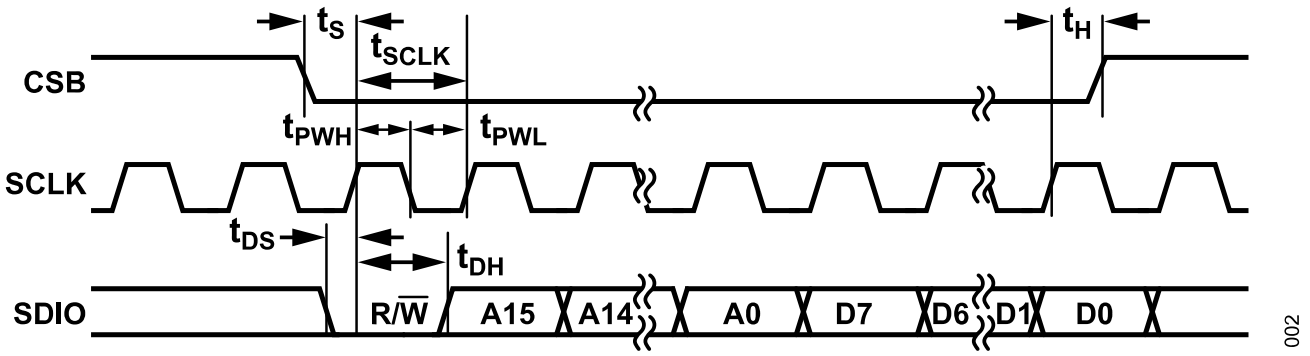

Figure 2. Timing Diagram for 3-Wire Write Operation

SPECIFICATIONS

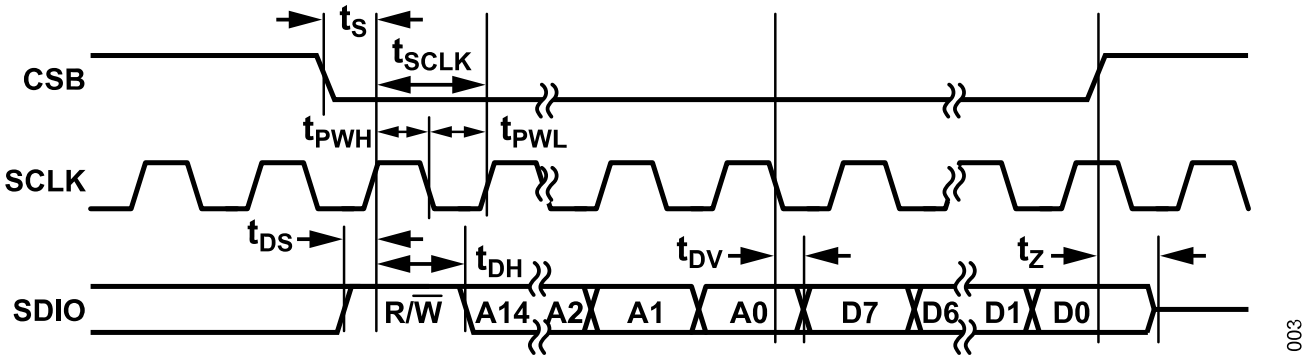

Figure 3. Timing Diagram for 3-Wire Read Operation

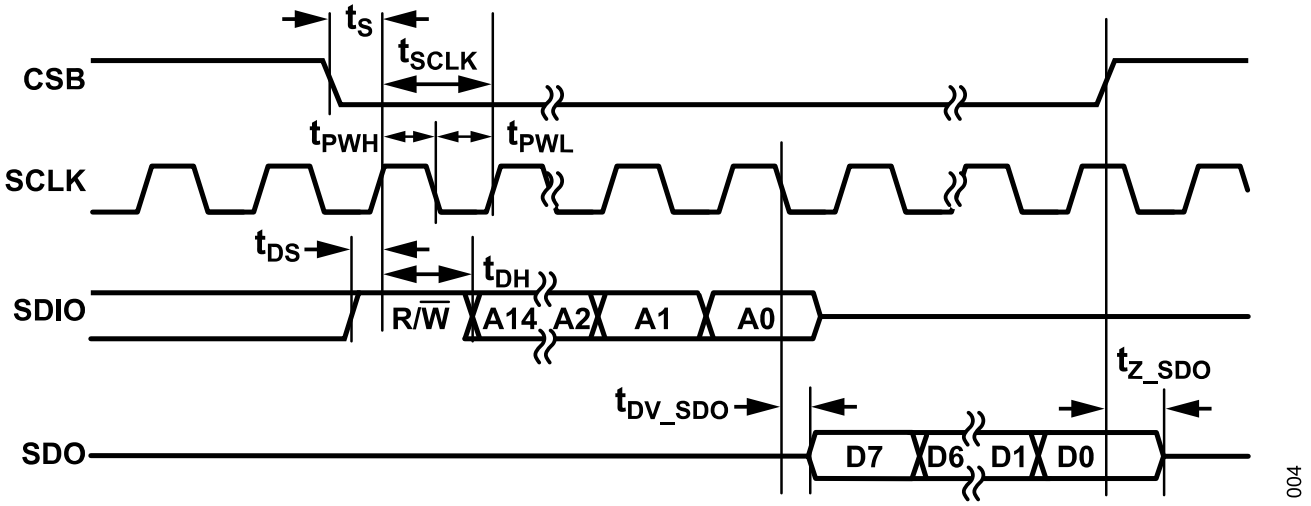

Figure 4. Timing Diagram for 4-Wire Read Operation

ABSOLUTE MAXIMUM RATINGS

Table 15.

Parameter	Rating
ISET, DACxP, DACxN	−0.3 V to AVDD2 + 0.3 V
VCO_COARSE, VCO_FINE, VCO_VCM, VCO_VREG	−0.3 V to AVDD2_PLL + 0.3 V
CLKINP, CLKINN	−0.2 V to PLLCLKVDD1 + 0.2 V
ADCDRVN, ADCDRVP	−0.2 V to CLKVDD1 + 0.2 V
SERDINx±	−0.2 V to SVDD1 + 0.2 V
SYSREFP, SYSREFN	−0.2 V to +2.5 V
SYNCxOUTB±, RESETB, TXENx, RXENx, IRQB_x, CSB, SCLK, SDIO, SDO, TMU_REFN, TMU_REFP, GPIOx	−0.3 V to DVDD1P8 + 0.3 V
AVDD2, AVDD2_PLL, SVDD2_PLL, DVDD1P8	−0.3 V to +2.2 V
PLLCLKVDD1, AVDD1, DAVDD1, DCLKVDD1, DVDD1, SVDD1, SVDD1_PLL	−0.2 V to +1.2 V
Temperature	
Maximum Junction (T_J)[1]	120°C
Storage Range	−65°C to +150°

[1] Do not exceed this temperature for any duration of time when the device is powered.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. The use of appropriate thermal management techniques is recommended to ensure that the maximum T_J does not exceed the limits shown in Table 15.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC_TOP} is the junction to case, thermal resistance.

θ_{JB} is the junction to board, thermal resistance.

Table 16. Simulated Thermal Resistance[1]

PCB Type	Airflow Velocity (m/sec)	θ_{JA}	θ_{JC_TOP}	θ_{JB}	Unit
JEDEC 2s2p Board	0.0	14.9	0.70	1.8	°C/W

[1] Thermal resistance values specified are simulated based on JEDEC specifications in compliance with JESD51-12 with the device power equal to 9 W.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

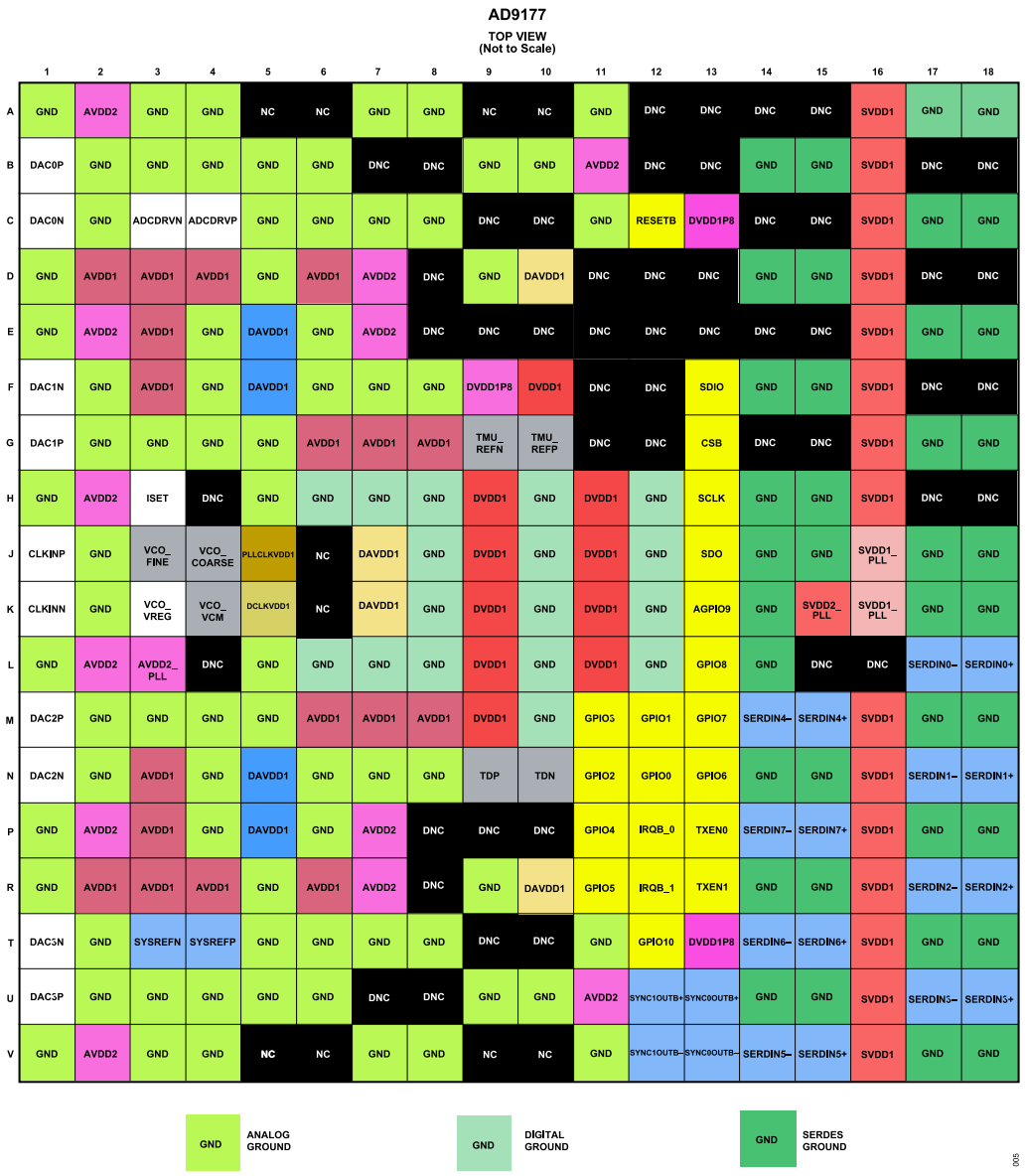

Figure 5. Pin Configuration

Table 17. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
POWER SUPPLIES			
A2, E2, H2, L2, P2, V2, D7, E7, P7, R7, B11, U11	AVDD2	Input	Analog 2.0 V Supply Inputs for DAC.
L3	AVDD2_PLL	Input	Analog 2.0 V Supply Input for Clock PLL Linear Dropout Regulator (LDO).
J5	PLLCLKVDD1	Input	Analog 1.0 V Supply Input for Clock PLL.
D2, D3, D4, E3, F3, N3, P3, R2, R3, R4, G7, G8, M7, M8, G6, M6, D6, R6	AVDD1	Input	Analog 1.0 V Supply Inputs for DAC Clock.
E5, F5, N5, P5, J7, K7, D10, R10	DAVDD1	Input	Digital Analog 1.0 V Supply Inputs.
F10, H9, H11, J9, J11, K9, K11, L9, L11, M9	DVDD1	Input	Digital 1.0 V Supply Inputs.
K5	DCLKVDD1	Input	Digital 1.0 V Clock Generation Supply.
A16, B16, C16, D16, E16, F16, G16, H16, M16, N16, P16, R16, T16, U16, V16	SVDD1	Input	Digital 1.0 V Supply Inputs for SERDES Deserializer and Serializer.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 17. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
K15	SVDD2_PLL	Input	Digital 2.0 V Supply Input for SERDES LDO.
J16, K16	SVDD1_PLL	Input	Digital 1.0 V Supply Inputs for SERDES Clock Generation and PLL.
C13, F9, T13	DVDD1P8	Input	Digital Interface and Temperature Monitoring Unit (TMU) Supply Inputs (Nominal 1.8 V).
A1, A3, A4, A7, A8, A11, A17, A18, B2 to B6, B9, B10, B14, B15, C2, C5 to C8, C11, C17, C18, D1, D5, D9, D14, D15, E1, E4, E6, E17, E18, F2, F4, F6 to F8, F14, F15, G2 to G5, G17, G18, H1, H5 to H8, H10, H12, H14, H15, J2, J8, J10, J12, J14, J15, J17, J18, K2, K8, K10, K12, K14, K17, K18, L1, L5 to L8, L10, L12, L14, M2 to M5, M10, M17, M18, N2, N4, N6 to N10, N14, N15, P1, P4, P6, P17, P18, R1, R5, R9, R14, R15, T2, T5 to T8, T11, T17, T18, U2 to U6, U9, U10, U14, U15, V1, V3, V4, V7, V8, V11, V17, V18	GND	Input/output	Ground References.
ANALOG OUTPUTS			
B1, C1	DAC0P, DAC0N	Output	DAC0 Output Currents, Ground Referenced. Tie these pins to GND if unused.
G1, F1	DAC1P, DAC1N	Output	DAC1 Output Currents, Ground Referenced. Tie these pins to GND if unused.
M1, N1	DAC2P, DAC2N	Output	DAC2 Output Currents, Ground Referenced. Tie these pins to GND if unused.
U1, T1	DAC3P, DAC3N	Output	DAC3 Output Currents, Ground Referenced. Tie these pins to GND if unused.
H3	ISET	Output	DAC Bias Current Setting Pin. Connect this pin with a 5 kΩ resistor to GND.
C4, C3	ADCDRVP, ADCDRVN	Output	Optional Clock Output (for example, ADC Clock Driver for an external ADC). These pins are disabled by default. Leave the pins floating if unused.
K3	VCO_VREG	Output	PLL LDO Regulator Output. Decouple this pin to GND with a 2.2 µF capacitor.
G9	TMU_REFN	Output	TMU ADC Negative Reference. Connect this pin to GND.
G10	TMU_REFP	Output	TMU ADC Positive Reference. Connect this pin to DVDD1P8.
ANALOG INPUTS			
J3	VCO_FINE	Input	On-Chip Device Clock Multiplier and PLL Fine Loop Filter Input. If the PLL is not in use, leave this pin floating and disable the PLL via the control registers.
J4	VCO_COARSE	Input	On-Chip Device Clock Multiplier and PLL Coarse Loop Filter Input. If the PLL is not in use, leave this pin floating and disable the PLL via the control registers.
K4	VCO_VCM	Input	On-Chip Device Clock Multiplier and VCO Common-Mode Input. If the PLL is not in use, leave this pin floating and disable the PLL via the control registers.
J1, K1	CLKINP, CLKINN	Input	Differential Clock Inputs with Nominal 100 Ω Termination. Self bias input requiring ac coupling. When the on-chip clock multiplier PLL is enabled, this input is the reference clock input. If the PLL is disabled, an RF clock equal to the DAC output sample rate is required.
CMOS INPUTS AND OUTPUTS[1]			
G13	CSB	Input	Serial Port Enable Input. Active low.
H13	SCLK	Input	Serial Plot Clock Input.
F13	SDIO	Input/output	Serial Port Bidirectional Data Input/Output.
J13	SDO	Output	Serial Port Data Output.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 17. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
C12	RESETB	Input	Active Low Reset Input. RESETB places digital logic and SPI registers in a known default state. RESETB must be connected to a digital IC that is capable of issuing a reset signal for the first step in the device initialization process.
E13, D13	RXEN0, RXEN1	Input	Active High ADC and Receive Datapath Enable Inputs. RXENx is also SPI configurable.
P13, R13	TXEN0, TXEN1	Input	Active High DAC and Transmit Datapath Enable Inputs. TXENx is also SPI configurable.
P12, R12	IRQB_0, IRQB_1	Output	Interrupt Request Outputs. These pins are open-drain, active low outputs (CMOS levels with respect to DVDD1P8). Connect a > 5 kΩ pull-up resistor to DVDD1P8 to prevent these pins from floating when unused.
M11, M12, N11, N12, P11, R11	GPIO0 to GPIO5	Input/output	General-Purpose Input or Output Pins. These pins control auxiliary functions related to the Tx datapaths.
K13, L13, M13, N13, T12	GPIO6 to GPIO10	Input/output	General-Purpose Input or Output Pins. These pins control auxiliary functions related to the Rx datapaths.
JESD204B or JESD204C COMPATIBLE SERDES DATA LANES AND CONTROL SIGNALS[2]			
L18, L17	SERDIN0+, SERDIN0−	Input	JRx Lane 0 Inputs, Data True/Complement.
N18, N17	SERDIN1+, SERDIN1−	Input	JRx Lane 1 Inputs, Data True/Complement.
R18, R17	SERDIN2+, SERDIN2−	Input	JRx Lane 2 Inputs, Data True/Complement.
U18, U17	SERDIN3+, SERDIN3−	Input	JRx Lane 3 Inputs, Data True/Complement.
M15, M14	SERDIN4+, SERDIN4−	Input	JRx Lane 4 Inputs, Data True/Complement.
V15, V14	SERDIN5+, SERDIN5−	Input	JRx Lane 5 Inputs, Data True/Complement.
T15, T14	SERDIN6+, SERDIN6−	Input	JRx Lane 6 Inputs, Data True/Complement.
P15, P14	SERDIN7+, SERDIN7−	Input	JRx Lane 7 Inputs, Data True/Complement.
U13, V13	SYNC0OUTB+, SYNC0OUTB−	Output	JRx Link 0 Synchronization Outputs for the JESD204B Interface. These pins are LVDS or CMOS configurable. These pins can also provide differential 100 Ω output impedance in LVDS mode.
U12, V12	SYNC1OUTB+, SYNC1OUTB−	Output	JRx Link 1 Synchronization Outputs for the JESD204B interface or CMOS Input to Control the Transmit Fast Frequency Hopping (FFH) Feature. For JRx link synchronization, these pins can be configured as LVDS or CMOS outputs and can provide differential 100 Ω output impedance in LVDS mode.
T4, T3	SYSREFP, SYSREFN	Input	Active High JESD204B/C System Reference Inputs. These pins are configurable for differential current mode logic (CML), PECL, and LVDS with internal 100 Ω termination or single-ended CMOS.
NO CONNECTS AND DO NOT CONNECTS			
J6, K6, A5, A6, V5, V6, A9, A10, V9, V10	NC		No Connect. These pins can be left open or connected.
H4, L4, L15, L16, U7, U8, E8 to E15, P8 to P10, R8, C9, C10, C14, C15, T9, T10, A12 to A15, H17, H18, B7, B8, B12, B13, B17, B18, D8, D11 to D13, D17, D18, F11, F12, F17, F18, G11, G12, G14, G15	DNC	DNC	Do Not Connect. The pins must be kept open.

[1] CMOS inputs do not have pull-up or pull-down resistors.

[2] SERDINx± and SERDOUTx± include 100 Ω internal termination resistors.

TYPICAL PERFORMANCE CHARACTERISTICS

DAC

The data curves represent the average performance across all outputs with harmonics and spurs falling in the first Nyquist zone (<f_{DAC}/2). All SFDR, IMD3, and NSD data measured on a laboratory evaluation board. All data for the phase noise and adjacent channel leakage ratio (ACLR) is measured on the AD9081-FMCA-EBZ customer evaluation board. For additional information on the JESD204B and JESD204C mode configurations, see the UG-1578 user guide.

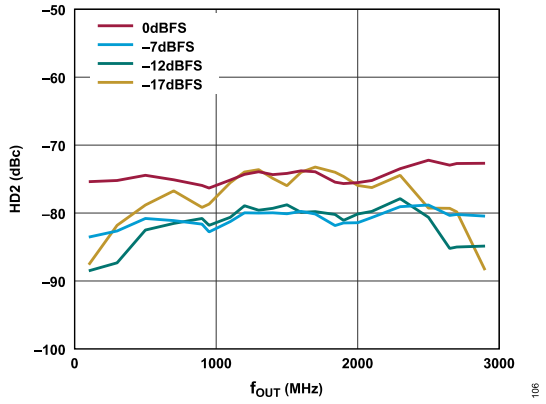

Figure 6. HD2 vs. f_{OUT} over Digital Scale, 6 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 4×, Mode 15C

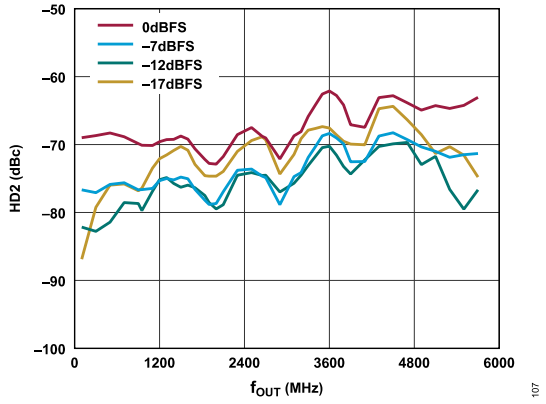

Figure 7. HD2 vs. f_{OUT} over Digital Scale, 12 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 8×, Mode 15C

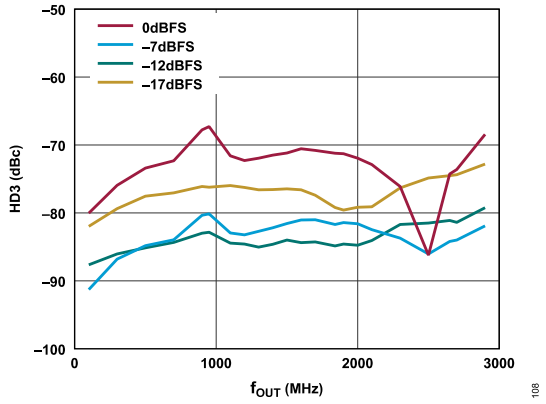

Figure 8. HD3 vs. f_{OUT} over Digital Scale, 6 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 4×, Mode 15C

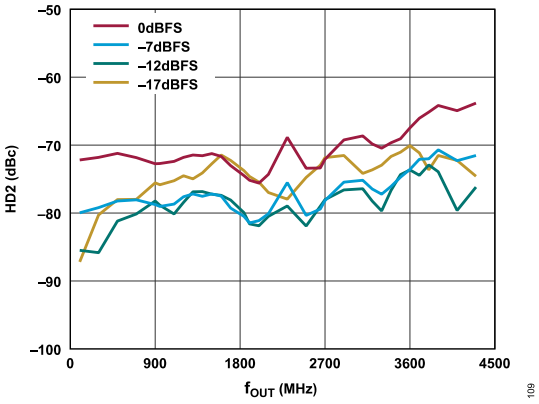

Figure 9. HD2 vs. f_{OUT} over Digital Scale, 9 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 6×, Mode 15C

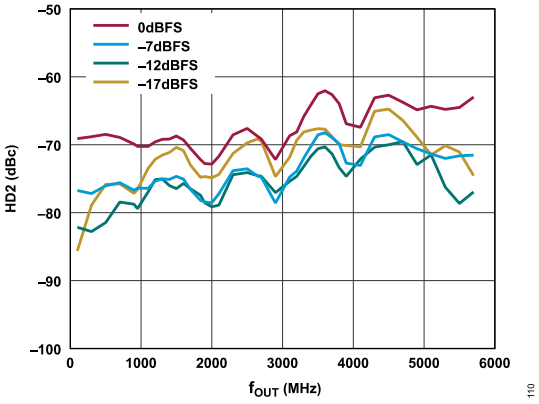

Figure 10. HD2 vs. f_{OUT} over Digital Scale, 12 GSPS DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×, Mode 16B

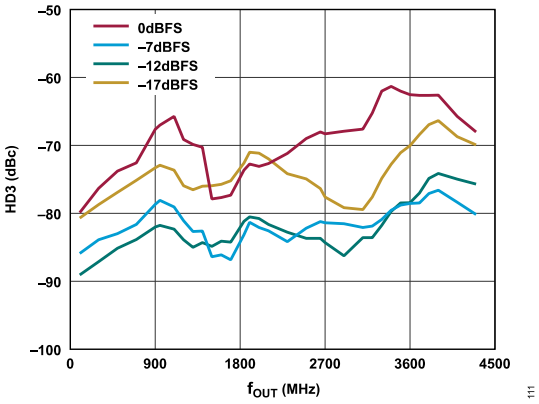

Figure 11. HD3 vs. f_{OUT} over Digital Scale, 9 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 6×, Mode 15C

TYPICAL PERFORMANCE CHARACTERISTICS

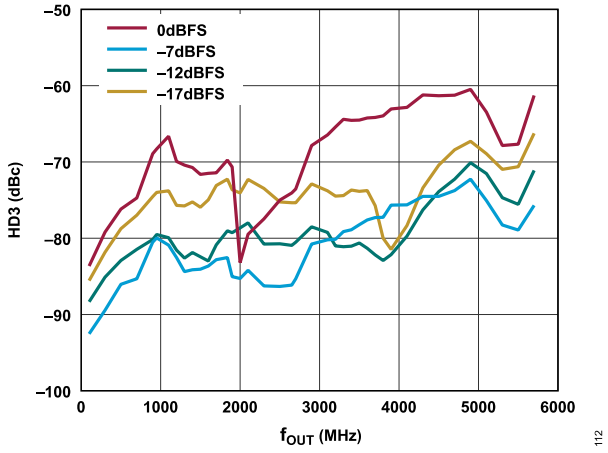

Figure 12. HD3 vs. f_{OUT} over Digital Scale, 12 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 8×, Mode 15C

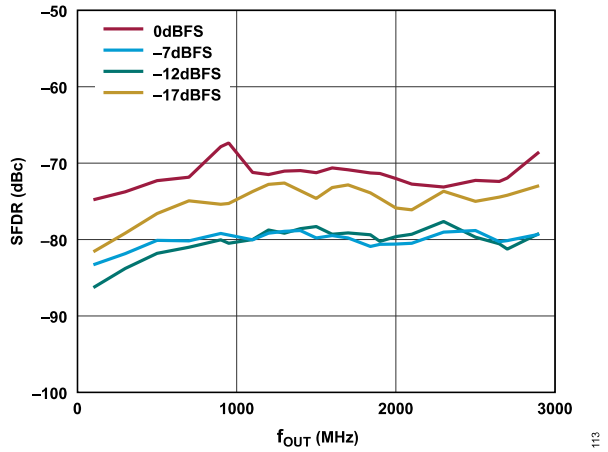

Figure 13. SFDR, Worst Spurious vs. f_{OUT} over Digital Scale, 6 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 4×, Mode 15C

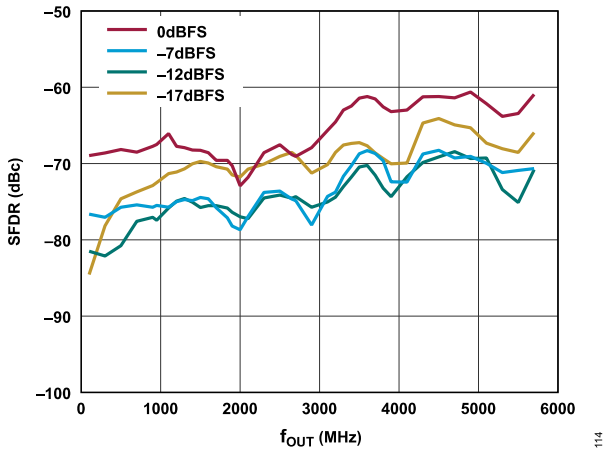

Figure 14. SFDR, Worst Spurious vs. f_{OUT} over Digital Scale, 12 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 8×, Mode 15C

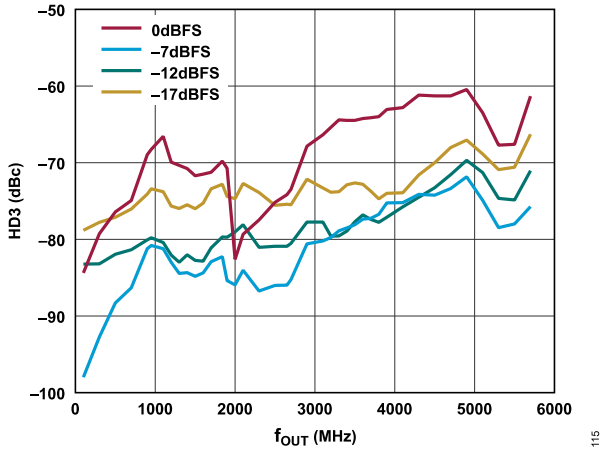

Figure 15. HD3 vs. f_{OUT} over Digital Scale, 12 GSPS DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×, Mode 16B

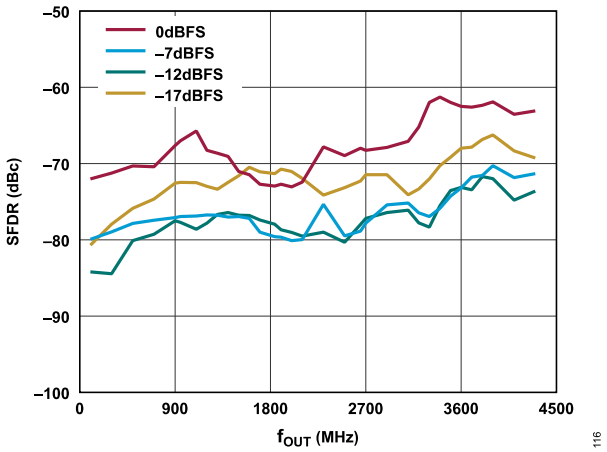

Figure 16. SFDR, Worst Spurious vs. f_{OUT} over Digital Scale, 9 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 6×, Mode 15C

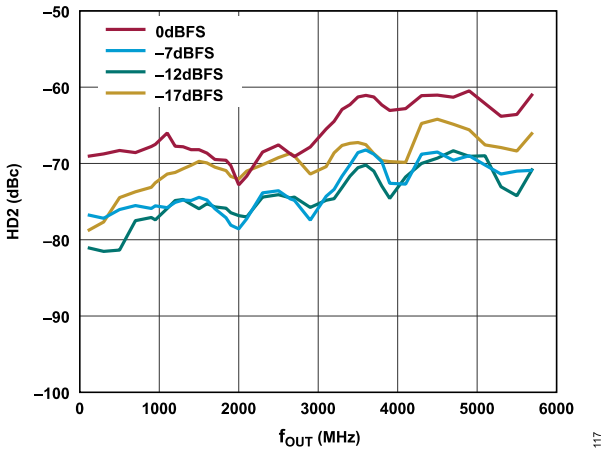

Figure 17. SFDR, Worst Spurious vs. f_{OUT} over Digital Scale, 12 GSPS DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×, Mode 16B

TYPICAL PERFORMANCE CHARACTERISTICS

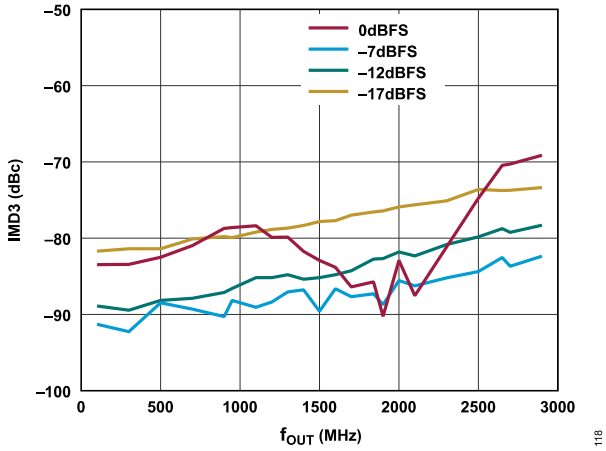

Figure 18. IMD3 vs. f_{OUT} over Digital Scale (Mode 17B), 6 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 4×, Mode 15C, IMD3 is a Two-Tone Test, and the Scale per Tone is 6 dB Lower than the Reported Digital Scale

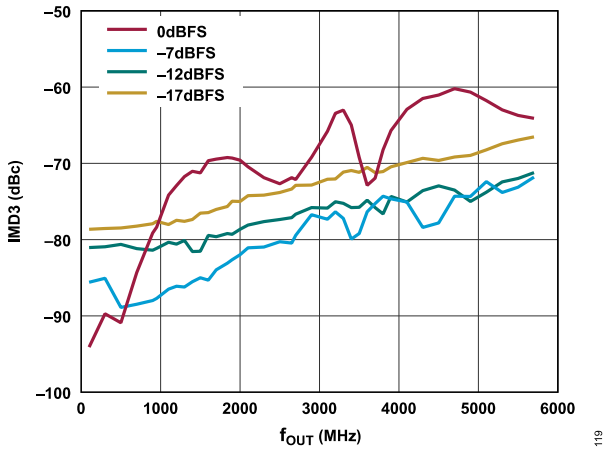

Figure 19. IMD3 vs. f_{OUT} over Digital Scale, 12 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 8×, Mode 15C, IMD3 is a Two-Tone Test, and the Scale per Tone is 6 dB Lower than the Reported Digital Scale

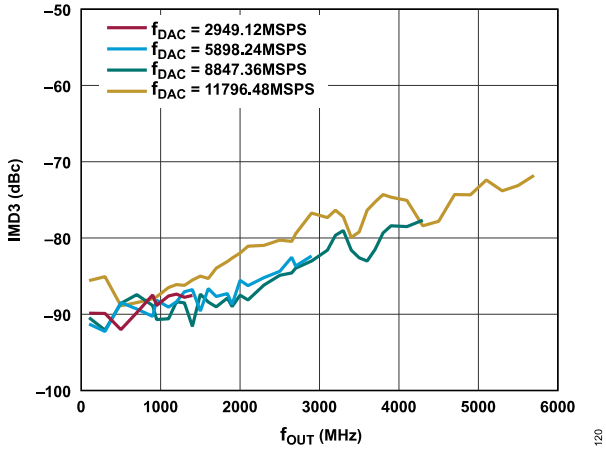

Figure 20. IMD3 vs. f_{OUT} over f_{DAC}, Digital Scale −7 dBFS, IMD3 is a Two-Tone Test, and the Scale per Tone is 6 dB Lower than the Reported Digital Scale

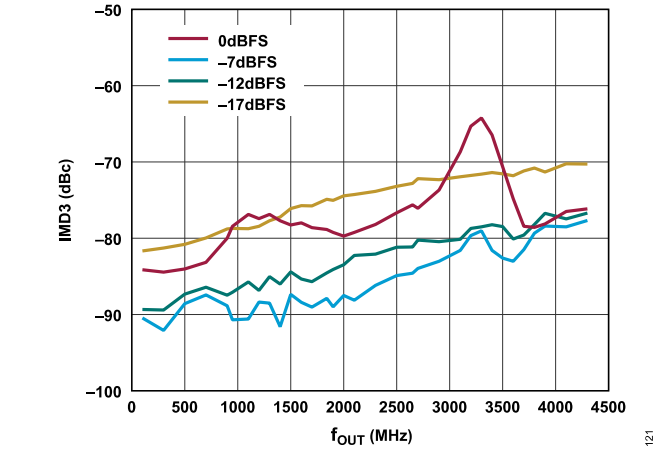

Figure 21. IMD3 vs. f_{OUT} over Digital Scale, 9 GSPS DAC Sample Rate, Channel Interpolation 1×, Main Interpolation 6×, Mode 15C, IMD3 is a Two-Tone Test, and the Scale per Tone is 6 dB Lower than the Reported Digital Scale

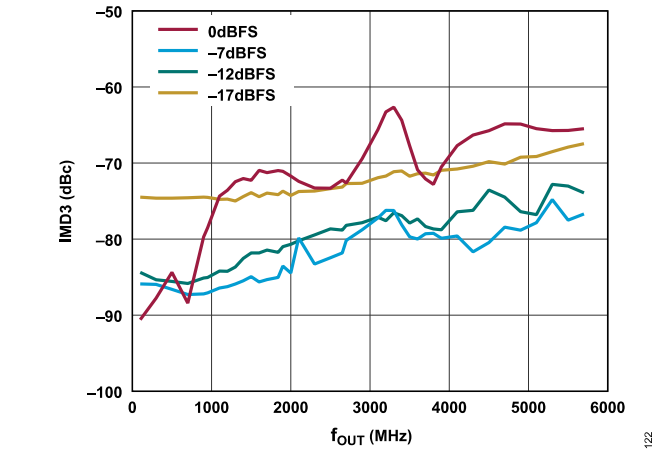

Figure 22. IMD3 vs. f_{OUT} over Digital Scale, 12 GSPS DAC Sample Rate, Channel Interpolation 4×, Main Interpolation 8×, Mode 16B, IMD3 is a Two-Tone Test, and the Scale per Tone is 6 dB Lower than the Reported Digital Scale

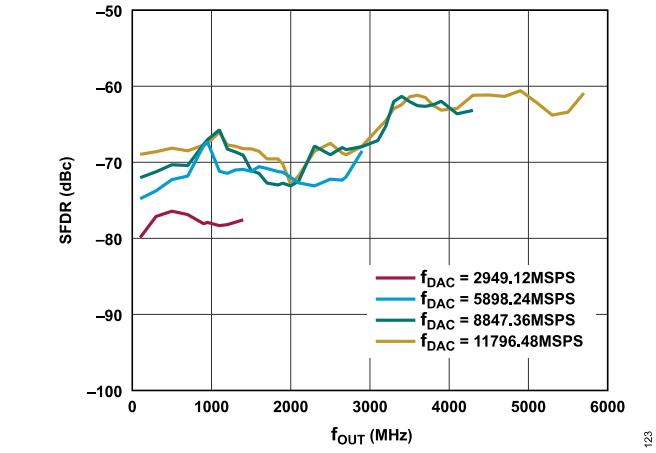

Figure 23. SFDR, Worst In-Band Spurious vs. f_{OUT} over f_{DAC}, with 0 dBFS Tone Level

TYPICAL PERFORMANCE CHARACTERISTICS

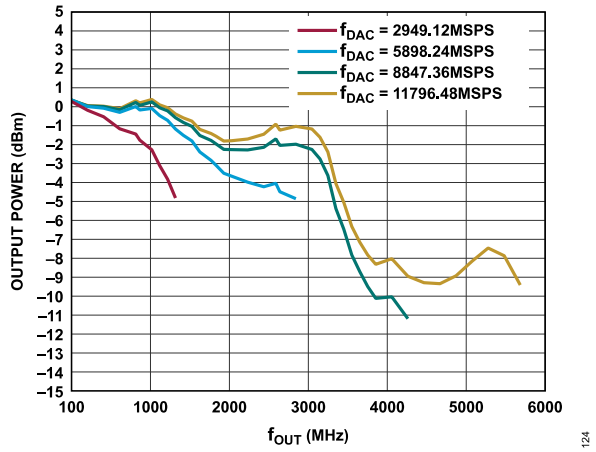

Figure 24. DAC0 Fundamental Output Power vs. f_{OUT} Across f_{DAC}, at 0 dBFS Digital Backoff, Measured on a Laboratory Evaluation Board, the AD9081-FMCA-EBZ Evaluation Board has a Different PCB Layout and Results in a Different Frequency Response when Compared to a Laboratory Evaluation Board

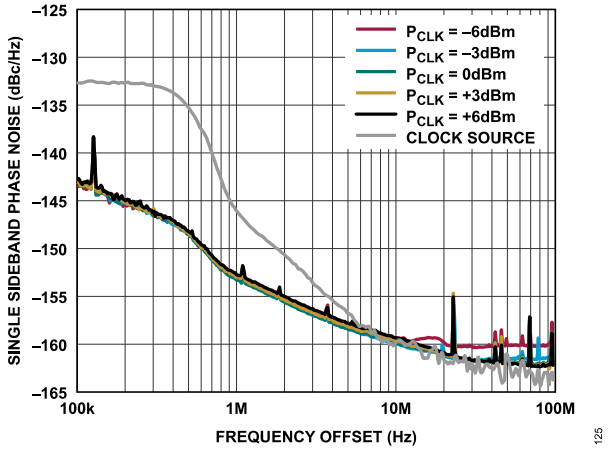

Figure 25. Single Sideband Phase Noise vs. Frequency Offset for Different Clock Input Power (P_{CLK}), f_{OUT} = 1.8 GHz, External 12 GHz Clock Input with Clock PLL Disabled

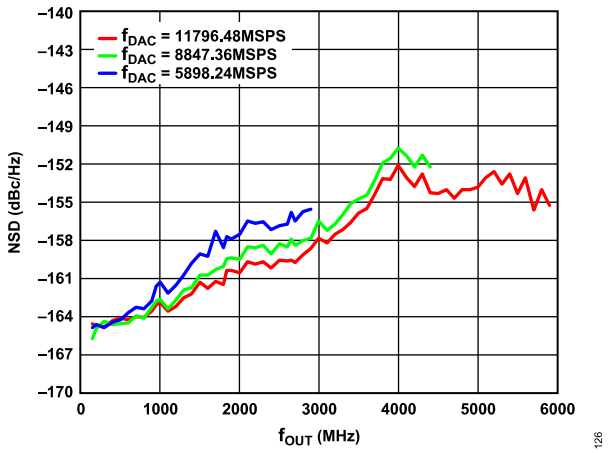

Figure 26. Single-Tone NSD Measured at 10% Offset from f_{OUT} vs. f_{OUT} over f_{DAC}, Shuffle On, 16-Bit Resolution, Mode 15C

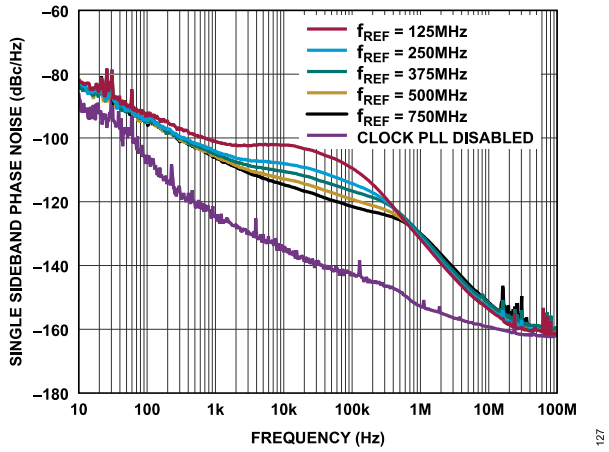

Figure 27. Single Sideband Phase Noise vs. Frequency Offset for Different PLL Reference Clocks (f_{REF}), f_{OUT} = 1.8 GHz, f_{DAC} = 12 GSPS, PLL Enabled with Exception of External 12 GHz Clock Input with Clock PLL Disabled

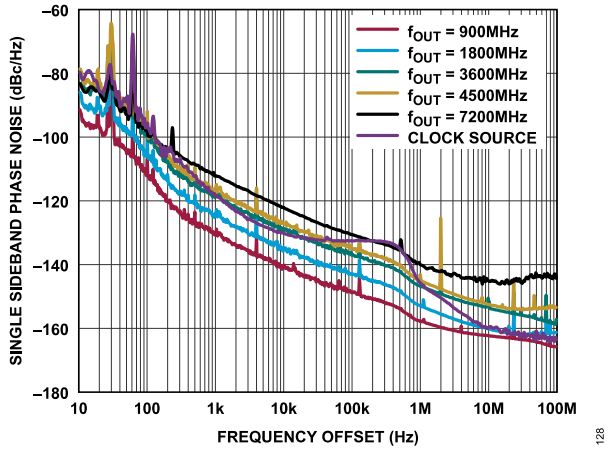

Figure 28. Single Sideband Phase Noise vs. Frequency Offset for Different DAC Output Frequencies (f_{OUT}), External 12 GHz Clock Input with Clock PLL Disabled

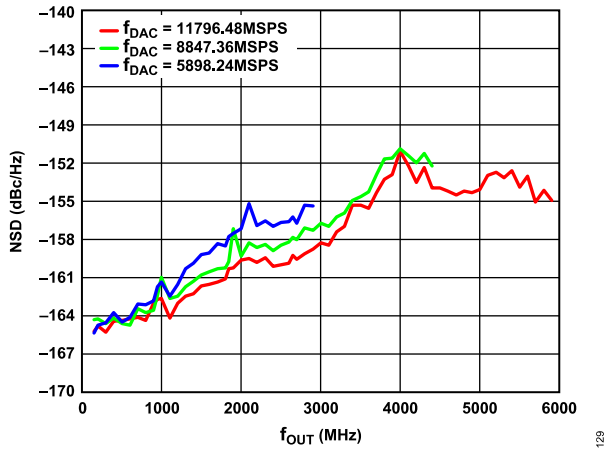

Figure 29. Single-Tone NSD Measured at 10% Offset from f_{OUT} vs. f_{OUT} over f_{DAC}, 12-Bit Resolution, Shuffle On, Mode 24C

TYPICAL PERFORMANCE CHARACTERISTICS

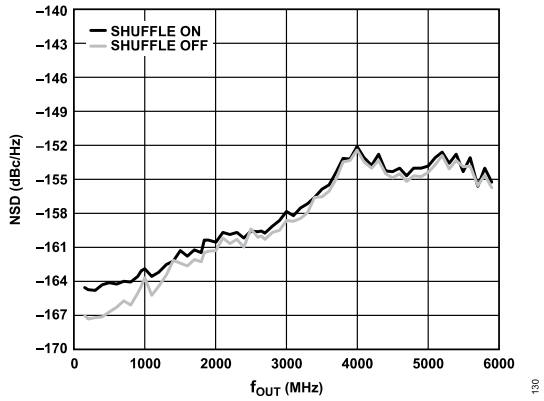

Figure 30. Single-Tone NSD Measured at 10% Offset from f_{OUT} vs. f_{OUT}, Shuffle Off vs. Shuffle On, f_{DAC} = 11796.48 MSPS, 16-Bit Resolution, Mode 15C

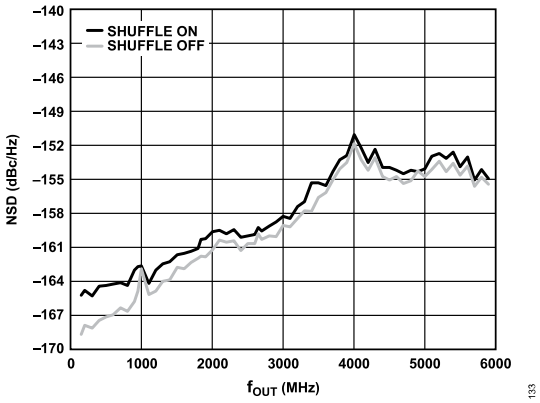

Figure 33. Single-Tone NSD Measured at 10% Offset from f_{OUT} vs. f_{OUT}, Shuffle Off vs. Shuffle On, f_{DAC} = 11796.48 MSPS, 12-Bit Resolution, Mode 24C

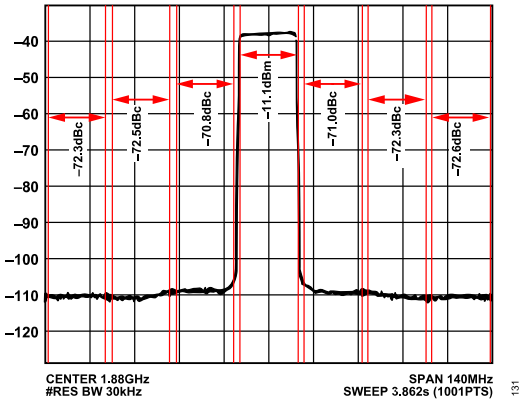

Figure 31. Dual Band ACLR Performance for Two 20 MHz LTE carriers at f_{OUT} = 1.88 GHz and f_{OUT} = 2.145 GHz (Refer to Figure 32 for a Wideband Plot), Showing a Close Up of One Carrier at f_{OUT} = 1.88 GHz, f_{DAC} = 11.796 GSPS, Test Vector PAR = 7.7 dB with −1 dBFS Backoff, Channel Interpolation 3×, Main Interpolation 8×, Mode 9C

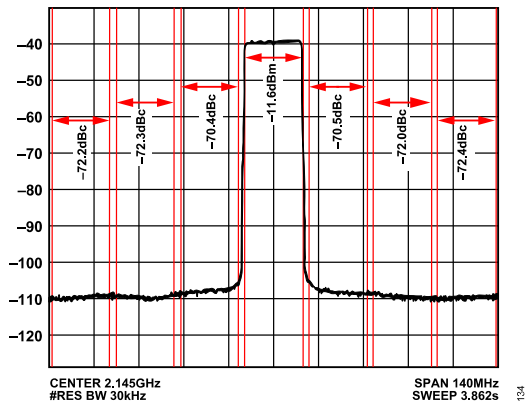

Figure 34. Dual Band ACLR Performance for two 20 MHz LTE carriers at f_{OUT} = 1.88 GHz and f_{OUT} = 2.145 GHz (Refer to Figure 32 for a Wideband Plot), Showing a Close-up of One Carrier at f_{OUT} = 2.145 GHz, f_{DAC} = 11.796 GSPS, Test Vector PAR = 7.7 dB with −1 dBFS Backoff, Channel Interpolation 3×, Main Interpolation 8×, Mode 9C

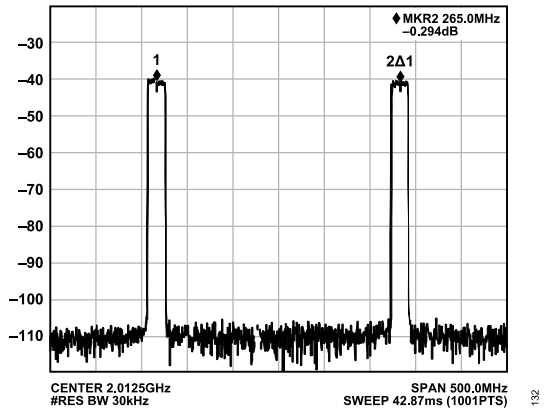

Figure 32. Dual Band Wideband Plot for Two 20 MHz LTE Carriers at f_{OUT} = 1.88 GHz and f_{OUT} = 2.145 GHz (3GPP Bands, B1 and B3, Respectively), at f_{DAC} = 11.796 GSPS, Test Vector PAR = 7.7 dB with −1 dBFS Backoff, Channel Interpolation 3×, Main Interpolation 8×, Mode 9C

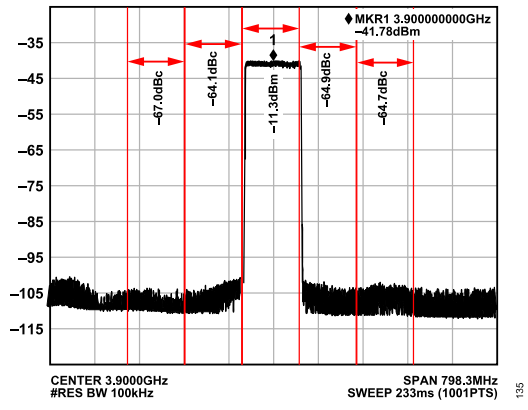

Figure 35. ACLR Performance for 100 MHz 5G Test Vector at f_{OUT} = 3.9 GHz and f_{DAC} = 11.898 GSPS, Test Vector Peak to RMS = 11.7 dB with −1 dBFS Backoff (Mode 9C), Channel Interpolation 3×, Main Interpolation 8×

THEORY OF OPERATION

The AD9177 is a highly integrated, 28 nm, RF DAC featuring four 16-bit, 12 GSPS DAC cores (see Figure 1). The DAC core is based on a current segmentation architecture providing a differential complementary current output with an adjustable I_{OUTFS} range of 6.43 mA to 37.75 mA.

An on-chip clock multiplier can be used to synthesize the RF DAC and ADC clocks or, alternatively, an external clock can be applied.

Flexible transmit DSP paths upsample the desired intermediate frequency (IF) and RF signal(s) to lower the required data interface rates and efficiently align with system bandwidth requirements. The channelizer datapath enables an efficient data transfer to allow multiband applications where up to eight unique RF bands are supported. The transmit DSP paths are symmetric and consist of four coarse DUC blocks in the main datapath along with eight fine DUC blocks in the channelizer datapath. Each DUC block includes multiple interpolation stages and a 48-bit NCO configurable for integer or fractional modes of operation. The NCO in each block supports fast frequency hopping, coherently, and can be controlled using GPIOs. The DUC blocks and the datapaths are fully bypassable to enable Nyquist operation.

Various auxiliary DSP features facilitate an improved system integration. The datapaths include adjustable delay lines to compensate for mismatch in channel delay paths that may occur external to the device. The datapaths also include digital gain control, fine delay adjust, and power amplifier (PA) protection to simplify digital pre-distortion (DPD) integration in a multiband transmitter. The datapaths also include features to reduce power consumption in time division duplex (TDD) applications. All the auxiliary DSP features are fully bypassable.

The AD9177 supports a digital loopback from an additional set of NCO blocks to the channelizer datapaths, which may be helpful in applications where extra NCOs are needed for system calibration to maintain phase coherency.

The data formatting across the datapaths can be real or complex (I/Q) with selectable resolutions of 8, 12, 16, and 24 bits depending on the JESD204B or the JESD204C mode.

An 8-lane JESD204 transmitter (JRx) port is available to support the high data throughput rates on the transmit datapath. The JRx port supports JESD204C up to 24.75 Gbps or JESD204B up to 15.5 Gbps lane rates. The JESD204 data link layer is highly flexible, allowing the user to adjust the lane count (or rate) required to support a target link throughput. An external alignment signal (SYSREF) can be used to synchronize the AD9177 to guarantee deterministic latency, NCO phase alignment, and multichip synchronization.

An on-chip thermal management unit (TMU) can be used to measure die temperature as part of a thermal management solution to guarantee better thermal stability during system operation.

APPLICATIONS INFORMATION

Refer to UG-1578, the device user guide, for more information on device initialization and other applications information.

OUTLINE DIMENSIONS

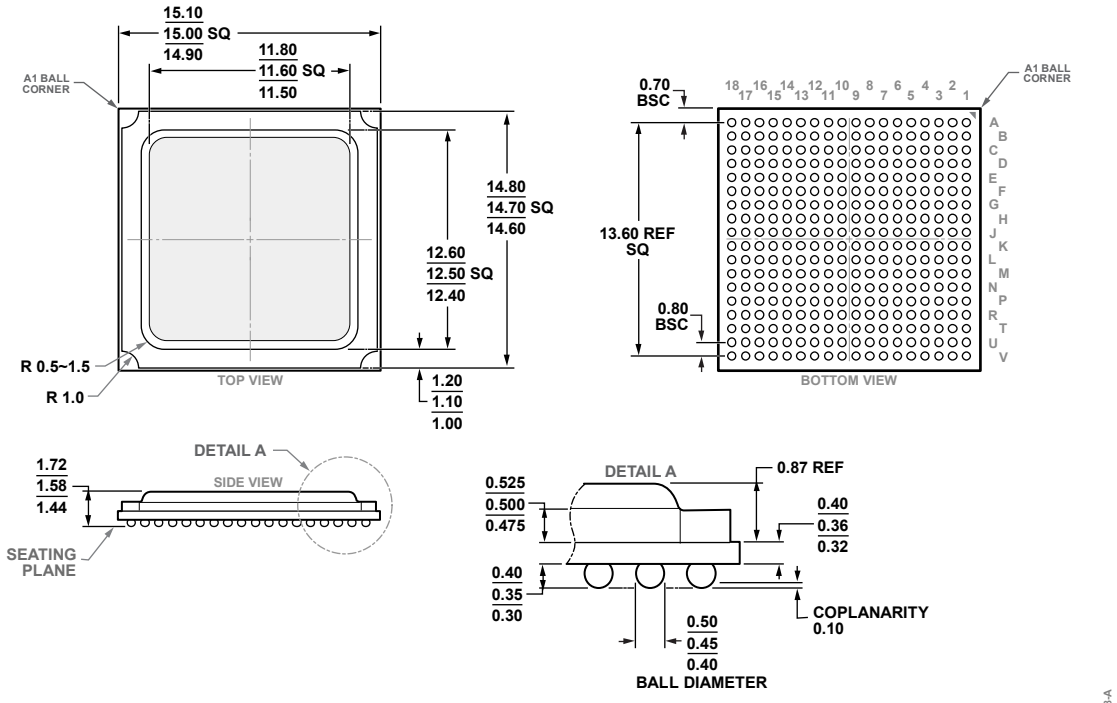

Figure 36. 324-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]
(BP-324-3)
Dimensions shown in millimeters

Updated: April 30, 2021

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD9177BBPZ	−40°C to +120°C	324-Ball BGA_ED (15 mm × 15 mm × 1.58 mm)	Tray, 126	BP-324-3
AD9177BBPZRL	−40°C to +120°C	324-Ball BGA_ED (15 mm × 15 mm × 1.58 mm)	Reel, 1000	BP-324-3

[1] Z = RoHS Compliant Part

EVALUATION BOARDS

Model[1]	Description
AD9081-FMCA-EBZ	AD9081 Evaluation Board with High Performance Analog Network

[1] The AD9081-FMCZ-EBZ is used to evaluate the AD9177.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Digital to Analog Converters - DAC ***category:***

Click to view products by Analog Devices ***manufacturer:***

Other Similar products are found below :

5962-8871903MYA 5962-8876601LA AD5311BRMZ-REEL7 AD664AJ AD7534JPZ TCC-103A-RT 057536E 5962-89657023A 702423BB TCC-202A-RT AD664BE TCC-303A-RT TCC-206A-RT AD5770RBCBZ-RL7 DAC8229FSZ-REEL AD5673RBCPZ-2 MCP48FVB24-20E/ST MCP48FVB28-E/MQ MCP48FEB18-20E/ST MCP48FEB18-E/MQ MCP48FEB24-E/MQ MCP48FEB28T-20E/ST MCP47FVB04T-E/MQ MCP48FEB28T-E/MQ MCP48FVB28T-20E/ST MCP47FVB28T-20E/ST MCP47FEB24T-E/MQ MCP48FVB24T-E/MQ MCP48FVB18T-20E/ST MCP47FEB14T-E/MQ MCP48FVB14T-20E/ST MCP48FEB08T-E/MQ MCP47FEB08T-E/MQ MCP48FVB08T-20E/ST MCP48FEB04T-20E/ST MCP47FEB04T-E/MQ MCP48FVB04T-20E/ST MCP47FVB04T-20E/ST AD7524JRZ-REEL LTC1664CGN LTC1664IGN LTC7545ACSW MCP47DA1T-A1E/OT MCP4921-E/MC UC3910D DAC39J84IAAV DAC8218SPAG DAC8562TDGSR MAX551ACUB+ MAX545BCPD+