ANALOG DEVICES

Quad PLL, Quad Input, Multiservice Line Card Adaptive Clock Translator

Data Sheet

AD9554

FEATURES

- **Supports GR-1244 Stratum 3 stability in holdover mode**
- **Supports smooth reference switchover with virtually no disturbance on output phase**
- **Supports Telcordia GR-253 jitter generation, transfer, and tolerance for SONET/SDH up to OC-192 systems**
- **Supports ITU-T G.8262 synchronous Ethernet slave clocks**
- **Supports ITU-T G.823, ITU-T G.824, ITU-T G.825, and ITU-T G.8261**
- **Auto/manual holdover and reference switchover**
- **Adaptive clocking allows dynamic adjustment of feedback dividers for use in OTN mapping/demapping applications**
- **Quad digital phase-locked loop (DPLL) architecture with four reference inputs (single-ended or differential)**
- **4 × 4 crosspoint allows any reference input to drive any PLL**
- **Input reference frequencies from 2 kHz to 1000 MHz**
- **Reference validation and frequency monitoring: 2 ppm**
- **Programmable input reference switchover priority**
- **20-bit programmable input reference divider**
- **8 differential clock outputs with each differential pair configurable as HCSL, LVDS-compatible, or LVPECL-compatible**
- **Output frequency range: 430 kHz to 941 MHz**
- **Programmable 18-bit integer and 24-bit fractional feedback divider in digital PLL**
- **Programmable loop bandwidths from 0.1 Hz to 4 kHz**
- **Optional off-chip EEPROM to store power-up profile**
- **72-lead (10 mm × 10 mm) LFCSP package**

APPLICATIONS

- **Network synchronization, including synchronous Ethernet and synchronous digital hierarchy (SDH) to optical transport network (OTN) mapping/demapping**
- **Cleanup of reference clock jitter**
- **SONET/SDH clocks up to OC-192, including FEC**
- **Stratum 3 holdover, jitter cleanup, and phase transient control**
- **Cable infrastructure**
- **Data communications**
- **Professional video**

GENERAL DESCRIPTION

The AD9554 is a low loop bandwidth clock translator that provides jitter cleanup and synchronization for many systems, including synchronous optical networks (SONET/SDH). The AD9554 generates an output clock synchronized to up to four external input references. The digital PLL (DPLL) allows for reduction of input time jitter or phase noise associated with the external references. The digitally controlled loop and holdover circuitry of the AD9554 continuously generates a low jitter output clock even when all reference inputs have failed.

The AD9554 operates over an industrial temperature range of −40°C to +85°C. If a smaller device is needed, the AD9554-1 is a version of this device with one output per PLL. If a single or dual DPLL version of this device is needed, refer to the AD9557 or AD9559, respectively.

FUNCTIONAL BLOCK DIAGRAM

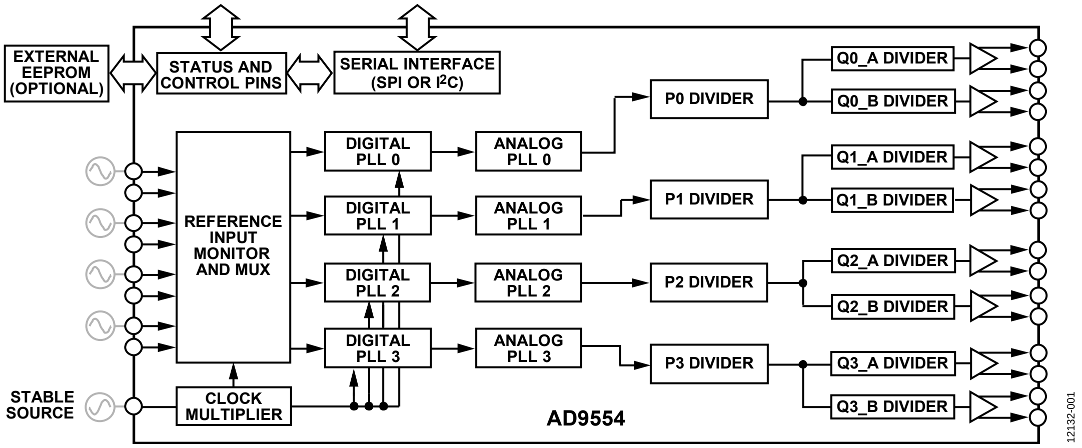

Figure 1.

Rev. D **Document Feedback**

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4/2014—Revision 0: Initial Version

SPECIFICATIONS

Minimum (min) and maximum (max) values apply for the full range of supply voltage and operating temperature variations. Typical (typ) values apply for VDD = 1.8 V, T_A = 25°C, unless otherwise noted.

SUPPLY VOLTAGE

Table 1.

Parameter	Min	Typ	Max	Unit
SUPPLY VOLTAGE for 1.8 V OPERATION				
VDD_SP	1.47	1.8	2.625	V
VDD	1.71	1.8	1.89	V
SUPPLY VOLTAGE for 1.5 V OPERATION				
VDD_SP	1.47	1.5	2.625	V
VDD	1.47	1.5	1.53	V

SUPPLY CURRENT

The test conditions for the maximum (max) supply current are at the maximum supply voltage found in Table 1. The test conditions for the typical (typ) supply current are at the typical supply voltage found in Table 1. The test conditions for the minimum (min) supply current are at the minimum supply voltage found in Table 1.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT FOR TYPICAL CONFIGURATION					Typical values are for the Typical Configuration parameter listed in Table 3; valid for both 1.5 V and 1.8 V operation
I_{VDD_SP}	0.01	0.04	0.1	mA	
I_{VDD}	430	520	575	mA	
SUPPLY CURRENT FOR ALL BLOCKS RUNNING CONFIGURATION					Maximum values are for the All Blocks Running parameter listed in Table 3; valid for both 1.5 V and 1.8 V operation
I_{VDD_SP}	0.01	0.04	0.1	mA	
I_{VDD}	615	745	780	mA	

POWER DISSIPATION

Typical (typ) values apply for VDD = 1.8 V and maximum (max) values for VDD = 1.89 V.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION					
Typical Configuration		0.94	1.1	W	System clock: 49.152 MHz crystal; four DPLLs active; two 19.44 MHz input references in differential mode; four ac-coupled output drivers in 21 mA mode at 644.53125 MHz
All Blocks Running		1.3	1.47	W	System clock: 49.152 MHz crystal; four DPLLs active, four 19.44 MHz input references in differential mode; eight ac-coupled output drivers in 28 mA mode at 750 MHz
Full Power-Down		174		mW	Measured using the Typical Configuration parameter (see Table 3) and then setting the full power down bit
Incremental Power Dissipation					Typical configuration; table values show the change in power due to the indicated operation
Complete DPLL/APLL On/Off		190		mW	Power delta computed relative to the typical configuration; the blocks powered down include one reference input, one DPLL, one APLL, one P divider, two channel dividers, and one output driver in 21 mA mode
Input Reference On/Off					
Differential (Normal Mode)		22.5		mW	f_{REF} = 19.44 MHz
Differential (DC-Coupled LVDS)		24.6		mW	f_{REF} = 19.44 MHz
Single-Ended		14.3		mW	f_{REF} = 19.44 MHz
Output Distribution Driver On/Off					
28 mA Mode (at 644.53 MHz)		70		mW	
21 mA Mode (at 644.53 MHz)		48		mW	
14 mA mode (at 644.53 MHz)		23.6		mW	

SYSTEM CLOCK INPUTS (XOA, XOB)

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYSTEM CLOCK MULTIPLIER					
PLL Output Frequency Range	2250		2415	MHz	Voltage controlled oscillator (VCO) range can place limitations on nonstandard system clock input frequencies
Phase Frequency Detector (PFD) Rate	10		300	MHz	
Frequency Multiplication Range	8		241		Assumes valid system clock and PFD rates
SYSTEM CLOCK REFERENCE INPUT PATH					System clock input must be ac-coupled
Input Frequency Range					
System Clock Input Doubler Disabled	10		268	MHz	
System Clock Input Doubler Enabled	16		150	MHz	
Minimum Input Slew Rate	250			V/µs	Minimum limit imposed for jitter performance
Self-Biased Common-Mode Voltage		0.72		V	Internally generated
Input High Voltage	0.9			V	For ac-coupled single-ended operation
Input Low Voltage			0.5	V	For ac-coupled single-ended operation
Differential Input Voltage Sensitivity	250			mV p-p	Minimum voltage across pins required to ensure switching between logic states; the instantaneous voltage on either pin must not exceed 1.14 V; single-ended input can be accommodated by ac grounding complementary input; 800 mV p-p recommended for optimal jitter performance
System Clock Input Doubler Duty Cycle					Amount of duty-cycle variation that can be tolerated on the system clock input to use the doubler
System Clock Input = 20 MHz to 150 MHz	43	50	57	%	
System Clock Input = 16 MHz to 20 MHz	47	50	53	%	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Input Capacitance		3		pF	Single-ended to ground, each pin
Input Resistance		5		kΩ	
CRYSTAL RESONATOR PATH					
Crystal Resonator Frequency Range	12		50	MHz	Fundamental mode, AT cut crystal
Input Capacitance		3		pF	Single-ended to ground, each pin
Maximum Crystal Motional Resistance			100	Ω	

REFERENCE INPUTS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL MODE					AC couple inputs in differential mode
Frequency Range					
Sinusoidal Input	10		475	MHz	
LVPECL Input	0.002		1000	MHz	
LVDS Input	0.002		700	MHz	Assumes an LVDS minimum of 494 mV p-p differential amplitude
Minimum Input Slew Rate					Minimum limit imposed for jitter performance
DPLL Loop Bandwidth = 50 Hz	40			V/μs	
DPLL Loop Bandwidth = 4 kHz	50			V/μs	Maximum loop bandwidth is f_{PFD}/50
Common-Mode Input Voltage		0.64		V	Internally generated self-bias voltage
Differential Input Voltage Sensitivity					Peak-to-peak differential voltage swing across pins required to ensure switching between logic levels as measured with a differential probe; instantaneous voltage on either pin must not exceed 1.3 V
f_{IN} < 400 MHz	400		2100	mV p-p	
f_{IN} = 400 MHz to 750 MHz	500		2100	mV p-p	
f_{IN} = 750 MHz to 1000 MHz	1000		2100	mV p-p	
Differential Input Voltage Hysteresis		55	100	mV	
Input Resistance		16		kΩ	Equivalent differential input resistance
Input Capacitance		9		pF	Single-ended to ground, each pin
Minimum Pulse Width High					
LVPECL	460			ps	
LVDS	560			ps	
Minimum Pulse Width Low					
LVPECL	460			ps	
LVDS	560			ps	
DC-COUPLED LVDS MODE					Intended for dc-coupled LVDS ≤10.24 MHz
Frequency Range	0.002		10.24	MHz	
Minimum Input Slew Rate					Minimum limit imposed for jitter performance
DPLL Loop Bandwidth = 50 Hz	40			V/μs	
DPLL Loop Bandwidth = 4 kHz	150			V/μs	Maximum loop bandwidth is f_{PFD}/50
Common-Mode Input Voltage	1.125		1.375	V	
Differential Input Voltage Sensitivity	400		1200	mV	Differential voltage across pins required to ensure switching between logic levels; instantaneous voltage on either pin must not exceed the supply rails
Differential Input Voltage Hysteresis		55	100	mV	
Input Resistance		21		kΩ	
Input Capacitance		7		pF	
Minimum Pulse Width High	25			ns	
Minimum Pulse Width Low	25			ns	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SINGLE-ENDED MODE					DC-coupled
Frequency Range (CMOS)	0.002		300	MHz	
Minimum Input Slew Rate					Minimum limit imposed for jitter performance
DPLL Loop Bandwidth = 50 Hz	40			V/µs	
DPLL Loop Bandwidth = 4 kHz	175			V/µs	Maximum loop bandwidth is f_{PFD}/50
Input Voltage High, V_{IH}	V_{DD} − 0.5			V	
Input Voltage Low, V_{IL}			0.5	V	
Input Resistance		30		kΩ	
Input Capacitance		5		pF	
Minimum Pulse Width High	1.5			ns	
Minimum Pulse Width Low	1.5			ns	

REFERENCE MONITORS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE MONITORS					
Reference Monitor					
Loss of Reference Detection Time			1.15	DPLL PFD period	Nominal phase detector period = R/f_{REF}, where R is the frequency division factor determined by the R divider, and f_{REF} is the frequency of the active reference
Frequency Out-of Range Limits	2		10^5	Δf/f_{REF} (ppm)	Programmable (lower bound subject to quality of the system clock [SYSCLK]); SYSCLK accuracy must be less than the lower bound
Validation Timer	0.001		65.535	sec	Programmable in 1 ms increments

REFERENCE SWITCHOVER SPECIFICATIONS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM OUTPUT PHASE PERTURBATION (PHASE BUILD-OUT SWITCHOVER)					Assumes a jitter-free reference; satisfies Telcordia GR-1244-CORE requirements; base loop filter selection bit set to 1b or all active references
50 Hz DPLL Loop Bandwidth					High phase margin mode; 19.44 MHz to 174.70308 MHz; DPLL bandwidth = 50 Hz; 49.152 MHz signal generator used for system clock source
Peak		±20	±130	ps	
Steady State		±20	±130	ps	
Time Required to Switch to a New Reference					
Phase Build-Out Switchover			10	DPLL PFD period	Calculated using the nominal phase detector period (NPDP = R/f_{REF}); the total time required is the time plus the reference validation time, plus the time required to lock to the new reference

DISTRIBUTION CLOCK OUTPUTS

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
14 mA (HCSL-, LVDS-COMPATIBLE) MODE					Unless otherwise stated, specifications dc-coupled with no output termination resistor; when ac-coupled, LVDS-compatible amplitudes are achieved with a 100 Ω resistor across the output pair; HCSL-compatible amplitudes achieved with no termination resistor across the output pair; output current setting: 14 mA
Output Frequency	0.430		941	MHz	Frequency range all four PLLs can generate using unique VCO frequencies; frequencies outside this range are possible on some of the PLLs, but can result in increased VCO coupling due to multiple PLLs using the same VCO frequency
Continuous Output Frequency Range	0.430		781	MHz	All four PLLs can generate this range at the same time while using unique VCO frequencies
Maximum Output Frequency					
PLL0 to PLL3 Using Unique VCO Frequencies		941		MHz	Maximum frequency all four PLLs can generate using unique VCO frequencies
PLL0, PLL1, and PLL2		1250		MHz	Limited by 1250 MHz maximum input frequency to channel divider (Q divider)
PLL3		1187		MHz	Limited by 4748 MHz maximum VCO frequency
Rise/Fall Time (20% to 80%)[1]		125	190	ps	
Duty Cycle					
Up to f_{OUT} = 750 MHz	45	50	55	%	
Up to f_{OUT} = 941 MHz	44	50	56	%	
Up to f_{OUT} = 1250 MHz		50		%	
Differential Output Voltage Swing					Differential voltage swing between output pins; measured with output driver static; peak-to-peak differential output amplitude 2× this level with driver toggling; see Figure 11 for output amplitude vs. output frequency
Without 100 Ω Termination Resistor	635	840	1000	mV	
With 100 Ω Termination Resistor Across Outputs	294	390	463	mV	
Common-Mode Output Voltage	310	420	525	mV	Output driver static; no termination resistor
Reference Input-to-Output Delay Variation over Temperature		600		fs/°C	DPLL locked to same input reference at all times; stable system clock source (noncrystal)
Static Phase Offset Variation from Active Reference to Output over Voltage Extremes		±75		fs/mV	
21 mA MODE					Unless otherwise stated, specifications dc-coupled with 50 Ω output termination resistor to ground; output current setting = 21 mA
Output Frequency	0.430		941	MHz	Frequency range all four PLLs can generate using unique VCO frequencies; frequencies outside this range are possible on some of the PLLs, but can result in increased VCO coupling due to multiple PLLs using the same VCO frequency
Continuous Output Frequency Range	0.430		781	MHz	All four PLLs can generate this range at the same time while using unique VCO frequencies
Maximum Output Frequency					
PLL0 to PLL3 Using Unique VCO Frequencies		941		MHz	Maximum frequency all four PLLs can generate using unique VCO frequencies
PLL0, PLL1, and PLL2		1250		MHz	Limited by 1250 MHz maximum input frequency to channel divider (Q divider)
PLL3		1187		MHz	Limited by 4748 MHz maximum VCO frequency
Rise/Fall Time (20% to 80%)[1]		125	190	ps	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Duty Cycle					
Up to f_{OUT} = 750 MHz	45	50	55	%	
Up to f_{OUT} = 941 MHz	44	50	56	%	
Up to f_{OUT} = 1250 MHz		50		%	
Differential Output Voltage Swing					Differential voltage swing between output pins; measured with output driver static; peak-to-peak differential output amplitude 2× this level with driver toggling; see Figure 13 for output amplitude vs. output frequency
No External Termination Resistor	779	1180	1510	mV	
With 50 Ω Termination Resistor to Ground on Each Leg	413	625	800	mV	
Common-Mode Output Voltage	206	312	400	mV	Output driver static with 50 Ω resistor to ground on each leg
Reference Input-to-Output Delay Variation over Temperature		600		fs/°C	DPLL locked to same input reference at all times; stable system clock source (noncrystal)
Static Phase Offset Variation from Active Reference to Output over Voltage Extremes		±75		fs/mV	
28 mA (LVPECL-COMPATIBLE) MODE					Specifications for dc-coupled, 50 Ω termination resistor from each leg to ground; ac coupling used in most applications; output current setting = 28 mA; in this mode, user must have either a 50 Ω resistor from each leg to ground, or a 100 Ω resistor across the differential pair
Output Frequency	0.430		941	MHz	Frequency range all four PLLs can be generated using unique VCO frequencies; frequencies outside this range are possible on some of the PLLs, but can result in increased VCO coupling due to multiple PLLs using the same VCO frequency
Continuous Output Frequency Range	0.430		781	MHz	Frequency range for each PLL such that all four PLLs are using unique VCO frequencies with no frequency gaps
Maximum Output Frequency					
PLL0 to PLL3 Using Unique VCO Frequencies		941		MHz	Maximum frequency all four PLLs can generate using unique VCO frequencies
PLL0, PLL1, and PLL2		1250		MHz	Limited by 1250 MHz maximum input frequency to channel divider (Q divider)
PLL3		1187		MHz	Limited by 4748 MHz maximum VCO frequency
Rise/Fall Time (20% to 80%)[1]		185	280	ps	
Duty Cycle					
Up to f_{OUT} = 750 MHz	45	50	55	%	
Up to f_{OUT} = 941 MHz	44	50	56	%	
Up to f_{OUT} = 1250 MHz		50		%	
Differential Output Voltage Swing	540	830	1020	mV	Differential voltage swing between output pins; measured with output driver static; peak-to-peak differential output amplitude 2× this level with driver toggling; see Figure 10 for output amplitude vs. output frequency
Common-Mode Output Voltage	275	415	510	mV	Output driver static; 50 Ω external termination resistor from each leg to ground
Reference Input-to-Output Delay Variation over Temperature		600		fs/°C	DPLL locked to same input reference at all times; stable system clock source (noncrystal)
Static Phase Offset Variation from Active Reference to Output over Voltage Extremes		±75		fs/mV	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT TIMING SKEW					Independent of output driver mode; rising edge only; any divide value; negative value means OUTxB is ahead of OUTxA
Between OUT0A, $\overline{\text{OUT0A}}$ and OUT0B, $\overline{\text{OUT0B}}$	−60	−6	+48	ps	
Between OUT1A, $\overline{\text{OUT1A}}$ and OUT1B, $\overline{\text{OUT1B}}$	−60	−6	+48	ps	
Between OUT2A, $\overline{\text{OUT2A}}$ and OUT2B, $\overline{\text{OUT2B}}$	−60	−6	+48	ps	
Between OUT3A, $\overline{\text{OUT3A}}$ and OUT3B, $\overline{\text{OUT3B}}$	−60	−6	+48	ps	

[1] The listed values are for the slower edge (rising or falling).

TIME DURATION OF DIGITAL FUNCTIONS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TIME DURATION OF DIGITAL FUNCTIONS					
EEPROM to Register Download Time		30		ms	Uses default EEPROM storage sequence (see Register 0x0E10 to Register 0x0E6F) assuming full 400 kHz throughput from EEPROM
Register to EEPROM Upload Time		Varies		ms	Value dependent on write throughput of the external EEPROM
Power-Down Exit Time		51		ms	Time from power-down exit to system clock stable (including the system clock stability timer default of 50 ms); does not include time to validate input references or lock the DPLL
Mx Pin to $\overline{\text{RESET}}$ Rising Edge Setup Time			1	ns	Mx refers to Pin M0 though Pin M9
Mx Pin to $\overline{\text{RESET}}$ Rising Edge Hold Time			1	ns	
$\overline{\text{RESET}}$ Falling Edge to Mx Pin High-Z Time			10	ns	

DIGITAL PLL (DPLL_0, DPLL_1, DPLL_2, AND DPLL_3)

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL PLL					
Phase Frequency Detector (PFD) Input Frequency Range	2		200	kHz	
Loop Bandwidth	0.1		4000	Hz	Programmable design parameter; note that (f_{PFD}/loop bandwidth) ≥ 50
Phase Margin	45		89	Degrees	Programmable design parameter
Closed Loop Peaking	<0.1			dB	Programmable design parameter; device can be programmed for <0.1 dB peaking in accordance with Telcordia GR-253-CORE jitter transfer

ANALOG PLL (APLL_0, APLL_1, APLL_2, AND APLL_3)

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG PLL0 (APLL_0)					
VCO Frequency Range	2424		3132	MHz	
Phase Frequency Detector (PFD) Input Frequency Range		320	350	MHz	The AD9554 evaluation software finds the optimal value for this setting based on user input.
Loop Bandwidth		240		kHz	
Phase Margin		68		Degrees	
ANALOG PLL1 (APLL_1)					
VCO Frequency Range	3232		3905	MHz	
Phase Frequency Detector (PFD) Input Frequency Range		320	350	MHz	The AD9554 evaluation software finds the optimal value for this setting based on user input.
Loop Bandwidth		240		kHz	
Phase Margin		68		Degrees	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG PLL2 (APLL_2)					
VCO Frequency Range	4842		5650	MHz	
Phase Frequency Detector (PFD) Input Frequency Range		320	350	MHz	The AD9554 evaluation software finds the optimal value for this setting based on user input.
Loop Bandwidth		240		kHz	
Phase Margin		68		Degrees	
ANALOG PLL3 (APLL_3)					
VCO Frequency Range	4040		4748	MHz	
Phase Frequency Detector (PFD) Input Frequency Range		320	350	MHz	The AD9554 evaluation software finds the optimal value for this setting based on user input.
Loop Bandwidth		240		kHz	
Phase Margin		68		Degrees	

DIGITAL PLL LOCK DETECTION

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PHASE LOCK DETECTOR					
Threshold Programming Range	10		$2^{24} - 1$	ps	Reference-to-feedback phase difference
Threshold Resolution		1		ps	
FREQUENCY LOCK DETECTOR					
Threshold Programming Range	10		$2^{24} - 1$	ps	Reference-to-feedback period difference
Threshold Resolution		1		ps	

HOLDOVER SPECIFICATIONS

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HOLDOVER SPECIFICATIONS					
Initial Frequency Accuracy		<0.01		ppm	Excludes frequency drift of SYSCLK source; excludes frequency drift of input reference prior to entering holdover; compliant with GR-1244 Stratum 3

SERIAL PORT SPECIFICATIONS—SERIAL PORT INTERFACE (SPI) MODE

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{\text{CS}}$					Valid for VDD_SP = 1.5 V, VDD_SP = 1.8 V, and VDD_SP = 2.5 V
Input Logic 1 Voltage	VDD_SP – 0.4			V	
Input Logic 0 Voltage			0.4	V	
Input Logic 1 Current		1		µA	
Input Logic 0 Current		1		µA	
Input Capacitance		3		pF	
SCLK					No internal pull-up or pull-down resistor
Input Logic 1 Voltage	VDD_SP – 0.4			V	
Input Logic 0 Voltage			0.4	V	
Input Logic 1 Current		1		µA	
Input Logic 0 Current		1		µA	
Input Capacitance		2		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDIO					
As an Input					
Input Logic 1 Voltage	VDD_SP – 0.4			V	
Input Logic 0 Voltage			0.4	V	
Input Logic 1 Current		1		µA	
Input Logic 0 Current		1		µA	
Input Capacitance		2		pF	
As an Output					
Output Logic 1 Voltage	VDD_SP – 0.2			V	1 mA load current
Output Logic 0 Voltage			0.1	V	1 mA load current
SDO					
Output Logic 1 Voltage	VDD_SP – 0.2			V	1 mA load current
Output Logic 0 Voltage			0.1	V	1 mA load current
High-Z Leakage Current		±6	±100	µA	
TIMING					Valid for VDD_SP = 1.5 V, VDD_SP = 1.8 V, and VDD_SP = 2.5 V
SCLK					
Clock Rate, 1/t_{CLK}			50	MHz	
Pulse Width High, t_{HIGH}	5			ns	
Pulse Width Low, t_{LOW}	8			ns	
SDIO to SCLK Setup, t_{DS}	1.5			ns	
SCLK to SDIO Hold, t_{DH}	0			ns	
SCLK to Valid SDIO and SDO, t_{DV}			8	ns	
$\overline{CS}$ to SCLK Setup, t_S	0			ns	
$\overline{CS}$ to SCLK Hold, t_C	0			ns	
$\overline{CS}$ Minimum Pulse Width High	1.5			ns	

SERIAL PORT SPECIFICATIONS—I^{2}C MODE

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL (AS INPUTS)					Valid for VDD_SP = 1.5 V, VDD_SP = 1.8 V, and VDD_SP = 2.5 V
Input Logic 1 Voltage	0.7 × VDD_SP			V	
Input Logic 0 Voltage			0.3 × VDD_SP	V	
Input Current	−10		+10	µA	For V_{IN} = 10% to 90% of VDD
Hysteresis of Schmitt Trigger Inputs	0.015 × VDD				
SDA (AS OUTPUT)					
Output Logic 0 Voltage			0.2	V	I_{OUT} = 3 mA
Output Fall Time from V_{IH} Minimum to V_{IL} Maximum	20 + 0.1 × C_b		250	ns	10 pF ≤ C_b ≤ 400 pF
TIMING					
SCL Clock Rate			400	kHz	
Bus-Free Time Between a Stop and Start Condition, t_{BUF}	1.3			µs	
Repeated Start Condition Setup Time, $t_{SU; STA}$	0.6			µs	
Repeated Hold Time Start Condition, $t_{HD; STA}$	0.6			µs	After this period, the first clock pulse is generated
Stop Condition Setup Time, $t_{SU; STO}$	0.6			µs	
Low Period of the SCL Clock, t_{LOW}	1.3			µs	
High Period of the SCL Clock, t_{HIGH}	0.6			µs	
SCL/SDA Rise Time, t_R	20 + 0.1 × C_b		300	ns	
SCL/SDA Fall Time, t_F	20 + 0.1 × C_b		300	ns	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Data Setup Time, $t_{SU; DAT}$	100			ns	
Data Hold Time, $t_{HD; DAT}$	100			ns	
Capacitive Load for Each Bus Line, C_b			400	pF	

LOGIC INPUTS ($\overline{\text{RESET}}$, M9 TO M0)

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{\text{RESET}}$ PIN					Valid for VDD_SP = 1.5 V, VDD_SP = 1.8 V, and VDD_SP = 2.5 V
Input High Voltage (V_{IH})	VDD_SP −0.5			V	
Input Low Voltage (V_{IL})			0.5	V	
Input Current (I_{INH}, I_{INL})		±85	±125	µA	
Input Capacitance (C_{IN})		3		pF	
LOGIC INPUTS (M9 to M0)					Valid for VDD = 1.5 V, and VDD = 1.8 V
Input High Voltage (V_{IH})	VDD − 0.5			V	
Input Low Voltage (V_{IL})			0.6	V	
Input Current (I_{INH}, I_{INL})		±15	±25	µA	
Input Capacitance (C_{IN})		5		pF	

LOGIC OUTPUTS (M9 TO M0)

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (M9 to M0)					VDD = 1.5 V and VDD = 1.8 V
Output High Voltage (V_{OH})	VDD − 0.2			V	I_{OH} = 1 mA using high drive strength (see Register 0x011E)
Output Low Voltage (V_{OL})			0.2	V	I_{OL} = 1 mA

JITTER GENERATION

Jitter Generation (Random Jitter)—49.152 MHz Crystal for System Clock Input

Table 18.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					System clock doubler enabled; high phase margin mode enabled; all PLLs are running with same output frequency; in cases where the four PLLs have different jitter, the higher jitter is listed; there is not a significant jitter difference between driver modes
f_{REF} = 19.44 MHz; f_{OUT} = 622.08 MHz; f_{LOOP} = 50 Hz					
Bandwidth					
5 kHz to 20 MHz		381		fs rms	
12 kHz to 20 MHz		375		fs rms	
20 kHz to 80 MHz		380		fs rms	
50 kHz to 80 MHz		365		fs rms	
4 MHz to 80 MHz		116		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 644.53 MHz; f_{LOOP} = 50 Hz					
Bandwidth					
5 kHz to 20 MHz		388		fs rms	
12 kHz to 20 MHz		381		fs rms	
20 kHz to 80 MHz		385		fs rms	
50 kHz to 80 MHz		368		fs rms	
4 MHz to 80 MHz		106		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 693.48 MHz; f_{LOOP} = 50 Hz					
Bandwidth					
5 kHz to 20 MHz		433		fs rms	
12 kHz to 20 MHz		427		fs rms	
20 kHz to 80 MHz		432		fs rms	
50 kHz to 80 MHz		419		fs rms	
4 MHz to 80 MHz		120		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 156.25 MHz; f_{LOOP} = 50 Hz					
Bandwidth					
5 kHz to 20 MHz		420		fs rms	
12 kHz to 20 MHz		414		fs rms	
20 kHz to 80 MHz		461		fs rms	
50 kHz to 80 MHz		449		fs rms	
4 MHz to 80 MHz		260		fs rms	
f_{REF} = 19.44 MHz; f_{OUT} = 174.703 MHz; f_{LOOP} = 50 Hz					
Bandwidth					
5 kHz to 20 MHz		398		fs rms	
12 kHz to 20 MHz		393		fs rms	
20 kHz to 80 MHz		439		fs rms	
50 kHz to 80 MHz		427		fs rms	
4 MHz to 80 MHz		231		fs rms	
f_{REF} = 25 MHz; f_{OUT} = 161.1328 MHz; f_{LOOP} = 100 Hz					
Bandwidth					
5 kHz to 20 MHz		385		fs rms	
12 kHz to 20 MHz		379		fs rms	
20 kHz to 80 MHz		423		fs rms	
50 kHz to 80 MHz		412		fs rms	
4 MHz to 80 MHz		250		fs rms	

ABSOLUTE MAXIMUM RATINGS

Table 19.

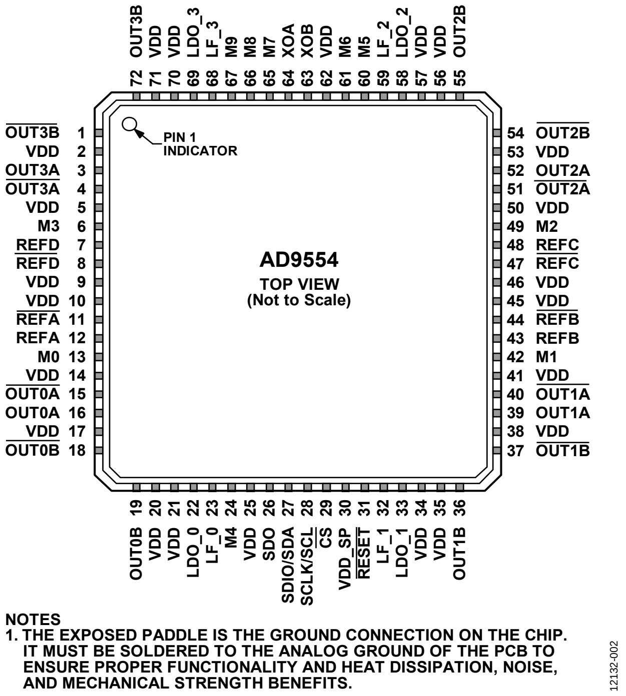
Parameter	Rating
1.8 V Supply Voltage (VDD)	2 V
Serial Port Supply Voltage (VDD_SP)	2.75 V
Maximum Digital Input Voltage Range	−0.5 V to VDD + 0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	115°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PADDLE IS THE GROUND CONNECTION ON THE CHIP. IT MUST BE SOLDERED TO THE ANALOG GROUND OF THE PCB TO ENSURE PROPER FUNCTIONALITY AND HEAT DISSIPATION, NOISE, AND MECHANICAL STRENGTH BENEFITS.

Figure 2. Pin Configuration

Table 20. Pin Function Descriptions

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
1	$\overline{\text{OUT3B}}$	O	HCSL, LVDS-compatible, LVPECL-Compatible	PLL3 Complementary Output 3B. Complementary signal to the output provided on Pin 72 (OUT3B).
2, 5, 9, 10, 14, 17, 20, 21, 25, 34, 35, 38, 41, 45, 46, 50, 53, 56, 57, 62, 70, 71	VDD	I	Power	1.5 V or 1.8 V Power Supply. See the Power Supply Partitions section for information about the recommended grouping of the power supply pins.
3	OUT3A	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL3 Output 3A. This HCSL output can be configured as a LVDS- or LVPECL-compatible output. LVPECL and LVDS levels can be achieved by ac coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.
4	$\overline{\text{OUT3A}}$	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL3 Complementary Output 3A. Complementary signal to the output provided on Pin 3 (OUT3A).
6, 13, 42, 49	M3, M0, M1, M2	I/O	1.5 V/1.8 V CMOS	Configurable Input/Output Pins. These pins are used for status and control of the AD9554. These pins are also used at power-up and reset to control the optional external EEPROM. See the Multifunction Pins at Reset/Power-Up section for more information about the internal 100 kΩ pull-up or pull-down resistors. These pins are on the VDD power domain (Pin 9, Pin 10, Pin 45, and Pin 46), and the logic high voltage for this pin matches the voltage of the VDD pins.
7	REFD	I	Differential input	Reference D Input. This internally biased input is typically ac-coupled; when configured in this manner, it can accept any differential signal with single-ended swing up to the VDD power supply. If dc-coupled, the input can be LVDS or single-ended CMOS provided that $V_{IH} \leq$ VDD.

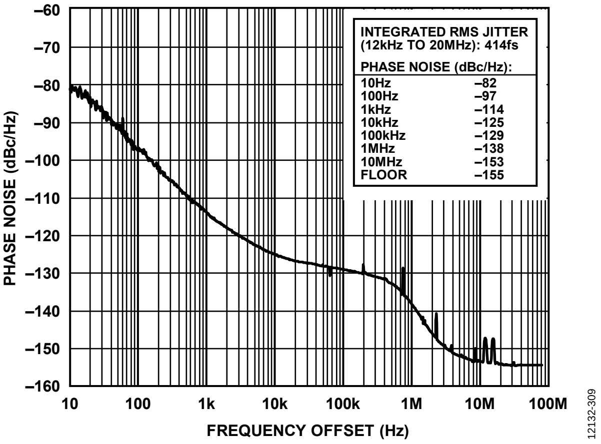
Pin No.	Mnemonic	Input/ Output	Pin Type	Description
8	$\overline{\text{REFD}}$	I	Differential input	Complementary Reference D Input. Complementary signal to the input provided on Pin 7 (REFD). This pin can be left floating if REFD is a single-ended input or if REFD is not used.
11	$\overline{\text{REFA}}$	I	Differential input	Complementary Reference A Input. Complementary signal to the input provided on Pin 12 (REFA). This pin can be left floating if REFA is a single-ended input or if REFA is not used.
12	REFA	I	Differential input	Reference A Input. This internally biased input is typically ac-coupled; when configured in this manner, it can accept any differential signal with single-ended swing up to the VDD power supply. If dc-coupled, the input can be LVDS or single-ended CMOS provided that $V_{IH} \leq$ VDD.
15	$\overline{\text{OUT0A}}$	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL0 Complementary Output 0A. Complementary signal to the output provided on Pin 16 (OUT0A).
16	OUT0A	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL0 Output 0A. This HCSL output can be configured as a LVDS- or LVPECL-compatible output. LVPECL and LVDS levels can be achieved by ac-coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.
18	$\overline{\text{OUT0B}}$	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL0 Complementary Output 0B. Complementary signal to the output provided on Pin 19 (OUT0A).
19	OUT0B	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL0 Output 0B. This HCSL output can be configured as a LVDS- or LVPECL-compatible output. LVPECL and LVDS levels can be achieved by ac-coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.
22	LDO_0	I	LDO bypass	APLL_0 Loop Filter Voltage Regulator. Connect a 0.22 µF capacitor from this pin to ground. This pin is also the ac ground reference for the integrated APLL_0 external loop filter.
23	LF_0	I/O	Loop filter for APLL_0	Loop Filter Node for the APLL_0. Connect an external 15 nF capacitor from this pin to Pin 22 (LDO_0).
24	M4	I/O	1.5 V/1.8 V CMOS	Configurable Input/Output Pin. This pin is used for status and control of the AD9554. At power-up and reset this pin controls whether or not the M1 and M2 pins are used for the serial port connection to the optional external EEPROM. See the Multifunction Pins at Reset/Power-Up section for more information about internal 100 kΩ pull-up or pull-down resistors. This pin is on the VDD power domain, and the logic high voltage for this pin matches the voltage of the VDD pins.
26	SDO	O	CMOS	Serial Data Output (SDO). In 4-wire SPI mode, this pin is used for reading serial data. The V_{IH}/V_{OH} of this pin tracks the VDD_SP power supply, which can be 1.5 V, 1.8 V, or 2.5 V.
27	SDIO/SDA	I/O	CMOS	In SPI mode, this is the serial data input/output (SDIO) pin. In 4-wire SPI mode, data is written via this pin. In 3-wire SPI mode, data reads and writes both occur on this pin. In I^{2}C mode, this is the serial data pin (SDA) pin. There is no internal pull-up/pull-down resistor on this pin. The V_{IH}/V_{OH} of this pin tracks the VDD_SP power supply, which can be 1.5 V, 1.8 V, or 2.5 V.
28	SCLK/SCL	I	CMOS	In SPI mode, this is the serial programming clock (SCLK) pin. In I^{2}C mode, this is the serial clock pin (SCL). The V_{IH}/V_{OH} of this pin tracks the VDD_SP power supply, which can be 1.5 V, 1.8 V, or 2.5 V.
29	$\overline{\text{CS}}$	I	CMOS	Chip Select in SPI Mode ($\overline{\text{CS}}$). Active low input. When programming a device in SPI, this pin must be held low. In systems where more than one AD9554 is present, this pin enables individual programming of each AD9554. This pin has an internal 10 kΩ pull-up resistor. The V_{IH} of this pin tracks the VDD_SP power supply, which can be 1.5 V, 1.8 V, or 2.5 V.
30	VDD_SP	I	Power	Serial Port Power Supply. The power supply can be 1.5 V, 1.8 V, or 2.5 V. If this pin is at the same voltage as VDD, it can be connected to VDD pins.
31	$\overline{\text{RESET}}$	I	1.5 V/1.8 V/ 2.5 V CMOS	Chip Reset. When this active low pin is asserted, the chip goes into reset. This pin has an internal 50 kΩ pull-up resistor. The V_{IH} of this pin tracks the VDD_SP power supply, which can be 1.5 V, 1.8 V, or 2.5 V.

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
32	LF_1	I/O	Loop filter for APLL_1	Loop Filter Node for the APLL_1. Connect an external 15 nF capacitor from this pin to Pin 33 (LDO_1).
33	LDO_1	I	LDO bypass	APLL_1 Loop Filter Voltage Regulator. Connect a 0.22 µF capacitor from this pin to ground. This pin is also the ac ground reference for the integrated APLL_1 external loop filter.
36	OUT1B	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL1 Output 1B. This HCSL output can be configured as a LVDS- or LVPECL-compatible output. LVPECL and LVDS levels can be achieved by ac-coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.
37	$\overline{\text{OUT1B}}$	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL1 Complementary Output 1B. Complementary signal to the output provided on Pin 36 (OUT1B).
39	OUT1A	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL1 Output 1A. This HCSL output can be configured as a LVDS- or LVPECL-compatible output. LVPECL and LVDS levels can be achieved by ac-coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.
40	$\overline{\text{OUT1A}}$	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL1 Complementary Output 1A. Complementary signal to the output provided on Pin 39 (OUT1A).
43	REFB	I	Differential input	Reference B Input. This internally biased input is typically ac-coupled; when configured in this manner, it can accept any differential signal with single-ended swing up to the VDD power supply. If dc-coupled, the input can be LVDS or single-ended CMOS provided that $V_{IH} \leq$ VDD.
44	$\overline{\text{REFB}}$	I	Differential input	Complementary Reference B Input. Complementary signal to the input provided on Pin 43 (REFB). This pin can be left floating if REFB is a single-ended input, or if REFB is not used.
47	$\overline{\text{REFC}}$	I	Differential input	Complementary Reference C Input. Complementary signal to the input provided on Pin 48 (REFC). This pin can be left floating if REFC is a single-ended input, or if REFC is not used.
48	REFC	I	Differential input	Reference C Input. This internally biased input is typically ac-coupled; when configured in this manner, it can accept any differential signal with single-ended swing up to the VDD power supply. If dc-coupled, the input can be LVDS or single-ended CMOS provided that $V_{IH} \leq$ VDD.
51	$\overline{\text{OUT2A}}$	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL2 Complementary Output 2A. Complementary signal to the output provided on Pin 52 (OUT2A).
52	OUT2A	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL2 Output 2A. This HCSL output can be configured as a LVDS- or LVPECL-compatible output. LVPECL and LVDS levels can be achieved by ac-coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.
54	$\overline{\text{OUT2B}}$	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL2 Complementary Output 2B. Complementary signal to the output provided on Pin 55 (OUT2B).
55	OUT2B	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL2 Output 2B. This HCSL output can be configured as a LVDS- or LVPECL-compatible output. LVPECL and LVDS levels can be achieved by ac-coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.
58	LDO_2	I	LDO bypass	APLL_2 Loop Filter Voltage Regulator. Connect a 0.22 µF capacitor from this pin to ground. This pin is also the ac ground reference for the integrated APLL_2 external loop filter.
59	LF_2	I/O	Loop filter for APLL_2	Loop Filter Node for the APLL_2. Connect an external 15 nF capacitor from this pin to Pin 58 (LDO_2).

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
60, 61, 65, 66, 67	M5, M6, M7, M8, M9	I/O	1.5 V/1.8 V CMOS	Configurable Input/Output Pins. These pins are used for status and control of the AD9554. These pins are also used at power-up and reset to determine the serial port and address. See the Multifunction Pins at Reset/Power-Up section for more information about the internal 100 kΩ pull-up or pull-down resistors. These pins are on the VDD digital power domain (Pin 62), and the logic high voltage for this pin matches the voltage of the VDD pins.
63	XOB	I	Differential input	Complementary System Clock Input. Complementary signal to XOA. XOB contains internal dc biasing and must be ac-coupled with a 0.1 µF capacitor except when using a crystal. When a crystal is used, connect the crystal across XOA and XOB.
64	XOA	I	Differential input	System Clock Input. XOA contains internal dc biasing and must be ac-coupled with a 0.1 µF capacitor except when using a crystal. When a crystal is used, connect the crystal across XOA and XOB. Single-ended CMOS is also an option, but a spur may be introduced if the duty cycle is not 50%. When using XOA as a single-ended input, connect a 0.1 µF capacitor from XOB to ground.
68	LF_3	I/O	Loop filter for APLL_3	Loop Filter Node for the APLL_3. Connect an external 15 nF capacitor from this pin to Pin 69 (LDO_3).
69	LDO_3	I	LDO bypass	APLL_3 Loop Filter Voltage Regulator. Connect a 0.22 µF capacitor from this pin to ground. This pin is also the ac ground reference for the integrated APLL_3 external loop filter.
72	OUT3B	O	HCSL, LVDS-compatible, LVPECL-compatible	PLL3 Output 3B. This HCSL output can be configured as a LVDS- or LVPECL-compatible output. LVPECL and LVDS levels can be achieved by ac-coupling and using the Thevenin equivalent termination as described in the Input/Output Termination Recommendations section.
0	EPAD	GND	Exposed pad	The exposed pad is the ground connection on the chip. It must be soldered to the analog ground of the printed circuit board (PCB) to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits.

TYPICAL PERFORMANCE CHARACTERISTICS

f_R = input reference clock frequency, f_{OUT} = output clock frequency, f_{SYS} = SYSCLK input frequency, and VDD at 1.8 V.

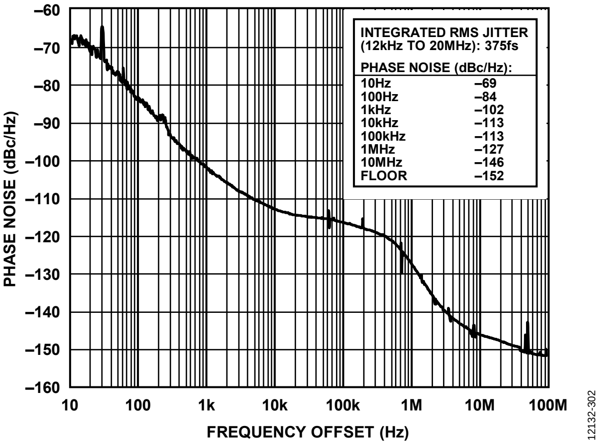


INTEGRATED RMS JITTER (12kHz TO 20MHz): 414fs

PHASE NOISE (dBc/Hz):

10Hz	–82
100Hz	–97
1kHz	–114
10kHz	–125
100kHz	–129
1MHz	–138
10MHz	–153
FLOOR	–155

Figure 3. Absolute Phase Noise (Output Driver = 21 mA Mode), f_R = 19.44 MHz, f_{OUT} = 156.25 MHz, DPLL Loop Bandwidth = 50 Hz, f_{SYS} = 49.152 MHz Crystal

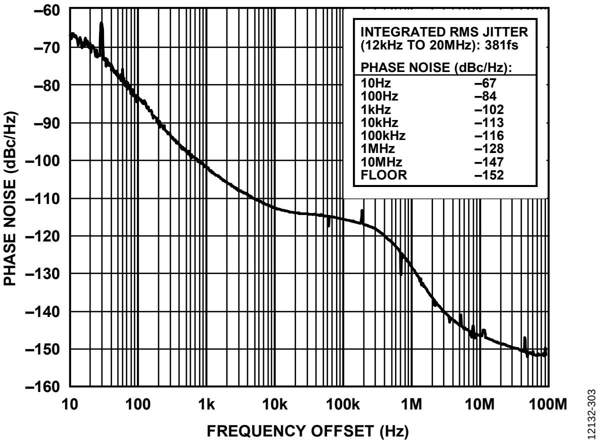


INTEGRATED RMS JITTER (12kHz TO 20MHz): 375fs

PHASE NOISE (dBc/Hz):

10Hz	–69
100Hz	–84
1kHz	–102
10kHz	–113
100kHz	–113
1MHz	–127
10MHz	–146
FLOOR	–152

Figure 4. Absolute Phase Noise (Output Driver = 21 mA Mode), f_R = 19.44 MHz, f_{OUT} = 622.08 MHz, DPLL Loop Bandwidth = 50 Hz, f_{SYS} = 49.152 MHz Crystal

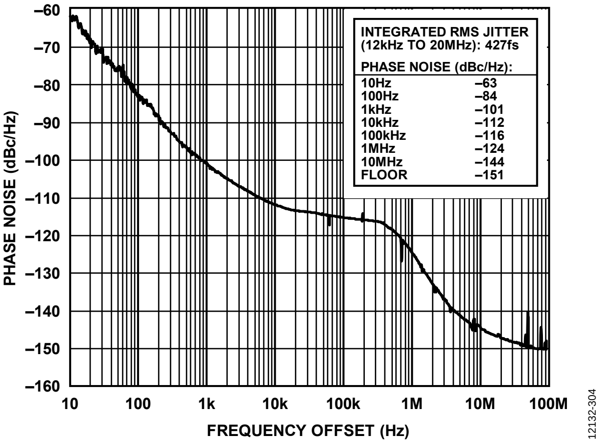


INTEGRATED RMS JITTER (12kHz TO 20MHz): 381fs

PHASE NOISE (dBc/Hz):

10Hz	–67
100Hz	–84
1kHz	–102
10kHz	–113
100kHz	–116
1MHz	–128
10MHz	–147
FLOOR	–152

Figure 5. Absolute Phase Noise (Output Driver = 21 mA Mode), f_R = 19.44 MHz, f_{OUT} = 644.53125 MHz, DPLL Loop Bandwidth = 50 Hz, f_{SYS} = 49.152 MHz Crystal

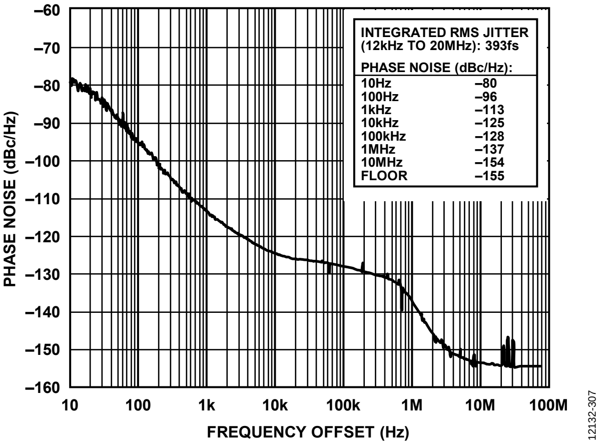


INTEGRATED RMS JITTER (12kHz TO 20MHz): 427fs

PHASE NOISE (dBc/Hz):

10Hz	–63
100Hz	–84
1kHz	–101
10kHz	–112
100kHz	–116
1MHz	–124
10MHz	–144
FLOOR	–151

Figure 6. Absolute Phase Noise (Output Driver = 21 mA Mode), f_R = 19.44 MHz, f_{OUT} = 693.482991 MHz, DPLL Loop Bandwidth = 50 Hz, f_{SYS} = 49.152 MHz Crystal

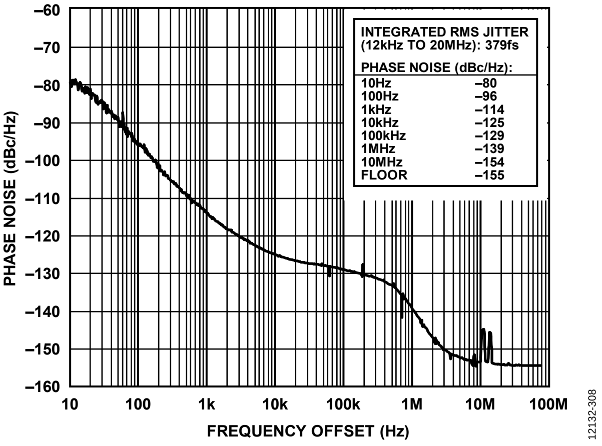


INTEGRATED RMS JITTER (12kHz TO 20MHz): 393fs

PHASE NOISE (dBc/Hz):

10Hz	–80
100Hz	–96
1kHz	–113
10kHz	–125
100kHz	–128
1MHz	–137
10MHz	–154
FLOOR	–155

Figure 7. Absolute Phase Noise (Output Driver = 21 mA Mode), f_R = 19.44 MHz, f_{OUT} = 174.703 MHz, DPLL Loop Bandwidth = 1 kHz, f_{SYS} = 49.152 MHz Crystal



INTEGRATED RMS JITTER (12kHz TO 20MHz): 379fs

PHASE NOISE (dBc/Hz):

10Hz	–80
100Hz	–96
1kHz	–114
10kHz	–125
100kHz	–129
1MHz	–139
10MHz	–154
FLOOR	–155

Figure 8. Absolute Phase Noise, f_R = 19.44 MHz, f_{OUT} = 161.1328125 MHz, DPLL Loop Bandwidth = 100 Hz, f_{SYS} = 49.152 MHz Crystal

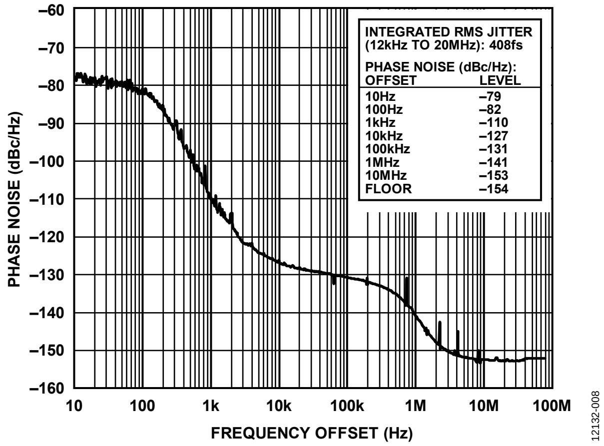


Figure 9. Absolute Phase Noise (Output Driver = 14 mA Mode), f_R = 2 kHz, f_{OUT} = 125 MHz, DPLL Loop Bandwidth = 100 Hz, f_{SYS} = 49.152 MHz Crystal

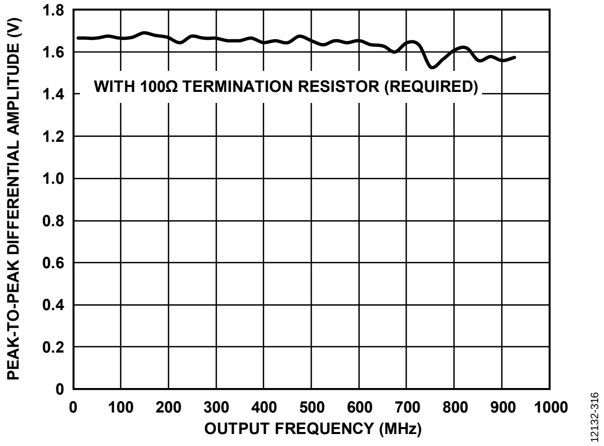


Figure 10. Peak-to-Peak Differential Amplitude vs. Output Frequency, 28 mA Mode (LVPECL-Compatible Mode) with 100 Ω Termination Resistor (Required)

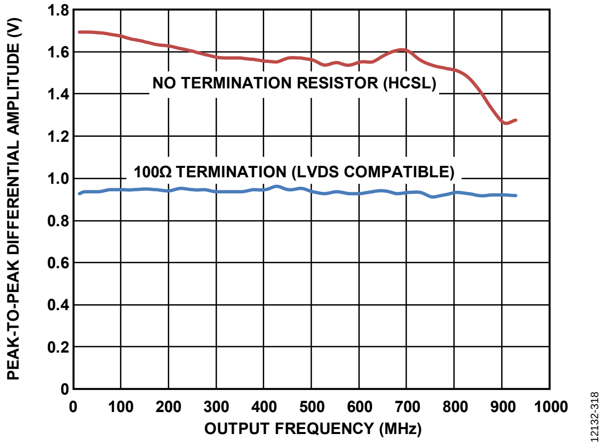


Figure 11. Peak-to-Peak Differential Amplitude vs. Output Frequency, 14 mA Mode

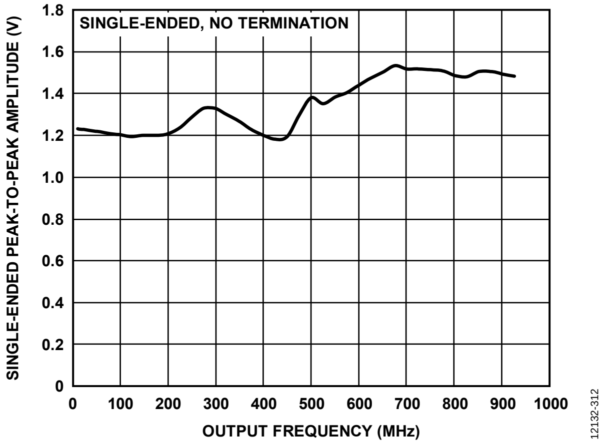


Figure 12. Single-Ended Peak-to-Peak Amplitude vs. Output Frequency, 21 mA Mode (No Termination)

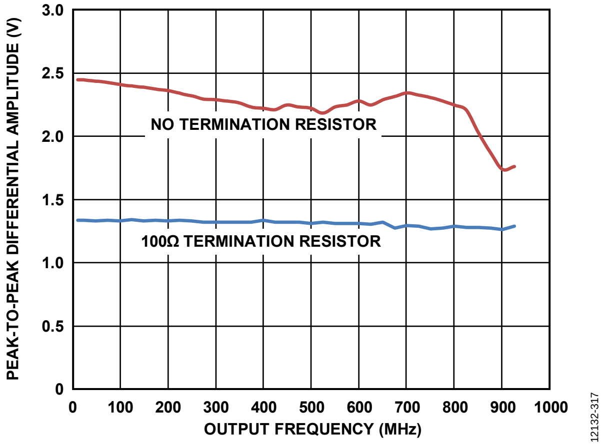


Figure 13. Peak-to-Peak Differential Amplitude vs. Output Frequency, 21 mA Mode

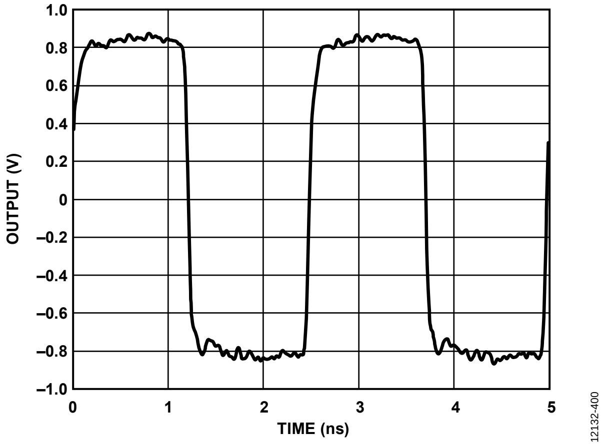


Figure 14. Output Waveform, 28 mA LVPECL-Compatible Mode (400 MHz) with 100 Ω Termination Resistor

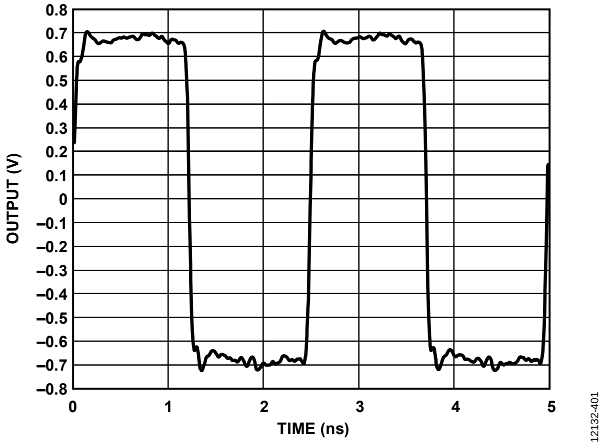


Figure 15. Output Waveform, 21 mA Mode (400 MHz) with 100 Ω Termination at Load

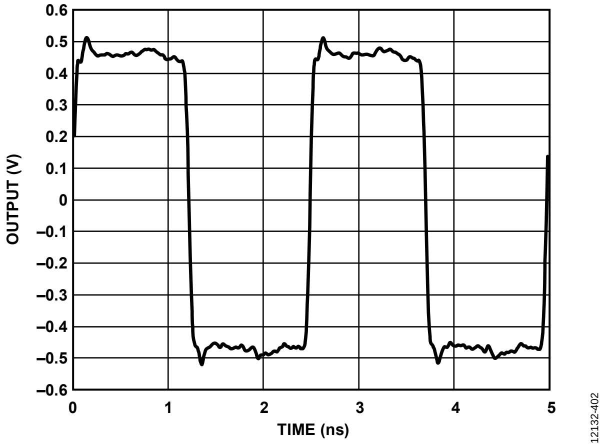


Figure 16. Output Waveform, 14 mA LVDS-Compatible Mode (400 MHz) with 100 Ω Termination at Load

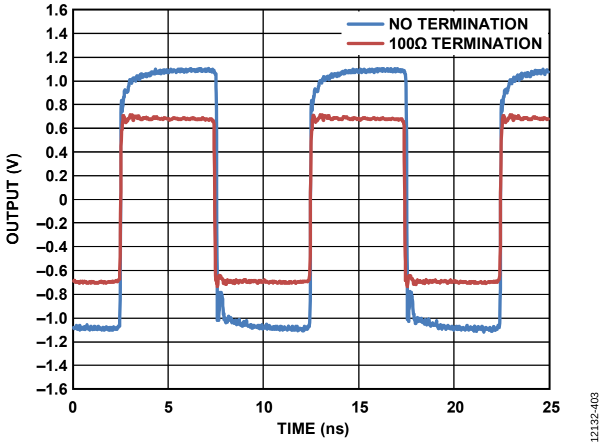


Figure 17. Output Waveform, 21 mA Mode (100 MHz)

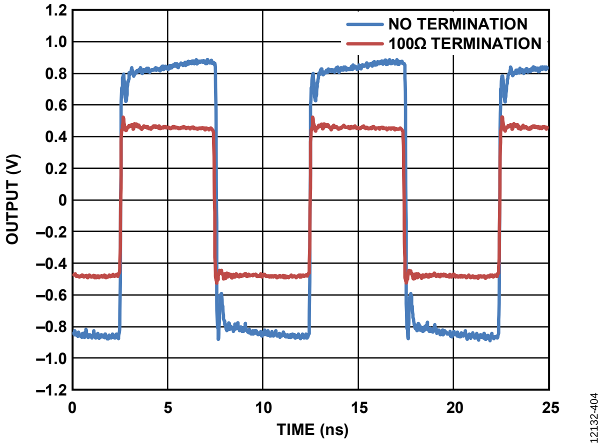


Figure 18. Output Waveform, 14 mA Mode (100 MHz)

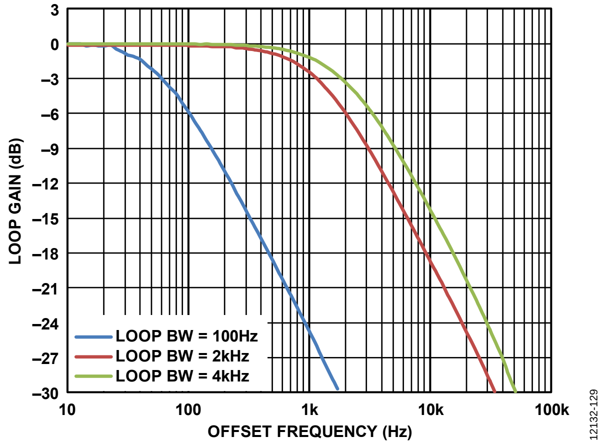


Figure 19. Closed-Loop Transfer Function for 100 Hz, 2 kHz, and 4 kHz Loop Bandwidth Settings; High Phase Margin Loop Filter Setting; Figure Compliant with Telcordia GR-253 Jitter Transfer Test for Loop Bandwidths <2 kHz (Note that the bandwidth register setting is the point where the open-loop gain = 0 dB.)

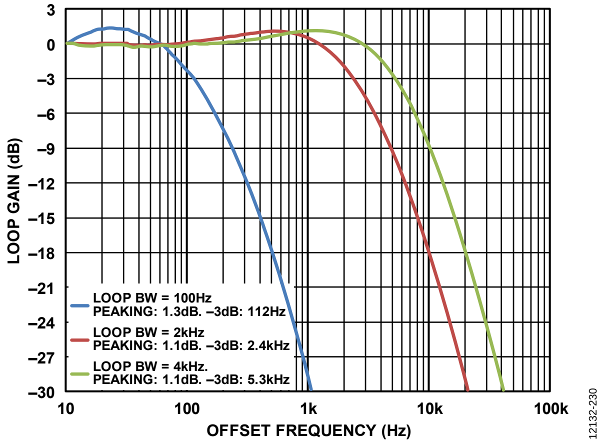


Figure 20. Closed-Loop Transfer Function for 100 Hz, 2 kHz, and 4 kHz Loop Bandwidth Settings; Normal Phase Margin Loop Filter Setting (Note that the bandwidth register setting is the point where the open-loop gain = 0 dB.)

INPUT/OUTPUT TERMINATION RECOMMENDATIONS

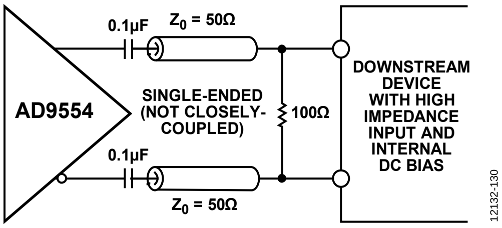


Figure 21. Destination Self-Biased Differential Receiver; Use 14 mA Mode for LVDS-Compatible Amplitude or 28 mA for LVPECL-Compatible Amplitudes (100 Ω resistor must be as close to the destination receiver as possible.)

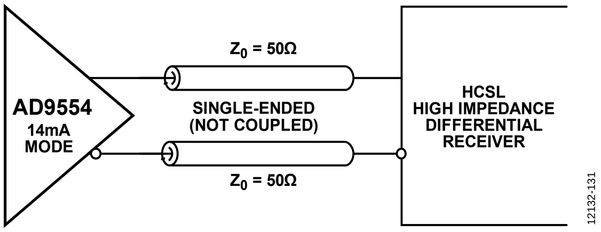


Figure 22. DC-Coupled HCSL Receiver

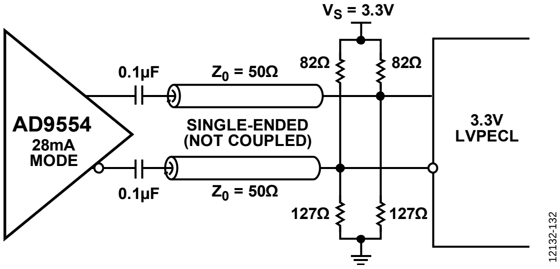


Figure 23. Interfacing the HCSL Driver to a 3.3 V LVPECL Input (This method incorporates impedance matching and dc-biasing for bipolar LVPECL receivers. If the receiver is self-biased, the termination scheme shown in Figure 21 is recommended.)

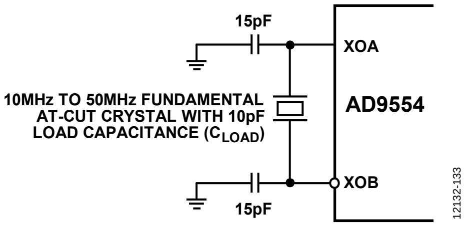


Figure 24. System Clock Input (XOA/XOB) in Crystal Mode (The recommended C_{LOAD} = 10 pF is shown. The values of 15 pF shunt capacitors shown here must equal 2 × (C_{LOAD} − C_{STRAY}), where C_{STRAY} is typically 2 pF to 5 pF.)

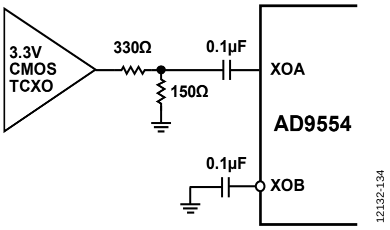


Figure 25. System Clock Input (XOA, XOB) When Using a TCXO/OCXO with 3.3 V CMOS Output

GETTING STARTED

CHIP POWER MONITOR AND STARTUP

The AD9554 monitors the voltage on the power supplies at power-up. The VDD pins provide power to the internal voltage regulators to provide a 1.2 V supply to the chip. When the internal 1.2 V supply is greater than 0.96 V ± 0.1 V, the device generates a 25 ms reset pulse. The power-up reset pulse is internal and independent of the $\overline{\text{RESET}}$ pin. This internal power-up reset sequence eliminates the need for the user to provide external power supply sequencing. The M0 pin to M8 pin values are latched 25 ms after the internal reset pulse, and the M0 to M9 multifunction pins behave as high impedance digital inputs and continue to do so until otherwise programmed. Activating the $\overline{\text{RESET}}$ pin initiates the same sequence with respect to the multifunction pins. Wait a minimum of 25 ms before programming the device to ensure that the power-on reset (POR) has completed.

MULTIFUNCTION PINS AT RESET/POWER-UP

The AD9554 Mx pins (where x is 0 through 9) have internal 100 kΩ pull-up/pull-down resistors, except for M1 and M2, and the Mx pin defaults are detailed in Table 21. Note that M0, M5, M6, and M7, are not mentioned in Table 21 for they are not used for the EEPROM function.

Table 21. Mx Pin Function at Startup

Mx Pin	Startup Function	Internal Resistor	High (Logic 1)	Low (Logic 0)
M0	I^{2}C address select	100 kΩ pull-down	Refer to Table 22	Refer to Table 22
M1	EEPROM SCL	None	Not applicable	Not applicable
M2	EEPROM SDA	None	Not applicable	Not applicable
M3	Load EEPROM at startup	100 kΩ pull-down	Loaded EEPROM	Do not load EEPROM[1]
M4	EEPROM I^{2}C enabled on M2 and M1 pins	100 kΩ pull-down	I^{2}C mode on M2 and M1 pins	Normal Mx pin function on M1and M2[1]
M5	SPI/I^{2}C select	100 kΩ pull-down	I^{2}C	SPI[1]
M6	I^{2}C address select	100 kΩ pull-up	Refer to Table 22	Refer to Table 22
M7	I^{2}C address select	100 kΩ pull-down	Refer to Table 22	Refer to Table 22
M8	EEPROM fast I^{2}C mode	100 kΩ pull-up	400 kHz[1]	100 kHz
M9	None	100 kΩ pull-down	Not applicable	Not applicable[1]

[1] Power-on default via a 100 kΩ internal pull-up/pull-down resistor. M1 and M2 do not have internal pull-up/pull-down resistors.

Table 22. SPI/I^{2}C Serial Port Setup

M7	M6	M5	M0	SPI/I^{2}C Address
Don't care	0	0	Don't care	Not applicable
Don't care	1	0	Don't care	Analog Devices, Inc., unified SPI (default)
0	0	1	0	I^{2}C, 1101000 (0x68)
0	1	1	0	I^{2}C, 1101001 (0x69)[1]
1	0	1	0	I^{2}C, 1101010 (0x6A)
1	1	1	0	I^{2}C, 1101011 (0x6B)
0	0	1	1	I^{2}C, 1101100 (0x6C)
0	1	1	1	I^{2}C, 1101101 (0x6D)
1	0	1	1	I^{2}C, 1101110 (0x6E)
1	1	1	1	I^{2}C, 1101111 (0x6F)

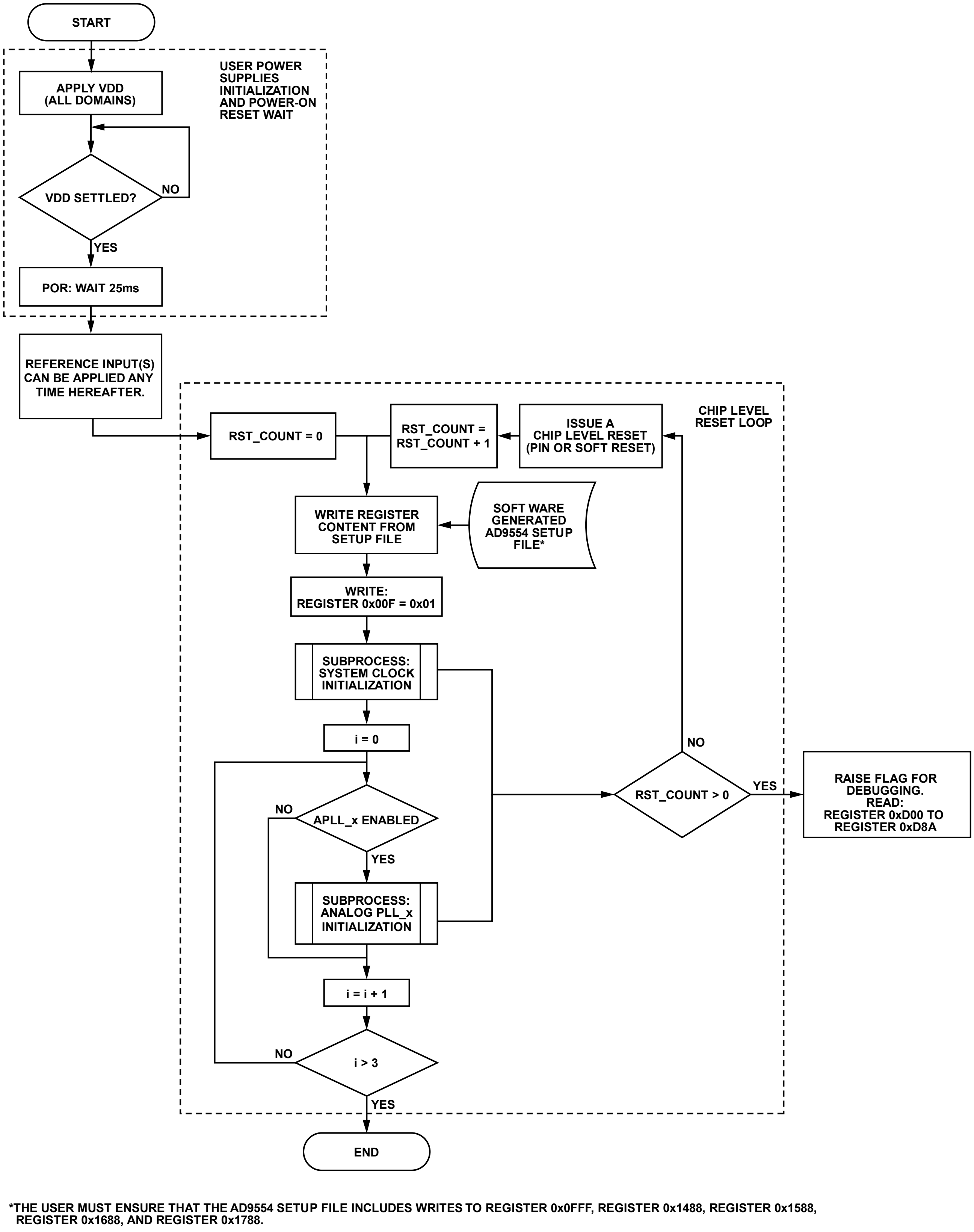
[1] If M5 is high, the I^{2}C power-on default is via internal pull-up/pull-down resistors. By pulling M5 high, the user selects I^{2}C mode; the default I^{2}C address is 0x69.

DEVICE REGISTER PROGRAMMING USING A REGISTER SETUP FILE

The evaluation software contains a programming wizard and a convenient graphical user interface (GUI) that assists the user in determining the optimal configuration for the DPLLs, APLLs, and SYSCLK based on the desired input and output frequencies. It generates a register setup file with a .STP extension that is easily readable using a text editor.

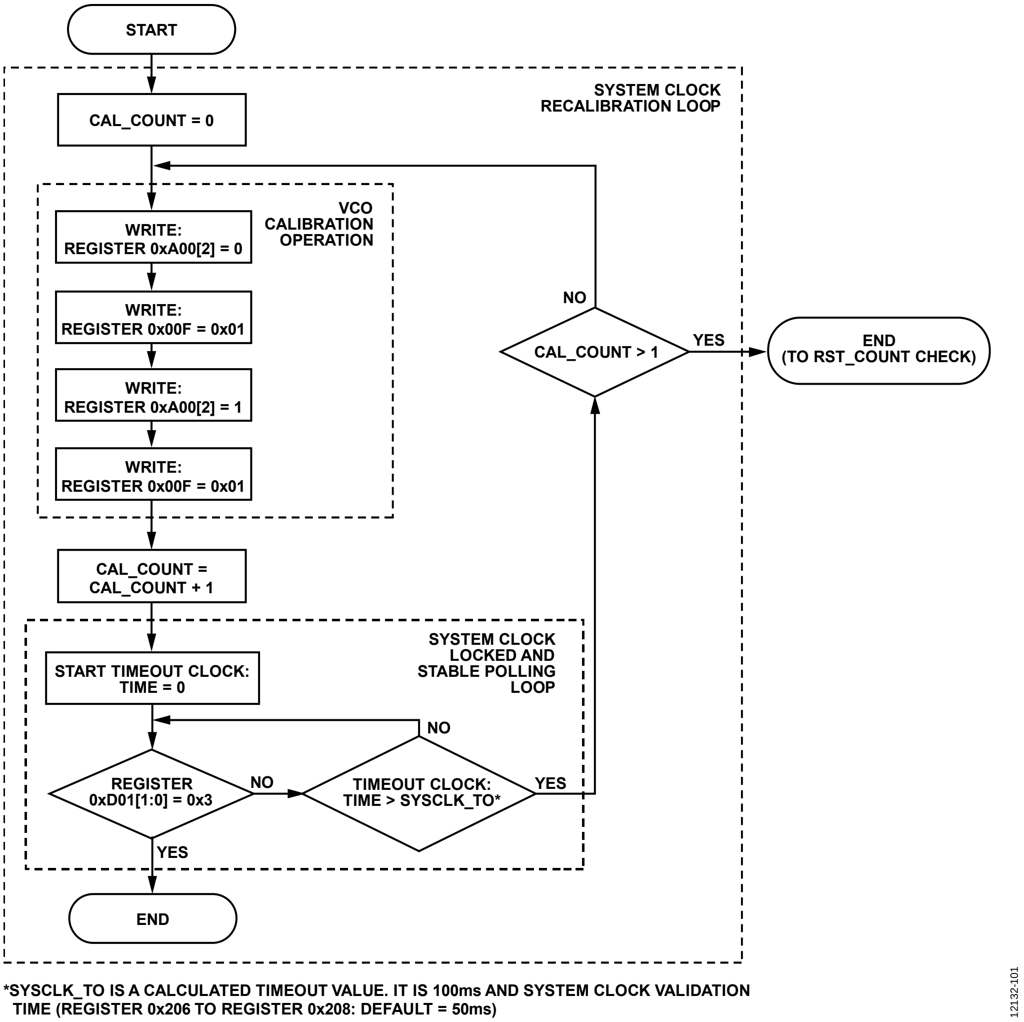
The user can configure PLL_0 through PLL_3 independently. To do so, program the common registers (such as the system clock and reference inputs) first. Next, the registers that are unique to PLL_0, PLL_1, PLL_2, or PLL_3 can be configured independently.

After using the evaluation software to create the setup file, use the sequence shown in Figure 26 through Figure 29 to program the AD9554.



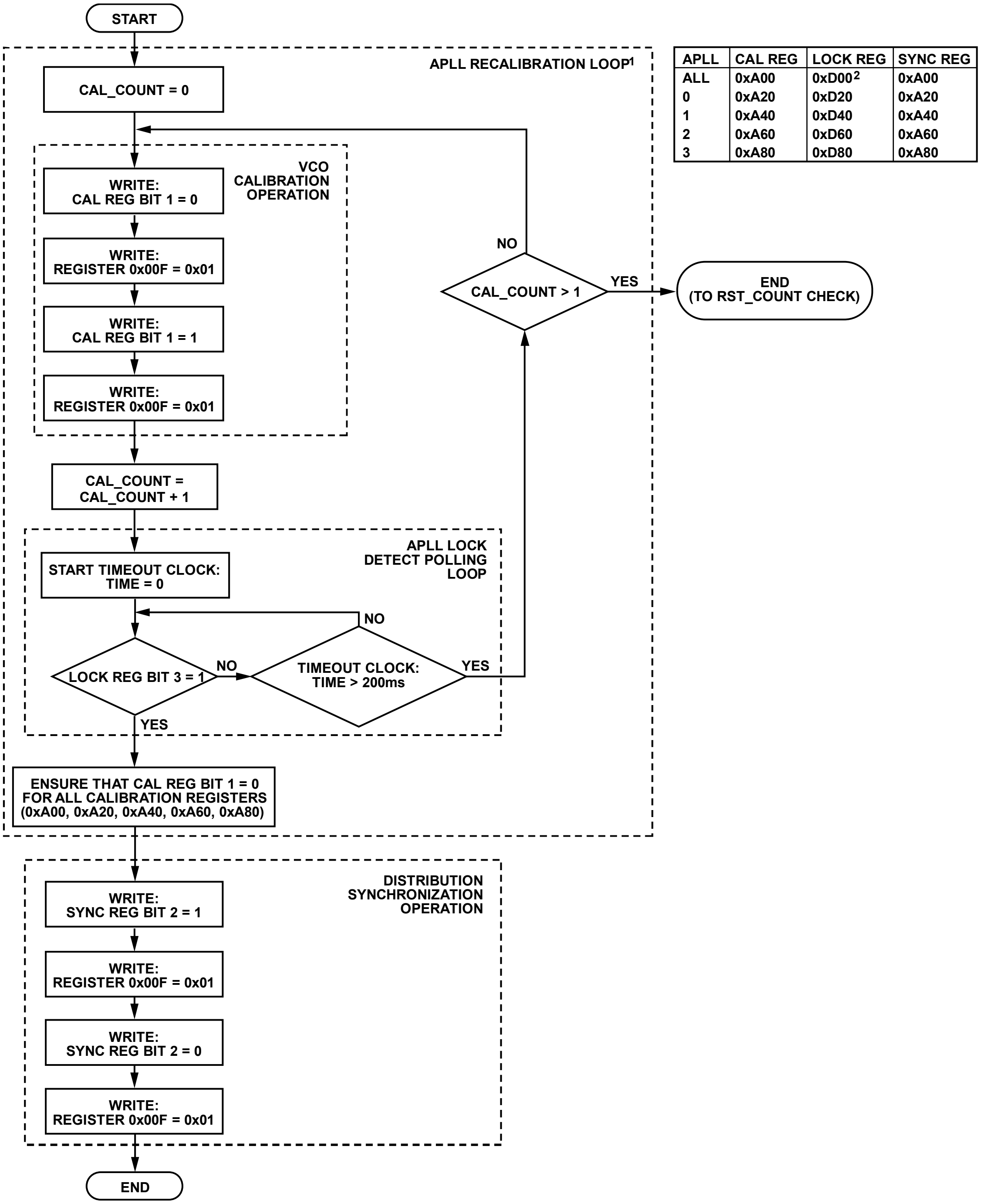
*THE USER MUST ENSURE THAT THE AD9554 SETUP FILE INCLUDES WRITES TO REGISTER 0x0FFF, REGISTER 0x1488, REGISTER 0x1588, REGISTER 0x1688, AND REGISTER 0x1788.

Figure 26. Main Process—Initialization



*SYSCLK_TO IS A CALCULATED TIMEOUT VALUE. IT IS 100ms AND SYSTEM CLOCK VALIDATION TIME (REGISTER 0x206 TO REGISTER 0x208: DEFAULT = 50ms)

Figure 27. Subprocess—System Clock Initialization



APLL	CAL REG	LOCK REG	SYNC REG
ALL	0xA00	0xD00[2]	0xA00
0	0xA20	0xD20	0xA20
1	0xA40	0xD40	0xA40
2	0xA60	0xD60	0xA60
3	0xA80	0xD80	0xA80

[1] NOTE THAT THE CALIBRATE ALL AND SOFT SYNC ALL BITS IN REGISTER 0x0A00 CAN BE USED IF THE USER WANTS TO CALIBRATE OR SYNC ALL FOUR PLLs SIMULTANEOUSLY INSTEAD OF ONE AT A TIME. HOWEVER, THE USER MUST STILL VERIFY THAT ALL FOUR APLLs ARE LOCKED BY READING THE INDIVIDUAL APLL LOCK REGISTERS.

[2] REGISTER 0x0D00 CAN ONLY BE USED TO VERIFY THE LOCK STATE OF EACH APLL IF THE CORRESPONDING DPLL IS ALSO LOCKED.

Figure 28. Subprocess—Analog PLL Initialization

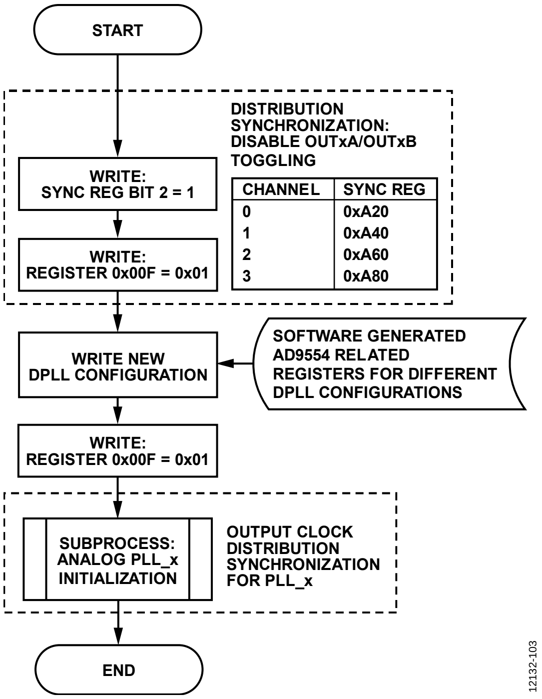


Figure 29. Main Process—Individual DPLL Reconfiguration

REGISTER PROGRAMMING OVERVIEW

This section provides a programming overview of the register blocks in the AD9554, describing what they do and why they are important. This is supplemental information only needed when loading the registers without using the .STP file.

The AD9554 evaluation software contains a wizard that determines the register settings based on the input and output frequencies of the user. It is strongly recommended that the evaluation software determine these settings.

Multifunction Pins (Optional)

To use any of the multifunction pins for status or control, this step is required. The multifunction pin parameters are located at Register 0x0100 to Register 0x010C.

Table 154 has a list of the Mx pin output functions, and Table 155 has a list of Mx pin input functions.

IRQ Functions (Optional)

To use the IRQ feature, this step is required. The IRQ functions are divided into five groups: common, PLL_0, PLL_1, PLL_2, and PLL_3.

First, choose the events that trigger an IRQ and then set them in Register 0x010F to Register 0x011D. Next, an Mx pin must be assigned to the IRQ function. The user can choose to dedicate one Mx pin to each of the five IRQ groups, or one Mx pin can be assigned for all IRQs.

The IRQ monitor registers are located at Register 0x0D08 to Register 0x0D16. If the desired bits in the IRQ mask registers at Register 0x010F to Register 0x011D are set high, the appropriate IRQ monitor bit at Register 0x0D08 to Register 0x0D16 is set high when the indicated event occurs.

Individual IRQ events are cleared by using the IRQ clearing registers at Register 0x0A05 to Register 0x0A14 or by setting the clear all IRQs bit (Register 0x0A05[0]) to 1b.

The default values of the IRQ mask registers are such that interrupts are not generated. The default IRQ pin (and Mx pins) mode is active high CMOS. The user can also select active low CMOS, open-drain PMOS, and open-drain NMOS independently on any of these pins.

Watchdog Timer (Optional)

To use the watchdog timer, this step is required. The watchdog timer control is located at Register 0x010D and Register 0x010E. The watchdog timer is disabled by default.

The watchdog timer is useful for generating an IRQ at a fixed interval. The timer is reset by setting the clear watchdog timer bit in Register 0x0A05[7] to 1.

The user can also program an Mx pin for the watchdog timer output. In this mode, the Mx pin generates a 40 ns pulse every time the watchdog timer expires.

System Clock Configuration

The system clock multiplier (SYSCLK) parameters are at Register 0x0200 to Register 0x0208. For optimal performance, use the following steps:

1. Set the system clock PLL input type and divider values.
2. Set the system clock period. It is essential to program the system clock period because many of the AD9554 subsystems rely on this value.
3. Set the system clock stability timer. The system clock stability timer specifies the amount of time that the system clock PLL must be locked before the device declares that the system clock is stable. It is critical that the system clock stability timer be set long enough to ensure that the external source is completely stable when the timer expires. For instance, a temperature compensated crystal oscillator (TCXO) can take longer than 50 ms (the default value for the stability timer) to stabilize after power is applied.
4. Update all registers (Register 0x000F = 0x01).
5. To calibrate the system clock on the next IO_UPDATE, write Register 0x0A00 = 0x04.
6. Update all registers (Register 0x000F = 0x01).

Important Notes

If Bit 2 in Register 0x0A00 is set independently to initiate a system clock PLL calibration, leave this bit set to 1 in all subsequent writes to Register 0x0A00. If this bit is accidentally cleared, recalibrate the system clock VCO or issue a calibrate all command by setting Bit 1 in Register 0x0A00 and by issuing an IO_UPDATE (Register 0x000F = 0x01).

In addition, the system clock PLL must be locked for the digital PLL blocks to function correctly and to read back the registers updated on the system clock domain. These registers include the status registers, as well as the free running tuning word. APLL calibration and input reference monitoring and validation require that the system clock be stable. Therefore, first ensure that the system clock is stable by checking Bit 1 in Register 0x0D01 when debugging the AD9554.

Reference Inputs

The reference input parameters and reference dividers are common to all PLLs; there is only one reference divider (R divider) for each reference input. The register address for each reference input follows:

- Register 0x0300 to Register 0x031E for REFA
- Register 0x0320 to Register 0x033E for REFB
- Register 0x0340 to Register 0x035E for REFC
- Register 0x0360 to Register 0x037E for REFD

These registers include the following settings:

- Reference logic type (such as differential, single-ended)
- Reference divider (20-bit R divider value)
- Reference input period and tolerance
- Reference validation timer
- Phase and frequency lock detector settings
- Phase step threshold

Other reference input settings are in the following registers:

- Reference input enable information is found in the DPLL Feedback Dividers section.
- Reference power-down information is found in Register 0x0A01.
- Reference switching mode settings are found in Register 0x0A22 (DPLL_0), Register 0x0A42 (DPLL_1), Register 0x0A62 (DPLL_2), and Register 0x0A82 (DPLL_3).

Digital PLL (DPLL) Controls and Settings

The DPLL control parameters are separate for DPLL_0 through DPLL_3. They reside in the following registers:

- Register 0x0400 to Register 0x041E (DPLL_0)
- Register 0x0500 to Register 0x051E (DPLL_1)
- Register 0x0600 to Register 0x061E (DPLL_2)
- Register 0x0700 to Register 0x071E (DPLL_3)

These registers include the following settings:

- 30-bit free running frequency
- DPLL pull-in range limits
- DPLL closed-loop phase offset
- Tuning word history control (for holdover operation)
- Phase slew control (for controlling the phase slew rate during a closed-loop phase adjustment)
- Demapping control

With the exception of the free running tuning word, the default values of these registers are fine for normal operation. The free running frequency of the DPLL determines the frequency that appears at the APLL input when user free run mode is selected. The correct free running frequency is required for the APLL to calibrate and lock correctly.

Output PLLs (APLLs) and Output Drivers

The registers that control the APLLs and output drivers reside in the following registers:

- Register 0x0430 to Register 0x043E (APLL_0)
- Register 0x0530 to Register 0x053E (APLL_1)
- Register 0x0630 to Register 0x063E (APLL_2)
- Register 0x0730 to Register 0x073E (APLL_3)

The following functions are controlled in these registers:

- APLL settings (feedback divider, charge pump current)
- Output synchronization mode
- Output divider values
- Output enable/disable (disabled by default)
- Output logic type

The APLL calibration and synchronization bits reside in the following registers:

- Register 0x0A20 (APLL_0)
- Register 0x0A40 (APLL_1)
- Register 0x0A60 (APLL_2)
- Register 0x0A80 (APLL_3)

DPLL Feedback Dividers

Each DPLL has separate feedback divider settings for each reference input, which allows the user to have each digital PLL perform a different frequency translation. However, there is only one reference divider (R divider) for each reference input.

The feedback divider register settings for DPLL_0 reside in the following registers. Feedback divider registers for the remaining three DPLLs mimic the structure of the DPLL_0 registers, but are offsets by 0x0100 registers.

- Register 0x0440 to Register 0x44C (DPLL_0 for REFA)
- Register 0x044D to Register 0x459 (DPLL_0 for REFB)
- Register 0x045A to Register 0x466 (DPLL_0 for REFC)
- Register 0x0467 to Register 0x473 (DPLL_0 for REFD)
- DPLL_1 for REFA to DPLL_1 for REFD: Same as DPLL_0 but offset by 0x0100 registers
- DPLL_2 for REFA to DPLL_2 for REFD: Same as DPLL_0 but offset by 0x0200 registers
- DPLL_3 for REFA to DPLL_3 for REFD: Same as DPLL_0 but offset by 0x0300 registers

These registers include the following settings:

- Reference priority
- Reference input enable (separate for each DPLL)
- DPLL loop bandwidth
- DPLL loop filter
- DPLL feedback divider (integer portion)
- DPLL feedback divider (fractional portion)
- DPLL feedback divider (modulus portion)

Common Operational Controls

The common operational controls reside at Register 0x0A00 to Register 0x0A14 and include the following:

- Simultaneous calibration and synchronization of all PLLs
- Global power-down
- Reference power-down
- Reference validation override
- IRQ clearing (for all IRQs)

PLL_0 Through PLL_3 Operational Controls

The PLL_0 through PLL_3 operational controls are located at Register 0x0A20 to Register 0x0A84 and include the following:

- APLL calibration and synchronization
- Output driver enable and power-down
- DPLL reference input switching modes
- DPLL open-loop phase stepping control

The user free run bits that enable user free run mode reside in the following registers:

- Register 0x0A22 = 0x01 (DPLL_0)
- Register 0x0A42 = 0x01 (DPLL_1)
- Register 0x0A62 = 0x01 (DPLL_2)
- Register 0x0A82 = 0x01 (DPLL_3)

APLL VCO Calibration

VCO calibration ensures that the VCO has sufficient operating margin to function across the full temperature range. The user can calibrate each of the four VCOs independently of one another. When calibrating the APLL VCO, it is important to remember the following conditions:

- The APLL VCO calibration does not occur until the system clock is stable.
- The APLL VCO must have the correct frequency from the 30-bit digitally controlled oscillator (DCO) during calibration. The free running tuning word is found in Register 0x0400 to Register 0x0403 (DPLL_0), Register 0x0500 to Register 0x0503 (DPLL_1), Register 0x0600 to Register 0x0603 (DPLL_2), and Register 0x0700 to Register 0x0703 (DPLL_3).
- The APLL VCO must be recalibrated any time the APLL frequency changes.
- APLL VCO calibration occurs on the low to high transition of the APLL VCO calibration bit (Register 0x0A20[1] for APLL_0, Register 0x0A40[1] for APLL_1, Register 0x0A60[1] for APLL_2, and Register 0x0A80[1] for APLL_3).
- The VCO calibration bit is not an autoclearing bit. Therefore, this bit must be cleared (and an IO_UPDATE issued) before the APLL is recalibrated.
- The best way to monitor successful APLL calibration is by monitoring the APLL locked bit in the following registers: Register 0x0D20[3] for APLL_0, Register 0x0D40[3] for APLL_1, Register 0x0D60[3] for APLL_2, and Register 0x0D80[3] for APLL_3.

Generate the Output Clock

If Register 0x0435 (for PLL_0), Register 0x0535 (for PLL_1), Register 0x0635 (for PLL_2), or Register 0x0735 (for PLL_3) is programmed for automatic clock distribution synchronization via the DPLL phase or frequency lock, the synthesized output signal appears at the clock distribution outputs. Otherwise, set and then clear the soft sync bit (Bit 2 in Register 0x0A20 for APLL_0, Bit 2 in Register 0x0A40 for APLL_1, Bit 2 in Register 0x0A60 for APLL_2, and Bit 2 in Register 0x0A80 for APLL_3) or use a multifunction pin input (if programmed accordingly) to generate a clock distribution sync pulse. This sync pulse causes the synthesized output signal to appear at the clock distribution outputs. Note that the sync pulse is delayed until the APLL achieves lock following APLL calibration.

Generate the Reference Acquisition

After the registers are programmed, the DPLLs lock to the reference input that has been manually selected (if any), or the first available reference that has the highest priority.

THEORY OF OPERATION

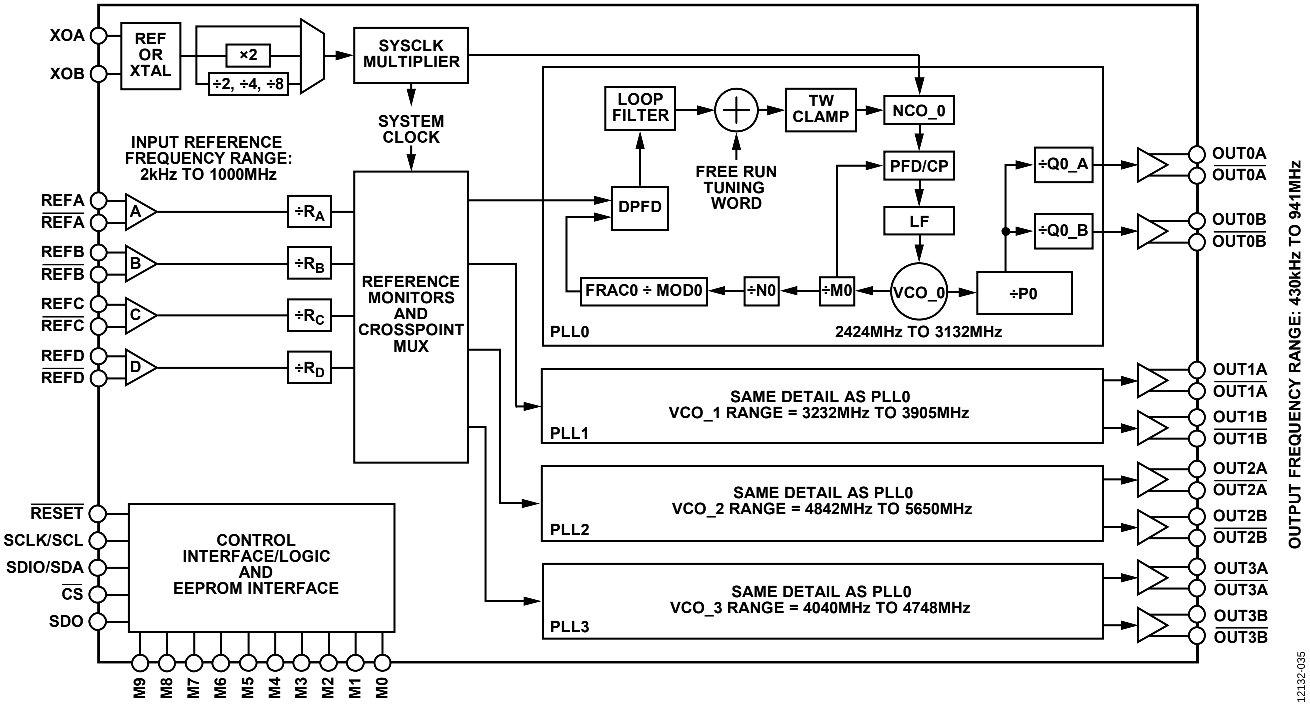


Figure 30. Detailed Block Diagram

OVERVIEW

The AD9554 provides clocking outputs that are directly related in phase and frequency to the selected (active) reference but with jitter characteristics governed by the system clock, the DCO, and the analog output PLL (APLL). The AD9554 can be thought of as four copies of the AD9557 inside one package, with a 4:4 crosspoint controlling the reference inputs. The AD9554 supports up to four reference inputs and input frequencies ranging from 2 kHz to 1000 MHz. The cores of this device are four digital phase-locked loops (DPLLs). Each DPLL has a programmable digital loop filter that greatly reduces jitter transferred from the active reference to the output, and these four DPLLs operate completely independently of each other. The AD9554 supports both manual and automatic holdover. While in holdover, the AD9554 continues to provide an output as long as the system clock is present. The holdover output frequency is a time average of the output frequency history prior to the transition to the holdover condition. The device offers manual and automatic reference switchover capability if the active reference is degraded or fails completely. The AD9554 also has adaptive clocking capability that allows the user to dynamically change the DPLL divide ratios while the DPLLs are locked.

The AD9554 includes a system clock multiplier, four DPLLs, and four APLLs. The input signal goes first to the DPLL, which performs the jitter cleaning and most of the frequency translation. Each DPLL features a 30-bit DCO output that generates a signal in the range of 283 MHz to 345 MHz.

The DCO output goes to the APLL, which multiplies the signal up to a range of 2.4 GHz to 5.6 GHz. This signal is then sent to the clock distribution section, which consists of a P divider cascaded with 10-bit channel dividers (divide by 1 to divide by 1024).

The XOA and XOB inputs provide the input for the system clock. These pins accept a reference clock in the 10 MHz to 268 MHz range or a 10 MHz to 50 MHz crystal connected directly across the XOA and XOB inputs. The system clock provides the clocks to the frequency monitors, the DPLLs, and internal switching logic.

Each APLL on the AD9554 has two differential output drivers. Each of the eight output drivers has a dedicated 10-bit programmable post divider. Each differential driver operates up to 1.25 GHz and is an HCSL driver with a 58 Ω internal termination resistor on each leg. There are three drive strengths:

- The 14 mA mode is used for HCSL and ac-coupled LVDS. When used as an LVDS-compatible driver, it must be ac-coupled and terminated with a 100 Ω resistor across the differential pair.
- The 28 mA mode produces a voltage swing and is compatible with LVPECL. If LVPECL signal levels are required, the designer must ac-couple the AD9554 output.
- The 21 mA mode is halfway in between the two other settings.

The AD9554 also includes a demapping control function that allows the user to adjust each of the AD9554 output frequencies dynamically by periodically writing the actual level and desired level of a first in, first out (FIFO). These levels are intended to match the actual levels on the user system.

REFERENCE INPUT PHYSICAL CONNECTIONS

Four pairs of pins (REFA, $\overline{\text{REFA}}$ to REFD, $\overline{\text{REFD}}$) provide access to the reference clock receivers. To accommodate input signals with slow rising and falling edges, both the differential and single-ended input receivers employ hysteresis. Hysteresis also ensures that a disconnected or floating input does not cause the receiver to oscillate.

When configured for differential operation, the input receivers accommodate either ac- or dc-coupled input signals. If the input receiver is configured for dc-coupled LVDS mode, the input receivers are capable of accepting dc-coupled LVDS signals; however, only up to a maximum of 10.24 MHz. For frequencies greater than that, ac-couple the input clock and use ac-coupled differential mode. The receiver is internally dc biased to handle ac-coupled operation; however, there is no internal 50 Ω or 100 Ω termination.

When configured for single-ended operation, the input receivers exhibit a pull-down load of 47 kΩ (typical). See Register 0x0300 to Register 0x037E for the settings for the reference inputs.

REFERENCE MONITORS

The accuracy of the input reference monitors depends on a known and accurate system clock period. Therefore, the function of the reference monitors is not operable until the system clock is stable.

Reference Period Monitor

Each reference input has a dedicated monitor that repeatedly measures the reference period. The AD9554 uses the reference period measurements to determine the validity of the reference based on a set of user provided parameters in the reference input area of the register map. See Register 0x0304 through Register 0x030E for the settings for Reference A, Register 0x0324 through Register 0x032E for the settings for Reference B, Register 0x0344 through Register 0x034E for the settings for Reference C, and Register 0x0364 through Register 0x036E for the settings for Reference D.

The monitor compares the measured period of a particular reference input with the parameters stored in the profile register assigned to that same reference input. The parameters include the reference period, an inner tolerance, and an outer tolerance. A 40-bit number defines the reference period in units of femtoseconds (fs). A 20-bit number defines the inner and outer tolerances. The value stored in the register is the reciprocal of the tolerance specification. For example, a tolerance specification of 50 ppm yields a register value of 1/(50 ppm) = 1/0.000050 = 20,000 (0x04E20).

The use of two tolerance values provides hysteresis for the monitor decision logic. The inner tolerance applies to a previously faulted reference and specifies the largest period tolerance that a previously faulted reference can exhibit before it qualifies as unfaulted. The outer tolerance applies to an already unfaulted reference. It specifies the largest period tolerance that an unfaulted reference can exhibit before being faulted.

To produce decision hysteresis, the inner tolerance must be less than the outer tolerance. That is, a faulted reference must meet tighter requirements to become unfaulted than an unfaulted reference must meet to become faulted.

Reference Validation Timer

Each reference input has a dedicated validation timer. The validation timer establishes the amount of time that a previously faulted reference must remain unfaulted before the AD9554 declares that it is valid. The timeout period of the validation timer is programmable via a 16-bit register (Address 0x030F and Address 0x0310 for Reference A). The 16-bit number stored in the validation register represents units of milliseconds (ms), which yields a maximum timeout period of 65,535 ms.

It is possible to disable the validation timer by programming the validation timer to 0. With the validation timer disabled, the user must validate a reference manually via the manual reference validation override controls register (Register 0x0A02).

Reference Validation Override Control

The user can also override the reference validation logic and either force an invalid reference to be treated as valid or force a valid reference to be treated as an invalid reference. These controls are in Register 0x0A02 to Register 0x0A03.

REFERENCE INPUT BLOCK

Unlike the AD9557, the AD9554 separates the DPLL reference dividers from the feedback dividers.

The reference input block includes the input receiver, the reference divider (R divider), and the reference input frequency monitor for each reference input. The reference input settings for REFA are grouped together in Register 0x0300 to Register 0x031E. The corresponding registers for REFB through REFD are the following: Register 0x320 to Register 0x33E, Register 0x340 to Register 0x35E, and Register 0x0360 to Register 0x037E, respectively.

These registers include the following settings:

- Reference logic type (such as differential, single-ended)
- Reference divider (20-bit R divider value)
- Reference input period and tolerance
- Reference validation timer
- Phase and frequency lock detector settings
- Phase step threshold

The reference prescaler reduces the frequency of this signal by an integer factor, R + 1, where R is the 20-bit value stored in the appropriate profile register and $0 \leq R \leq 1{,}048{,}575$. Therefore, the frequency at the output of the R divider (or the input to the time-to-digital converter [TDC]) is as follows:

$$f_{TDC} = \frac{f_R}{R+1}$$

After the R divider, the signal passes to a 4:4 crosspoint that allows any reference input signal to go to any DPLL.

Each DPLL on the AD9554 has an independent set of feedback dividers for each reference input. A description of these settings can be found in the Digital PLL (DPLL) Core section.

The AD9554 evaluation software includes a frequency planning wizard that configures the profile parameters based on the input and output frequencies.

REFERENCE SWITCHOVER

An attractive feature of the AD9554 is its versatile reference switchover capability. The flexibility of the reference switchover functionality resides in a sophisticated prioritization algorithm that is coupled with register-based controls. This scheme provides the user with maximum control over the state machine that handles the reference switchover.

The main reference switchover control resides in the user mode registers in the PLL_0 through PLL_3 operational controls registers. The reference switching mode bits for each DPLL include the following:

- Register 0x0A22[4:2] for DPLL_0
- Register 0x0A42[4:2] for DPLL_1
- Register 0x0A62[4:2] for DPLL_2
- Register 0x0A82[4:2] for DPLL_3

These bits allow the user to select one of the five operating modes of the reference switchover state machine that follows:

- Automatic revertive mode
- Automatic nonrevertive mode
- Manual with automatic fallback mode
- Manual with holdover fallback mode
- Full manual mode without holdover fallback

In automatic modes, a fully automatic priority-based algorithm selects the active reference. When programmed for automatic mode, the device chooses the highest priority valid reference. When two or more references have the same priority, REFA has preference over REFB, and so on in alphabetical order. However, the reference position is used as a tiebreaker only and does not initiate a reference switch.

An overview of the five operating modes follows:

- Automatic revertive mode. The device selects the highest priority valid reference and switches to a higher priority reference if it becomes available, even if the reference in use is still valid. In this mode, the user reference is ignored.
- Automatic nonrevertive mode. The device stays with the currently selected reference as long as it is valid, even if a higher priority reference becomes available. The user reference is ignored in this mode.
- Manual with automatic fallback mode. The device uses the user reference for as long as it is valid. If it becomes invalid, the reference input with the highest priority is chosen in accordance with the priority-based algorithm.
- Manual with holdover fallback mode. The user reference is the active reference until it becomes invalid. At that point, the device goes into holdover.
- Full manual mode without holdover fallback. The user reference is the active reference, regardless of whether it is valid.

The user also can force the device directly into holdover or free run operation via the user holdover and user free run bits. In free run mode, the free run frequency tuning word registers define the free run output frequency. In holdover mode, the output frequency depends on the holdover control settings (see the Holdover section).

Phase Build-Out Reference Switching

The AD9554 supports phase build-out reference switching, which refers to a reference switchover that completely masks any phase difference between the previous reference and the new reference. That is, there is virtually no phase change detectable at the output when a phase build-out switchover occurs.

DIGITAL PLL (DPLL) CORE

DPLL Overview

The AD9554 contains four separate DPLL cores (one each for DPLL_0 through DPLL_3), and each core operates independently of one another. A diagram of a single core is shown in Figure 27. Many of the blocks shown in this diagram are purely digital.

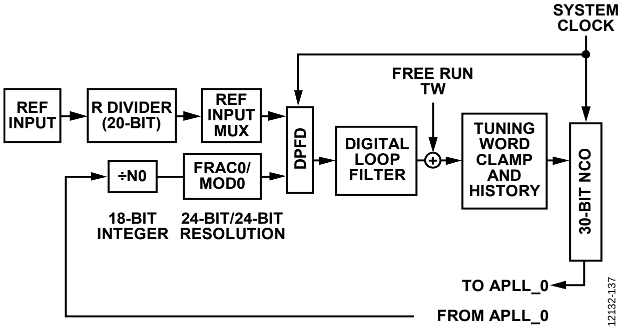


Figure 31. DPLL_0 Core

The start of the DPLL signal chain is the reference signal, f_R, which has been divided by the R divider and then routed through the crosspoint switch to the DPLL. The frequency of this signal (f_{TDC}) is

$$f_{TDC} = f_R / \frac{f_R}{R+1}$$

This is the frequency used by the TDC inside the DPLL.

A TDC samples the output of the R divider. The TDC/phase frequency detector (PFD) produces a time series of digital words and delivers them to the digital loop filter. The digital loop filter offers the following:

- The determination of the filter response by numeric coefficients rather than by discrete component values
- The absence of analog components (R/L/C) that eliminate tolerance variations due to aging
- The absence of thermal noise associated with analog components
- The absence of control node leakage current associated with analog components (a source of reference feedthrough spurs in the output spectrum of a traditional APLL)

The digital loop filter produces a time series of digital words at its output and delivers them to the frequency tuning input of a Σ-Δ modulator. The digital words from the loop filter steer the Σ-Δ modulator frequency toward frequency and phase lock with the input signal (f_{TDC}).

Each DPLL includes a feedback divider that causes the digital loop to operate at an integer-plus-fractional multiple. The output of the DPLL is

$$f_{OUT\_DPLL} = f_{TDC} \times \left[(N+1) + \frac{FRAC}{MOD} \right]$$

where:
N is the 18-bit value stored in the appropriate profile registers (Register 0x0444 to Register 0x0446 for DPLL_0 REFA).
FRAC and *MOD* are the 24-bit numerators and denominators of the fractional feedback divider block. The fractional portion of the feedback divider can be bypassed by setting FRAC or MOD to 0.

Note that there are four DPLLs. In the Register Map section and the Register Map Bit Descriptions section, N0, FRAC0, and MOD0 are used for DPLL_0, and N1, FRAC1, MOD1 are used for DPLL_1, and so on.

For optimal performance, the DPLL output frequency is typically 300 MHz to 350 MHz. Note that the DPLL output frequency is the same as APLL input frequency.

TDC/PFD

The PFD is an all-digital block. It compares the digital output from the TDC (which relates to the active reference edge) with the digital word from the feedback block. It uses a digital code pump (rather than a conventional charge pump) to generate the error signal that steers the Σ-Δ modulator frequency toward phase lock.

Programmable Digital Loop Filter

The AD9554 loop filter is a third-order digital IIR filter that is analogous to the third-order analog filter shown in Figure 28.

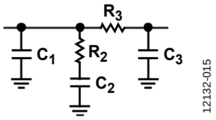


Figure 32. Third-Order Analog Loop Filter

The AD9554 has a default loop filter coefficient for two DPLL settings: nominal (70°) phase margin and high (88.5°) phase margin. The high phase margin setting is for applications that require <0.1 dB of closed-loop peaking. While these settings do not normally need to be changed, the user can contact Analog Devices for assistance with calculating new coefficients to tailor the loop filter to specific requirements.

The AD9554 loop filter block features a simplified architecture in which the user enters the desired loop characteristics (such as loop bandwidth) directly into the DPLL registers. This architecture makes the calculation of individual coefficients unnecessary in most cases, while still offering extensive flexibility.

DPLL Digitally Controlled Oscillator (DCO) Free Run Frequency

The AD9554 uses a Σ-Δ modulator as a DCO. The DCO free run frequency can be calculated by

$$f_{DCO\_FREERUN} = f_{SYS} \times \frac{1}{DCOint + \frac{FTW0}{2^{30}}}$$

where:
f_{SYS} is the system clock frequency. See the System Clock (SYSCLK) section for information on calculating the system clock frequency.
DCOint is the DCO integer setting. The DCO integer is usually 7, and it can be found in Register 0x0404[3:0] for DPLL_0.
FTW0 is the value in Register 0x0400 to Register 0x0403 for DPLL_0 (see Table 32 for corresponding values for DPLL_1 through DPLL_3).

Adaptive Clocking

The AD9554 supports adaptive clocking applications such as asynchronous mapping and demapping. For these applications, the output frequency can be dynamically adjusted by up to ±100 ppm from the nominal output frequency without manually breaking the DPLL loop and reprogramming the device.

The following registers are used in this function:

- Register 0x0444 to Register 0x0446 (DPLL_0 N0 divider)
- Register 0x0447 to Register 0x0449 (DPLL_0 FRAC0 divider)
- Register 0x044A to Register 0x044C (DPLL_0 MOD0 divider)

Note that the register values shown are for REFA/DPLL_0. There are corresponding registers for all reference input and DPLL combinations.

Writing to these registers requires an IO_UPDATE by writing 0x01 to Register 0x000F before the new values take effect.

To make small adjustments to the output frequency, vary the FRAC (FRAC0 through FRAC3) and issue an IO_UPDATE. The advantage to using only FRAC to adjust the output frequency is that the DPLL does not briefly enter holdover. Therefore, the FRAC bit can be updated as quickly as the phase detector frequency of the DPLL.

Writing to the N (N0 through N3) and MOD (M0 through M3) dividers allows larger changes to the output frequency. When the AD9554 detects a write in the N or MOD value, it automatically enters and exits holdover for a brief instant without any disturbance in the output frequency. This limits how quickly the output frequency can be adapted.

It is important to note that the amount of frequency adjustment is limited to ±100 ppm before the output PLL (APLL) needs a recalibration. Variations larger than ±100 ppm are possible, but such variations can compromise the ability of the AD9554 to maintain lock over temperature extremes.

It is also important to remember that the rate of change in output frequency depends on the DPLL loop bandwidth.

DPLL Phase Lock Detector

The DPLL contains an all-digital phase lock detector. The user controls the threshold sensitivity and hysteresis of the phase detector via the profile registers.

The lock detector behaves in a manner analogous to water in a tub (see Figure 29). The total capacity of the tub is 4096 units, with −2048 denoting empty, 0 denoting the 50% point, and +2048 denoting full. The tub also has a safeguard to prevent overflow. Furthermore, the tub has a low water mark at −1024 and a high water mark at +1024. To change the water level, the user adds water with a fill bucket or removes water with a drain bucket. The user specifies the size of the fill and drain buckets via the 8-bit fill rate and drain rate values in the profile registers.

The water level in the tub is what the lock detector uses to determine the lock and unlock conditions. When the water level is below the low water mark (−1024), the lock detector indicates an unlock condition. Conversely, when the water level is above the high water mark (+1024), the lock detector indicates a lock condition. When the water level is between the marks, the lock detector holds its last condition. This concept appears graphically in Figure 29, with an overlay of an example of the instantaneous water level (vertical) vs. time (horizontal) and the resulting lock/unlock states.

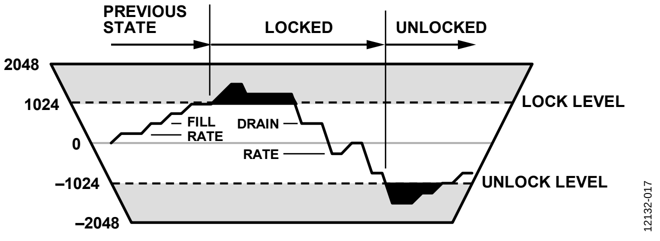


Figure 33. Lock Detector Diagram

During any given PFD phase error sample, the lock detector either adds water with the fill bucket or removes water with the drain bucket (one or the other but not both). The decision of whether to add or remove water depends on the threshold level specified by the user. The phase lock threshold value is a 24-bit number stored in the profile registers and is expressed in picoseconds. Thus, the phase lock threshold extends from 10 ns to ±16.7 µs and represents the magnitude of the phase error at the output of the PFD.

The phase lock detector compares each phase error sample at the output of the PFD to the programmed phase threshold value. If the absolute value of the phase error sample is less than or equal to the programmed phase threshold value, the detector control logic dumps one fill bucket into the tub. Otherwise, it removes one drain bucket from the tub. Note that it is the magnitude, relative to the phase threshold value, that determines whether to fill or drain the bucket, and not the polarity of the phase error sample.

If more filling is taking place than draining, the water level in the tub eventually rises above the high water mark (+1024), which causes the lock detector to indicate lock. If more draining is taking place than filling, the water level in the tub eventually falls below the low water mark (−1024), which causes the lock detector to indicate unlock. The ability to specify the threshold level, fill rate, and drain rate enables the user to tailor the operation of the lock detector to the statistics of the timing jitter associated with the input reference signal.

Note that whenever the AD9554 enters the free run or holdover mode, the DPLL phase lock detector indicates an unlocked state. However, when the AD9554 performs a reference switch, phase step detection, or loop bandwidth change, the state of the lock detector prior to the switch is preserved during the transition period.

DPLL Frequency Lock Detector

The operation of the frequency lock detector is identical to that of the phase lock detector. The only difference is that the fill or drain decision is based on the period deviation between the reference and feedback signals of the DPLL instead of the phase error at the output of the PFD.

The frequency lock detector uses a 24-bit frequency threshold register specified in units of picoseconds. Thus, the frequency threshold value extends from 10 ps to ±16.7 µs. It represents the magnitude of the difference in period between the reference and feedback signals at the input to the DPLL. For example, if the divided down reference signal is 80 kHz and the feedback signal is 79.32 kHz, the period difference is approximately 107.16 ns ($|1/80,000 - 1/79,320| \approx 107.16$ ns).

Frequency Clamp

The AD9554 digital PLL features a digital tuning word clamp that ensures that the digital PLL output frequency stays within a defined range. This feature is very useful to eliminate undesirable behavior in cases where the reference input clocks may be unpredictable.

The tuning word clamp is also useful to guarantee that the APLL never loses lock by ensuring that the APLL VCO frequency stays within its tuning range.

Frequency Tuning Word History

The AD9554 has the ability to track the history of the tuning word samples generated by the DPLL digital loop filter output. It does so by periodically computing the average tuning word value over a user-specified interval. This average tuning word is used during holdover mode to maintain the average frequency when no input references are present.

LOOP CONTROL STATE MACHINE

Switchover

Switchover occurs when the loop controller switches directly from one input reference to another. The AD9554 handles a reference switchover by briefly entering holdover mode, loading the new DPLL parameters, and then immediately recovering. During the switchover event, however, the AD9554 preserves the status of the lock detectors to avoid phantom unlock indications.

Holdover

The holdover state of the DPLL is typically used when none of the input references are present; although, the user can also manually engage holdover mode. In holdover mode, the output frequency remains constant. The accuracy of the AD9554 in holdover mode is dependent on the device programming and availability of the tuning word history.

Recovery from Holdover

When in holdover and a valid reference becomes available, the device exits holdover operation. The loop state machine restores the DPLL to closed-loop operation, locks to the selected reference, and sequences the recovery of all the loop parameters based on the profile settings for the active reference.

Note that, if the DPLL_x user holdover bit is set, the device does not automatically exit holdover when a valid reference is available. However, automatic recovery can occur after clearing the user holdover bit.

SYSTEM CLOCK (SYSCLK)

SYSCLK INPUTS

Functional Description

The SYSCLK circuit provides a low jitter, stable, high frequency clock for use by the rest of the chip. The XOA and XOB pins connect to the internal SYSCLK multiplier. The SYSCLK multiplier can synthesize the system clock by connecting a crystal resonator across the XOA and XOB input pins or by connecting a low frequency clock source. The optimal signal for the system clock input is either a crystal in the 50 MHz range or an ac-coupled square wave with 800 mV p-p amplitude.

SYSCLK Reference Frequency

For the AD9554 to function properly, enter the system clock reference frequency into Register 0x0202 to Register 0x0205. The ability of the AD9554 to accurately measure the frequency of the reference input depends on how accurately this register setting matches the frequency on the system clock input.

Choosing the SYSCLK Source

There are two internal paths for the SYSCLK input signal: crystal resonator (XTAL) and nonXTAL.

Using a TCXO for the system clock is a common use for the nonXTAL path. Applications requiring DPLL loop bandwidths of less than 50 Hz or high stability in holdover mode require a TCXO or oven controlled crystal oscillator (OCXO). As an alternative to the 49.152 MHz crystal for these applications, the AD9554 reference design uses a 19.2 MHz TCXO, which offers excellent holdover stability and a good combination of low jitter and low spurious content.

The differential receiver connected to the XOA and XOB pins is self-biased to a dc level of ~0.6 V, and ac coupling is strongly recommended to maintain a 50% input duty cycle. When a 3.3 V CMOS oscillator is in use, it is important to ac-couple and use a voltage divider to reduce the input high voltage to a maximum of 1.14 V. The target voltage swing is 800 mV p-p. See Figure 25 for details on connecting a 3.3 V CMOS TCXO to the system clock input.

The nonXTAL input path permits the user to provide an LVPECL, LVDS, CMOS, or sinusoidal low frequency clock for multiplication by the integrated SYSCLK PLL. However, when using a sinusoidal input signal, it is best to use a frequency of ≥20 MHz. Otherwise, the resulting low slew rate can lead to poor noise performance. Note that there is an optional 2× frequency multiplier to double the rate at the input to the SYSCLK PLL and potentially reduce the PLL in-band noise. However, to avoid exceeding the maximum PFD rate of 300 MHz, the 2× frequency multiplier is only for input frequencies less than 150 MHz. Note that using the doubler when the duty is not close to 50% results in higher spurious noise and may prevent the system clock PLL from locking.

The nonXTAL path also includes an input divider (M) that is programmable for divide-by-1, -2, -4, or -8. The purpose of the divider is to allow additional flexibility in setting the system clock frequency to avoid spurs in the output clocks.

The XTAL path enables the connection of a crystal resonator (typically 12 MHz to 50 MHz) across the XOA and XOB pins. An internal amplifier provides the negative resistance required to induce oscillation. The internal amplifier expects an AT cut, fundamental mode crystal with a 100 Ω maximum motional resistance. The following crystals, listed in alphabetical order, may meet these criteria. Analog Devices does not guarantee their operation with the AD9554, nor does Analog Devices endorse one crystal supplier over another. The AD9554 reference design uses a 49.152 MHz crystal, which is high performance, low spurious content, and readily available.

- AVX/Kyocera CX3225SB
- ECS, Inc. ECX-32
- Epson/Toyocom TSX-3225
- Fox FX3225BS
- NDK NX3225SA
- Siward SX-3225
- Suntsu SCM10B48-49.152 MHz

SYSCLK MULTIPLIER

The SYSCLK PLL multiplier is an integer-N design with an integrated VCO. It provides a means to convert a low frequency clock input to the desired system clock frequency, f_{SYS} (2250 MHz to 2415 MHz). The SYSCLK PLL multiplier accepts input signals of between 10 MHz and 268 MHz. The PLL contains a feedback divider (K) that is programmable for divide values between 4 and 255.

$$f_{SYS} = f_{OSC} \times \frac{SYSCLK\_KDIV}{SYSCLK\_JDIV}$$

where:
f_{OSC} is the frequency at the XOA and XOB pins.
SYSCLK_KDIV is the K divider value stored in Register 0x0200.
SYSCLK_JDIV is the system clock J1 divider that is determined by setting Register 0x0201[2:1].

If the system clock doubler is used, the value of SYSCLK_KDIV must be half of its original value.

The system clock multiplier features a simple lock detector that compares the time difference between the reference and feedback edges. The most common cause of the SYSCLK multiplier not locking is a non-50% duty cycle at the SYSCLK input while the system clock doubler is enabled.

System Clock Stability Timer

Because multiple blocks inside the AD9554 depend on the system clock being at a known frequency, the system clock must be stable before activating the monitors. At initial power-up, the system clock status is not known; therefore, it is reported as being unstable. After the system clock registers have been programmed and the SYSCLK VCO has been calibrated, the system clock PLL locks shortly thereafter.

When the SYSCLK PLL locks, a timer runs for the duration stored in the system clock stability period registers. If the locked condition is violated any time during this waiting period, the timer is reset and halted until a locked condition is reestablished. After the specified period elapses, the internal logic of the AD9554 reports the system clock as stable.

Note that any time the system clock stability timer is changed in Register 0x0206 through Register 0x0208, it is reset automatically. The system clock stability timer starts counting when the next IO_UPDATE is issued (assuming that the system clock PLL is locked).

OUTPUT ANALOG PLL (APLL)

There are four output analog PLLs (APLLs) on the AD9554. They provide the frequency upconversion from the digital PLL (DPLL) outputs. The frequency ranges for each APLL are in Table 11.

Each APLL also provides a noise filter on the DPLL output. The APLL reference input is the output of the DPLL. The feedback divider is an integer divider. The loop filter is partially integrated with one external 15 nF capacitor that connects to the internal LDO. In addition to the capacitor, there is an additional 0.22 µF capacitor from the LDO pin to ground. The nominal loop bandwidth for all four APLLs is 240 kHz.

The APLL_0 block diagram is shown in Figure 34. APLL_1 through APLL_3 are copies of APLL_0 with different VCO ranges. Each APLL_x input is connected to the respective DPLL_x output, and each APLL_x output is connected to the respective Px divider.

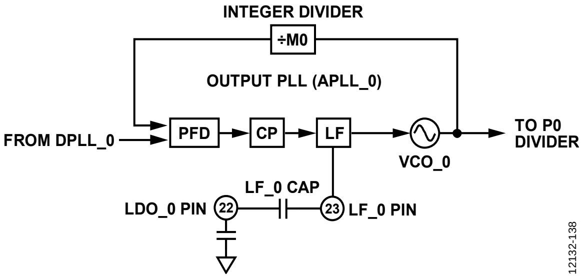


Figure 34. APLL_0 Block Diagram

APLL CONFIGURATION

The frequency wizard that is included in the evaluation software configures the APLL, and the user must not need to make changes to the APLL settings. However, there may be special cases where the user may want to adjust the APLL loop bandwidth to meet a specific phase noise requirement. The easiest way to change the APLL loop bandwidth is to adjust the APLL charge pump current, which is controlled in the following registers:

- Register 0x0430 (APLL_0)
- Register 0x0530 (APLL_1)
- Register 0x0630 (APLL_2)
- Register 0x0730 (APLL_3)

There is sufficient stability (68° of phase margin) in the APLL default settings to permit a broad range of adjustment without causing the APLL to be unstable.

APLL CALIBRATION

Calibration of the APLLs must be performed at startup and whenever the nominal input frequency to the APLL changes by more than ±100 ppm; although, the APLL maintains lock over voltage and temperature extremes without recalibration.

APLL calibration at startup is normally performed during initial register loading, see the detailed instructions in the Device Register Programming Using a Register Setup File section.

To recalibrate the APLL VCO after the chip has been running, first, input the new settings (if any). The user can calibrate APLL_0 without disturbing any of the other three APLLs (APLL_1, APLL_2, and APLL_3).

Use the following steps to recalibrate the APLL VCO. It is important to note that an IO_UPDATE (Register 0x000F = 0x01) is needed after each of these steps.

1. Ensure that the DPLL free run tuning word is set (Register 0x0A22[0] = 1b for DPLL_0,
   Register 0x0A42[0] = 1b for DPLL_1,
   Register 0x0A62[0] = 1b for DPLL_2, and
   Register 0x0A82[0] = 1b for DPLL_3).
2. Clear the desired APLL calibration bit (Register 0x0A20[1] = 0b for APLL_0,
   Register 0x0A40[1] = 0b for APLL_1,
   Register 0x0A60[1] = 0b for APLL_2, and
   Register 0x0A80[1] = 0b for APLL_3).
   Alternatively, the user can write Register 0xA00 = 0x00 to clear the calibrate all bit. This allows the user to set this bit in the next step to calibrate all four VCOs at the same time.
3. Set the desired APLL calibration bit (Register 0x0A20[1] = 1b for APLL_0,
   Register 0x0A40[1] = 1b for APLL_1,
   Register 0x0A60[1] = 1b for APLL_2, and
   Register 0x0A80[1] = 1b for APLL_3).
   Alternatively, the user can write Register 0xA00 = 0x02 to calibrate all four VCOs at the same time.
4. To ensure that the APLLs have locked, poll the APLL lock status (Register 0x0D20[3] = 1b indicates lock for APLL_0,
   Register 0x0D40[3] = 1b indicates lock for APLL_1,
   Register 0x0D60[3] = 1b indicates lock for APLL_2, and
   Register 0x0D80[3] = 1b indicates lock for APLL_3).
5. Ensure that the DPLL free run tuning word is cleared (Register 0x0A22[0] = 0b for DPLL_0,
   Register 0x0A42[0] = 0b for DPLL_1,
   Register 0x0A62[0] = 0b for DPLL_2, and
   Register 0x0A82[0] = 0b for DPLL_3).

CLOCK DISTRIBUTION

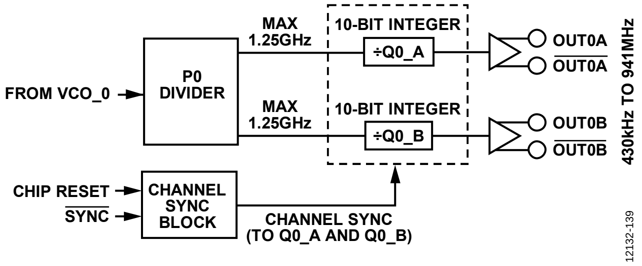


Figure 35. Clock Distribution Block Diagram from VCO_0 for the PLL_0

The AD9554 has four identical clock distribution sections for PLL_0 through PLL_3. See Figure 35 for a diagram of the clock distribution block for PLL_0.

CLOCK DIVIDERS

P Dividers

The first block in each clock distribution section is the P divider. The P divider divides the VCO output frequency down to a frequency of ≤1.25 GHz and has special circuitry to maintain a 50% duty cycle for any divide ratio.

The following registers contain the P divider settings:

- Register 0x0434[3:0] for PLL_0, P0 divider
- Register 0x0534[3:0] for PLL_1, P1 divider
- Register 0x0634[3:0] for PLL_2, P2 divider
- Register 0x0734[3:0] for PLL_3, P3 divider

Channel Dividers

The channel divider blocks, Q0_A and Q0_B through Q3_A and Q1_B are 10-bit integer dividers with a divide range of 1 to 1024. The channel divider block contains duty cycle correction that generates approximately 50% duty cycle for both even and odd divide ratios. The maximum input frequency to the channel dividers is 1.25 GHz.

The following registers contain the channel dividers:

- Register 0x0438 to Register 0x043A for Q0_A divider
- Register 0x043C to Register 0x043E for Q0_B divider
- Q1 dividers: same as Q0 but offset by 0x0100 registers
- Q2 dividers: same as Q0 but offset by 0x0200 registers
- Q3 dividers: same as Q0 but offset by 0x0300 registers

OUTPUT AMPLITUDE AND POWER-DOWN

The output drivers can be individually powered down. The output mode control (including power-down) can be found in the following registers:

- Register 0x0437[2:0] for OUT0A
- Register 0x043B[2:0] for OUT0B
- Register 0x0537[2:0] for OUT1A
- Register 0x053B[2:0] for OUT1B
- Register 0x0637[2:0] for OUT2A
- Register 0x063B[2:0] for OUT2B
- Register 0x0737[2:0] for OUT3A
- Register 0x073B[2:0] for OUT3B

The operating mode controls include the following:

- Output drive strength
- Output polarity
- Divide ratio
- Phase of each output channel

The HCSL drivers feature a programmable drive strength that allows the user to choose between a strong, high performance driver or a lower power setting with less electromagnetic interference (EMI) and crosstalk. The best setting is application dependent.

All outputs have three current settings that provide increased output amplitude in applications that require it. However, the only modes that support dc-coupling without termination at the destination are the 14 mA HCSL and 21 mA modes. The 28 mA mode must have either 50 Ω to ground on each leg or 100 Ω across the differential pair.

For applications where LVPECL levels are required, the user must choose the 28 mA mode, ac-couple the output signal, and provide 100 Ω termination across the differential pair at the destination. Damage to the output drivers can result if 28 mA mode is used without external termination resistors (either to ground or across the differential pair). See the Input/Output Termination Recommendations section for recommended termination schemes.

CLOCK DISTRIBUTION SYNCHRONIZATION

Divider Synchronization

The dividers in the channels can be synchronized with each other. At power-up, they are held static until a synchronization signal is initiated through the serial port, an EEPROM event, a DPLL locked synchronization. This mode of operation provides time for APLL calibration before the outputs are enabled.

A user initiated sync signal can also be supplied to the dividers at any time (as a manual synchronization) using an Mx pin.

A channel can be programmed to ignore the sync function. When programmed to ignore the sync function, the channel sync block issues a sync pulse immediately, and the channel ignores all other sync signals.

The digital logic triggers a sync event from one of the following sources:

- Register programming through serial port
- EEPROM programming
- A multifunction pin configured for the sync signal
- Other automatic conditions determined by the DPLL configuration: DPLL lock or reference clock synchronization

STATUS AND CONTROL

MULTIFUNCTION PINS (M0 TO M9)

The AD9554 has ten digital CMOS input/output pins (M0 to M9) that are configurable for a variety of uses. The function of these pins is programmable via the register map. Each pin can control or monitor an assortment of internal functions based on Register 0x0103 to Register 0x010C.

The Mx pins feature a special write detection logic that prevents these pins from behaving unpredictably when the Mx pins function changes. When the user writes to these registers, the existing Mx pin function stops. The new Mx pin function takes effect on the next IO_UPDATE (Register 0x000F = 0x01).

The Mx pins operate in one of four modes: active high CMOS, active low CMOS, open-drain PMOS, and open-drain NMOS.

Table 23. Mx Pins Four Modes of Operation

Setting	Mode	Description
00	Active high CMOS	When deasserted, the Mx pin is Logic 0. When asserted, the Mx pin is Logic 1, which is the default operating mode
01	Active low CMOS	When deasserted, the Mx pin is Logic 1. When asserted, the Mx pin is Logic 0.
10	Open-drain PMOS	When deasserted, the Mx pin is high impedance. When the Mx pin is asserted, it is active high; it requires an external pull-down resistor.
11	Open-drain NMOS	When deasserted, the Mx pin is high impedance. When the Mx pin is asserted, it is active low; it requires an external pull-up resistor.

To monitor an internal function with a multifunction pin, write a Logic 1 to the most significant bit of the register associated with the desired multifunction pin. The value of the seven least significant bits of the register defines the control function, as shown in Table 154.

To control an internal function with a multifunction pin, write a Logic 0 to the most significant bit of the register associated with the desired multifunction pin. The monitored function depends on the value of the seven least significant bits of the register, as shown in Table 155.

Note that each Mx pin has an open-drain mode that allows the user to perform logical AND and logical OR functions with the Mx pin outputs. For instance, it is possible to connect the IRQ lines of multiple AD9554s on one board together and to make the IRQ line the logical OR of each AD9554 IRQ line.

It is also possible to have an input function like IRQ clearing to be the logical combination of multiple inputs. For example, IRQ clearing is desired only if M2 is high and M3 is low, and either M0 is high or M1 is low.

In function form, this is the following:

Result = (M0 || !M1) && M2 && !M3

To accomplish this, set the M0 through M3 pins as the IRQ clearing function, and set the Mx pin modes of operation as the following:

- M0 = OR true signal (Register 0x100[1:0] = 10)
- M1 = OR inverted signal (Register 0x100[3:2] = 11)
- M2 = AND true signal (Register 0x100[5:4] = 00)
- M3 = AND inverted signal (Register 0x100[7:6] = 01)

IRQ FUNCTION

The AD9554 IRQ function can be assigned to any Mx pin. There are five IRQ categories: PLL0, PLL1, PLL2, PLL3, and common. This means an Mx pin can be set to respond only to IRQs that relate to one of the PLLs or to common functions. An Mx pin can also be set to respond to all IRQs.

The AD9554 asserts an IRQ when any bit in the IRQ monitor register (Register 0x0D08 to Register 0x0D16) is a Logic 1. Each bit in this register is associated with an internal function that is capable of producing an interrupt. Furthermore, each bit of the IRQ monitor register is the result of a logical AND of the associated internal interrupt signal and the corresponding bit in the IRQ mask register (Register 0x010F to Register 0x011D). That is, the bits in the IRQ mask registers have a one-to-one correspondence with the bits in the IRQ monitor registers. When an internal function produces an interrupt signal and the associated IRQ mask bit is set, the corresponding bit in the IRQ monitor register is set. Be aware that clearing a bit in the IRQ mask register removes only the mask associated with the internal interrupt signal. It does not clear the corresponding bit in the IRQ monitor register.

The IRQ function is edge triggered which means that if the condition that generated an IRQ (for example, loss of DPLL_0 lock) still exists after an IRQ is cleared, the IRQ does not reactivate until DPLL_0 lock is restored and lost again. However, if the IRQs are enabled when DPLL_0 is not locked, an IRQ is generated.

The IRQ function of an Mx pin is the result of a logical OR of all the IRQ monitor register bits. The AD9554 asserts an IRQ as long as any of the IRQ monitor register bits is a Logic 1. Note that it is possible to have multiple bits set in the IRQ monitor registers. Therefore, when the AD9554 asserts an IRQ, it may indicate an interrupt from several different internal functions. The IRQ monitor registers provide a way to interrogate the AD9554 to determine which internal function(s) produced the interrupt.

Typically, when the AD9554 asserts an IRQ, the user interrogates the IRQ monitor registers to identify the source of the interrupt request. After servicing an indicated interrupt, the user must clear the associated IRQ monitor register bit via the IRQ clearing registers (Address 0x0A05 to Address 0x0A14). The bits in the IRQ clearing registers have a one-to-one correspondence with the bits in the IRQ monitor registers.

Note that the IRQ clearing registers are autoclearing. The Mx pin associated with an IRQ remains asserted until the user clears all of the bits in the IRQ monitor registers that indicate an interrupt.

All IRQ monitor register bits can be cleared by setting the clear all IRQs bit in the IRQ register (Register 0x0A05). Note that the bits in Register 0x0A05 are autoclearing. Setting Bit 0 results in the deassertion of all IRQs. Alternatively, the user can program any of the multifunction pins to clear all IRQs, which allows the user to clear all IRQs by means of a hardware pin rather than by a serial input/output port operation.

WATCHDOG TIMER

The watchdog timer is a general-purpose programmable timer. To set the timeout period, the user writes to the 16-bit watchdog timer register (Address 0x010D to Address 0x010E). A value of 0x0000 in this register disables the timer. A nonzero value sets the timeout period in milliseconds, giving the watchdog timer a range of 1 ms to 65.535 sec. The relative accuracy of the timer is approximately 0.1% with an uncertainty of 0.5 ms.

If enabled, the timer runs continuously and generates a timeout event when the timeout period expires. The user has access to the watchdog timer status via the IRQ mechanism and the multifunction pins (M0 to M9). In the case of the multifunction pins, the timeout event of the watchdog timer is a pulse that lasts 96 system clock periods (which approximately 40 ns).

There are two ways to reset the watchdog timer (thereby preventing it from causing a timeout event). The first method is to write a Logic 1 to the autoclearing clear watchdog timer bit in the clear IRQ groups register (Register 0x0A05, Bit 7). Alternatively, the user can program any of the multifunction pins to reset the watchdog timer. When used in this way, the user can reset the timer by means of a hardware pin rather than by a serial input/output port operation.

EEPROM

EEPROM Overview

The AD9554 contains an EEPROM controller that allows the user to connect an external 2048-byte, electrically erasable, programmable read only memory (EEPROM). The AD9554 can be configured to perform a download at power-up via the multifunction pins, however, uploads and downloads can also be performed on demand via the EEPROM control registers (Address 0x0E00 to Address 0x0E03).

To enable the EEPROM I^{2}C controller, the M4 pin must be pulled high at power-up or reset.

To enable the I^{2}C EEPROM interface, pull the M4 pin high at power-up or reset. To load from the EEPROM at power-up or reset, pull the M3 pin high at power-up or reset.

When configured for external EEPROM operation, the M1 (SCL) and M2 pins (SDA) are open-drain NMOS, and external pull-up resistors are needed into for the I^{2}C EEPROM interface to function.

The EEPROM provides the ability to upload and download configuration settings to and from the register map. Figure 36 shows a functional diagram of the EEPROM.

Register 0x0E10 to Register 0x0E6F represent a 96-byte EEPROM storage sequence area (referred to as the scratchpad in this section) that enables the user to store a sequence of instructions for transferring data to the EEPROM from the device settings portion of the register map. Note that the default values for these registers provide a sample sequence for saving/retrieving all of the AD9554 EEPROM accessible registers. Figure 36 shows the connectivity between the EEPROM and the controller that manages the data transfer between the EEPROM and the register map.

The controller oversees the process of transferring EEPROM data to and from the register map. There are two modes of operation handled by the controller: saving data to the EEPROM (upload mode) or retrieving data from the EEPROM (download mode). In either case, the controller relies on a specific instruction set.

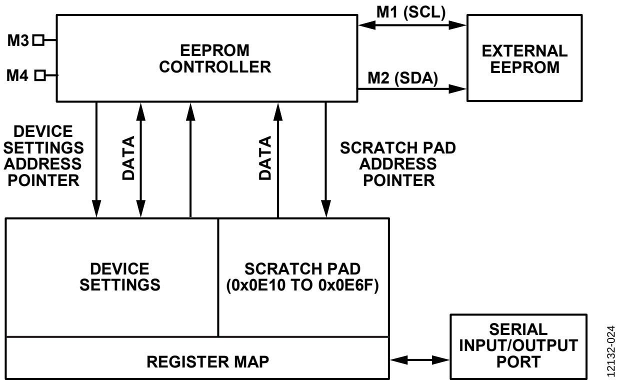


Figure 36. EEPROM Functional Diagram

EEPROM Instructions

Table 24 lists the EEPROM controller instruction set. The controller recognizes all instruction types, whether it is in upload or download mode, except for the pause instruction, which it only recognizes in upload mode.

The IO_UPDATE, calibrate, distribution sync, and end instructions are, for the most part, self-explanatory. The others, however, warrant further detail, as described in the EEPROM Data Instruction section and Table 24.

EEPROM Data Instruction

Data instructions are those that have a value from 0x00 to 0x7F. A data instruction tells the controller to transfer data between the EEPROM and the register map. The controller needs the following two parameters to carry out the data transfer:

- The number of bytes to transfer
- The register map starting address

The controller decodes the number of bytes to transfer directly from the data instruction itself by adding 1 to the value of the instruction.

For example, Data Instruction 0x1A has a decimal value of 26; therefore, the controller knows to transfer 27 bytes (one more than the value of the instruction). When the controller encounters a data instruction, it automatically reads the next two bytes because these contain the starting address of the AD9554 register map. The starting address is the LSB, and then the MSB. For example, storing five bytes at Starting Address 0x00FE is entered into the EEPROM buffer segment as 0x04, then 0xFE, and then 0x00.

Note that the internal EEPROM controller always starts at the register map starting address and counts upward, regardless of the mode of the main serial port.

As part of the transfer process during an EEPROM upload, the controller calculates a CRC-32 checksum and stores it at the end of the data transfer. As part of the transfer process during an EEPROM download, however, the controller again calculates the CRC-32 checksum and compares the newly calculated checksum with the one that was stored during the upload process. If an upload/download checksum pair does not match, the controller sets the EEPROM fault status bit. If the upload/download checksums match for all instructions encountered during a download sequence, the controller sets the EEPROM complete status bit.

Table 24. EEPROM Controller Instruction Set

Instruction Value (Hex)	Instruction Type	Bytes Needed	Description
0x00 to 0x7F	Data	3	A data instruction tells the controller to transfer data to or from the device settings part of the register map. A data instruction requires two additional bytes that, together, indicate a starting address in the register map. Encoded in the data instruction is the number of bytes to transfer, which is one more than the instruction value.
0x80	IO_UPDATE	1	The controller issues a soft IO_UPDATE (that is analogous to the user writing Register 0x000F = 0x01).
0x90	Calibrate all PLLs	1	The EEPROM controller initiates a calibration sequence to the SYSCLK PLL, as well as all of the APLLs, while downloading from the EEPROM. APLL calibration does not start until the SYSCLK PLL is stable.
0x91	Calibrate SYSCLK	1	When the controller encounters this instruction while downloading from the EEPROM, it initiates an SYSCLK calibration sequence.
0x92	Calibrate all APLLs	1	The controller initiates an APLL calibration sequence to all four APLLs while downloading from the EEPROM. APLL calibration is gated by the system clock being stable.
0x93/0x94/ 0x95/0x96	Calibrate APLL_0/APLL_1/ APLL_2/APLL_3	1	When the controller encounters this instruction while downloading from the EEPROM, it initiates an APLL_0/APLL_1/APLL_2/APLL_3 calibration sequence. APLL calibration is gated by the system clock being stable. 0x93 is for APLL_0, 0x94 is for APLL_1, and so on.
0x98	Set user free run mode (all PLLs)	1	When the controller encounters this instruction while downloading from the EEPROM, it forces all of the DPLLs into user free run mode. The force state is cleared automatically when EEPROM loading is complete. However, the user free run bits in the register map are not changed with this command and retain their programmed values.
0x99/0x9A/ 0x9B/0x9C	Set DPLL_0/ DPLL_1/DPLL_2/ DPLL_3 user free run mode	1	When the controller encounters this instruction while downloading from the EEPROM, it forces DPLL_0/DPLL_1/DPLL_2/DPLL_3 into user free run mode. The force state is cleared automatically when EEPROM loading is complete. However, the user free run bits in the register map are not changed with this command, and retain their programmed values.
0xA0	Distribution sync (all outputs)	1	When the controller encounters this instruction while downloading from the EEPROM, it issues a sync pulse to the PLL0, PLL1, PLL2, and PLL3 channel dividers. Note that the APLL associated with a given channel must be locked before the sync pulse reaches the output dividers of that channel.
0xA1/0xA2/ 0xA3/0xA4	Distribution sync (PLL0/PLL1/PLL2/ PLL3 outputs)	1	When the controller encounters this instruction while downloading from the EEPROM, it issues a sync pulse to the PLL0/PLL1/PLL2/PLL3 channel dividers. Note that, unless overridden, this sync pulse is gated by the APLL lock detect signal associated with that channel.
0xB0	Clear condition	1	0xB0 is the null condition instruction.
0xB1 to 0xBF	Condition	1	0xB1 to 0xBF are condition instructions and correspond to Condition 1 through Condition 15, respectively.
0xFE	Pause	1	When the controller encounters this instruction in the scratchpad while uploading to the EEPROM, it resets the scratchpad address pointer and holds the EEPROM address pointer at its last value. This allows storage of more than one instruction sequence in the EEPROM. The controller does not copy this instruction to the EEPROM during upload.
0xFF	End of data	1	When the controller encounters this instruction in the scratchpad while uploading to the EEPROM, it resets both the scratchpad address pointer and the EEPROM address pointer and then enters an idle state. When the controller encounters this instruction while downloading from the EEPROM, it resets the EEPROM address pointer and then enters an idle state.

The Condition and Pause Instructions

Condition instructions are those that have a value from 0xB0 to 0xBF. The 0xB1 to 0xBF condition instructions represent Condition 1 to Condition 15, respectively. The 0xB0 condition instruction is special because it represents the null condition.

A pause instruction, like an end instruction, is stored at the end of a sequence of instructions in the scratchpad. When the controller encounters a pause instruction during an upload sequence, it keeps the EEPROM address pointer at its last value. Then, the user can store a new instruction sequence in the scratchpad and upload the new sequence to the EEPROM. The new sequence is stored in the EEPROM address locations immediately following the previously saved sequence. This process is repeatable until an upload sequence contains an end instruction. The pause instruction is also useful when used in conjunction with condition processing. It allows the EEPROM to contain multiple occurrences of the same registers, with each occurrence linked to a set of conditions.

EEPROM Upload

o upload data to the EEPROM, take the following steps:

1. Program the AD9554 to the desired configuration.
2. Write Register 0x0FFF = 0xF9 to enable the manual V_{CAL} reference programming.
3. Write Register 0x0E00 = 0x03 (for 400 kHz transfer rate) or 0x01 for 100 kHz EEPROM transfer rate.
4. Write Register 0x0E02 = 0x01 to initiate the EEPROM data storage process. This bit is autoclearing.
5. Write Register 0x0FFF = 0x00 to disable accidental writes to registers addresses higher than Register 0x0FFF.

During the upload process, the controller reads the scratchpad data byte by byte, starting at Register 0x0E10 and incrementing the scratchpad address pointer, as it goes, until it reaches a pause or end instruction.

As the controller reads the scratchpad data, it transfers the data from the scratchpad to the EEPROM (byte by byte) and increments the EEPROM address pointer accordingly, unless it encounters a data instruction. A data instruction tells the controller to transfer data from the device settings portion of the register map to the EEPROM. The number of bytes to transfer is encoded within the data instruction, and the starting address for the transfer appears in the next two bytes in the scratchpad.

When the controller encounters a data instruction, it stores the instruction in the EEPROM, increments the EEPROM address pointer, decodes the number of bytes to be transferred, and increments the scratchpad address pointer. Then, it retrieves the next two bytes from the scratchpad (the target address) and increments the scratchpad address pointer by 2. Next, the controller transfers the specified number of bytes from the register map (beginning at the target address) to the EEPROM.

When it completes the data transfer, the controller stores a CRC-32 checksum. Note that, when the controller transfers data associated with an active register, it actually transfers the buffered contents of the register (refer to the Buffered/Active Registers section for details on the difference between buffered and active registers). The use of the buffered registers (as opposed to the live registers) allows for the transfer of nonzero autoclearing register contents.

Conditional processing does not occur during an upload sequence.

Manual EEPROM Download

An EEPROM download results in a data transfer from the external EEPROM to the device register map. To download data, set the autoclearing load from EEPROM bit (Register 0x0E03, Bit 0). This commands the controller to initiate the EEPROM download process. During download, the controller reads the EEPROM data byte by byte, incrementing the EEPROM address pointer as it goes, until it reaches an end instruction. As the controller reads the EEPROM data, it executes the stored instructions, which includes transferring stored data to the device settings portion of the register map whenever it encounters a data instruction.

Note that conditional processing is applicable only when downloading manually. The condition value is stored in Bits[3:0] of Register 0x0E01. Automatic downloads use a condition value of 1.

Automatic EEPROM Download

If the M3 pin and M4 pin are high following a power-up, a hard reset using the $\overline{\text{RESET}}$ pin, or a soft reset (Register 0x0000, Bit 7 = 1), the instruction sequence stored in the external EEPROM executes automatically.

If M4 is high and M3 is low, the external EEPROM I^2C port is enabled on the M1 and M2 pins; however, the contents of the external EEPROM are not loaded. In that case, factory defaults are used.

If M4 is low, the M3 status is ignored, and the external EEPROM I^2C port is disabled. The M1 and M2 pins can be used for other status and control functions.

Important Update to EEPROM Programming Sequence

The following changes must be applied to the default EEPROM storage sequence in Register 0x0E10 to Register 0x0E6F. The AD9554 evaluation software, Version 1.0.3.0 or later, checks these registers and prompts the user to update these registers in the register programming file to this sequence:

1. Register 0x0E10 = 0x01 (write 2 bytes)
2. Register 0x0E11 = 0x00 (at Register 0x0B00)
3. Register 0x0E12 = 0x0B
4. Register 0x0E13 = 0x98 (Set all channels to Freerun mode)
5. Register 0x0E14 = 0x01 (write 2 bytes)
6. Register 0x0E15 = 0xFE (at Register 0x00FE)
7. Register 0x0E16 = 0x00
8. Register 0x0E17 = 0x1F (write 32 bytes)
9. Register 0x0E18 = 0x00 (at Register 0x0100)
10. Register 0x0E19 = 0x01
11. Register 0x0E1A = 0x08 (write 9 bytes)
12. Register 0x0E1B = 0x00 (at Register 0x0200)
13. Register 0x0E1C = 0x02
14. Register 0x0E1D = 0x80 (input/output update)
15. Register 0x0E1E = 0x91 (calibrate SYSCLK)
16. Register 0x0E1F = 0x1E (write 32 bytes)
17. Register 0x0E20 = 0x00 (at Register 0x0300)
18. Register 0x0E21 = 0x03
19. Register 0x0E22 = 0x1E (write 31 bytes)
20. Register 0x0E23 = 0x20 (at Register 0x0320)
21. Register 0x0E24 = 0x03
22. Register 0x0E25 = 0x1E (write 31 bytes)
23. Register 0x0E26 =0x40 (at Register 0x0340)
24. Register 0x0E27 = 0x03
25. Register 0x0E28 = 0x1E (write 31 bytes)
26. Register 0x0E29 = 0x60 (at Register 0x0360)
27. Register 0x0E2A = 0x03
28. Register 0x0E2B = 0x1E (write 31 bytes)
29. Register 0x0E2C = 0x00 (at Register 0x0400)
30. Register 0x0E2D = 0x04
31. Register 0x0E2E = 0x0E (write 15 bytes)
32. Register 0x0E2F = 0x30 (at Register 0x0430)
33. Register 0x0E30 = 0x04
34. Register 0x0E31 = 0x33 (write 52 bytes)
35. Register 0x0E32 = 0x40 (at Register 0x0440)
36. Register 0x0E33 = 0x04
37. Register 0x0E34 = 0x1E (write 31 bytes)
38. Register 0x0E35 = 0x00 (at Register 0x0500)
39. Register 0x0E36 = 0x05
40. Register 0x0E37 = 0x0E (write 15 bytes)
41. Register 0x0E38 = 0x30 (at Register 0x0530)
42. Register 0x0E39 = 0x05
43. Register 0x0E3A = 0x33 (write 52 bytes)
44. Register 0x0E3B = 0x40 (at Register 0x0540)
45. Register 0x0E3C = 0x05
46. Register 0x0E3D = 0x1E (write 31 bytes)
47. Register 0x0E3E = 0x00 (at Register 0x0600)
48. Register 0x0E3F = 0x06
49. Register 0x0E40 = 0x0E (write 15 bytes)
50. Register 0x0E41 = 0x30 (at Register 0x0630)
51. Register 0x0E42 = 0x06
52. Register 0x0E43 = 0x33 (write 52 bytes)
53. Register 0x0E44 = 0x40 (at Register 0x0640)
54. Register 0x0E45 = 0x06
55. Register 0x0E46 = 0x1E (write 31 bytes)
56. Register 0x0E47 = 0x00 (at Register 0x0700)
57. Register 0x0E48 = 0x07
58. Register 0x0E49 = 0x0E (write 15 bytes)
59. Register 0x0E4A = 0x30 (at Register 0x0730)
60. Register 0x0E4B = 0x07
61. Register 0x0E4C = 0x33 (write 52 bytes)
62. Register 0x0E4D = 0x40 (at Register 0x0740)
63. Register 0x0E4E = 0x07
64. Register 0x0E4F = 0x24 (write 37 bytes)
65. Register 0x0E50 = 0x00 (at Register 0x0A00)
66. Register 0x0E51 = 0x0A
67. Register 0x0E52 = 0x04 (write 5 bytes)
68. Register 0x0E53 = 0x40 (at Register 0x0A40)
69. Register 0x0E54 = 0x0A
70. Register 0x0E55 = 0x04 (write 5 bytes)
71. Register 0x0E56 = 0x60 (at Register 0x0A60)
72. Register 0x0E57 = 0x0A
73. Register 0xE58 = 0x04 (write 5 bytes)
74. Register 0xE59 = 0x80 (at Register 0x0A80)
75. Register 0xE5A = 0x0A
76. Register 0xE5B = 0x80 (input/output update)
77. Register 0xE5C = 0x00 (write 1 byte)
78. Register 0xE5D = 0xFF (at Register 0x0FFF)
79. Register 0xE5E = 0x0F
80. Register 0xE5F = 0x00 (write 1 byte)
81. Register 0xE60 = 0x88 (at Register 0x1488)
82. Register 0xE61 = 0x14
83. Register 0xE62 = 0x00 (write 1 byte)
84. Register 0xE63 = 0x88 (at Register 0x1588)
85. Register 0xE64 = 0x15
86. Register 0xE65 = 0x00 (write 1 byte)
87. Register 0xE66 = 0x88 (at Register 0x1688)
88. Register 0xE67 = 0x16
89. Register 0xE68 = 0x00 (write 1 byte)
90. Register 0xE69 = 0x88 (at Register 0x1788)
91. Register 0xE6A = 0x17
92. Register 0xE6B = 0x80 (input/output update)
93. Register 0xE6C = 0x92 (calibrate all APLLs)
94. Register 0xE6D = 0xA0 (sync all outputs)
95. Register 0xE6E = 0xFF (end of data)
96. Register 0xE6F = 0x55 (This register is past the end of the data command in R0x0E6E and is ignored.)

SERIAL CONTROL PORT

The AD9554 serial control port is a flexible, synchronous serial communications port that provides a convenient interface to many industry-standard microcontrollers and microprocessors. The AD9554 serial control port is compatible with most synchronous transfer formats, including I^{2}C, Motorola SPI, and Intel SSR protocols. The serial control port allows read/write access to the AD9554 register map.

The AD9554 uses the Analog Devices unified SPI protocol (see Analog Devices Serial Control Interface Standard). The unified SPI protocol guarantees that all new Analog Devices products using the unified protocol have consistent serial port characteristics. The SPI port configuration is programmable via Register 0x0000. This register is a part of the SPI control logic rather than in the register map and is distinct from the I^{2}C Register 0x0000.

Unified SPI differs from the SPI port found on older products like the AD9557 and AD9558 in the following ways:

- Unified SPI does not have byte counts. A transfer is terminated when the $\overline{CS}$ pin goes high. The W1 and W0 bits in the traditional SPI become the A12 and A13 bits of the register address. This is similar to streaming mode in the traditional SPI.
- The address ascension bit (Register 0x0000) controls whether register addresses are automatically incremented or decremented regardless of the LSB/MSB first setting. In traditional SPI, LSB first dictated autoincrements and MSB first dictated autodecrements of the register address.
- Devices that adhere to the unified serial port have a consistent structure of the first 16 register addresses.

Although the AD9554 supports both the SPI and I^{2}C serial port protocols, only one is active following power-up (as determined by the M0, M5, M6, and M7 multifunction pins during the start-up sequence). The only way to change the serial port protocol is to reset (or power cycle) the device.

SPI/I^{2}C PORT SELECTION

Because the AD9554 supports both SPI and I^{2}C protocols, the active serial port protocol depends on the logic state of M0, M5, M6, and M7 pins at reset or power-on. See Table 22 for the I^{2}C address assignments.

SPI SERIAL PORT OPERATION

Pin Descriptions

The SCLK (serial clock) pin serves as the serial shift clock. This pin is an input. SCLK synchronizes serial control port read and write operations. The rising edge SCLK registers write data bits, and the falling edge registers read data bits. The SCLK pin supports a maximum clock rate of 50 MHz.

The SPI port supports both 3-wire (bidirectional) and 4-wire (unidirectional) hardware configurations and both MSB-first and LSB-first data formats. Both the hardware configuration and data format features are programmable. The 3-wire mode uses the SDIO (serial data input/output) pin for transferring data in both directions. The 4-wire mode uses the SDIO pin for transferring data to the AD9554, and the SDO pin for transferring data from the AD9554.

The $\overline{CS}$ (chip select) pin is an active low control that gates read and write operations. Assertion (active low) of the $\overline{CS}$ pin initiates a write or read operation to the AD9554 SPI port. Any number of data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented based on the setting of the address ascension bit (Register 0x0000). $\overline{CS}$ must be deasserted at the end of the last byte transferred, thereby ending the stream mode. This pin is internally connected to a 10 kΩ pull-up resistor. When $\overline{CS}$ is high, the SDIO and SDO pins go into a high impedance state.

Implementation Specific Details

A detailed description of the unified SPI protocol can be found in the AN-877 Application Note, which covers items such as timing, command format, and addressing.

The following product specific items are defined in the unified SPI protocol:

- Analog Devices unified SPI protocol revision: 1.0
- Chip type: 0x5
- Product ID: 0x009
- Physical layer: 3- and 4-wire supported and 1.5 V, 1.8 V, and 2.5 V operation supported
- Optional single-byte instruction mode: not supported
- Data link: not used
- Control: not used

Communication Cycle—Instruction Plus Data

The unified SPI protocol consists of a two-part communication cycle. The first part is a 16-bit instruction word that is coincident with the first 16 SCLK rising edges and a payload. The instruction word provides the AD9554 serial control port with information regarding the payload. The instruction word includes the $R/\overline{W}$ bit that indicates the direction of the payload transfer (that is, a read or write operation). The instruction word also indicates the starting register address of the first payload byte.

Write

If the instruction word indicates a write operation, the payload is written into the serial control port buffer of the AD9554. Data bits are registered on the rising edge of SCLK. Generally, it does not matter what data is written to blank registers; however, it is customary to use 0s. Note that the user must verify that all reserved registers within a specific range have a default value of 0x00; however, Analog Devices makes every effort to avoid having reserved registers with nonzero default values.

Most of the serial port registers are buffered (see the Buffered/Active Registers section for details on the difference between buffered and active registers). Therefore, data written into buffered registers does not take effect immediately. An additional operation is needed to transfer buffered serial control port contents to the registers that actually control the device. This transfer is accomplished with an IO_UPDATE operation, which is performed in one of two ways. One method is to write a Logic 1 to Register 0x000F, Bit 0 (this bit is an autoclearing bit). The other method is to use an external signal via an appropriately programmed multifunction pin. The user can change as many register bits as desired before executing an IO_UPDATE. The IO_UPDATE operation transfers the buffer register contents to their active register counterparts.

Read

If the instruction word indicates a read operation, the next N × 8 SCLK cycles clock out the data starting from the address specified in the instruction word. N is the number of data bytes read. The readback data is driven to the pin on the falling edge and must be latched on the rising edge of SCLK. Blank registers are not skipped over during readback.

A readback operation takes data from either the serial control port buffer registers or the active registers, as determined by Register 0x0001, Bit 5.

SPI Instruction Word (16 Bits)

The MSB of the 16-bit instruction word is R/$\overline{W}$, which indicates whether the instruction is a read or a write. The next 15 bits are the register address (A14 to A0), which indicates the starting register address of the read/write operation (see Table 26). Note that A14 and A13 are ignored and treated as zeros in the AD9554 because there are no registers that require more than 13 address bits.

SPI MSB-/LSB-First Transfers

The AD9554 instruction word and payload can be MSB first or LSB first. The default for the AD9554 is MSB first. The LSB first mode can be set by writing a 1 to Register 0x0000, Bit 6. Immediately after the LSB first bit is set, subsequent serial control port operations are LSB first.

Address Ascension

If the address ascension bit (Register 0x0000, Bit 5) is zero, the serial control port register address decrements from the specified starting address toward Address 0x0000.

If the address ascension bit (Register 0x0000, Bit 5) is one, the serial control port register address increments from the starting address toward Address 0x0FFF. Reserved addresses are not skipped during multibyte input/output operations; therefore, write the default value to a reserved register and 0s to unmapped registers. Note that it is more efficient to issue a new write command than to write the default value to more than two consecutive reserved (or unmapped) registers.

Table 25. Streaming Mode (No Addresses Skipped)

Address Ascension	Stop Sequence
Increment	0x0000 … 0x0FFF
Decrement	0x0FFF … 0x0000

Table 26. Serial Control Port, 16-Bit Instruction Word

MSB **LSB**

I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R/$\overline{W}$	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

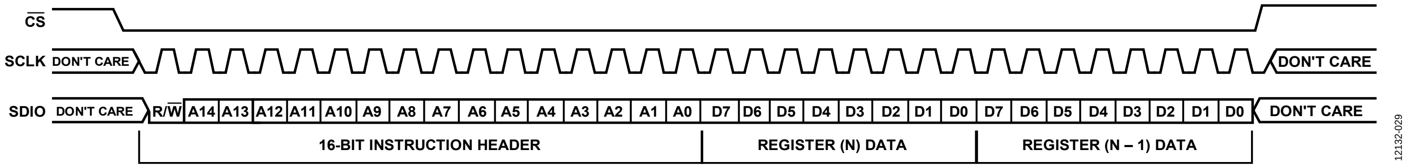


Figure 37. Serial Control Port Write—MSB First, Address Decrement, Two Bytes of Data

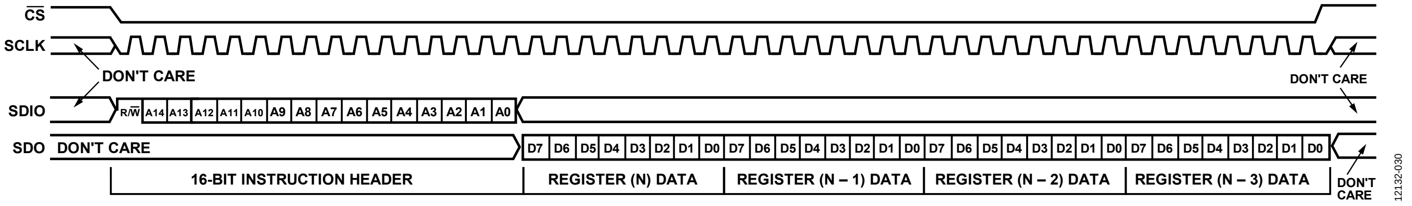


Figure 38. Serial Control Port Read—MSB First, Address Decrement, Four Bytes of Data

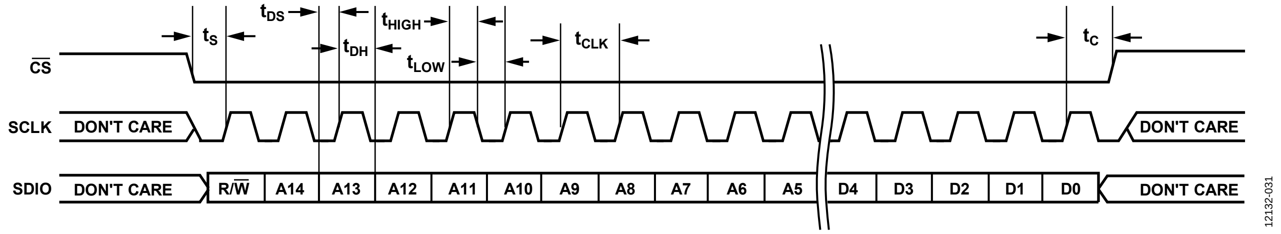


Figure 39. Timing Diagram for Serial Control Port Write—MSB First

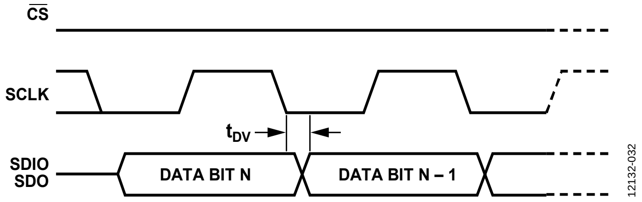


Figure 40. Timing Diagram for Serial Control Port Register Read—MSB First

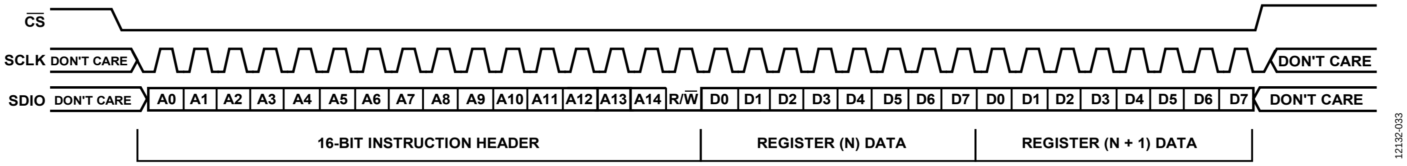


Figure 41. Serial Control Port Write—LSB First, Address Increment, Two Bytes of Data

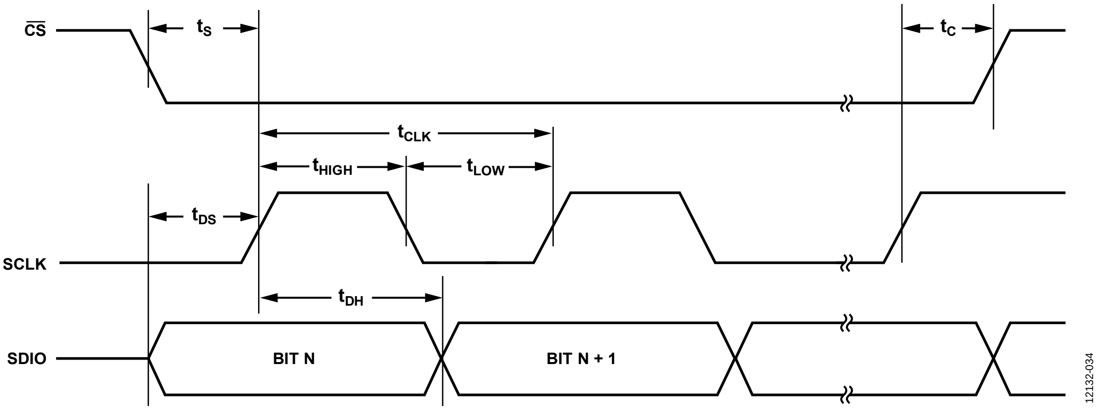


Figure 42. Serial Control Port Timing—Write

Table 27. Serial Control Port Timing

Parameter	Description
t_{DS}	Setup time between data and the rising edge of SCLK
t_{DH}	Hold time between data and the rising edge of SCLK
t_{CLK}	Period of the clock
t_S	Setup time between the $\overline{CS}$ falling edge and the SCLK rising edge (start of the communication cycle)
t_C	Setup time between the SCLK rising edge and $\overline{CS}$ rising edge (end of the communication cycle)
t_{HIGH}	Minimum period that SCLK must be in a logic high state
t_{LOW}	Minimum period that SCLK must be in a logic low state
t_{DV}	SCLK to valid SDIO (see Figure 40)

I²C SERIAL PORT OPERATION

The I²C interface is popular because it requires only two pins and easily supports multiple devices on the same bus. Its main disadvantage is programming speed, which is 400 kbps maximum. The AD9554 I²C port design uses the I²C fast mode; however, it supports both the 100 kHz standard mode and 400 kHz fast mode.

In an effort to support 1.5 V, 1.8 V, and 2.5 V I²C operation, the AD9554 does not strictly adhere to every requirement in the original I²C specification. In particular, specifications such as slew rate limiting and glitch filtering are not implemented. Therefore, the AD9554 is I²C compatible, but may not be fully I²C compliant.

The AD9554 I²C port consists of a serial data line (SDA) and a serial clock line (SCL). In an I²C bus system, the AD9554 is connected to the serial bus (data bus SDA and clock bus SCL) as a slave device; that is, no clock is generated by theAD9554. The AD9554 uses direct 16-bit memory addressing instead of more common 8-bit memory addressing.

The AD9554 allows up to seven unique slave devices to occupy the I²C bus. These are accessed via a 7-bit slave address transmitted as part of an I²C packet. Only the device with a matching slave address responds to subsequent I²C commands. Table 22 lists the supported device slave addresses.

I²C Bus Characteristics

A summary of the various I²C abbreviations appears in Table 28.

Table 28. I²C Bus Abbreviation Definitions

Abbreviation	Definition
S	Start
Sr	Repeated start
P	Stop
A	Acknowledge
$\overline{A}$	Nonacknowledge
$\overline{W}$	Write
R	Read

The transfer of data is shown in Figure 43. One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can change only when the clock signal on the SCL line is low.

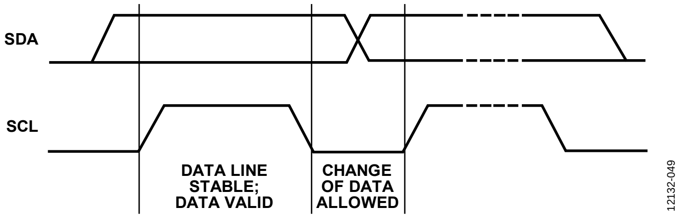


Figure 43. Valid Bit Transfer

Start/stop functionality is shown in Figure 44. The start condition is characterized by a high to low transition on the SDA line while SCL is high. The master always generates the start condition to initialize a data transfer. The stop condition is characterized by a low to high transition on the SDA line while SCL is high. The master always generates the stop condition to terminate a data transfer. Every byte on the SDA line must be eight bits long. Each byte must be followed by an acknowledge bit; bytes are sent MSB first.

The acknowledge bit (A) is the ninth bit attached to any 8-bit data byte. An acknowledge bit is always generated by the receiving device (receiver) to inform the transmitter that the byte has been received. It is done by pulling the SDA line low during the ninth clock pulse after each 8-bit data byte.

The nonacknowledge bit ($\overline{A}$) is the ninth bit attached to any 8-bit data byte. A nonacknowledge bit is always generated by the receiving device (receiver) to inform the transmitter that the byte has not been received. It is done by leaving the SDA line high during the ninth clock pulse after each 8-bit data byte. After issuing a nonacknowledge bit, the AD9554 I²C state machine goes into an idle state.

Data Transfer Process

The master initiates data transfer by asserting a start condition, which indicates that a data stream follows. All I²C slave devices connected to the serial bus respond to the start condition.

The master then sends an 8-bit address byte over the SDA line, consisting of a 7-bit slave address (MSB first) plus an R/$\overline{W}$ bit. This bit determines the direction of the data transfer, that is, whether data is written to or read from the slave device (0 = write and 1 = read).

The peripheral whose address corresponds to the transmitted address responds by sending an acknowledge bit. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is 0, the master (transmitter) writes to the slave device (receiver). If the R/$\overline{W}$ bit is 1, the master (receiver) reads from the slave device (transmitter).

The format for these commands is described in the Data Transfer Format section.

Data is then sent over the serial bus in the format of nine clock pulses, one data byte (eight bits) from either master (write mode) or slave (read mode) followed by an acknowledge bit from the receiving device. The number of bytes that can be transmitted per transfer is unrestricted. In write mode, the first two data bytes immediately after the slave address byte are the internal memory (control registers) address bytes, with the high address byte first. This addressing scheme gives a memory address of up to $2^{16} - 1 = 65,535$. The data bytes after these two memory address bytes are register data written to or read from the control registers. In read mode, the data bytes after the slave address byte are register data written to or read from the control registers.

When all the data bytes are read or written, stop conditions are established. In write mode, the master (transmitter) asserts a stop condition to end data transfer during the clock pulse following the acknowledge bit for the last data byte from the slave device (receiver). In read mode, the master device (receiver) receives the last data byte from the slave device (transmitter) but does not pull SDA low during the ninth clock pulse. This is known as a nonacknowledge bit.

By receiving the nonacknowledge bit, the slave device knows that the data transfer is finished and enters idle mode. The master then takes the data line low during the low period before the 10th clock pulse, and high during the 10th clock pulse to assert a stop condition.

A start condition can be used in place of a stop condition. Furthermore, a start or stop condition can occur at any time, and partially transferred bytes are discarded.

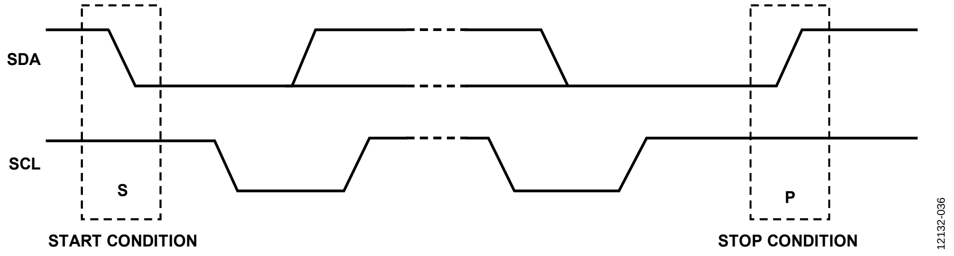


Figure 44. Start and Stop Conditions

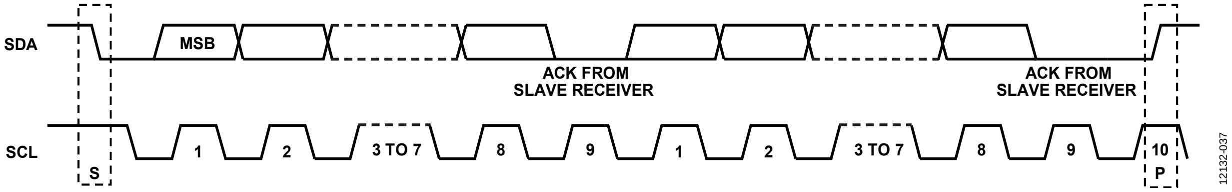


Figure 45. Acknowledge Bit

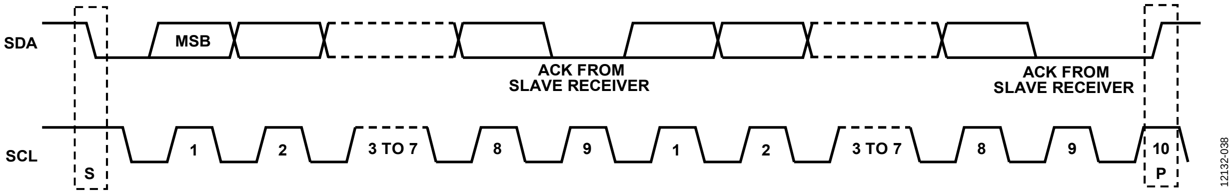


Figure 46. Data Transfer Process (Master Write Mode, 2-Byte Transfer)

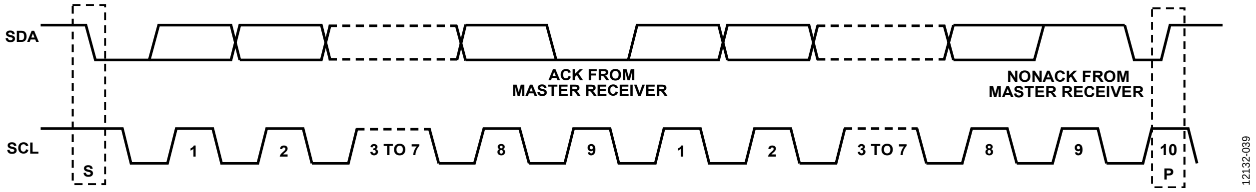


Figure 47. Data Transfer Process (Master Read Mode, 2-Byte Transfer), First Acknowledge From Slave

Data Transfer Format

The write byte format writes a register address to the RAM starting from the specified RAM address.

S	Slave address	$\overline{W}$	A	RAM address high byte	A	RAM address low byte	A	RAM Data 0	A	RAM Data 1	A	RAM Data 2	A	P

The send byte format sets up the register address for subsequent reads.

S	Slave address	$\overline{W}$	A	RAM address high byte	A	RAM address low byte	A	P

The receive byte format reads the data byte(s) from RAM starting from the current address.

S	Slave address	R	A	RAM Data 0	A	RAM Data 1	A	RAM Data 2	$\overline{A}$	P

The read byte format is the combined format of the send byte and the receive byte.

S	Slave address	$\overline{W}$	A	RAM address high byte	A	RAM address low byte	A	Sr	Slave address	R	A	RAM Data 0	A	RAM Data 1	A	RAM Data 2	$\overline{A}$	P

I²C Serial Port Timing

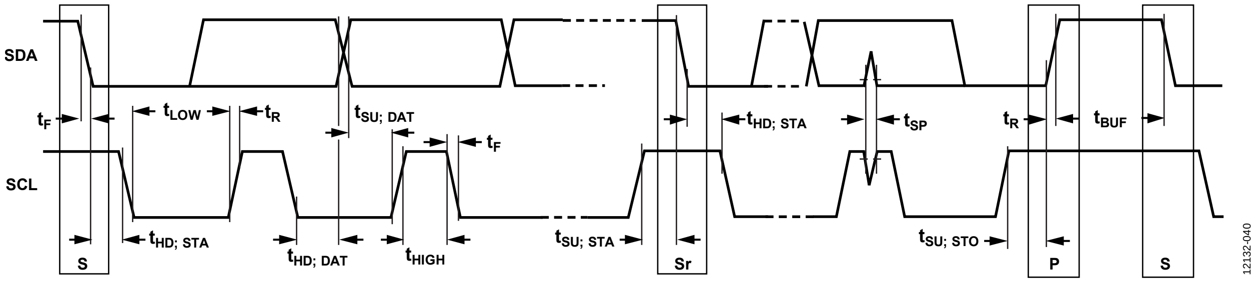


Figure 48. I²C Serial Port Timing

Table 29. I²C Timing Definitions

Parameter	Description
f_{SCL}	Serial clock
t_{BUF}	Bus free time between stop and start conditions
$t_{HD; STA}$	Repeated hold time start condition
$t_{SU; STA}$	Repeated start condition setup time
$t_{SU; STO}$	Stop condition setup time
$t_{HD; DAT}$	Data hold time
$t_{SU; DAT}$	Data setup time
t_{LOW}	SCL clock low period
t_{HIGH}	SCL clock high period
t_R	Minimum/maximum receive SCL and SDA rise time
t_F	Minimum/maximum receive SCL and SDA fall time
t_{SP}	Pulse width of voltage spikes that must be suppressed by the input filter

PROGRAMMING THE INPUT/OUTPUT REGISTERS

The register map (see Table 32) spans an address range from 0x0000 through 0x1788. Each address provides access to one byte (eight bits) of data. Each individual register is identified by its four digit hexadecimal address (for example, Register 0x0A23). In some cases, a group of addresses collectively defines a register.

In general, when a group of registers defines a control parameter, the LSB of the value resides in the D0 position of the register with the lowest address. The bit weight increases right to left, from the lowest register address to the highest register address.

BUFFERED/ACTIVE REGISTERS

There are two copies of most registers: buffered and active. The value in the active registers is the one that is in use. The buffered registers are the ones that take effect the next time the user writes 0x01 to Register 0x000F (IO_UPDATE). Buffering the registers allows the user to update a group of registers (like the APLL settings) simultaneously, avoiding the potential of unpredictable behavior in the device. Registers with an L in the option column of the register map (see Table 32) are live, meaning that they take effect the moment the serial port transfers that data byte.

WRITE DETECT REGISTERS

A Wx (where x equals 1 to 8) in the option column of the register map (see Table 32) identifies a register with write detection. These registers contain additional logic to avoid glitches or unwanted operation.

Table 30. Register Write Detection Description

Option	Register Operation
W1	When these registers are written to, the lock detector immediately declares it is unlocked. The lock detection restarts when the next IO_UPDATE occurs.
W2	After these registers are written to, the DPLL faults the reference input and automatically enters holdover for one PFD cycle (and then exits) when an IO_UPDATE is issued. However, this action is only performed if the written register belongs to the actively selected reference.
W3	After these registers are written to, the DPLL lock detector unlocks.
W5	The watchdog timer resets automatically when these registers are written to and then resumes counting on the next IO_UPDATE.
W6	The system clock stability timer is automatically reset when these registers are changed and then resumes counting on the next IO_UPDATE. (Note that the SYSCLK stability timer starts only after the system clock is locked.
W7	If these registers are written to while they are assigned to an existing function, the existing function stops immediately. The new function starts when the next IO_UPDATE occurs.
W8	Almost identical to W2; however, the DPLL must be in demapping mode.

AUTOCLEAR REGISTERS

An A in the option column of the register map (see Table 32) identifies an autoclearing register. Typically, the active value for an autoclearing register takes effect following an IO_UPDATE. The bit is cleared by the internal device logic upon completion of the prescribed action.

REGISTER ACCESS RESTRICTIONS

Read and write access to the register map may be restricted, depending on the register in question, the source and direction of access, and the current state of the device. Each register can be classified into one or more access types. When more than one type applies, the most restrictive condition is the one that applies.

When access is denied to a register, all attempts to read the register return a 0 byte, and all attempts to write to the register are ignored. Access to nonexistent registers is handled in the same way as for a denied register.

Regular Access

Registers with regular access do not fall into any other category. Both read and write access to registers of this type can be from either the serial ports or EEPROM controller. However, only one of these sources can have access to a register at any given time (access is mutually exclusive). When the EEPROM controller is active, in either upload or download mode, it has exclusive access to these registers.

Read Only Access

An R in the option column of the register map (see Table 32) identifies read only registers. Serial port access is available at all times, including when the EEPROM controller is active. Note that read only registers (R) are inaccessible to the EEPROM as well.

Exclusion from EEPROM Access

An E in the option column of the register map (see Table 32) identifies a register with contents that are inaccessible to the EEPROM. That is, the contents of this type of register cannot be transferred directly to the EEPROM or vice versa. Note that read only registers (R) are inaccessible to the EEPROM as well.

THERMAL PERFORMANCE

Table 31. Thermal Parameters for the 72-Lead LFCSP Package

Symbol	Thermal Characteristic Using a JEDEC 51-7 Plus JEDEC 51-5 2S2P Test Board[1]	Value[2]	Unit
θ_{JA}	Junction-to-ambient thermal resistance, 0.0 m/sec airflow per JEDEC JESD51-2 (still air)	20.0	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance, 1.0 m/sec airflow per JEDEC JESD51-6 (moving air)	18.0	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance, 2.5 m/sec airflow per JEDEC JESD51-6 (moving air)	16.0	°C/W
θ_{JB}	Junction-to-board thermal resistance, 0.0 m/sec airflow per JEDEC JESD51-8 (still air)	10.7	°C/W
θ_{JC}	Junction-to-case thermal resistance (die-to-heat sink) per MIL-Standard 883, Method 1012.1	1.1	°C/W
Ψ_{JT}	Junction-to-top-of-package characterization parameter, 0 m/sec airflow per JEDEC JESD51-2 (still air)	0.1	°C/W
Ψ_{JT}	Junction-to-top-of-package characterization parameter, 1.0 m/sec airflow per JEDEC JESD51-6 (moving air)	0.1	°C/W
Ψ_{JT}	Junction-to-top-of-package characterization parameter, 2.5 m/sec airflow per JEDEC JESD51-6 (moving air)	0.2	°C/W

[1] The exposed pad on the bottom of the package must be soldered to analog ground of the PCB to achieve the specified thermal performance.

[2] Results are from simulations. The PCB is a JEDEC multilayer type. Thermal performance for actual applications requires careful inspection of the conditions in the application to determine if they are similar to those assumed in these calculations.

The AD9554 is specified for a case temperature (T_{CASE}). To ensure that T_{CASE} is not exceeded, an airflow source can be used. Use the following equation to determine the junction temperature on the application PCB:

$$T_J = T_{CASE} + (\Psi_{JT} \times PD)$$

where:
T_J is the junction temperature (°C).
T_{CASE} is the case temperature (°C) measured by the customer at the top center of the package.
Ψ_{JT} is the value as indicated in Table 31.
PD is the power dissipation (see Table 3).

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the equation

$$T_J = T_A + (\theta_{JA} \times PD)$$

where T_A is the ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations.

POWER SUPPLY PARTITIONS

The AD9554 power supplies are in two groups: VDD and VDD_SP. All power and ground pins must be connected, even if certain blocks of the chip are powered down.

VDD SUPPLIES

All of the VDD supplies can be connected to one common source that is either 1.5 V or 1.8 V.

Place the 0.1 μF bypass capacitors as close as possible to each power supply pin.

In addition to these bypass capacitors, the AD9554 evaluation board uses eight ferrite beads between the 1.8 V (or 1.5 V) source and Pin 2, Pin 17, Pin 20, Pin 35, Pin 38, Pin 53, Pin 56, and Pin 71.

Although these ferrite beads may not be needed for every application, the use of these ferrite beads is strongly recommended. At a minimum, include a place for the ferrite beads (as close to the bypass capacitors as possible) and populate the board with 0402, 0 Ω resistors. By doing so, there is a place for the ferrite beads, if needed.

The ferrite beads are required if the AD9554 is powered directly from a switching power supply.

Ferrite beads with low (<0.7 Ω) dc resistance and approximately 30 Ω impedance at 100 MHz are suitable for this application. For example, the Murata BLM15AX300SN1D is suitable.

VDD_SP SUPPLY

Pin 30 (VDD_SP) is the serial port power supply pin and can be connected to a 2.5 V, 1.8 V, or 1.5 V power supply.

If the user needs to operate the serial port at the same voltage as the device itself, VDD_SP can be joined to VDD.

REGISTER MAP

Register addresses that are not listed in Table 32 are not used, and writing to those registers has no effect. Write the default value to sections of registers marked reserved. In the option column, R = read only; A = autoclear; E = excluded from EEPROM loading; W1, W2, W3, W5, W6, W7, and W8 = write detection (see Table 30 for more information); and L = live (IO_UPDATE not required for register to take effect or for a read only register to be updated). N/A = not applicable.

Table 32.

Reg Addr (Hex)	Option	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
Serial Control Port and Part Identification											
0x0000	L, E	SPI Config A	Soft reset	LSB first (SPI only)	Address ascension (SPI only)	SDO active (SPI only)	SDO active (SPI only)	Address ascension (SPI only)	LSB first (SPI only)	Soft reset	0x00
0x0001	L, E	SPI Config B	Reserved		Read buffer register	Reserved		Reset sans-regmap	Reserved		0x00
0x0002	E	Reserved	Reserved								0x00
0x0003	R	Chip type	Reserved				Chip type, Bits[3:0]				0x05
0x0004	R	Product ID	Clock part serial ID, Bits[3:0]				Reserved				0x9F
0x0005	R		Clock part serial ID, Bits[11:4]								0x00
0x0006	R	Revision	Part version, Bits[7:0]								0x05
0x0007		Reserved	Reserved								0x00
0x0008		Reserved	Reserved								0x00
0x0009		Reserved	Reserved								0x00
0x000A		Reserved	Reserved								0x00
0x000B	R	SPI version	SPI version, Bits[7:0]								0x00
0x000C	R	Vendor ID	Vendor ID, Bits[7:0]								0x56
0x000D	R		Vendor ID, Bits[15:8]								0x04
0x000E		Reserved	Reserved								0x00
0x000F	L, A, E	IO_UPDATE	Reserved							IO_UPDATE	0x00
User Scratchpad											
0x00FE	L	User scratchpad	User scratchpad[7:0]								0x00
0x00FF	L		User scratchpad[15:8]								0x00
General Configuration											
0x0100		Mx pin drivers	M3 driver mode, Bits[1:0]		M2 driver mode, Bits[1:0]		M1 driver mode, Bits[1:0]		M0 driver mode, Bits[1:0]		0x00
0x0101			M7 driver mode, Bits[1:0]		M6 driver mode, Bits[1:0]		M5 driver mode, Bits[1:0]		M4 driver mode, Bits[1:0]		0x00
0x0102			Reserved				M9 driver mode, Bits[1:0]		M8 driver mode, Bits[1:0]		0x00
0x0103	W7	M0FUNC	M0 output/$\overline{\text{input}}$	M0 function, Bits[6:0]							0x00
0x0104	W7	M1FUNC	M1 output/$\overline{\text{input}}$	M1 function, Bits[6:0]							0x00
0x0105	W7	M2FUNC	M2 output/$\overline{\text{input}}$	M2 function, Bits[6:0]							0x00
0x0106	W7	M3FUNC	M3 output/$\overline{\text{input}}$	M3 function, Bits[6:0]							0x00
0x0107	W7	M4FUNC	M4 output/$\overline{\text{input}}$	M4 function, Bits[6:0]							0x00
0x0108	W7	M5FUNC	M5 output/$\overline{\text{input}}$	M5 function, Bits[6:0]							0x00
0x0109	W7	M6FUNC	M6 output/$\overline{\text{input}}$	M6 function, Bits[6:0]							0x00
0x010A	W7	M7FUNC	M7 output/$\overline{\text{input}}$	M7 function, Bits[6:0]							0x00

Reg Addr (Hex)	Option	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
0x010B	W7	M8FUNC	M8 output/ input	M8 function, Bits[6:0]							0x00
0x010C	W7	M9FUNC	M9 output/ input	M9 function, Bits[6:0]							0x00
0x010D	W5	Watchdog timer	Watchdog timer (ms), Bits[7:0]								0x00
0x010E	W5		Watchdog timer (ms), Bits[15:8]								0x00
0x010F		IRQ mask common	SYSCLK unlocked	SYSCLK stable	SYSCLK locked	SYSCLK calibration ended	SYSCLK calibration started	Watchdog timer	EEPROM fault	EEPROM complete	0x00
0x0110			Reserved	REFB validated	REFB fault cleared	REFB fault	Reserved	REFA validated	REFA fault cleared	REFA fault	0x00
0x0111			Reserved	REFD validated	REFD fault cleared	REFD fault	Reserved	REFC validated	REFC fault cleared	REFC fault	0x00
0x0112		IRQ mask DPLL_0	Frequency unclamped	Frequency clamped	Phase slew unlimited	Phase slew limited	Frequency unlocked	Frequency locked	Phase unlocked	Phase locked	0x00
0x0113			Switching	Free run	Holdover	History updated	REFD activated	REFC activated	REFB activated	REFA activated	0x00
0x0114			Phase step detected	Demap controller unclamped	Demap controller clamped	Sync clock distribution	APLL_0 unlocked	APLL_0 locked	APLL_0 cal complete	APLL_0 cal started	0x00
0x0115		IRQ mask DPLL_1	Frequency unclamped	Frequency clamped	Phase slew unlimited	Phase slew limited	Frequency unlocked	Frequency locked	Phase unlocked	Phase locked	0x00
0x0116			Switching	Free run	Holdover	History updated	REFD activated	REFC activated	REFB activated	REFA activated	0x00
0x0117			Phase step detected	Demap controller unclamped	Demap controller clamped	Sync clock distribution	APLL_1 unlocked	APLL_1 locked	APLL_1 cal complete	APLL_1 cal started	0x00
0x0118		IRQ mask DPLL_2	Frequency unclamped	Frequency clamped	Phase slew unlimited	Phase slew limited	Frequency unlocked	Frequency locked	Phase unlocked	Phase locked	0x00
0x0119			Switching	Free run	Holdover	History updated	REFD activated	REFC activated	REFB activated	REFA activated	0x00
0x011A			Phase step detected	Demap controller unclamped	Demap controller clamped	Sync clock distribution	APLL_2 unlocked	APLL_2 locked	APLL_2 cal complete	APLL_2 cal started	0x00
0x011B		IRQ mask DPLL_3	Frequency unclamped	Frequency clamped	Phase slew unlimited	Phase slew limited	Frequency unlocked	Frequency locked	Phase unlocked	Phase locked	0x00
0x011C			Switching	Free run	Holdover	History updated	REFD activated	REFC activated	REFB activated	REFA activated	0x00
0x011D			Phase step detected	Demap controller unclamped	Demap controller clamped	Sync clock distribution	APLL_3 unlocked	APLL_3 locked	APLL_3 cal complete	APLL_3 cal started	0x00
0x011E	L	Pad control	M7 config	M6 config	M5 config	M4 config	M3 config	M2 config	M1 config	M0 config	0x00
0x011F	L		Reserved					SPI config	M9 config	M8 config	0x00
System Clock											
0x0200		SYSCLK PLL feedback divider and configuration	System clock K divider, Bits[7:0]								0x00
0x0201			Reserved				SYSCLK XTAL enable	SYSCLK J1 divider, Bits[1:0]		SYSCLK doubler enable (J0 divider)	0x08
0x0202	W6	SYSCLK reference frequency	System clock reference frequency (Hz), Bits[7:0]								0x00
0x0203	W6		System clock reference frequency (Hz), Bits[15:8]								0x00
0x0204	W6		System clock reference frequency (Hz), Bits[23:16]								0x00
0x0205	W6		Reserved					System clock reference frequency (Hz), Bits[27:24]			0x00
0x0206	W6	SYSCLK stability	System clock stability period (ms), Bits[7:0]								0x32
0x0207	W6		System clock stability period (ms), Bits[15:8]								0x00
0x0208	W6		Reserved				System clock stability period (ms), Bits[19:16]				0x00
Reference Input A											
0x0300	W1, L	REFA logic type	Reserved						REFA logic type, Bits[1:0]		0x00

Reg Addr (Hex)	Option	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
0x0301	W1, L	REFA R divider (20 bits)	R divider, Bits[7:0]								0x00
0x0302	W1, L		R divider, Bits[15:8]								0x00
0x0303	W1, L		Reserved				R divider, Bits[19:16]				0x00
0x0304	W2, L	REFA period	Nominal reference period (fs), Bits[7:0]								0x00
0x0305	W2, L		Nominal reference period (fs), Bits[15:8]								0x00
0x0306	W2, L		Nominal reference period (fs), Bits[23:16]								0x00
0x0307	W2, L		Nominal reference period (fs), Bits[31:24]								0x00
0x0308	W2, L		Nominal reference period (fs), Bits[39:32]								0x00
0x0309	W2, L	REFA frequency tolerance	Inner tolerance (1/(ppm error)), Bits[7:0] (for invalid to valid condition; maximum: 6.55%, minimum: 2 ppm) (default: 5%)								0x14
0x030A	W2, L		Inner tolerance (1/(ppm error)), Bits[15:8] (for invalid to valid condition; maximum: 6.55%, minimum: 2 ppm)								0x00
0x030B	W2, L		Reserved				Inner tolerance (1/(ppm error)), Bits[19:16]				0x00
0x030C	W2, L		Outer tolerance (1/(ppm error)), Bits[7:0] (for valid to invalid; maximum: 6.55%, minimum: 2 ppm) (default: 10%)								0x0A
0x030D	W2, L		Outer tolerance (1/(ppm error)), Bits[15:8] (for valid to invalid; max: 6.55%, min: 2 ppm)								0x00
0x030E	W2, L		Reserved				Outer tolerance (1/(ppm error)), Bits[19:16]				0x00
0x030F	W2, L	REFA validation timer	Validation timer (ms), Bits[7:0] (up to 65.5 sec)								0x0A
0x0310	W2, L		Validation timer (ms), Bits[15:8] (up to 65.5 sec)								0x00
0x0311	W3, L	REFA phase lock detector	Phase lock threshold (ps), Bits[7:0]								0xBC
0x0312	W3, L		Phase lock threshold (ps), Bits[15:8]								0x02
0x0313	W3, L		Phase lock threshold (ps), Bits[23:16]								0x00
0x0314	W3, L		Phase lock fill rate, Bits[7:0]								0x0A
0x0315	W3, L		Phase lock drain rate, Bits[7:0]								0x0A
0x0316	W3, L	REFA frequency lock detector	Frequency lock threshold (ps), Bits[7:0]								0xBC
0x0317	W3, L		Frequency lock threshold (ps), Bits[15:8]								0x02
0x0318	W3, L		Frequency lock threshold (ps), Bits[23:16]								0x00
0x0319	W3, L		Frequency lock fill rate, Bits[7:0]								0x0A
0x031A	W3, L		Frequency lock drain rate, Bits[7:0]								0x0A
0x031B	W3, L	REFA phase step threshold	Phase step threshold (ps), Bits[7:0]								0x00
0x031C	W3, L		Phase step threshold (ps), Bits[15:8]								0x00
0x031D	W3, L		Phase step threshold (ps), Bits[23:16]								0x00
0x031E	W3, L		Reserved				Phase step threshold (ps), Bits[27:24]				0x00
Reference Input B											
0x0320 to 0x033E			These registers mimic the Reference Input A registers (0x0300 through 0x031E) but the register addresses are offset by 0x0020. All default values are identical.								
Reference Input C											
0x0340 to 0x035E			These registers mimic the Reference Input A registers (0x0300 through 0x031E) but register addresses are offset by 0x0040. All default values are identical.								
Reference Input D											
0x0360 to 0x037E			These registers mimic the Reference Input A registers (0x0300 through 0x031E) but the register addresses are offset by 0x0060. All default values are identical.								
DPLL_0 General Settings											
0x0400		DPLL_0 free run frequency TW	30-bit free running frequency tuning word, Bits[7:0]								0x00
0x0401			30-bit free running frequency tuning word, Bits[15:8]								0x00
0x0402			30-bit free running frequency tuning word, Bits[23:16]								0x00
0x0403			Reserved		30-bit free running frequency tuning word, Bits[29:24]						0x00
0x0404		DPLL_0 DCO integer	Reserved				DCO integer, Bits[3:0]				0x17
0x0405		DPLL_0 frequency clamp	Lower limit of pull-in range, Bits[7:0]								0xCC
0x0406			Lower limit of pull-in range, Bits[15:8]								0xCC
0x0407			Reserved				Lower limit of pull-in range, Bits[19:16]				0x00
0x0408			Upper limit of pull-in range, Bits[7:0]								0x33
0x0409			Upper limit of pull-in range, Bits[15:8]								0x33
0x040A			Reserved				Upper limit of pull-in range, Bits[19:16]				0x0F
0x040B		DPLL_0 holdover history	History accumulation timer (ms), Bits[7:0] (up to 65 sec)								0x0A
0x040C			History accumulation timer (ms), Bits[15:8] (up to 65 sec)								0x00

Reg Addr (Hex)	Option	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
0x040D		DPLL_0 history mode	Reserved			Single sample fallback	Persistent history	Incremental average, Bits[2:0]			0x00
0x040E		DPLL_0 closed loop phase offset (±0.5 ms)	Fixed phase offset (signed; ps), Bits[7:0]								0x00
0x040F			Fixed phase offset (signed; ps), Bits[15:8]								0x00
0x0410			Fixed phase offset (signed; ps), Bits[23:16]								0x00
0x0411			Reserved		Fixed phase offset (signed; ps), Bits[29:24]						0x00
0x0412			Incremental phase offset step size (ps/step), Bits[7:0] (up to 65.5 ns/step)								0x00
0x0413			Incremental phase offset step size (ps/step), Bits[15:8] (up to 65.5 ns/step)								0x00
0x0414		DPLL_0 phase slew limit	Phase slew rate limit (μs/sec), Bits[7:0] (315 μs/sec up to 65.536 ms/sec)								0x00
0x0415			Phase slew rate limit (μs/sec), Bits[15:8] (315 μs/sec up to 65.536 ms/sec)								0x00
0x0416		Demap enable	Reserved							Enable demap controller	0x00
0x0417		Demap sampled address	Sampled address, Bits[7:0]								0x00
0x0418			Sampled address, Bits[15:8]								0x00
0x0419		Demap set point address	Set point address, Bits[7:0]								0x00
0x041A			Set point address, Bits[15:8]								0x00
0x041B		Demap gain control	Gain, Bits[7:0]								0x00
0x041C			Gain, Bits[15:8]								0x00
0x041D			Gain, Bits[23:16]								0x00
0x041E		Demap clamp control	Clamp value, Bits[7:0]								0x00
Output PLL_0 (APLL_0) and Channel 0 Output Drivers											
0x0430		APLL_0 charge pump	Reserved	Output PLL0 (APLL_0) charge pump current, Bits[6:0]							0x2E
0x0431		APLL_0 M0 divider	Output PLL0 (APLL_0) feedback (M0) divider, Bits[7:0]								0x00
0x0432		APLL_0 loop filter control	APLL_0 loop filter control, Bits[7:0]								0x7F
0x0433			Reserved						P0 divider reset	APLL_0 loop filter control, Bit 8	0x00
0x0434		P0 divider	Reserved				P0 divider divide ratio, Bits[3:0]				0x00
0x0435		OUT0 sync	Reserved					Sync source selection	Auto sync mode, Bits[1:0]		0x00
0x0436			Reserved					APLL_0 mask sync	Mask OUT0B sync	Mask OUT0A sync	0x00
0x0437		OUT0A	Reserved					OUT0A mode		Invert polarity	0x00
0x0438		Q0_A divider	Q0_A divider, Bits[7:0]								0x00
0x0439			Reserved						Q0_A divider, Bits[9:8]		0x00
0x043A			Reserved		Q0_A divider phase, Bits[5:0]						0x00
0x043B		OUT0B	Reserved					OUT0B mode		Invert polarity	0x08
0x043C		Q0_B divider	Q0_B divider, Bits[7:0]								0x00
0x043D			Reserved						Q0_B divider, Bits[9:8]		0x00
0x043E			Reserved		Q0_B divider phase, Bits[5:0]						0x00
DPLL_0 Settings for Reference Input A											
0x0440		Reference priority	Reserved					REFA priority		Enable REFA	0x00
0x0441	W2, L	DPLL_0 loop BW (17 bits)	Digital PLL_0 loop bandwidth scaling factor, Bits[7:0] (in units of 0.1 Hz)								0x00
0x0442	W2, L		Digital PLL_0 loop bandwidth scaling factor, Bits[15:8] (in units of 0.1 Hz)								0x00
0x0443	W2, L		Reserved						Base loop filter selection	Digital PLL_0 loop BW scaling factor, Bit 16	0x00

Reg Addr (Hex)	Option	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
0x0444	W2	DPLL_0 N0 divider (18 bits)	Digital PLL_0 feedback divider—Integer Part N0, Bits[7:0]								0x00
0x0445	W2		Digital PLL_0 feedback divider—Integer Part N0, Bits[15:8]								0x00
0x0446	W2		Reserved						Digital PLL_0 feedback divider, Integer Part N0, Bits[17:16]		0x00
0x0447	W8	DPLL_0 fractional feedback divider (24 bits)	Digital PLL_0 fractional feedback divider—FRAC0, Bits[7:0]								0x00
0x0448	W8		Digital PLL_0 fractional feedback divider—FRAC0, Bits[15:8]								0x00
0x0449	W8		Digital PLL_0 fractional feedback divider—FRAC0, Bits[23:16]								0x00
0x044A	W2	DPLL_0 fractional feedback divider modulus (24 bits)	Digital PLL_0 feedback divider modulus—MOD0, Bits[7:0]								0x00
0x044B	W2		Digital PLL_0 feedback divider modulus—MOD0, Bits[15:8]								0x00
0x044C	W2		Digital PLL_0 feedback divider modulus—MOD0, Bits[23:16]								0x00
DPLL_0 Settings for Reference Input B											
0x044D		Reference priority	Reserved					REFB priority		Enable REFB	0x00
0x044E	W2, L	DPLL_0 loop BW (17 bits)	Digital PLL_0 loop bandwidth scaling factor, Bits[7:0] (unit: 0.1 Hz)								0x00
0x044F	W2, L		Digital PLL_0 loop bandwidth scaling factor, Bits[15:8] (unit: 0.1 Hz)								0x00
0x0450	W2, L		Reserved						Base loop filter selection	Digital PLL_0 loop BW scaling factor, Bit 16	0x00
0x0451	W2	DPLL_0 N0 divider (18 bits)	Digital PLL_0 feedback divider—Integer Part N0, Bits[7:0]								0x00
0x0452	W2		Digital PLL_0 feedback divider—Integer Part N0, Bits[15:8]								0x00
0x0453	W2		Reserved						Digital PLL_0 feedback divider—Integer Part N0, Bits[17:16]		0x00
0x0454	W8	DPLL_0 fractional feedback divider (24 bits)	Digital PLL_0 fractional feedback divider—FRAC0, Bits[7:0]								0x00
0x0455	W8		Digital PLL_0 fractional feedback divider—FRAC0, Bits[15:8]								0x00
0x0456	W8		Digital PLL_0 fractional feedback divider—FRAC0, Bits[23:16]								0x00
0x0457	W2	DPLL_0 fractional feedback divider modulus (24 bits)	Digital PLL_0 feedback divider modulus—MOD0, Bits[7:0]								0x00
0x0458	W2		Digital PLL_0 feedback divider modulus—MOD0, Bits[15:8]								0x00
0x0459	W2		Digital PLL_0 feedback divider modulus—MOD0, Bits[23:16]								0x00
DPLL_0 Settings for Reference Input C											
0x045A		Reference priority	Reserved					REFC priority		Enable REFC	0x00
0x045B	W2, L	DPLL_0 loop BW (17 bits)	Digital PLL_0 loop bandwidth scaling factor, Bits[7:0] (unit: 0.1 Hz)								0x00
0x045C	W2, L		Digital PLL_0 loop bandwidth scaling factor, Bits[15:8] (unit: 0.1 Hz)								0x00
0x045D	W2, L		Reserved						Base loop filter selection	Digital PLL_0 loop BW scaling factor, Bit 16	0x00
0x045E	W2	DPLL_0 N0 divider (18 bits)	Digital PLL_0 feedback divider—Integer Part N0, Bits[7:0]								0x00
0x045F	W2		Digital PLL_0 feedback divider—Integer Part N0, Bits[15:8]								0x00
0x0460	W2		Reserved						Digital PLL_0 feedback divider—Integer Part N0, Bits[17:16]		0x00
0x0461	W8	DPLL_0 fractional feedback divider (24 bits)	Digital PLL_0 fractional feedback divider—FRAC0, Bits[7:0]								0x00
0x0462	W8		Digital PLL_0 fractional feedback divider—FRAC0, Bits[15:8]								0x00
0x0463	W8		Digital PLL_0 fractional feedback divider—FRAC0, Bits[23:16]								0x00
0x0464	W2	DPLL_0 fractional feedback divider modulus (24 bits)	Digital PLL_0 feedback divider modulus—MOD0, Bits[7:0]								0x00
0x0465	W2		Digital PLL_0 feedback divider modulus—MOD0, Bits[15:8]								0x00
0x0466	W2		Digital PLL_0 feedback divider modulus—MOD0, Bits[23:16]								0x00

Reg Addr (Hex)	Option	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
DPLL_0 Settings for Reference Input D											
0x0467		Reference priority	Reserved					REFD priority		Enable REFD	0x00
0x0468	W2, L	DPLL_0 loop BW (17 bits)	Digital PLL_0 loop bandwidth scaling factor, Bits[7:0] (unit: 0.1 Hz)								0x00
0x0469	W2, L		Digital PLL_0 loop bandwidth scaling factor, Bits[15:8] (unit: 0.1 Hz)								0x00
0x046A	W2, L		Reserved						Base loop filter selection	Digital PLL_0 loop BW scaling factor, Bit 16	0x00
0x046B	W2	DPLL_0 N0 divider (18 bits)	Digital PLL_0 feedback divider—Integer Part N0, Bits[7:0]								0x00
0x046C	W2		Digital PLL_0 feedback divider—Integer Part N0, Bits[15:8]								0x00
0x046D	W2		Reserved						Digital PLL_0 feedback divider—Integer Part N0, Bits[17:16]		0x00
0x046E	W8	DPLL_0 fractional feedback divider (24 bits)	Digital PLL_0 fractional feedback divider—FRAC0, Bits[7:0]								0x00
0x046F	W8		Digital PLL_0 fractional feedback divider—FRAC0, Bits[15:8]								0x00
0x0470	W8		Digital PLL_0 fractional feedback divider—FRAC0, Bits[23:16]								0x00
0x0471	W2	DPLL_0 fractional feedback divider modulus (24 bits)	Digital PLL_0 feedback divider modulus—MOD0, Bits[7:0]								0x00
0x0472	W2		Digital PLL_0 feedback divider modulus—MOD0, Bits[15:8]								0x00
0x0473	W2		Digital PLL_0 feedback divider modulus—MOD0, Bits[23:16]								0x00
DPLL_1 General Settings											
0x0500 to 0x051E			These registers mimic the DPLL_0 general settings registers (0x0400 through 0x041E) but the register addresses are offset by 0x0100. All default values are identical.								
Output PLL_1 (APLL_1) and Channel 1 Output Drivers											
0x0530 to 0x053E			These registers mimic the output PLL_0 (APLL_0) general settings registers (0x0430 through 0x043E) but the register addresses are offset by 0x0100. All default values are identical.								
DPLL_1 Settings for Reference Input A											
0x0540 to 0x054C			These registers mimic the DPLL_0 settings for Reference Input A registers (0x0440 through 0x044C) but the register addresses are offset by 0x0100. All default values are identical.								
DPLL_1 Settings for Reference Input B											
0x054D to 0x0559			These registers mimic the DPLL_0 settings for Reference Input B registers (0x044D through 0x0459) but the register addresses are offset by 0x0100. All default values are identical.								
DPLL_1 Settings for Reference Input C											
0x055A to 0x0566			These registers mimic the DPLL_0 settings for Reference Input C registers (0x045A through 0x0466) but the register addresses are offset by 0x0100. All default values are identical.								
DPLL_1 Settings for Reference Input D											
0x0567 to 0x0573			These registers mimic the DPLL_0 settings for Reference Input D registers (0x0467 through 0x0473) but the register addresses are offset by 0x0100. All default values are identical.								
DPLL_2 General Settings											
0x0600 to 0x061E			These registers mimic the DPLL_0 general settings registers (0x0400 through 0x041E) but the register addresses are offset by 0x0200. All default values are identical.								
Output PLL_2 (APLL_2) and Channel 2 Output Drivers											
0x0630 to 0x063E			These registers mimic the output PLL_0 (APLL_0) general settings registers (0x0430 through 0x043E) but the register addresses are offset by 0x0200. All default values are identical.								
DPLL_2 Settings for Reference Input A											
0x0640 to 0x064C			These registers mimic the DPLL_0 settings for Reference Input A registers (0x0440 through 0x044C) but the register addresses are offset by 0x0200. All default values are identical.								

Reg Addr (Hex)	Option	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
DPLL_2 Settings for Reference Input B											
0x064D to 0x0659			These registers mimic the DPLL_0 settings for Reference Input B registers (0x044D through 0x0459) but the register addresses are offset by 0x0200. All default values are identical.								
DPLL_2 Settings for Reference Input C											
0x065A to 0x0666			These registers mimic the DPLL_0 settings for Reference Input C registers (0x045A through 0x0466) but the register addresses are offset by 0x0200. All default values are identical.								
DPLL_2 Settings for Reference Input D											
0x0667 to 0x0673			These registers mimic the DPLL_0 settings for Reference Input D registers (0x0467 through 0x0473) but the register addresses are offset by 0x0200. All default values are identical.								
DPLL_3 General Settings											
0x0700 to 0x071E			These registers mimic the DPLL_0 general settings registers (0x0400 through 0x041E) but the register addresses are offset by 0x0300. All default values are identical.								
Output PLL_3 (APLL_3) and Channel 3 Output Drivers											
0x0730 to 0x073E			These registers mimic the output PLL_0 (APLL_0) general settings registers (0x0430 through 0x043E) but the register addresses are offset by 0x0300. All default values are identical.								
DPLL_3 Settings for Reference Input A											
0x0740 to 0x074C			These registers mimic the DPLL_0 settings for Reference Input A registers (0x0440 through 0x044C) but the register addresses are offset by 0x0300. All default values are identical.								
DPLL_3 Settings for Reference Input B											
0x074D to 0x0759			These registers mimic the DPLL_0 settings for Reference Input B registers (0x044D through 0x0459) but the register addresses are offset by 0x0300. All default values are identical.								
DPLL_3 Settings for Reference Input C											
0x075A to 0x0766			These registers mimic the DPLL_0 Settings for Reference Input C registers (0x045A through 0x0466) but the register addresses are offset by 0x0300. All default values are identical.								
DPLL_3 Settings for Reference Input D											
0x0767 to 0x0773			These registers mimic the DPLL_0 Settings for Reference Input D registers (0x0467 through 0x0473) but the register addresses are offset by 0x0300. All default values are identical.								
Digital Loop Filter Coefficients											
0x0800	L	Base loop filter coefficient set (normal phase margin of 70°)	NPM Alpha-0 linear, Bits[7:0]								0x24
0x0801	L		NPM Alpha-0 linear, Bits[15:8]								0x8C
0x0802	L		Reserved	NPM Alpha-1 exponent, Bits[6:0]							0x49
0x0803	L		NPM Beta-0 linear, Bits[7:0]								0x55
0x0804	L		NPM Beta-0 linear, Bits[15:8]								0xC9
0x0805	L		Reserved	NPM Beta-1 exponent, Bits[6:0]							0x7B
0x0806	L		NPM Gamma-0 linear, Bits[7:0]								0x9C
0x0807	L		NPM Gamma-0 linear, Bits[15:8]								0xFA
0x0808	L		Reserved	NPM Gamma-1 exponent, Bits[6:0]							0x55
0x0809	L		NPM Delta-0 linear, Bits[7:0]								0xEA
0x080A	L		NPM Delta-0 linear, Bits[15:8]								0xE2
0x080B	L		Reserved	NPM Delta-1 exponent, Bits[6:0]							0x57
0x080C	L	Base loop filter coefficient set (high phase margin)	HPM Alpha-0 linear, Bits[7:0]								0x8C
0x080D	L		HPM Alpha-0 linear, Bits[15:8]								0xAD
0x080E	L		Reserved	HPM Alpha-1 exponent, Bits[6:0]							0x4C
0x080F	L		HPM Beta-0 linear, Bits[7:0]								0xF5
0x0810	L		HPM Beta-0 linear, Bits[15:8]								0xCB
0x0811	L		Reserved	HPM Beta-1 exponent, Bits[6:0]							0x73
0x0812	L		HPM Gamma-0 linear, Bits[7:0]								0x24
0x0813	L		HPM Gamma-0 linear, Bits[15:8]								0xD8
0x0814	L		Reserved	HPM Gamma-1 exponent, Bits[6:0]							0x59
0x0815	L		HPM Delta-0 linear, Bits[7:0]								0xD2
0x0816	L		HPM Delta-0 linear, Bits[15:8]								0x8D
0x0817	L		Reserved	HPM Delta-1 exponent, Bits[6:0]							0x5A

Reg Addr (Hex)	Option	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
Global Demapping Control											
0x0900	L	Demap control IO_UPDATE	Reserved							Demap control IO_ UPDATE	0x00
0x0901		DPLL_0	DPLL_0 sampled address, Bits[7:0]								0x00
0x0902			DPLL_0 sampled address, Bits[15:8]								0x00
0x0903		DPLL_1	DPLL_1 sampled address, Bits[7:0]								0x00
0x0904			DPLL_1 sampled address, Bits[15:8]								0x00
0x0905		DPLL_2	DPLL_2 sampled address, Bits[7:0]								0x00
0x0906			DPLL_2 sampled address, Bits[15:8]								0x00
0x0907		DPLL_3	DPLL_3 sampled address, Bits[7:0]								0x00
0x0908			DPLL_3 sampled address, Bits[15:8]								0x00
0x0909		Demap control IO_UPDATE	Reserved							Demap control IO_ UPDATE	0x00
Common Operational Controls											
0x0A00		Global	Reserved				Soft sync all	Calibrate SYSCLK	Calibrate all	Power-down all	0x00
0x0A01		Reference inputs	Reserved				REFD power-down	REFC power-down	REFB power-down	REFA power-down	0x00
0x0A02	A		Reserved				REFD timeout	REFC timeout	REFB timeout	REFA timeout	0x00
0x0A03			Reserved				REFD fault	REFC fault	REFB fault	REFA fault	0x00
0x0A04			Reserved				REFD monitor bypass	REFC monitor bypass	REFB monitor bypass	REFA monitor bypass	0x00
0x0A05	A	Clear IRQ groups	Clear watchdog timer	Reserved	Clear DPLL_3 IRQs	Clear DPLL_2 IRQs	Clear DPLL_1 IRQs	Clear DPLL_0 IRQs	Clear common IRQs	Clear all IRQs	0x00
0x0A06	A	Clear common IRQ	SYSCLK unlocked	SYSCLK stable	SYSCLK locked	SYSCLK cal ended	SYSCLK cal started	Watchdog timer	EEPROM fault	EEPROM complete	0x00
0x0A07	A		Reserved	REFB validated	REFB fault cleared	REFB fault	Reserved	REFA validated	REFA fault cleared	REFA fault	0x00
0x0A08	A		Reserved	REFD validated	REFD fault cleared	REFD fault	Reserved	REFC validated	REFC fault cleared	REFC fault	0x00
0x0A09	A	Clear DPLL_0 IRQ	Frequency unclamped	Frequency clamped	Phase slew unlimited	Phase slew limited	Frequency unlocked	Frequency locked	Phase unlocked	Phase locked	0x00
0x0A0A	A		DPLL_0 switching	DPLL_0 free run	DPLL_0 holdover	History updated	REFD activated	REFC activated	REFB activated	REFA activated	0x00
0x0A0B	A		Phase step detected	Demap control unclamped	Demap control clamped	Clock dist sync'd	APLL_0 unlocked	APLL_0 locked	APLL_0 cal ended	APLL_0 cal started	0x00
0x0A0C	A	Clear DPLL_1 IRQ	Frequency unclamped	Frequency clamped	Phase slew unlimited	Phase slew limited	Frequency unlocked	Frequency locked	Phase unlocked	Phase locked	0x00
0x0A0D	A		DPLL_1 switching	DPLL_1 free run	DPLL_1 holdover	History updated	REFD activated	REFC activated	REFB activated	REFA activated	0x00
0x0A0E	A		Phase step detected	Demap control unclamped	Demap control clamped	Clock dist sync'd	APLL_1 unlocked	APLL_1 locked	APLL_1 cal ended	APLL_1 cal started	0x00
0x0A0F	A	Clear DPLL_2 IRQ	Frequency unclamped	Frequency clamped	Phase slew unlimited	Phase slew limited	Frequency unlocked	Frequency locked	Phase unlocked	Phase locked	0x00
0x0A10	A		DPLL_2 switching	DPLL_2 free run	DPLL_2 holdover	History updated	REFD activated	REFC activated	REFB activated	REFA activated	0x00
0x0A11	A		Phase step detected	Demap control unclamped	Demap control clamped	Clock dist sync'd	APLL_2 unlocked	APLL_2 locked	APLL_2 cal ended	APLL_2 cal started	0x00
0x0A12	A	Clear DPLL_3 IRQ	Frequency unclamped	Frequency clamped	Phase slew unlimited	Phase slew limited	Frequency unlocked	Frequency locked	Phase unlocked	Phase locked	0x00
0x0A13	A		DPLL_3 switching	DPLL_3 free run	DPLL_3 holdover	History updated	REFD activated	REFC activated	REFB activated	REFA activated	0x00
0x0A14	A		Phase step detected	Demap control unclamped	Demap control clamped	Clock dist sync'd	APLL_3 unlocked	APLL_3 locked	APLL_3 cal ended	APLL_3 cal started	0x00

Reg Addr (Hex)	Option	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
PLL_0 Operational Controls											
0x0A20		PLL_0 sync cal	Reserved					APLL_0 soft sync	APLL_0 calibrate (not self-clearing)	PLL_0 power-down	0x00
0x0A21		PLL_0 output	Reserved				OUT0B disable	OUT0A disable	OUT0B power-down	OUT0A power-down	0x00
0x0A22		PLL_0 user mode	Reserved	DPLL_0 manual reference		DPLL_0 switching mode			DPLL_0 user holdover	DPLL_0 user free run	0x00
0x0A23	A	PLL_0 reset	Reserved					Reset DPLL_0 loop filter	Reset DPLL_0 TW history	Reset DPLL_0 autosync	0x00
0x0A24	A	PLL_0 phase	Reserved					DPLL_0 reset phase offset	DPLL_0 decrement phase offset	DPLL_0 increment phase offset	0x00
PLL_1 Operational Controls											
0x0A40 to 0x0A44			These registers mimic the PLL_0 operational controls registers (0x0A20 through 0x0A24) but the register addresses are offset by 0x0020. All default values are identical.								
PLL_2 Operational Controls											
0x0A60 to 0x0A64			These registers mimic the PLL_0 operational controls registers (0x0A20 through 0x0A24) but the register addresses are offset by 0x0040. All default values are identical.								
PLL_3 Operational Controls											
0x0A80 to 0x0A84			These registers mimic the PLL_0 operational controls registers (0x0A20 through 0x0A24) but the register addresses are offset by 0x0060. All default values are identical.								
Voltage Regulator											
0x0B00	L	Voltage regulator	VREG, Bits[7:0]								0x00
0x0B01	L		Reserved						VREG, Bits[9:8]		0x00
Read Only Status Common Blocks (These registers are accessible during EEPROM transactions. To show the latest status, Register 0x0D02 to Register 0x0D05 require an IO_UPDATE before being read.)											
0x0D00	R, L	EEPROM	Reserved				EEPROM CRC fault detected	EEPROM fault detected	EEPROM download in progress	EEPROM upload in progress	N/A
0x0D01	R, L	SYSCLK and PLL status	PLL_3 all locked	PLL_2 all locked	PLL_1 all locked	PLL_0 all locked	Reserved	SYSCLK calibration busy	SYSCLK stable	SYSCLK lock detect	N/A
0x0D02	R	Reference status	DPLL_3 REFA active	DPLL_2 REFA active	DPLL_1 REFA active	DPLL_0 REFA active	REFA valid	REFA fault	REFA fast	REFA slow	N/A
0x0D03	R		DPLL_3 REFB active	DPLL_2 REFB active	DPLL_1 REFB active	DPLL_0 REFB active	REFB valid	REFB fault	REFB fast	REFB slow	N/A
0x0D04	R		DPLL_3 REFC active	DPLL_2 REFC active	DPLL_1 REFC active	DPLL_0 REFC active	REFC valid	REFC fault	REFC fast	REFC slow	N/A
0x0D05	R		DPLL_3 REFD active	DPLL_2 REFD active	DPLL_1 REFD active	DPLL_0 REFD active	REFD valid	REFD fault	REFD fast	REFD slow	N/A
0x0D06	R		Reserved								N/A
0x0D07	R		Reserved								N/A
IRQ Monitor											
0x0D08	R, L	IRQ, common	SYSCLK unlocked	SYSCLK stable	SYSCLK locked	SYSCLK cal ended	SYSCLK cal started	Watchdog timer	EEPROM fault	EEPROM complete	N/A
0x0D09	R, L		Reserved	REFB validated	REFB fault cleared	REFB fault	Reserved	REFA validated	REFA fault cleared	REFA fault	N/A
0x0D0A	R, L		Reserved	REFD validated	REFD fault cleared	REFD fault	Reserved	REFC validated	REFC fault cleared	REFC fault	N/A
0x0D0B	R, L	IRQ, DPLL_0	Frequency unclamped	Frequency clamped	Phase slew unlimited	Phase slew limited	Frequency unlocked	Frequency locked	Phase unlocked	Phase locked	N/A
0x0D0C	R, L		DPLL_0 switching	DPLL_0 free run	DPLL_0 holdover	DPLL_0 history updated	REFD activated	REFC activated	REFB activated	REFA activated	N/A
0x0D0D	R, L		Phase step direction	Demap control unclamped	Demap control clamped	Clock dist sync'd	APLL_0 unlocked	APLL_0 locked	APLL_0 cal ended	APLL_0 cal started	N/A

Reg Addr (Hex)	Option	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
0x0D0E	R, L	IRQ, DPLL_1	Frequency unclamped	Frequency clamped	Phase slew unlimited	Phase slew limited	Frequency unlocked	Frequency locked	Phase unlocked	Phase locked	N/A
0x0D0F	R, L		DPLL_1 switching	DPLL_1 free run	DPLL_1 holdover	DPLL_1 history updated	REFD activated	REFC activated	REFB activated	REFA activated	N/A
0x0D10	R, L		Phase step direction	Demap control unclamped	Demap control clamped	Clock dist sync'd	APLL_1 unlocked	APLL_1 locked	APLL_1 cal ended	APLL_1 cal started	N/A
0x0D11	R, L	IRQ, DPLL_2	Frequency unclamped	Frequency clamped	Phase slew unlimited	Phase slew limited	Frequency unlocked	Frequency locked	Phase unlocked	Phase locked	N/A
0x0D12	R, L		DPLL_2 switching	DPLL_2 free run	DPLL_2 holdover	DPLL_2 history updated	REFD activated	REFC activated	REFB activated	REFA activated	N/A
0x0D13	R, L		Phase step direction	Demap control unclamped	Demap control clamped	Clock dist sync'd	APLL_2 unlocked	APLL_2 locked	APLL_2 cal ended	APLL_2 cal started	N/A
0x0D14	R, L	IRQ, DPLL_3	Frequency unclamped	Frequency clamped	Phase slew unlimited	Phase slew limited	Frequency unlocked	Frequency locked	Phase unlocked	Phase locked	N/A
0x0D15	R, L		DPLL_3 switching	DPLL_3 free run	DPLL_3 holdover	DPLL_3 history updated	REFD activated	REFC activated	REFB activated	REFA activated	N/A
0x0D16	R, L		Phase step direction	Demap control unclamped	Demap control clamped	Clock dist sync'd	APLL_3 unlocked	APLL_3 locked	APLL_3 cal ended	APLL_3 cal started	N/A
PLL_0 Read Only Status (To show the latest status, these registers require an IO_UPDATE before being read.)											
0x0D20	R, L	PLL_0 lock status	Reserved			APLL_0 cal in progress	APLL_0 freq lock	DPLL_0 freq lock	DPLL_0 phase lock	PLL_0 all locked	N/A
0x0D21	R	DPLL_0 loop state	Reserved			DPLL_0 active ref		DPLL_0 switching	DPLL_0 holdover	DPLL_0 free run	N/A
0x0D22	R		Reserved				Demap controller clamped	DPLL_0 phase slew limited	DPLL_0 frequency clamped	DPLL_0 history available	N/A
0x0D23	R	DPLL_0 holdover history	DPLL_0 tuning word readback, Bits[7:0]								N/A
0x0D24	R		DPLL_0 tuning word readback, Bits[15:8]								N/A
0x0D25	R		DPLL_0 tuning word readback, Bits[23:16]								N/A
0x0D26	R		Reserved		DPLL_0 tuning word readback, Bits[29:24]						N/A
0x0D27	R	DPLL_0 phase lock detect bucket	DPLL_0 phase lock detect bucket level, Bits[7:0]								N/A
0x0D28	R		Reserved				DPLL_0 phase lock detect bucket level, Bits[11:8]				N/A
0x0D29	R	DPLL_0 frequency lock detect bucket	DPLL_0 frequency lock detect bucket level, Bits[7:0]								N/A
0x0D2A	R		Reserved				DPLL_0 frequency lock detect bucket level, Bits[11:8]				N/A
PLL_1 Read Only Status (To show the latest status, these registers require an IO_UPDATE before being read.)											
0x0D40 to 0x0D4A			These registers mimic the PLL_0 read only status registers (0x0D20 through 0x0D2A) but the register addresses are offset by 0x0020. All default values are identical.								N/A
PLL_2 Read Only Status (To show the latest status, these registers require an IO_UPDATE before being read.)											
0x0D60 to 0x0D6A			These registers mimic the PLL_0 read only status registers (0x0D20 through 0x0D2A) but the register addresses are offset by 0x0040. All default values are identical.								N/A
PLL_3 Read Only Status (To show the latest status, these registers require an IO_UPDATE before being read.)											
0x0D80 to 0x0D8A			These registers mimic the PLL_0 Read Only Status registers (0x0D20 through 0x0D2A) but the register addresses are offset by 0x0060. All default values are identical.								N/A
Nonvolatile Memory (EEPROM) Control											
0x0E00	E	Write protect	Reserved						Enable I^{2}C fast mode	Write enable	0x00
0x0E01	E, L	Condition	Reserved				Conditional value				0x00
0x0E02	L, A, E	Save	Reserved							Save to EEPROM	0x00
0x0E03	L, A, E	Load	Reserved							Load from EEPROM	0x00

Reg Addr (Hex)	Option	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
EEPROM Storage Sequence											
0x0E10	L	User free run	Command: set user free run mode								0x98
0x0E11	L	User scratchpad	Size of transfer: two bytes								0x01
0x0E12	L		Starting Address 0x00FE								0xFE
0x0E13	L										0x00
0x0E14	L	Mx pins and IRQ masks	Size of transfer: 32 bytes								0x1F
0x0E15	L		Starting Address 0x0100								0x00
0x0E16	L										0x01
0x0E17	L	System clock	Size of transfer: nine bytes								0x08
0x0E18	L		Starting Address 0x0200								0x00
0x0E19	L										0x02
0x0E1A	L	IO_UPDATE	Command: IO_UPDATE								0x80
0x0E1B	L	Calibrate SYSCLK	Command: calibrate system clock								0x91
0x0E1C	L	REFA	Size of transfer: 31 bytes								0x1E
0x0E1D	L		Starting Address 0x0300								0x00
0x0E1E	L										0x03
0x0E1F	L	REFB	Size of transfer: 31 bytes								0x1E
0x0E20	L		Starting Address 0x0320								0x20
0x0E21	L										0x03
0x0E22	L	REFC	Size of transfer: 31 bytes								0x1E
0x0E23	L		Starting Address 0x0340								0x40
0x0E24	L										0x03
0x0E25	L	REFD	Size of transfer: 31 bytes								0x1E
0x0E26	L		Starting Address 0x0360								0x60
0x0E27	L										0x03
0x0E28	L	DPLL_0 general settings	Size of transfer: 31 bytes								0x1E
0x0E29	L		Starting Address 0x0400								0x00
0x0E2A	L										0x04
0x0E2B	L	APLL_0 config and output drivers	Size of transfer: 15 bytes								0x0E
0x0E2C	L		Starting Address 0x0430								0x30
0x0E2D	L										0x04
0x0E2E	L	DPLL_0 dividers and BW	Size of transfer: 52 bytes								0x33
0x0E2F	L		Starting Address 0x0440								0x40
0x0E30	L										0x04
0x0E31	L	DPLL_1 general settings	Size of transfer: 31 bytes								0x1E
0x0E32	L		Starting Address 0x0500								0x00
0x0E33	L										0x05
0x0E34	L	APLL_1 config and output drivers	Size of transfer: 15 bytes								0x0E
0x0E35	L		Starting Address 0x0530								0x30
0x0E36	L										0x05
0x0E37	L	DPLL_1 dividers and BW	Size of transfer: 52 bytes								0x33
0x0E38	L		Starting Address 0x0540								0x40
0x0E39	L										0x05
0x0E3A	L	DPLL_2 general settings	Size of transfer: 31 bytes								0x1E
0x0E3B	L		Starting Address 0x0600								0x00
0x0E3C	L										0x06
0x0E3D	L	APLL_2 config and output drivers	Size of transfer: 15 bytes								0x0E
0x0E3E	L		Starting Address 0x0630								0x30
0x0E3F	L										0x06
0x0E40	L	DPLL_2 dividers and BW	Size of transfer: 52 bytes								0x33
0x0E41	L		Starting Address 0x0640								0x40
0x0E42	L										0x06
0x0E43	L	DPLL_3 general settings	Size of transfer: 31 bytes								0x1E
0x0E44	L		Starting Address 0x0700								0x00
0x0E45	L										0x07

Reg Addr (Hex)	Option	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
0x0E46	L	APLL_3 config and output drivers	Size of transfer: 15 bytes								0x0E
0x0E47	L		Starting Address 0x0730								0x30
0x0E48	L										0x07
0x0E49	L	DPLL_3 dividers and BW	Size of transfer: 52 bytes								0x33
0x0E4A	L		Starting Address 0x0740								0x40
0x0E4B	L										0x07
0x0E4C	L	DPLL loop filters	Size of transfer: 24 bytes								0x17
0x0E4D	L		Starting Address 0x0800								0x00
0x0E4E	L										0x08
0x0E4F	L	Operational controls (common)	Size of transfer: 21 bytes								0x14
0x0E50	L		Starting Address 0x0A00								0x00
0x0E51	L										0x0A
0x0E52	L	PLL_0 operational controls	Size of transfer: five bytes								0x04
0x0E53	L		Starting Address 0x0A20								0x20
0x0E54	L										0x0A
0x0E55	L	PLL_1 operational controls	Size of transfer: five bytes								0x04
0x0E56	L		Starting Address 0x0A40								0x40
0x0E57	L										0x0A
0x0E58	L	PLL_2 operational controls	Size of transfer: five bytes								0x04
0x0E59	L		Starting Address 0x0A60								0x60
0x0E5A	L										0x0A
0x0E5B	L	PLL_3 operational controls	Size of transfer: five bytes								0x04
0x0E5C	L		Starting Address 0x0A80								0x80
0x0E5D	L										0x0A
0x0E5E	L	IO_UPDATE	Command: IO_UPDATE								0x80
0x0E5F	L	Calibrate APLLs	Command: calibrate output PLLs								0x92
0x0E60	L	Sync outputs	Command: distribution sync								0xA0
0x0E61	L	End of data	Command: end of data								0xFF
0x0E62 to 0x0E6F	L	Unused	Unused (available for additional data transfers and/or commands)								0x00
V_{CAL} Reference Control											
0x0FFF		V_{CAL} reference access	V_{CAL} reference access								0x00
0x1488		APLL_0 V_{CAL} reference	Reserved					APLL_0 manual cal level, Bits[1:0]		En APLL_0 man cal level	0x00
0x1588		APLL_1 V_{CAL} reference	Reserved					APLL_1 manual cal level, Bits[1:0]		En APLL_1 man cal level	0x00
0x1688		APLL_2 V_{CAL} reference	Reserved					APLL_2 manual cal level, Bits[1:0]		En APLL_2 man cal level	0x00
0x1788		APLL_3 V_{CAL} reference	Reserved					APLL_3 manual cal level, Bits[1:0]		En APLL_3 man cal level	0x00

REGISTER MAP BIT DESCRIPTIONS

SERIAL CONTROL PORT CONFIGURATION (REGISTER 0x0000 TO REGISTER 0x0001)

Table 33. SPI Configuration A (Note that the contents of Register 0x0000 are not stored to the EEPROM.)

Address	Bits	Bit Name	Description
0x0000	7	Soft reset (SPI only)	Device reset (invokes an EEPROM download or pin program ROM download if EEPROM is enabled).
	6	LSB first (SPI only)	Bit order for SPI port. This bit has no effect in I^{2}C mode. 1 = least significant bit first. 0 (default) = most significant bit first.
	5	Address ascension (SPI only)	This bit controls whether the register address is automatically incremented during a multibyte transfer. This bit has no effect in I^{2}C mode. 1 = Register addresses are automatically incremented in multibyte transfers. 0 (default) = Register addresses are automatically decremented in multibyte transfers.
	4	SDO active (SPI only)	Enables SPI port SDO pin. This bit has no effect in I^{2}C mode. 1 = 4-wire mode (SDO pin enabled). 0 (default) = 3-wire mode.
	[3:0]		These bits are mirrors of Bits[7:4] of this register so that when the serial port is configured, the pattern written is independent of an MSB first/LSB first setting interpretation. The AD9554 internal logic performs a logical OR on the corresponding bits. Bit 3 corresponds to Bit 4. Bit 2 corresponds to Bit 5. Bit 1 corresponds to Bit 6. Bit 0 corresponds to Bit 7.

Table 34. SPI Configuration B (Note that the contents of Register 0x0001 are not stored to the EEPROM.)

Address	Bits	Bit Name	Description
0x0001	[7:6]	Reserved	Reserved.
	5	Read buffer register	For buffered registers, this bit controls whether the value read from the serial port is from the actual (active) registers or the buffered copy. 1 = reads buffered values that take effect on the next assertion of IO_UPDATE. 0 (default) = reads values currently applied to the internal logic of the device.
	[4:3]	Reserved	Reserved.
	2	Reset sans regmap	This bit resets the device while maintaining the current register settings. 1 = resets the device. 0 (default) = no action.
	[1:0]	Reserved	Reserved.

CLOCK PART FAMILY ID (REGISTER 0x0003 TO REGISTER 0x0006)

Table 35. Clock Part Family ID

Address	Bits	Bit Name	Description
0x0003	[7:4]	Reserved	Reserved.
	[3:0]	Chip type, Bits[3:0]	The Analog Devices unified SPI protocol reserves this read only register location for identifying the type of device. The default value of 0x05 identifies the AD9554 as a clock IC.
0x0004	[7:4]	Clock part serial ID, Bits[3:0]	The Analog Devices unified SPI protocol reserves this read only register location as the lower four bits of the clock part serial ID that (along with Register 0x0005) uniquely identifies the AD9554 within the Analog Devices clock chip family. No other Analog Devices chip that adheres to the Analog Devices unified SPI has these values for Register 0x0003, Register 0x0004, and Register 0x0005. Default: 0x9F.
	[3:0]	Reserved	Default: 0xF.
0x0005	[7:0]	Clock part serial ID, Bits[11:4]	The Analog Devices unified SPI protocol reserves this read only register location as the upper eight bits of the clock part serial ID that (along with Register 0x0004) uniquely identifies the AD9554 within the Analog Devices clock chip family. No other Analog Devices chip that adheres to the Analog Devices unified SPI has these values for Register 0x0003, Register 0x0004, and Register 0x0005. Default: 0x00.
0x0006	[7:0]	Part version, Bits[7:0]	The Analog Devices unified SPI protocol reserves this read only register location for identifying the die revision. Default: 0x05.

SPI VERSION (REGISTER 0x000B)

Table 36. SPI Version

Address	Bits	Bit Name	Description
0x000B	[7:0]	SPI version, Bits[7:0]	The Analog Devices unified SPI protocol reserves this read only register location for identifying the version of the unified SPI protocol. Default: 0x00.

VENDOR ID (REGISTER 0x000C TO REGISTER 0x000D)

Table 37. Vendor ID

Address	Bits	Bit Name	Description
0x000C	[7:0]	Vendor ID, Bits[7:0]	The Analog Devices unified SPI protocol reserves this read only register location for identifying Analog Devices as the chip vendor of this device. All Analog Devices devices adhering to the unified serial port specification have the same value in this register. Default: 0x56.
0x000D	[7:0]	Vendor ID, Bits[15:8]	The Analog Devices unified SPI protocol reserves this read only register location for identifying Analog Devices as the chip vendor of this device. All Analog Devices devices adhering to the unified serial port specification have the same value in this register. Default: 0x04.

IO_UPDATE (REGISTER 0x000F)

Table 38. IO_UPDATE

Address	Bits	Bit Name	Description
0x000F	[7:1]	Reserved	Reserved. Default: 0000000b
	0	IO_UPDATE	Writing a 1 to this bit transfers the data in the serial input/output buffer registers to the internal control registers of the device. This is an autoclearing bit.

USER SCRATCHPAD (REGISTER 0x00FE TO REGISTER 0x00FF)

Table 39. User Scratchpad

Address	Bits	Bit Name	Description
0x00FE	[7:0]	User scratchpad, Bits[7:0]	This register has no effect on device operation. It is available for serial port debugging or register setting revision control. Default: 0x00.
0x00FF	[7:0]	User scratchpad, Bits[15:8]	This register has no effect on device operation. It is available for serial port debugging or register setting revision control. Default: 0x00.

GENERAL CONFIGURATION (REGISTER 0x0100 TO REGISTER 0x010E)

Multifunction Pin Control (M0 to M9) and Watchdog Timer

Table 40. Multifunction Pins (M0 to M9) Control

Address	Bits	Bit Name	Description
0x0100	[7:6]	M3 driver mode, Bits[1:0]	00 (default) = active high CMOS. 01 = active low CMOS. 10 = open-drain PMOS (requires an external pull-down resistor). 11 = open-drain NMOS (requires an external pull-up resistor).
	[5:4]	M2 driver mode, Bits[1:0]	The settings of these bits are identical to Register 0x0100, Bits[7:6].
	[3:2]	M1 driver mode, Bits[1:0]	The settings of these bits are identical to Register 0x0100, Bits[7:6].
	[1:0]	M0 driver mode, Bits[1:0]	The settings of these bits are identical to Register 0x0100, Bits[7:6].
0x0101	[7:6]	M7 driver mode, Bits[1:0]	The settings of these bits are identical to Register 0x0100, Bits[7:6].
	[5:4]	M6 driver mode, Bits[1:0]	The settings of these bits are identical to Register 0x0100, Bits[7:6].
	[3:2]	M5 driver mode, Bits[1:0]	The settings of these bits are identical to Register 0x0100, Bits[7:6].
	[1:0]	M4 driver mode, Bits[1:0]	The settings of these bits are identical to Register 0x0100, Bits[7:6].
0x0102	[7:4]	Reserved	Reserved.
	[3:2]	M9 driver mode, Bits[1:0]	The settings of these bits are identical to Register 0x0100, Bits[7:6].
	[1:0]	M8 driver mode, Bits[1:0]	The settings of these bits are identical to Register 0x0100, Bits[7:6].
0x0103	7	M0 output/$\overline{\text{input}}$	Input/output control for M0 pin. 0 (default) = input (control pin). 1 = output (status pin).
	[6:0]	M0 function, Bits[6:0]	These bits control the function of the M0 pin. See Table 154 and Table 155 for details about the input and output functions that are available. Default: 0x00 = high impedance control pin, no function assigned.
0x0104	7	M1 output/$\overline{\text{input}}$	Input/output control for M1 pin (same as for the M0 pin, Register0x0103, Bit 7).
	[6:0]	M1 function, Bits[6:0]	These bits control the function of the M1 pin and are the same as Register 0x0103, Bits[6:0]. Default: 0x00 = high impedance control pin, no function assigned.
0x0105	7	M2 output/$\overline{\text{input}}$	Input/output control for M2 pin (same as for the M0 pin, Register0x0103, Bit 7).
	[6:0]	M2 function, Bits[6:0]	These bits control the function of the M2 pin and are the same as Register 0x0103, Bits[6:0]. Default: 0x00 = high impedance control pin, no function assigned.
0x0106	7	M3 output/$\overline{\text{input}}$	Input/output control for M3 pin (same as for the M0 pin, Register0x0103, Bit 7).
	[6:0]	M3 function, Bits[6:0]	These bits control the function of the M3 pin and are the same as Register 0x0103, Bits[6:0]. Default: 0x00 = high impedance control pin, no function assigned.
0x0107	7	M4 output/$\overline{\text{input}}$	Input/output control for M4 pin (same as for the M0 pin, Register0x0103, Bit 7).
	[6:0]	M4 function, Bits[6:0]	These bits control the function of the M4 pin and are the same as Register 0x0103, Bits[6:0]. Default: 0x00 = high impedance control pin, no function assigned.
0x0108	7	M5 output/$\overline{\text{input}}$	Input/output control for M5 pin (same as for the M0 pin, Register0x0103, Bit 7).
	[6:0]	M5 function, Bits[6:0]	These bits control the function of the M5 pin and are the same as Register 0x0103, Bits[6:0]. Default: 0x00 = high impedance control pin, no function assigned.
0x0109	7	M6 output/$\overline{\text{input}}$	Input/output control for M6 pin (same as for the M0 pin, Register0x0103, Bit 7).
	[6:0]	M6 function, Bits[6:0]	These bits control the function of the M6 pin and are the same as Register 0x0103, Bits[6:0]. Default: 0x00 = high impedance control pin, no function assigned.
0x010A	7	M7 output/$\overline{\text{input}}$	Input/output control for M7 pin (same as for the M0 pin, Register0x0103).
	[6:0]	M7 function, Bits[6:0]	These bits control the function of the M7 pin and are the same as Register 0x0103, Bits[6:0]. Default: 0x00 = high impedance control pin, no function assigned.
0x010B	7	M8 output/$\overline{\text{input}}$	Input/output control for M8 pin (same as for the M0 pin, Register0x0103, Bit 7).
	[6:0]	M8 function, Bits[6:0]	These bits control the function of the M8 pin and are the same as Register 0x0103, Bits[6:0]. Default: 0x00 = high impedance control pin, no function assigned.
0x010C	7	M9 output/$\overline{\text{input}}$	Input/output control for M9 pin (same as for the M0 pin, Register0x0103, Bit 7).
	[6:0]	M9 function, Bits[6:0]	These bits control the function of the M9 pin and are the same as Register 0x0103, Bits[6:0]. Default: 0x00 = high impedance control pin, no function assigned.

Address	Bits	Bit Name	Description
0x010D	[7:0]	Watchdog timer	Watchdog timer, Bits[7:0]. The watchdog timer stops when this register is written and restarts on the next IO_UPDATE (Register 0x000F = 0x01). Default: 0x00 (0x0000 = disabled). The units are in milliseconds.
0x010E	[7:0]		Watchdog timer, Bits[15:8]. The watchdog timer stops when this register is written and restarts on the next IO_UPDATE (Register 0x000F = 0x01). Default: 0x00.

IRQ MASK (REGISTER 0x010F TO REGISTER 0x011F)

The IRQ mask register bits form a one-to-one correspondence with the bits of the IRQ monitor register (0x0D08 to 0x0D16). When set to Logic 1, the IRQ mask bits enable the corresponding IRQ monitor bits to indicate an IRQ event. The default for all IRQ mask bits is Logic 0, which prevents the IRQ monitor from detecting any internal interrupts.

Table 41. IRQ Mask for SYSCLK, Watchdog Timer, and EEPROM

Address	Bits	Bit Name	Description
0x010F	7	SYSCLK unlocked	Enables IRQ to indicate that the system clock has gone from locked to unlocked.
	6	SYSCLK stable	Enables IRQ to indicate that the system clock has gone from unstable to stable.
	5	SYSCLK locked	Enables IRQ to indicate that the system clock has gone from unlocked to locked.
	4	SYSCLK calibration ended	Enables IRQ to indicate that the system clock calibration sequence has ended.
	3	SYSCLK calibration started	Enables IRQ to indicate that the system clock calibration sequence has started.
	2	Watchdog timer	Enables IRQ to indicate expiration of the watchdog timer.
	1	EEPROM fault	Enables IRQ to indicate a fault during an EEPROM upload or download operation.
	0	EEPROM complete	Enables IRQ to indicate successful completion of an EEPROM upload or download operation.

Table 42. IRQ Mask for Reference Inputs

Address	Bits	Bit Name	Description
0x0110	7	Reserved	Reserved.
	6	REFB validated	Enables IRQ to indicate that REFB has been validated.
	5	REFB fault cleared	Enables IRQ to indicate that REFB has been cleared of a previous fault.
	4	REFB fault	Enables IRQ to indicate that REFB has been faulted.
	3	Reserved	Reserved.
	2	REFA validated	Enables IRQ to indicate that REFA has been validated.
	1	REFA fault cleared	Enables IRQ to indicate that REFA has been cleared of a previous fault.
	0	REFA fault	Enables IRQ to indicate that REFA has been faulted.
0x0111	7	Reserved	Reserved.
	6	REFD validated	Enables IRQ to indicate that REFD has been validated.
	5	REFD fault cleared	Enables IRQ to indicate that REFD has been cleared of a previous fault.
	4	REFD fault	Enables IRQ to indicate that REFD has been faulted.
	3	Reserved	Reserved.
	2	REFC validated	Enables IRQ to indicate that REFC has been validated.
	1	REFC fault cleared	Enables IRQ to indicate that REFC has been cleared of a previous fault.
	0	REFC fault	Enables IRQ to indicate that REFC has been faulted.

Table 43. IRQ Mask for the Digital PLL0 (DPLL_0)

Address	Bits	Bit Name	Description
0x0112	7	Frequency unclamped	Enables IRQ to indicate that DPLL_0 has exited a frequency clamped state.
	6	Frequency clamped	Enables IRQ to indicate that DPLL_0 has entered a frequency clamped state.
	5	Phase slew unlimited	Enables IRQ to indicate that DPLL_0 has exited a phase slew limited state.
	4	Phase slew limited	Enables IRQ to indicate that DPLL_0 has entered a phase slew limited state.
	3	Frequency unlocked	Enables IRQ to indicate that DPLL_0 has lost frequency lock.
	2	Frequency locked	Enables IRQ to indicate that DPLL_0 has acquired frequency lock.
	1	Phase unlocked	Enables IRQ to indicate that DPLL_0 has lost phase lock.
	0	Phase locked	Enables IRQ to indicate that DPLL_0 has acquired phase lock.
0x0113	7	Switching	Enables IRQ to indicate that DPLL_0 is switching to a new reference.
	6	Free run	Enables IRQ to indicate that DPLL_0 has entered free run mode.
	5	Holdover	Enables IRQ to indicate that DPLL_0 has entered holdover mode.
	4	History updated	Enables IRQ to indicate that DPLL_0 has updated its tuning word history.
	3	REFD activated	Enables IRQ to indicate that DPLL_0 has activated REFD.
	2	REFC activated	Enables IRQ to indicate that DPLL_0 has activated REFC.
	1	REFB activated	Enables IRQ to indicate that DPLL_0 has activated REFB.
	0	REFA activated	Enables IRQ to indicate that DPLL_0 has activated REFA.
0x0114	7	Phase step detection	Enables IRQ to indicate that DPLL_0 has detected a large phase step at the reference input.
	6	Demap control unclamped	Enables IRQ to indicate that the DPLL_0 demapping controller tuning word has become unclamped.
	5	Demap control clamped	Enables IRQ to indicate that the DPLL_0 demapping controller tuning word has become clamped.
	4	Sync clock distribution	Enables IRQ for indicating a distribution sync event.
	3	APLL_0 unlocked	Enables IRQ for APLL_0 unlocked.
	2	APLL_0 locked	Enables IRQ for APLL_0 locked.
	1	APLL_0 calibration complete	Enables IRQ for APLL_0 calibration complete.
	0	APLL_0 calibration started	Enables IRQ for APLL_0 calibration started.

Table 44. IRQ Mask for the Digital PLL1 (DPLL_1)

Address	Bits	Bit Name	Description
0x0115	[7:0]	See Table 43	IRQ mask for DPLL_1, same as IRQ mask for the digital PLL0 (DPLL_0) registers (Register 0x0112 through Register 0x0114). All default values are identical.
0x0116	[7:0]	See Table 43	
0x0117	[7:0]	See Table 43	

Table 45. IRQ Mask for the Digital PLL2 (DPLL_2)

Address	Bits	Bit Name	Description
0x0118	[7:0]	See Table 43	IRQ mask for DPLL_2, same as IRQ mask for the digital PLL0 (DPLL_0) registers (Register 0x0112 through Register 0x0114). All default values are identical.
0x0119	[7:0]	See Table 43	
0x011A	[7:0]	See Table 43	

Table 46. IRQ Mask for the Digital PLL3 (DPLL_3)

Address	Bits	Bit Name	Description
0x011B	[7:0]	See Table 43	IRQ mask for DPLL_3, same as IRQ mask for the digital PLL0 (DPLL_0) registers (Register 0x0112 through Register 0x0114). All default values are identical.
0x011C	[7:0]	See Table 43	
0x011D	[7:0]	See Table 43	

Table 47. Pad Control for Mx Pins

Address	Bits	Bit Name	Description
0x011E	7	M7 configuration	M7 pin output drive strength. 0 (default) = high (approximately 6 mA) drive strength. 1 = low (approximately 3 mA) drive strength.
	6	M6 configuration	Same as Bit 7 of this register, except that it applies to the M6 pin.
	5	M5 configuration	Same as Bit 7 of this register, except that it applies to the M5 pin.
	4	M4 configuration	Same as Bit 7 of this register, except that it applies to the M4 pin.
	3	M3 configuration	Same as Bit 7 of this register, except that it applies to the M3 pin.
	2	M2 configuration	Same as Bit 7 of this register, except that it applies to the M2 pin.
	1	M1 configuration	Same as Bit 7 of this register, except that it applies to the M1 pin.
	0	M0 configuration	Same as Bit 7 of this register, except that it applies to the M0 pin.
0x011F	[7:3]	Reserved	Default: 00000b.
	2	SPI configuration	Same as Bit 7 of Register 0x011E, except that it applies to the M6 pin.
	1	M9 configuration	Same as Bit 7 of Register 0x011E, except that it applies to the M9 pin.
	0	M8 configuration	Same as Bit 7 of Register 0x011E, except that it applies to the M8 pin.

SYSTEM CLOCK (REGISTER 0x0200 TO REGISTER 0x0208)

Table 48. System Clock PLL Feedback Divider (K Divider) and Configuration

Address	Bits	Bit Name	Description
0x0200	[7:0]	System clock K divider, Bits[7:0]	System clock PLL feedback divider value = 4 ≤ K ≤ 255. Default: 0x00.

Table 49. SYSCLK Configuration

Address	Bits	Bit Name	Description
0x0201	[7:4]	Reserved	Reserved.
	3	SYSCLK XTAL enable	Enables the crystal maintaining amplifier for the system clock input. 1 (default) = crystal mode (crystal maintaining amplifier enabled). 0 = external crystal oscillator or other system clock source.
	[2:1]	SYSCLK J1 divider, Bits[1:0]	System clock input divider. 00 (default): ÷1. 01: ÷2. 10: ÷4. 11: ÷8.
	0	SYSCLK doubler enable (J0 divider)	Enables the clock doubler on the system clock input to reduce noise. Setting this bit may prevent the SYSCLK PLL from locking if the input duty cycle is not close enough to 50%. See Table 4 for the limits on duty cycle. 0 (default) = disable. 1 = enable.

Table 50. System Clock Reference Frequency

Address	Bits	Bit Name	Description
0x0202	[7:0]	System clock reference frequency (Hz), Bits[23:0]	System clock reference frequency, Bits[7:0]. Default: 0x00.
0x0203	[7:0]		System clock reference frequency, Bits[15:8]. Default: 0x00.
0x0204	[7:0]		System clock reference frequency, Bits[23:16]. Default: 0x00.
0x0205	[7:4]	Reserved	Default: 0x0.
	[3:0]	System clock reference frequency(Hz), Bits[27:24]	System clock reference frequency, Bits[27:24]. Default: 0x0.

Table 51. System Clock Stability Period

Address	Bits	Bit Name	Description
0x0206	[7:0]	System clock stability period (ms), Bits[15:0]	System clock period, Bits[7:0]. The system clock stability period is the amount of time that the system clock PLL must be locked before it is declared stable. The system clock stability period is reset automatically if the user writes to this register. The system clock stability period restarts on the next IO_UPDATE (Register 0x000F = 0x01). Default: 0x32 (0x000032 = 50 ms).
0x0207	[7:0]		System clock period, Bits[15:8]. The system clock stability period is reset automatically if the user writes to this register. The system clock stability timer restarts on the next IO_UPDATE (Register 0x000F = 0x01). Default: 0x00.
0x0208	[7:4]	Reserved	Default: 0x0.
	[3:0]	System clock stability period, Bits[19:16]	System clock period, Bits[19:16]. The system clock stability period is reset automatically if the user writes to this register. The system clock stability period restarts on the next IO_UPDATE (Register 0x000F = 0x01). Default: 0x0. The units are in milliseconds.

REFERENCE INPUT A (REGISTER 0x0300 TO REGISTER 0x031E)

Table 52. REFA Logic Type

Address	Bits	Bit Name	Description
0x0300	[7:2]	Reserved	Default: 000000b.
	[1:0]	REFA logic type, Bits[1:0]	Selects logic family for REFA input receiver; only the REFA pin is used in CMOS mode. 00b (default) = 1.8 V or 1.5 V single-ended CMOS. 01b = ac-coupled differential. 10b = dc-coupled LVDS (f_{IN} ≤ 10.24 MHz). 11b = unused.

Table 53. REFA R Divider (20 Bits) DPLL

Address	Bits	Bit Name	Description
0x0301	[7:0]	R divider, Bits[15:0]	DPLL integer reference divider (minus 1), Bits[7:0]. Default: 0x00. (For example, 0x00000 equals an R divider of 1.)
0x0302	[7:0]		DPLL integer reference divider (minus 1), Bits[15:8]. Default: 0x00.
0x0303	[7:4]	Reserved	Default: 0x0.
	[3:0]	R divider, Bits[19:16]	DPLL integer reference divider (minus 1), Bits[19:16]. Default: 0x0.

Table 54. Nominal Period of REFA Input Clock

Address	Bits	Bit Name	Description
0x0304	[7:0]	REFA period (fs), Bits[39:0]	Nominal reference period, Bits[7:0]. Default: 0x00.
0x0305	[7:0]		Nominal reference period, Bits[15:8]. Default: 0x00.
0x0306	[7:0]		Nominal reference period, Bits[23:16]. Default: 0x00.
0x0307	[7:0]		Nominal reference period, Bits[31:24]. Default: 0x00.
0x0308	[7:0]		Nominal reference period, Bits[39:32]. Default: 0x00.

Table 55. REFA Frequency Tolerance

Address	Bits	Bit Name	Description
0x0309	[7:0]	Inner tolerance (1/(ppm error)), Bits[15:0]	Input reference frequency monitor inner tolerance, Bits[7:0]. Default: 0x14.
0x030A	[7:0]		Input reference frequency monitor inner tolerance, Bits[15:8]. Default: 0x00.
0x030B	[7:4]	Reserved	Default: 0x0.
	[3:0]	Inner tolerance (1/(ppm error)), Bits[19:16]	Input reference frequency monitor inner tolerance, Bits[19:16]. Default for Register 0x0309 to Register 0x30B: 0x000014 = 20 (5% or 50,000 ppm). The Stratum 3 clock requires an inner tolerance of ±9.2 ppm and an outer tolerance of ±12 ppm. An SMC clock requires an outer tolerance of ±48 ppm. The allowable range for the inner tolerance is 0x00A (10%) to 0x8FF (2 ppm).
0x030C	[7:0]	Outer tolerance (1/(ppm error)), Bits[15:0]	Input reference frequency monitor outer tolerance, Bits[7:0]. Default: 0x0A.
0x030D	[7:0]		Input reference frequency monitor outer tolerance, Bits[15:8]. Default: 0x00.
0x030E	[7:4]	Reserved	Default: 0x0.
	[3:0]	Outer tolerance (1/(ppm error)), Bits[19:16]	Input reference frequency monitor outer tolerance, Bits[19:16]. Default for Register 0x030C to Register 0x30E = 0x00000A = 10 (10% or 100,000 ppm). The Stratum 3 clock requires an inner tolerance of ±9.2 ppm and an outer tolerance of ±12 ppm. An SMC clock requires an outer tolerance of ±48 ppm. The outer tolerance must be greater than the inner tolerance so that there is hysteresis.

Table 56. REFA Validation Timer

Address	Bits	Bit Name	Description
0x030F	[7:0]	Validation timer (ms), Bits[15:0] (up to 65.5 sec)	Validation timer, Bits[7:0]. Default: 0x0A. This is the amount of time a reference input must be unfaulted before it is declared valid by the reference input monitor. Default: 10 ms.
0x0310	[7:0]		Validation timer, Bits[15:8]. Default: 0x00.

Table 57. REFA Phase/Frequency Lock Detectors

Address	Bits	Bit Name	Description
0x0311	[7:0]	Phase lock threshold (ps), Bits[23:0]	Phase lock threshold, Bits[7:0]. Default: 0xBC. Default of 0x0002BC for Register 0x0311 through Register 0x313 = 700 ps.
0x0312	[7:0]		Phase lock threshold, Bits[15:8]. Default: 0x02.
0x0313	[7:0]		Phase lock threshold, Bits[23:16]. Default: 0x00.
0x0314	[7:0]	Phase lock fill rate, Bits[7:0]	Phase lock fill rate, Bits[7:0]. Default: 0x0A = 10 code/PFD cycle.
0x0315	[7:0]	Phase lock drain rate, Bits[7:0]	Phase lock drain rate, Bits[7:0]. Default: 0x0A = 10 code/PFD cycle.
0x0316	[7:0]	Frequency lock threshold (ps), Bits[23:0]	Frequency lock threshold, Bits[7:0]. Default: 0xBC. Default of 0x0002BC for Register 0x0316 through Register 0x318 = 700 ps. This is correct.
0x0317	[7:0]		Frequency lock threshold, Bits[15:8]. Default: 0x02.
0x0318	[7:0]		Frequency lock threshold, Bits[23:16]. Default: 0x00.
0x0319	[7:0]	Frequency lock fill rate, Bits[7:0]	Frequency lock fill rate, Bits[7:0]. Default: 0x0A = 10 code/PFD cycle.
0x031A	[7:0]	Frequency lock drain rate, Bits[7:0]	Frequency lock drain rate, Bits[7:0]. Default: 0x0A = 10 code/PFD cycle.

Table 58. REFA Phase Step Threshold

Address	Bits	Bit Name	Description
0x031B	[7:0]	Phase step threshold (ps), Bits[23:0]	Phase step threshold, Bits[7:0]. Default: 0x00. Note that a phase step threshold of 0x000000 means that this feature is disabled.
0x031C	[7:0]		Phase step threshold, Bits[15:8]. Default: 0x00.
0x031D	[7:0]		Phase step threshold, Bits[23:16]. Default: 0x00.
0x031E	[7:4]	Reserved	Default: 0x0.
	[3:0]	Phase step threshold (ps), Bits[27:24]	Phase step threshold, Bits[27:24].

REFERENCE INPUT B (REGISTER 0x0320 TO REGISTER 0x033E)

These registers mimic the Reference Input A registers (Register 0x0300 through Register 0x031E) but the register addresses are offset by 0x0020. All default values are identical.

REFERENCE INPUT C (REGISTER 0x0340 TO REGISTER 0x035E)

These registers mimic the Reference Input A registers (Register 0x0300 through Register 0x031E) but the register addresses are offset by 0x0040. All default values are identical.

REFERENCE INPUT D (REGISTER 0x0360 TO REGISTER 0x037E)

These registers mimic the Reference Input A registers (Register 0x0300 through Register 0x031E) but the register addresses are offset by 0x0060. All default values are identical.

DPLL_0 CONTROLS (REGISTER 0x0400 TO REGISTER 0x041E)

Table 59. DPLL_0 Free Run Frequency Tuning Word

Address	Bits	Bit Name	Description
0x0400	[7:0]	30-bit free running frequency tuning word Bits[23:0]	Free running frequency tuning word, Bits[7:0]. Default: 0x00.
0x0401	[7:0]		Free running frequency tuning word, Bits[15:8]. Default: 0x00.
0x0402	[7:0]		Free running frequency tuning word, Bits[23:16]. Default: 0x00.
0x0403	[7:6]	Reserved	Default: 00b.
	[5:0]	30-bit free running frequency tuning word Bits[29:24]	Free running frequency tuning word, Bits[29:24]. Default: 0x00.

Table 60. DPLL_0 DCO Integer

Address	Bits	Bit Name	Description
0x0404	[7:4]	Reserved	This register is used internally. It is usually 0x1 but may differ depending on how the device is configured. When writing to this register, read the current value and write the same value back to this register.
	[3:0]	DCO integer, Bits[3:0]	This register contains the integer part of the DCO frequency divider. Valid values are 0x7 to 0xD, and the AD9554 evaluation software frequency planning wizard can help determine the optimal value. Default: 0x7.

Table 61. DPLL_0 Frequency Clamp

Address	Bits	Bit Name	Description
0x0405	[7:0]	Lower limit of pull-in range, Bits [15:0]	Lower limit pull-in range, Bits[7:0]. The value in these registers is the 20 most significant bits of the lowest allowable tuning word used by the DPLL. Default: 0xCC.
0x0406	[7:0]		Lower limit pull-in range, Bits[15:8]. Default: 0xCC.
0x0407	[7:4]	Reserved	Default: 0x0.
	[3:0]	Lower limit of pull-in range, Bits[19:16]	Lower limit pull-in range, Bits[19:16]. Default: 0x0.
0x0408	[7:0]	Upper limit of pull-in range, Bits[15:0]	Upper limit pull-in range, Bits[7:0]. Default: 0x33.
0x0409	[7:0]		Upper limit pull-in range, Bits[15:8]. Default: 0x33.
0x040A	[7:4]	Reserved	Default: 0x0.
	[3:0]	Upper limit of pull-in range, Bits[19:16]	Upper limit pull-in range, Bits[19:16]. Default: 0xF.

Table 62. DPLL_0 Holdover History

Address	Bits	Bit Name	Description
0x040B	[7:0]	DPLL_0 history accumulation timer (ms), Bits[15:0]	History accumulation timer, Bits[7:0]. Default: 0x0A. For Register 0x040B and Register 0x040C, 0x000A = 10 ms. Maximum: 65 sec. This register controls the amount of tuning word averaging that determines the tuning word used in holdover. Behavior is undefined for a timer value of 0. Default value: 0x000A = 10 ms.
0x040C	[7:0]		History accumulation timer, Bits[15:8]. Default: 0x00.

Table 63. DPLL_0 History Mode

Address	Bits	Bit Name	Description
0x040D	[7:5]	Reserved	Reserved.
	4	Single sample fallback	Controls holdover history. If tuning word history is not available for the reference that was active just prior to holdover, then the following: 0 (default) = uses the free running frequency tuning word register value. 1 = uses the last tuning word from the DPLL.
	3	Persistent history	Controls holdover history initialization. When switching to a new reference: 0 (default) = clears the tuning word history. 1 = retains the previous tuning word history.
	[2:0]	Incremental average, Bits[2:0]	History mode value from 0 to 7. Default: 0. When set to nonzero, causes the first history accumulation to update prior to the first complete averaging period. After the first full interval, updates occur only at the full period. 0 (default) = update only after the full interval has elapsed. 1 = update at 1/2 the full interval. 2 = update at 1/4 and 1/2 of the full interval. 3 = update at 1/8, 1/4, and 1/2 of the full interval. … 7 = update at 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, and 1/2 of the full interval.

Table 64. DPLL_0 Fixed Closed Loop Phase Offset

Address	Bits	Bit Name	Description
0x040E	[7:0]	Fixed phase offset (signed; ps)	Fixed phase offset, Bits[7:0]. Default: 0x00.
0x040F	[7:0]		Fixed phase offset, Bits[15:8]. Default 0x00.
0x0410	[7:0]		Fixed phase offset, Bits[23:16]. Default: 0x00.
0x0411	[7:6]	Reserved	Reserved; default: 0x0.
	[5:0]	Fixed phase offset (signed; ps)	Fixed phase offset, Bits[29:24]. Default: 0x00.

Table 65. DPLL_0 Incremental Closed-Loop Phase Offset Step Size

Address	Bits	Bit Name	Description
0x0412	[7:0]	Incremental phase offset step size (ps), Bits[15:0]	Incremental phase offset step size, Bits[7:0]. Default: 0x00. This register controls the static phase offset step size of the DPLL while it is locked. See Register 0x0A24 for the bits that increment, decrement, and reset the phase offset.
0x0413	[7:0]		Incremental phase offset step size, Bits[15:8]. Default: 0x00. This register controls the static phase offset step size of the DPLL while it is locked.

Table 66. DPLL_0 Phase Slew Rate Limit

Address	Bits	Bit Name	Description
0x0414	[7:0]	Phase slew rate limit (μs/sec), Bits[15:0]	Phase slew rate limit, Bits[7:0]. Default: 0x00. This register controls the maximum allowable phase slewing during phase adjustment. (The phase adjustment controls are in Register 0x040E to Register 0x0411.) Default phase slew rate limit: 0, or disabled. Minimum useful value is 100 μs/sec.
0x0415	[7:0]		Phase slew rate limit, Bits[15:8]. Default = 0x00.

Table 67. DPLL_0 Demapping Control

Address	Bits	Bit Name	Description
0x0416	[7:1]	Reserved	Reserved, Bits[7:1] (default: 0x00)
	0	Enable demap controller	Enables the demapping controller. 0 (default) = The demapping controller is disabled. 1 = The demapping controller is enabled.
0x0417	[7:0]	Sampled address, Bits[15:0]	Sampled address, Bits[7:0]. Default: 0x00.
0x0418	[7:0]		Sampled address, Bits[15:8]. Default: 0x00.
0x0419	[7:0]	Set point address, Bits[15:0]	Set point address, Bits[7:0]. Default: 0x00.
0x041A	[7:0]		Set point address, Bits[15:8]. Default: 0x00.
0x041B	[7:0]	Gain, Bits[23:0]	Gain, Bits[7:0]. Default: 0x00.
0x041C	[7:0]		Gain, Bits[15:8]. Default: 0x00.
0x041D	[7:0]		Gain, Bits[23:16]. Default: 0x00.
0x041E	[7:0]	Clamp value, Bits[7:0]	Clamp value, Bits[7:0]. Default: 0x00.

APLL_0 CONFIGURATION (REGISTER 0x0430 TO REGISTER 0x0434)

Table 68. Output PLL_0 (APLL_0) Setting[1]

Address	Bits	Bit Name	Description			
0x0430	7	Reserved	Default: 0b.			
	[6:0]	Output PLL0 (APLL_0) charge pump current, Bits[6:0]	LSB: 3.5 μA. 0000001b = 1 × LSB; 0000010b = 2 × LSB; 1111111b = 127 × LSB. Default: 0x2E = 451 μA CP current.			
0x0431	[7:0]	Output PLL0 (APLL_0) feedback M0 divider, Bits[7:0]	Division: 14 to 255. Default: 0x00.			
0x0432	[7:6]	APLL_0 loop filter control, Bits[7:0]	Second pole resistor (R_{P2}). Default: 0x7F.			
			R_{P2} (Ω)	**Bit 7**	**Bit 6**	
			500	0	0	
			333 (default)	0	1	
			250	1	0	
			200	1	1	
	[5:3]		Zero resistor (R_{ZERO}).			
			R_{ZERO} (Ω)	**Bit 5**	**Bit 4**	**Bit 3**
			1500	0	0	0
			1250	0	0	1
			1000	0	1	0
			930	0	1	1
			1250	1	0	0
			1000	1	0	1
			750	1	1	0
			680 (default)	1	1	1
	[2:0]		First pole capacitor (C_{P1}).			
			C_{P1} (pF)	**Bit 2**	**Bit 1**	**Bit 0**
			10	0	0	0
			30	0	0	1
			40	0	1	0
			70	0	1	1
			90	1	0	0
			110	1	0	1
			130	1	1	0
			150 (default)	1	1	1

Address	Bits	Bit Name	Description
0x0433	[7:2]	Reserved	Default: 0x00.
	1	P0 divider reset	0 (default) = normal operation for the P0 divider. 1 = P0 divider held in reset.
	0	APLL_0 loop filter control, Bit 8	Bypass internal R_{ZERO}.
			0 (default) = use the internal R_{ZERO} resistor.
			1 = bypass the internal R_{ZERO} resistor (makes R_{ZERO} = 0 Ω and requires the use of an external zero resistor in addition to the capacitor to ground on the LF_0 pin).

[1] Note that the default APLL loop bandwidth is 240 kHz.

OUTPUT PLL_0 (APLL_0) SYNC AND CLOCK DISTRIBUTION (REGISTER 0x0434 TO REGISTER 0x043E)

Table 69. P0 Divider Settings[1]

Address	Bits	Bit Name	Description
0x0434	[7:4]	Reserved	Default: 0x0.
	[3:0]	P0 divider divide ratio, Bits[3:0]	0000b (default)/0001b: undefined. 0010b: ÷2. This setting is permitted only if the APLL VCO frequency is ≤2500 MHz. 0011b: ÷3. 0101b: ÷5. 0110b: ÷6. 0111b: ÷7. 1000b: ÷8. 1001b: ÷9. 1010 b: ÷10. 1011b: ÷11.

[1] If the user changes this register after APLL calibration, the user must either issue another APLL calibration (see Figure 28), or issue a P divider reset for that PLL. For example, if the user reconfigures the P0 divider after APLL_0 calibration, the user must reset the P0 divider using Bit 1 in Register 0x0433.

Table 70. Distribution Output Synchronization Settings (OUT0)

Address	Bits	Bit Name	Description
0x0435	[7:3]	Reserved	Default: 0x00.
	2	Sync source selection	Selects the sync source for the clock distribution output channels. 0 (default) = direct. The sync pulse is gated only by APLL calibration and lock. 1 = active reference. This mode is similar to direct mode except that the sync pulse occurs on the next edge of the actively selected reference.
	[1:0]	Automatic sync mode, Bits[1:0]	Auto sync mode. 00 = (default) disabled. 01 = sync on DPLL frequency lock. 10 = sync on DPLL phase lock. 11 = reserved.
0x0436	[7:3]	Reserved	Reserved.
	2	APLL_0 mask sync	0 (default) = the clock distribution SYNC function is delayed until the APLL has been calibrated and is locked. After APLL calibration and lock, the output clock distribution sync is armed, and the SYNC function for the clock outputs is under the control of Register 0x0435. 1 = overrides the lock detector state of the APLL; allows Register 0x0435 to control the output SYNC function, regardless of the APLL lock status.
	1	Mask OUT0B sync	Masks the synchronous reset to the OUT0B divider. 0 (default) = unmasked. 1 = masked. Setting this bit asynchronously releases the OUT0B divider from static sync state, thus allowing the OUT0B divider to toggle. OUT0B ignores all sync events while this bit is set. Setting this bit does not enable the output drivers connected to this channel.

Address	Bits	Bit Name	Description
	0	Mask OUT0A sync	Masks the synchronous reset to the OUT0A divider. 0 (default) = unmasked. 1 = masked. Setting this bit asynchronously releases the OUT0A divider from static sync state, thus allowing the OUT0A divider to toggle. OUT0A ignores all sync events while this bit is set. Setting this bit does not enable the output drivers connected to this channel.

Table 71. Distribution OUT0A Settings

Address	Bits	Bit Name	Description
0x0437	[7:3]	Reserved	Default: 00.
	[2:1]	OUT0A mode	Selects the operating mode of OUT0A. 00 (default) = 14 mA (used for ac-coupled LVDS and dc-coupled HCSL). 01 = 21 mA (intended as an intermediate amplitude setting). 10 = 28 mA (used for ac-coupled LVPECL-compatible amplitudes with 100 Ω termination). Damage to the output drivers can result if the 28 mA mode is used without external termination resistors (either to ground or across the differential pair). 11 = power down and tristate outputs.
	0	Invert polarity	Controls the OUT0A polarity. 0 (default) = normal polarity. 1 = inverted polarity.

Table 72. Q0_A Divider Settings

Address	Bits	Bit Name	Description
0x0438	[7:0]	Q0_A divider , Bits[7:0]	10-bit channel divider, Bits[7:0] (LSB). Division equals channel divider, Bits[9:0] + 1. Default: 0x00. [9:0] = 0 is divide-by-1. [9:0] = 1 is divide-by-2. … [9:0] = 1023 is divide-by-1024.
0x0439	[7:2]	Reserved	Reserved. Default: 0x00.
	[1:0]	Q0_A divider, Bits[9:8]	10-bit channel divider, Bits[9:8] (MSB). Default: 0x0.
0x043A	[7:6]	Reserved	Reserved. Default: 0x0.
	[5:0]	Q0_A divider phase, Bits[5:0]	Divider initial phase after sync relative to the divider input clock (from the P0 divider output). LSB is ½ of a period of the divider input clock. Phase = 0 is no phase offset. Phase = 1 is ½ a period offset. Default: 0x0.

Table 73. Distribution OUT0B Settings

Address	Bits	Bit Name	Description
0x043B	[7:3]	Reserved	Reserved. Default: 0x00
	[2:1]	OUT0B mode	Selects the operating mode of OUT0B. 00 (default) = 14 mA (used for ac-coupled LVDS and dc-coupled HCSL). 01 = 21 mA (intended as an intermediate amplitude setting). 10 = 28 mA (used for ac-coupled LVPECL-compatible amplitudes with 100 Ω termination).Damage to the output drivers can result if the 28 mA mode is used without external termination resistors (either to ground or across the differential pair). 11 = power down and tristate outputs.
	0	Invert polarity	Controls the OUT0B polarity. 0 (default) = normal polarity. 1= inverted polarity.

Table 74. Q0_B Divider Setting

Address	Bits	Bit Name	Description
0x043C	[7:0]	Q0_B divider, Bits[7:0]	10-bit channel divider, Bits[7:0] (LSB). Default: 0x00. Division equals channel divider, Bits[9:0] + 1. [9:0] = 0 is divide-by-1. [9:0] = 1 is divide-by-2. … [9:0] = 1023 is divide-by-1024.
0x043D	[7:2]	Reserved	Default: 0x00.
	[1:0]	Q0_B divider, Bits[9:8]	10-bit channel divider, Bits[9:8] (MSB).
0x043E	[7:6]	Reserved	Default: 0x0.
	[5:0]	Q0_B divider phase, Bits[5:0]	Divider initial phase after sync relative to the divider input clock (from the P0 divider output). LSB is ½ of a period of the divider input clock. Default: 0x0. Phase = 0 is no phase offset. Phase = 1 is ½ a period offset.

DPLL_0 SETTINGS FOR REFERENCE INPUT A (REFA) (REGISTER 0x0440 TO REGISTER 0x044C)

Table 75. DPLL_0 REFA Priority Setting

Address	Bits	Bit Name	Description
0x0440	[7:3]	Reserved	Default: 00000b.
	[2:1]	REFA priority	These bits set the priority level (0 to 3) of REFA relative to the other input references. 00 (default) = 0 (highest). 01 = 1. 10 = 2. 11 = 3.
	0	Enable REFA	This bit enables DPLL_0 to lock to REFA. 0 (default) = REFA is not enabled for use by DPLL_0. 1 = REFA is enabled for use by DPLL_0.

Table 76. DPLL_0 REFA Loop Bandwidth Scaling Factor

Address	Bits	Bit Name	Description
0x0441	[7:0]	Digital PLL_0 loop bandwidth scaling factor, Bits[15:0] (unit of 0.1 Hz)	Digital PLL loop bandwidth scaling factor, Bits[7:0]. Default: 0x0.
0x0442	[7:0]		Digital PLL loop bandwidth scaling factor, Bits[15:8]. Default: 0x00. The default for Register 0x0441 to Register 0x0443 = 0x000000. The loop bandwidth must always be less than the DPLL phase detector frequency divided by 50. The DPLL may not lock reliably if the DPLL loop bandwidth is <50 Hz and a crystal is used for the system clock. See the Choosing the SYSCLK Source section for details.
0x0443	[7:2]	Reserved	Default: 0x00.
	1	Base loop filter selection	0 = base loop filter with normal (70°) phase margin (default). 1 = base loop filter with high phase margin. (For loop bandwidth ≤2 kHz, there is ≤0.1 dB peaking in the closed-loop transfer function. Setting this bit is also recommended for loop bandwidths >2 kHz.)
	0	Digital PLL_0 loop BW scaling factor, Bit 16 (unit of 0.1 Hz)	Digital PLL loop bandwidth scaling factor, Bit 16. Default: 0x0.

Table 77. DPLL_0 REFA Integer Part of Feedback (N0) Divider

Address	Bits	Bit Name	Description
0x0444	[7:0]	Digital PLL_0 feedback divider—Integer Part N0	DPLL integer feedback divider (minus 1), Bits[7:0]. Default: 0x00. (For example, an N0 divider value of one is achieved by writing 0x000000 to Register 0x0444 to Register 0x0446.)
0x0445	[7:0]		DPLL integer feedback divider, Bits[15:8]. Default: 0x00.
0x0446	[7:2]	Reserved	Default: 0x00.
	[1:0]	Digital PLL_0 feedback divider—Integer Part N0	DPLL integer feedback divider, Bits[17:16]. Default: 0b. Default for Register 0x0444 to Register 0x0446: 0x000000.

Table 78. DPLL_0 REFA Fractional Part of Fractional Feedback Divider—FRAC0

Address	Bits	Bit Name	Description
0x0447	[7:0]	Digital PLL_0 fractional feedback divider—FRAC0, Bits[23:0]	The numerator of the fractional-N feedback divider, Bits[7:0]. Default: 0x00.
0x0448	[7:0]		The numerator of the fractional-N feedback divider, Bits[15:8]. Default: 0x00.
0x0449	[7:0]		The numerator of the fractional-N feedback divider, Bits[23:16]. Default: 0x00.

Table 79. DPLL_0 REFA Modulus of Fractional Feedback Divider—MOD0

Address	Bits	Bit Name	Description
0x044A	[7:0]	Digital PLL_0 feedback divider modulus—MOD0, Bits[23:0]	The denominator of the fractional-N feedback divider, Bits[7:0]. Default: 0x00. Setting MOD0 to 0x000000 disables and bypasses the fractional divider.
0x044B	[7:0]		The denominator of the fractional-N feedback divider, Bits[15:8]. Default: 0x00.
0x044C	[7:0]		The denominator of the fractional-N feedback divider, Bits[23:16]. Default: 0x00.

DPLL_0 SETTINGS FOR REFERENCE INPUT B (REFB) (REGISTER 0x044D TO REGISTER 0x0459)

Table 80. DPLL_0 REFB Priority Setting

Address	Bits	Bit Name	Description
0x044D	[7:3]	Reserved	Default: 0x00.
	[2:1]	REFB priority	These bits set the priority level (0 to 3) of REFB relative to the other input references. 00 (default) = 0 (highest). 01 = 1. 10 = 2. 11 = 3.
	0	Enable REFB	This bit enables DPLL_0 to lock to REFB. 0 (default) = REFB is not enabled for use by DPLL_0. 1 = REFB is enabled for use by DPLL_0.

Table 81. DPLL_0 REFB Loop Bandwidth Scaling Factor

Address	Bits	Bit Name	Description
0x044E	[7:0]	Digital PLL_0 loop bandwidth scaling factor (unit of 0.1 Hz)	Digital PLL_0 loop bandwidth scaling factor, Bits[7:0]. Default: 0x00. Operation with the digital PLL_0 loop bandwidth scaling factor set to zero is undefined.
0x044F	[7:0]		Digital PLL_0 loop bandwidth scaling factor, Bits[15:8]. Default: 0x00. The default for Register 0x044E to Register 0x0450 = 0x000000. The loop bandwidth must always be less than the DPLL phase detector frequency divided by 20. The DPLL may not lock reliably if the DPLL loop bandwidth is <50 Hz and a crystal is used for the system clock. See the Choosing the SYSCLK Source section for details.
0x0450	[7:2]	Reserved	Default: 0x00.
	1	Base loop filter selection	0 = base loop filter with normal (70°) phase margin (default). 1 = base loop filter with high phase margin. (For loop bandwidths ≤2 kHz, there is ≤0.1 dB peaking in the closed-loop transfer function. Setting this bit is also recommended for loop bandwidths >2 kHz.)
	0	Digital PLL_0 loop BW scaling factor (unit of 0.1 Hz)	Digital PLL loop bandwidth scaling factor, Bit 16. Default: 0b.

Table 82. DPLL_0 REFB Integer Part of Feedback (N0) Divider

Address	Bits	Bit Name	Description
0x0451	[7:0]	Digital PLL_0 feedback divider—Integer Part N0	Digital PLL_0 integer feedback divider (minus 1), Bits[7:0]. Default: 0x00.
0x0452	[7:0]		Digital PLL_0 integer feedback divider, Bits[15:8]. Default: 0x00.
0x0453	[7:2]	Reserved	Default: 0x00.
	[1:0]	Digital PLL_0 feedback divider—Integer Part N0	Digital PLL_0 integer feedback divider, Bits[17:16]. Default: 00.

Table 83. DPLL_0 REFB Fractional Part of Fractional Feedback Divider—FRAC0

Address	Bits	Bit Name	Description
0x0454	[7:0]	Digital PLL_0 fractional feedback divider—FRAC0	The numerator of the fractional-N feedback divider, Bits[7:0]. Default: 0x00.
0x0455	[7:0]		The numerator of the fractional-N feedback divider, Bits[15:8]. Default: 0x00.
0x0456	[7:0]		The numerator of the fractional-N feedback divider, Bits[23:16]. Default: 0x00.

Table 84. DPLL_0 REFB Modulus of Fractional Feedback Divider—MOD0

Address	Bits	Bit Name	Description
0x0457	[7:0]	Digital PLL_0 feedback divider modulus—MOD0	The denominator of the fractional-N feedback divider, Bits[7:0]. Default: 0x00.
0x0458	[7:0]		The denominator of the fractional-N feedback divider, Bits[15:8]. Default: 0x00.
0x0459	[7:0]		The denominator of the fractional-N feedback divider, Bits[23:16]. Default: 0x00.

DPLL_0 SETTINGS FOR REFERENCE INPUT C (REFC) (REGISTER 0x045A TO REGISTER 0x0466)

Table 85. DPLL_0 REFC Priority Setting

Address	Bits	Bit Name	Description
0x045A	[7:3]	Reserved	Default: 00000b.
	[2:1]	REFC priority	These bits set the priority level (0 to 3) of REFC relative to the other input references. 00 (default) = 0 (highest). 01 = 1. 10 = 2. 11 = 3.
	0	Enable REFC	This bit enables DPLL_0 to lock to REFC. 0 (default) = REFC is not enabled for use by DPLL_0. 1 = REFC is enabled for use by DPLL_0.

Table 86. DPLL_0 REFC Loop Bandwidth Scaling Factor

Address	Bits	Bit Name	Description
0x045B	[7:0]	Digital PLL_0 loop bandwidth scaling factor (unit of 0.1 Hz)	Digital PLL_0 loop bandwidth scaling factor, Bits[7:0]. Default: 0x00.
0x045C	[7:0]		Digital PLL_0 loop bandwidth scaling factor, Bits[15:8]. Default: 0x00. The default for Register 0x045B to Register 0x045D = 0x000000. The loop bandwidth must always be less than the DPLL phase detector frequency divided by 20. The DPLL may not lock reliably if the DPLL loop bandwidth is <50 Hz and a crystal is used for the system clock. See the Choosing the SYSCLK Source section for details.
0x045D	[7:2]	Reserved	Default: 0x00.
	1	Base loop filter selection	0 = base loop filter with normal (70°) phase margin (default). 1 = base loop filter with high phase margin. For loop bandwidth ≤2 kHz, there is ≤0.1 dB peaking in the closed-loop transfer function. Setting this bit is also recommended for loop bandwidths >2 kHz.)
	0	Digital PLL_0 loop BW scaling factor (unit of 0.1 Hz)	Digital PLL_0 loop bandwidth scaling factor, Bit 16 (default: 0b).

Table 87. DPLL_0 REFC Integer Part of Feedback (N0) Divider

Address	Bits	Bit Name	Description
0x045E	[7:0]	Digital PLL_0 feedback divider—Integer Part N0	Digital PLL_0 integer feedback divider (minus 1), Bits[7:0]. Default: 0x00.
0x045F	[7:0]		Digital PLL_0 integer feedback divider, Bits[15:8]. Default: 0x00.
0x0460	[7:2]	Reserved	Default: 0x00.
	[1:0]	Digital PLL_0 feedback divider—Integer Part N0	Digital PLL_0 integer feedback divider, Bits[17:16]. Default: 00b. The default for Register 0x045E to Register 0x460: 0x000000.

Table 88. DPLL_0 REFC Fractional Part of Fractional Feedback Divider—FRAC0

Address	Bits	Bit Name	Description
0x0461	[7:0]	Digital PLL_0 fractional feedback divider—FRAC0	The numerator of the fractional-N feedback divider, Bits[7:0]. Default: 0x00.
0x0462	[7:0]		The numerator of the fractional-N feedback divider, Bits[15:8]. Default: 0x00.
0x0463	[7:0]		The numerator of the fractional-N feedback divider, Bits[23:16]. Default: 0x00.

Table 89. DPLL_0 REFC Modulus of Fractional Feedback Divider—MOD0

Address	Bits	Bit Name	Description
0x0464	[7:0]	Digital PLL_0 feedback divider modulus—MOD0	The denominator of the fractional-N feedback divider, Bits[7:0]. Default: 0x00.
0x0465	[7:0]		The denominator of the fractional-N feedback divider, Bits[15:8]. Default: 0x00.
0x0466	[7:0]		The denominator of the fractional-N feedback divider, Bits[23:16]. Default: 0x00.

DPLL_0 SETTINGS FOR REFERENCE INPUT D (REFD) (REGISTER 0x0467 TO REGISTER 0x0473)

Table 90. DPLL_0 REFD Priority Setting

Address	Bits	Bit Name	Description
0x0467	[7:3]	Reserved	Default: 00000b.
	[2:1]	REFD priority	These bits set the priority level (0 to 3) of REFD relative to the other input references. 00 (default) = 0 (highest). 01 = 1. 10 = 2. 11 = 3.
	0	Enable REFD	This bit enables DPLL_0 to lock to REFD. 0 (default) = REFD is not enabled for use by DPLL_0. 1 = REFD is enabled for use by DPLL_0.

Table 91. DPLL_0 REFD Loop Bandwidth Scaling Factor

Address	Bits	Bit Name	Description
0x0468	[7:0]	Digital PLL_0 loop bandwidth scaling factor (unit of 0.1 Hz)	Digital PLL_0 loop bandwidth scaling factor, Bits[7:0]. Default: 0x00.
0x0469	[7:0]		Digital PLL_0 loop bandwidth scaling factor, Bits[15:8]. Default: 0x00. The loop bandwidth must always be less than the DPLL phase detector frequency divided by 20. The DPLL may not lock reliably if the DPLL loop bandwidth is <50 Hz and a crystal is used for the system clock. See the Choosing the SYSCLK Source section for details.
0x046A	[7:2]	Reserved	Default: 0x00.
	1	Base loop filter selection	0 = base loop filter with normal (70°) phase margin (default). 1 = base loop filter with high phase margin. For loop bandwidths ≤2 kHz, there is ≤0.1 dB peaking in the closed-loop transfer function. Setting this bit is also recommended for loop bandwidths >2 kHz.
	0	Digital PLL_0 loop BW scaling factor (unit of 0.1 Hz)	Digital PLL loop bandwidth scaling factor, Bit 16. Default: 0b.

Table 92. DPLL_0 REFD Integer Part of Feedback (N0) Divider

Address	Bits	Bit Name	Description
0x046B	[7:0]	Digital PLL_0 feedback divider—Integer Part N0	Digital PLL_0 integer feedback divider (minus 1), Bits[7:0]. Default: 0x00.
0x046C	[7:0]		Digital PLL_0 integer feedback divider, Bits[15:8]. Default: 0x00.
0x046D	[7:2]	Reserved	Default: 0x00.
	[1:0]	Digital PLL_0 feedback divider—Integer Part N0	Digital PLL_0 integer feedback divider, Bits[17:16]. Default: 00b.

Table 93. DPLL_0 REFD Fractional Part of Fractional Feedback Divider—FRAC0

Address	Bits	Bit Name	Description
0x046E	[7:0]	Digital PLL_0 fractional feedback divider—FRAC0	The numerator of the fractional-N feedback divider, Bits[7:0]. Default: 0x00.
0x046F	[7:0]		The numerator of the fractional-N feedback divider, Bits[15:8]. Default: 0x00.
0x0470	[7:0]		The numerator of the fractional-N feedback divider, Bits[23:16]. Default: 0x00.

Table 94. DPLL_0 REFD Modulus of Fractional Feedback Divider—MOD0

Address	Bits	Bit Name	Description
0x0471	[7:0]	Digital PLL_0 feedback divider modulus—MOD0	The denominator of the fractional-N feedback divider, Bits[7:0]. Default: 0x00.
0x0472	[7:0]		The denominator of the fractional-N feedback divider, Bits[15:8]. Default: 0x00.
0x0473	[7:0]		The denominator of the fractional-N feedback divider, Bits[23:16]. Default: 0x00.

DPLL_1 CONTROLS (REGISTER 0x0500 TO REGISTER 0x051E)

These registers mimic the DPLL_0 general settings registers (Register 0x0400 through Register 0x041E) but the register addresses are offset by 0x0100. All default values are identical.

APLL_1 CONFIGURATION (REGISTER 0x0530 TO REGISTER 0x0533)

These registers mimic the APLL_0 configuration registers (Register 0x0430 through Register 0x0433) but the register addresses are offset by 0x0100. All default values are identical.

PLL_1 OUTPUT SYNC AND CLOCK DISTRIBUTION (REGISTER 0x0534 TO REGISTER 0x053E)

These registers mimic the PLL_0 output SYNC and clock distribution registers (Register 0x0434 through Register 0x043E) but the register addresses are offset by 0x0100. All default values are identical.

DPLL_1 SETTINGS FOR REFERENCE INPUT A (REFA) (REGISTER 0x0540 TO REGISTER 0x054C)

These registers mimic the DPLL_0 settings for the Reference Input A (REFA) registers (Register 0x0440 through Register 0x044C) but the register addresses are offset by 0x0100. All default values are identical.

DPLL_1 SETTINGS FOR REFERENCE INPUT B (REFB) (REGISTER 0x054D TO REGISTER 0x0559)

These registers mimic the DPLL_0 settings for the Reference Input B (REFB) registers (Register 0x044D through Register 0x0459) but the register addresses are offset by 0x0100. All default values are identical.

DPLL_1 SETTINGS FOR REFERENCE INPUT C (REFC) (REGISTER 0x055A TO REGISTER 0x0566)

These registers mimic the DPLL_0 settings for the Reference Input C (REFC) registers (Register 0x045A through Register 0x0466) but the register addresses are offset by 0x0100. All default values are identical.

DPLL_1 SETTINGS FOR REFERENCE INPUT D (REFD) (REGISTER 0x0567 TO REGISTER 0x0573)

These registers mimic the DPLL_0 settings for the Reference Input D (REFD) registers (Register 0x0467 through Register 0x0473) but the register addresses are offset by 0x0100. All default values are identical.

DPLL_2 CONTROLS (REGISTER 0x0600 TO REGISTER 0x061E)

These registers mimic the DPLL_0 controls registers (Register 0x0400 through Register 0x041E) but the register addresses are offset by 0x0200. All default values are identical.

APLL_2 CONFIGURATION (REGISTER 0x0630 TO REGISTER 0x0633)

These registers mimic the APLL_0 configuration registers (Register 0x0430 through Register 0x0433) but the register addresses are offset by 0x0200. All default values are identical.

PLL_2 OUTPUT SYNC AND CLOCK DISTRIBUTION (REGISTER 0x0634 TO REGISTER 0x063E)

These registers mimic the PLL_0 output SYNC and clock distribution registers (Register 0x0434 through Register 0x043E) but the register addresses are offset by 0x0200. All default values are identical.

DPLL_2 SETTINGS FOR REFERENCE INPUT A (REFA) (REGISTER 0x0640 TO REGISTER 0x064C)

These registers mimic the DPLL_0 settings for the Reference Input A (REFA) registers (Register 0x0440 through Register 0x044C) but the register addresses are offset by 0x0200. All default values are identical.

DPLL_2 SETTINGS FOR REFERENCE INPUT B (REFB) (REGISTER 0x064D TO REGISTER 0x0659)

These registers mimic the DPLL_0 settings for the Reference Input B (REFB) registers (Register 0x044D through Register 0x0459) but the register addresses are offset by 0x0200. All default values are identical.

DPLL_2 SETTINGS FOR REFERENCE INPUT C (REFC) (REGISTER 0x065A TO REGISTER 0x0666)

These registers mimic the DPLL_0 settings for the Reference Input C (REFC) registers (Register 0x045A through Register 0x0466) but the register addresses are offset by 0x0200. All default values are identical.

DPLL_2 SETTINGS FOR REFERENCE INPUT D (REFD) (REGISTER 0x0667 TO REGISTER 0x0673)

These registers mimic the DPLL_0 settings for the Reference Input D (REFD) registers (Register 0x0467 through Register 0x0473) but the register addresses are offset by 0x0200. All default values are identical.

DPLL_3 CONTROLS (REGISTER 0x0700 TO REGISTER 0x071E)

These registers mimic the DPLL_0 controls registers (Register 0x0400 through Register 0x041E) but the register addresses are offset by 0x0300. All default values are identical.

APLL_3 CONFIGURATION (REGISTER 0x0730 TO REGISTER 0x0733)

These registers mimic the APLL_0 configuration registers (Register 0x0430 through Register 0x0433) but the register addresses are offset by 0x0300. All default values are identical.

PLL_3 OUTPUT SYNC AND CLOCK DISTRIBUTION (REGISTER 0x0734 TO REGISTER 0x073E)

These registers mimic the PLL_0 output SYNC and clock distribution registers (Register 0x0434 through Register 0x043E) but the register addresses are offset by 0x0300. All default values are identical.

DPLL_3 SETTINGS FOR REFERENCE INPUT A (REFA) (REGISTER 0x0740 TO REGISTER 0x074C)

These registers mimic the DPLL_0 settings for the Reference Input A (REFA) registers (Register 0x0440 through Register 0x044C) but the register addresses are offset by 0x0300. All default values are identical.

DPLL_3 SETTINGS FOR REFERENCE INPUT B (REFB) (REGISTER 0x074D TO REGISTER 0x0759)

These registers mimic the DPLL_0 settings for the Reference Input B (REFB) registers (Register 0x044D through Register 0x0459) but the register addresses are offset by 0x0300. All default values are identical.

DPLL_3 SETTINGS FOR REFERENCE INPUT C (REFC) (REGISTER 0x075A TO REGISTER 0x0766)

These registers mimic the DPLL_0 settings for the Reference Input C (REFC) registers (Register 0x045A through Register 0x0466) but the register addresses are offset by 0x0300. All default values are identical.

DPLL_3 SETTINGS FOR REFERENCE INPUT D (REFD) (REGISTER 0x0767 TO REGISTER 0x0773)

These registers mimic the DPLL_0 settings for the Reference Input D (REFD) registers (Register 0x0467 through Register 0x0473) but the register addresses are offset by 0x0300. All default values are identical.

DIGITAL LOOP FILTER COEFFICIENTS (REGISTER 0x0800 TO REGISTER 0x0817)

Note that the digital loop filter base coefficients (α, β, γ, and δ) have the general form: $x(2^y)$, where x is the linear component, and y is the exponential component of the coefficient. The value of the linear component (x) constitutes a fraction, where $0 \leq x \leq 1$. The exponential component (y) is a signed integer. These are live registers; therefore, an IO_UPDATE is not needed. However, the updated coefficients do not take effect while the loop is active.

Table 95. Base Digital Loop Filter with Normal Phase Margin (PM = 70°)

Address	Bits	Bit Name	Description
0x0800	[7:0]	NPM Alpha-0 linear	Alpha-0 coefficient linear, Bits[7:0]. Default: 0x24.
0x0801	[7:0]		Alpha-0 coefficient linear, Bits[15:8]. Default: 0x8C.
0x0802	7	Reserved	Default: 0b.
	[6:0]	NPM Alpha-1 exponent	Alpha-1 coefficient exponent, Bits[6:0]. Default: 0x49.
0x0803	[7:0]	NPM Beta-0 linear	Beta-0 coefficient linear, Bits[7:0]. Default: 0x55.
0x0804	[7:0]		Beta-0 coefficient linear, Bits[15:8]. Default: 0xC9.
0x0805	7	Reserved	Default: 0b.
	[6:0]	NPM Beta-1 exponent	Beta-1 coefficient exponent, Bits[6:0]. Default: 0x7B.
0x0806	[7:0]	NPM Gamma-0 linear	Gamma-0 coefficient linear, Bits[7:0]. Default: 0x9C.
0x0807	[7:0]		Gamma-0 coefficient linear, Bits[15:8]. Default: 0xFA.
0x0808	7	Reserved	Default: 0b.
	[6:0]	NPM Gamma -1 exponent	Gamma-1 coefficient exponent, Bits[6:0]. Default: 0x55.
0x0809	[7:0]	NPM Delta-0 linear	Delta-0 coefficient linear, Bits[7:0]. Default: 0xEA.
0x080A	[7:0]		Delta-0 coefficient linear, Bits[15:8]. Default: 0xE2.
0x080B	7	Reserved	Default: 0b.
	[6:0]	NPM Delta-1 exponent	Delta-1 coefficient exponent, Bits[6:0]. Default: 0x57.

Note that the base digital loop filter coefficients (α, β, γ, and δ) have the general form: $x(2_y)$, where x is the linear component, and y is the exponential component of the coefficient. The value of the linear component (x) constitutes a fraction, where $0 \leq x \leq 1$. The exponential component (y) is a signed integer. These are live registers; therefore, an IO_UPDATE is not needed. However, the updated coefficients do not take effect while the loop is active.

Table 96. Base Digital Loop Filter with High Phase Margin (PM = 88.5°)

Address	Bits	Bit Name	Description
0x080C	[7:0]	HPM Alpha-0 linear	Alpha-0 coefficient linear, Bits[7:0]. Default = 0x8C.
0x080D	[7:0]		Alpha-0 coefficient linear, Bits[15:8]. Default: 0xAD.
0x080E	7	Reserved	Default: 0b.
	[6:0]	HPM Alpha-1 exponent	Alpha-1 coefficient exponent, Bits[6:0]. Default: 0x4C.
0x080F	[7:0]	HPM Beta-0 linear	Beta-0 coefficient linear, Bits[7:0]. Default: 0xF5.
0x0810	[7:0]		Beta-0 coefficient linear, Bits[15:8]. Default: 0xCB.
0x0811	7	Reserved	Default: 0b.
	[6:0]	HPM Beta-1 exponent	Beta-1 coefficient exponent, Bits[6:0]. Default: 0x73.
0x0812	[7:0]	HPM Gamma-0 linear	Gamma-0 coefficient linear, Bits[7:0]. Default: 0x24.
0x0813	[7:0]		Gamma-0 coefficient linear, Bits[15:8]. Default: 0xD8.
0x0814	7	Reserved	Default: 0b.
	[6:0]	HPM Gamma-1 exponent	Gamma-1 coefficient exponent, Bits[6:0]. Default: 0x59.
0x0815	[7:0]	HPM Delta-0 linear	Delta-0 coefficient linear, Bits[7:0]. Default: 0xD2.
0x0816	[7:0]		Delta-0 coefficient linear, Bits[15:8]. Default: 0x8D.
0x0817	7	Reserved	Default: 0b.
	[6:0]	HPM Delta-1 exponent	Delta-1 coefficient exponent, Bits[6:0]. Default: 0x5A.

Table 97. Global Demapping Control

Address	Bits	Bit Name	Description
0x0900	[7:1]	Reserved	Reserved, Bits[7:1]. Default = 0x00.
	0	Demap control IO_UPDATE	Demap control IO_UPDATE, Bit 0. Default = 0b.
0x0901	[7:0]	DPLL_0 sampled address, Bits[15:0]	DPLL_0 sampled address, Bits[7:0]. Default = 0x00.
0x0902	[7:0]		DPLL_0 sampled address, Bits[15:8]. Default: 0x00.
0x0903	[7:0]	DPLL_1 sampled address, Bits[15:0]	DPLL_1 sampled address, Bits[7:0]. Default = 0x00.
0x0904	[7:0]		DPLL_1 sampled address, Bits[15:8]. Default: 0x00.
0x0905	[7:0]	DPLL_2 sampled address, Bits[15:0]	DPLL_2 sampled address, Bits[7:0]. Default = 0x00.
0x0906	[7:0]		DPLL_2 sampled address, Bits[15:8]. Default: 0x00
0x0907	[7:0]	DPLL_3 sampled address, Bits[15:0]	DPLL_3 sampled address, Bits[7:0]. Default = 0x00.
0x0908	[7:0]		DPLL_3 sampled address, Bits[15:8]. Default: 0x00.
0x0909	[7:1]	Reserved	Reserved, Bits[7:1]. Default = 0x00.
	0	Demap control IO_UPDATE	Demap control IO_UPDATE, Bit 0. Default = 0b.

COMMON OPERATIONAL CONTROLS (REGISTER 0x0A00 TO REGISTER 0x0A0E)

Table 98. Global Operational Controls

Address	Bits	Bit Name	Description
0x0A00	[7:4]	Reserved	Default: 0x0.
	3	Soft sync all	Setting this bit initiates synchronization of all clock distribution outputs (default = 0b). Nonmasked outputs stall when value is 1; restart is initialized on a 1-to-0 transition. Note that like all buffered registers, an IO_UPDATE (0x000F = 0x01) is needed every time there is a change for this bit to take effect.
	2	Calibrate SYSCLK	A 0-to-1 transition of this bit (followed by an IO_UPDATE) calibrates the SYSCLK PLL. Default: 0b.
	1	Calibrate all	A 0-to-1 transition of this bit (followed by an IO_UPDATE) calibrates the system clock PLL, as well as all four output PLLs (APLL_0, APLL_1, APLL_2, APLL_3). Default: 0b. Note that like all buffered registers, an IO_UPDATE (0x000F = 0x01) is needed every time there is a change for this bit to take effect. This bit is not self clearing; however, it is strongly recommended to clear this bit after using it. If this bit is set, calibration of the individual APLLs (APLL_0, APLL_1, APLL_2, and APLL_3) in Register 0xA20, Register 0xA40, Register 0xA60, and Register 0xA80 is masked and APLL calibration does not occur.
	0	Power-down all	Places the entire device in deep sleep mode. Default: device is not powered down.

Table 99. Power Down of Reference Inputs

Address	Bits	Bit Name	Description
0x0A01	[7:4]	Reserved	Default: 0x0
	3	REFD power-down	Powers down REFD input receiver 0 (default) = not powered down 1 = powered down
	2	REFC power-down	Powers down REFC input receiver 0 (default) = not powered down 1 = powered down
	1	REFB power-down	Powers down REFB input receiver 0 (default) = not powered down 1 = powered down
	0	REFA power-down	Powers down REFA input receiver 0 (default) = not powered down 1 = powered down

Table 100. Reference Input Validation Timeout

Address	Bits	Bit Name	Description
0x0A02	[7:4]	Reserved	Default: 0x0.
	3	REFD timeout	If REFD is unfaulted, setting this autoclearing bit forces the reference validation timer for REFD to zero, thus making it valid immediately. Default = 0b.
	2	REFC timeout	If REFC is unfaulted, setting this autoclearing bit forces the reference validation timer for REFC to zero, thus making it valid immediately. Default = 0b.
	1	REFB timeout	If REFB is unfaulted, setting this autoclearing bit forces the reference validation timer for REFB to zero, thus making it valid immediately. Default = 0b.
	0	REFA timeout	If REFA is unfaulted, setting this autoclearing bit forces the reference validation timer for REFA to zero, thus making it valid immediately. Default = 0b.

Table 101. Force Reference Input Fault

Address	Bits	Bit Name	Description
0x0A03	[7:4]	Reserved	Default: 0x0
	3	REFD fault	Faults REFD input receiver 0 (default) = not faulted 1 = faulted (REFD is not used)
	2	REFC fault	Faults REFC input receiver 0 (default) = not faulted 1 = faulted (REFC is not used)
	1	REFB fault	Faults REFB input receiver 0 (default) = not faulted 1 = faulted (REFB is not used)
	0	REFA fault	Faults REFA input receiver 0 (default) = not faulted 1 = faulted (REFA is not used)

Table 102. Reference Input Monitor Bypass

Address	Bits	Bit Name	Description
0x0A04	[7:4]	Reserved	Default: 0x0
	3	REFD monitor bypass	Bypasses REFD input receiver frequency monitor; setting this bit to 1 forces REFD to be unfaulted as long as the REFD fault bit in Register 0x0A03 is not set. 0 (default) = REFD frequency monitor not bypassed. 1 = REFD frequency monitor bypassed.
	2	REFC monitor bypass	Bypasses REFC input receiver frequency monitor; setting this bit to 1 forces REFC to be unfaulted as long as the REFC fault bit in Register 0x0A03 is not set. 0 (default) = REFC frequency monitor not bypassed. 1 = REFC frequency monitor bypassed.
	1	REFB monitor bypass	Bypasses REFB input receiver frequency monitor; setting this bit to 1 forces REFB to be unfaulted as long as the REFB fault bit in Register 0x0A03 is not set. 0 (default) = REFB frequency monitor not bypassed. 1 = REFBB frequency monitor bypassed.
	0	REFA monitor bypass	Bypasses REFA input receiver frequency monitor; setting this bit to 1 forces REFA to be unfaulted as long as the REFA fault bit in Register 0x0A03 is not set. 0 (default) = REFA frequency monitor not bypassed. 1 = REFA frequency monitor bypassed.

IRQ CLEARING (REGISTER 0x0A05 TO REGISTER 0x0A14)

The IRQ clearing registers are identical in format to the IRQ monitor registers (Register 0x0D08 to Register 0x0A14). When set to Logic 1, an IRQ clearing bit resets the corresponding IRQ monitor bit, thereby cancelling the interrupt request for the indicated event. The IRQ clearing registers are autoclearing.

Table 103. Clear IRQ Groups

Address	Bits	Bit Name	Description
0x0A05	7	Clear watchdog timer	Clears watchdog timer alert
	6	Reserved	Reserved
	5	Clear DPLL_3 IRQs	Clears all IRQs associated with DPLL_3
	4	Clear DPLL_2 IRQs	Clears all IRQs associated with DPLL_2
	3	Clear DPLL_1 IRQs	Clears all IRQs associated with DPLL_1
	2	Clear DPLL_0 IRQs	Clears all IRQs associated with DPLL_0
	1	Clear common IRQs	Clears all IRQs associated with common IRQ group
	0	Clear all IRQs	Clears all IRQs

Table 104. IRQ Clearing for SYSCLK and EEPROM

Address	Bits	Bit Name	Description
0x0A06	7	SYSCLK unlocked	Clears IRQ indicating a SYSCLK PLL state transition from locked to unlocked
	6	SYSCLK stable	Clears IRQ indicating that SYSCLK stability time has expired and that the SYSCLK PLL is considered to be stable
	5	SYSCLK locked	Clears IRQ indicating a SYSCLK PLL state transition from unlocked to locked
	4	SYSCLK cal ended	Clears IRQ indicating a SYSCLK PLL calibration has ended
	3	SYSCLK cal started	Clears IRQ indicating a SYSCLK PLL calibration has started
	2	Watchdog timer	Clears IRQ indicating expiration of the watchdog timer
	1	EEPROM fault	Clears IRQ indicating a fault during an EEPROM upload or download operation
	0	EEPROM complete	Clears IRQ indicating successful completion of an EEPROM upload or download operation

Table 105. IRQ Clearing for Reference Inputs

Address	Bits	Bit Name	Description
0x0A07	7	Reserved	Reserved
	6	REFB validated	Clears IRQ indicating that REFB has been validated
	5	REFB fault cleared	Clears IRQ indicating that REFB has been cleared of a previous fault
	4	REFB fault	Clears IRQ indicating that REFB has been faulted
	3	Reserved	Reserved
	2	REFA validated	Clears IRQ indicating that REFA has been validated
	1	REFA fault cleared	Clears IRQ indicating that REFA has been cleared of a previous fault
	0	REFA fault	Clears IRQ indicating that REFA has been faulted
0x0A08	7	Reserved	Reserved
	6	REFD validated	Clears IRQ indicating that REFD has been validated
	5	REFD fault cleared	Clears IRQ indicating that REFD has been cleared of a previous fault
	4	REFD fault	Clears IRQ indicating that REFD has been faulted
	3	Reserved	Reserved
	2	REFC validated	Clears IRQ indicating that REFC has been validated
	1	REFC fault cleared	Clears IRQ indicating that REFC has been cleared of a previous fault
	0	REFC fault	Clears IRQ indicating that REFC has been faulted

Table 106. IRQ Clearing for Digital PLL0 (DPLL_0)

Address	Bits	Bit Name	Description
0x0A09	7	Frequency unclamped	Clears IRQ indicating that DPLL_0 has exited a frequency unclamped state
	6	Frequency clamped	Clears IRQ indicating that DPLL_0 has entered a frequency clamped state
	5	Phase slew unlimited	Clears IRQ indicating that DPLL_0 has exited a phase slew limited state
	4	Phase slew limited	Clears IRQ indicating that DPLL_0 has entered a phase slew limited state
	3	Frequency unlocked	Clears IRQ indicating that DPLL_0 has lost frequency lock
	2	Frequency locked	Clears IRQ indicating that DPLL_0 has acquired frequency lock
	1	Phase unlocked	Clears IRQ indicating that DPLL_0 has lost phase lock
	0	Phase locked	Clears IRQ indicating that DPLL_0 has acquired phase lock
0x0A0A	7	DPLL_0 switching	Clears IRQ indicating that DPLL_0 is switching to a new reference
	6	DPLL_0 free run	Clears IRQ indicating that DPLL_0 has entered free run mode
	5	DPLL_0 holdover	Clears IRQ indicating that DPLL_0 has entered holdover mode
	4	History updated	Clears IRQ indicating that DPLL_0 has updated its tuning word history
	3	REFD activated	Clears IRQ indicating that DPLL_0 has activated REFD
	2	REFC activated	Clears IRQ indicating that DPLL_0 has activated REFC
	1	REFB activated	Clears IRQ indicating that DPLL_0 has activated REFB
	0	REFA activated	Clears IRQ indicating that DPLL_0 has activated REFA
0x0A0B	7	Phase step detected	Clears IRQ indicating that DPLL_0 has detected a large phase step at its input
	6	Demap control unclamped	Clears IRQ indicating that the DPLL_0 demapping controller has an unclamped state
	5	Demap control clamped	Clears IRQ indicating that the DPLL_0 demapping controller has a clamped state
	4	Clock dist sync'd	Clears IRQ indicating a distribution sync event
	3	APLL_0 unlocked	Clears IRQ indicating that APLL_0 has been unlocked
	2	APLL_0 locked	Clears IRQ indicating that APLL_0 has been locked
	1	APLL_0 cal ended	Clears IRQ indicating that APLL_0 calibration complete
	0	APLL_0 cal started	Clears IRQ indicating that APLL_0 calibration started

Table 107. IRQ Clearing for Digital PLL1 (DPLL_1)

Address	Bits	Bit Name	Description
0x0A0C	7	Frequency unclamped	Clears IRQ indicating that DPLL_1 has exited a frequency unclamped state
	6	Frequency clamped	Clears IRQ indicating that DPLL_1 has entered a frequency clamped state
	5	Phase slew unlimited	Clears IRQ indicating that DPLL_1 has exited a phase slew limited state
	4	Phase slew limited	Clears IRQ indicating that DPLL_1 has entered a phase slew limited state
	3	Frequency unlocked	Clears IRQ indicating that DPLL_1 has lost frequency lock
	2	Frequency locked	Clears IRQ indicating that DPLL_1 has acquired frequency lock
	1	Phase unlocked	Clears IRQ indicating that DPLL_1 has lost phase lock
	0	Phase locked	Clears IRQ indicating that DPLL_1 has acquired phase lock
0x0A0D	7	DPLL_1 switching	Clears IRQ indicating that DPLL_1 is switching to a new reference
	6	DPLL_1 free run	Clears IRQ indicating that DPLL_1 has entered free run mode
	5	DPLL_1 holdover	Clears IRQ indicating that DPLL_1 has entered holdover mode
	4	History updated	Clears IRQ indicating that DPLL_1 has updated its tuning word history
	3	REFD activated	Clears IRQ indicating that DPLL_1 has activated REFD
	2	REFC activated	Clears IRQ indicating that DPLL_1 has activated REFC
	1	REFB activated	Clears IRQ indicating that DPLL_1 has activated REFB
	0	REFA activated	Clears IRQ indicating that DPLL_1 has activated REFA

Address	Bits	Bit Name	Description
0x0A0E	7	Phase step detected	Clears IRQ indicating that DPLL_1 has detected a large phase step at its input
	6	Demap control unclamped	Clears IRQ indicating that the DPLL_1 demapping controller has an unclamped state
	5	Demap control clamped	Clears IRQ indicating that the DPLL_1 demapping controller has a clamped state
	4	Clock dist sync'd	Clears IRQ indicating a distribution sync event
	3	APLL_1 unlocked	Clears IRQ indicating that APLL_1 has been unlocked
	2	APLL_1 locked	Clears IRQ indicating that APLL_1 has been locked
	1	APLL_1 cal ended	Clears IRQ indicating that APLL_1 calibration complete
	0	APLL_1 cal started	Clears IRQ indicating that APLL_1 calibration started

Table 108. IRQ Clearing for Digital PLL2 (DPLL_2)

Address	Bits	Bit Name	Description
0x0A0F	7	Frequency unclamped	Clears IRQ indicating that DPLL_2 has exited a frequency unclamped state
	6	Frequency clamped	Clears IRQ indicating that DPLL_2 has entered a frequency clamped state
	5	Phase slew unlimited	Clears IRQ indicating that DPLL_2 has exited a phase slew limited state
	4	Phase slew limited	Clears IRQ indicating that DPLL_2 has entered a phase slew limited state
	3	Frequency unlocked	Clears IRQ indicating that DPLL_2 has lost frequency lock
	2	Frequency locked	Clears IRQ indicating that DPLL_2 has acquired frequency lock
	1	Phase unlocked	Clears IRQ indicating that DPLL_2 has lost phase lock
	0	Phase locked	Clears IRQ indicating that DPLL_2 has acquired phase lock
0x0A10	7	DPLL_2 switching	Clears IRQ indicating that DPLL_2 is switching to a new reference
	6	DPLL_2 free run	Clears IRQ indicating that DPLL_2 has entered free run mode
	5	DPLL_2 holdover	Clears IRQ indicating that DPLL_2 has entered holdover mode
	4	History updated	Clears IRQ indicating that DPLL_2 has updated its tuning word history
	3	REFD activated	Clears IRQ indicating that DPLL_2 has activated REFD
	2	REFC activated	Clears IRQ indicating that DPLL_2 has activated REFC
	1	REFB activated	Clears IRQ indicating that DPLL_2 has activated REFB
	0	REFA activated	Clears IRQ indicating that DPLL_2 has activated REFA
0x0A11	7	Phase step detected	Clears IRQ indicating that DPLL_2 has detected a large phase step at its input
	6	Demap control unclamped	Clears IRQ indicating that the DPLL_2 demapping controller is unclamped
	5	Demap control clamped	Clears IRQ indicating that the DPLL_2 demapping controller is clamped
	4	Clock dist sync'd	Clears IRQ indicating a distribution sync event
	3	APLL_2 unlocked	Clears IRQ indicating that APLL_2 has been unlocked
	2	APLL_2 locked	Clears IRQ indicating that APLL_2 has been locked
	1	APLL_2 cal ended	Clears IRQ indicating that APLL_2 calibration complete
	0	APLL_2 cal started	Clears IRQ indicating that APLL_2 calibration started

Table 109. IRQ Clearing for Digital PLL3 (DPLL_3)

Address	Bits	Bit Name	Description
0x0A12	7	Frequency unclamped	Clears IRQ indicating that DPLL_3 has exited a frequency unclamped state
	6	Frequency clamped	Clears IRQ indicating that DPLL_3 has entered a frequency clamped state
	5	Phase slew unlimited	Clears IRQ indicating that DPLL_3 has exited a phase slew limited state
	4	Phase slew limited	Clears IRQ indicating that DPLL_3 has entered a phase slew limited state
	3	Frequency unlocked	Clears IRQ indicating that DPLL_3 has lost frequency lock
	2	Frequency locked	Clears IRQ indicating that DPLL_3 has acquired frequency lock
	1	Phase unlocked	Clears IRQ indicating that DPLL_3 has lost phase lock
	0	Phase locked	Clears IRQ indicating that DPLL_3 has acquired phase lock
0x0A13	7	DPLL_3 switching	Clears IRQ indicating that DPLL_3 is switching to a new reference
	6	DPLL_3 free run	Clears IRQ indicating that DPLL_3 has entered free run mode
	5	DPLL_3 holdover	Clears IRQ indicating that DPLL_3 has entered holdover mode
	4	History updated	Clears IRQ indicating that DPLL_3 has updated its tuning word history
	3	REFD activated	Clears IRQ indicating that DPLL_3 has activated REFD
	2	REFC activated	Clears IRQ indicating that DPLL_3 has activated REFC
	1	REFB activated	Clears IRQ indicating that DPLL_3 has activated REFB
	0	REFA activated	Clears IRQ indicating that DPLL_3 has activated REFA
0x0A14	7	Phase step detected	Clears IRQ indicating that DPLL_3 has detected a large phase step at its input
	6	Demap control unclamped	Clears IRQ indicating that the DPLL_3 demapping controller is unclamped
	5	Demap control clamped	Clears IRQ indicating that the DPLL_3 demapping controller is clamped
	4	Clock dist sync'd	Clears IRQ indicating a distribution sync event
	3	APLL_3 unlocked	Clears IRQ indicating that APLL_3 has been unlocked
	2	APLL_3 locked	Clears IRQ indicating that APLL_3 has been locked
	1	APLL_3 cal ended	Clears IRQ indicating that APLL_3 calibration complete
	0	APLL_3 cal started	Clears IRQ indicating that APLL_3 calibration started

PLL_0 OPERATIONAL CONTROLS (REGISTER 0x0A20 TO REGISTER 0x0A24)

Table 110. PLL_0 Sync and Calibration

Address	Bits	Bit Name	Description
0x0A20	[7:3]	Reserved	Default: 0x0.
	2	APLL_0 soft sync	Setting this bit initiates synchronization of the clock distribution output. 0 (default) = normal operation. 1 = nonmasked PLL_0 outputs stall; restart initialized on a 1-to-0 transition.
	1	APLL_0 calibrate (not self-clearing)	1 = initiates VCO calibration (calibration occurs on the IO_UPDATE following a 0-to-1 transition of this bit.) This bit is not autoclearing. 0 (default) = does nothing.
	0	PLL_0 power-down	Places DPLL_0, APLL_0, and PLL_0 clock in deep sleep mode. 0 (default) = normal operation. 1 = powered down.

Table 111. PLL_0 Output

Address	Bits	Bit Name	Description
0x0A21	[7:4]	Reserved	Default 0x0
	3	OUT0B disable	Setting this bit puts the OUT0B driver into power-down. Default: 0b. Channel synchronization is maintained, but runt pulses may be generated.
	2	OUT0A disable	Setting this bit puts the OUT0A driver into power-down. Default: 0b. Channel synchronization is maintained, but runt pulses may be generated.
	1	OUT0B power-down	Setting this bit puts the OUT0B divider and driver into power-down. Default: 0b. This mode saves the most power, but runt pulses may be generated during exit.
	0	OUT0A power-down	Setting this bit puts the OUT0A divider and driver into power-down. Default: 0b. This mode saves the most power, but runt pulses may be generated during exit.

Table 112. PLL_0 User Mode

<table>
<tr><th>Address</th><th>Bits</th><th>Bit Name</th><th colspan="2">Description</th></tr>
<tr><td rowspan="16">0x0A22</td><td>7</td><td>Reserved</td><td colspan="2">Default: 0b.</td></tr>
<tr><td>[6:5]</td><td>DPLL_0 manual reference</td><td colspan="2">Input reference when user selection mode = 00, 01, 10, or 11.
00 (default) = Input Reference A.
01 = Input Reference B.
10 = Input Reference C.
11 = Input Reference D.</td></tr>
<tr><td rowspan="10">[4:2]</td><td rowspan="10">DPLL_0 switching mode</td><td colspan="2">Selects the operating mode of the reference switching state machine.</td></tr>
<tr><td>Reference Switchover Mode, Bits[2:0]</td><td>Reference Selection Mode</td></tr>
<tr><td>000b</td><td>Automatic revertive mode</td></tr>
<tr><td>001b</td><td>Automatic nonrevertive mode</td></tr>
<tr><td>010b</td><td>Manual reference select mode (with automatic fallback)</td></tr>
<tr><td>011b</td><td>Manual reference select mode (with holdover fallback)</td></tr>
<tr><td>100b</td><td>Manual reference select mode (without holdover fallback)</td></tr>
<tr><td>101b</td><td>Not used</td></tr>
<tr><td>110b</td><td>Not used</td></tr>
<tr><td>111b</td><td>Not used</td></tr>
<tr><td>1</td><td>DPLL_0 user holdover</td><td colspan="2">Forces DPLL_0 into holdover mode. Note that the AD9554 enters free run mode if this bit is set when there is no holdover history available.
0 (default) = normal operation.
1 = DPLL_0 is forced into holdover mode until this bit is cleared. Note that holdover mode is used if the holdover history is available. User free run mode is used if the holdover history is not available. See Register 0x0D22, Bit 0 for the DPLL_0 history available indication.</td></tr>
<tr><td>0</td><td>DPLL_0 user free run</td><td colspan="2">Forces DPLL_0 into free run mode.
0 (default) = normal operation.
1 = DPLL_0 is forced into free run mode until this bit is cleared.</td></tr>
</table>

Table 113. PLL_0 Reset

Address	Bits	Bit Name	Description
0x0A23	[7:3]	Reserved	Default: 00000b.
	2	Reset DPLL_0 loop filter	Resets the digital loop filter. 0 (default) = normal operation. 1 = DPLL_0 digital loop filter is reset. This is an autoclearing bit.
	1	Reset DPLL_0 TW history	Resets the tuning word history (part of holdover functionality). 0 (default) = normal operation. 1 = DPLL_0 tuning word history is reset. This is an autoclearing bit.
	0	Reset DPLL_0 autosync	Resets the automatic synchronization logic (see Register 0x0435). 0 (default) = normal operation. 1 = DPLL_0 automatic synchronization logic is reset. This is an autoclearing bit.

Table 114. PLL_0 Phase

Address	Bits	Bit Name	Description
0x0A24	[7:3]	Reserved	Default: 00000b.
	2	DPLL_0 reset phase offset	Resets the incremental phase offset to zero. This is an autoclearing bit.
	1	DPLL_0 decrement phase offset	Decrements the incremental phase offset by the amount specified in the incremental phase lock offset step size registers (Register 0x0412 and Register 0x0413). This is an autoclearing bit.
	0	DPLL_0 increment phase offset	Increments the incremental phase offset by the amount specified in the incremental phase lock offset step size registers (Register 0x0412 and Register 0x0413). This is an autoclearing bit.

PLL_1 OPERATIONAL CONTROLS (REGISTER 0x0A40 TO REGISTER 0x0A44)

These registers mimic the PLL_0 controls registers (Register 0x0A20 through Register 0x0A24) but the register addresses are offset by 0x0020. All default values are identical.

PLL_2 OPERATIONAL CONTROLS (REGISTER 0x0A60 TO REGISTER 0x0A64)

These registers mimic the PLL_0 controls registers (Register 0x0A20 through Register 0x0A24) but the register addresses are offset by 0x0040. All default values are identical.

PLL_3 OPERATIONAL CONTROLS (REGISTER 0x0A80 TO REGISTER 0x0A84)

These registers mimic the PLL_0 controls registers (Register 0x0A20 through Register 0x0A24) but the register addresses are offset by 0x0060. All default values are identical.

VOLTAGE REGULATOR (REGISTER 0x0B00 TO REGISTER 0x0B01)

The bits in these registers adjust the internal voltage regulator for 1.5 V input voltage operation.

Table 115. Voltage Regulator

Address	Bits	Bit Name	Description
0x0B00	[7:0]	VREG, Bits[7:0]	Adjusts internal voltage regulators for 1.5 V operation. There are only two valid settings for this register, and all bits in VREG[9:0] must be all 1s or all 0s, depending on whether the device is powered at 1.5 V or 1.8 V. 0x00 (default) = 1.8 V operation. 0xFF = 1.5 V operation.
0x0B01	[7:2]	Reserved	Default: 000000b.
	[1:0]	VREG, Bits[9:8]	Adjusts internal voltage regulators for 1.5 V operation. There are only two valid settings for this register. 00b (default): 1.8 V operation. 11b: 1.5 V operation.

STATUS READBACK (REGISTER 0x0D00 TO REGISTER 0x0D05)

All bits in Register 0x0D00 to Register 0x0D05 are read only. To report the latest status, these bits require an IO_UPDATE (Register 0x000F = 0x01) immediately before being read.

Table 116. EEPROM Status

Address	Bits	Bit Name	Description
0x0D00	[7:4]	Reserved	Default: 00000b.
	3	EEPROM CRC fault detected	An CRC error occurred during an EEPROM operation.
	2	EEPROM fault detected	An error occurred during an EEPROM operation.
	1	EEPROM download in progress	The control logic sets this bit while data is being downloaded from the EEPROM.
	0	EEPROM upload in progress	The control logic sets this bit while data is being uploaded to the EEPROM.

Table 117. SYSCLK and PLL Status

Address	Bits	Bit Name	Description
0x0D01	7	PLL_3 all locked	Indicates the status of the system clock, APLL_3, and DPLL_3. 0 = system clock or APLL_3 or DPLL_3 is unlocked. 1 = all three PLLs (system clock, APLL_3, and DPLL_3) are locked.
	6	PLL_2 all locked	Indicates the status of the system clock, APLL_2, and DPLL_2. 0 = system clock or APLL_2 or DPLL_2 is unlocked. 1 = all three PLLs (system clock, APLL_2, and DPLL_2) are locked.
	5	PLL_1 all locked	Indicates the status of the system clock, APLL_1, and DPLL_1. 0 = system clock or APLL_1 or DPLL_1 is unlocked. 1 = all three PLLs (system clock, APLL_1, and DPLL_1) are locked.
	4	PLL_0 all locked	Indicates the status of the system clock, APLL_0, and DPLL_0. 0 = system clock or APLL_0 or DPLL_0 is unlocked. 1 = all three PLLs (system clock, APLL_0, and DPLL_0) are locked.
	3	Reserved	Default: 0b.

Address	Bits	Bit Name	Description
	2	SYSCLK calibration busy	Indicates the status of the system clock calibration. 0 (default) = normal operation. 1 = system clock calibration in progress.
	1	SYSCLK stable	The control logic sets this bit when the device considers the system clock to be stable (see the System Clock Stability Timer section).
	0	SYSCLK lock detect	Indicates the status of the system clock PLL. 0 = unlocked. 1 = locked.

Table 118. Status of Reference Inputs

Address	Bits	Bit Name	Description
0x0D02	7	DPLL_3 REFA active	This bit is 1 if DPLL_3 is either locked to or attempting to lock to REFA.
	6	DPLL_2 REFA active	This bit is 1 if DPLL_2 is either locked to or attempting to lock to REFA.
	5	DPLL_1 REFA active	This bit is 1 if DPLL_1 is either locked to or attempting to lock to REFA.
	4	DPLL_0 REFA active	This bit is 1 if DPLL_0 is either locked to or attempting to lock to REFA.
	3	REFA valid	This bit is 1 if the REFA frequency is within the programmed limits and the validation timer has expired.
	2	REFA fault	This bit is 1 if the REFA frequency is outside of the programmed limits.
	1	REFA fast	This bit is 1 if the REFA frequency is higher than allowed by its profile settings. (Note that if no REFA input is detected, the REFA fast and slow bits may both be high.)
	0	REFA slow	This bit is 1 if the REFA frequency is lower than allowed by its profile settings.
0x0D03	7	DPLL_3 REFB active	This bit is 1 if DPLL_3 is either locked to or attempting to lock to REFB.
	6	DPLL_2 REFB active	This bit is 1 if DPLL_2 is either locked to or attempting to lock to REFB.
	5	DPLL_1 REFB active	This bit is 1 if DPLL_1 is either locked to or attempting to lock to REFB.
	4	DPLL_0 REFB active	This bit is 1 if DPLL_0 is either locked to or attempting to lock to REFB.
	3	REFB valid	This bit is 1 if the REFB frequency is within the programmed limits and the validation timer has expired.
	2	REFB fault	This bit is 1 if the REFB frequency is outside of the programmed limits.
	1	REFB fast	This bit is 1 if the REFB frequency is higher than allowed by its profile settings. (Note that if no REFB input is detected, the REFB fast and slow bits may both be high.)
	0	REFB slow	This bit is 1 if the REFB frequency is lower than allowed by its profile settings.
0x0D04	7	DPLL_3 REFC active	This bit is 1 if DPLL_3 is either locked to or attempting to lock to REFC.
	6	DPLL_2 REFC active	This bit is 1 if DPLL_2 is either locked to or attempting to lock to REFC.
	5	DPLL_1 REFC active	This bit is 1 if DPLL_1 is either locked to or attempting to lock to REFC.
	4	DPLL_0 REFC active	This bit is 1 if DPLL_0 is either locked to or attempting to lock to REFC.
	3	REFC valid	This bit is 1 if the REFC frequency is within the programmed limits and the validation timer has expired.
	2	REFC fault	This bit is 1 if the REFC frequency is outside of the programmed limits.
	1	REFC fast	This bit is 1 if the REFC frequency is higher than allowed by its profile settings. (Note that if no REFC input is detected, the REFC fast and slow bits may both be high.)
	0	REFC slow	This bit is 1 if the REFC frequency is lower than allowed by its profile settings.
0x0D05	7	DPLL_3 REFD active	This bit is 1 if DPLL_3 is either locked to or attempting to lock to REFD.
	6	DPLL_2 REFD active	This bit is 1 if DPLL_2 is either locked to or attempting to lock to REFD.
	5	DPLL_1 REFD active	This bit is 1 if DPLL_1 is either locked to or attempting to lock to REFD.
	4	DPLL_0 REFD active	This bit is 1 if DPLL_0 is either locked to or attempting to lock to REFD.
	3	REFD valid	This bit is 1 if the REFD frequency is within the programmed limits and the validation timer has expired.
	2	REFD fault	This bit is 1 if the REFD frequency is outside of the programmed limits.
	1	REFD fast	This bit is 1 if the REFD frequency is higher than allowed by its profile settings. (Note that if no REFD input is detected, the REFD fast and slow bits may both be high.)
	0	REFD slow	This bit is 1 if the REFD frequency is lower than allowed by its profile settings.

IRQ MONITOR (REGISTER 0x0D08 TO REGISTER 0x0D16)

If not masked via the IRQ mask registers (Register 0x010F to Register 0x011D), the appropriate IRQ monitor bit is set to Logic 1 when the indicated event occurs. These bits can be cleared by writing a 1 to the corresponding bit in the IRQ clearing registers (Register 0x0A05 to Register 0x0A0E) by setting the clear all IRQs bit in Register 0x0A05 or by a device reset.

Table 119. IRQ Common Functions

Address	Bits	Bit Name	Description
0x0D08	7	SYSCLK unlocked	IRQ indicating a SYSCLK PLL state transition from locked to unlocked
	6	SYSCLK stable	IRQ indicating that SYSCLK stability time has expired and that the SYSCLK PLL is considered to be stable
	5	SYSCLK locked	IRQ indicating a SYSCLK PLL state transition from unlocked to locked
	4	SYSCLK cal ended	IRQ indicating a SYSCLK PLL has ended its calibration
	3	SYSCLK cal started	IRQ indicating a SYSCLK PLL has started its calibration
	2	Watchdog timer	IRQ indicating expiration of the watchdog timer
	1	EEPROM fault	IRQ indicating a fault during an EEPROM operation
	0	EEPROM complete	IRQ indicating successful completion of an EEPROM operation
0x0D09	7	Reserved	Reserved
	6	REFB validated	IRQ indicating that REFB has been validated
	5	REFB fault cleared	IRQ indicating that REFB has been cleared of a previous fault
	4	REFB fault	IRQ indicating that REFB has been faulted
	3	Reserved	Reserved
	2	REFA validated	IRQ indicating that REFA has been validated
	1	REFA fault cleared	IRQ indicating that REFA has been cleared of a previous fault
	0	REFA fault	IRQ indicating that REFA has been faulted
0x0D0A	7	Reserved	Reserved
	6	REFD validated	IRQ indicating that REFD has been validated
	5	REFD fault cleared	IRQ indicating that REFD has been cleared of a previous fault
	4	REFD fault	IRQ indicating that REFD has been faulted
	3	Reserved	Reserved
	2	REFC validated	IRQ indicating that REFC has been validated
	1	REFC fault cleared	IRQ indicating that REFC has been cleared of a previous fault
	0	REFC fault	IRQ indicating that REFC has been faulted

Table 120. IRQ Monitor for Digital PLL0 (DPLL_0)

Address	Bits	Bit Name	Description
0x0D0B	7	Frequency unclamped	IRQ indicating that DPLL_0 has exited a frequency clamped state
	6	Frequency clamped	IRQ indicating that DPLL_0 has entered a frequency clamped state
	5	Phase slew unlimited	IRQ indicating that DPLL_0 has exited a phase slew limited state
	4	Phase slew limited	IRQ indicating that DPLL_0 has entered a phase slew limited state
	3	Frequency unlocked	IRQ indicating that DPLL_0 has lost frequency lock
	2	Frequency locked	IRQ indicating that DPLL_0 has acquired frequency lock
	1	Phase unlocked	IRQ indicating that DPLL_0 has lost phase lock
	0	Phase locked	IRQ indicating that DPLL_0 has acquired phase lock
0x0D0C	7	DPLL_0 switching	IRQ indicating that DPLL_0 is switching to a new reference
	6	DPLL_0 free run	IRQ indicating that DPLL_0 has entered free run mode
	5	DPLL_0 holdover	IRQ indicating that DPLL_0 has entered holdover mode
	4	DPLL_0 history updated	IRQ indicating that DPLL_0 has updated its tuning word history
	3	REFD activated	IRQ indicating that DPLL_0 has activated REFD
	2	REFC activated	IRQ indicating that DPLL_0 has activated REFC
	1	REFB activated	IRQ indicating that DPLL_0 has activated REFB
	0	REFA activated	IRQ indicating that DPLL_0 has activated REFA

Address	Bits	Bit Name	Description
0x0D0D	7	Phase step direction	IRQ indicating that the DPLL_0 demapping controller phase step direction
	6	Demap control unclamped	IRQ indicating that the DPLL_0 demapping controller is unclamped
	5	Demap control clamped	IRQ indicating that the DPLL_0 demapping controller is clamped
	4	Clock dist sync'd	IRQ indicating a distribution sync event
	3	APLL_0 unlocked	IRQ indicating that APLL_0 has been unlocked
	2	APLL_0 locked	IRQ indicating that APLL_0 has been locked
	1	APLL_0 cal ended	IRQ indicating that APLL_0 calibration complete
	0	APLL_0 cal started	IRQ indicating that APLL_0 calibration started

Table 121. IRQ Monitor for Digital PLL1 (DPLL_1)

Address	Bits	Bit Name	Description
0x0D0E	7	Frequency unclamped	IRQ indicating that DPLL_1 has exited a frequency clamped state
	6	Frequency clamped	IRQ indicating that DPLL_1 has entered a frequency clamped state
	5	Phase slew unlimited	IRQ indicating that DPLL_1 has exited a phase slew limited state
	4	Phase slew limited	IRQ indicating that DPLL_1 has entered a phase slew limited state
	3	Frequency unlocked	IRQ indicating that DPLL_1 has lost frequency lock
	2	Frequency locked	IRQ indicating that DPLL_1 has acquired frequency lock
	1	Phase unlocked	IRQ indicating that DPLL_1 has lost phase lock
	0	Phase locked	IRQ indicating that DPLL_1 has acquired phase lock
0x0D0F	7	DPLL_1 switching	IRQ indicating that DPLL_1 is switching to a new reference
	6	DPLL_1 free run	IRQ indicating that DPLL_1 has entered free run mode
	5	DPLL_1 holdover	IRQ indicating that DPLL_1 has entered holdover mode
	4	DPLL_1 history updated	IRQ indicating that DPLL_1 has updated its tuning word history
	3	REFD activated	IRQ indicating that DPLL_1 has activated REFD
	2	REFC activated	IRQ indicating that DPLL_1 has activated REFC
	1	REFB activated	IRQ indicating that DPLL_1 has activated REFB
	0	REFA activated	IRQ indicating that DPLL_1 has activated REFA
0x0D10	7	Phase step direction	IRQ indicating that the DPLL_1 demapping controller phase step direction
	6	Demap control unclamped	IRQ indicating that the DPLL_1 demapping controller is unclamped
	5	Demap control clamped	IRQ indicating that the DPLL_1 demapping controller is clamped
	4	Clock dist sync'd	IRQ indicating a distribution sync event
	3	APLL_1 unlocked	IRQ indicating that APLL_1 has been unlocked
	2	APLL_1 locked	IRQ indicating that APLL_1 has been locked
	1	APLL_1 cal ended	IRQ indicating that APLL_1 calibration complete
	0	APLL_1 cal started	IRQ indicating that APLL_1 calibration started

Table 122. IRQ Monitor for Digital PLL2 (DPLL_2)

Address	Bits	Bit Name	Description
0x0D11	7	Frequency unclamped	IRQ indicating that DPLL_2 has exited a frequency clamped state
	6	Frequency clamped	IRQ indicating that DPLL_2 has entered a frequency clamped state
	5	Phase slew unlimited	IRQ indicating that DPLL_2 has exited a phase slew limited state
	4	Phase slew limited	IRQ indicating that DPLL_2 has entered a phase slew limited state
	3	Frequency unlocked	IRQ indicating that DPLL_2 has lost frequency lock
	2	Frequency locked	IRQ indicating that DPLL_2 has acquired frequency lock
	1	Phase unlocked	IRQ indicating that DPLL_2 has lost phase lock
	0	Phase locked	IRQ indicating that DPLL_2 has acquired phase lock
0x0D12	7	DPLL_2 switching	IRQ indicating that DPLL_2 is switching to a new reference
	6	DPLL_2 free run	IRQ indicating that DPLL_2 has entered free run mode
	5	DPLL_2 holdover	IRQ indicating that DPLL_2 has entered holdover mode
	4	DPLL_2 history updated	IRQ indicating that DPLL_2 has updated its tuning word history
	3	REFD activated	IRQ indicating that DPLL_2 has activated REFD
	2	REFC activated	IRQ indicating that DPLL_2 has activated REFC
	1	REFB activated	IRQ indicating that DPLL_2 has activated REFB
	0	REFA activated	IRQ indicating that DPLL_2 has activated REFA
0x0D13	7	Phase step direction	IRQ indicating that the DPLL_2 demapping controller phase step direction
	6	Demap control unclamped	IRQ indicating that the DPLL_2 demapping controller is unclamped
	5	Demap control clamped	IRQ indicating that the DPLL_2 demapping controller is clamped
	4	Clock dist sync'd	IRQ indicating a distribution sync event
	3	APLL_2 unlocked	IRQ indicating that APLL_2 has been unlocked
	2	APLL_2 locked	IRQ indicating that APLL_2 has been locked
	1	APLL_2 cal ended	IRQ indicating that APLL_2 calibration complete
	0	APLL_2 cal started	IRQ indicating that APLL_2 calibration started

Table 123. IRQ Monitor for Digital PLL3 (DPLL_3)

Address	Bits	Bit Name	Description
0x0D14	7	Frequency unclamped	IRQ indicating that DPLL_3 has exited a frequency clamped state
	6	Frequency clamped	IRQ indicating that DPLL_3 has entered a frequency clamped state
	5	Phase slew unlimited	IRQ indicating that DPLL_3 has exited a phase slew limited state
	4	Phase slew limited	IRQ indicating that DPLL_3 has entered a phase slew limited state
	3	Frequency unlocked	IRQ indicating that DPLL_3 has lost frequency lock
	2	Frequency locked	IRQ indicating that DPLL_3 has acquired frequency lock
	1	Phase unlocked	IRQ indicating that DPLL_3 has lost phase lock
	0	Phase locked	IRQ indicating that DPLL_3 has acquired phase lock
0x0D15	7	DPLL_3 switching	IRQ indicating that DPLL_3 is switching to a new reference
	6	DPLL_3 free run	IRQ indicating that DPLL_3 has entered free run mode
	5	DPLL_3 holdover	IRQ indicating that DPLL_3 has entered holdover mode
	4	DPLL_3 history updated	IRQ indicating that DPLL_3 has updated its tuning word history
	3	REFD activated	IRQ indicating that DPLL_3 has activated REFD
	2	REFC activated	IRQ indicating that DPLL_3 has activated REFC
	1	REFB activated	IRQ indicating that DPLL_3 has activated REFB
	0	REFA activated	IRQ indicating that DPLL_3 has activated REFA
0x0D16	7	Phase step direction	IRQ indicating that the DPLL_3 demapping controller phase step direction
	6	Demap control unclamped	IRQ indicating that the DPLL_3 demapping controller is unclamped
	5	Demap control clamped	IRQ indicating that the DPLL_3 demapping controller is clamped
	4	Clock dist sync'd	IRQ indicating a distribution sync event
	3	APLL_3 unlocked	IRQ indicating that APLL_3 has been unlocked
	2	APLL_3 locked	IRQ indicating that APLL_3 has been locked
	1	APLL_3 cal ended	IRQ indicating that APLL_3 calibration complete
	0	APLL_3 cal started	IRQ indicating that APLL_3 calibration started

PLL_0 READ ONLY STATUS (REGISTER 0x0D20 TO REGISTER 0x0D2A)

All bits in Register 0x0D20 to Register 0x0D2A are read only. To report the latest status, these bits require an IO_UPDATE (Register 0x000F = 0x01) immediately before being read.

Table 124. PLL_0 Lock Status

Address	Bits	Bit Name	Description
0x0D20	[7:5]	Reserved	Default: 000b.
	4	APLL_0 cal in progress	The control logic holds this bit set while the calibration of the APLL_0 VCO is in progress.
	3	APLL_0 frequency lock	Indicates the status of APLL_0. 0 = unlocked. 1 = locked.
	2	DPLL_0 frequency lock	Indicates the frequency lock status of DPLL_0. 0 = unlocked. 1 = locked.
	1	DPLL_0 phase lock	Indicates the phase lock status of DPLL_0. 0 = unlocked. 1 = locked.
	0	PLL_0 all locked	Indicates the status of the system clock, APLL_0, and DPLL_0. 0 = system clock PLL, APLL_0, or DPLL_0 is unlocked. 1 = all three PLLs (system clock PLL, APLL_0, and DPLL_0) are locked.

Table 125. DPLL_0 Loop State

Address	Bits	Bit Name	Description
0x0D21	[7:5]	Reserved	Default: 000b.
	[4:3]	DPLL_0 active ref	Indicates the reference input that DPLL_0 is using. 00 = DPLL_0 has selected REFA. 01 = DPLL_0 has selected REFB. 10 = DPLL_0 has selected REFC. 11 = DPLL_0 has selected REFD.
	2	DPLL_0 switching	Indicates that DPLL_0 is switching input references. 0 = DPLL is not switching. 1 = DPLL is switching input references.
	1	DPLL_0 holdover	Indicates that DPLL_0 is in holdover mode. 0 = not in holdover. 1 = in holdover mode.
	0	DPLL_0 free run	Indicates that DPLL_0 is in free run mode. 0 = not in free run mode. 1 = in free run mode.
0x0D22	[7:4]	Reserved	Default: 00000b.
	3	Demap controller clamped	The control logic sets this bit when DPLL_0 demapping controller is clamped.
	2	DPLL_0 phase slew limited	The control logic sets this bit when DPLL_0 is phase slew limited.
	1	DPLL_0 frequency clamped	The control logic sets this bit when DPLL_0 is frequency clamped.
	0	DPLL_0 history available	The control logic sets this bit when the tuning word history of DPLL_0 is available. (See Register 0x0D23 to Register 0x0D26 for the tuning word.)

Table 126. DPLL_0 Holdover History

Address	Bits	Bit Name	Description
0x0D23	[7:0]	DPLL_0 tuning word readback, Bits[23:0]	DPLL_0 tuning word readback bits, Bits[7:0]. This group of registers contains the averaged digital PLL tuning word used when the DPLL enters holdover. Setting the history accumulation timer to its minimal value allows the user to use these registers for a read back of the most recent DPLL tuning word with only 1 ms of averaging. Instantaneous tuning word readback is not available.
0x0D24	[7:0]		DPLL_0 tuning word readback, Bits[15:8].
0x0D25	[7:0]		DPLL_0 tuning word readback, Bits[23:16].
0x0D26	[7:6]	Reserved	Reserved.
	[5:0]	DPLL_0 tuning word readback, Bits[29:24]	DPLL_0 tuning word readback, Bits[29:24].

Table 127. DPLL_0 Phase Lock and Frequency Lock Bucket Levels

Address	Bits	Bit Name	Description
0x0D27	[7:0]	DPLL_0 phase lock detect bucket level	Read only digital PLL lock detect bucket level, Bits[7:0]; see the DPLL Frequency Lock Detector section for details.
0x0D28	[7:4]	Reserved	Reserved.
	[3:0]	DPLL_0 phase lock detect bucket level	Read only digital PLL lock detect bucket level, Bits[11:8]; see the DPLL Frequency Lock Detector section for details.
0x0D29	[7:0]	DPLL_0 frequency lock detect bucket level	Read only digital PLL lock detect bucket level, Bits[7:0]; see the DPLL Phase Lock Detector section for details.
0x0D2A	[7:4]	Reserved	Reserved.
	[3:0]	DPLL_0 frequency lock detect bucket level	Read only digital PLL lock detect bucket level, Bits[11:8]; see the DPLL Phase Lock Detector section for details.

PLL_1 READ ONLY STATUS (REGISTER 0x0D40 TO REGISTER 0x0D4A)

These registers mimic the PLL_0 control registers (Register 0x0D20 through Register 0x0D2A) but the register addresses are offset by 0x0020. All default values are identical. All bits in Register 0x0D40 to Register 0x0D4A are read only. To report the latest status, these bits require an IO_UPDATE (Register 0x000F = 0x01) immediately before being read.

PLL_2 READ ONLY STATUS (REGISTER 0x0D60 TO REGISTER 0x0D6A)

These registers mimic the PLL_0 control registers (Register 0x0D20 through Register 0x0D2A) but the register addresses are offset by 0x0040. All bits in Register 0x0D60 to Register 0x0D6A are read only. To report the latest status, these bits require an IO_UPDATE (Register 0x000F = 0x01) immediately before being read.

PLL_3 READ ONLY STATUS (REGISTER 0x0D80 TO REGISTER 0x0D8A)

These registers mimic the PLL_0 control registers (Register 0x0D20 through Register 0x0D2A) but the register addresses are offset by 0x0060. All bits in Register 0x0D40 to Register 0x0D4A are read only. To report the latest status, these bits require an IO_UPDATE (Register 0x000F = 0x01) immediately before being read.

EEPROM CONTROL (REGISTER 0x0E00 TO REGISTER 0x0E03)

Table 128. Nonvolatile Memory (EEPROM) Control

Address	Bits	Bit Name	Description
0x0E00	[7:2]	Reserved	Reserved
	1	Enable I^2C fast mode	Sets the speed of the external I^2C EEPROM interface. 0 (default) = 100 kHz. 1 = 400 kHz.
	0	Write enable	EEPROM write enable. 0 (default) = EEPROM write disabled. 1 = EEPROM write enabled. Note that the external EEPROM may have its own write protect mechanism that is not controlled by this bit.
0x0E01	[7:4]	Reserved	Reserved.
	[3:0]	Conditional value	When set to a nonzero value, it establishes the condition for EEPROM downloads. The default value is 0. A value of 0 indicates that the power-up/reset condition is used. Any nonzero value overrides this condition.
0x0E02	[7:1]	Reserved	Reserved.
	0	Save to EEPROM	Uploads data to the EEPROM (see the EEPROM Storage Sequence (Register 0x0E10 to Register 0x0E61) section for more information). This bit is autoclearing.
0x0E03	[7:1]	Reserved	Reserved.
	0	Load from EPROM	Downloads data from the EEPROM. This bit is autoclearing.

EEPROM STORAGE SEQUENCE (REGISTER 0x0E10 TO REGISTER 0x0E61)

The default settings of Register 0x0E10 to Register 0x0E61 contain the default EEPROM instruction sequence. Table 129 to Table 152 provide descriptions of the register defaults. The default values assume that the user wishes to carry out an EEPROM storage sequence in which all of the registers are stored and loaded by the EEPROM.

Table 129. EEPROM Storage Sequence for Mx Pin Settings and IRQ Masks

Address	Bits	Bit Name	Description
0x0E10	[7:0]	User free run	The default value of this register is 0x98, which is a user free run command for all PLLs. The controller stores 0x98 in the EEPROM and increments the EEPROM address pointer.
0x0E11	[7:0]	User scratchpad	The default value of this register is 0x01, which is a data instruction. Its decimal value is 1, which tells the controller to transfer two bytes of data (1 + 1), beginning at the address specified by the next two bytes.
0x0E12	[7:0]		The default value of these two registers is 0x00FE. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x00FE in the EEPROM and increments the EEPROM pointer by 2. It then transfers two bytes from the register map (beginning at Address 0x00FE) to the external EEPROM. The two bytes transferred are the EEPROM ID (user scratchpad) in the register map.
0x0E13			
0x0E14	[7:0]	Mx pins and IRQ masks	The default value of this register is 0x1F, which is a data instruction. Its decimal value is 31, which tells the controller to transfer 32 bytes of data (31 + 1), beginning at the address specified by the next two bytes.
0x0E15	[7:0]		The default value of these two registers is 0x0100. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0100 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 32 bytes from the register map (beginning at Address 0x0200) to the external EEPROM. The 32 bytes transferred are the Mx pin and IRQ settings in the register map.
0x0E16			

Table 130. EEPROM Storage Sequence for System Clock Settings

Address	Bits	Bit Name	Description
0x0E17	[7:0]	System clock	The default value of this register is 0x08, which is a data instruction. Its decimal value is 8, which tells the controller to transfer nine bytes of data (8 + 1), beginning at the address specified by the next two bytes. The controller stores 0x08 in the EEPROM and increments the EEPROM address pointer.
0x0E18	[7:0]		The default value of these two registers is 0x0200. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0200 in the EEPROM and increments the EEPROM pointer by 2. It then transfers nine bytes from the register map (beginning at Address 0x0200) to the external EEPROM and increments the EEPROM address pointer by 9. The nine bytes transferred are the system clock settings in the register map.
0x0E19	[7:0]		
0x0E1A	[7:0]	IO_UPDATE	The default value of this register is 0x80, which is an IO_UPDATE instruction. The controller stores 0x80 in the EEPROM and increments the EEPROM address pointer.
0x0E1B	[7:0]	Calibrate SYSCLK	The default value of this register is 0x91, which is a SYSCLK Calibrate instruction. The controller stores 0x91 in the EEPROM and increments the EEPROM address pointer.

Table 131. EEPROM Storage Sequence for Reference Input Settings

Address	Bits	Bit Name	Description
0x0E1C	[7:0]	REFA	The default value of this register is 0x1E, which is a data instruction. Its decimal value is 30, which tells the controller to transfer 31 bytes of data (30 + 1), beginning at the address specified by the next two bytes. The controller stores 0x1E in the EEPROM and increments the EEPROM address pointer.
0x0E1D	[7:0]		The default value of these two registers is 0x0300. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0300 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 31 bytes from the register map (beginning at Address 0x0300) to the external EEPROM and increments the EEPROM address pointer by 31. The 31 bytes transferred are the REFA parameters in the register map.
0x0E1E	[7:0]		

Address	Bits	Bit Name	Description
0x0E1F	[7:0]	REFB	The default value of this register is 0x1E, which is a data instruction. Its decimal value is 30, which tells the controller to transfer 31 bytes of data (30 + 1), beginning at the address specified by the next two bytes. The controller stores 0x1E in the EEPROM and increments the EEPROM address pointer.
0x0E20	[7:0]		The default value of these two registers is 0x0320. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0320 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 31 bytes from the register map (beginning at Address 0x0320) to the external EEPROM and increments the EEPROM address pointer by 31. The 31 bytes transferred are the REFB parameters in the register map.
0x0E21	[7:0]		
0x0E22	[7:0]	REFC	The default value of this register is 0x1E, which is a data instruction. Its decimal value is 30, which tells the controller to transfer 31 bytes of data (30 + 1), beginning at the address specified by the next two bytes. The controller stores 0x1A in the EEPROM and increments the EEPROM address pointer.
0x0E23	[7:0]		The default value of these two registers is 0x0340. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0340 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 31 bytes from the register map (beginning at Address 0x0340) to the external EEPROM and increments the EEPROM address pointer by 31. The 31 bytes transferred are the REFC parameters in the register map.
0x0E24	[7:0]		
0x0E25	[7:0]	REFD	The default value of this register is 0x1E, which is a data instruction. Its decimal value is 30, which tells the controller to transfer 31 bytes of data (30 + 1), beginning at the address specified by the next two bytes. The controller stores 0x1A in the EEPROM and increments the EEPROM address pointer.
0x0E26	[7:0]		The default value of these two registers is 0x0360. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0360 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 31 bytes from the register map (beginning at Address 0x0360) to the external EEPROM and increments the EEPROM address pointer by 31. The 31 bytes transferred are the REFD parameters in the register map.
0x0E27	[7:0]		

Table 132. EEPROM Storage Sequence for DPLL_0 General Settings

Address	Bits	Bit Name	Description
0x0E28	[7:0]	DPLL_0 general settings	The default value of this register is 0x1E, which the controller interprets as a data instruction. Its decimal value is 30, which tells the controller to transfer 31 bytes of data (30 + 1), beginning at the address specified by the next two bytes. The controller stores 0x1E in the EEPROM and increments the EEPROM address pointer.
0x0E29	[7:0]		The default value of these two registers is 0x0400. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0400 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 31 bytes from the register map (beginning at Address 0x0400) to the external EEPROM and increments the EEPROM address pointer by 32 (31 data bytes and one checksum byte). The 31 bytes transferred correspond to the DPLL_0 general settings (for example, free running tuning word) in the register map.
0x0E2A	[7:0]		

Table 133. EEPROM Storage Sequence for APLL_0 Configuration and Output Drivers

Address	Bits	Bit Name	Description
0x0E2B	[7:0]	APLL_0 config and output drivers	The default value of this register is 0x0E, which is a data instruction. Its decimal value is 14, which tells the controller to transfer 15 bytes of data (14 + 1) beginning at the address specified by the next two bytes. The controller stores 0x0E in the EEPROM and increments the EEPROM address pointer.
0x0E2C	[7:0]		The default value of these two registers is 0x0430. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0430 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 31 bytes from the register map (beginning at Address 0x0430) to the external EEPROM and increments the EEPROM address pointer by 15. The 15 bytes transferred correspond to the APLL_0 settings as well as the PLL_0 output driver settings in the register map.
0x0E2D	[7:0]		

Table 134. EEPROM Storage Sequence for PLL_0 Dividers and Bandwidth Settings

Address	Bits	Bit Name	Description
0x0E2E	[7:0]	DPLL_0 dividers and BW	The default value of this register is 0x33, which is a data instruction. Its decimal value is 51, which tells the controller to transfer 52 bytes of data (51 + 1), beginning at the address specified by the next two bytes. The controller stores 0x33 in the EEPROM and increments the EEPROM address pointer.
0x0E2F	[7:0]		The default value of these two registers is 0x0440. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0440 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 52 bytes from the register map (beginning at Address 0x0440) to the external EEPROM and increments the EEPROM address pointer by 52. The 52 bytes transferred correspond to the DPLL_0 feedback dividers and loop bandwidth settings in the register map.
0x0E30	[7:0]		

Table 135. EEPROM Storage Sequence for DPLL_1 General Settings

Address	Bits	Bit Name	Description
0x0E31	[7:0]	DPLL_1 general settings	The default value of this register is 0x1E, which is a data instruction. Its decimal value is 30, which tells the controller to transfer 31 bytes of data (30 + 1), beginning at the address specified by the next two bytes. The controller stores 0x1E in the EEPROM and increments the EEPROM address pointer.
0x0E32	[7:0]		The default value of these two registers is 0x0500. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0500 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 31 bytes from the register map (beginning at Address 0x0500) to the external EEPROM and increments the EEPROM address pointer by 31. The 31 bytes transferred correspond to the DPLL_1 general settings (for example, free running tuning word) in the register map.
0x0E33	[7:0]		

Table 136. EEPROM Storage Sequence for APLL_1 Configuration and Output Drivers

Address	Bits	Bit Name	Description
0x0E34	[7:0]	APLL_1 config and output drivers	The default value of this register is 0x0E, which is a data instruction. Its decimal value is 14, which tells the controller to transfer 15 bytes of data (14 + 1) beginning at the address specified by the next two bytes. The controller stores 0x0E in the EEPROM and increments the EEPROM address pointer.
0x0E35	[7:0]		The default value of these two registers is 0x0530. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0530 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 31 bytes from the register map (beginning at Address 0x0530) to the external EEPROM and increments the EEPROM address pointer by 31. The 31 bytes transferred correspond to the APLL_1 settings as well as the PLL_1 output driver settings in the register map.
0x0E36	[7:0]		

Table 137. EEPROM Storage Sequence for PLL_1 Dividers and Bandwidth Settings

Address	Bits	Bit Name	Description
0x0E37	[7:0]	DPLL_1 dividers and BW	The default value of this register is 0x33, which is a data instruction. Its decimal value is 52, which tells the controller to transfer 53 bytes of data (52 + 1), beginning at the address specified by the next two bytes. The controller stores 0x33 in the EEPROM and increments the EEPROM address pointer.
0x0E38	[7:0]		The default value of these two registers is 0x0540. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0540 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 52 bytes from the register map (beginning at Address 0x0540) to the external EEPROM and increments the EEPROM address pointer by 52. The 52 bytes transferred correspond to the DPLL_1 feedback dividers and loop bandwidth settings in the register map.
0x0E39	[7:0]		

Table 138. EEPROM Storage Sequence for DPLL_2 General Settings

Address	Bits	Bit Name	Description
0x0E3A	[7:0]	DPLL_2 general settings	The default value of this register is 0x1E, which is a data instruction. Its decimal value is 30, which tells the controller to transfer 31 bytes of data (30 + 1), beginning at the address specified by the next two bytes. The controller stores 0x1E in the EEPROM and increments the EEPROM address pointer.
0x0E3B	[7:0]		The default value of these two registers is 0x0600. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0600 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 31 bytes from the register map (beginning at Address 0x0600) to the external EEPROM and increments the EEPROM address pointer by 31. The 31 bytes transferred correspond to the DPLL_2 general settings (for example, free running tuning word) in the register map.
0x0E3C	[7:0]		

Table 139. EEPROM Storage Sequence for APLL_2 Configuration and Output Drivers

Address	Bits	Bit Name	Description
0x0E3D	[7:0]	APLL_2 config and output drivers	The default value of this register is 0x0E, which is a data instruction. Its decimal value is 14, which tells the controller to transfer 15 bytes of data (14 + 1) beginning at the address specified by the next two bytes. The controller stores 0x0E in the EEPROM and increments the EEPROM address pointer.
0x0E3E	[7:0]		The default value of these two registers is 0x0630. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0630 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 31 bytes from the register map (beginning at Address 0x0630) to the external EEPROM and increments the EEPROM address pointer by 31. The 31 bytes transferred correspond to the APLL_2 settings as well as the PLL_2 output driver settings in the register map.
0x0E3F	[7:0]		

Table 140. EEPROM Storage Sequence for PLL_2 Dividers and Bandwidth Settings

Address	Bits	Bit Name	Description
0x0E40	[7:0]	DPLL_2 dividers and BW	The default value of this register is 0x33, which is a data instruction. Its decimal value is 51, which tells the controller to transfer 52 bytes of data (51 + 1), beginning at the address specified by the next two bytes. The controller stores 0x33 in the EEPROM and increments the EEPROM address pointer.
0x0E41	[7:0]		The default value of these two registers is 0x0640. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0640 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 52 bytes from the register map (beginning at Address 0x0640) to the external EEPROM and increments the EEPROM address pointer by 52. The 52 bytes transferred correspond to the DPLL_2 feedback dividers and loop bandwidth settings in the register map.
0x0E42	[7:0]		

Table 141. EEPROM Storage Sequence for DPLL_3 General Settings

Address	Bits	Bit Name	Description
0x0E43	[7:0]	DPLL_3 general settings	The default value of this register is 0x1E, which is a data instruction. Its decimal value is 30, which tells the controller to transfer 31 bytes of data (30 + 1), beginning at the address specified by the next two bytes. The controller stores 0x1E in the EEPROM and increments the EEPROM address pointer.
0x0E44	[7:0]		The default value of these two registers is 0x0700. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0700 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 31 bytes from the register map (beginning at Address 0x0700) to the external EEPROM and increments the EEPROM address pointer by 31. The 31 bytes transferred correspond to the DPLL_3 general settings (for example, free running tuning word) in the register map.
0x0E45	[7:0]		

Table 142. EEPROM Storage Sequence for APLL_3 Configuration and Output Drivers

Address	Bits	Bit Name	Description
0x0E46	[7:0]	APLL_3 config and output drivers	The default value of this register is 0x0E, which is a data instruction. Its decimal value is 14, which tells the controller to transfer 15 bytes of data (14 + 1) beginning at the address specified by the next two bytes. The controller stores 0x0E in the EEPROM and increments the EEPROM address pointer.
0x0E47	[7:0]		The default value of these two registers is 0x0730. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0730 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 31 bytes from the register map (beginning at Address 0x0730) to the external EEPROM and increments the EEPROM address pointer by 31. The 31 bytes transferred correspond to the APLL_3 settings as well as the PLL_3 output driver settings in the register map.
0x0E48	[7:0]		

Table 143. EEPROM Storage Sequence for PLL_3 Dividers and Bandwidth Settings

Address	Bits	Bit Name	Description
0x0E49	[7:0]	DPLL_3 dividers and BW	The default value of this register is 0x33, which is a data instruction. Its decimal value is 52, which tells the controller to transfer 53 bytes of data (52 + 1), beginning at the address specified by the next two bytes. The controller stores 0x33 in the EEPROM and increments the EEPROM address pointer.
0x0E4A	[7:0]		The default value of these two registers is 0x0740. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0740 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 52 bytes from the register map (beginning at Address 0x0740) to the external EEPROM and increments the EEPROM address pointer by 52. The 52 bytes transferred correspond to the DPLL_3 feedback dividers and loop bandwidth settings in the register map.
0x0E4B	[7:0]		

Table 144. EEPROM Storage Sequence for Loop Filter Settings

Address	Bits	Bit Name	Description
0x0E4C	[7:0]	DPLL loop filters	The default value of this register is 0x17, which is a data instruction. Its decimal value is 23, which tells the controller to transfer 24 bytes of data (23 + 1), beginning at the address specified by the next two bytes. The controller stores 0x17 in the EEPROM and increments the EEPROM address pointer.
0x0E4D	[7:0]		The default value of these two registers is 0x0800. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0800 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 24 bytes from the register map (beginning at Address 0x0800) to the external EEPROM and increments the EEPROM address pointer by 24. The 24 bytes transferred are the digital loop filter settings in the register map.
0x0E4E	[7:0]		

Table 145. EEPROM Storage Sequence for Operational Control Common Settings

Address	Bits	Bit Name	Description
0x0E4F	[7:0]	Operational controls (common)	The default value of this register is 0x14, which is a data instruction. Its decimal value is 20, which tells the controller to transfer 21 bytes of data (20 + 1), beginning at the address specified by the next two bytes. The controller stores 0x0E in the EEPROM and increments the EEPROM address pointer.
0x0E50	[7:0]		The default value of these two registers is 0x0A00. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0A00 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 21 bytes from the register map (beginning at Address 0x0A00) to the external EEPROM and increments the EEPROM address pointer by 21. The 21 bytes transferred correspond to the common operational controls in the register map.
0x0E51	[7:0]		

Table 146. EEPROM Storage Sequence for PLL_0 Operational Control Settings

Address	Bits	Bit Name	Description
0x0E52	[7:0]	PLL_0 operational controls	The default value of this register is 0x04, which is a data instruction. Its decimal value is 4, which tells the controller to transfer five bytes of data (4 + 1), beginning at the address specified by the next two bytes. The controller stores 0x04 in the EEPROM and increments the EEPROM address pointer.
0x0E53	[7:0]		The default value of these two registers is 0x0A20. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0A20 in the EEPROM and increments the EEPROM pointer by 2. It then transfers five bytes from the register map (beginning at Address 0x0A20) to the external EEPROM and increments the EEPROM address pointer by five. The five bytes transferred correspond to the PLL_0 operational controls in the register map.
0x0E54	[7:0]		

Table 147. EEPROM Storage Sequence for PLL_1 Operational Control Settings

Address	Bits	Bit Name	Description
0x0E55	[7:0]	PLL_1 operational controls	The default value of this register is 0x04, which is a data instruction. Its decimal value is 4, which tells the controller to transfer five bytes of data (4 + 1), beginning at the address specified by the next two bytes. The controller stores 0x04 in the EEPROM and increments the EEPROM address pointer.
0x0E56	[7:0]		The default value of these two registers is 0x0A40. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0A40 in the EEPROM and increments the EEPROM pointer by 2. It then transfers five bytes from the register map (beginning at Address 0x0A40) to the external EEPROM and increments the EEPROM address pointer by five. The five bytes transferred correspond to the PLL_1 operational controls in the register map.
0x0E57	[7:0]		

Table 148. EEPROM Storage Sequence for PLL_2 Operational Control Settings

Address	Bits	Bit Name	Description
0x0E58	[7:0]	PLL_2 operational controls	The default value of this register is 0x04, which is a data instruction. Its decimal value is 4, which tells the controller to transfer five bytes of data (4 + 1), beginning at the address specified by the next two bytes. The controller stores 0x04 in the EEPROM and increments the EEPROM address pointer.
0x0E59	[7:0]		The default value of these two registers is 0x0A60. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0A60 in the EEPROM and increments the EEPROM pointer by 2. It then transfers five bytes from the register map (beginning at Address 0x0A60) to the external EEPROM and increments the EEPROM address pointer by five. The five bytes transferred correspond to the PLL_2 operational controls in the register map.
0x0E5A	[7:0]		

Table 149. EEPROM Storage Sequence for PLL_3 Operational Control Settings

Address	Bits	Bit Name	Description
0x0E5B	[7:0]	PLL_3 operational controls	The default value of this register is 0x04, which is a data instruction. Its decimal value is 4, which tells the controller to transfer five bytes of data (4 + 1), beginning at the address specified by the next two bytes. The controller stores 0x04 in the EEPROM and increments the EEPROM address pointer.
0x0E5C	[7:0]		The default value of these two registers is 0x0A80. This is the starting address of an EEPROM data transfer because the previous register contains a data instruction that specifies the number of bytes (minus one) to transfer. The controller stores 0x0A80 in the EEPROM and increments the EEPROM pointer by 2. It then transfers five bytes from the register map (beginning at Address 0x0A80) to the external EEPROM and increments the EEPROM address pointer by five. The five bytes transferred correspond to the PLL_3 operational controls in the register map.
0x0E5D	[7:0]		

Table 150. EEPROM Storage Sequence for APLL Calibration

Address	Bits	Bit Name	Description
0x0E5E	[7:0]	IO_UPDATE	The default value of this register is 0x80, which is an IO_UPDATE instruction. The controller stores 0x80 in the EEPROM and increments the EEPROM address pointer.
0x0E5F	[7:0]	Calibrate APLLs	The default value of this register is 0x92, which is a calibrate instruction for all of the APLLs. The controller stores 0x92 in the EEPROM and increments the EEPROM address pointer.
0x0E60	[7:0]	Sync outputs	The default value of this register is 0xA0, which is a distribution sync instruction for all of the output dividers. The controller stores 0xA0 in the EEPROM and increments the EEPROM address pointer.

Table 151. EEPROM Storage Sequence for End of Data

Address	Bits	Bit Name	Description
0x0E61	[7:0]	End of data	The default value of this register is 0xFF, which is an end of data instruction. The controller stores this instruction, as well as four CRC-32 bytes in the EEPROM, resets the EEPROM address pointer, and enters an idle state. Note that if the user replaces this command with a pause rather than an end instruction, the controller actions are the same except that the controller increments the EEPROM address pointer rather than resetting it. This allows the user to store multiple EEPROM profiles in the EEPROM.

Table 152. Unused

Address	Bits	Bit Name	Description
0x0E62 to 0x0E6F	[7:0]	Unused	This area is unused in the default configuration and is available for additional EEPROM storage sequence commands. Note that the EEPROM storage sequence must always end with either an end of data or pause command.

Table 153. V_{CAL} Reference Settings

Address	Bits	Bit Name	Description
0x0FFF	[7:0]	V_{CAL} reference access	Writing 0xF9 to this register allows access to V_{CAL} reference registers at Register 0x1488, Register 0x1588, Register 0x1688, and Register 0x1788. Set this register back to 0x00 after writing to Register 0x1488, Register 0x1588, Register 0x1688, and Register 0x1788 to avoid accidental writes above Register 0x0FFF. 0x00 (and all other values except 0xF9) = access disabled. Default: 0x00. 0xF9 = access enabled.
0x1488	[7:3]	Reserved	Default: 00000b.
	[2:1]	APLL_0 manual cal level	APLL_0 reference voltage used during APLL_0 calibration. Set these bits (and issue an IO_UPDATE by writing Register 0x000F = 0x01) before calibrating the APLLs to ensure optimal performance over temperature and voltage extremes. These bits must be set only once per power cycle. Before writing to this register, Register 0x0FFF must be 0xF9. 00b = Reference Voltage 0 (default). 01b = Reference Voltage 1 (recommended). 10b = Reference Voltage 2. 11b = Reference Voltage 3.
	0	En APLL_0 man cal level	Enables manual control of the V_{CAL} reference setting for APLL_0. 0 = manual control disabled (default). 1 = manual control enabled (recommended).
0x1588	[7:3]	Reserved	Default: 00000b.
	[2:1]	APLL_1 manual cal level	APLL_1 reference voltage used during APLL_0 calibration. Set these bits (and issue an IO_UPDATE by writing Register 0x000F = 0x01) before calibrating the APLLs to ensure optimal performance over temperature and voltage extremes. These bits must be set only once per power cycle. Before writing to this register, Register 0x0FFF must be 0xF9. 00b = Reference Voltage 0 (default). 01b = Reference Voltage 1 (recommended). 10b = Reference Voltage 2. 11b = Reference Voltage 3.
	0	En APLL_1 man cal level	Enables manual control of the V_{CAL} reference setting for APLL_1. 0 = manual control disabled (default). 1 = manual control enabled (recommended).

Address	Bits	Bit Name	Description
0x1688	[7:3]	Reserved	Default: 00000b.
	[2:1]	APLL_2 manual cal level	APLL_2 reference voltage used during APLL_0 calibration. Set these bits (and issue an IO_UPDATE by writing Register 0x000F = 0x01) before calibrating the APLLs to ensure optimal performance over temperature and voltage extremes. These bits must be set only once per power cycle. Before writing to this register, Register 0x0FFF must be 0xF9. 00b = Reference Voltage 0 (default). 01b = Reference Voltage 1 (recommended). 10b = Reference Voltage 2. 11b = Reference Voltage 3.
	0	En APLL_2 man cal level	Enables manual control of the V_{CAL} reference setting for APLL_2. 0 = manual control disabled (default). 1 = manual control enabled (recommended).
0x1788	[7:3]	Reserved	Default: 00000b.
	[2:1]	APLL_3 manual cal level	APLL_3 reference voltage used during APLL_0 calibration. Set these bits (and issue an IO_UPDATE by writing Register 0x000F = 0x01) before calibrating the APLLs to ensure optimal performance over temperature and voltage extremes. These bits must be set only once per power cycle. Before writing to this register, Register 0x0FFF must be 0xF9. 00b = Reference Voltage 0 (default). 01b = Reference Voltage 1 (recommended). 10b = Reference Voltage 2. 11b = Reference Voltage 3.
	0	En APLL_3 man cal level	Enables manual control of the V_{CAL} reference setting for APLL_3. 0 = manual control disabled (default). 1 = manual control enabled (recommended).

Table 154. Multifunction Pin Output Functions (D7 = 1)

Bits[D7:D0] Value	Output Function	Source Proxy
0x80	Static Logic 0	None
0x81	Static Logic 1	None
0x82	System clock divided by 32	None
0x83	Watchdog timer output; this is a strobe whose duration equals (32/(one system clock period)) when timer expires	None
0x84	SYSCLK PLL calibration busy	Register 0x0D01, Bit 2
0x85	SYSCLK PLL lock detected	Register 0x0D01, Bit 0
0x86	SYSCLK PLL stable	Register 0x0D01, Bit 1
0x87	All PLLs locked (logical AND of 0x88, 0x89, 0x8A, 0x8B)	Register 0x0D01, Bits[7:4]
0x88	(DPLL_0 phase lock) AND (APLL_0 lock) AND (SYSCLK PLL lock)	Register 0x0D01, Bit 4
0x89	(DPLL_1 phase lock) AND (APLL_1 lock) AND (SYSCLK PLL lock)	Register 0x0D01, Bit 5
0x8A	(DPLL_2 phase lock) AND (APLL_2 lock) AND (SYSCLK PLL lock)	Register 0x0D01, Bit 6
0x8B	(DPLL_3 phase lock) AND (APLL_3 lock) AND (SYSCLK PLL lock)	Register 0x0D01, Bit 7
0x8C	EEPROM upload (write to EEPROM) in progress	Register 0x0D00, Bit 0
0x8D	EEPROM download (read from EEPROM) in progress	Register 0x0D00, Bit 1
0x8E	EEPROM fault detected	Register 0x0D00, Bit 2
0x90	All IRQs: (IRQ_common) OR (IRQ_PLL_0) OR (IRQ_PLL_1) OR (IRQ_PLL_2) OR (IRQ_PLL_3)	None
0x91	IRQ_common	None
0x92/0x93/0x94/0x95	IRQ_PLL_0/IRQ_PLL_1/IRQ_PLL_2/IRQ_PLL_3	None
0xA0/0xA1/0xA2/0xA3	REFA/REFB/REFC/REFD fault	Register 0x0D02/Register 0x0D03/ Register 0x0D04/Register 0x0D05, Bit 2
0xA8/0xA9/0xAA/0xAB	REFA/REFB/REFC/REFD valid	Register 0x0D02/Register 0x0D03/ Register 0x0D04/Register 0x0D05, Bit 3
0xB0	REFA active (any PLL)	Register 0x0D02, Bit 4||Bit 5||Bit 6||Bit 7
0xB1	REFB active (any PLL)	Register 0x0D03, Bit 4||Bit 5||Bit 6||Bit 7
0xB2	REFC active (any PLL)	Register 0x0D04, Bit 4||Bit 5||Bit 6||Bit 7

Bits[D7:D0] Value	Output Function	Source Proxy
0xB3	REFD active (any PLL)	Register 0x0D05, Bit 4||Bit 5||Bit 6||Bit 7
0xC0	DPLL_0 phase locked	Register 0x0D20, Bit 1
0xC1	DPLL_0 frequency locked	Register 0x0D20, Bit 2
0xC2	APLL_0 frequency lock	Register 0x0D20, Bit 3
0xC3	APLL_0 cal in process	Register 0x0D20, Bit 4
0xC4	DPLL_0 active	Logical OR of Bit 4 in Register 0x0D02 through Register 0x0D05
0xC5	DPLL_0 in free run mode	Register 0x0D21, Bit 0
0xC6	DPLL_0 in holdover	Register 0x0D21, Bit 1
0xC7	DPLL_0 switching	Register 0x0D21, Bit 2
0xC8	DPLL_0 history available	Register 0x0D22, Bit 0
0xC9	DPLL_0 history updated	Register 0x0D0C, Bit 4 (IRQ does not need to be set for this setting to work)
0xCA	DPLL_0 clamp	Register 0x0D22, Bit 1
0xCB	DPLL_0 phase slew limited	Register 0x0D22, Bit 2
0xCC	PLL_0 clock distribution sync pulse	None
0xCD	DPLL_1 demapping controller clamped	Register 0x0D22, Bit 3
0xD0	DPLL_1 phase locked	Register 0x0D40, Bit 1
0xD1	DPLL_1 frequency locked	Register 0x0D40, Bit 2
0xD2	APLL_1 frequency lock	Register 0x0D40, Bit 3
0xD3	APLL_1 cal in process	Register 0x0D40, Bit 4
0xD4	DPLL_1 active	Logical OR of Bit 5 in Register 0x0D02 through Register 0x0D05
0xD5	DPLL_1 in free run mode	Register 0x0D41, Bit 0
0xD6	DPLL_1 in holdover	Register 0x0D41, Bit 1
0xD7	DPLL_1 in switchover	Register 0x0D41, Bit 2
0xD8	DPLL_1 history available	Register 0x0D42, Bit 0
0xD9	DPLL_1 history updated	Register 0x0D0F, Bit 4 (IRQ does not need to be set for this setting to work)
0xDA	DPLL_1 clamp	Register 0x0D42, Bit 1
0xDB	DPLL_1 phase slew limited	Register 0x0D42, Bit 2
0xDC	PLL_1 clock distribution sync pulse	None
0xDD	DPLL_1 demapping controller clamped	Register 0x0D42, Bit 3
0xE0	DPLL_2 phase locked	Register 0x0D60, Bit 1
0xE1	DPLL_2 frequency locked	Register 0x0D60, Bit 2
0xE2	APLL_2 frequency lock	Register 0x0D60, Bit 3
0xE3	APLL_2 cal in process	Register 0x0D60, Bit 4
0xE4	DPLL_2 active	Logical OR of Bit 6 in Register 0x0D02 through Register 0x0D05
0xE5	DPLL_2 in free run mode	Register 0x0D61, Bit 0
0xE6	DPLL_2 in holdover	Register 0x0D61, Bit 1
0xE7	DPLL_2 in switchover	Register 0x0D61, Bit 2
0xE8	DPLL_2 history available	Register 0x0D62, Bit 0
0xE9	DPLL_2 history updated	Register 0x0D0C, Bit 4 (IRQ does not need to be set for this setting to work)
0xEA	DPLL_2 clamp	Register 0x0D62, Bit 1
0xEB	DPLL_2 phase slew limited	Register 0x0D62, Bit 2
0xEC	PLL_2 clock distribution sync pulse	None
0xED	DPLL_2 demapping controller clamped	Register 0x0D62, Bit 4
0xF0	DPLL_3 phase locked	Register 0x0D80, Bit 1
0xF1	DPLL_3 frequency locked	Register 0x0D80, Bit 2
0xF2	APLL_3 frequency lock	Register 0x0D80, Bit 3
0xF3	APLL_3 cal in process	Register 0x0D80, Bit 4

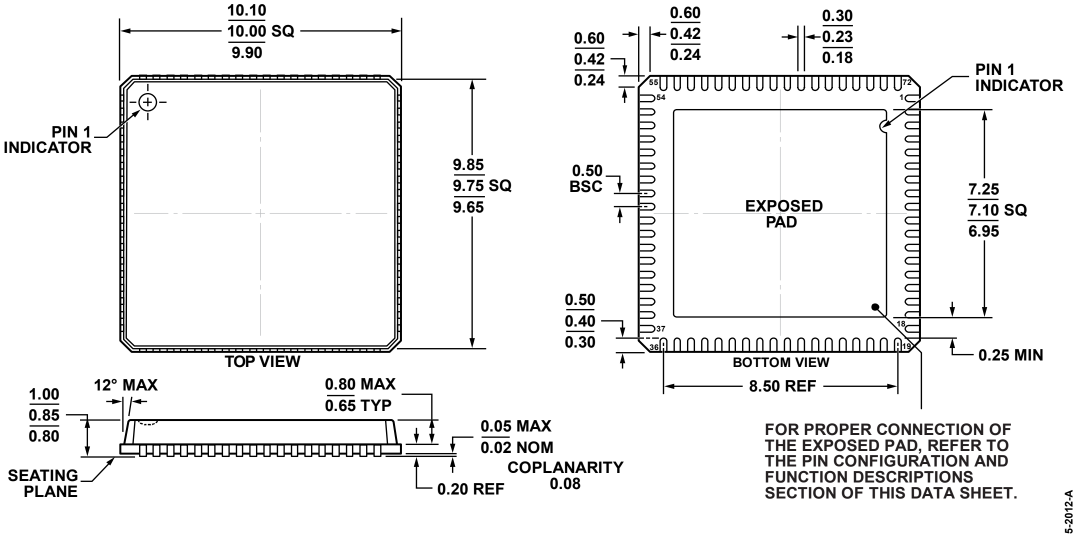
Bits[D7:D0] Value	Output Function	Source Proxy
0xF4	DPLL_3 active	Logical OR of Bit 7 in Register 0x0D02 through Register 0x0D05
0xF5	DPLL_3 in free run mode	Register 0x0D81, Bit 0
0xF6	DPLL_3 in holdover	Register 0x0D81, Bit 1
0xF7	DPLL_3 in switchover	Register 0x0D81, Bit 2
0xF8	DPLL_3 history available	Register 0x0D82, Bit 0
0xF9	DPLL_3 history updated	Register 0x0D0F, Bit 4 (IRQ does not need to be set for this setting to work)
0xFA	DPLL_3 clamp	Register 0x0D82, Bit 1
0xFB	DPLL_3 phase slew limited	Register 0x0D82, Bit 2
0xFC	PLL_3 clock distribution sync pulse	None
0xFD	DPLL_3 demapping controller clamped	Register 0x0D82, Bit 3
0xFE to 0xFF	Reserved	None

Table 155. Multifunction Pin Input Functions (D7 = 0)

Bits[D7:D0] Value	Input Function	Destination Proxy
0x00	No function	None
0x01	IO_UPDATE	Register 0x000F, Bit 0
0x02	Full power-down	Register 0x0A00, Bit 0
0x03	Clear watchdog timer	Register 0x0A05, Bit 7
0x04	Soft sync all	Register 0x0A00, Bit 3
0x10	Clear all IRQs	Register 0x0A05, Bit 0
0x11	Clear common IRQs	Register 0x0A05, Bit 1
0x12	Clear DPLL_0 IRQs	Register 0x0A05, Bit 2
0x13	Clear DPLL_1 IRQs	Register 0x0A05, Bit 3
0x14	Clear DPLL_2 IRQs	Register 0x0A05, Bit 4
0x15	Clear DPLL_3 IRQs	Register 0x0A05, Bit 5
0x20/0x21/0x22/0x23	Force fault REFA/REFB/REFC/REFD	Register 0x0A03, Bits[3:0]
0x28/0x29/0x2A/0x2B	Force validation timeout REFA/REFB/REFC/REFD	Register 0x0A02, Bits[3:0]
0x40	PLL_0 power-down	Register 0x0A20, Bit 0
0x41	DPLL_0 user free run	Register 0x0A22, Bit 0
0x42	DPLL_0 user holdover	Register 0x0A22, Bit 1
0x43	DPLL_0 tuning word history reset	Register 0x0A23, Bit 1
0x44	DPLL_0 increment phase offset	Register 0x0A24, Bit 0
0x45	DPLL_0 decrement phase offset	Register 0x0A24, Bit 1
0x46	DPLL_0 reset phase offset	Register 0x0A24, Bit 2
0x48	APLL_0 soft sync	Register 0x0A20, Bit 2
0x49	PLL_0 disable all output drivers	Register 0x0A21, Bits[3:2]
0x4A	PLL_0 disable OUT0A	Register 0x0A21, Bit 2
0x4B	PLL_0 disable OUT0B	Register 0x0A21, Bit 3
0x4C	PLL_0 manual reference input selection, Bit 0	Register 0x0A22, Bit 5
0x4D	PLL_0 manual reference input selection, Bit 1	Register 0x0A22, Bit 6
0x50	PLL_1 power-down	Register 0x0A40, Bit 0
0x51	DPLL_1 user free run	Register 0x0A42, Bit 0
0x52	DPLL_1 user holdover	Register 0x0A42, Bit 1
0x53	DPLL_1 tuning word history reset	Register 0x0A43, Bit 1
0x54	DPLL_1 increment phase offset	Register 0x0A44, Bit 0
0x55	DPLL_1 decrement phase offset	Register 0x0A44, Bit 1
0x56	DPLL_1 reset phase offset	Register 0x0A44, Bit 2
0x58	APLL_1 soft sync	Register 0x0A40, Bit 2
0x59	PLL_1 disable all output drivers	Register 0x0A41, Bits[3:2]
0x5A	PLL_1 disable OUT1A	Register 0x0A41, Bit 2
0x5B	PLL_1 disable OUT1B	Register 0x0A41, Bit 3

Bits[D7:D0] Value	Input Function	Destination Proxy
0x5C	PLL_1 manual reference input selection, Bit 0	Register 0x0A42, Bit 5
0x5D	PLL_1 manual reference input selection, Bit 1	Register 0x0A42, Bit 6
0x60	PLL_2 power-down	Register 0x0A60, Bit 0
0x61	DPLL_2 user free run	Register 0x0A62, Bit 0
0x62	DPLL_2 user holdover	Register 0x0A62, Bit 1
0x63	DPLL_2 tuning word history reset	Register 0x0A63, Bit 1
0x64	DPLL_2 increment phase offset	Register 0x0A64, Bit 0
0x65	DPLL_2 decrement phase offset	Register 0x0A64, Bit 1
0x66	DPLL_2 reset phase offset	Register 0x0A64, Bit 2
0x68	APLL_2 soft sync	Register 0x0A60, Bit 2
0x69	PLL_2 disable all output drivers	Register 0x0A61, Bits[3:2])
0x6A	PLL_2 disable OUT2A	Register 0x0A61, Bit 2
0x6B	PLL_2 disable OUT2B	Register 0x0A61, Bit 3
0x6C	PLL_2 manual reference input selection, Bit 0	Register 0x0A62, Bit 5
0x6D	PLL_2 manual reference input selection, Bit 1	Register 0x0A62, Bit 6
0x70	PLL_2 power-down	Register 0x0A60, Bit 0
0x71	DPLL_3 user free run	Register 0x0A82, Bit 0
0x72	DPLL_3 user holdover	Register 0x0A82, Bit 1
0x73	DPLL_3 tuning word history reset	Register 0x0A83, Bit 1
0x74	DPLL_3 increment phase offset	Register 0x0A84, Bit 0
0x75	DPLL_3 decrement phase offset	Register 0x0A84, Bit 1
0x76	DPLL_3 reset phase offset	Register 0x0A84, Bit 2
0x78	APLL_3 soft sync	Register 0x0A80, Bit 2
0x79	PLL_3 disable all output drivers	Register 0x0A81, Bits[3:2]
0x7A	PLL_3 disable OUT3A	Register 0x0A81, Bit 2
0x7B	PLL_3 disable OUT3B	Register 0x0A81, Bit 3
0x7C	PLL_3 manual reference input selection, Bit 0	Register 0x0A82, Bit 5
0x7D	PLL_3 manual reference input selection, Bit 1	Register 0x0A82, Bit 6
0x7E to 0x7F	Reserved	None

OUTLINE DIMENSIONS



FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

COMPLIANT TO JEDEC STANDARDS MO-220-VNND-4

Figure 49. 72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
10 mm × 10 mm Body, Very Thin Quad
(CP-72-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9554BCPZ	−40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-4
AD9554BCPZ-REEL	−40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-4
AD9554BCPZ-REEL7	−40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-4
AD9554/PCBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

I^{2}C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

D12132-0-3/17(D)