Ultralow Distortion, Wide Bandwidth Voltage Feedback Op Amps

Data Sheet

AD9631/AD9632

FEATURES

Wide bandwidth
- **AD9631, G = +1**
- **AD9632, G = +2**
- **Small signal**
  - **AD9631, 320 MHz**
  - **AD9632, 250 MHz**
- **Large signal (4 V p-p)**
  - **AD9631, 175 MHz**
  - **AD9632, 180 MHz**

Ultralow distortion (SFDR), low noise
- **−113 dBc typical @ 1 MHz**
- **−95 dBc typical @ 5 MHz**
- **−72 dBc typical @ 20 MHz**
- **46 dBm third-order intercept @ 25 MHz**
- **7.0 nV/√Hz spectral noise density**

High speed
- **Slew rate: 1300 V/μs**
- **Settling time to 0.01%, 2 V step: 16 ns**
- **±3 V to ±5 V supply operation**
- **17 mA supply current**

APPLICATIONS

ADC input driver
Differential amplifiers
IF/RF amplifiers
Pulse amplifiers
Professional video
DAC current to voltage
Baseband and video communications
Pin diode receivers
Active filters/integrators/log amps

GENERAL DESCRIPTION

The AD9631/AD9632 are very high speed and wide bandwidth amplifiers. The AD9631 is unity gain stable. The AD9632 is stable at gains of 2 or greater. Using a voltage feedback architecture, the exceptional settling time, bandwidth, and low distortion of the AD9631/AD9632 meet the requirements of many applications that previously depended on current feedback amplifiers. Its classical op amp structure works much more predictably in many designs.

PIN CONFIGURATION

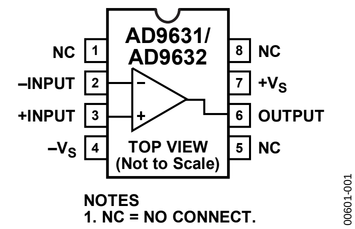

Figure 1. 8-Lead PDIP (N) and SOIC (R) Packages

A proprietary design architecture has produced an amplifier that combines many of the best characteristics of both current feedback and voltage feedback amplifiers. The AD9631/AD9632 exhibit exceptionally fast and accurate pulse response (16 ns to 0.01%) as well as extremely wide small signal and large signal bandwidth and ultralow distortion. The AD9631 achieves −72 dBc at 20 MHz, 320 MHz small signal bandwidth, and 175 MHz large signal bandwidths.

These characteristics position the AD9631/AD9632 ideally for driving flash as well as high resolution ADCs. Additionally, the balanced high impedance inputs of the voltage feedback architecture allow maximum flexibility when designing active filters.

The AD9631/AD9632 are offered in the industrial (−40°C to +85°C) temperature range. They are available in PDIP and SOIC.

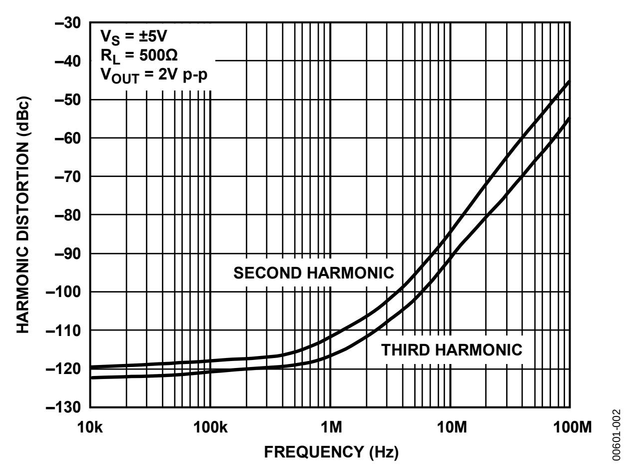

Figure 2. AD9631 Harmonic Distortion vs. Frequency, G = +1

Rev. D **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support **www.analog.com**

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7/03—Rev. B to Rev. C

Deleted Evaluation Boards information ..... Universal
Deleted military CERDIP version ..... Universal
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Updated Outline Dimensions 17

1/03—Rev. A to Rev. B

Deleted DIP (N) Inverter, SOIC (R) Inverter, and DIP (N) Noninverter Evaluation Boards in Figures 12–14 17
Updated Outline Dimensions 18

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$\pm V_S = \pm 5$ V; $R_{LOAD} = 100\ \Omega$; $A_V = 1$ (AD9631); $A_V = 2$ (AD9632), unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	AD9631 Min	AD9631 Typ	AD9631 Max	AD9632 Min	AD9632 Typ	AD9632 Max	Unit
DYNAMIC PERFORMANCE								
Bandwidth (–3 dB)								
Small Signal	$V_{OUT} \leq 0.4$ V p-p	220	320		180	250		MHz
Large Signal[1]	$V_{OUT} = 4$ V p-p	150	175		155	180		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT} = 300$ mV p-p							
	$R_F = 140\ \Omega$ (AD9631); $R_F = 425\ \Omega$ (AD9632)		130			130		MHz
Slew Rate, Average ±	$V_{OUT} = 4$ V step	1000	1300		1200	1500		V/µs
Rise/Fall Time	$V_{OUT} = 0.5$ V step		1.2			1.4		ns
	$V_{OUT} = 4$ V step		2.5			2.1		ns
Settling Time								
To 0.1%	$V_{OUT} = 2$ V step		11			11		ns
To 0.01%	$V_{OUT} = 2$ V step		16			16		ns
HARMONIC/NOISE PERFORMANCE								
Second Harmonic Distortion	2 V p-p; 20 MHz, $R_L = 100\ \Omega$		−64	−57		−54	−47	dBc
	$R_L = 500\ \Omega$		−72	−65		−72	−65	dBc
Third Harmonic Distortion	2 V p-p; 20 MHz, $R_L = 100\ \Omega$		−76	−69		−74	−67	dBc
	$R_L = 500\ \Omega$		−81	−74		−81	−74	dBc
Third-Order Intercept	25 MHz		46			41		dBm
Noise Figure	$R_S = 50\ \Omega$		18			14		dB
Input Voltage Noise	1 MHz to 200 MHz		7.0			4.3		nA/√Hz
Input Current Noise	1 MHz to 200 MHz		2.5			2.0		pA/√Hz
Average Equivalent Integrated Input Noise Voltage	0.1 MHz to 200 MHz		100			60		µV rms
Differential Gain Error (3.58 MHz)	$R_L = 150\ \Omega$		0.03	0.06		0.02	0.04	%
Differential Phase Error (3.58 MHz)	$R_L = 150\ \Omega$		0.02	0.04		0.02	0.04	Degree
Phase Nonlinearity	DC to 100 MHz		1.1			1.1		Degree
DC PERFORMANCE[2]	$R_L = 150\ \Omega$							
Input Offset Voltage[3]			3	10		2	5	mV
	$T_{MIN} – T_{MAX}$			13			8	mV
Offset Voltage Drift			±10			±10		µV/°C
Input Bias Current			2	7		2	7	µA
	$T_{MIN} – T_{MAX}$			10			10	µA
Input Offset Current			0.1	3		0.1	3	µA
	$T_{MIN} – T_{MAX}$			5			5	µA
Common-Mode Rejection Ratio	$V_{CM} = \pm 2.5$ V	70	90		70	90		dB
Open-Loop Gain	$V_{OUT} = \pm 2.5$ V	46	52		46	52		dB
	$T_{MIN} – T_{MAX}$	40			40			dB
INPUT CHARACTERISTICS								
Input Resistance			500			500		kΩ
Input Capacitance			1.2			1.2		pF
Input Common-Mode Voltage Range			±3.4			±3.4		V

Parameter	Test Conditions/Comments	AD9631 Min	AD9631 Typ	AD9631 Max	AD9632 Min	AD9632 Typ	AD9632 Max	Unit
OUTPUT CHARACTERISTICS								
Output Voltage Range	R_L = 150 Ω	±3.2	±3.9		±3.2	±3.9		V
Output Current			70			70		mA
Output Resistance			0.3			0.3		Ω
Short Circuit Current			240			240		mA
POWER SUPPLY								
Operating Range		±3.0	±5.0	±6.0	±3.0	±5.0	±6.0	V
Quiescent Current			17	18		16	17	mA
	T_{MIN} – T_{MAX}			21			20	mA
Power Supply Rejection Ratio	T_{MIN} – T_{MAX}	50	60		56	66		dB

[1] See the Absolute Maximum Ratings and Theory of Operation sections of this data sheet.
[2] Measured at A_V = 50.
[3] Measured with respect to the inverting input.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage ($+V_S$ to $-V_S$)	12.6 V
Voltage Swing × Bandwidth Product	550 V × MHz
Internal Power Dissipation	
PDIP (N)	1.3 W
SOIC (R)	0.9 W
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	±1.2 V
Output Short Circuit Duration	Observe Power Derating Curves
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range (A Grade)	−40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

METALLIZATION PHOTO

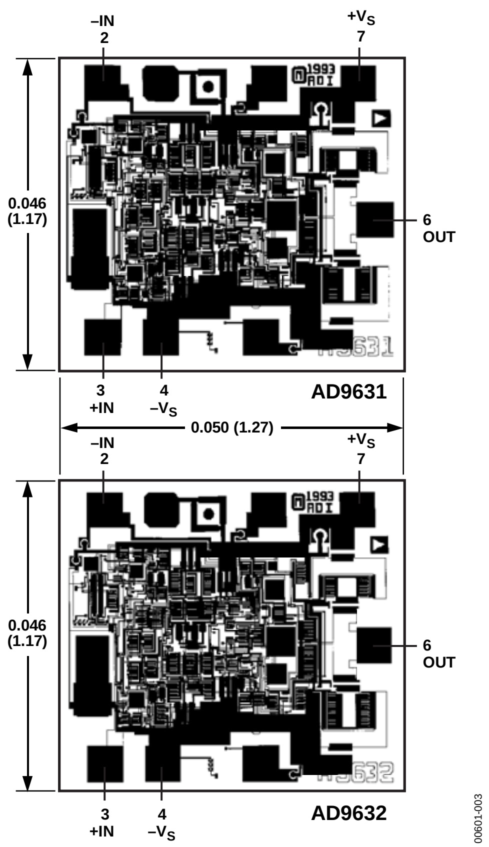

Figure 3. Dimensions shown in inches and (millimeters) Connect Substrate to $-V_S$

THERMAL RESISTANCE

Table 3.

Package Type[1]	θ_{JA}	Unit
8-Lead PDIP (N)	90	°C/W
8-Lead SOIC (R)	140	°C/W

[1] For device in free air.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by these devices is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD9631 and AD9632 are internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

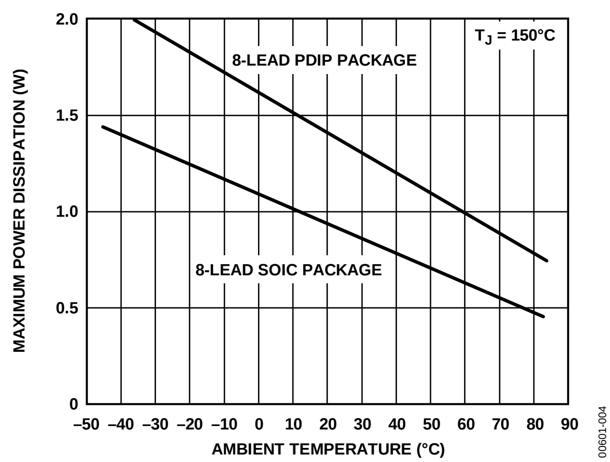

Figure 4. Maximum Power Dissipation vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

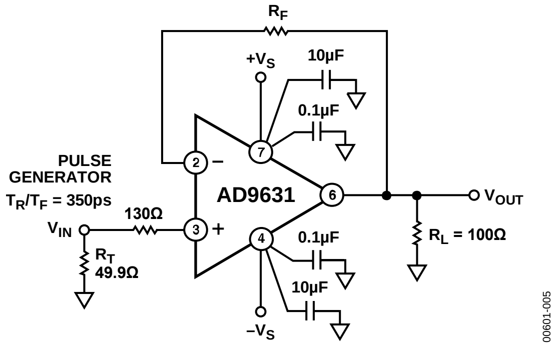

Figure 5. AD9631 Noninverting Configuration, $G = +1$

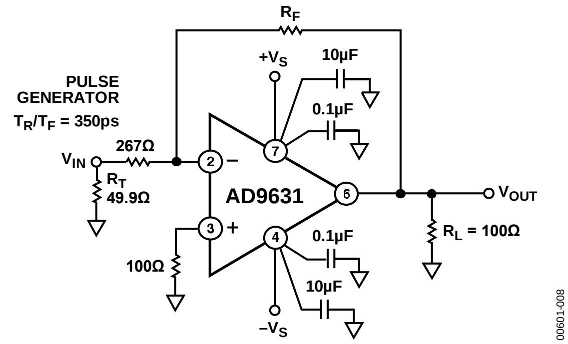

Figure 8. AD9631 Inverting Configuration, $G = -1$

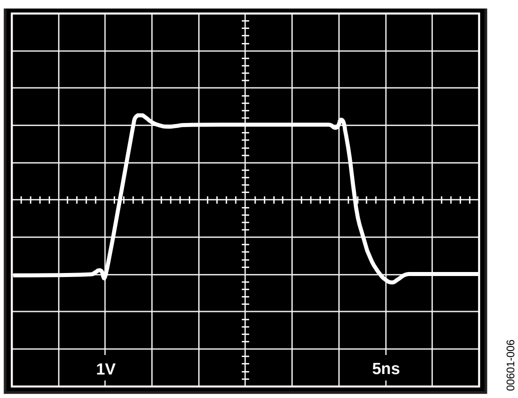

Figure 6. AD9631 Large Signal Transient Response; $V_{OUT} = 4$ V p-p, $G = +1$, $R_F = 250\ \Omega$

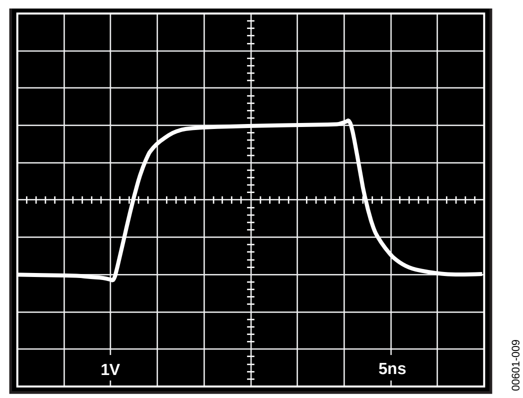

Figure 9. AD9631 Large Signal Transient Response; $V_{OUT} = 4$ V p-p, $G = -1$, $R_F = R_{IN} = 267\ \Omega$

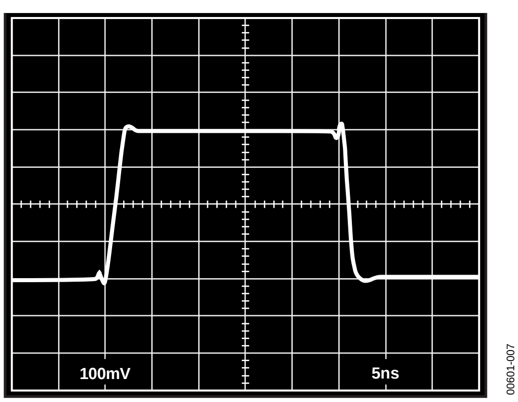

Figure 7. AD9631 Small Signal Transient Response; $V_{OUT} = 400$ mV p-p, $G = +1$, $R_F = 140\ \Omega$

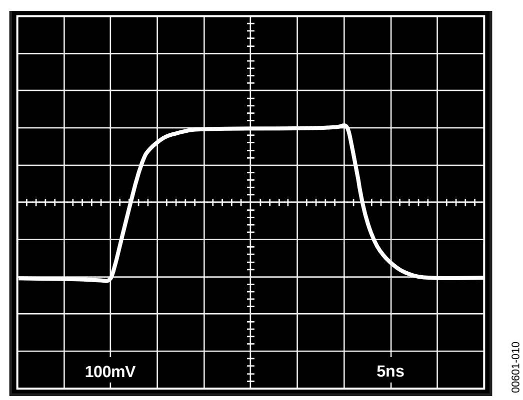

Figure 10. AD9631 Small Signal Transient Response; $V_{OUT} = 400$ mV p-p, $G = -1$, $R_F = R_{IN} = 267\ \Omega$

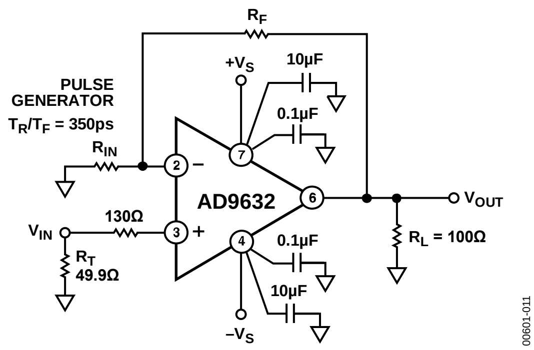

Figure 11. AD9632 Noninverting Configuration, G = +2

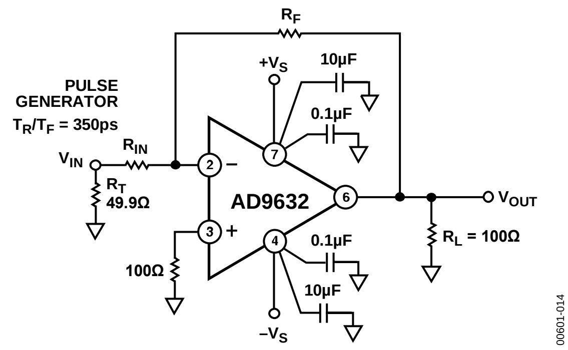

Figure 14. AD9632 Inverting Configuration, G = −1

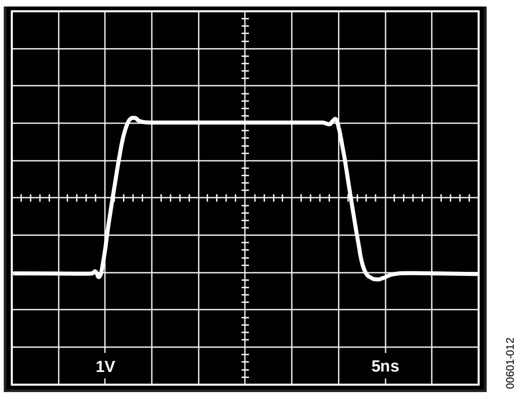

Figure 12. AD9632 Large Signal Transient Response; V_{OUT} = 4 V p-p, G = +2, $R_F = R_{IN}$ = 422 Ω

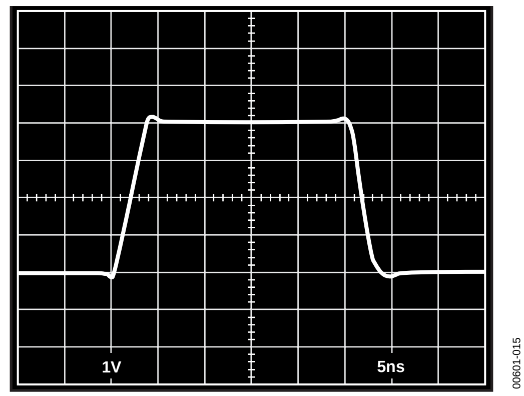

Figure 15. AD9632 Large Signal Transient Response; V_{OUT} = 4 V p-p, G = −1, $R_F = R_{IN}$ = 422 Ω, R_T = 56.2 Ω

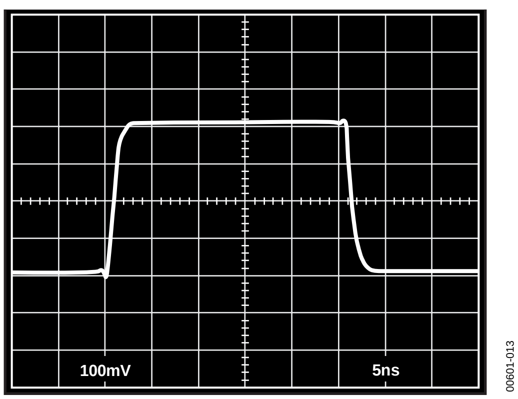

Figure 13. AD9632 Small Signal Transient Response; V_{OUT} = 400 mV p-p, G = +2, $R_F = R_{IN}$ = 274 Ω

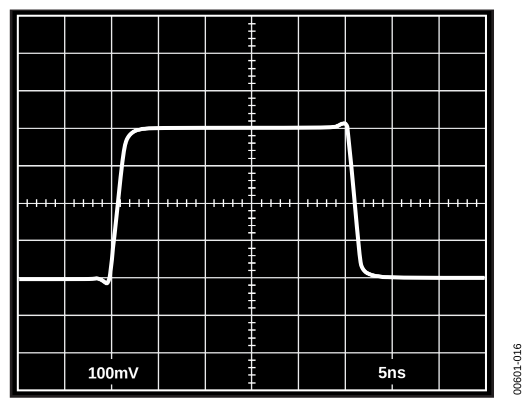

Figure 16. AD9632 Small Signal Transient Response; V_{OUT} = 400 mV p-p, G = −1, $R_F = R_{IN}$ = 267 Ω, R_T = 61.9 Ω

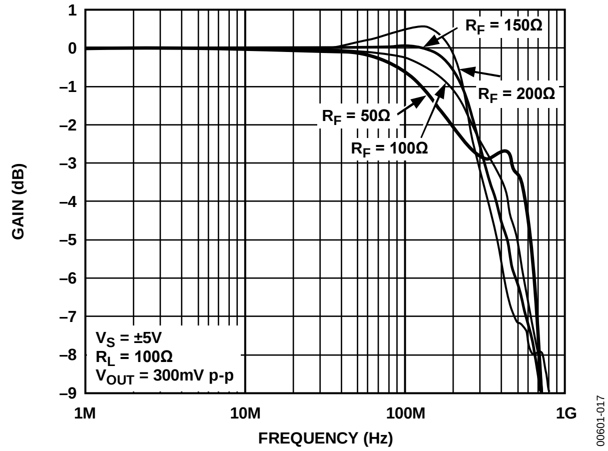

Figure 17. AD9631 Small Signal Frequency Response, G = +1

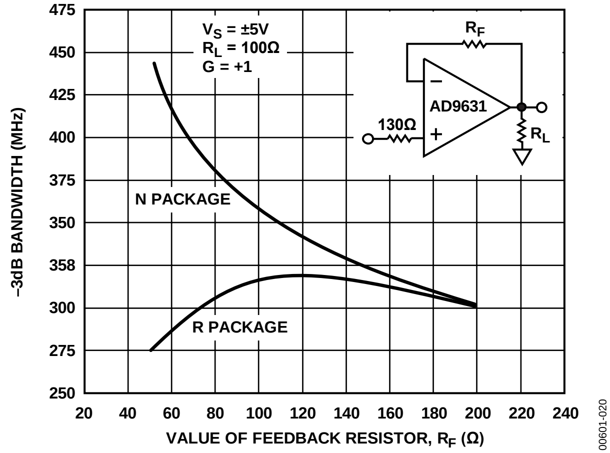

Figure 20. AD9631 Small Signal −3 dB Bandwidth vs. R_F

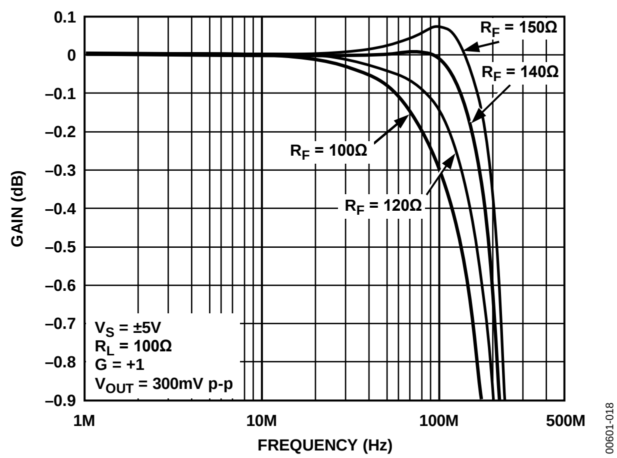

Figure 18. AD9631 0.1 dB Flatness, N Package (for R Package Add 20 Ω to R_F)

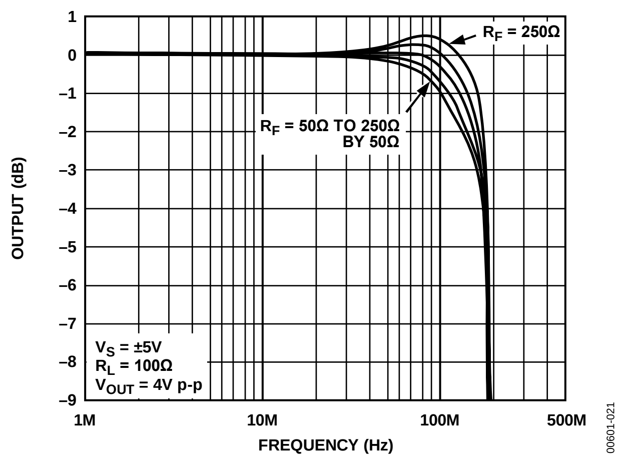

Figure 21. AD9631 Large Signal Frequency Response, G = +1

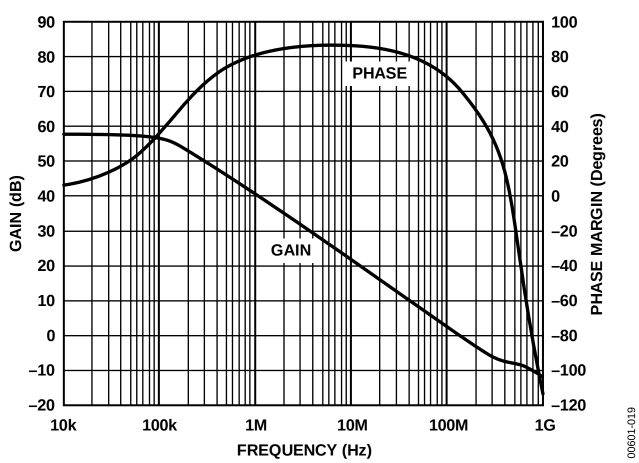

Figure 19. AD9631 Open-Loop Gain and Phase Margin vs. Frequency, R_L = 100 Ω

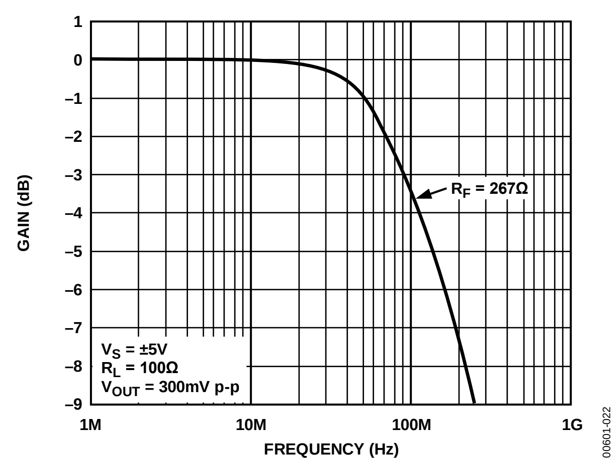

Figure 22. AD9631 Small Signal Frequency Response, G = −1

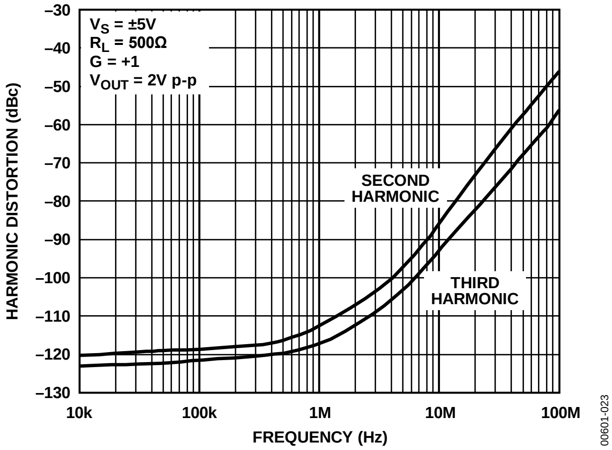

Figure 23. AD9631 Harmonic Distortion vs. Frequency, R_L = 500 Ω

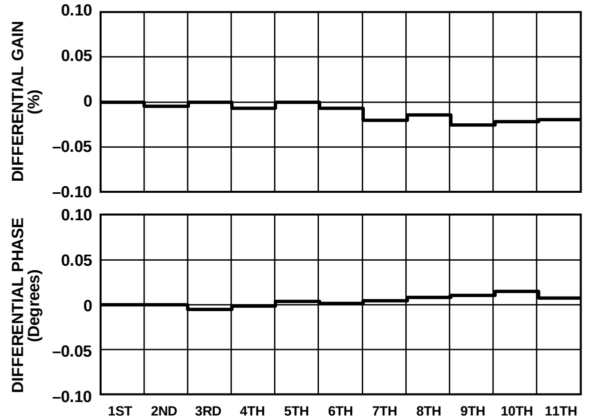

Figure 26. AD9631 Differential Gain and Phase Error, G = +2, R_L = 150 Ω

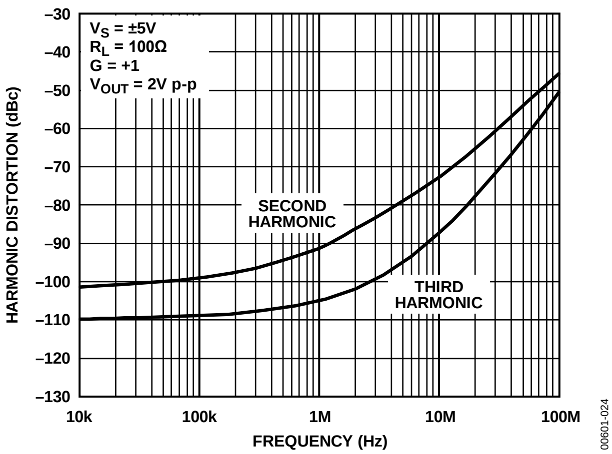

Figure 24. AD9631 Harmonic Distortion vs. Frequency, R_L = 100 Ω

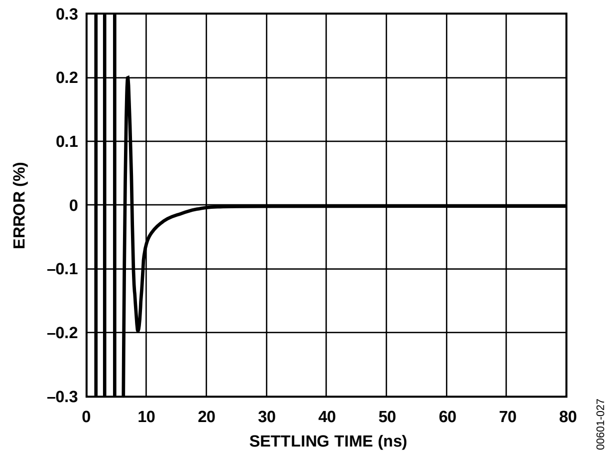

Figure 27. AD9631 Short-Term Settling Time, 2 V Step, R_L = 100 Ω

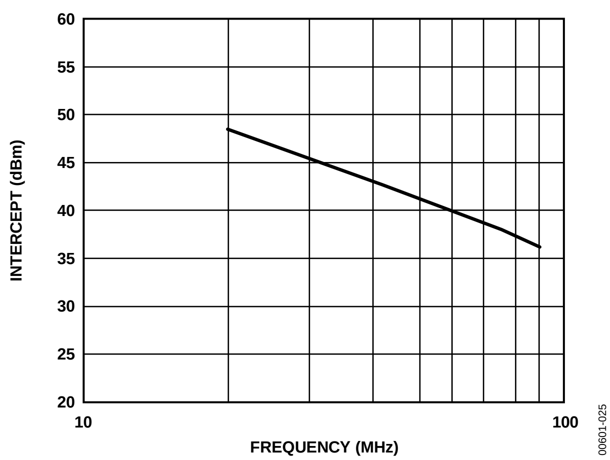

Figure 25. AD9631 Third Order Intercept vs. Frequency

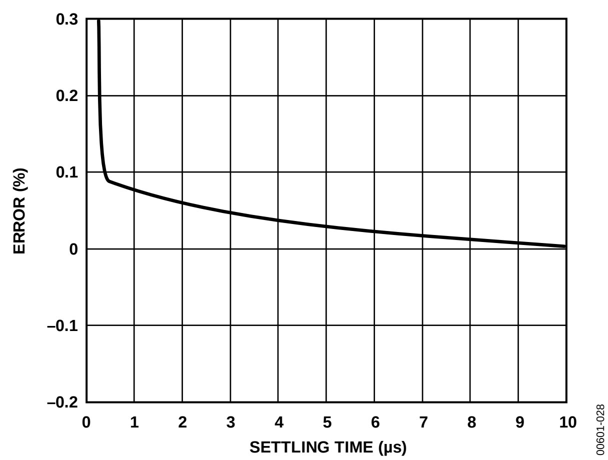

Figure 28. AD9631 Long-Term Settling Time, 2 V Step, R_L = 100 Ω

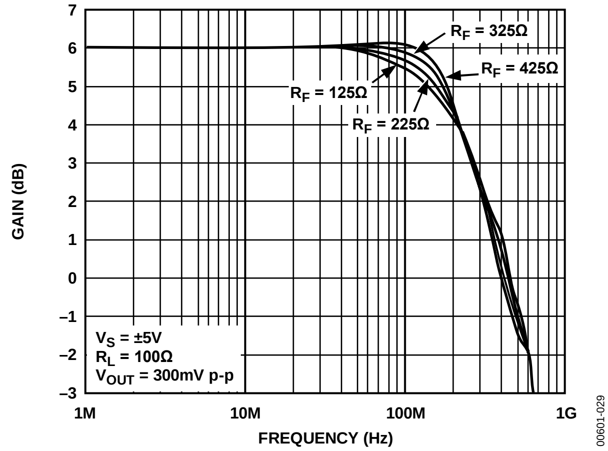

Figure 29. AD9632 Small Signal Frequency Response, G = +2

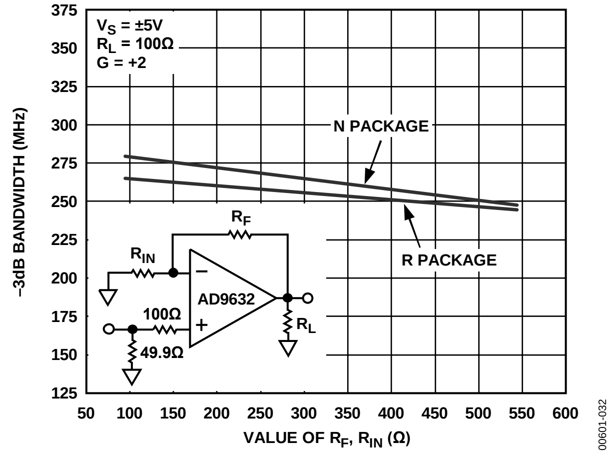

Figure 32. AD9632 Small Signal –3 dB Bandwidth vs. R_F, R_{IN}

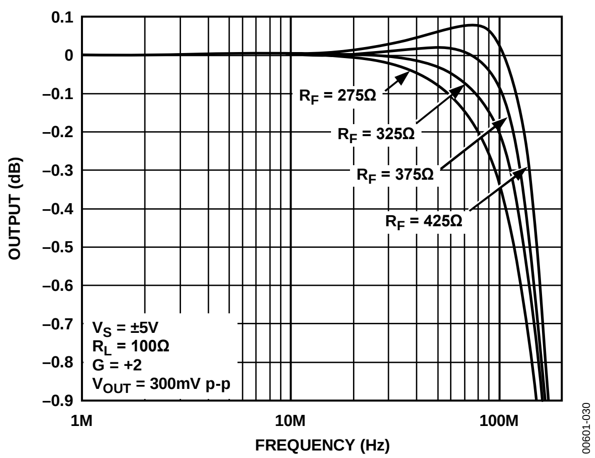

Figure 30. AD9632 0.1 dB Flatness, N Package (for R Package Add 20 Ω to R_F)

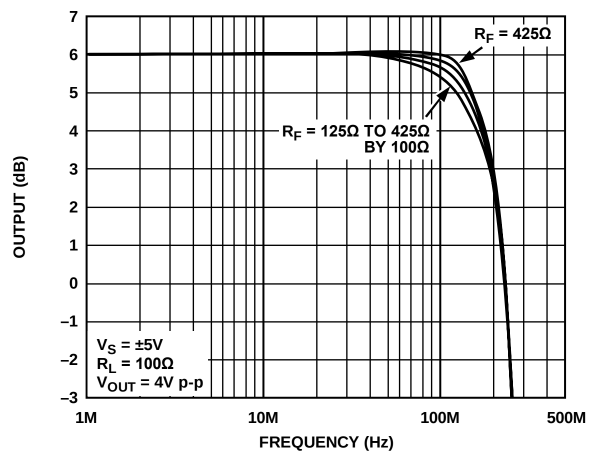

Figure 33. AD9632 Large Signal Frequency Response, G = +2

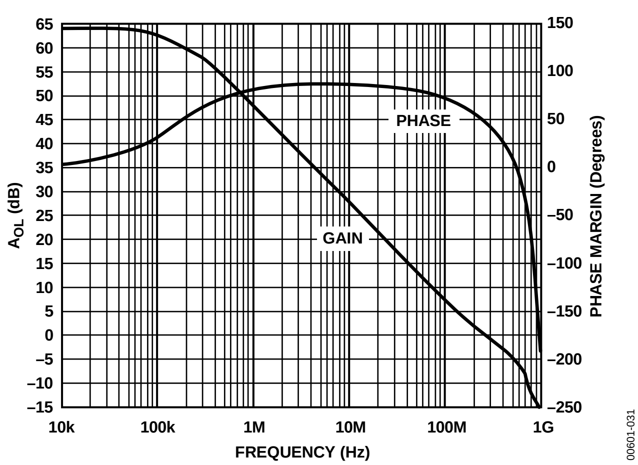

Figure 31. AD9632 Open-Loop Gain and Phase Margin vs. Frequency, R_L = 100 Ω

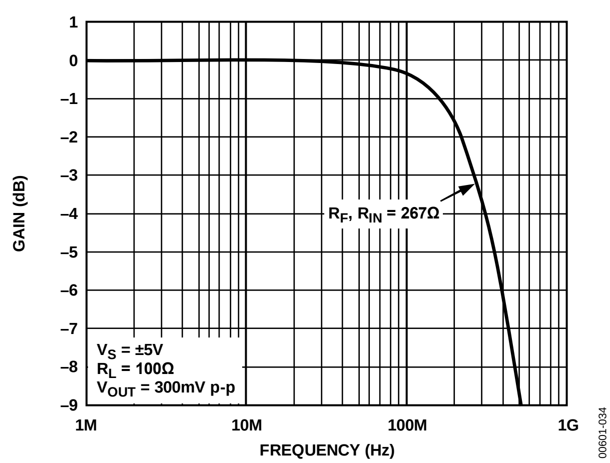

Figure 34. AD9632 Small Signal Frequency Response, G = –1

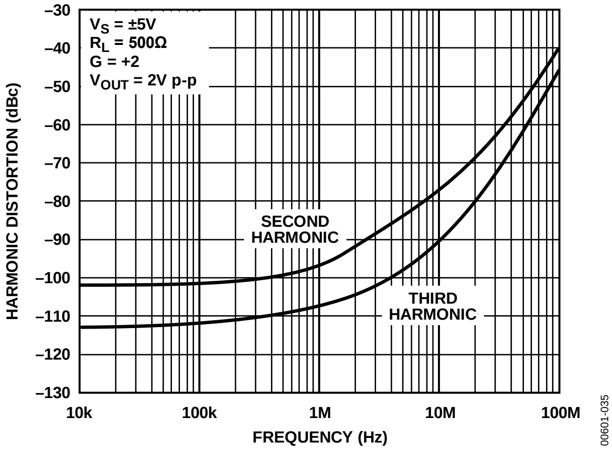

Figure 35. AD9632 Harmonic Distortion vs. Frequency, $R_L = 500\ \Omega$

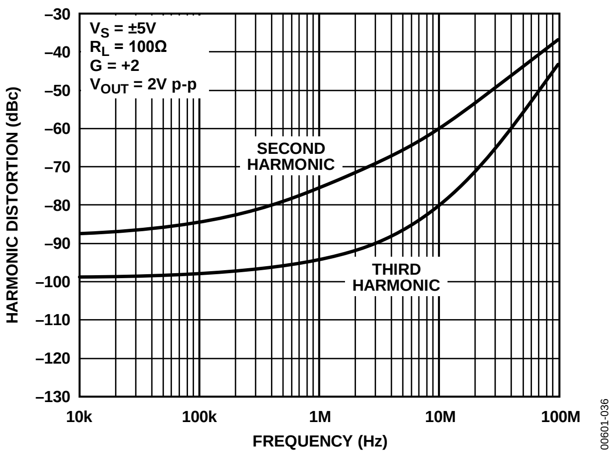

Figure 36. AD9632 Harmonic Distortion vs. Frequency, $R_L = 100\ \Omega$

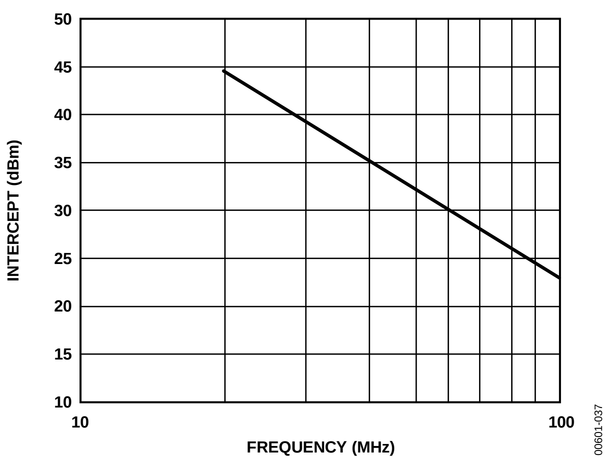

Figure 37. AD9632 Third Order Intercept vs. Frequency

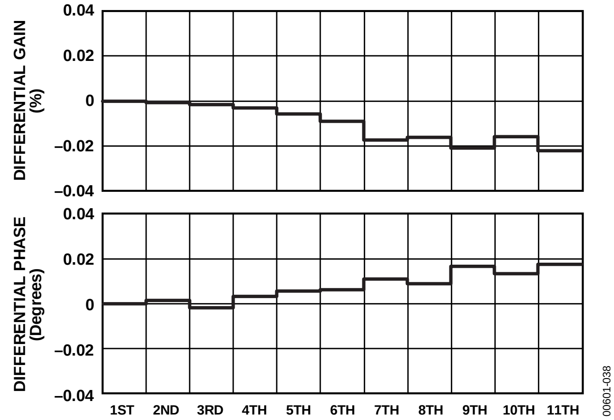

Figure 38. AD9632 Differential Gain and Phase Error $G = +2$, $R_L = 150\ \Omega$

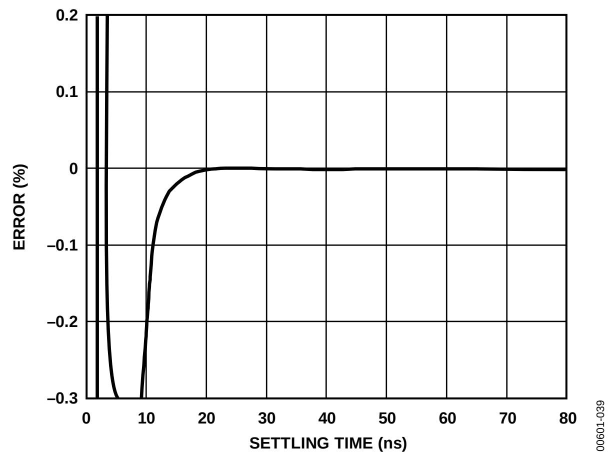

Figure 39. AD9632 Short-Term Settling Time, 2 V Step, $R_L = 100\ \Omega$

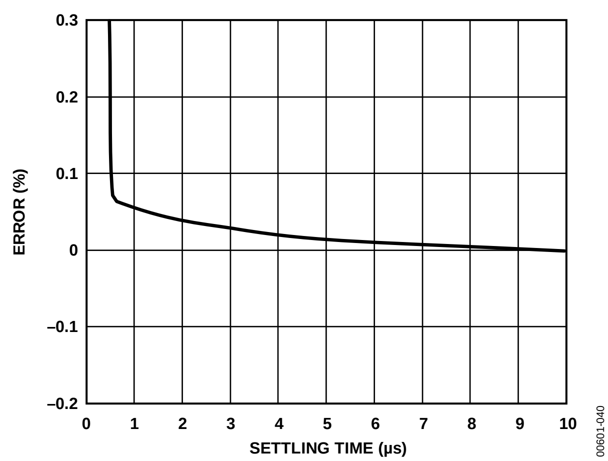

Figure 40. AD9632 Long-Term Settling Time, 2 V Step, $R_L = 100\ \Omega$

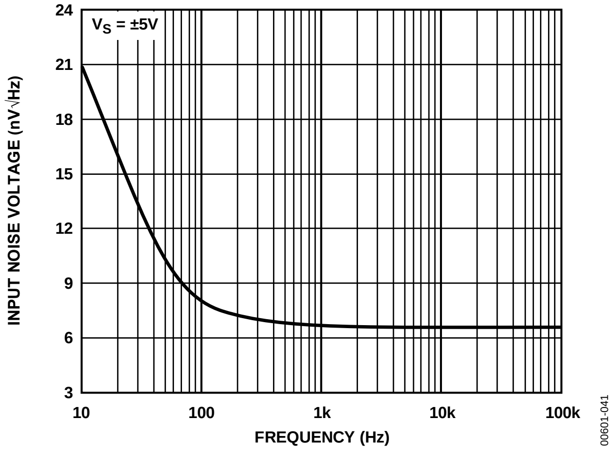

Figure 41. AD9631 Noise vs. Frequency

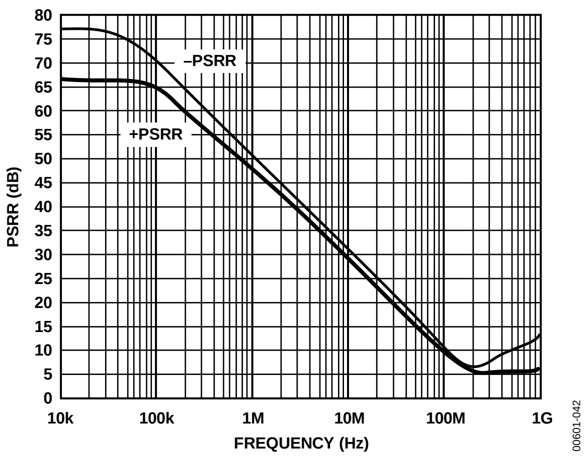

Figure 42. AD9631 PSRR vs. Frequency

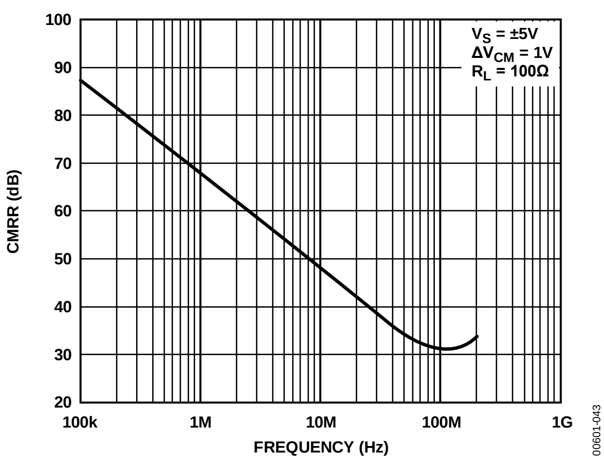

Figure 43. AD9631 CMRR vs. Frequency

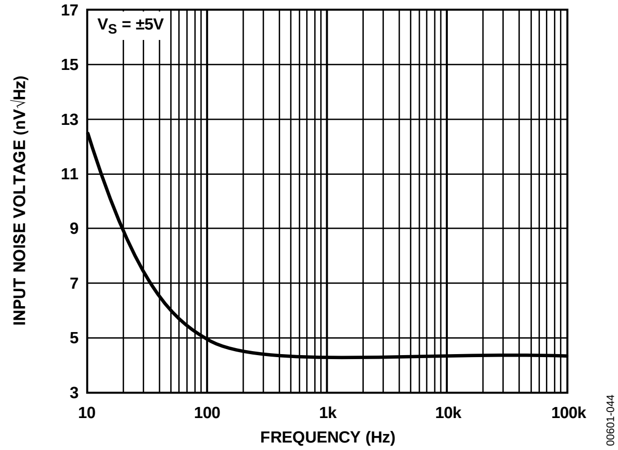

Figure 44. AD9632 Noise vs. Frequency

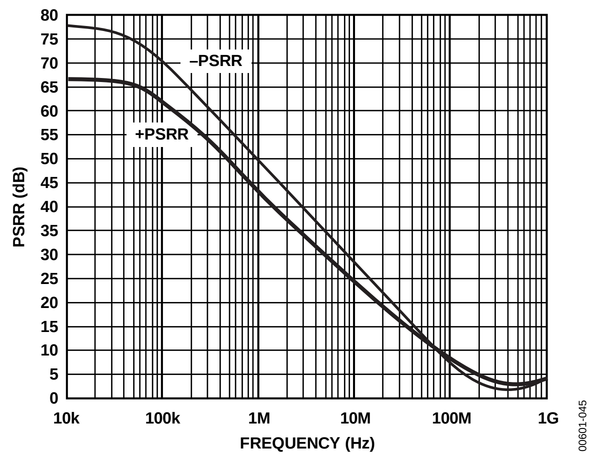

Figure 45. AD9632 PSRR vs. Frequency

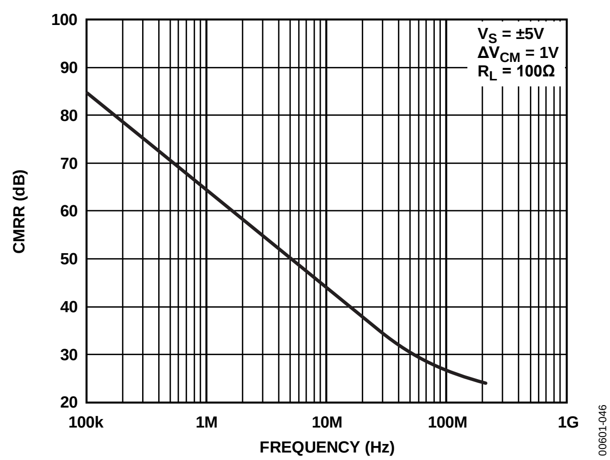

Figure 46. AD9632 CMRR vs. Frequency

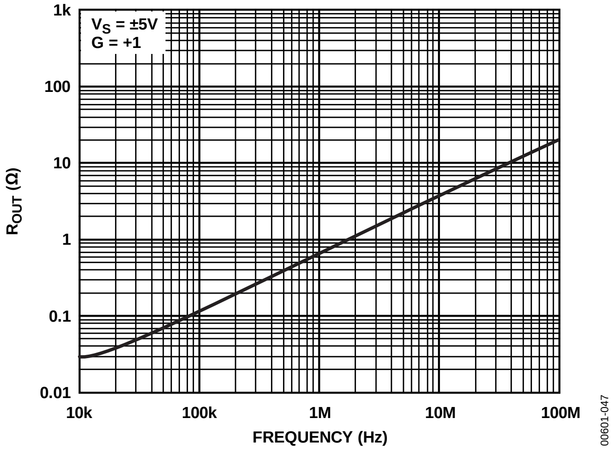

Figure 47. AD9631 Output Resistance vs. Frequency

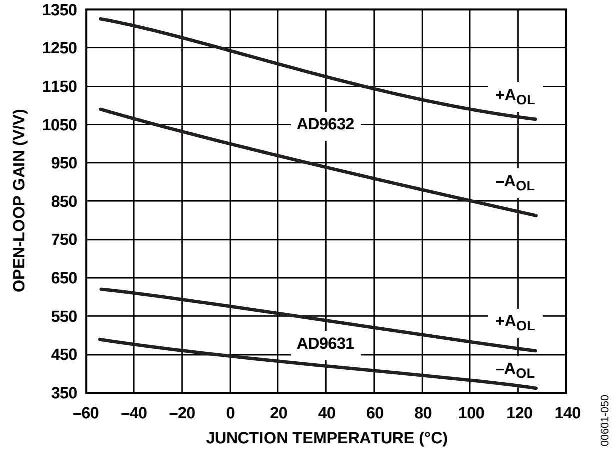

Figure 50. Open-Loop Gain vs. Temperature

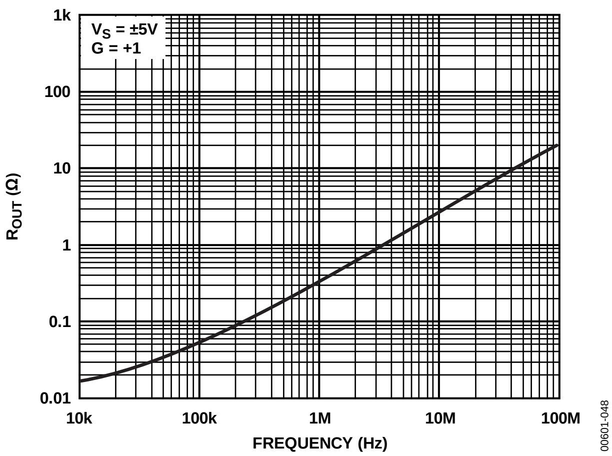

Figure 48. AD9632 Output Resistance vs. Frequency

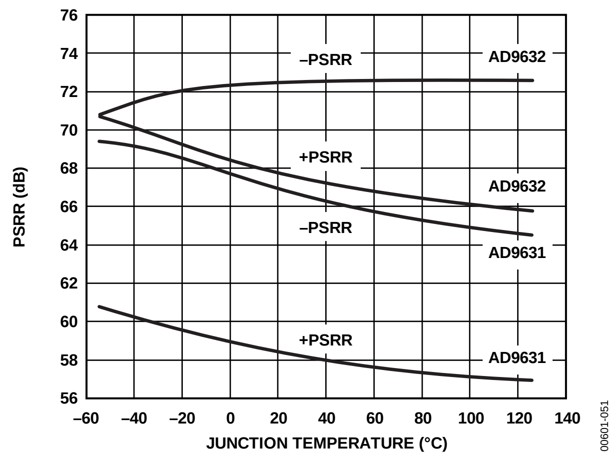

Figure 51. PSRR vs. Temperature

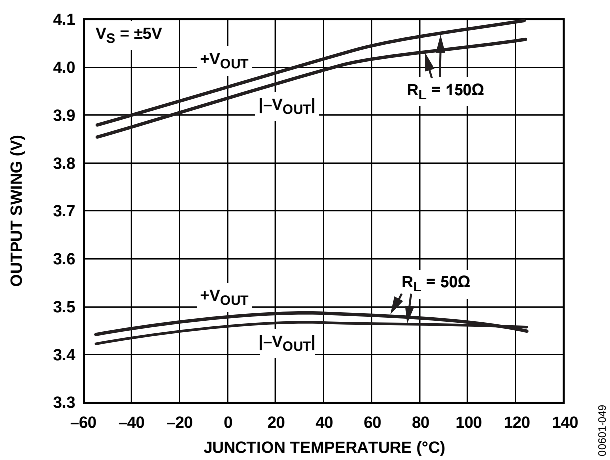

Figure 49. Output Swing vs. Temperature

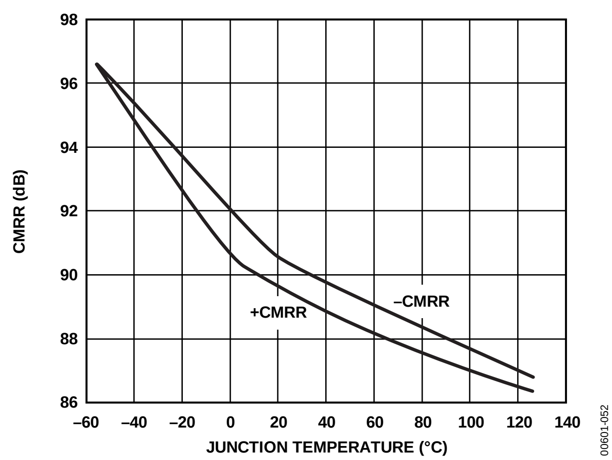

Figure 52. CMRR vs. Temperature

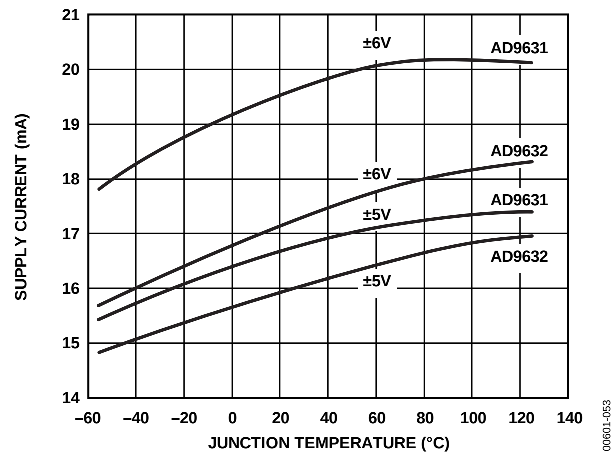

Figure 53. Supply Current vs. Temperature

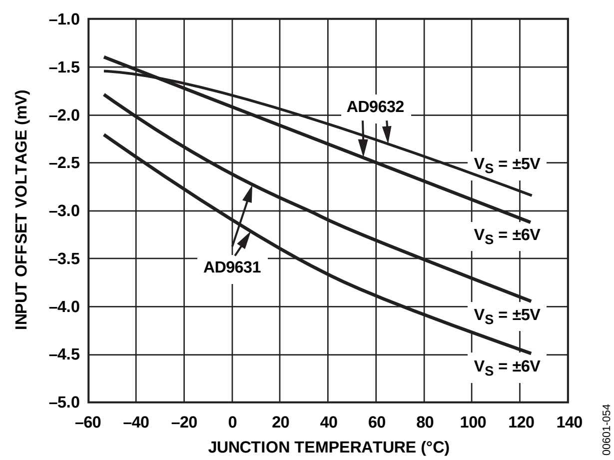

Figure 54. Input Offset Voltage vs. Temperature

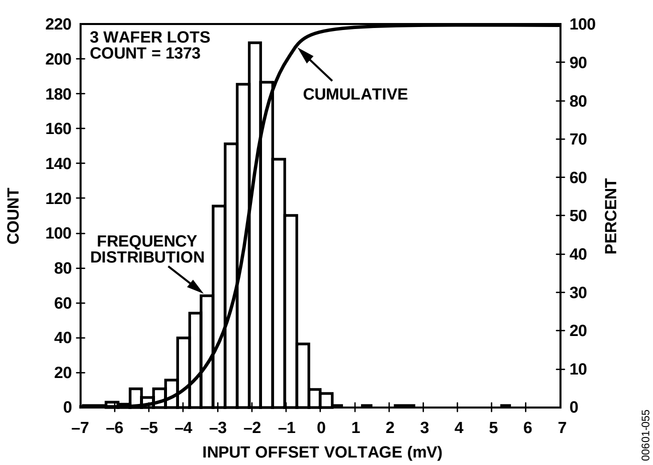

Figure 55. AD9631 Input Offset Voltage Distribution

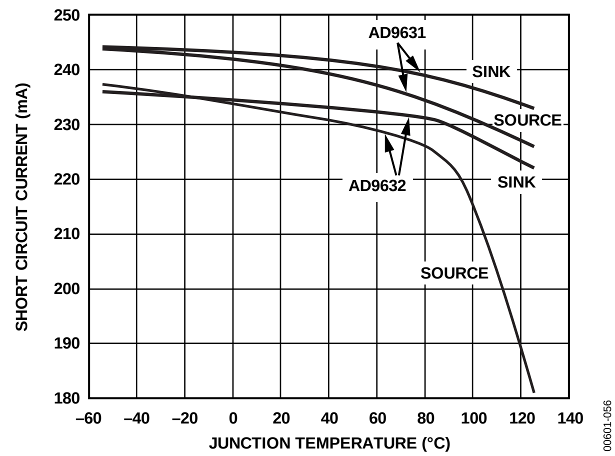

Figure 56. Short Circuit Current vs. Temperature

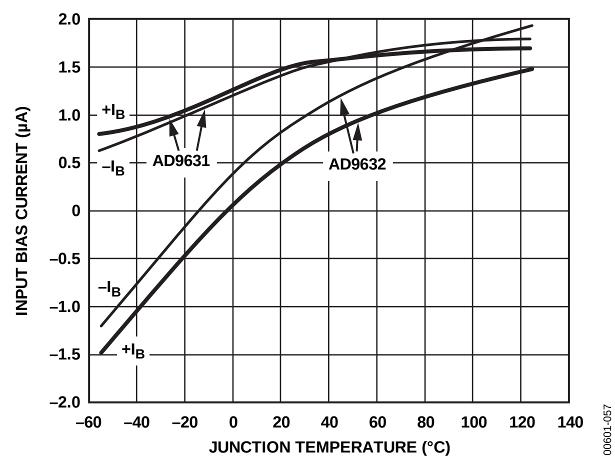

Figure 57. Input Bias Current vs. Temperature

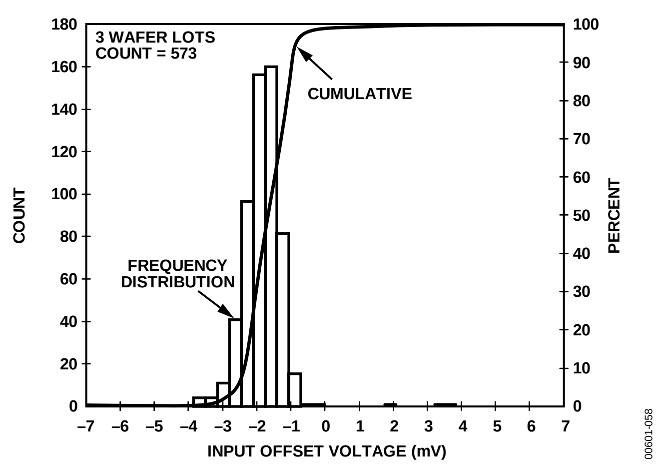

Figure 58. AD9632 Input Offset Voltage Distribution

THEORY OF OPERATION

GENERAL

The AD9631/AD9632 are wide bandwidth, voltage feedback amplifiers. Because their open-loop frequency response follows the conventional 6 dB/octave roll-off, their gain bandwidth product is basically constant. Increasing their closed-loop gain results in a corresponding decrease in small signal bandwidth. This can be observed by noting the bandwidth specification between the AD9631 (gain of +1) and AD9632 (gain of +2). The AD9631/AD9632 typically maintain 65° of phase margin. This high margin minimizes the effects of signal and noise peaking.

FEEDBACK RESISTOR CHOICE

The value of the feedback resistor is critical for optimum performance on the AD9631 (gain of +1) and less critical as the gain increases. Therefore, this section is specifically targeted at the AD9631.

At the minimum stable gain (+1), the AD9631 provides optimum dynamic performance with R_F = 140 Ω. This resistor acts as a parasitic suppressor only against damped RF oscillations that can occur due to lead (input, feedback) inductance and parasitic capacitance. This value of R_F provides the best combination of wide bandwidth, low parasitic peaking, and fast settling time.

In fact, for the same reasons, place a 100 Ω to 130 Ω resistor in series with the positive input for other AD9631 noninverting and all AD9631 inverting configurations. The correct connection is shown in Figure 59 and Figure 60.

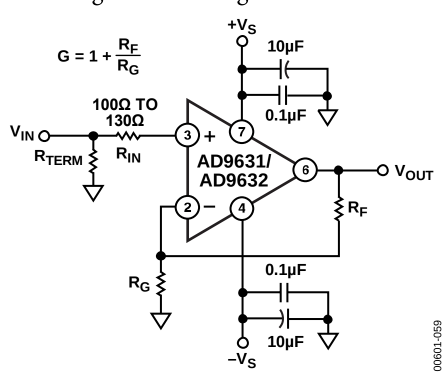

Figure 59. Noninverting Operation

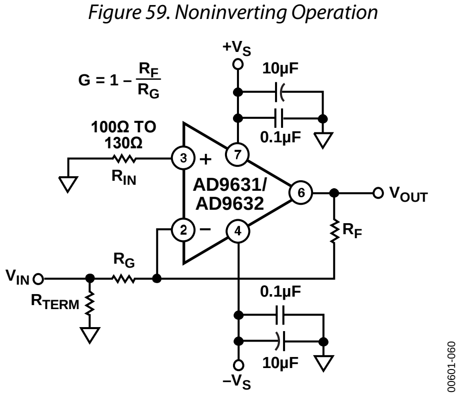

Figure 60. Inverting Operation

When the AD9631 is used in the transimpedance (I to V) mode, such as in photodiode detection, the value of R_F and diode capacitance (C_I) are usually known. Generally, the value of R_F selected will be in the kΩ range, and a shunt capacitor (C_F) across R_F will be required to maintain good amplifier stability. The value of C_F required to maintain optimal flatness (<1 dB peaking) and settling time can be estimated by

$$C_F \cong \left[\left(2\omega_O C_I R_F - 1\right) / \omega_O{}^2 R_F{}^2\right]^{\frac{1}{2}}$$

where:

ω_O is equal to the unity gain bandwidth product of the amplifier in rad/sec.

C_I is the equivalent total input capacitance at the inverting input.

Typically $\omega_O = 800 \times 10^6$ rad/sec (see Figure 19).

As an example, choosing R_F = 10 kΩ and C_I = 5 pF requires C_F to be 1.1 pF (Note that C_I includes both source and parasitic circuit capacitance). The bandwidth of the amplifier can be estimated using C_F:

$$f_{3dB} \cong \frac{1.6}{2\pi R_F C_F}$$

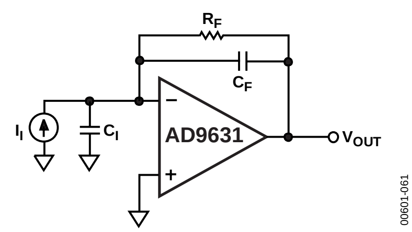

Figure 61. Transimpedance Configuration

For general voltage gain applications, the amplifier bandwidth can be closely estimated as

$$f_{3dB} \cong \frac{\omega_O}{2\pi\left(1 + R_F / R_G\right)}$$

This estimation loses accuracy for gains of +2/−1 or lower due to the damping factor of the amplifier. For these low gain cases, the bandwidth will actually extend beyond the calculated value (see Figure 17 and Figure 29).

As a general rule, Capacitor C_F will not be required if

$$\left(R_F \| R_G\right) \times C_I \le \frac{NG}{4\omega_O}$$

where *NG* is the noise gain (1 + R_F/R_G) of the circuit. For most voltage gain applications, this should be the case.

PULSE RESPONSE

Unlike a traditional voltage feedback amplifier, where the slew speed is dictated by its front end dc quiescent current and gain bandwidth product, the AD9631/AD9632 provide on-demand current that increases proportionally to the input step signal amplitude. This results in slew rates (1300 V/μs) comparable to wideband current feedback designs. This, combined with relatively low input noise current (2.0 pA/√Hz), gives the AD9631/AD9632 the best attributes of both voltage and current feedback amplifiers.

LARGE SIGNAL PERFORMANCE

The outstanding large signal operation of the AD9631 and AD9632 is due to a unique, proprietary design architecture. To maintain this level of performance, the maximum 550 V × MHz product must be observed (for example, @ 100 MHz, $V_{OUT} \leq$ 5.5 V p-p).

POWER SUPPLY BYPASSING

Adequate power supply bypassing can be critical when optimizing the performance of a high frequency circuit. Inductance in the power supply leads can form resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to the load, then bypass capacitors (typically greater than 1 μF) will be required to provide the best settling time and lowest distortion. A parallel combination of at least 4.7 μF, and between 0.1 μF and 0.01 μF, is recommended. Some brands of electrolytic capacitors will require a small series damping resistor ≈4.7 Ω for optimum results.

DRIVING CAPACITIVE LOADS

The AD9631/AD9632 were designed primarily to drive nonreactive loads. If driving loads with a capacitive component is desired, the best frequency response is obtained by the addition of a small series resistance as shown in Figure 62. Figure 63 shows the optimum value for R_{SERIES} vs. capacitive load. It is worth noting that the frequency response of the circuit when driving large capacitive loads will be dominated by the passive roll-off of R_{SERIES} and C_L.

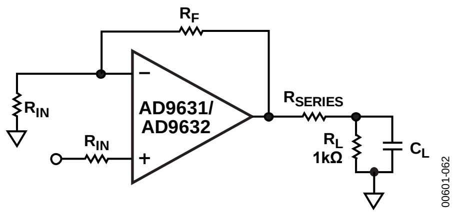

Figure 62. Driving Capacitive Loads

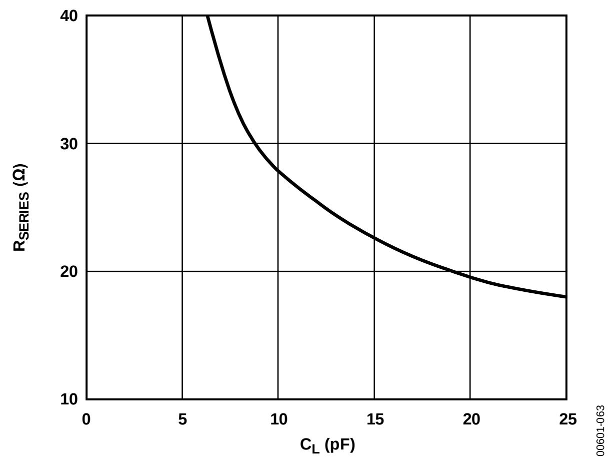

Figure 63. Recommended R_{SERIES} vs. Capacitive Load

APPLICATIONS INFORMATION

The AD9631/AD9632 are voltage feedback amplifiers well suited for applications such as photodetectors, active filters, and log amplifiers. The wide bandwidth (320 MHz), phase margin (65°), low current noise (2.0 pA/√Hz), and slew rate (1300 V/μs) of the devices give higher performance capabilities to these applications over previous voltage feedback designs.

With a settling time of 16 ns to 0.01% and 11 ns to 0.1%, the devices are an excellent choice for DAC I/V conversion. The same characteristics along with low harmonic distortion make them a good choice for ADC buffering/amplification. With superb linearity at relatively high signal frequencies, the AD9631/AD9632 are ideal drivers for ADCs up to 12 bits.

OPERATION AS A VIDEO LINE DRIVER

The AD9631/AD9632 have been designed to offer outstanding performance as video line drivers. The important specifications of differential gain (0.02%) and differential phase (0.02°) meet the most exacting HDTV demands for driving video loads.

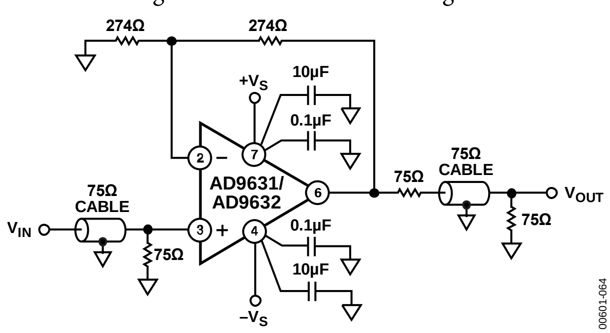

Figure 64. Video Line Driver

ACTIVE FILTERS

The wide bandwidth and low distortion of the AD9631/AD9632 are ideal for the realization of higher bandwidth active filters. These characteristics, while being more common in many current feedback op amps, are offered in the AD9631/AD9632 in a voltage feedback configuration. Many active filter configurations are not realizable with current feedback amplifiers.

A multiple feedback active filter requires a voltage feedback amplifier and is more demanding of op amp performance than other active filter configurations, such as the Sallen-Key. In general, the amplifier should have a bandwidth that is at least 10 times the bandwidth of the filter if problems due to phase shift of the amplifier are to be avoided.

Figure 65 is an example of a 20 MHz low-pass multiple feedback active filter using an AD9632.

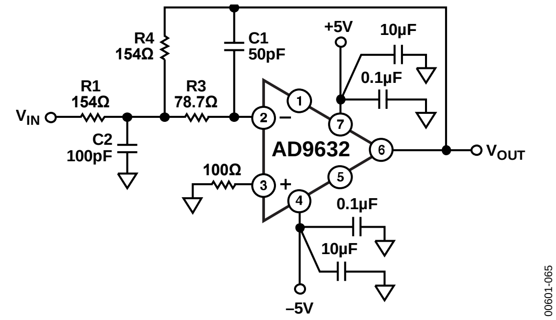

Figure 65. Active Filter Circuit

Choose

F_O = cutoff frequency = 20 MHz

α = damping ratio = $1/Q = 2$

H = absolute value of circuit gain = $\left|\frac{-R4}{R1}\right| = 1$

Then

$$k = 2\pi F_O C1$$

$$C2 = \frac{4C1(H+1)}{\alpha^2}$$

$$R1 = \frac{\alpha}{2HK}$$

$$R3 = \frac{\alpha}{2K(H+1)}$$

$$R4 = H(R1)$$

ANALOG-TO-DIGITAL CONVERTER (ADC) DRIVER

As ADCs move toward higher speeds with higher resolutions, there becomes a need for high performance drivers that will not degrade the analog signal to the converter. It is desirable from a system's standpoint that the ADC be the element in the signal chain that ultimately limits overall distortion. Figure 66 is such an example.

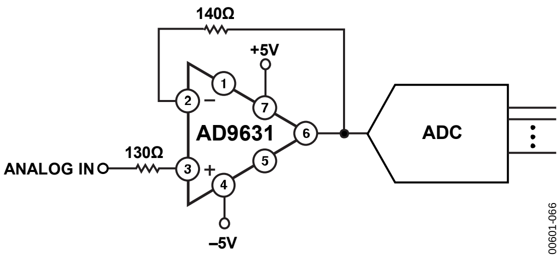

Figure 66. AD9631 Used as Driver for an ADC Signal Chain

LAYOUT CONSIDERATIONS

The specified high speed performance of the AD9631/AD9632 requires careful attention to board layout and component selection. Proper RF design techniques and low-pass parasitic component selection are mandatory.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance path. Remove the ground plane from the area near the input pins to reduce stray capacitance.

Use chip capacitors for supply bypassing (see Figure 59 and Figure 60). Connect one end to the ground plane, and the other within 1/8 inch of each power pin. Connect an additional large (0.47 μF to 10 μF) tantalum electrolytic capacitor in parallel, though not necessarily so close, to supply current for fast, large signal changes at the output.

The feedback resistor should be located close to the inverting input pin to keep the stray capacitance at this node to a minimum. Capacitance variations of less than 1 pF at the inverting input will significantly affect high speed performance.

Use stripline design techniques for long signal traces (greater than about 1 inch). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end.

OUTLINE DIMENSIONS

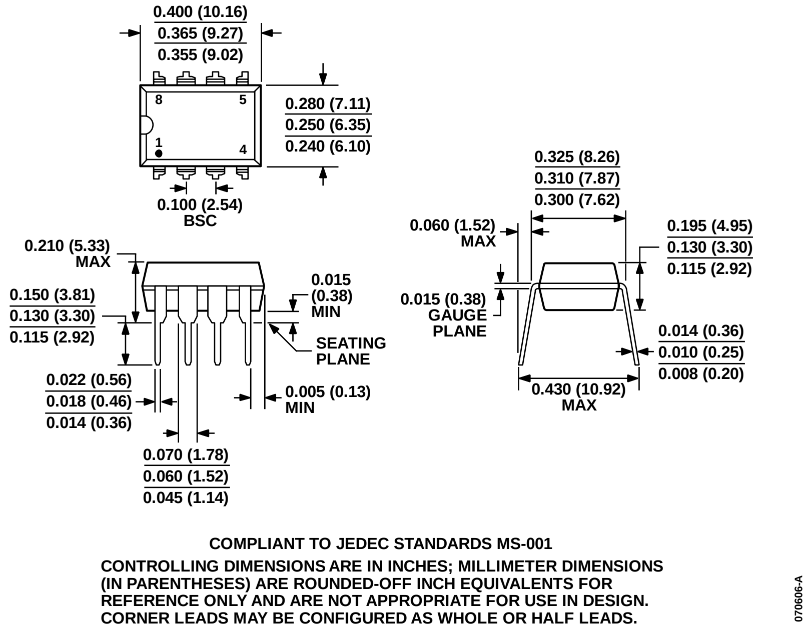

Figure 67. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-8)
Dimensions shown in inches and (millimeters)

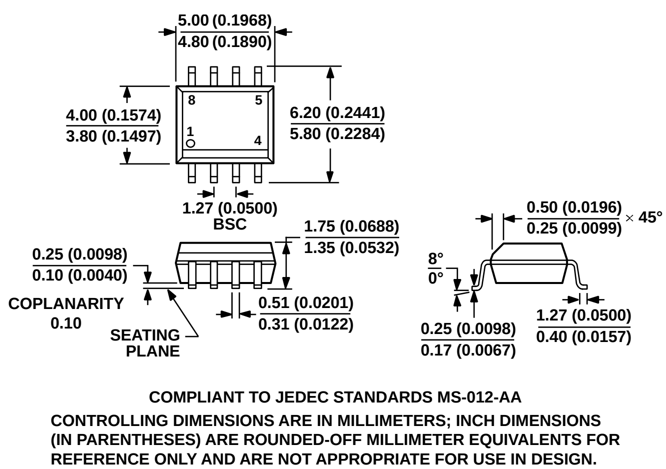

Figure 68. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9631ANZ	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
AD9631AR	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD9631AR-REEL	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD9631AR-REEL7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD9631ARZ	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD9631ARZ-REEL	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD9631ARZ-REEL7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD9631AR-EBZ		AD9631 Evaluation Board	
AD9631ACHIPS		Die	
AD9632ANZ	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
AD9632AR	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD9632ARZ	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD9632ARZ-REEL	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD9632ARZ-REEL7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD9632AR-EBZ		AD9632 Evaluation Board	

[1] Z = RoHS Compliant Part.

D00601-0-2/14(D)

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