Dual, 12-Bit, 80 MSPS/125 MSPS, Serial LVDS 1.8 V Analog-to-Digital Converter

Data Sheet **AD9635**

FEATURES

1.8 V supply operation
Low power: 115 mW per channel at 125 MSPS with scalable power options
SNR = 71 dBFS (to Nyquist)
SFDR = 93 dBc at 70 MHz
DNL = −0.1 LSB to +0.2 LSB (typical); INL = ±0.4 LSB (typical)
Serial LVDS (ANSI-644, default) and low power, reduced range option (similar to IEEE 1596.3)
650 MHz full power analog bandwidth
2 V p-p input voltage range
Serial port control
- **Full chip and individual channel power-down modes**
- **Flexible bit orientation**
- **Built-in and custom digital test pattern generation**
- **Clock divider**
- **Programmable output clock and data alignment**
- **Programmable output resolution**
- **Standby mode**

APPLICATIONS

Communications
Diversity radio systems
Multimode digital receivers
GSM, EDGE, W-CDMA, LTE, CDMA2000, WiMAX, TD-SCDMA
I/Q demodulation systems
Smart antenna systems
Broadband data applications
Battery-powered instruments
Handheld scope meters
Portable medical imaging and ultrasound
Radar/LIDAR

GENERAL DESCRIPTION

The AD9635 is a dual, 12-bit, 80 MSPS/125 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit designed for low cost, low power, small size, and ease of use. The product operates at a conversion rate of up to 125 MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications.

FUNCTIONAL BLOCK DIAGRAM

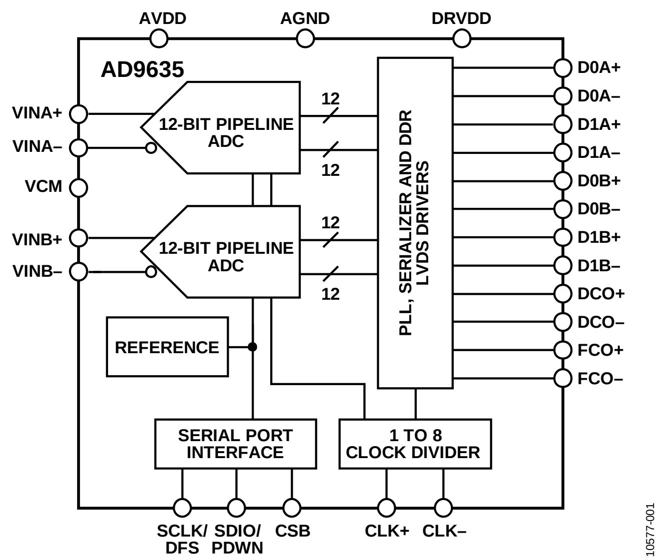

Figure 1.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. A data clock output (DCO) for capturing data on the output and a frame clock output (FCO) for signaling a new output byte are provided. Individual channel power-down is supported; the AD9635 typically consumes less than 2 mW in the full power-down state. The ADC provides several features designed to maximize flexibility and minimize system cost, such as programmable output clock and data alignment and digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

The AD9635 is available in a RoHS-compliant, 32-lead LFCSP. It is specified over the industrial temperature range of −40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Small Footprint. Two ADCs are contained in a small, space-saving package.
2. Low Power. The AD9635 uses 115 mW/channel at 125 MSPS with scalable power options.
3. Pin Compatibility with the AD9645, a 14-Bit Dual ADC.
4. Ease of Use. A data clock output (DCO) operates at frequencies of up to 500 MHz and supports double data rate (DDR) operation.
5. User Flexibility. SPI control offers a wide range of flexible features to meet specific system requirements.

Rev. B Document Feedback

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REVISION HISTORY

10/15—Rev. A to Rev. B

Changed t_{SAMPLE}/16 to t_{SAMPLE}/12, AD9516 to AD9516-0/ AD9516-1/AD9516-2/AD9516-3/AD9516-4/AD9516-5, and AD9517 to AD9517-0/AD9517-1/AD9517-2/AD9517-3/ AD9517-4 ... Throughout
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6/12—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, unless otherwise noted.

Table 1.

Parameter[1]	Temp	AD9635-80 Min	AD9635-80 Typ	AD9635-80 Max	AD9635-125 Min	AD9635-125 Typ	AD9635-125 Max	Unit
RESOLUTION		12			12			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full	−0.6	−0.3	+0.1	−0.6	−0.3	+0.2	% FSR
Offset Matching	Full	−0.2	+0.1	+0.4	−0.2	+0.1	+0.4	% FSR
Gain Error	Full	−4.0	−0.8	+2.1	−4.7	−0.4	+4.8	% FSR
Gain Matching	Full		0.5	2.4		0.6	2.9	% FSR
Differential Nonlinearity (DNL)	Full	−0.2		+0.4	−0.3		+0.6	LSB
	25°C		−0.1 to +0.2			−0.1 to +0.2		LSB
Integral Nonlinearity (INL)	Full	−0.7		+0.7	−1.1		+1.1	LSB
	25°C		±0.3			±0.4		LSB
TEMPERATURE DRIFT								
Offset Error	Full		2.9			3.7		ppm/°C
INTERNAL VOLTAGE REFERENCE								
Output Voltage (1 V Mode)	Full	0.98	1.0	1.02	0.98	1.0	1.02	V
Load Regulation at 1.0 mA (V_{REF} = 1 V)	25°C		2			2		mV
Input Resistance	25°C		7.5			7.5		kΩ
INPUT-REFERRED NOISE								
V_{REF} = 1.0 V	25°C		0.41			0.42		LSB rms
ANALOG INPUTS								
Differential Input Voltage (V_{REF} = 1 V)	Full		2			2		V p-p
Common-Mode Voltage	Full		0.9			0.9		V
Common-Mode Range	25°C	0.5		1.3	0.5		1.3	V
Differential Input Resistance	25°C		5.2			5.2		kΩ
Differential Input Capacitance	25°C		3.5			3.5		pF
POWER SUPPLY								
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
I_{AVDD}[2]	Full		57	61		75	81	mA
I_{DRVDD} (ANSI-644 Mode)[2]	Full		45	47		52	55	mA
I_{DRVDD} (Reduced Range Mode)[2]	25°C		36			43		mA
TOTAL POWER CONSUMPTION								
DC Input	Full		174	186		215	232	mW
Sine Wave Input (Two Channels; Includes Output Drivers in ANSI-644 Mode)	Full		184	194		229	245	mW
Sine Wave Input (Two Channels; Includes Output Drivers in Reduced Range Mode)	25°C		167			212		mW
Power-Down	25°C		2			2		mW
Standby[3]	Full		91	99		114	124	mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured with a low input frequency, full-scale sine wave on both channels.
[3] Can be controlled via the SPI.

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, unless otherwise noted.

Table 2.

Parameter[1]	Temp	AD9635-80 Min	AD9635-80 Typ	AD9635-80 Max	AD9635-125 Min	AD9635-125 Typ	AD9635-125 Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)								
f_{IN} = 9.7 MHz	25°C		71.8			71.5		dBFS
f_{IN} = 30.5 MHz	25°C		71.7			71.5		dBFS
f_{IN} = 70 MHz	Full	70.6	71.2		70.1	71.1		dBFS
f_{IN} = 139.5 MHz	25°C		69.9			70.2		dBFS
f_{IN} = 200.5 MHz	25°C		68.4			68.9		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)								
f_{IN} = 9.7 MHz	25°C		71.8			71.5		dBFS
f_{IN} = 30.5 MHz	25°C		71.6			71.5		dBFS
f_{IN} = 70 MHz	Full	70.5	71.2		69.7	71.1		dBFS
f_{IN} = 139.5 MHz	25°C		69.6			70.2		dBFS
f_{IN} = 200.5 MHz	25°C		68.2			68.7		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 9.7 MHz	25°C		11.6			11.6		Bits
f_{IN} = 30.5 MHz	25°C		11.6			11.6		Bits
f_{IN} = 70 MHz	Full	11.4	11.5		11.3	11.5		Bits
f_{IN} = 139.5 MHz	25°C		11.3			11.4		Bits
f_{IN} = 200.5 MHz	25°C		11.0			11.1		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 9.7 MHz	25°C		93			92		dBc
f_{IN} = 30.5 MHz	25°C		90			93		dBc
f_{IN} = 70 MHz	Full	82	94		82	93		dBc
f_{IN} = 139.5 MHz	25°C		81			92		dBc
f_{IN} = 200.5 MHz	25°C		82			83		dBc
WORST HARMONIC (SECOND OR THIRD)								
f_{IN} = 9.7 MHz	25°C		−93			−92		dBc
f_{IN} = 30.5 MHz	25°C		−90			−93		dBc
f_{IN} = 70 MHz	Full		−94	−85		−93	−82	dBc
f_{IN} = 139.5 MHz	25°C		−81			−92		dBc
f_{IN} = 200.5 MHz	25°C		−82			−83		dBc
WORST OTHER HARMONIC OR SPUR								
f_{IN} = 9.7 MHz	25°C		−96			−95		dBc
f_{IN} = 30.5 MHz	25°C		−95			−95		dBc
f_{IN} = 70 MHz	Full		−94	−82		−94	−82	dBc
f_{IN} = 139.5 MHz	25°C		−95			−93		dBc
f_{IN} = 200.5 MHz	25°C		−92			−89		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)—AIN1 AND AIN2 = −7.0 dBFS								
f_{IN1} = 70.5 MHz, f_{IN2} = 72.5 MHz	25°C		−92			−92		dBc
CROSSTALK[2]	25°C		−97			−97		dB
CROSSTALK (OVERRANGE CONDITION)[3]	25°C		−97			−97		dB
POWER SUPPLY REJECTION RATIO (PSRR)[4]								
AVDD	25°C		44			43		dB
DRVDD	25°C		59			66		dB
ANALOG INPUT BANDWIDTH, FULL POWER	25°C		650			650		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Crosstalk is measured at 70 MHz with −1.0 dBFS analog input on one channel and no input on the adjacent channel.
[3] Overrange condition is specified with 3 dB of the full-scale input range.
[4] PSRR is measured by injecting a sinusoidal signal at 10 MHz to the power supply pin and measuring the output spur on the FFT. PSRR is calculated as the ratio of the amplitude of the spur voltage over the amplitude of the pin voltage, expressed in decibels (dB).

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, unless otherwise noted.

Table 3.

Parameter[1]	Temp	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[2]	Full	0.2		3.6	V p-p
Input Voltage Range	Full	AGND − 0.2		AVDD + 0.2	V
Input Common-Mode Voltage	Full		0.9		V
Input Resistance (Differential)	25°C		15		kΩ
Input Capacitance	25°C		4		pF
LOGIC INPUT (SCLK/DFS)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUT (CSB)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		2		pF
LOGIC INPUT (SDIO/PDWN)					
Logic 1 Voltage	Full	1.2		AVDD + 0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		5		pF
LOGIC OUTPUT (SDIO/PDWN)[3]					
Logic 1 Voltage (I_{OH} = 800 μA)	Full		1.79		V
Logic 0 Voltage (I_{OL} = 50 μA)	Full			0.05	V
DIGITAL OUTPUTS (D0x±, D1x±), ANSI-644					
Logic Compliance			LVDS		
Differential Output Voltage Magnitude (V_{OD})	Full	290	345	400	mV
Output Offset Voltage (V_{OS})	Full	1.15	1.25	1.35	V
Output Coding (Default)			Twos complement		
DIGITAL OUTPUTS (D0x±, D1x±), LOW POWER, REDUCED SIGNAL OPTION					
Logic Compliance			LVDS		
Differential Output Voltage Magnitude (V_{OD})	Full	160	200	230	mV
Output Offset Voltage (V_{OS})	Full	1.15	1.25	1.35	V
Output Coding (Default)			Twos complement		

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Specified for LVDS and LVPECL only.
[3] Specified for 13 SDIO/PDWN pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, 2 V p-p differential input, 1.0 V internal reference, AIN = −1.0 dBFS, unless otherwise noted.

Table 4.

Parameter[1, 2]	Temp	Min	Typ	Max	Unit
CLOCK[3]					
Input Clock Rate	Full	10		1000	MHz
Conversion Rate[4]	Full	10		80/125	MSPS
Clock Pulse Width High (t_{EH})	Full		6.25/4.00		ns
Clock Pulse Width Low (t_{EL})	Full		6.25/4.00		ns
OUTPUT PARAMETERS[3]					
Propagation Delay (t_{PD})	Full	1.5	2.3	3.1	ns
Rise Time (t_R) (20% to 80%)	Full		300		ps
Fall Time (t_F) (20% to 80%)	Full		300		ps
FCO Propagation Delay (t_{FCO})	Full	1.5	2.3	3.1	ns
DCO Propagation Delay (t_{CPD})[5]	Full		t_{FCO} + (t_{SAMPLE}/12)		ns
DCO to Data Delay (t_{DATA})[5]	Full	(t_{SAMPLE}/12) − 300	t_{SAMPLE}/12	(t_{SAMPLE}/12) + 300	ps
DCO to FCO Delay (t_{FRAME})[5]	Full	(t_{SAMPLE}/12) − 300	t_{SAMPLE}/12	(t_{SAMPLE}/12) + 300	ps
Lane Delay (t_{LD})			90		ps
Data-to-Data Skew ($t_{DATA-MAX}$ − $t_{DATA-MIN}$)	Full		±50	±200	ps
Wake-Up Time (Standby)	25°C		250		ns
Wake-Up Time (Power-Down)[6]	25°C		375		µs
Pipeline Latency	Full		16		Clock cycles
APERTURE					
Aperture Delay (t_A)	25°C		1		ns
Aperture Uncertainty (Jitter, t_J)	25°C		174		fs rms
Out-of-Range Recovery Time	25°C		1		Clock cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Measured on standard FR-4 material.
[3] Can be adjusted via the SPI. The conversion rate is the clock rate after the divider.
[4] The maximum conversion rate is based on two-lane output mode. See the Digital Outputs and Timing section for the maximum conversion rate in one-lane output mode.
[5] t_{SAMPLE}/12 is based on the number of bits in two LVDS data lanes. t_{SAMPLE} = 1/f_S.
[6] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Description	Limit	Unit
SPI TIMING REQUIREMENTS	See Figure 68		
t_{DS}	Setup time between the data and the rising edge of SCLK	2	ns min
t_{DH}	Hold time between the data and the rising edge of SCLK	2	ns min
t_{CLK}	Period of the SCLK	40	ns min
t_S	Setup time between CSB and SCLK	2	ns min
t_H	Hold time between CSB and SCLK	2	ns min
t_{HIGH}	SCLK pulse width high	10	ns min
t_{LOW}	SCLK pulse width low	10	ns min
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 68)	10	ns min
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 68)	10	ns min

Timing Diagrams

Refer to the Memory Map Register Descriptions section and Table 20 for SPI register settings.

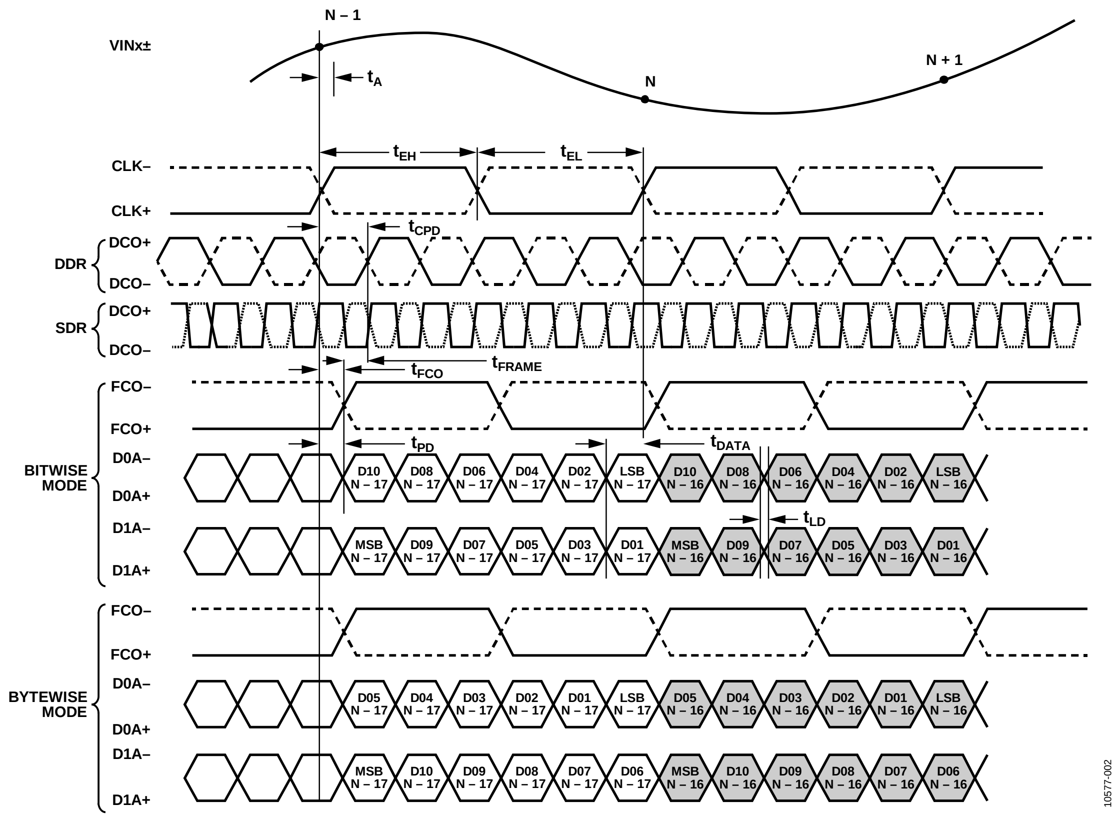


Figure 2. 12-Bit DDR/SDR, Two-Lane, 1× Frame Mode (Default)

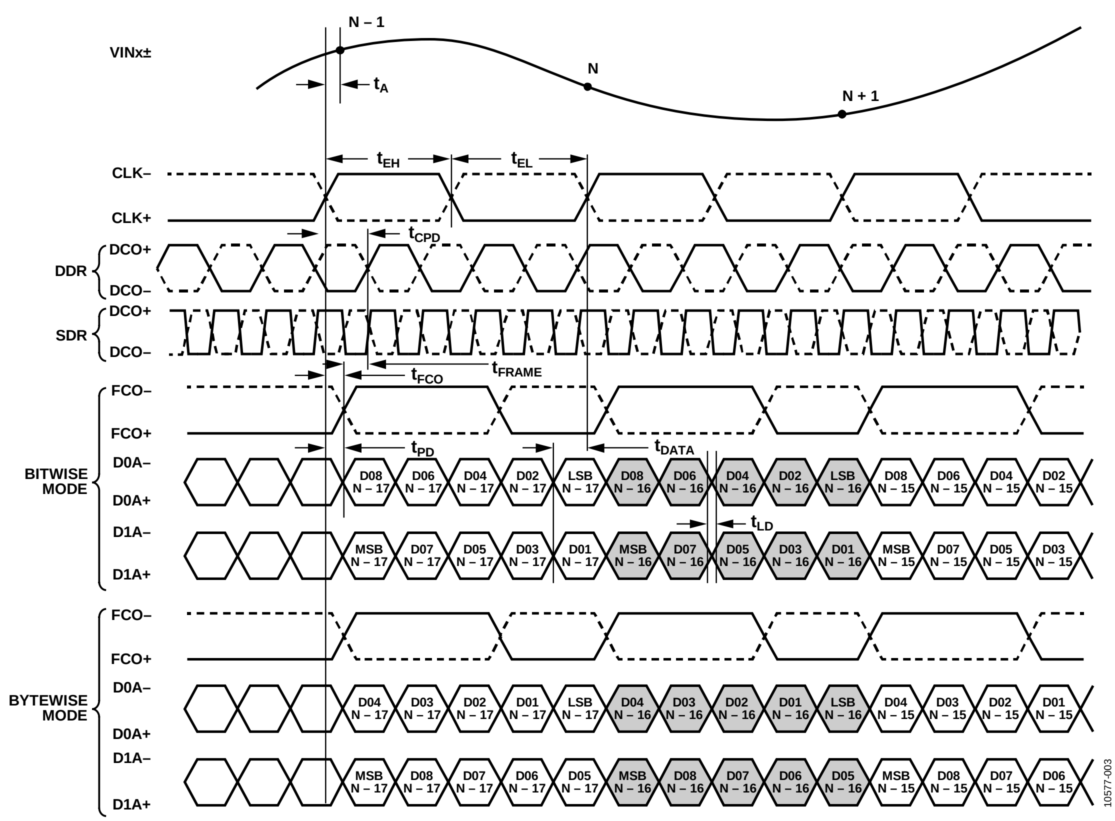


Figure 3. 10-Bit DDR/SDR, Two-Lane, 1× Frame Mode

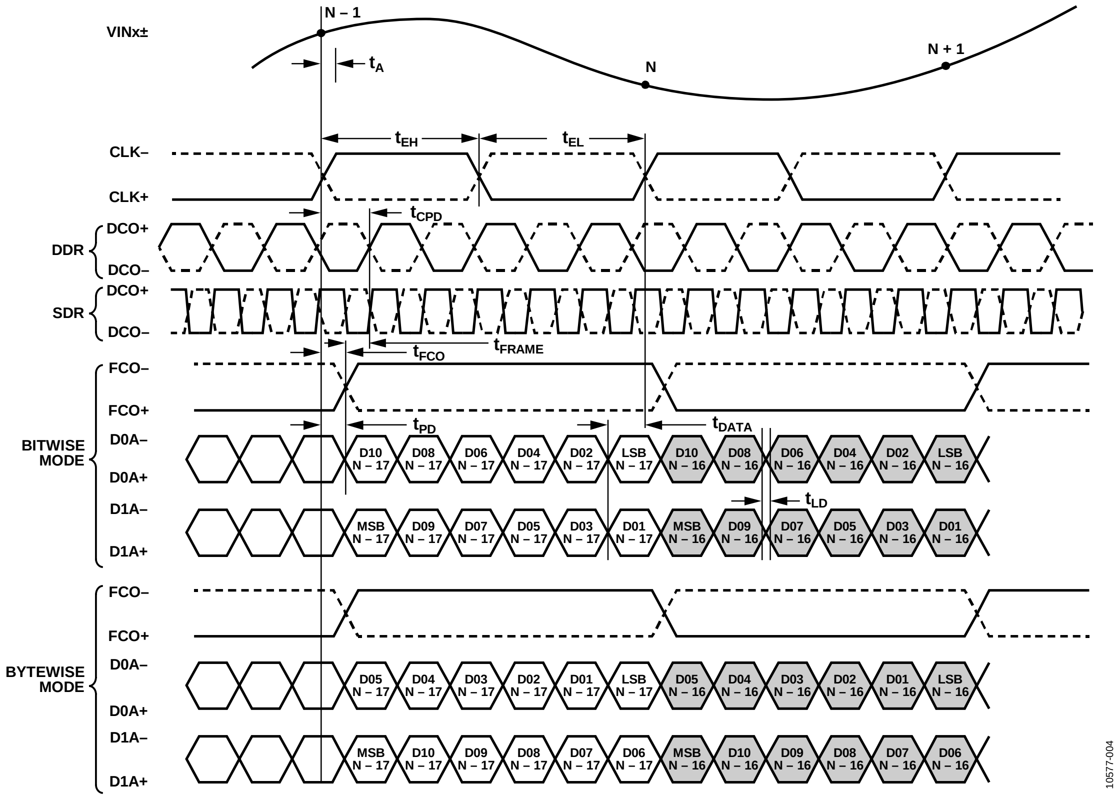


Figure 4. 12-Bit DDR/SDR, Two-Lane, 2× Frame Mode

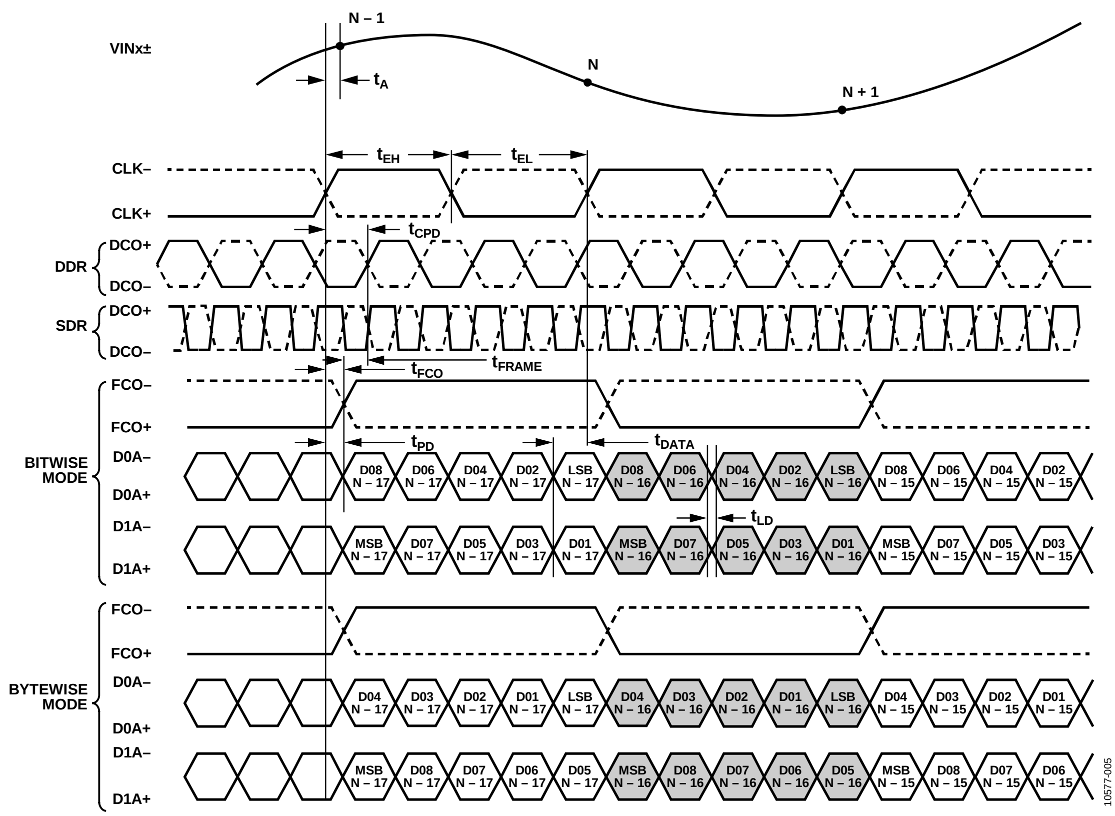


Figure 5. 10-Bit DDR/SDR, Two-Lane, 2× Frame Mode

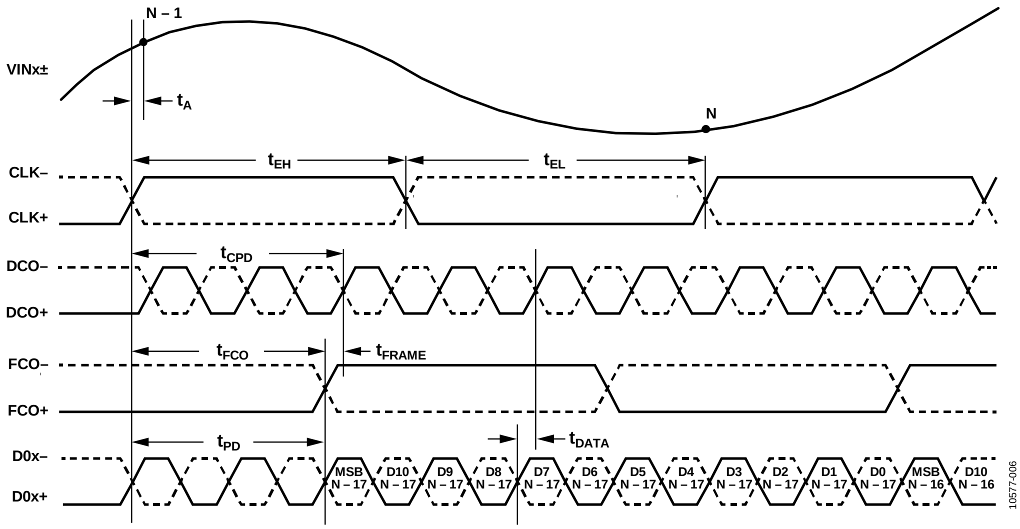


Figure 6. Wordwise DDR, One-Lane, 1× Frame, 12-Bit Output Mode

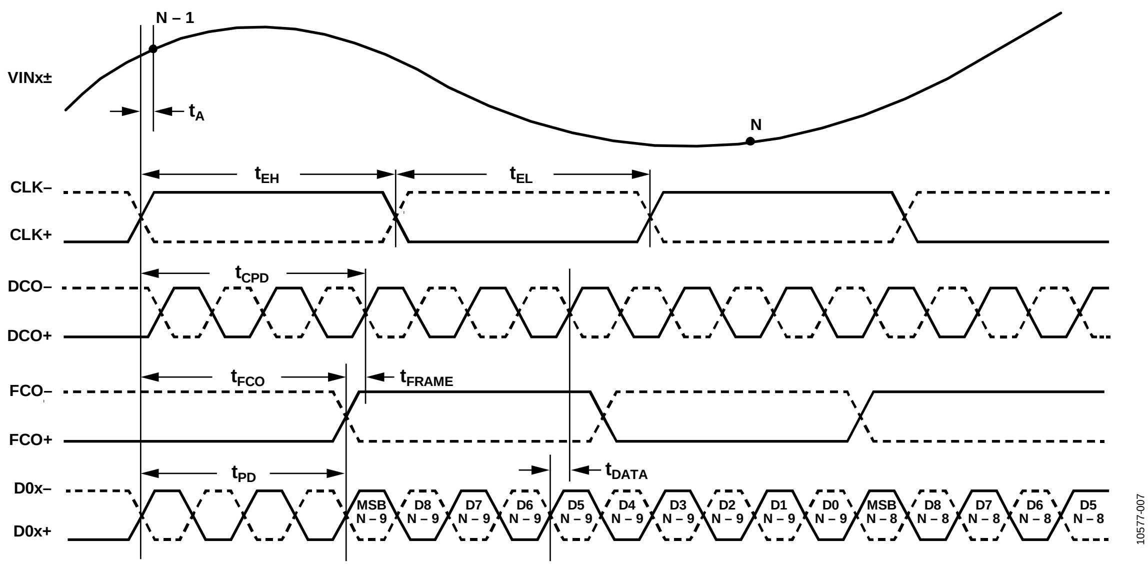


Figure 7. Wordwise DDR, One-Lane, 1× Frame, 10-Bit Output Mode

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
Digital Outputs to AGND (D0x±, D1x±, DCO+, DCO−, FCO+, FCO−)	−0.3 V to +2.0 V
CLK+, CLK− to AGND	−0.3 V to +2.0 V
VINx+, VINx− to AGND	−0.3 V to +2.0 V
SCLK/DFS, SDIO/PDWN, CSB to AGND	−0.3 V to +2.0 V
RBIAS to AGND	−0.3 V to +2.0 V
VREF to AGND	−0.3 V to +2.0 V
VCM to AGND	−0.3 V to +2.0 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

The exposed paddle is the only ground connection on the chip. The exposed paddle must be soldered to the AGND plane of the user's circuit board. Soldering the exposed paddle to the user's board also increases the reliability of the solder joints and maximizes the thermal capability of the package.

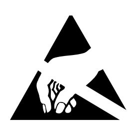
Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA} [1, 2]	θ_{JC} [1, 3]	θ_{JB} [1, 4]	Ψ_{JT} [1, 2]	Unit
32-Lead LFCSP, 5 mm × 5 mm	0	37.1	3.1	20.7	0.3	°C/W
	1.0	32.4			0.5	°C/W
	2.5	29.1			0.8	°C/W

[1] Per JEDEC JESD51-7, plus JEDEC JESD51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-STD 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown in Table 7, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

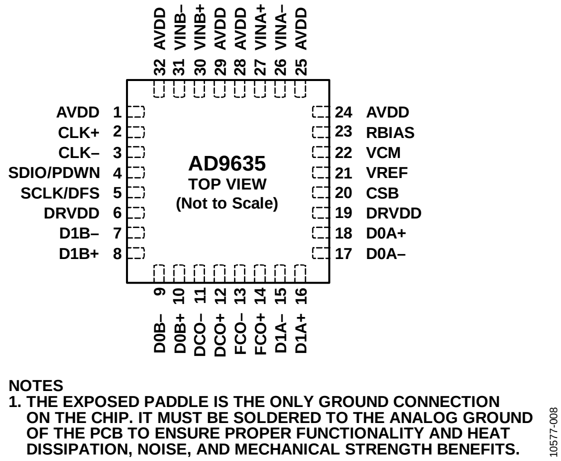


Figure 8. Pin Configuration, Top View

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	AGND, Exposed Pad	The exposed paddle is the only ground connection on the chip. It must be soldered to the analog ground of the PCB to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits.
1, 24, 25, 28 29, 32	AVDD	1.8 V Supply Pins for ADC Analog Core Domain.
2, 3	CLK+, CLK−	Differential Encode Clock for LVPECL, LVDS, or 1.8 V CMOS Inputs.
4	SDIO/PDWN	Data Input/Output in SPI Mode (SDIO). Bidirectional SPI data I/O with 30 kΩ internal pull-down. Power-Down in Non-SPI Mode (PDWN). Static control of chip power-down with 30 kΩ internal pull-down.
5	SCLK/DFS	SPI Clock Input in SPI Mode (SCLK). 30 kΩ internal pull-down. Data Format Select in Non-SPI Mode (DFS). Static control of data output format, with 30 kΩ internal pull-down. DFS high = twos complement output; DFS low = offset binary output.
6, 19	DRVDD	1.8 V Supply Pins for Output Driver Domain.
7, 8	D1B−, D1B+	Channel B Digital Outputs.
9, 10	D0B−, D0B+	Channel B Digital Outputs.
11, 12	DCO−, DCO+	Data Clock Outputs.
13, 14	FCO−, FCO+	Frame Clock Outputs.
15, 16	D1A−, D1A+	Channel A Digital Outputs.
17, 18	D0A−, D0A+	Channel A Digital Outputs.
20	CSB	SPI Chip Select. Active low enable with 15 kΩ internal pull-up.
21	VREF	1.0 V Voltage Reference Output.
22	VCM	Analog Output Voltage at Mid AVDD Supply. Sets the common-mode voltage of the analog inputs.
23	RBIAS	Sets the analog current bias. Connect this pin to a 10 kΩ (1% tolerance) resistor to ground.
26, 27	VINA−, VINA+	Channel A ADC Analog Inputs.
30, 31	VINB+, VINB−	Channel B ADC Analog Inputs.

TYPICAL PERFORMANCE CHARACTERISTICS

AD9635-80

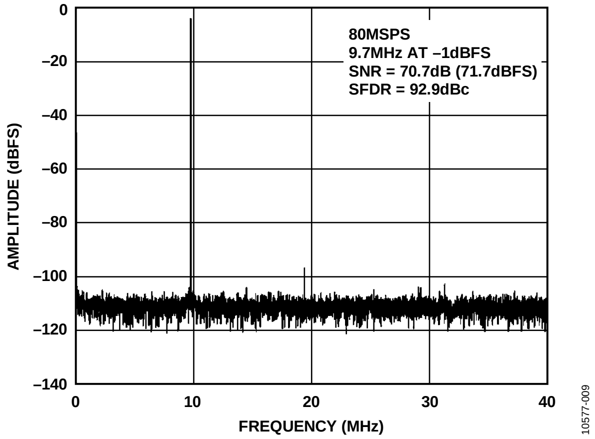


Figure 9. Single-Tone 16k FFT with f_{IN} = 9.7 MHz, f_{SAMPLE} = 80 MSPS

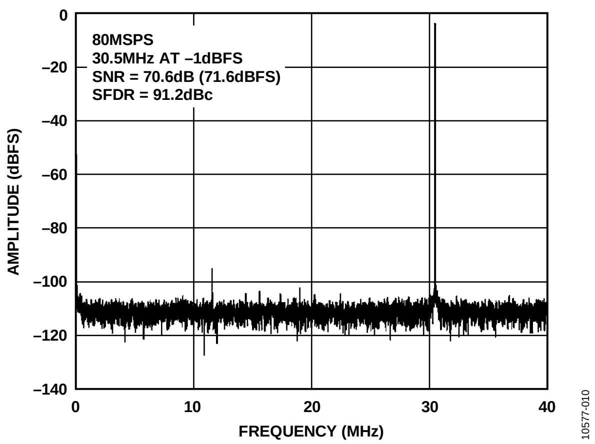


Figure 10. Single-Tone 16k FFT with f_{IN} = 30.5 MHz, f_{SAMPLE} = 80 MSPS

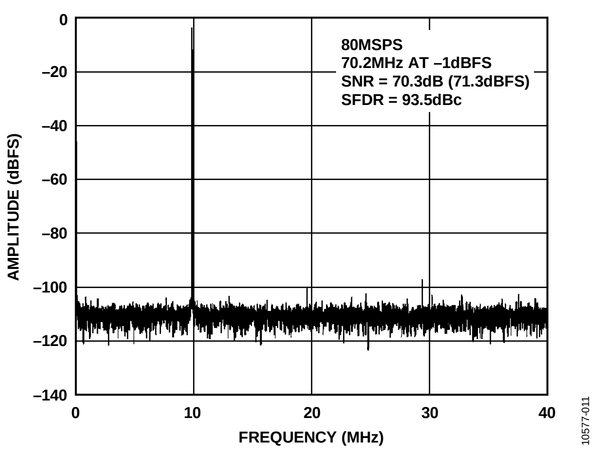


Figure 11. Single-Tone 16k FFT with f_{IN} = 70.2 MHz, f_{SAMPLE} = 80 MSPS

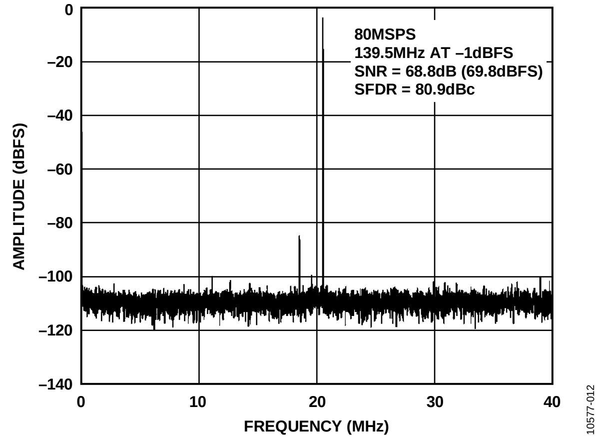


Figure 12. Single-Tone 16k FFT with f_{IN} = 139.5 MHz, f_{SAMPLE} = 80 MSPS

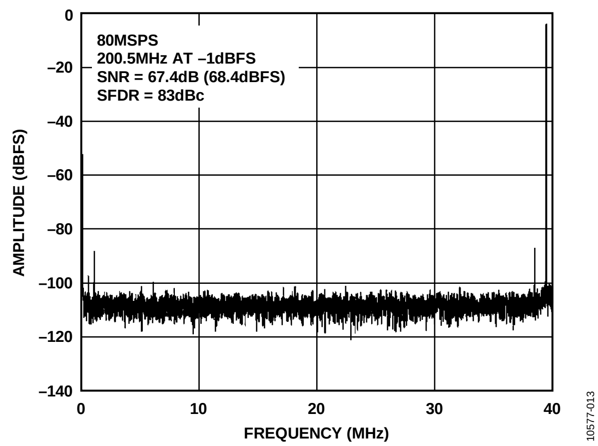


Figure 13. Single-Tone 16k FFT with f_{IN} = 200.5 MHz, f_{SAMPLE} = 80 MSPS

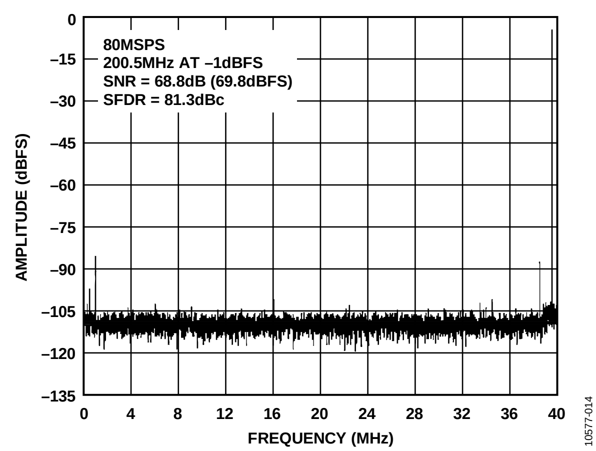


Figure 14. Single-Tone 16k FFT with f_{IN} = 200.5 MHz, f_{SAMPLE} = 80 MSPS, Clock Divide = Divide-by-8

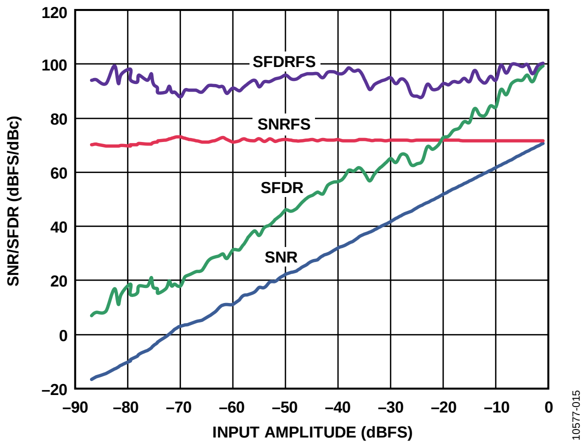


Figure 15. SNR/SFDR vs. Analog Input Level; f_{IN} = 9.7 MHz, f_{SAMPLE} = 80 MSPS

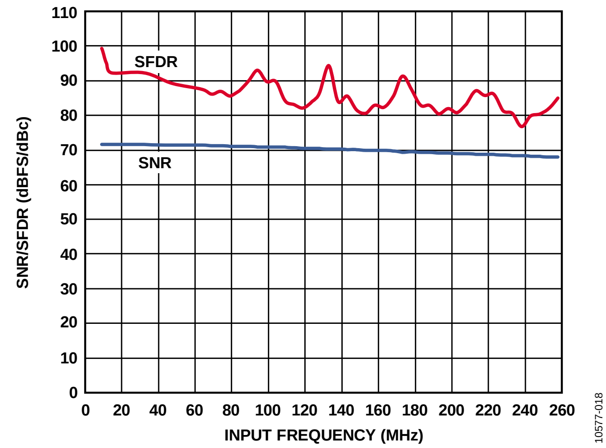


Figure 18. SNR/SFDR vs. f_{IN}; f_{SAMPLE} = 80 MSPS

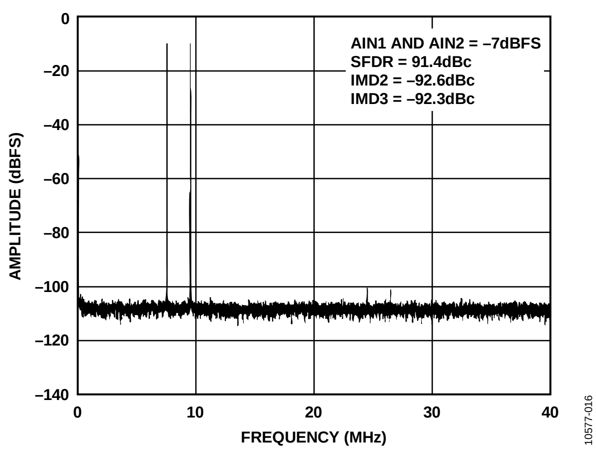


Figure 16. Two-Tone 16k FFT with f_{IN1} = 70.5 MHz and f_{IN2} = 72.5 MHz, f_{SAMPLE} = 80 MSPS

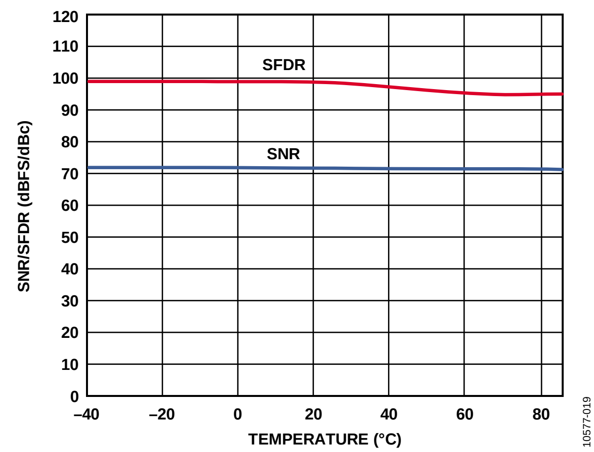


Figure 19. SNR/SFDR vs. Temperature; f_{IN} = 9.7 MHz, f_{SAMPLE} = 80 MSPS

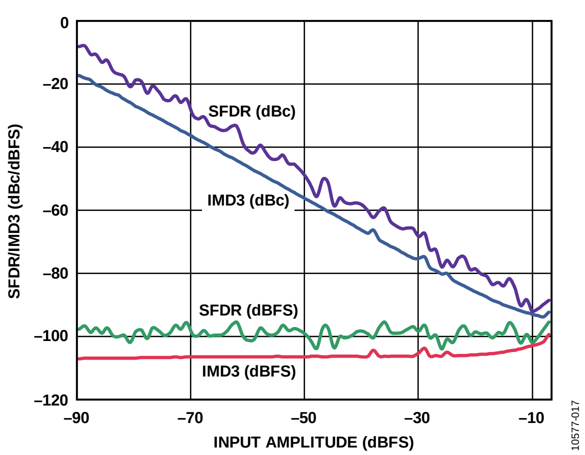


Figure 17. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with f_{IN1} = 70.5 MHz and f_{IN2} = 72.5 MHz, f_{SAMPLE} = 80 MSPS

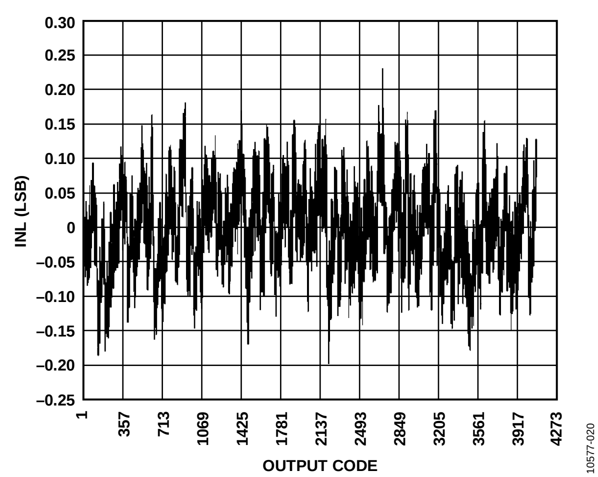


Figure 20. INL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 80 MSPS

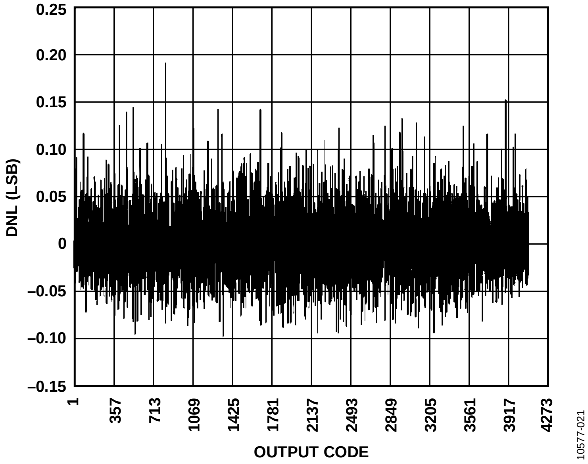


Figure 21. DNL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 80 MSPS

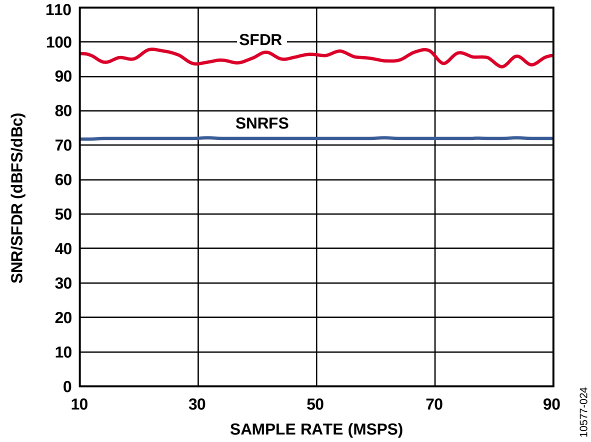


Figure 24. SNR/SFDR vs. Sample Rate; f_{IN} = 9.7 MHz, f_{SAMPLE} = 80 MSPS

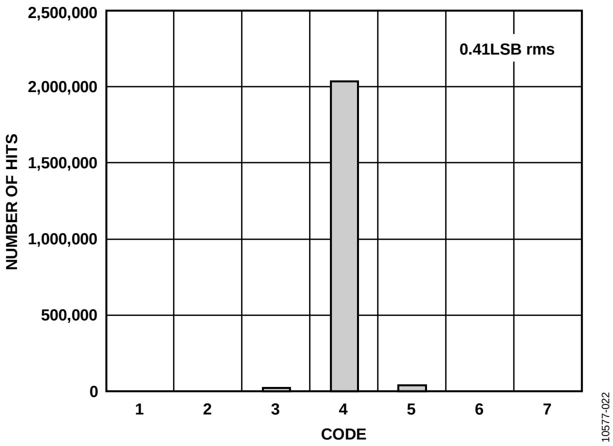


Figure 22. Input Referred Noise Histogram; f_{SAMPLE} = 80 MSPS

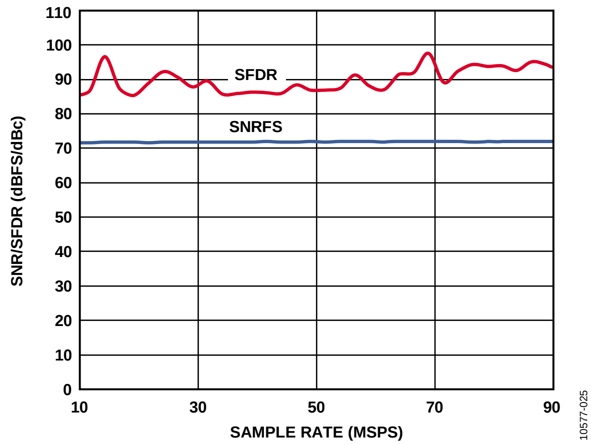


Figure 25. SNR/SFDR vs. Sample Rate; f_{IN} = 70 MHz, f_{SAMPLE} = 80 MSPS

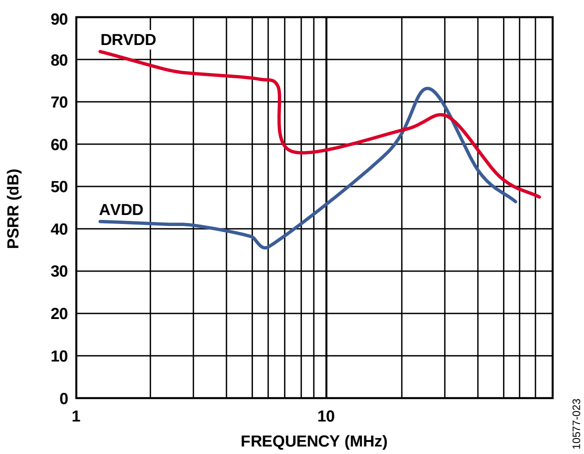


Figure 23. PSRR vs. Frequency; f_{CLK} = 125 MHz, f_{SAMPLE} = 80 MSPS

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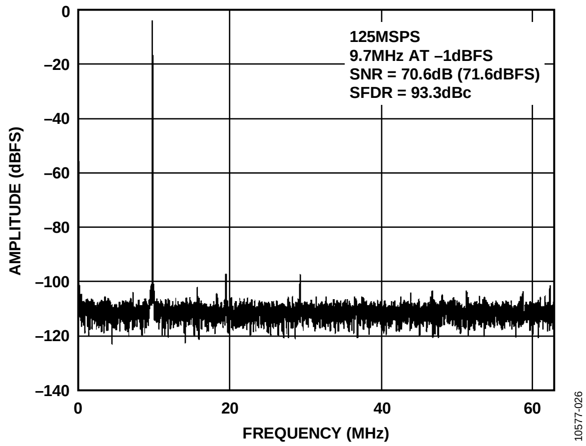

Figure 26. Single-Tone 16k FFT with f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS

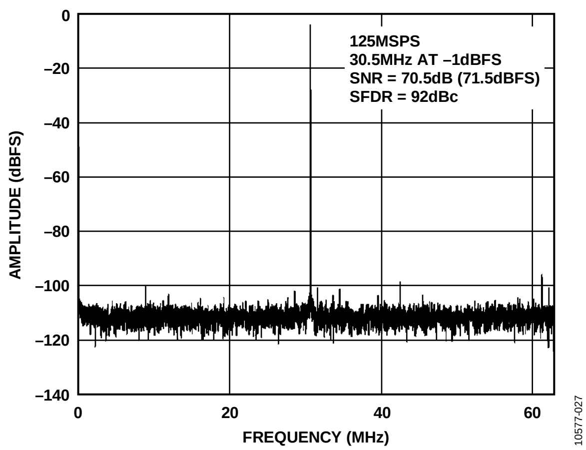

Figure 27. Single-Tone 16k FFT with f_{IN} = 30.5 MHz, f_{SAMPLE} = 125 MSPS

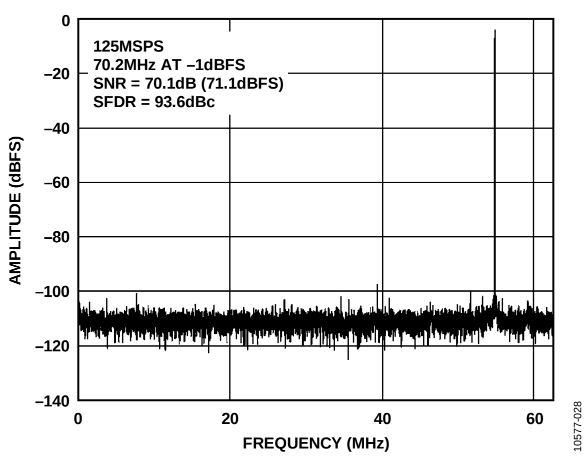

Figure 28. Single-Tone 16k FFT with f_{IN} = 70.2 MHz, f_{SAMPLE} = 125 MSPS

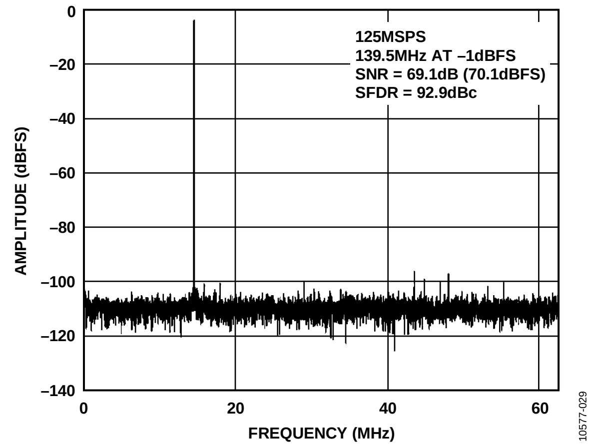

Figure 29. Single-Tone 16k FFT with f_{IN} = 139.5 MHz, f_{SAMPLE} = 125 MSPS

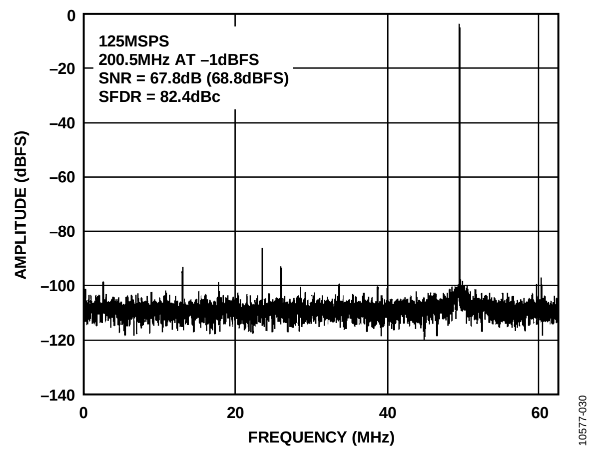

Figure 30. Single-Tone 16k FFT with f_{IN} = 200.5 MHz, f_{SAMPLE} = 125 MSPS

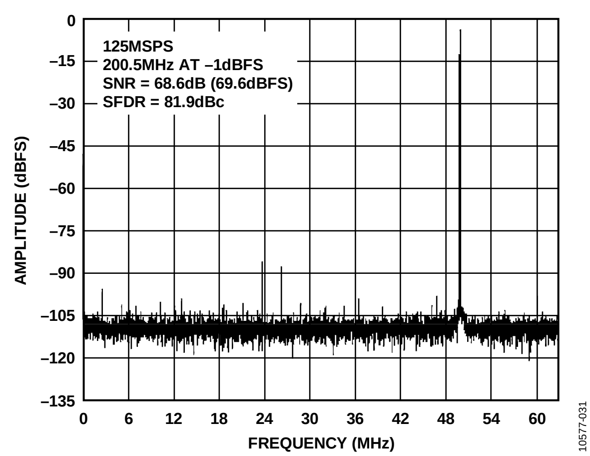

Figure 31. Single-Tone 16k FFT with f_{IN} = 200.5 MHz, f_{SAMPLE} = 125 MSPS, Clock Divide = Divide-by-8

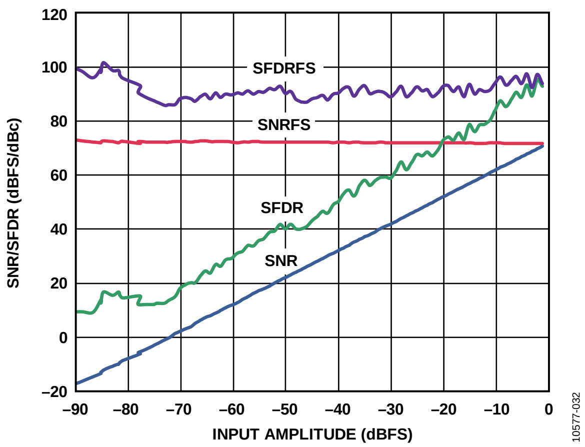

Figure 32. SNR/SFDR vs. Analog Input Level; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS

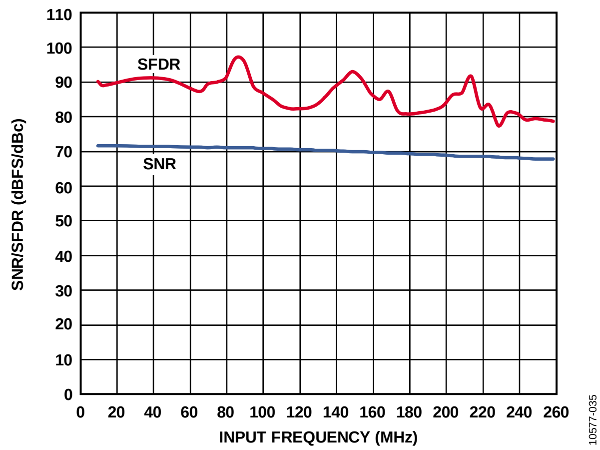

Figure 35. SNR/SFDR vs. f_{IN}; f_{SAMPLE} = 125 MSPS

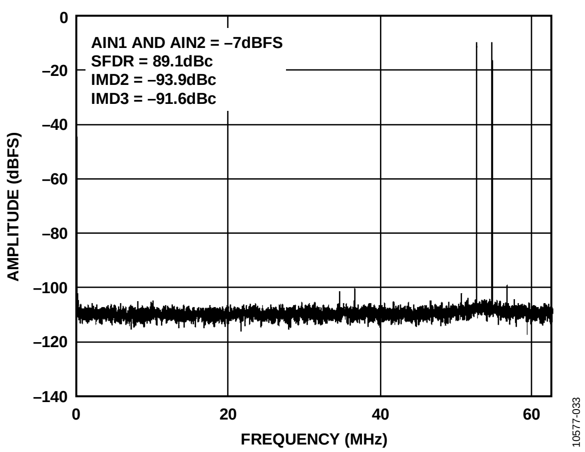

Figure 33. Two-Tone 16k FFT with f_{IN1} = 70.5 MHz and f_{IN2} = 72.5 MHz, f_{SAMPLE} = 125 MSPS

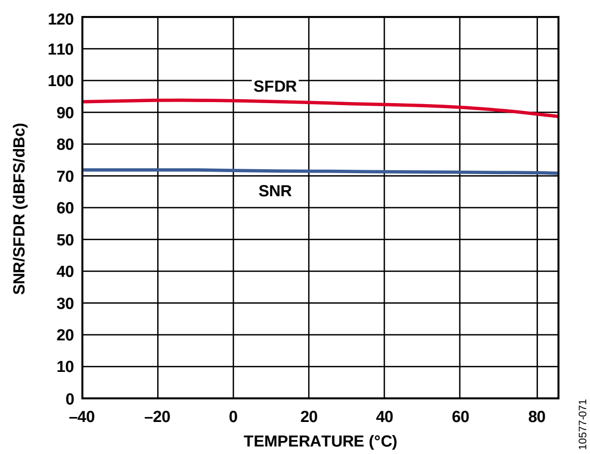

Figure 36. SNR/SFDR vs. Temperature; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS

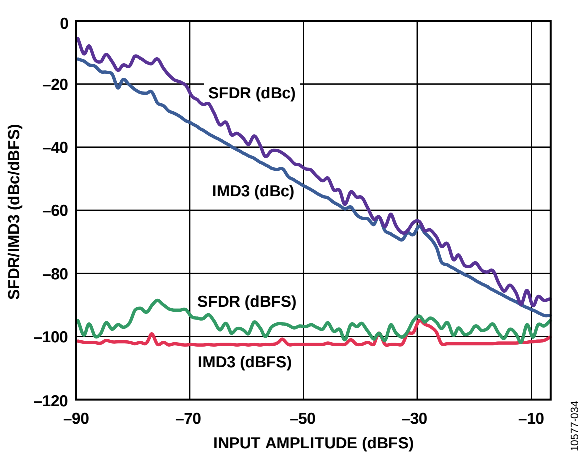

Figure 34. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with f_{IN1} = 70.5 MHz and f_{IN2} = 72.5 MHz, f_{SAMPLE} = 125 MSPS

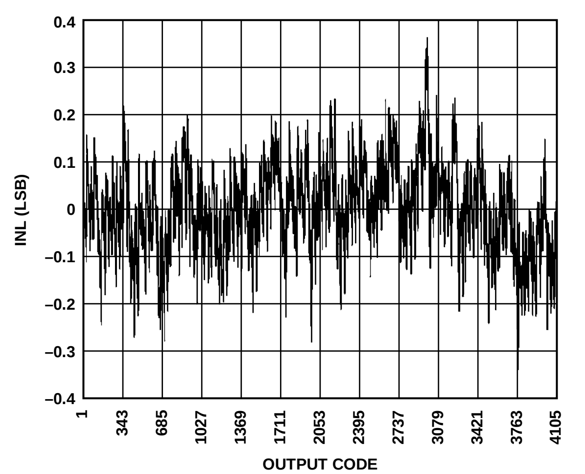

Figure 37. INL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS

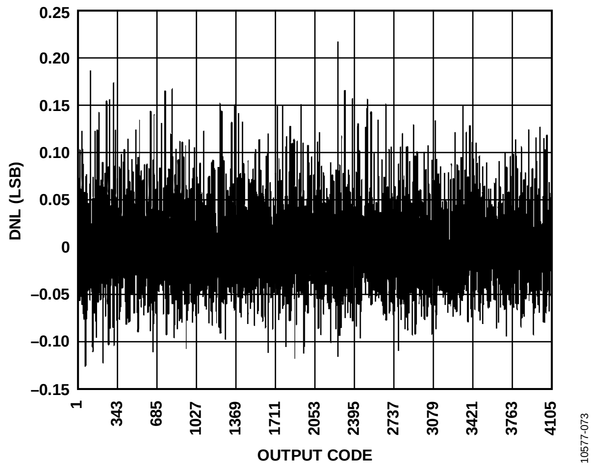

Figure 38. DNL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS

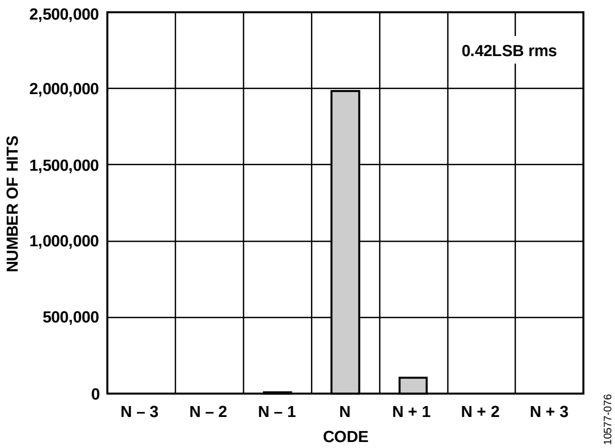

Figure 39. Input-Referred Noise Histogram; f_{SAMPLE} = 125 MSPS

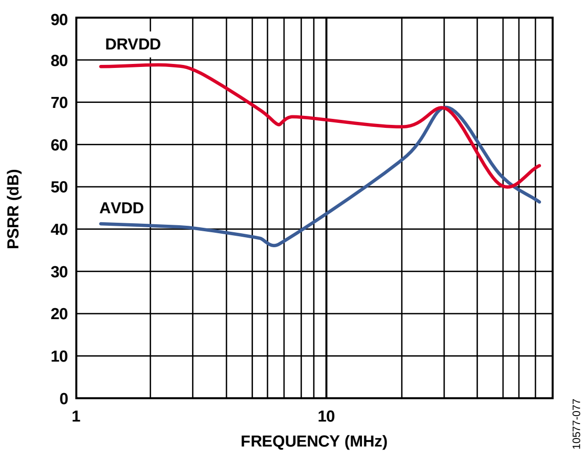

Figure 40. PSRR vs. Frequency; f_{CLK} = 125 MHz, f_{SAMPLE} = 125 MSPS

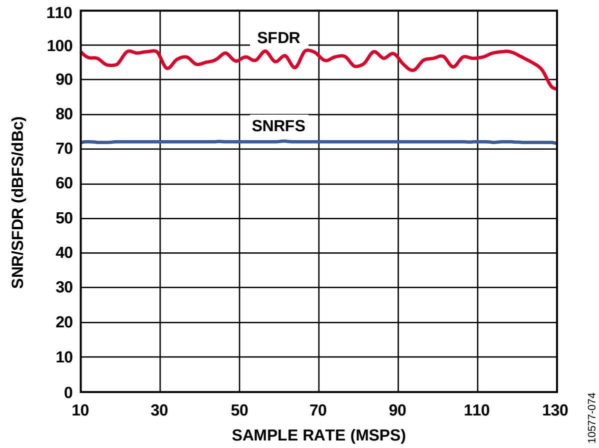

Figure 41. SNR/SFDR vs. Sample Rate; f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS

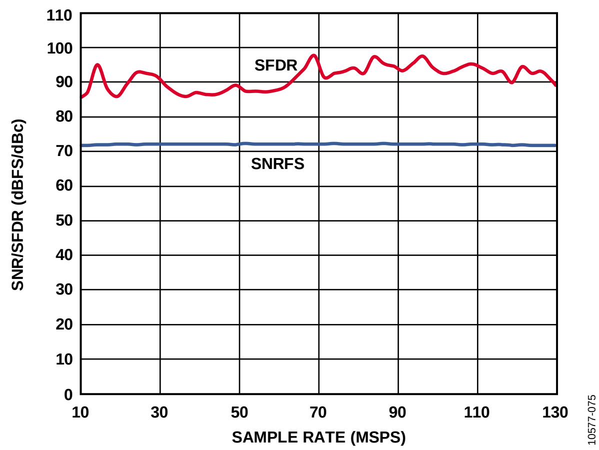

Figure 42. SNR/SFDR vs. Sample Rate; f_{IN} = 70 MHz, f_{SAMPLE} = 125 MSPS

EQUIVALENT CIRCUITS

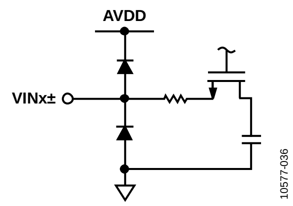

Figure 43. Equivalent Analog Input Circuit

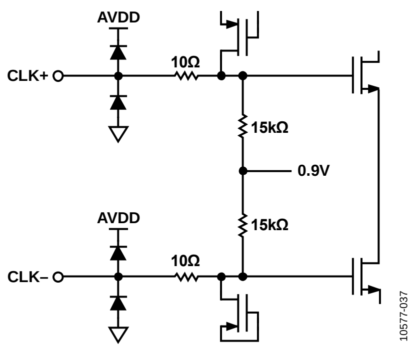

Figure 44. Equivalent Clock Input Circuit

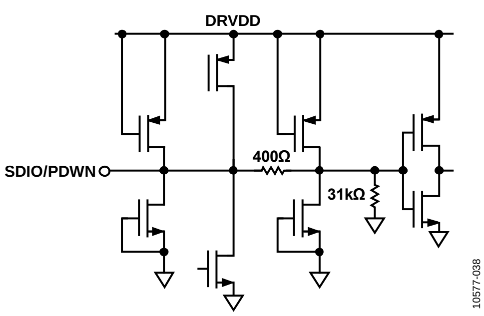

Figure 45. Equivalent SDIO/PDWN Input Circuit

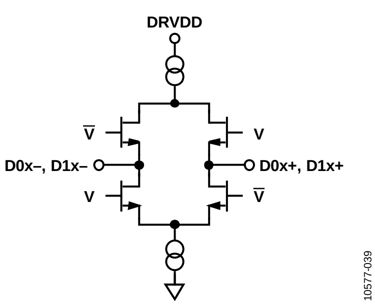

Figure 46. Equivalent Digital Output Circuit

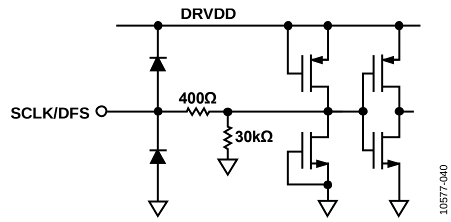

Figure 47. Equivalent SCLK/DFS Input Circuit

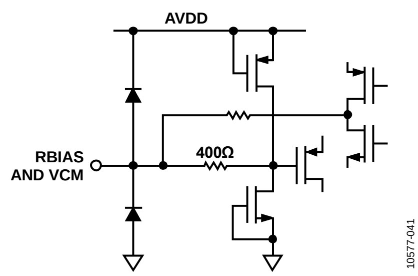

Figure 48. Equivalent RBIAS and VCM Circuit

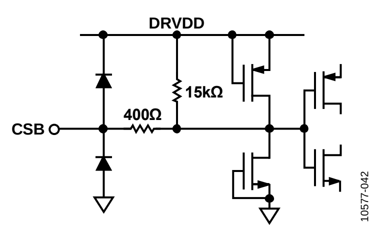

Figure 49. Equivalent CSB Input Circuit

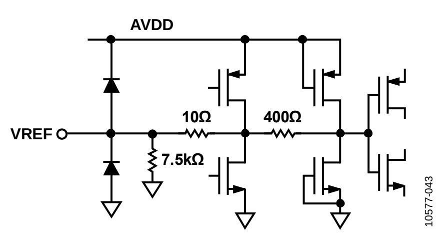

Figure 50. Equivalent VREF Circuit

THEORY OF OPERATION

The AD9635 is a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture allows the first stage to operate with a new input sample while the remaining stages operate with the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and data clocks.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9635 is a differential switched-capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal-dependent errors and achieve optimum performance.

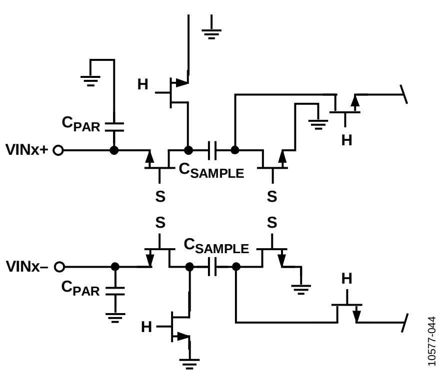

Figure 51. Switched-Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 51). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle.

A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, therefore, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a differential capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values depend on the application.

Input Common Mode

The analog inputs of the AD9635 are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide this bias externally. Setting the device so that V_{CM} = AVDD/2 is recommended for optimum performance, but the device can function over a wider range with reasonable performance, as shown in Figure 52.

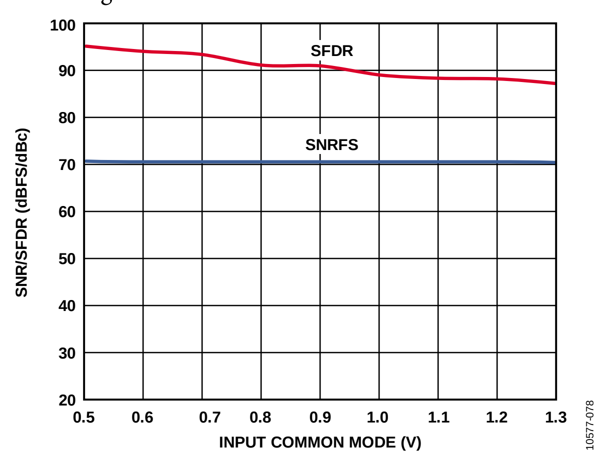

Figure 52. SNR/SFDR vs. Input Common-Mode Voltage, f_{IN} = 9.7 MHz, f_{SAMPLE} = 125 MSPS

An on-chip, common-mode voltage reference is included in the design and is available from the VCM pin. The VCM pin must be decoupled to ground by a 0.1 µF capacitor, as described in the Applications Information section.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9635, the largest input span available is 2 V p-p.

Differential Input Configurations

There are several ways to drive the AD9635 either actively or passively. However, optimum performance is achieved by driving the analog inputs differentially. Using a differential double balun configuration to drive the AD9635 provides excellent performance and a flexible interface to the ADC for baseband applications (see Figure 55).

For applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration (see Figure 56) because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9635.

Regardless of the configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

It is not recommended to drive the AD9635 inputs single-ended.

VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the AD9635. The VREF pin should be externally decoupled to ground with a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

Figure 53 shows how the internal reference voltage is affected by loading. Figure 54 shows the typical drift characteristics of the internal reference in 1.0 V mode.

The internal buffer generates the positive and negative full-scale references for the ADC core.

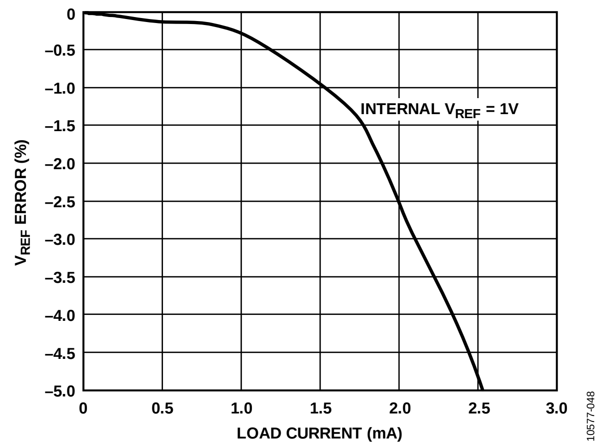

Figure 53. V_{REF} Error vs. Load Current

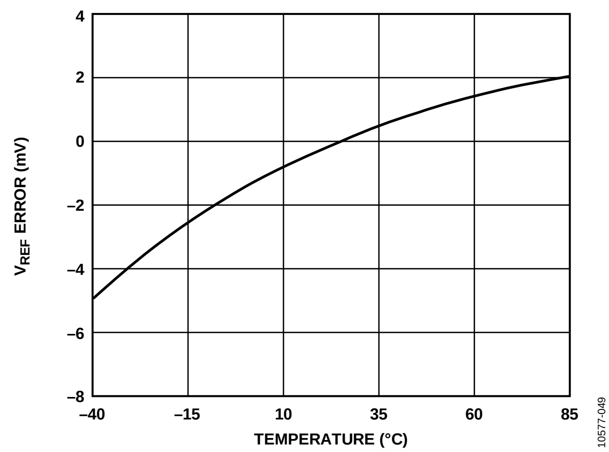

Figure 54. Typical V_{REF} Drift

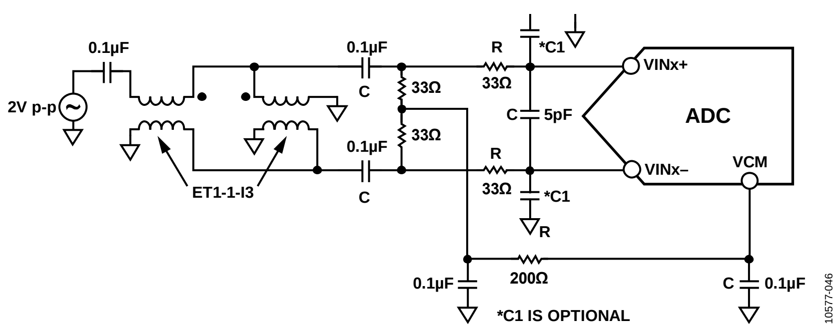

Figure 55. Differential Double Balun Input Configuration for Baseband Applications

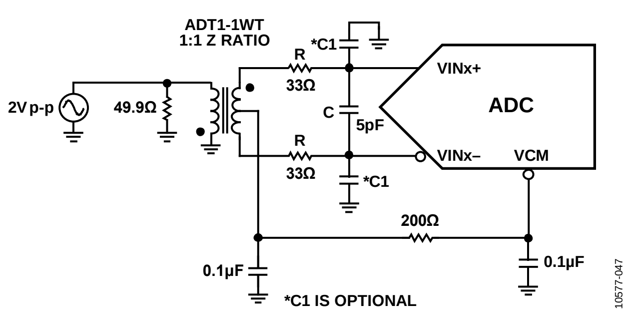

Figure 56. Differential Transformer-Coupled Configuration for Baseband Applications

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD9635 sample clock inputs, CLK+ and CLK−, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or capacitors. These pins are biased internally (see Figure 44) and require no external bias.

Clock Input Options

The AD9635 has a flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the most concern, as described in the Jitter Considerations section.

Figure 57 and Figure 58 show two preferred methods for clocking the AD9635 (at clock rates up to 1 GHz prior to the internal clock divider). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF transformer or an RF balun.

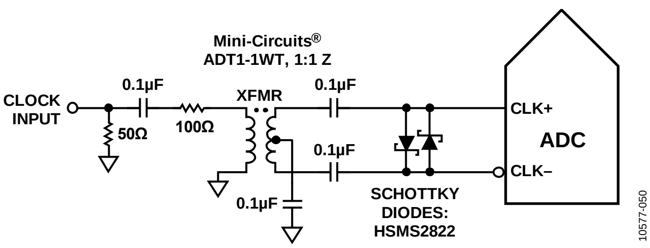

Figure 57. Transformer-Coupled Differential Clock (Up to 200 MHz)

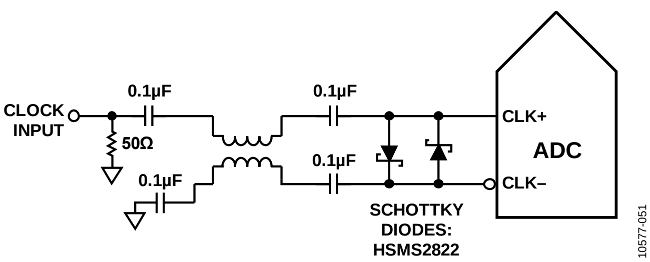

Figure 58. Balun-Coupled Differential Clock (Up to 1 GHz)

The RF balun configuration is recommended for clock frequencies between 125 MHz and 1 GHz, and the RF transformer configuration is recommended for clock frequencies from 10 MHz to 200 MHz. The back-to-back Schottky diodes across the transformer/balun secondary winding limit clock excursions into the AD9635 to approximately 0.8 V p-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9635 while preserving the fast rise and fall times of the signal that are critical to achieving low jitter performance. However, the diode capacitance comes into play at frequencies above 500 MHz. Care must be taken when choosing the appropriate signal limiting diode.

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 59. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-0/AD9516-1/AD9516-2/AD9516-3/AD9516-4/AD9516-5/AD9517-0/AD9517-1/AD9517-2/AD9517-3/AD9517-4 clock drivers offer excellent jitter performance.

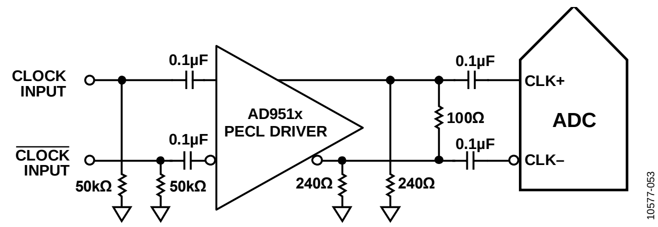

Figure 59. Differential PECL Sample Clock (Up to 1 GHz)

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 60. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-0/AD9516-1/AD9516-2/AD9516-3/AD9516-4/AD9516-5/AD9517-0/AD9517-1/AD9517-2/AD9517-3/AD9517-4 clock drivers offer excellent jitter performance.

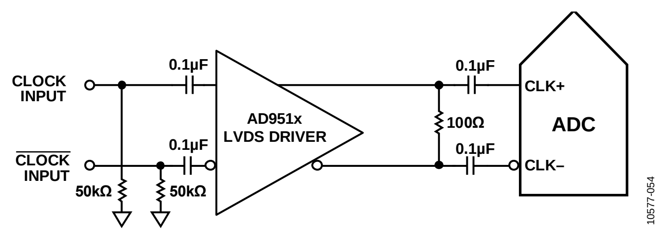

Figure 60. Differential LVDS Sample Clock (Up to 1 GHz)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended 1.8 V CMOS signal. In such applications, drive the CLK+ pin directly from a CMOS gate, and bypass the CLK− pin to ground with a 0.1 µF capacitor (see Figure 61).

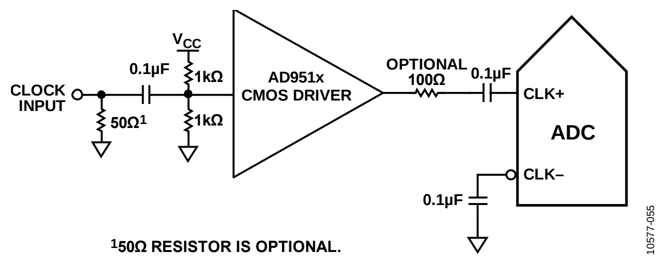

Figure 61. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

Input Clock Divider

The AD9635 contains an input clock divider that can divide the input clock by integer values from 1 to 8. To achieve a given sample rate, the frequency of the externally applied clock must be multiplied by the divide value. The increased rate of the external clock normally results in lower clock jitter, which is beneficial for IF undersampling applications.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to the clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9635 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9635. Noise and distortion performance are nearly flat for a wide range of duty cycles with the DCS on.

Jitter in the rising edge of the input is still of concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates of less than 20 MHz, nominally. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by the following equation:

$$SNR\ Degradation = 20\log_{10}\left(\frac{1}{2\pi \times f_A \times t_J}\right)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 62).

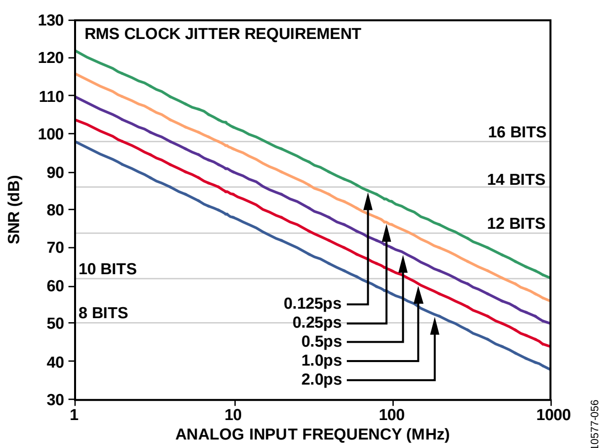

Figure 62. Ideal SNR vs. Input Frequency and Jitter

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9635. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock as the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs.

POWER DISSIPATION AND POWER-DOWN MODE

As shown in Figure 63, the power dissipated by the AD9635 is proportional to its sample rate. The AD9635 is placed in power-down mode either by the SPI port or by asserting the PDWN pin high. In this state, the ADC typically dissipates 2 mW. During power-down, the output drivers are placed in a high impedance state. Asserting the PDWN pin low returns the AD9635 to its normal operating mode. Note that PDWN is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

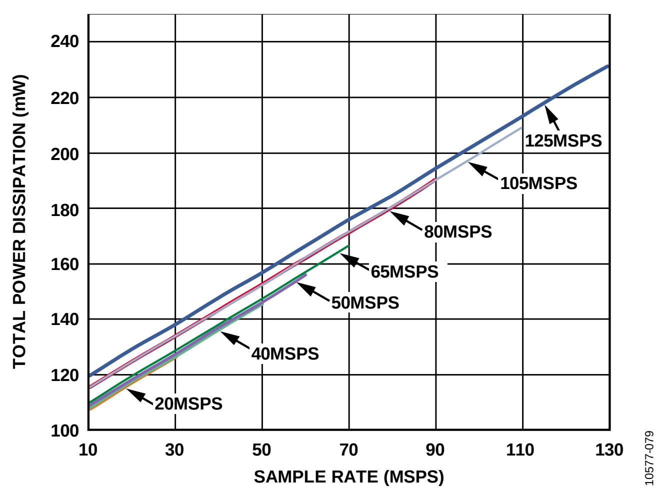

Figure 63. Total Power Dissipation vs. f_{SAMPLE} for f_{IN} = 9.7 MHz

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when the part enters power-down mode and must then be recharged when the part returns to normal operation. As a result, wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times. When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map section for more details on using these features.

DIGITAL OUTPUTS AND TIMING

The AD9635 differential outputs conform to the ANSI-644 LVDS standard on default power-up. This default setting can be changed to a low power, reduced signal option (similar to the IEEE 1596.3 standard) via the SPI. The LVDS driver current is derived on chip and sets the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing (or 700 mV p-p differential) at the receiver.

When operating in reduced range mode, the output current is reduced to 2 mA. This results in a 200 mV swing (or 400 mV p-p differential) across a 100 Ω termination at the receiver.

The LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor placed as close as possible to the receiver. If there is no far-end receiver termination or there is poor differential trace routing, timing errors may result. To avoid such timing errors, ensure that the trace length is less than 24 inches and that the differential output traces are close together and at equal lengths.

Figure 64 shows an example of the FCO and data stream with proper trace length and position.

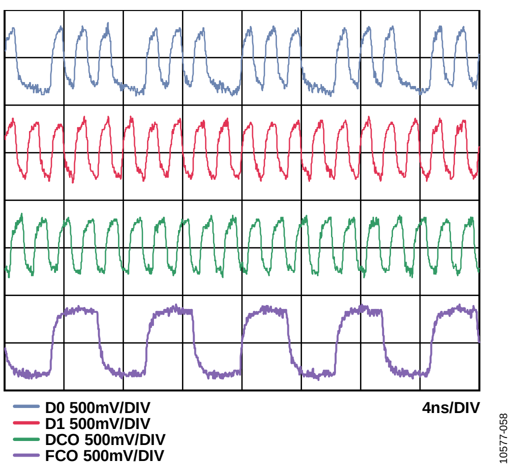

Figure 64. AD9635-125, LVDS Output Timing Example in ANSI-644 Mode (Default)

Figure 65 shows the LVDS output timing example in reduced range mode.

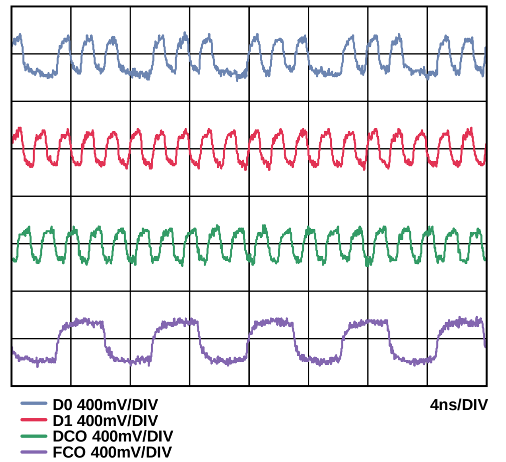

Figure 65. AD9635-125, LVDS Output Timing Example in Reduced Range Mode

Figure 66 shows an example of the LVDS output using the ANSI-644 standard (default) data eye and a time interval error (TIE) jitter histogram with trace lengths of less than 24 inches on standard FR-4 material.

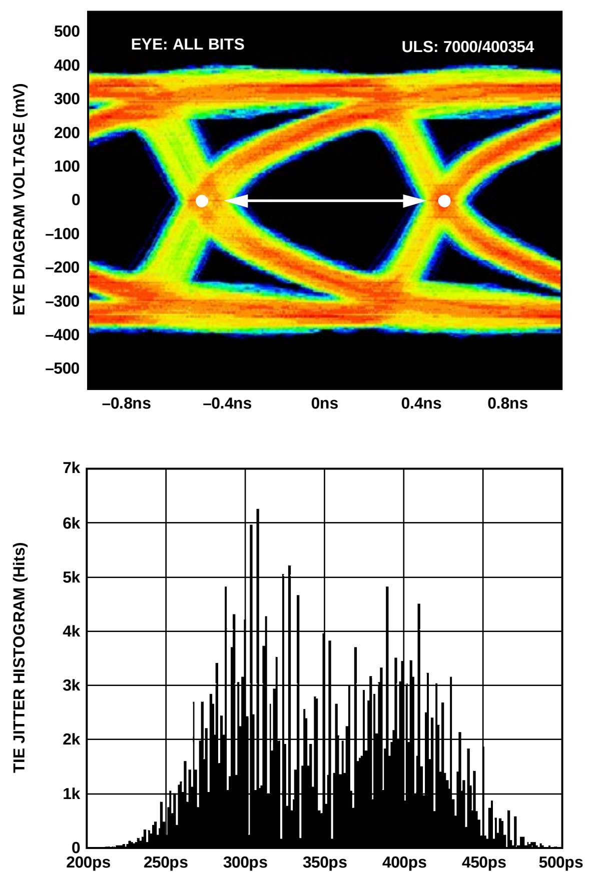

Figure 66. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Less Than 24 Inches on Standard FR-4 Material, External 100 Ω Far-End Termination Only

Figure 67 shows an example of trace lengths exceeding 24 inches on standard FR-4 material. Note that the TIE jitter histogram reflects the decrease of the data eye opening as the edge deviates from the ideal position.

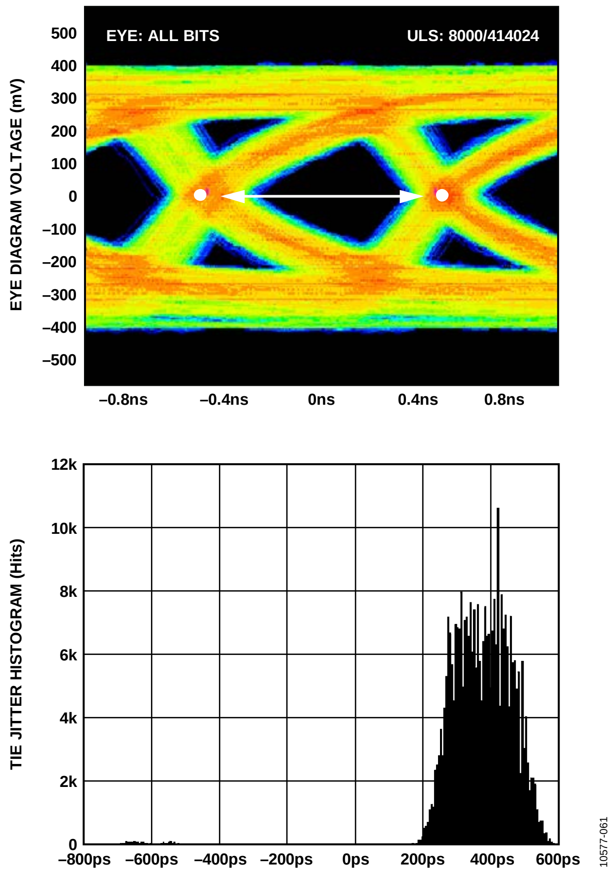

Figure 67. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths Greater Than 24 Inches on Standard FR-4 Material, External 100 Ω Far-End Termination Only

It is the responsibility of the user to determine if the waveforms meet the timing budget of the design when the trace lengths exceed 24 inches. Additional SPI options allow the user to further increase the internal termination (increasing the current) of both outputs to drive longer trace lengths. This increase in current can be achieved by programming Register 0x15. Although an increase in current produces sharper rise and fall times on the data edges and is less prone to bit errors, the power dissipation of the DRVDD supply increases when this option is used.

The format of the output data is twos complement by default. An example of the output coding format can be found in Table 9. To change the output data format to offset binary, see the Memory Map section.

Data from each ADC is serialized and provided on a separate channel in two lanes in DDR mode. The data rate for each serial stream is equal to (12 bits × the sample clock rate)/2 lanes, with a maximum of 750 Mbps/lane ((12 bits × 125 MSPS)/(2 lanes) = 750 Mbps/lane)). The maximum allowable output data rate is 1 Gbps/lane. If one-lane mode is used, the data rate doubles for a given sample rate. To stay within the maximum data rate of 1 Gbps/lane, the sample rate is limited to a maximum of 83.3 MSPS in one-lane output mode.

The lowest typical conversion rate is 10 MSPS. For conversion rates of less than 20 MSPS, the SPI must be used to reconfigure the integrated PLL. See Register 0x21 in the Memory Map section for details on enabling this feature.

Two output clocks are provided to assist in capturing data from the AD9635. The DCO is used to clock the output data and is equal to 3× the sample clock (CLK) rate for the default mode of operation. Data is clocked out of the AD9635 and must be captured on the rising and falling edges of the DCO that supports double data rate (DDR) capturing. The FCO is used to signal the start of a new output byte and is equal to the sample clock rate in 1× frame mode. See the Timing Diagrams section for more information.

When the SPI is used, the DCO phase can be adjusted in 60° increments relative to the data edge. This enables the user to refine system timing margins, if required. The default DCO+ and DCO− timing, as shown in Figure 2, is 180° relative to the output data edge.

A 10-bit serial stream can also be initiated from the SPI. This allows the user to implement and test compatibility to lower resolution systems. When changing the resolution to a 10-bit serial stream, the data stream is shortened.

In default mode, as shown in Figure 2, the MSB is first in the data output serial stream. This can be inverted, by using the SPI, so that the LSB is first in the data output serial stream.

Table 9. Digital Output Coding

Input (V)	Condition (V)	Offset Binary Output Mode	Twos Complement Mode
VIN+ − VIN−	<−VREF − 0.5 LSB	0000 0000 0000	1000 0000 0000
VIN+ − VIN−	−VREF	0000 0000 0000	1000 0000 0000
VIN+ − VIN−	0 V	1000 0000 0000	0000 0000 0000
VIN+ − VIN−	+VREF − 1.0 LSB	1111 1111 1111	0111 1111 1111
VIN+ − VIN−	>+VREF − 0.5 LSB	1111 1111 1111	0111 1111 1111

Table 10. Flexible Output Test Modes

Output Test Mode Bit Sequence	Pattern Name	Digital Output Word 1	Digital Output Word 2	Subject to Data Format Select	Notes
0000	Off (default)	Not applicable	Not applicable	N/A	
0001	Midscale short	10 0000 0000 (10-bit) 1000 0000 0000 (12-bit)	Not applicable	Yes	Offset binary code shown
0010	+Full-scale short	11 1111 1111 (10-bit) 1111 1111 1111 (12-bit)	Not applicable	Yes	Offset binary code shown
0011	−Full-scale short	00 0000 0000 (10-bit) 0000 0000 0000 (12-bit)	Not applicable	Yes	Offset binary code shown
0100	Checkerboard	10 1010 1010 (10-bit) 1010 1010 1010 (12-bit)	01 0101 0101 (10-bit) 0101 0101 0101 (12-bit)	No	
0101	PN sequence long[1]	Not applicable	Not applicable	Yes	PN23, ITU 0.150 $X^{23} + X^{18} + 1$
0110	PN sequence short[1]	Not applicable	Not applicable	Yes	PN9 ITU 0.150 $X^9 + X^5 + 1$
0111	One-/zero-word toggle	11 1111 1111 (10-bit) 1111 1111 1111 (12-bit)	00 0000 0000 (10-bit) 0000 0000 0000 (12-bit)	No	
1000	User input	Register 0x19 to Register 0x1A	Register 0x1B to Register 0x1C	No	
1001	1-/0-bit toggle	10 1010 1010 (10-bit) 1010 1010 1010 (12-bit)	Not applicable	No	
1010	1× sync	00 0011 1111 (10-bit) 0000 0111 1111 (12-bit)	Not applicable	No	
1011	One bit high	10 0000 0000 (10-bit) 1000 0000 0000 (12-bit)	Not applicable	No	Pattern associated with the external pin
1100	Mixed frequency	10 0011 0011 (10-bit) 1000 0110 0111 (12-bit)	Not applicable	No	

[1] All test mode options except PN sequence short and PN sequence long can support 10-bit to 12-bit word lengths to verify data capture to the receiver.

There are 12 digital output test pattern options available that can be initiated through the SPI. This is a useful feature when validating receiver capture and timing. Refer to Table 10 for the output bit sequencing options available. Some test patterns have two serial sequential words and can be alternated in various ways, depending on the test pattern chosen.

Note that some patterns do not adhere to the data format select option. In addition, custom user-defined test patterns can be assigned in the 0x19, 0x1A, 0x1B, and 0x1C register addresses.

The PN sequence short pattern produces a pseudorandom bit sequence that repeats itself every $2^9 - 1$ or 511 bits. A description of the PN sequence and how it is generated can be found in Section 5.1 of the ITU-T 0.150 (05/96) standard. The seed value is all 1s (see Table 11 for the initial values). The output is a parallel representation of the serial PN9 sequence in MSB-first format. The first output word is the first 12 bits of the PN9 sequence in MSB aligned form.

Table 11. PN Sequence

Sequence	Initial Value	Next Three Output Samples (MSB First), Twos Complement
PN Sequence Short	0x7F8	0xBDF, 0x973, 0xA09
PN Sequence Long	0x7FF	0x7FE, 0x800, 0xFC0

The PN sequence long pattern produces a pseudorandom bit sequence that repeats itself every $2^{23} - 1$ or 8,388,607 bits. A description of the PN sequence and how it is generated can be found in Section 5.6 of the ITU-T 0.150 (05/96) standard. The seed value is all 1s (see Table 11 for the initial values) and the AD9635 inverts the bit stream with relation to the ITU standard. The output is a parallel representation of the serial PN23 sequence in MSB-first format. The first output word is the first 12 bits of the PN23 sequence in MSB aligned form.

Consult the Memory Map section for information on how to change these additional digital output timing features through the SPI.

SDIO/PDWN Pin

For applications that do not require SPI mode operation, the CSB pin is tied to DRVDD, and the SDIO/PDWN pin controls power-down mode according to Table 12.

Table 12. Power-Down Mode Pin Settings

PDWN Pin Voltage	Device Mode
AGND (Default)	Run device, normal operation
DRVDD	Power down device

Note that in non-SPI mode (CSB tied to DRVDD), the power-up sequence described in the Power and Ground Guidelines section must be adhered to. Violating the power-up sequence necessitates a soft reset via the SPI, which is not possible in non-SPI mode.

SCLK/DFS Pin

The SCLK/DFS pin is used for output format selection in applications that do not require SPI mode operation. This pin determines the digital output format when the CSB pin is held high during device power-up. When SCLK/DFS is tied to DRVDD, the ADC output format is twos complement; when SCLK/DFS is tied to AGND, the ADC output format is offset binary.

Table 13. Digital Output Format

DFS Voltage	Output Format
AGND	Offset binary
DRVDD	Twos complement

CSB Pin

The CSB pin should be tied to DRVDD for applications that do not require SPI mode operation. By tying CSB high, all SCLK and SDIO information is ignored.

Note that, in non-SPI mode (CSB tied to DRVDD), the power-up sequence described in the Power and Ground Guidelines section must be adhered to. Violating the power-up sequence necessitates a soft reset via SPI, which is not possible in non-SPI mode.

RBIAS Pin

To set the internal core bias current of the ADC, place a 10.0 kΩ, 1% tolerance resistor to ground at the RBIAS pin.

OUTPUT TEST MODES

The output test options are described in Table 10 and are controlled by the output test mode bits at Address 0x0D. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not. The PN generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x0D. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), but they do require an encode clock. For more information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

SERIAL PORT INTERFACE (SPI)

The AD9635 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI offers the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, which are documented in the Memory Map section. For general operational information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK/DFS pin, the SDIO/PDWN pin, and the CSB pin (see Table 14). SCLK/DFS (a serial clock when CSB is low) is used to synchronize the read and write data presented from and to the ADC. SDIO/PDWN (serial data input/output when CSB is low) is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. CSB (chip select bar) is an active low control that enables or disables the SPI read and write cycles.

Table 14. Serial Port Interface Pins

Pin	Function
SCLK/DFS	Serial clock when CSB is low. The serial shift clock input, which is used to synchronize serial interface reads and writes.
SDIO/PDWN	Serial data input/output when CSB is low. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that enables the SPI mode read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK/DFS, determines the start of the framing. An example of the serial timing is shown in Figure 68. See Table 5 for definitions of the timing parameters.

Other modes involving the CSB pin are available. CSB can be held low indefinitely, which permanently enables the device; this is called streaming. CSB can stall high between bytes to allow for additional external timing. When the CSB pin is tied high, SPI functions are placed in high impedance mode. This mode turns on the secondary functions of the SPI pins.

During the instruction phase of a SPI operation, a 16-bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and W1 bits.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. The first bit of the first byte in a multibyte serial data transfer frame indicates whether a read command or a write command is issued. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

All data is composed of 8-bit words. Data can be sent in MSB-first mode or in LSB-first mode. MSB-first mode is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

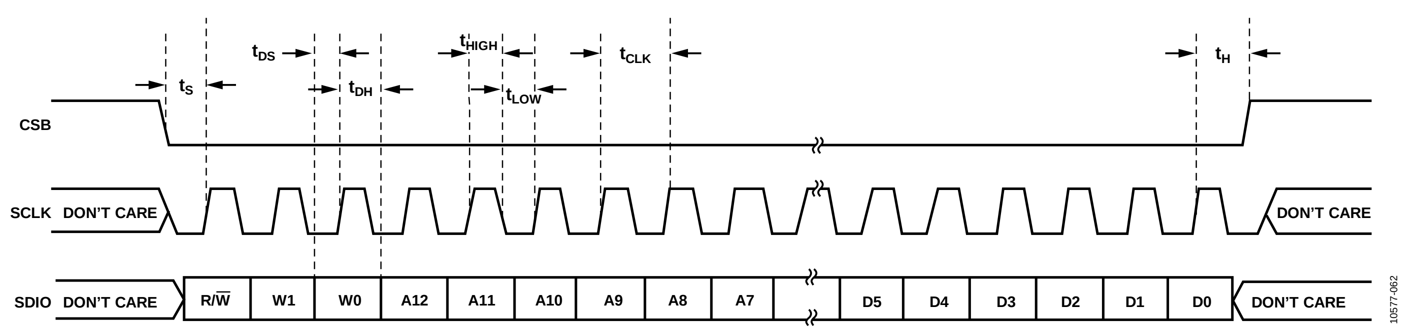

Figure 68. Serial Port Interface Timing Diagram

HARDWARE INTERFACE

The pins described in Table 14 comprise the physical interface between the user programming device and the serial port of the AD9635. The SCLK/DFS pin and the CSB pin function as inputs when using the SPI interface. The SDIO/PDWN pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK/DFS signal, the CSB signal, and the SDIO/PDWN signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9635 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

The SCLK/DFS and SDIO/PDWN pins serve a dual function when the SPI interface is not being used. When the pins are strapped to DRVDD or ground during device power-on, they are associated with a specific function. Table 12 and Table 13 describe the strappable functions supported on the AD9635.

CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SCLK/DFS pin and the SDIO/PDWN pin serve as standalone CMOS-compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the output data format and power-down feature control. In this mode, CSB should be connected to DRVDD, which disables the serial port interface.

Note that in non-SPI mode (CSB tied to DRVDD), the power-up sequence described in the Power and Ground Guidelines section must be adhered to. Violating the power-up sequence necessitates a soft reset via the SPI, which is not possible in non-SPI mode.

SPI ACCESSIBLE FEATURES

Table 15 provides a brief description of the general features that are accessible via the SPI. These features are described in general in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. The AD9635 part-specific features are described in detail in Table 16, the external memory map register table, and the following text.

Table 15. Features Accessible Using the SPI

Feature Name	Description
Power Mode	Allows the user to set either power-down mode or standby mode
Clock	Allows the user to access the DCS, set the clock divider, and set the clock divider phase
Offset	Allows the user to digitally adjust the converter offset
Test I/O	Allows the user to set test modes to have known data on output bits
Output Mode	Allows the user to set the output mode
Output Phase	Allows the user to set the output clock polarity
ADC Resolution	Allows for power consumption scaling with respect to sample rate

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table (see Table 16) has eight bit locations. The memory map is roughly divided into three sections: the chip configuration registers (Address 0x00 to Address 0x02); the device index and transfer registers (Address 0x05 and Address 0xFF); and the global ADC function registers, including setup, control, and test (Address 0x08 to Address 0x102).

The memory map register table lists the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x05, the device index register, has a hexadecimal default value of 0x33. This means that in Address 0x05, Bits[7:6] = 00, Bits[5:4] = 11, Bits[3:2] = 00, and Bits[1:0] = 11 (in binary). This setting is the default channel index setting. The default value results in both ADC channels receiving the next write command. For more information on this function and others, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI.* This application note details the functions controlled by Register 0x00 to Register 0xFF. The remaining registers are documented in the Memory Map Register Descriptions section.

Open Locations

All address and bit locations that are not included in Table 16 are not currently supported for this device. Unused bits of a valid address location should be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x05). If the entire address location is open or not listed in Table 16 (for example, Address 0x13), this address location should not be written.

Default Values

After the AD9635 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 16.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Channel-Specific Registers

Some channel setup functions can be programmed differently for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 16 as local. These local registers and bits can be accessed by setting the appropriate data channel bits (A or B) and the clock channel DCO bit (Bit 5) and FCO bit (Bit 4) in Register 0x05. If all the bits are set, the subsequent write affects the registers of both channels and the DCO/FCO clock channels. In a read cycle, only one channel (A or B) should be set to read one of the two registers. If all the bits are set during a SPI read cycle, the part returns the value for Channel A. Registers and bits that are designated as global in Table 16 affect the entire part or the channel features for which independent settings are not allowed between channels. The settings in Register 0x05 do not affect the global registers and bits.

MEMORY MAP REGISTER TABLE

The AD9635 uses a 3-wire interface and 16-bit addressing and, therefore, Bit 0 and Bit 7 in Register 0x00 are set to 0, and Bit 3 and Bit 4 are set to 1.

When Bit 5 in Register 0x00 is set high, the SPI enters a soft reset, where all of the user registers revert to their default values and Bit 2 is automatically cleared.

Table 16.

Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Comments
Chip Configuration Registers											
0x00	SPI port configuration	0 = SDO active	LSB first	Soft reset	1 = 16-bit address	1 = 16-bit address	Soft reset	LSB first	0 = SDO active	0x18	Nibbles are mirrored to allow a given register value to perform the same function for either MSB-first or LSB-first mode.
0x01	Chip ID (global)	8-bit chip ID, Bits[7:0] AD9635 0x8D = dual, 12-bit, 80 MSPS/125 MSPS, serial LVDS								0x8D	Unique chip ID used to differentiate devices; read only.
0x02	Chip grade (global)	Open	Speed grade ID, Bits[6:4] 100 = 80 MSPS 110 = 125 MSPS			Open	Open	Open	Open		Unique speed grade ID used to differentiate graded devices; read only.
Device Index and Transfer Registers											
0x05	Device index	Open	Open	Clock Channel DCO	Clock Channel FCO	Open	Open	Data Channel B	Data Channel A	0x33	Bits are set to determine which device on chip receives the next write command. Default is all devices on chip.
0xFF	Transfer	Open	Open	Open	Open	Open	Open	Open	Initiate override	0x00	Set resolution/ sample rate override.
Global ADC Function Registers											
0x08	Power modes (global)	Open	Open	Open	Open	Open	Open	Power mode 00 = chip run 01 = full power-down 10 = standby 11 = reset		0x00	Determines various generic modes of chip operation.
0x09	Clock (global)	Open	Open	Open	Open	Open	Open	Open	Duty cycle stabilizer 0 = off 1 = on	0x00	Turns duty cycle stabilizer on or off.
0x0B	Clock divide (global)	Open	Open	Open	Open	Open	Clock divide ratio[2:0] 000 = divide by 1 001 = divide by 2 010 = divide by 3 011 = divide by 4 100 = divide by 5 101 = divide by 6 110 = divide by 7 111 = divide by 8			0x00	
0x0C	Enhancement control	Open	Open	Open	Open	Open	Chop mode 0 = off 1 = on	Open	Open	0x00	Enables/ disables chop mode.

Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Comments
0x0D	Test mode (local except for PN sequence resets)	User input test mode 00 = single 01 = alternate 10 = single once 11 = alternate once (affects user input test mode only, Bits[3:0] = 1000)		Reset PN long gen	Reset PN short gen	Output test mode, Bits[3:0] (local) 0000 = off (default) 0001 = midscale short 0010 = positive FS 0011 = negative FS 0100 = alternating checkerboard 0101 = PN23 sequence 0110 = PN9 sequence 0111 = one-/zero-word toggle 1000 = user input 1001 = 1-/0-bit toggle 1010 = 1× sync 1011 = one bit high 1100 = mixed bit frequency				0x00	When set, the test data is placed on the output pins in place of normal data.
0x10	Offset adjust (local)	8-bit device offset adjustment, Bits[7:0] (local) Offset adjust in LSBs from +127 to −128 (twos complement format)								0x00	Device offset trim.
0x14	Output mode	Open	LVDS-ANSI/ LVDS-IEEE option 0 = LVDS-ANSI 1 = LVDS-IEEE reduced range link (global) see Table 17	Open	Open	Open	Output invert (local)	Open	Output format 0 = offset binary 1 = twos comple-ment (global)	0x01	Configures the outputs and format of the data.
0x15	Output adjust	Open	Open	Output driver termination, Bits[1:0] 00 = none 01 = 200 Ω 10 = 100 Ω 11 = 100 Ω		Open	Open	Open	Output drive 0 = 1× drive 1 = 2× drive	0x00	Determines LVDS or other output properties.
0x16	Output phase	Open	Input clock phase adjust, Bits[6:4] (value is number of input clock cycles of phase delay); see Table 18			Output clock phase adjust, Bits[3:0] (0000 through 1011); see Table 19				0x03	On devices using global clock divide, determines which phase of the divider output is used to supply the output clock. Internal latching is unaffected.
0x18	V_{REF}	Open	Open	Open	Open	Open	Internal V_{REF} adjustment digital scheme, Bits[2:0] 000 = 1.0 V p-p 001 = 1.14 V p-p 010 = 1.33 V p-p 011 = 1.6 V p-p 100 = 2.0 V p-p			0x04	Selects and/or adjusts V_{REF}.
0x19	USER_PATT1_LSB (global)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User Defined Pattern 1 LSB.
0x1A	USER_PATT1_MSB (global)	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User Defined Pattern 1 MSB.
0x1B	USER_PATT2_LSB (global)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User Defined Pattern 2 LSB.
0x1C	USER_PATT2_MSB (global)	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User Defined Pattern 2 MSB.

Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Comments
0x21	Serial output data control (global)	LVDS output 0 = MSB first (default) 1 = LSB first	SDR/DDR one-lane/two-lane, bitwise/bytewise, Bits[6:4] 000 = SDR two-lane, bitwise 001 = SDR two-lane, bytewise 010 = DDR two-lane, bitwise 011 = DDR two-lane, bytewise (default) 100 = DDR one-lane, wordwise			Encode mode 0 = normal encode rate mode (default) 1 = low encode mode for sample rate of <20 MSPS	0 = 1× frame (default) 1 = 2× frame	Serial output number of bits 10 = 12 bits (default) 11 = 10 bits		0x32	Serial stream control. Sample rate of <20 MSPS requires that Bits[6:4] = 100 (DDR one-lane) and Bit 3 = 1 (low encode mode).
0x22	Serial channel status (local)	Open	Open	Open	Open	Open	Open	Channel output reset	Channel power-down	0x00	Used to power down individual sections of a converter.
0x100	Resolution/ sample rate override	Open	Resolution/ sample rate override enable	Resolution 10 = 12 bits 11 = 10 bits		Open	Sample rate 000 = 20 MSPS 001 = 40 MSPS 010 = 50 MSPS 011 = 65 MSPS 100 = 80 MSPS 101 = 105 MSPS 110 = 125 MSPS			0x00	Resolution/ sample rate override (requires writing to the transfer register, 0xFF).
0x101	User I/O Control 2	Open	Open	Open	Open	Open	Open	Open	SDIO pull-down	0x00	Disables SDIO pull-down.
0x102	User I/O Control 3	Open	Open	Open	Open	VCM power-down	Open	Open	Open	0x00	VCM control.

MEMORY MAP REGISTER DESCRIPTIONS

For additional information about functions controlled in Register 0x00 to Register 0xFF, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Device Index (Register 0x05)

There are certain features in the map that can be set independently for each channel, whereas other features apply globally to all channels (depending on context), regardless of which is selected. Bits[1:0] in Register 0x05 can be used to select which individual data channel is affected. The output clock channels can be selected in Register 0x05, as well. A smaller subset of the independent feature list can be applied to those devices.

Transfer (Register 0xFF)

All registers except Register 0x100 are updated the moment they are written. Setting Bit 0 of Register 0xFF high initializes the settings in the ADC sample rate override register (Address 0x100).

Power Modes (Register 0x08)

Bits[7:2]—Open

Bits[1:0]—Power Mode

In normal operation (Bits[1:0] = 00), both ADC channels are active.

In power-down mode (Bits[1:0] = 01), the digital datapath clocks are disabled while the digital datapath is reset. Outputs are disabled.

In standby mode (Bits[1:0] = 10), the digital datapath clocks and the outputs are disabled.

During a digital reset (Bits[1:0] = 11), all the digital datapath clocks and the outputs (where applicable) on the chip are reset, except the SPI port. Note that the SPI is always left under control of the user; that is, it is never automatically disabled or in reset (except by power-on reset).

Enhancement Control (Register 0x0C)

Bits[7:3]—Open

Bit 2—Chop Mode

For applications that are sensitive to offset voltages and other low frequency noise, such as homodyne or direct conversion receivers, chopping in the first stage of the AD9635 is a feature that can be enabled by setting Bit 2. In the frequency domain, chopping translates offsets and other low frequency noise to $f_{CLK}/2$, where it can be filtered.

Bits[1:0]—Open

Output Mode (Register 0x14)

Bit 7—Open

Bit 6—LVDS-ANSI/LVDS-IEEE Option

Setting this bit selects the LVDS-IEEE (reduced range) option.

The default setting is LVDS-ANSI. When LVDS-ANSI or the LVDS-IEEE reduced range link is selected, the user can select the driver termination (see Table 17). The driver current is automatically selected to give the proper output swing.

Table 17. LVDS-ANSI/LVDS-IEEE Options

Output Mode, Bit 6	Output Mode	Output Driver Termination	Output Driver Current
0	LVDS-ANSI	User selectable	Automatically selected to give proper swing
1	LVDS-IEEE reduced range link	User selectable	Automatically selected to give proper swing

Bits[5:3]—Open

Bit 2—Output Invert

Setting this bit inverts the output bit stream.

Bit 1—Open

Bit 0—Output Format

By default, this bit is set to send the data output in twos complement format. Clearing this bit to 0 changes the output mode to offset binary.

Output Adjust (Register 0x15)

Bits[7:6]—Open

Bits[5:4]—Output Driver Termination

These bits allow the user to select the internal termination resistor.

Bits[3:1]—Open

Bit 0—Output Drive

Bit 0 of the output adjust register controls the drive strength on the LVDS driver of the FCO and DCO outputs only. The default values set the drive to 1×, or the drive can be increased to 2× by setting the appropriate channel bit in Register 0x05 and then setting Bit 0. These features cannot be used with the output driver termination select. The termination selection takes precedence over the 2× driver strength on FCO and DCO when both the output driver termination and output drive are selected.

Output Phase (Register 0x16)

Bit 7—Open

Bits[6:4]—Input Clock Phase Adjust

When the clock divider (Register 0x0B) is used, the applied clock is at a higher frequency than the internal sampling clock. Bits[6:4] determine at which phase of the external clock sampling occurs. This is only applicable when the clock divider is used. Setting Bits[6:4] greater than Register 0x0B, Bits[2:0] is prohibited.

Table 18. Input Clock Phase Adjust Options

Input Clock Phase Adjust, Bits[6:4]	Number of Input Clock Cycles of Phase Delay
000 (Default)	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Bits[3:0]—Output Clock Phase Adjust

See Table 19 for details.

Table 19. Output Clock Phase Adjust Options

Output Clock (DCO), Phase Adjust, Bits[3:0]	DCO Phase Adjustment (Degrees Relative to D0x±/D1x± Edge)
0000	0
0001	60
0010	120
0011 (Default)	180
0100	240
0101	300
0110	360
0111	420
1000	480
1001	540
1010	600
1011	660

Serial Output Data Control (Register 0x21)

The serial output data control register is used to program the AD9635 in various output data modes, depending on the data capture solution. Table 20 describes the various serialization options available in the AD9635.

Resolution/Sample Rate Override (Register 0x100)

This register allows the user to downgrade the resolution and/or the maximum sample rate (for lower power) in applications that do not require full resolution and/or sample rate. Settings in this register are not initialized until Bit 0 of the transfer register (Register 0xFF) is written high.

Bits[2:0] do not affect the sample rate; they affect the maximum sample rate capability of the ADC.

User I/O Control 2 (Register 0x101)

Bits[7:1]—Open

Bit 0—SDIO Pull-Down

Bit 0 can be set to disable the internal 30 kΩ pull-down on the SDIO pin, which can be used to limit the loading when many devices are connected to the SPI bus.

User I/O Control 3 (Register 0x102)

Bits[7:4]—Open

Bit 3—VCM Power-Down

Bit 3 can be set high to power down the internal VCM generator. This feature is used when applying an input common mode voltage from an external source.

Bits[2:0]—Open

Table 20. SPI Register Options

	Serialization Options Selected				
Register 0x21 Contents	Serial Output Number of Bits (SONB)	Frame Mode	Serial Data Mode	DCO Multiplier	Timing Diagram
0x32	12-bit	1×	DDR two-lane bytewise	$3 \times f_S$	See Figure 2 (default setting)
0x22	12-bit	1×	DDR two-lane bitwise	$3 \times f_S$	See Figure 2
0x12	12-bit	1×	SDR two-lane bytewise	$6 \times f_S$	See Figure 2
0x02	12-bit	1×	SDR two-lane bitwise	$6 \times f_S$	See Figure 2
0x36	12-bit	2×	DDR two-lane bytewise	$3 \times f_S$	See Figure 4
0x26	12-bit	2×	DDR two-lane bitwise	$3 \times f_S$	See Figure 4
0x16	12-bit	2×	SDR two-lane bytewise	$6 \times f_S$	See Figure 4
0x06	12-bit	2×	SDR two-lane bitwise	$6 \times f_S$	See Figure 4
0x42	12-bit	1×	DDR one-lane wordwise	$6 \times f_S$	See Figure 6
0x33	10-bit	1×	DDR two-lane bytewise	$2.5 \times f_S$	See Figure 3
0x23	10-bit	1×	DDR two-lane bitwise	$2.5 \times f_S$	See Figure 3
0x13	10-bit	1×	SDR two-lane bytewise	$5 \times f_S$	See Figure 3
0x03	10-bit	1×	SDR two-lane bitwise	$5 \times f_S$	See Figure 3
0x37	10-bit	2×	DDR two-lane bytewise	$2.5 \times f_S$	See Figure 5
0x27	10-bit	2×	DDR two-lane bitwise	$2.5 \times f_S$	See Figure 5
0x17	10-bit	2×	SDR two-lane bytewise	$5 \times f_S$	See Figure 5
0x07	10-bit	2×	SDR two-lane bitwise	$5 \times f_S$	See Figure 5
0x43	10-bit	1×	DDR one-lane wordwise	$5 \times f_S$	See Figure 7

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting design and layout of the AD9635 as a system, it is recommended that the designer become familiar with these guidelines, which describe the special circuit connections and layout requirements that are needed for certain pins.

POWER AND GROUND GUIDELINES

When connecting power to the AD9635, it is recommended that two separate 1.8 V supplies be used. Use one supply for analog (AVDD); use a separate supply for the digital outputs (DRVDD). For both AVDD and DRVDD, several different decoupling capacitors should be used to cover both high and low frequencies. Place these capacitors close to the point of entry at the PCB level and close to the pins of the part, with minimal trace length.

If two supplies are used, AVDD must not power up before DRVDD. DRVDD must power up before, or simultaneously with, AVDD. If this sequence is violated, a soft reset via SPI Register 0x00 (Bits[7:0] = 0x3C), followed by a digital reset via SPI Register 0x08 (Bits[7:0] = 0x03, then Bits[7:0] = 0x00), restores the part to proper operation.

In non-SPI mode, the supply sequence is mandatory; in this case, violating the supply sequence is nonrecoverable.

A single PCB ground plane should be sufficient when using the AD9635. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

CLOCK STABILITY CONSIDERATIONS

When powered on, the AD9635 enters an initialization phase during which an internal state machine sets up the biases and the registers for proper operation. During the initialization process, the AD9635 needs a stable clock. If the ADC clock source is not present or not stable during ADC power-up, it disrupts the state machine and causes the ADC to start up in an unknown state. To correct this, reinvoke an initialization sequence after the ADC clock is stable by issuing a digital reset via Register 0x08. In the default configuration (internal V_{REF}, ac-coupled input) where V_{REF} and V_{CM} are supplied by the ADC itself, a stable clock during power-up is sufficient. In the case where V_{CM} is supplied by an external source, this, too, must be stable at power-up; otherwise, a subsequent digital reset via Register 0x08 is needed. The pseudo code sequence for a digital reset is as follows:

```
SPI_Write (0x08, 0x03);   # Digital Reset
SPI_Write (0x08, 0x00);   # Normal Operation
```

EXPOSED PAD THERMAL HEAT SLUG RECOMMENDATIONS

It is required that the exposed pad on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance of the AD9635. An exposed continuous copper plane on the PCB should mate to the AD9635 exposed pad, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be solder-filled or plugged.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous copper plane by overlaying a silkscreen on the PCB into several uniform sections. This provides several tie points between the ADC and PCB during the reflow process, whereas using one continuous plane with no partitions only guarantees one tie point. See Figure 69 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*, at www.analog.com.

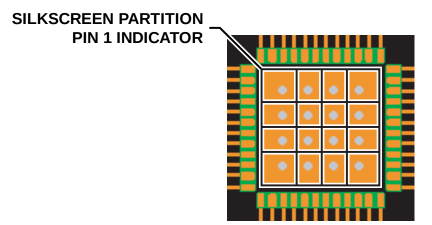

Figure 69. Typical PCB Layout

VCM

The VCM pin should be decoupled to ground with a 0.1 µF capacitor.

REFERENCE DECOUPLING

The VREF pin should be externally decoupled to ground with a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

SPI PORT

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9635 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

OUTLINE DIMENSIONS

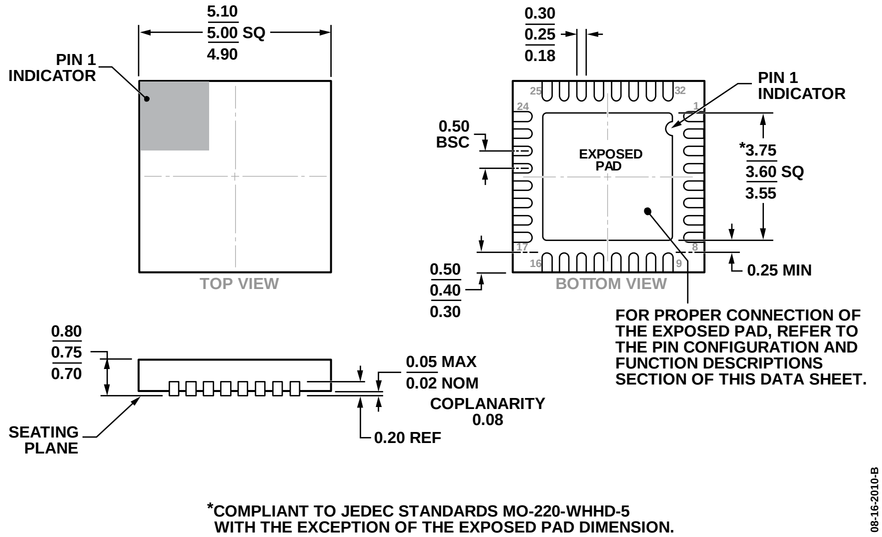

Figure 70. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9635BCPZ-80	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-12
AD9635BCPZRL7-80	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-12
AD9635BCPZ-125	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-12
AD9635BCPZRL7-125	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-12
AD9635-125EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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