14-Bit, 125 MSPS, 1.8 V Dual Analog-to-Digital Converter

Enhanced Product

AD9648-EP

FEATURES

- 1.8 V analog supply operation
- 1.8 V CMOS or LVDS outputs
- SNR = 74.5 dBFS at 70 MHz
- SFDR = 91 dBc at 70 MHz
- Low power: 106 mW/channel at 125 MSPS
- Differential analog input with 650 MHz bandwidth
- IF sampling frequencies to 200 MHz
- On-chip voltage reference and sample-and-hold circuit
- 2 V p-p differential analog input
- DNL = ±0.5 LSB at 25°C
- Serial port control options
  - Offset binary, gray code, or twos complement data format
  - Optional clock duty cycle stabilizer
  - Integer 1-to-8 input clock divider
  - Data output multiplex option
  - Built-in selectable digital test pattern generation
  - Energy-saving power-down modes
  - Data clock out with programmable clock and data alignment

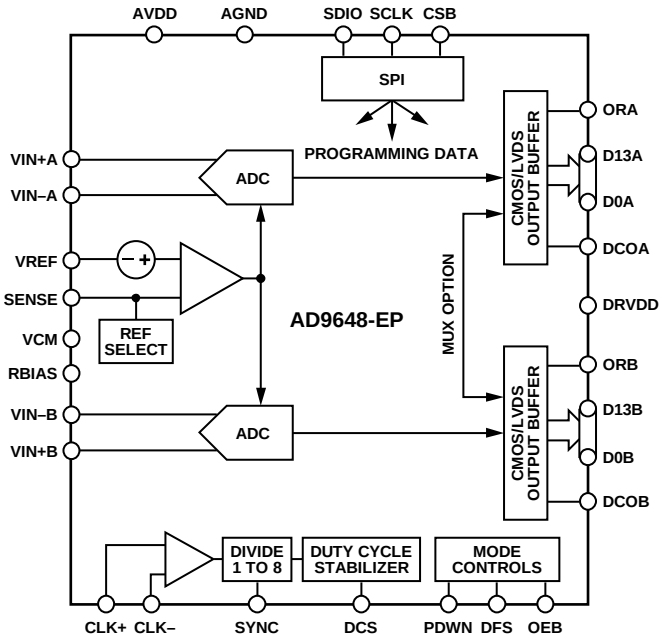
ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range: −55°C to +125°C
- Controlled manufacturing baseline
- Qualification data available on request

APPLICATIONS

- Communications
- Diversity radio systems
- Multimode digital receivers
  - GSM, EDGE, W-CDMA, LTE, CDMA2000, WiMAX, TD-SCDMA
- I/Q demodulation systems
- Smart antenna systems
- Broadband data applications
- Battery-powered instruments
- Handheld scope meters
- Portable medical imaging
- Ultrasound
- Radar/LIDAR

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. PIN NAMES ARE FOR THE CMOS PIN CONFIGURATION ONLY; SEE FIGURE 7 FOR LVDS PIN NAMES.

13386-001

Figure 1.

PRODUCT HIGHLIGHTS

1. The AD9648-EP operates from a single 1.8 V analog power supply and features a separate digital output driver supply to accommodate 1.8 V CMOS or LVDS logic families.
2. The sample-and-hold circuit maintains excellent performance for input frequencies up to 200 MHz and is designed for low cost, low power, and ease of use.
3. A standard serial port interface supports various product features and functions, such as data output formatting, internal clock divider, power-down, DCO/data timing and offset adjustments.
4. The AD9648-EP is packaged in a 64-lead, RoHS-compliant LFCSP that is pin-compatible with the AD9650/AD9269/AD9268 16-bit ADC, the AD9258 14-bit ADC, the AD9628/AD9231 12-bit ADCs, and the AD9608/AD9204 10-bit ADCs, enabling a simple migration path between 10-bit and 16-bit converters sampling from 20 MSPS to 125 MSPS.

Rev. B
Document Feedback

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GENERAL DESCRIPTION

The AD9648-EP is a monolithic, dual-channel, 1.8 V supply, 14-bit, 125 MSPS analog-to-digital converter (ADC). It features a high performance sample-and-hold circuit and on-chip voltage reference.

The product uses multistage differential pipeline architecture with output error correction logic to provide 14-bit accuracy at 125 MSPS data rates and to guarantee no missing codes over the full operating temperature range.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

A differential clock input controls all internal conversion cycles. An optional duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance.

The digital output data is presented in offset binary, Gray code, or twos complement format. A data output clock (DCO) is provided for each ADC channel to ensure proper latch timing with receiving logic. Output logic levels of 1.8 V CMOS or LVDS are supported. Output data can also be multiplexed onto a single output bus.

The AD9648-EP is available in a 64-lead RoHS-compliant LFCSP and is specified over the −55°C to +125°C temperature range. Additional information, including Typical Performance Characteristics at 125 MSPS, can be found in the AD9648 data sheet.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 1.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION	Full	14			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−0.8	−0.3	+0.2	% FSR
Gain Error	Full	−6.3	±1.3	+6.3	% FSR
Differential Nonlinearity (DNL)[1]	Full	−0.7		+1.3	LSB
	25°C		±0.5		LSB
Integral Nonlinearity (INL)[1]	Full	−2.6		+2.6	LSB
	25°C		±1.0		LSB
MATCHING CHARACTERISTIC					
Offset Error	Full		±0.01	±0.8	% FSR
Gain Error	Full		±0.5	±7.0	% FSR
TEMPERATURE DRIFT					
Offset Error	Full		±2		ppm/°C
Gain Error	Full		±50		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage (1 V Mode)	Full	0.98	1.00	1.02	V
Load Regulation Error at 1.0 mA	Full		2		mV
INPUT REFERRED NOISE					
VREF = 1.0 V	25°C		0.98		LSB rms
ANALOG INPUT					
Input Span, VREF = 1.0 V	Full		2		V p-p
Input Capacitance[2]	Full		5		pF
Input Resistance (Differential)	Full		7.5		kΩ
Input Common-Mode Voltage	Full		0.9		V
Input Common-Mode Range	Full	0.5		1.3	V
POWER SUPPLIES					
Supply Voltage					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
Supply Current					
I_{AVDD}[1]	Full		95	100	mA
I_{DRVDD} (1.8 V CMOS)[1]	Full		22.5	23.8	mA
I_{DRVDD}(1.8 V LVDS)[1]	Full		65.0	66.4	mA
POWER CONSUMPTION					
DC Input	Full		155.5		mW
Sine Wave Input (DRVDD = 1.8 V CMOS Output Mode)	Full		211.5	223	mW
Sine Wave Input (DRVDD = 1.8 V LVDS Output Mode)	Full		288	300	mW
Standby Power[3]	Full		120		mW
Power-Down Power	Full		2.0		mW

[1] Measure with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND.
[3] Standby power is measured with a dc input and with the CLK± pins active (1.8 V CMOS mode).

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 2.

Parameter[1]	Temperature	Min	Typ	Max	Unit
SIGNAL-TO-NOISE-RATIO (SNR)					
f_{IN} = 9.7 MHz	25°C		75.0		dBFS
f_{IN} = 30.5 MHz	25°C		74.7		dBFS
f_{IN} = 70 MHz	25°C		74.5		dBFS
	Full	72.5			dBFS
f_{IN} = 100 MHz	25°C		73.9		dBFS
f_{IN} = 200 MHz	25°C		71.5		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)					
f_{IN} = 9.7 MHz	25°C		73.9		dBFS
f_{IN} = 30.5 MHz	25°C		73.4		dBFS
f_{IN} = 70 MHz	25°C		73.3		dBFS
	Full	72.3			dBFS
f_{IN} = 100 MHz	25°C		72.8		dBFS
f_{IN} = 200 MHz	25°C		70.3		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 9.7 MHz	25°C		12		Bits
f_{IN} = 30.5 MHz	25°C		11.9		Bits
f_{IN} = 70 MHz	Full	11.8	11.9		Bits
f_{IN} = 100 MHz	25°C		11.8		Bits
f_{IN} = 200 MHz	25°C		11.4		Bits
WORST SECOND OR THIRD HARMONIC					
f_{IN} = 9.7 MHz	25°C		−96		dBc
f_{IN} = 30.5 MHz	25°C		−90		dBc
f_{IN} = 70 MHz	25°C		−91		dBc
	Full			−82	dBc
f_{IN} = 100 MHz	25°C		−90		dBc
f_{IN} = 200 MHz	25°C		−84		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 9.7 MHz	25°C		96		dBc
f_{IN} = 30.5 MHz	25°C		90		dBc
f_{IN} = 70 MHz	25°C		91		dBc
	Full	82			dBc
f_{IN} = 100 MHz	25°C		90		dBc
f_{IN} = 200 MHz	25°C		84		dBc
WORST OTHER (HARMONIC OR SPUR)					
f_{IN} = 9.7 MHz	25°C		−97		dBc
f_{IN} = 30.5 MHz	25°C		−97		dBc
f_{IN} = 70 MHz	25°C		−97		dBc
	Full			−89	dBc
f_{IN} = 100 MHz	25°C		−92		dBc
f_{IN} = 200 MHz	25°C		−90		dBc
TWO-TONE SFDR					
f_{IN} = 29 MHz (−7 dBFS), 32 MHz (−7 dBFS)	25°C		84		dBc
CROSSTALK[2]	Full		−95		dB
ANALOG INPUT BANDWIDTH	25°C		650		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Crosstalk is measured at 100 MHz with −1.0 dBFS on one channel and no input on the alternate channel.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK–)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND − 0.3		AVDD + 0.2	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	−10		+10	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
LOGIC INPUT (CSB)[1]					
High Level Input Voltage	Full	1.22		DRVDD + 0.2	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	40		132	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK/DFS/SYNC)[2]					
High Level Input Voltage	Full	1.22		DRVDD + 0.2	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (VIN = 1.8 V)	Full	−92		−135	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT/OUTPUT (SDIO/DCS)[1]					
High Level Input Voltage	Full	1.22		DRVDD + 0.2	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	38		128	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
LOGIC INPUTS (OEB, PDWN)[2]					
High Level Input Voltage	Full	1.22		DRVDD + 0.2	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (VIN = 1.8 V)	Full	−90		−134	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF

Parameter	Temperature	Min	Typ	Max	Unit
DIGITAL OUTPUTS					
CMOS Mode—DRVDD = 1.8 V					
High Level Output Voltage					
I_{OH} = 50 µA	Full	1.79			V
I_{OH} = 0.5 mA	Full	1.75			V
Low Level Output Voltage					
I_{OL} = 1.6 mA	Full			0.2	V
I_{OL} = 50 µA	Full			0.05	V
LVDS Mode—DRVDD = 1.8 V					
Differential Output Voltage (V_{OD}), ANSI Mode	Full	290	345	400	mV
Output Offset Voltage (V_{OS}), ANSI Mode	Full	1.15	1.25	1.35	V
Differential Output Voltage (V_{OD}), Reduced Swing Mode	Full	160	200	230	mV
Output Offset Voltage (V_{OS}), Reduced Swing Mode	Full	1.15	1.25	1.35	V

[1] Pull up.
[2] Pull down.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

Table 4.

Parameter	Temperature	Min	Typ	Max	Unit
CLOCK INPUT PARAMETERS					
Input Clock Rate	Full			1000	MHz
Conversion Rate[1]					
DCS Enabled	Full	20		125	MSPS
DCS Disabled	Full	10		125	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full		8		ns
CLK Pulse Width High (t_{CH})	Full		4		ns
Aperture Delay (t_A)	Full		1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.137		ps rms
DATA OUTPUT PARAMETERS					
CMOS Mode (DRVDD = 1.8 V)					
Data Propagation Delay (t_{PD})	Full	1.8	2.9	4.4	ns
DCO Propagation Delay (t_{DCO})[2]	Full	2.0	3.1	4.4	ns
DCO to Data Skew (t_{SKEW})	Full	−1.2	−0.1	+1.0	ns
LVDS Mode (DRVDD = 1.8 V)					
Data Propagation Delay (t_{PD})	Full		2.4		ns
DCO Propagation Delay (t_{DCO})[2]	Full		2.4		ns
DCO to Data Skew (t_{SKEW})	Full	−0.20	+0.03	+0.25	ns
CMOS Mode Pipeline Delay (Latency)	Full		16		Cycles
LVDS Mode Pipeline Delay (Latency) Channel A/Channel B	Full		16/16.5		Cycles
Wake-Up Time (Power Down)[3]	Full		350		µs
Wake-Up Time (Standby)	Full		250		ns
Out-of-Range Recovery Time	Full		2		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] Additional DCO delay can be added by writing to Bits[2:0] in SPI Register 0x17 (see the standard AD9648 datasheet).
[3] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Description	Limit	Unit
SYNC TIMING REQUIREMENTS			
t_{SSYNC}	SYNC to rising edge of CLK+ setup time	0.24	ns typ
t_{HSYNC}	SYNC to rising edge of CLK+ hold time	0.40	ns typ
SPI TIMING REQUIREMENTS			
t_{DS}	Setup time between the data and the rising edge of SCLK	2	ns min
t_{DH}	Hold time between the data and the rising edge of SCLK	2	ns min
t_{CLK}	Period of the SCLK	40	ns min
t_S	Setup time between CSB and SCLK	2	ns min
t_H	Hold time between CSB and SCLK	2	ns min
t_{HIGH}	SCLK pulse width high	10	ns min
t_{LOW}	SCLK pulse width low	10	ns min
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10	ns min
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10	ns min

Timing Diagrams

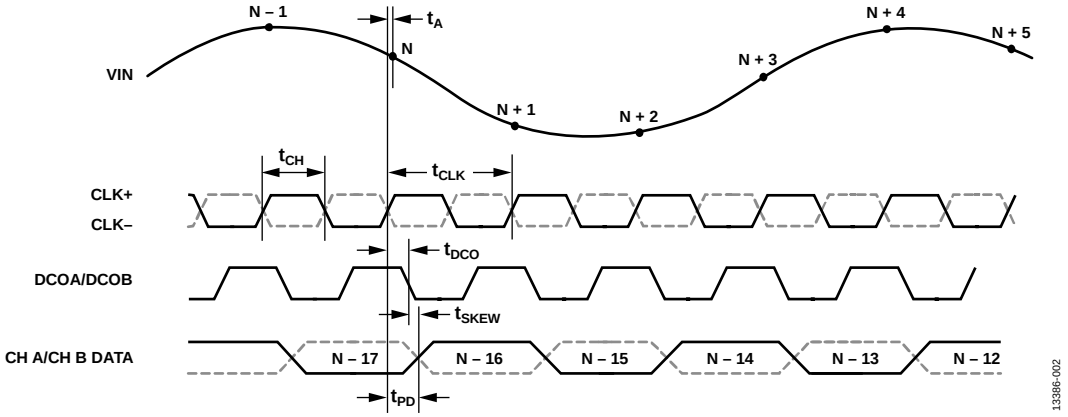


Figure 2. CMOS Default Output Mode Data Output Timing

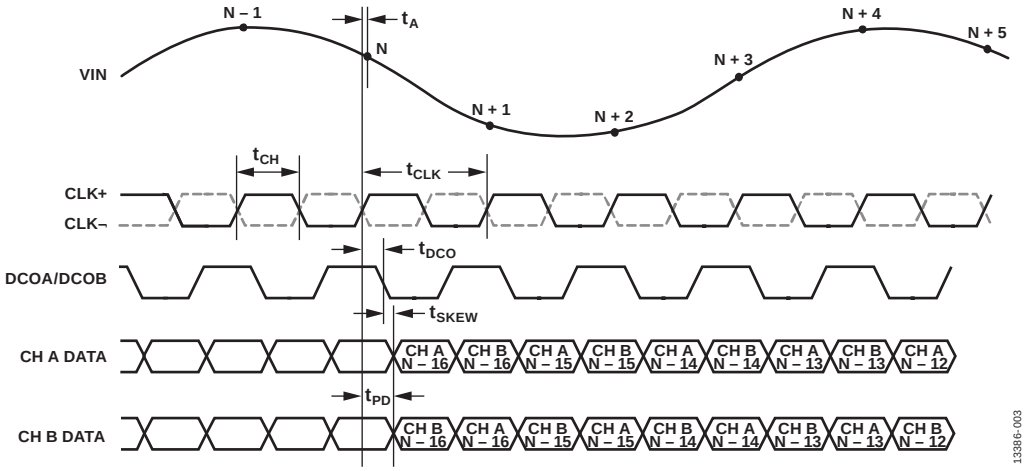


Figure 3. CMOS Interleaved Output Mode Data Output Timing

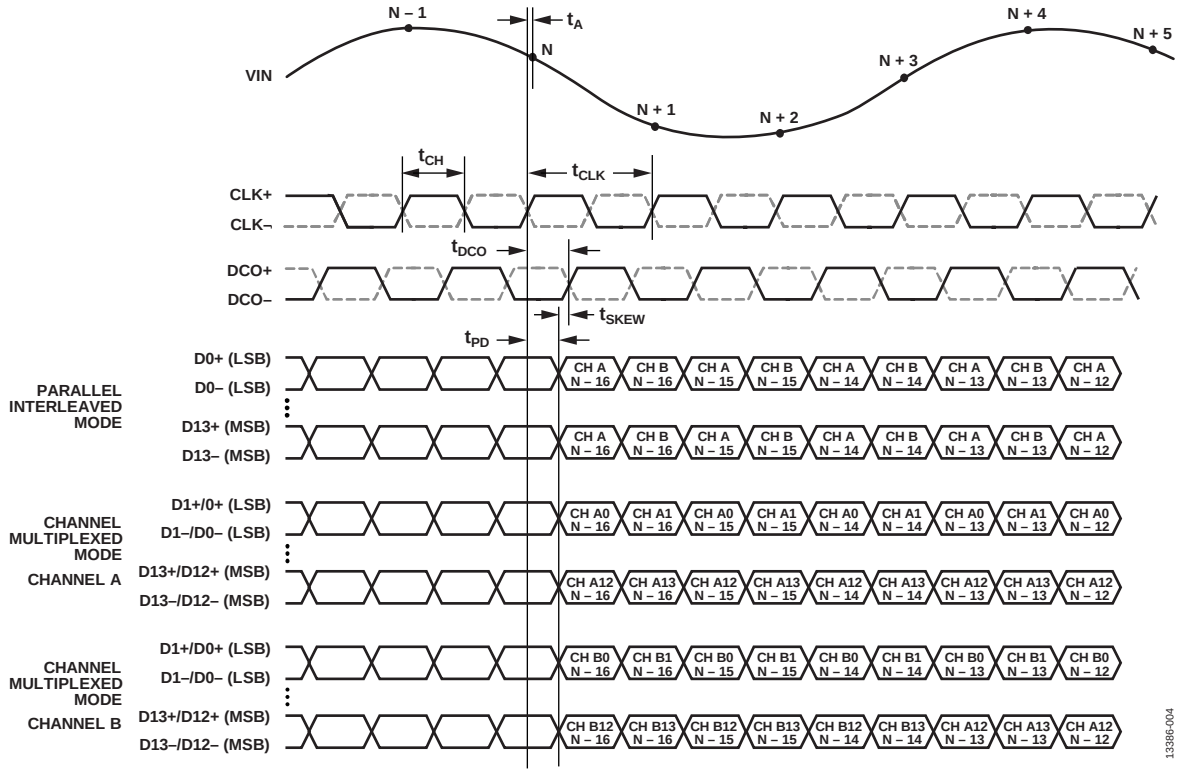


Figure 4. LVDS Modes for Data Output Timing

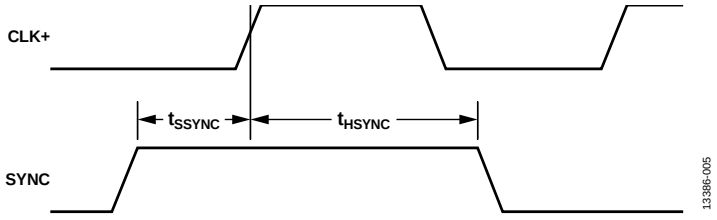


Figure 5. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
VIN+A/VIN+B, VIN−A/VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
SYNC to DRVDD	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
RBIAS to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.2 V
SCLK/DFS to AGND	−0.3 V to DRVDD + 0.2 V
SDIO/DCS to AGND	−0.3 V to DRVDD + 0.2 V
OEB	−0.3 V to DRVDD + 0.2 V
PDWN	−0.3 V to DRVDD + 0.2 V
D0A/D0B through D13A/D13B to AGND	−0.3 V to DRVDD + 0.2 V
DCOA/DCOB to AGND	−0.3 V to DRVDD + 0.2 V
Environmental	
Operating Temperature Range (Ambient)	−55°C to +125°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the printed circuit board (PCB) increases the reliability of the solder joints and maximizes the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Ψ_{JT}[1, 2]	Unit
64-Lead LFCSP 9 mm × 9 mm (CP-64-4)	0	22.3	1.4	11.8	0.1	°C/W
	1.0	19.5	N/A	N/A	0.2	°C/W
	2.5	17.5	N/A	N/A	0.2	°C/W

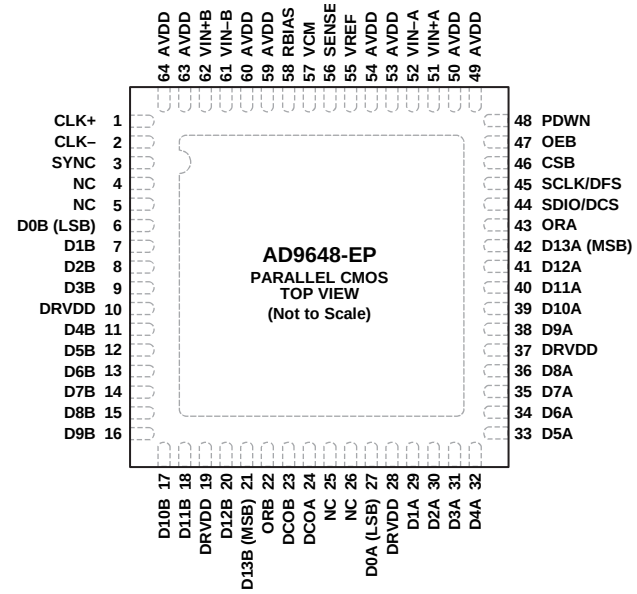
[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown Table 7, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE DEVICE. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

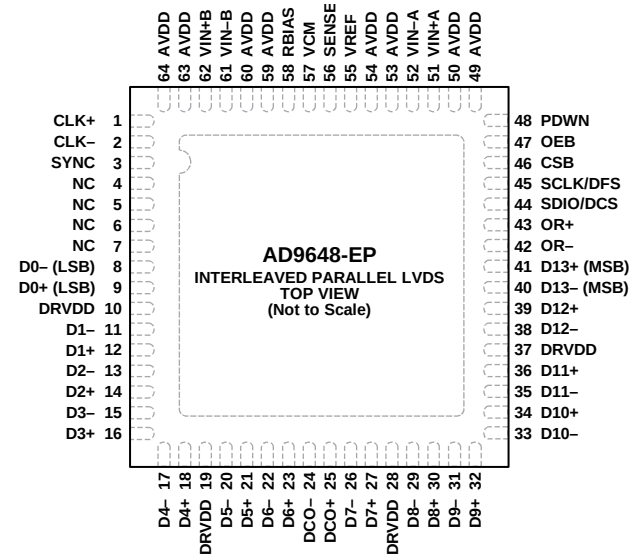
13386-006

Figure 6. Parallel CMOS Pin Configuration (Top View)

Table 8. Pin Function Descriptions (Parallel CMOS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
4, 5, 25, 26	NC		No Connect. Do not connect to these pins.
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the device. This exposed pad must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
55	VREF	Input/Output	Voltage Reference Input/Output.
56	SENSE	Input	Reference Mode Selection.
58	RBIAS	Input/Output	External Reference Bias Resistor. Connect to a 10 kΩ (1% tolerance) resistor to ground.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs.
1	CLK+	Input	ADC Clock Input—True.
2	CLK−	Input	ADC Clock Input—Complement.
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.

Pin No.	Mnemonic	Type	Description
Digital Outputs			
27	D0A (LSB)	Output	Channel A CMOS Output Data.
29	D1A	Output	Channel A CMOS Output Data.
30	D2A	Output	Channel A CMOS Output Data.
31	D3A	Output	Channel A CMOS Output Data.
32	D4A	Output	Channel A CMOS Output Data.
33	D5A	Output	Channel A CMOS Output Data.
34	D6A	Output	Channel A CMOS Output Data.
35	D7A	Output	Channel A CMOS Output Data.
36	D8A	Output	Channel A CMOS Output Data.
38	D9A	Output	Channel A CMOS Output Data.
39	D10A	Output	Channel A CMOS Output Data.
40	D11A	Output	Channel A CMOS Output Data.
41	D12A	Output	Channel A CMOS Output Data.
42	D13A (MSB)	Output	Channel A CMOS Output Data.
43	ORA	Output	Channel A Overrange Output.
6	D0B (LSB)	Output	Channel B CMOS Output Data.
7	D1B	Output	Channel B CMOS Output Data.
8	D2B	Output	Channel B CMOS Output Data.
9	D3B	Output	Channel B CMOS Output Data.
11	D4B	Output	Channel B CMOS Output Data.
12	D5B	Output	Channel B CMOS Output Data.
13	D6B	Output	Channel B CMOS Output Data.
14	D7B	Output	Channel B CMOS Output Data.
15	D8B	Output	Channel B CMOS Output Data.
16	D9B	Output	Channel B CMOS Output Data.
17	D10B	Output	Channel B CMOS Output Data.
18	D11B	Output	Channel B CMOS Output Data.
20	D12B	Output	Channel B CMOS Output Data.
21	D13B (MSB)	Output	Channel B CMOS Output Data.
22	ORB	Output	Channel B Overrange Output
24	DCOA	Output	Channel A Data Clock Output.
23	DCOB	Output	Channel B Data Clock Output.
SPI Control			
45	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
44	SDIO/DCS	Input/Output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
46	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
47	OEB	Input	Output Enable Input (Active Low).
48	PDWN	Input	Power-Down Input in External Pin Mode. In SPI mode, this input can be configured as power-down or standby.



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE DEVICE. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

13386-007

Figure 7. Interleaved Parallel LVDS Pin Configuration (Top View)

Table 9. Pin Function Descriptions (Interleaved Parallel LVDS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
4, 5, 6, 7	NC		No Connect. Do not connect to these pins.
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the device. This exposed pad must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN−A	Input	Differential Analog Input Pin (–) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN−B	Input	Differential Analog Input Pin (–) for Channel B.
55	VREF	Input/Output	Voltage Reference Input/Output.
56	SENSE	Input	Reference Mode Selection.
58	RBIAS	Input/Output	External Reference Bias Resistor. Connect to a 10 kΩ (1% tolerance) resistor to ground.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs.
1	CLK+	Input	ADC Clock Input—True.
2	CLK–	Input	ADC Clock Input—Complement.
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.

Pin No.	Mnemonic	Type	Description
Digital Outputs			
9	D0+ (LSB)	Output	Channel A/Channel B LVDS Output Data 0—True.
8	D0− (LSB)	Output	Channel A/Channel B LVDS Output Data 0—Complement.
12	D1+	Output	Channel A/Channel B LVDS Output Data 1—True.
11	D1−	Output	Channel A/Channel B LVDS Output Data 1—Complement.
14	D2+	Output	Channel A/Channel B LVDS Output Data 2—True.
13	D2−	Output	Channel A/Channel B LVDS Output Data 2—Complement.
16	D3+	Output	Channel A/Channel B LVDS Output Data 3—True.
15	D3−	Output	Channel A/Channel B LVDS Output Data 3—Complement.
18	D4+	Output	Channel A/Channel B LVDS Output Data 4—True.
17	D4−	Output	Channel A/Channel B LVDS Output Data 4—Complement.
21	D5+	Output	Channel A/Channel B LVDS Output Data 5—True.
20	D5−	Output	Channel A/Channel B LVDS Output Data 5—Complement.
23	D6+	Output	Channel A/Channel B LVDS Output Data 6—True.
22	D6−	Output	Channel A/Channel B LVDS Output Data 6—Complement.
27	D7+	Output	Channel A/Channel B LVDS Output Data 7—True.
26	D7−	Output	Channel A/Channel B LVDS Output Data 7—Complement.
30	D8+	Output	Channel A/Channel B LVDS Output Data 8—True.
29	D8−	Output	Channel A/Channel B LVDS Output Data 8—Complement.
32	D9+	Output	Channel A/Channel B LVDS Output Data 9—True.
31	D9−	Output	Channel A/Channel B LVDS Output Data 9—Complement.
34	D10+	Output	Channel A/Channel B LVDS Output Data 10—True.
33	D10−	Output	Channel A/Channel B LVDS Output Data 10—Complement.
36	D11+	Output	Channel A/Channel B LVDS Output Data 11—True.
35	D11−	Output	Channel A/Channel B LVDS Output Data 11—Complement.
39	D12+	Output	Channel A/Channel B LVDS Output Data 12—True.
38	D12−	Output	Channel A/Channel B LVDS Output Data 12—Complement.
41	D13+ (MSB)	Output	Channel A/Channel B LVDS Output Data 13—True.
40	D13− (MSB)	Output	Channel A/Channel B LVDS Output Data 13—Complement.
43	OR+	Output	Channel A/Channel B LVDS Overrange Output—True.
42	OR−	Output	Channel A/Channel B LVDS Overrange Output—Complement.
25	DCO+	Output	Channel A/Channel B LVDS Data Clock Output—True.
24	DCO−	Output	Channel A/Channel B LVDS Data Clock Output—Complement.
SPI Control			
45	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
44	SDIO/DCS	Input/Output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
46	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
47	OEB	Input	Output Enable Input (Active Low).
48	PDWN	Input	Power-Down Input in External Pin Mode. In SPI mode, this input can be configured as power-down or standby.

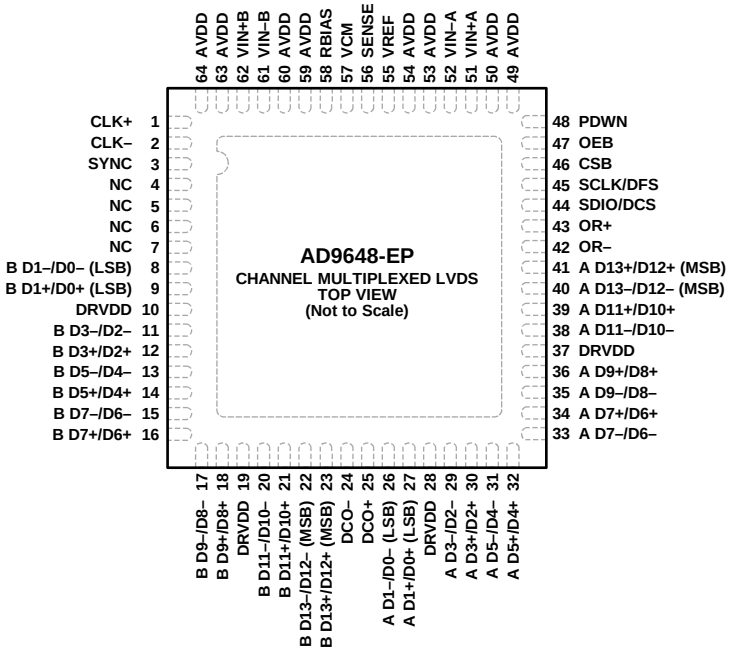


Figure 8. Channel Multiplexed LVDS Pin Configuration (Top View)

Table 10 Pin Function Descriptions (Channel Multiplexed Parallel LVDS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
10, 19, 28, 37	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
49, 50, 53, 54, 59, 60, 63, 64	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
4, 5, 6, 7	NC		Do Not Connect.
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the device. This exposed pad must be connected to ground for proper operation.
ADC Analog			
51	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
52	VIN−A	Input	Differential Analog Input Pin (–) for Channel A.
62	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
61	VIN−B	Input	Differential Analog Input Pin (–) for Channel B.
55	VREF	Input/Output	Voltage Reference Input/Output.
56	SENSE	Input	Reference Mode Selection.
58	RBIAS	Input/Output	External Reference Bias Resistor. Connect to a 10 kΩ (1% tolerance) resistor to ground.
57	VCM	Output	Common-Mode Level Bias Output for Analog Inputs.
1	CLK+	Input	ADC Clock Input—True.
2	CLK−	Input	ADC Clock Input—Complement.
Digital Input			
3	SYNC	Input	Digital Synchronization Pin. Slave mode only.

Pin No.	Mnemonic	Type	Description
Digital Outputs			
8	B D1−/D0− (LSB)	Output	Channel B LVDS Output Data 1/Data 0—Complement.
9	B D1+/D0+ (LSB)	Output	Channel B LVDS Output Data 1/Data 0—True.
11	B D3−/D2−	Output	Channel B LVDS Output Data 3/Data 2—Complement.
12	B D3+/D2+	Output	Channel B LVDS Output Data 3/Data 2—True.
13	B D5−/D4−	Output	Channel B LVDS Output Data 5/Data 4—Complement.
14	B D5+/D4+	Output	Channel B LVDS Output Data 5/Data 4—True.
15	B D7−/D6−	Output	Channel B LVDS Output Data 7/Data 6—Complement.
16	B D7+/D6+	Output	Channel B LVDS Output Data 7/Data 6—True.
17	B D9−/D8−	Output	Channel B LVDS Output Data 9/Data 8—Complement.
18	B D9+/D8+	Output	Channel B LVDS Output Data 9/Data 8—True.
20	B D11−/D10−	Output	Channel B LVDS Output Data 11/Data 10—Complement.
21	B D11+/D10+	Output	Channel B LVDS Output Data 11/Data 10—True.
22	B D13−/D12− (MSB)	Output	Channel B LVDS Output Data 13/Data 12—Complement.
23	B D13+/D12+ (MSB)	Output	Channel B LVDS Output Data 13/Data 12—True.
26	A D1−/D0− (LSB)	Output	Channel A LVDS Output Data 1/Data 0—Complement.
27	A D1+/D0+ (LSB)	Output	Channel A LVDS Output Data 1/Data 0—True.
29	A D3−/D2−	Output	Channel A LVDS Output Data 3/Data 2—Complement.
30	A D3+/D2+	Output	Channel A LVDS Output Data 3/Data 2—True.
32	A D5+/D4+	Output	Channel A LVDS Output Data 5/Data 4—True.
31	A D5−/D4−	Output	Channel A LVDS Output Data 5/Data 4—Complement.
34	A D7+/D6+	Output	Channel A LVDS Output Data 7/Data 6—True.
33	A D7−/D6−	Output	Channel A LVDS Output Data 7/Data 6—Complement.
36	A D9+/D8+	Output	Channel A LVDS Output Data 9/Data 8—True.
35	A D9−/D8−	Output	Channel A LVDS Output Data 9/Data 8—Complement.
39	A D11+/D10+	Output	Channel A LVDS Output Data 11/Data 10—True.
38	A D11−/D10−	Output	Channel A LVDS Output Data 11/Data 10—Complement.
41	A D13+/D12+ (MSB)	Output	Channel A LVDS Output Data 13/Data 12—True.
40	A D13−/D12− (MSB)	Output	Channel A LVDS Output Data 13/Data 12—Complement.
43	OR+	Output	Channel A/Channel B LVDS Overrange Output—True.
42	OR−	Output	Channel A/Channel B LVDS Overrange Output—Complement.
25	DCO+	Output	Channel A/Channel B LVDS Data Clock Output—True.
24	DCO−	Output	Channel A/Channel B LVDS Data Clock Output—Complement.
SPI Control			
45	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
44	SDIO/DCS	Input/Output	SPI Serial Data I/O/Duty Cycle Stabilizer Pin in External Pin Mode.
46	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
47	OEB	Input	Output Enable Input (Active Low).
48	PDWN	Input	Power-Down Input in External Pin Mode. In SPI mode, this input can be configured as power-down or standby.

OUTLINE DIMENSIONS

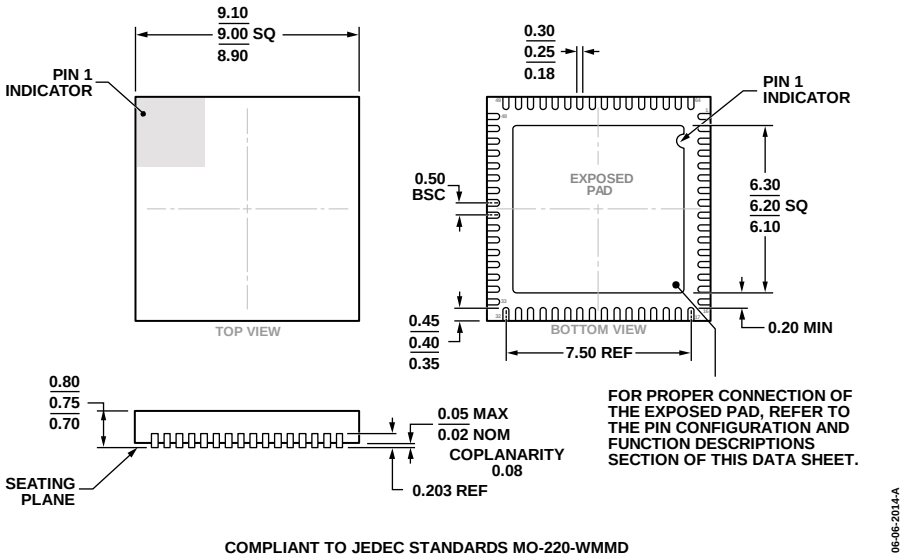


Figure 9. 64-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
9 mm × 9 mm Body, Very Very Thin Quad
(CP-64-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9648TCPZ-125-EP	−55°C to +125°C	64-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-64-17
AD9648TCPZ125EPRL7	−55°C to +125°C	64-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-64-17

[1] Z = RoHS Compliant Part.

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