14-Bit, 500 MSPS, JESD204B, Quad Analog-to-Digital Converter

Data Sheet **AD9694**

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
  - Lane rates up to 15 Gbps
- 1.66 W total power at 500 MSPS
  - 415 mW per ADC channel
- SFDR = 82 dBFS at 305 MHz (1.80 V p-p input range)S
- SNR = 66.8 dBFS at 305 MHz (1.80 V p-p input range)
- Noise density = −151.5 dBFS/Hz (1.80 V p-p input range)
- 0.975 V, 1.8 V, and 2.5 V dc supply operation
- No missing codes
- Internal ADC voltage reference
- Analog input buffer
- On-chip dithering to improve small signal linearity
- Flexible differential input range
  - 1.44 V p-p to 2.16 V p-p (1.80 V p-p nominal)
- 1.4 GHz analog input full power bandwidth
- Amplitude detect bits for efficient AGC implementation
- 4 integrated wideband digital processors
  - 48-bit NCO, up to 4 cascaded half-band filters
- Differential clock input
- Integer clock divide by 1, 2, 4, or 8
- On-chip temperature diode
- Flexible JESD204B lane configurations

APPLICATIONS

- Communications
- Diversity multiband, multimode digital receivers
  - 3G/4G, W-CDMA, GSM, LTE, LTE-A
- General-purpose software radios
- Ultrawideband satellite receivers
- Instrumentation
- Radars
- Signals intelligence (SIGINT)

FUNCTIONAL BLOCK DIAGRAM

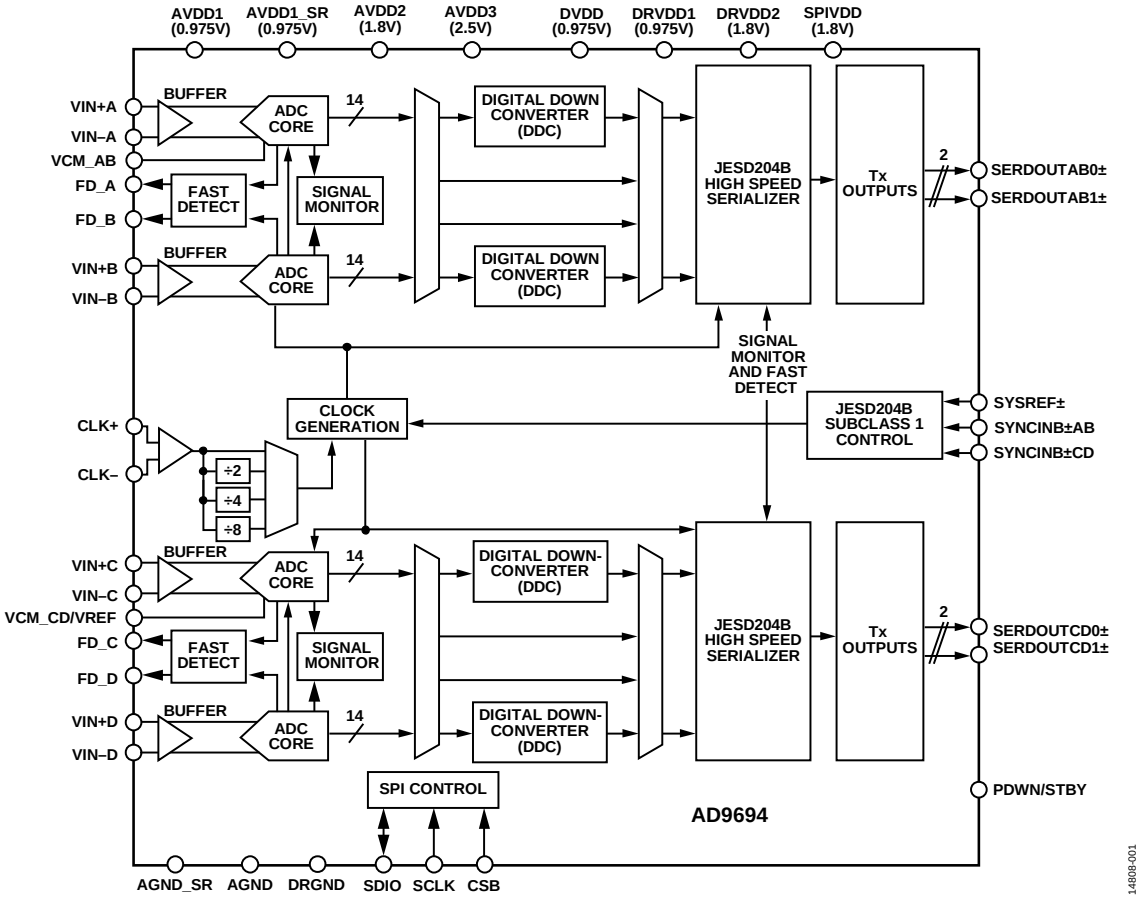

Figure 1.

Rev. B Document Feedback

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REVISION HISTORY

2/2018—Rev. A to Rev. B

Changed Document Title from Dual 14-Bit, 1.25 GSPS, 1.2 V/ 2.5 V Analog-to-Digital Converter to 14-Bit, 500 MSPS, JESD204B Analog-to-Digital Converter ..... Universal
Change to Table 10 14
Moved Temperature Diode Section 28

12/2017—Rev. 0 to Rev. A

Changed 1.8 V p-p to 1.80 V p-p ..... Throughout
Changes to Figure 1 1
Changes to Endnote 3, Table 2 7
Changes to Logic Outputs (FD_A, FD_B, FD_C, FD_D) Parameter and DIGITAL OUTPUTS (SERDOUTABx±/ SERDOUTCDx±, x = 0 OR 1) Parameter, Table 5 9
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Added Example Latency Calculations Section, Example Configuration 1 Section, Example Configuration 2 Section, Table 29, and Table 30; Renumbered Sequentially 60
Added Deterministic Latency Section, Subclass 0 Operation Section, Subclass 1 Operation Section, Deterministic Latency Requirements Section, Setting Deterministic Latency Registers Section, and Figure 94; Renumbered Sequentially 61
Added Figure 95 and Figure 96 62
Added Multichip Synchronization Section, Normal Mode Section, Timestamp Mode Section, Figure 97 63
Added Figure 98 64
Added SYSREF± Input Section, SYSREF± Control Features Section, Figure 99, Figure 100, Figure 101, and Figure 102 65
Changes to SYSREF± Setup/Hold Window Monitor Section 66
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Deleted Register Table Summary Section and Table 38; Renumbered Sequentially 69
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10/2016—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9694 is a quad, 14-bit, 500 MSPS analog-to-digital converter (ADC). The device has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This device is designed for sampling wide bandwidth analog signals of up to 1.4 GHz. The AD9694 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The quad ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The analog inputs and clock signals are differential inputs. Each pair of ADC data outputs is internally connected to two DDCs through a crossbar mux. Each DDC consists of up to five cascaded signal processing stages: a 48-bit frequency translator, NCO, and up to four half-band decimation filters.

In addition to the DDC blocks, the AD9694 has several functions that simplify the automatic gain control (AGC) function in the communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

Users can configure each pair of intermediate frequency (IF) receiver outputs onto either one or two lanes of Subclass 1 JESD204B-based high speed serialized outputs, depending on the decimation ratio and the acceptable lane rate of the receiving logic device. Multiple device synchronization is supported through the SYSREF±, SYNCINB±AB, and SYNCINB±CD input pins.

The AD9694 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using the 1.8 V capable, 3-wire SPI.

The AD9694 is available in a Pb-free, 72-lead LFCSP and is specified over the −40°C to +105°C junction temperature range. This product may be protected by one or more U.S. or international patents.

PRODUCT HIGHLIGHTS

1. Low power consumption per channel.
2. JESD204B lane rate support up to 15 Gbps.
3. Wide full power bandwidth supports IF sampling of signals up to 1.4 GHz.
4. Buffered inputs ease filter design and implementation.
5. Four integrated wideband decimation filters and numerically controlled oscillator (NCO) blocks supporting multiband receivers.
6. Programmable fast overrange detection.
7. On-chip temperature diode for system thermal management.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, 500 MSPS, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = 50°C (T_A = 25°C).

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION	14			Bits
ACCURACY				
No Missing Codes		Guaranteed		
Offset Error		0		% FSR
Offset Matching		0		% FSR
Gain Error	−5.0		+5.0	% FSR
Gain Matching		1.0	3.7	% FSR
Differential Nonlinearity (DNL)	−0.7	±0.4	+0.7	LSB
Integral Nonlinearity (INL)	−5.1	±1.0	+5.1	LSB
TEMPERATURE DRIFT				
Offset Error		8		ppm/°C
Gain Error		214		ppm/°C
INTERNAL VOLTAGE REFERENCE		0.5		V
INPUT REFERRED NOISE		2.6		LSB rms
ANALOG INPUTS				
Differential Input Voltage Range (Programmable)	1.44	1.80	2.16	V p-p
Common-Mode Voltage (V_{CM})		1.34		V
Differential Input Capacitance[1]		1.75		pF
Differential Input Resistance		200		Ω
Analog Input Full Power Bandwidth		1.4		GHz
POWER SUPPLY				
AVDD1	0.95	0.975	1.00	V
AVDD1_SR	0.95	0.975	1.00	V
AVDD2	1.71	1.8	1.89	V
AVDD3	2.44	2.5	2.56	V
DVDD	0.95	0.975	1.00	V
DRVDD1	0.95	0.975	1.00	V
DRVDD2	1.71	1.8	1.89	V
SPIVDD	1.71	1.8	1.89	V
I_{AVDD1}		319	482	mA
I_{AVDD1_SR}		21	53	mA
I_{AVDD2}		438	473	mA
I_{AVDD3}		87	103	mA
I_{DVDD}[2]		121	180	mA
I_{DRVDD1}[1]		162	207	mA
I_{DRVDD2}[1]		23	29	mA
I_{SPIVDD}		1	1.6	mA
POWER CONSUMPTION				
Total Power Dissipation (Including Output Drivers)[2]		1.66	2.07	W
Power-Down Dissipation		325		mW
Standby[3]		1.20		W

[1] All lanes running. Power dissipation on DRVDD1 changes with lane rate and number of lanes used.
[2] Full bandwidth mode.
[3] Standby mode is controlled by the SPI.

AC SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, specified maximum sampling rate, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = 50°C (T_A = 25°C).

Table 2. 500 MSPS AC Specifications

	Analog Input Full Scale = 1.44 V p-p			Analog Input Full Scale = 1.80 V p-p			Analog Input Full Scale = 2.16 V p-p			
Parameter[1]	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
ANALOG INPUT FULL SCALE		1.44			1.80			2.16		V p-p
NOISE DENSITY[2]		−149.7			−151.5			−153.0		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)[3]										
f_{IN} = 10 MHz		65.4			67.1			68.4		dBFS
f_{IN} = 155 MHz		65.3		64.8	67.0			68.3		dBFS
f_{IN} = 305 MHz		65.2			66.8			68.0		dBFS
f_{IN} = 450 MHz		65.0			66.6			67.8		dBFS
f_{IN} = 765 MHz		64.8			66.5			67.5		dBFS
f_{IN} = 985 MHz		64.5			66.0			66.9		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)										
f_{IN} = 10 MHz		65.3			67.0			68.2		dBFS
f_{IN} = 155 MHz		65.2		64.5	66.8			67.9		dBFS
f_{IN} = 305 MHz		65.1			66.6			67.6		dBFS
f_{IN} = 450 MHz		65.0			66.4			67.3		dBFS
f_{IN} = 765 MHz		64.7			66.1			66.9		dBFS
f_{IN} = 985 MHz		64.2			65.5			66.2		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)										
f_{IN} = 10 MHz		10.5			10.8			11.0		Bits
f_{IN} = 155 MHz		10.5		10.4	10.8			10.9		Bits
f_{IN} = 305 MHz		10.5			10.7			10.9		Bits
f_{IN} = 450 MHz		10.5			10.7			10.8		Bits
f_{IN} = 765 MHz		10.4			10.6			10.8		Bits
f_{IN} = 985 MHz		10.3			10.6			10.7		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)										
f_{IN} = 10 MHz		89			90			80		dBFS
f_{IN} = 155 MHz		89		75	85			77		dBFS
f_{IN} = 305 MHz		82			82			78		dBFS
f_{IN} = 450 MHz		82			83			77		dBFS
f_{IN} = 765 MHz		77			75			72		dBFS
f_{IN} = 985 MHz		82			79			76		dBFS
SPURIOUS-FREE DYNAMIC RANGE (SFDR) AT −3 dBFS										
f_{IN} = 10 MHz		94			94			86		dBFS
f_{IN} = 155 MHz		94			90			82		dBFS
f_{IN} = 305 MHz		89			90			83		dBFS
f_{IN} = 450 MHz		87			86			84		dBFS
f_{IN} = 765 MHz		82			80			77		dBFS
f_{IN} = 985 MHz		85			82			79		dBFS
WORST HARMONIC, SECOND OR THIRD										
f_{IN} = 10 MHz		−89			−90			−80		dBFS
f_{IN} = 155 MHz		−89			−85	−75		−77		dBFS
f_{IN} = 305 MHz		−82			−82			−78		dBFS
f_{IN} = 450 MHz		−82			−83			−77		dBFS
f_{IN} = 765 MHz		−77			−75			−72		dBFS
f_{IN} = 985 MHz		−82			−79			−76		dBFS

Parameter[1]	Analog Input Full Scale = 1.44 V p-p Min	Typ	Max	Analog Input Full Scale = 1.80 V p-p Min	Typ	Max	Analog Input Full Scale = 2.16 V p-p Min	Typ	Max	Unit
WORST HARMONIC, SECOND OR THIRD AT −3 dBFS										
f_{IN} = 10 MHz		−94			−94			−86		dBFS
f_{IN} = 155 MHz		−94			−90			−82		dBFS
f_{IN} = 305 MHz		−89			−90			−83		dBFS
f_{IN} = 450 MHz		−87			−86			−84		dBFS
f_{IN} = 765 MHz		−82			−80			−77		dBFS
f_{IN} = 985 MHz		−85			−82			−79		dBFS
WORST OTHER, EXCLUDING SECOND OR THIRD HARMONIC										
f_{IN} = 10 MHz		−96			−98			−99		dBFS
f_{IN} = 155 MHz		−97			−97	−86		−97		dBFS
f_{IN} = 305 MHz		−97			−98			−97		dBFS
f_{IN} = 450 MHz		−95			−96			−96		dBFS
f_{IN} = 765 MHz		−92			−91			−88		dBFS
f_{IN} = 985 MHz		−90			−89			−86		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD), A_{IN1} AND A_{IN2} = −7 dBFS										
f_{IN1} = 154 MHz, f_{IN2} = 157 MHz		−93			−90			−84		dBFS
f_{IN1} = 302 MHz, f_{IN2} = 305 MHz		−90			−90			−84		dBFS
CROSSTALK[4]		82			82			82		dB
FULL POWER BANDWIDTH[5]		1.4			1.4			1.4		GHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] Noise density is measured at a low analog input frequency (30 MHz).
[3] See Table 11 for recommended settings for the buffer current setting.
[4] Crosstalk is measured at 155 MHz with a −1.0 dBFS analog input on one channel and no input on the adjacent channel.
[5] Measured with the circuit shown in Figure 56.

Table 3. 600 MSPS AC Specifications, Analog Input = 1.80 V p-p

Parameter[1]	Min	Typ	Max	Unit
ANALOG INPUT FULL SCALE		1.80		V p-p
SIGNAL-TO-NOISE RATIO (SNR)				
f_{IN} = 10 MHz		66.6		dBFS
f_{IN} = 155 MHz		67		dBFS
f_{IN} = 305 MHz		66.8		dBFS
f_{IN} = 450 MHz		66.4		dBFS
f_{IN} = 765 MHz		66		dBFS
f_{IN} = 985 MHz		65.5		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)				
f_{IN} = 10 MHz		66.5		dBFS
f_{IN} = 155 MHz		66.8		dBFS
f_{IN} = 305 MHz		66.5		dBFS
f_{IN} = 450 MHz		66.3		dBFS
f_{IN} = 765 MHz		65.4		dBFS
f_{IN} = 985 MHz		64.8		dBFS
SPURIOUS-FREE DYNAMIC RANGE (SFDR)				
f_{IN} = 10 MHz		86		dBFS
f_{IN} = 155 MHz		81		dBFS
f_{IN} = 305 MHz		81		dBFS
f_{IN} = 450 MHz		84		dBFS
f_{IN} = 765 MHz		76		dBFS
f_{IN} = 985 MHz		75		dBFS

Parameter[1]	Min	Typ	Max	Unit
WORST HARMONIC, SECOND OR THIRD				
f_{IN} = 10 MHz		−86		dBFS
f_{IN} = 155 MHz		−81		dBFS
f_{IN} = 305 MHz		−81		dBFS
f_{IN} = 450 MHz		−84		dBFS
f_{IN} = 765 MHz		−76		dBFS
f_{IN} = 985 MHz		−75		dBFS

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.

Table 4. 600 MSPS Power Consumption

Parameter	Min	Typ	Max	Unit
POWER SUPPLY				
AVDD1	0.95	0.975	1.00	V
AVDD1_SR	0.95	0.975	1.00	V
AVDD2	1.71	1.8	1.89	V
AVDD3	2.44	2.5	2.56	V
DVDD	0.95	0.975	1.00	V
DRVDD1	0.95	0.975	1.00	V
DRVDD2	1.71	1.8	1.89	V
SPIVDD	1.71	1.8	1.89	V
I_{AVDD1}		352	513	mA
I_{AVDD1_SR}		23	55	mA
I_{AVDD2}		443	478	mA
I_{AVDD3}		87	104	mA
I_{DVDD}[1]		146	200	mA
I_{DRVDD1}[2]		183	235	mA
I_{DRVDD2}[2]		23	28	mA
I_{SPIVDD}		1	1.6	mA
POWER CONSUMPTION				
Total Power Dissipation (Including Output Drivers)		1.75	2.16	W

[1] Full bandwidth mode.
[2] All lanes running. Power dissipation on DRVDD1 changes with lane rate and number of lanes used.

DIGITAL SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, 500 MSPS, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = 50°C (T_A = 25°C).

Table 5.

Parameter	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	600	800	1600	mV p-p
Input Common-Mode Voltage		0.69		V
Input Resistance (Differential)		32		kΩ
Input Capacitance			0.9	pF
SYSTEM REFERENCE (SYSREF) INPUTS (SYSREF+, SYSREF−)[1]				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage	0.6	0.69	2.2	V
Input Resistance (Differential)	18	22		kΩ
Input Capacitance (Single-Ended per Pin)		0.7		pF
LOGIC INPUTS (PDWN/STBY)				
Logic Compliance		CMOS		
Logic 1 Voltage	0.65 × SPIVDD			V
Logic 0 Voltage	0		0.35 × SPIVDD	V
Input Resistance		10		MΩ
LOGIC INPUTS (SDIO, SCLK, CSB)				
Logic Compliance		CMOS		
Logic 1 Voltage	0.65 × SPIVDD			V
Logic 0 Voltage	0		0.35 × SPIVDD	V
Input Resistance		56		kΩ
LOGIC OUTPUT (SDIO)				
Logic Compliance		CMOS		
Logic 1 Voltage (I_{OH} = 800 µA)	SPIVDD − 0.45 V			V
Logic 0 Voltage (I_{OL} = 50 µA)	0		0.45	V
SYNCIN INPUT (SYNCINB+AB/SYNCINB−AB/ SYNCINB+CD/SYNCINB−CD)				
Logic Compliance		LVDS/LVPECL/CMOS		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage	0.6	0.69	2.2	V
Input Resistance (Differential)	18	22		kΩ
Input Capacitance (Single Ended per Pin)		0.7		pF
LOGIC OUTPUTS (FD_A, FD_B, FD_C, FD_D)				
Logic Compliance		CMOS		
Logic 1 Voltage	0.8 × SPIVDD			V
Logic 0 Voltage	0		0.5	V
Input Resistance		56		kΩ
DIGITAL OUTPUTS (SERDOUTABx±/SERDOUTCDx±, x = 0 OR 1)				
Logic Compliance		CML		
Differential Output Voltage		455.8		mV p-p
Short-Circuit Current ($I_{D\ SHORT}$)		15		mA
Differential Termination Impedance		100		Ω

[1] DC-coupled input only.

SWITCHING SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, 500 MSPS, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = 50°C (T_A = 25°C).

Table 6.

Parameter	Min	Typ	Max	Unit
CLOCK				
Clock Rate (at CLK+/CLK− Pins)	0.3		2.4	GHz
Maximum Sample Rate[1]	600			MSPS
Minimum Sample Rate[2]	240			MSPS
Clock Pulse Width High	125			ps
Clock Pulse Width Low	125			ps
OUTPUT				
Unit Interval (UI)[3]	66.67	100	593	ps
Rise Time (t_R) (20% to 80% into 100 Ω Load)		31.25		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)		31.37		ps
PLL Lock Time		5		ms
Data Rate per Channel (Nonreturn-to-Zero (NRZ))[4]	1.6875	10	15	Gbps
LATENCY[5]				
Pipeline Latency		54		Sample clock cycles
Fast Detect Latency			30	Sample clock cycles
WAKE-UP TIME				
From Standby		3		ms
From Power-Down		10		ms
APERTURE				
Aperture Delay (t_A)		160		ps
Aperture Uncertainty (Jitter, t_j)		44		fs rms
Out of Range Recovery Time		1		Sample clock cycles

[1] The maximum sample rate is the clock rate after the divider.
[2] The minimum sample rate operates at 240 MSPS with L = 2 or L = 1. See SPI Register 0x011A to reduce the threshold of the clock detection circuit.
[3] Baud rate = 1/UI. A subset of this range can be supported.
[4] Default L = 2 for each link. This number can be changed based on the sample rate and decimation ratio.
[5] No DDCs used. L = 2, M = 2, F = 2 for each link.

TIMING SPECIFICATIONS

Table 7.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLK+ to SYSREF+ TIMING REQUIREMENTS	See Figure 3				
t_{SU_SR}	Device clock to SYSREF+ setup time		–44.8		ps
t_{H_SR}	Device clock to SYSREF+ hold time		64.4		ps
SPI TIMING REQUIREMENTS	See Figure 4				
t_{DS}	Setup time between the data and the rising edge of SCLK	4			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK must be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK must be in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		6	10	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the CSB rising edge (not shown in Figure 4)	10			ns

Timing Diagrams

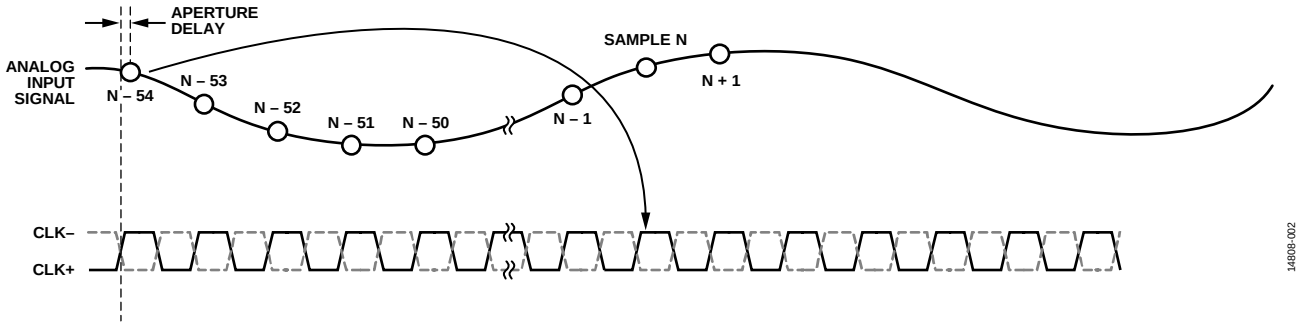


Figure 2. Data Output Timing (Full Bandwidth Mode; L = 4, M = 2, F = 1)

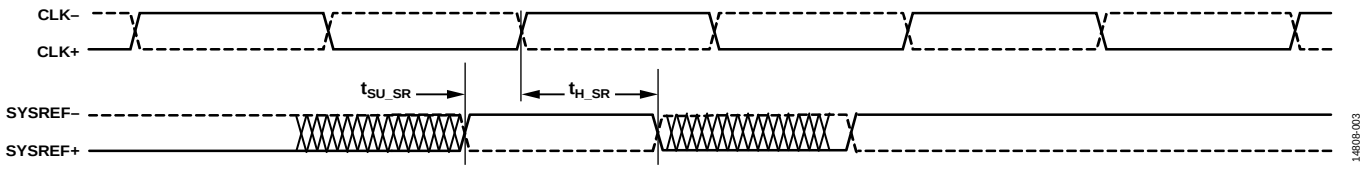


Figure 3. SYSREF± Setup and Hold Timing

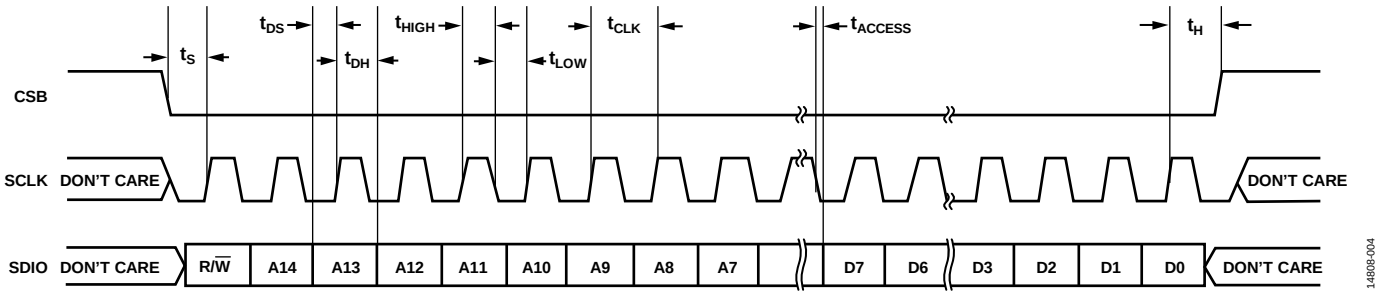


Figure 4. Serial Port Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.05 V
AVDD1_SR to AGND	1.05 V
AVDD2 to AGND	2.00 V
AVDD3 to AGND	2.70 V
DVDD to DGND	1.05 V
DRVDD1 to DRGND	1.05 V
DRVDD2 to DRGND	2.00 V
SPIVDD to AGND	2.00 V
VIN±x to AGND	−0.3 V to AVDD3 + 0.3 V
CLK± to AGND	−0.3 V to AVDD1 + 0.3 V
SCLK, SDIO, CSB to DGND	−0.3 V to SPIVDD + 0.3 V
PDWN/STBY to DGND	−0.3 V to SPIVDD + 0.3 V
SYSREF± to AGND_SR	0 V to 2.5 V
SYNCINB±AB/SYNCINB±CD to DRGND	0 V to 2.5 V
Environmental	
Operating Junction Temperature Range	−40°C to +105°C
Maximum Junction Temperature	125°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC_BOT} is the bottom junction to case thermal resistance.

Table 9. Thermal Resistance

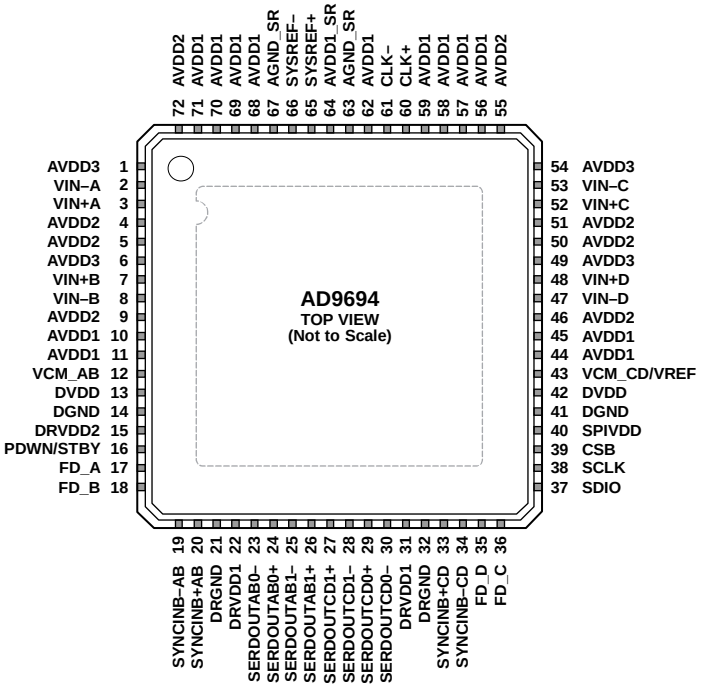
PCB Type	Airflow Velocity (m/sec)	θ_{JA}	θ_{JC_BOT}	Unit
JEDEC 2s2p Board	0.0	21.58[1, 2]	1.95[1, 4]	°C/W
	1.0	17.94[1, 2]	N/A[3]	°C/W
	2.5	16.58[1, 2]	N/A[3]	°C/W
10-Layer Board	0.0	9.74	1.00	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] N/A means not applicable.
[4] Per MIL-STD 883, Method 1012.1.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. ANALOG GROUND. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE GROUND REFERENCE FOR AVDDx, SPIVDD, DVDD, DRVDD1, AND DRVDD2. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

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Figure 5. Pin Configuration (Top View)

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
0	AGND/EPAD	Ground	Exposed Pad. Analog Ground. The exposed thermal pad on the bottom of the package provides the ground reference for AVDDx, SPIVDD, DVDD, DRVDD1, and DRVDD2. This exposed pad must be connected to ground for proper operation.
1, 6, 49, 54	AVDD3	Supply	Analog Power Supply (2.5 V Nominal).
2, 3	VIN−A, VIN+A	Input	ADC A Analog Input Complement/True.
4, 5, 9, 46, 50, 51, 55, 72	AVDD2	Supply	Analog Power Supply (1.8 V Nominal).
7, 8	VIN+B, VIN−B	Input	ADC B Analog Input True/Complement.
10, 11, 44, 45, 56, 57, 58, 59, 62, 68, 69, 70, 71	AVDD1	Supply	Analog Power Supply (0.975 V Nominal).
12	VCM_AB	Output	Common-Mode Level Bias Output for Analog Input Channel A and Channel B.
13, 42	DVDD	Supply	Digital Power Supply (0.975 V Nominal).
14, 41	DGND	Ground	Ground Reference for DVDD and SPIVDD.
15	DRVDD2	Supply	Digital Power Supply for JESD204B PLL (1.8 V Nominal).
16	PDWN/STBY	Input	Power-Down Input/Standby (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby. This pin requires external 10 kΩ pull-down resistor.
17, 18, 35, 36	FD_A, FD_B, FD_D, FD_C	Output	Fast Detect Outputs for Channel A, Channel B, Channel C, and Channel D.
19	SYNCINB−AB	Input	Active Low JESD204B LVDS Sync Input Complement for Channel A and Channel B.
20	SYNCINB+AB	Input	Active Low JESD204B LVDS/CMOS Sync Input True for Channel A and Channel B.

Pin No.	Mnemonic	Type	Description
21, 32	DRGND	Ground	Ground Reference for DRVDD1 and DRVDD2.
22, 31	DRVDD1	Supply	Digital Power Supply for SERDOUTABx±/SERDOUTCDx± Pins (0.975 V Nominal).
23, 24	SERDOUTAB0−, SERDOUTAB0+	Output	Lane 0 Output Data Complement/True for Channel A and Channel B.
25, 26	SERDOUTAB1−, SERDOUTAB1+	Output	Lane 1 Output Data Complement/True for Channel A and Channel B.
27, 28	SERDOUTCD1+, SERDOUTCD1−	Output	Lane 1 Output Data True/Complement for Channel C and Channel D.
29, 30	SERDOUTCD0+, SERDOUTCD0−	Output	Lane 0 Output Data True/Complement for Channel C and Channel D.
33	SYNCINB+CD	Input	Active Low JESD204B LVDS/CMOS/LVPECL Sync Input True for Channel C and Channel D.
34	SYNCINB−CD	Input	Active Low JESD204B LVDS/CMOS/LVPECL Sync Input Complement for Channel C and Channel D.
37	SDIO	Input/output	SPI Serial Data Input/Output.
38	SCLK	Input	SPI Serial Clock.
39	CSB	Input	SPI Chip Select (Active Low).
40	SPIVDD	Supply	Digital Power Supply for SPI (1.8 V Nominal).
43	VCM_CD/VREF	Output/input	Common-Mode Level Bias Output for Analog Input Channel C and Channel D/0.5 V Reference Voltage Input. This pin is configurable through the SPI as an output or an input. Use this pin as the common-mode level bias output if using the internal reference. This pin requires a 0.5 V reference voltage input if using an external voltage reference source.
47, 48	VIN−D, VIN+D	Input	ADC D Analog Input Complement/True.
52, 53	VIN+C, VIN−C	Input	ADC C Analog Input True/Complement.
60, 61	CLK+, CLK−	Input	Clock Input True/Complement.
63, 67	AGND_SR	Ground	Ground Reference for SYSREF±.
64	AVDD1_SR	Supply	Analog Power Supply for SYSREF± (0.975 V Nominal).
65, 66	SYSREF+, SYSREF−	Input	Active Low JESD204B LVDS System Reference Input True/Complement. DC-coupled input only.
	EPAD		Exposed Pad. Analog ground. The exposed thermal pad on the bottom of the package provides the ground reference for AVDDX, SPIVDD, DVDD, DRVDD1, and DRVDD2. This exposed pad must be connected to ground for proper operation.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.80 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, specified maximum sampling rate, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference, A_{IN} = −1.0 dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of −40°C to +105°C. Typical specifications represent performance at T_J = 50°C (T_A = 25°C).

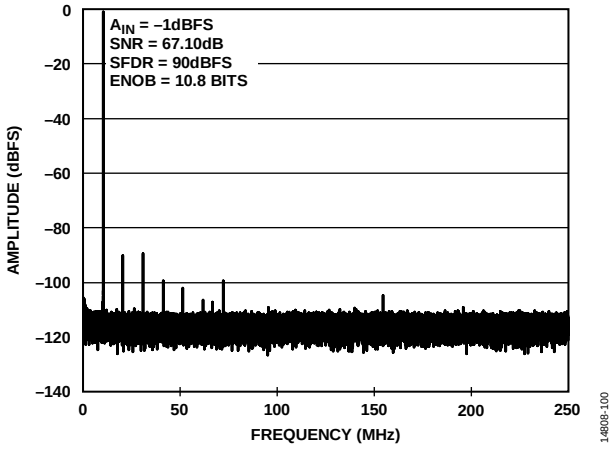

Figure 6. Single-Tone FFT with f_{IN} = 10.3 MHz

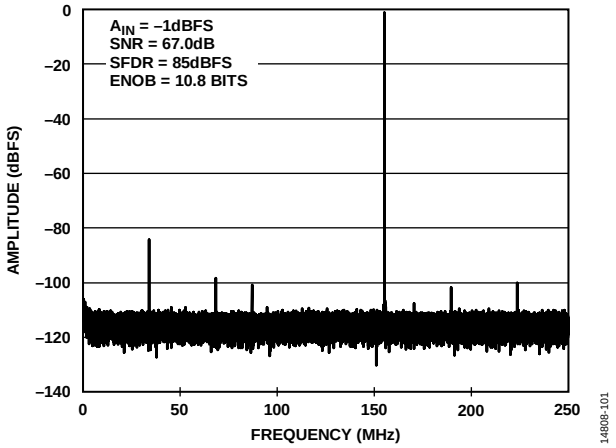

Figure 7. Single-Tone FFT with f_{IN} = 155 MHz

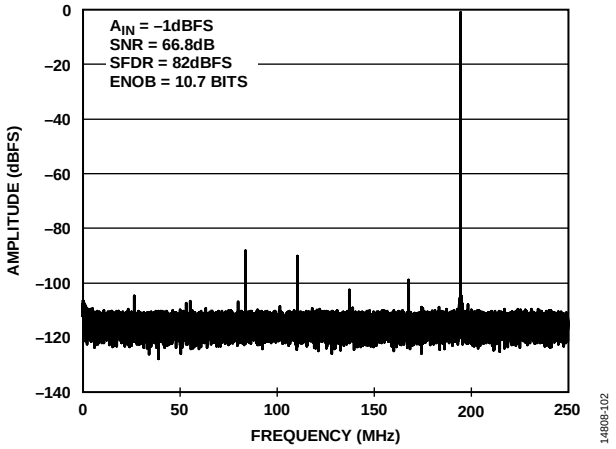

Figure 8. Single-Tone FFT with f_{IN} = 305 MHz

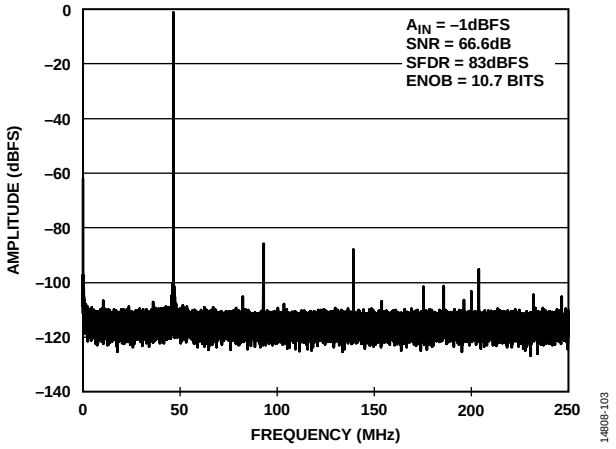

Figure 9. Single-Tone FFT with f_{IN} = 453 MHz

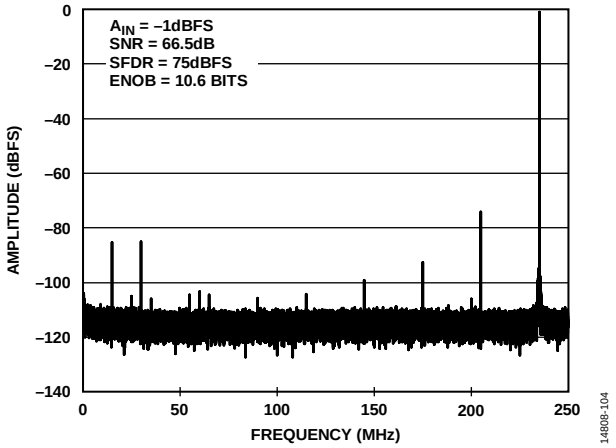

Figure 10. Single-Tone FFT with f_{IN} = 765 MHz

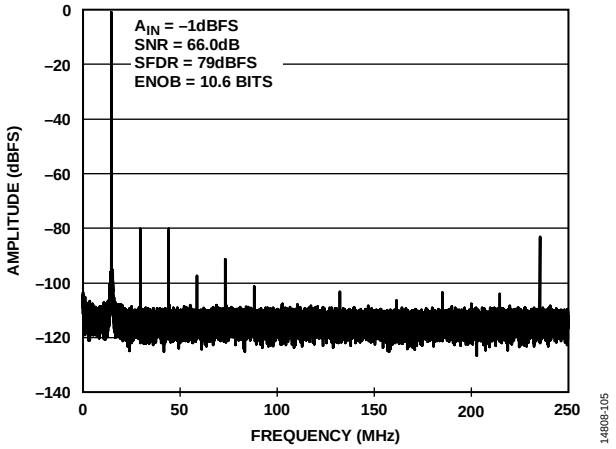

Figure 11. Single-Tone FFT with f_{IN} = 985 MHz

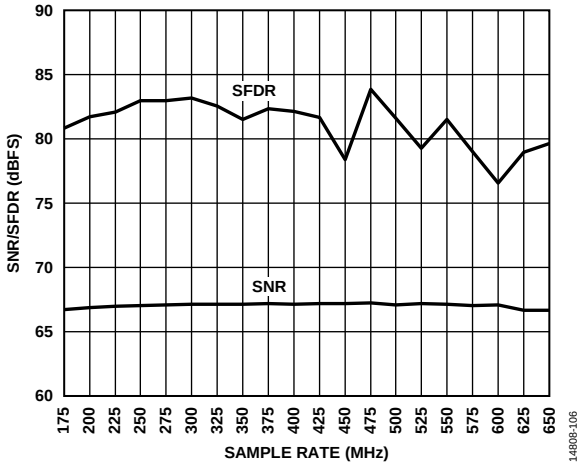

Figure 12. SNR/SFDR vs. Sample Rate (f_S), f_{IN} = 155 MHz

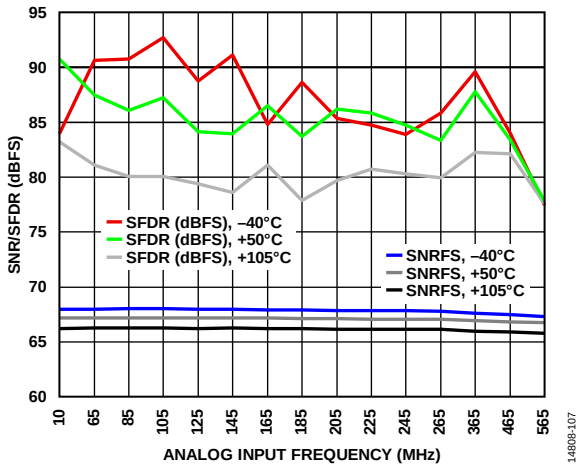

Figure 13. SNR/SFDR vs. Analog Input Frequency (f_{IN})

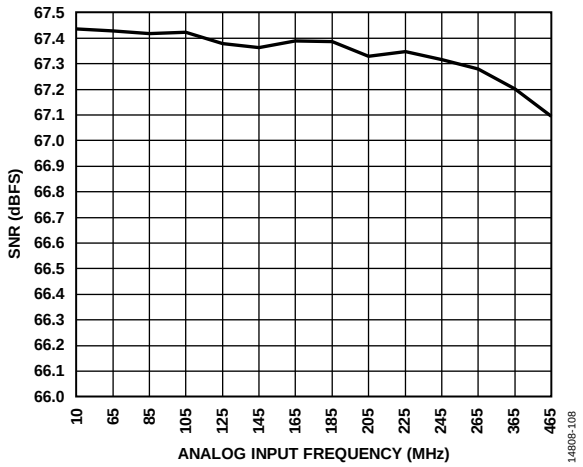

Figure 14. SNR vs. Analog Input Frequency (f_{IN}), First and Second Nyquist Zones; A_{IN} at –3 dBFS

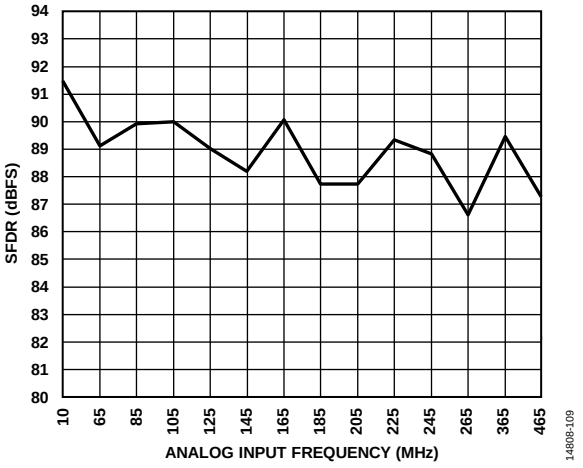

Figure 15. SFDR vs. Analog Input Frequency (f_{IN}), First and Second Nyquist Zones; A_{IN} at –3 dBFS

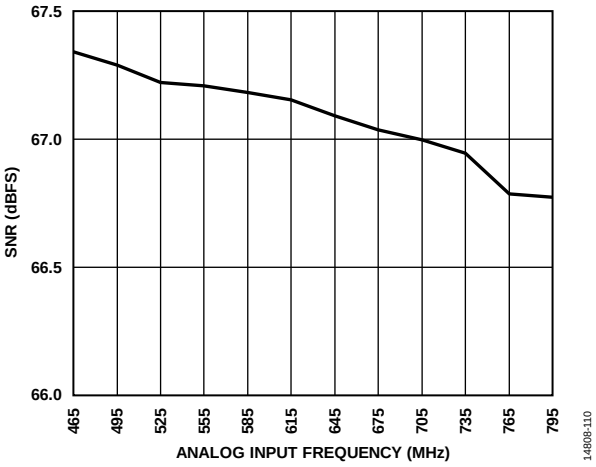

Figure 16. SNR vs. Analog Input Frequency (f_{IN}), Third Nyquist Zone A_{IN} at –3 dBFS

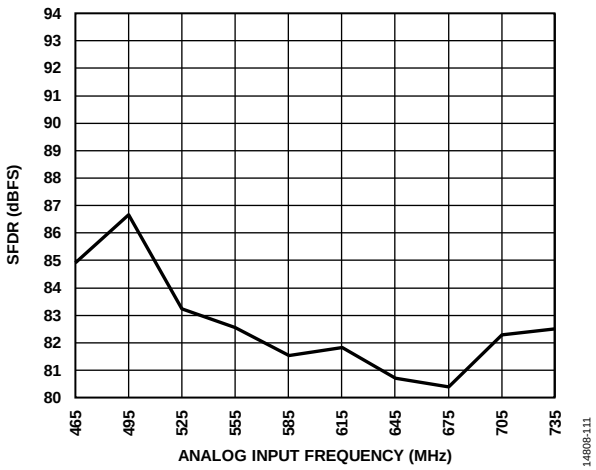

Figure 17. SFDR vs. Analog Input Frequency (f_{IN}), Third Nyquist Zone; A_{IN} at –3 dBFS

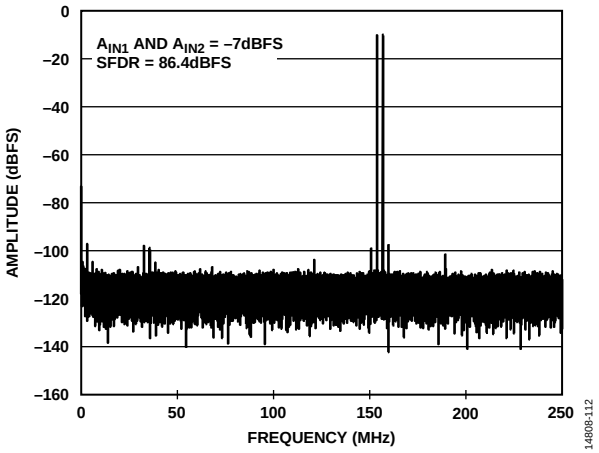

Figure 18. Two-Tone FFT; f_{IN1} = 153.5 MHz, f_{IN2} = 156.5 MHz

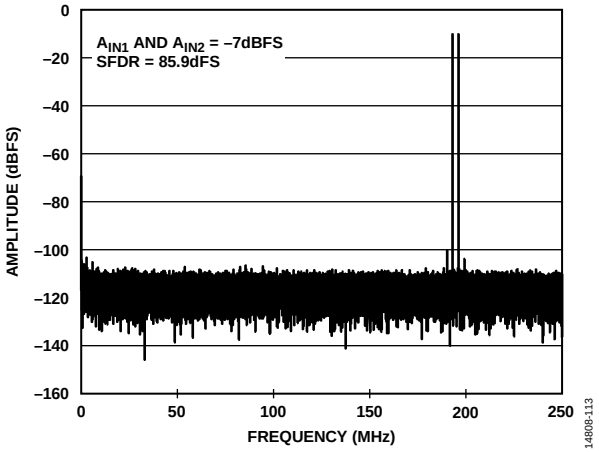

Figure 19. Two-Tone FFT; f_{IN1} = 303.5 MHz, f_{IN2} = 306.5 MHz

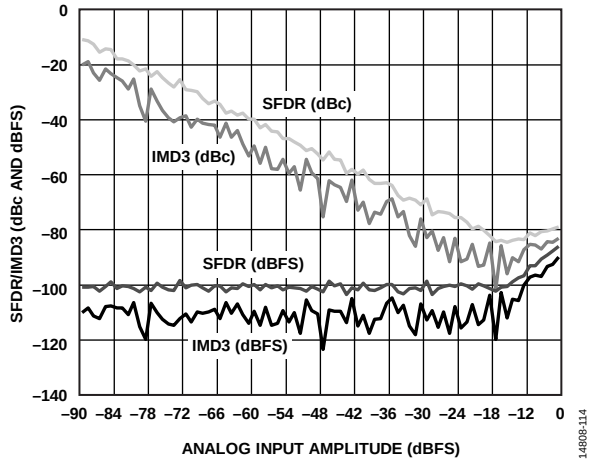

Figure 20. Two-Tone SFDR/IMD3 vs. Analog Input Amplitude (A_{IN}) with f_{IN1} = 303.5 MHz and f_{IN2} = 306.5 MHz

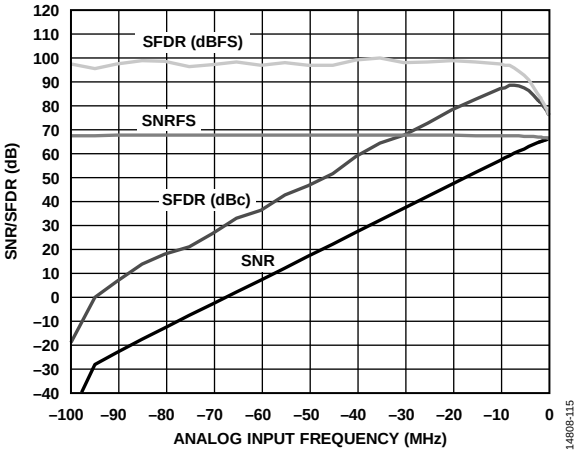

Figure 21. SNR/SFDR vs. Analog Input Frequency, f_{IN} = 155 MHz

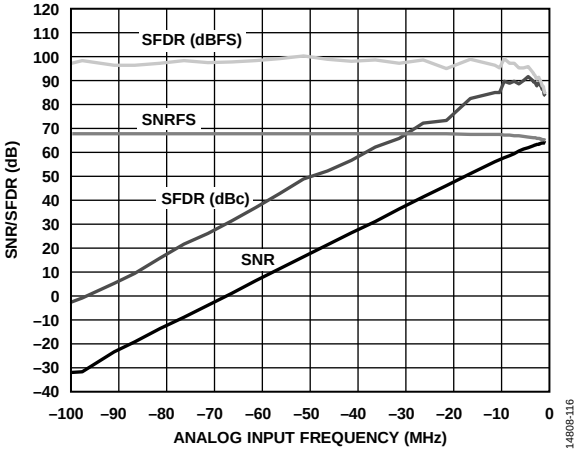

Figure 22. SNR/SFDR vs. Analog Input Frequency, f_{IN} = 305 MHz

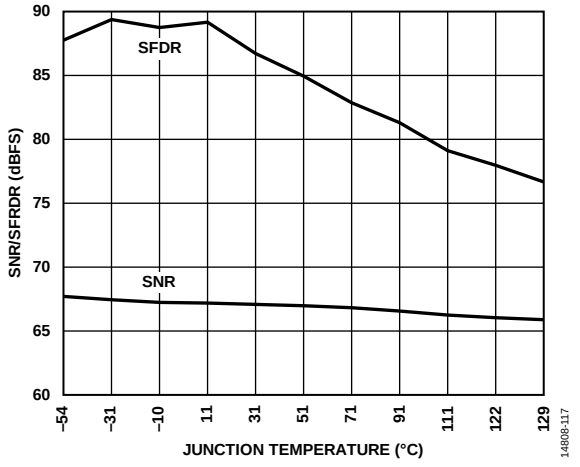

Figure 23. SNR/SFDR vs. Junction Temperature, f_{IN} = 155 MHz

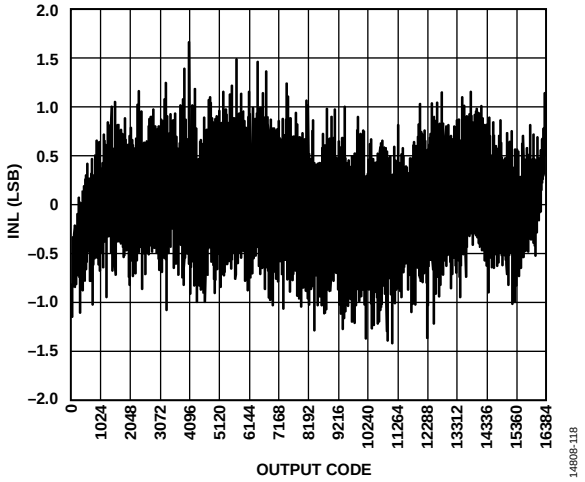

Figure 24. INL, f_{IN} = 10.3 MHz

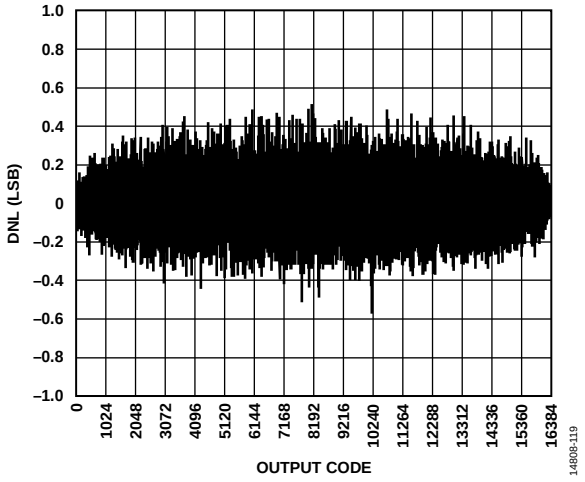

Figure 25. DNL, f_{IN} = 10.3 MHz

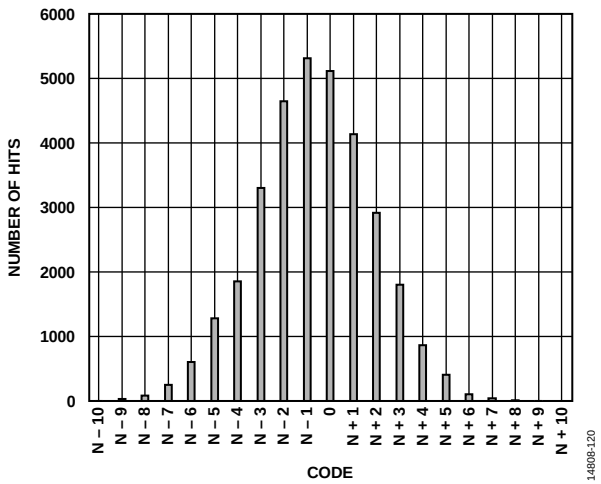

Figure 26. Input Referred Noise Histogram

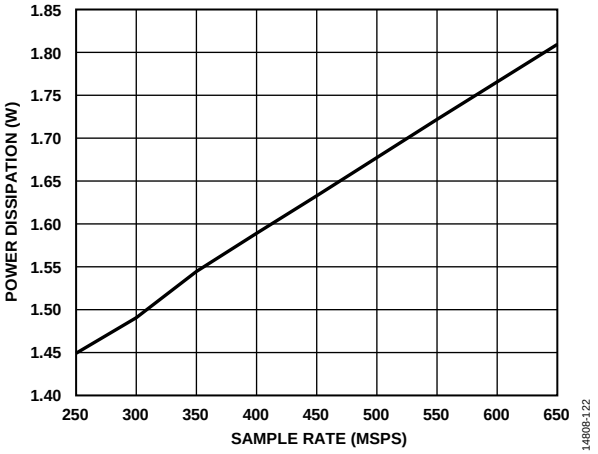

Figure 27. Power Dissipation vs. Sample Rate (f_S)

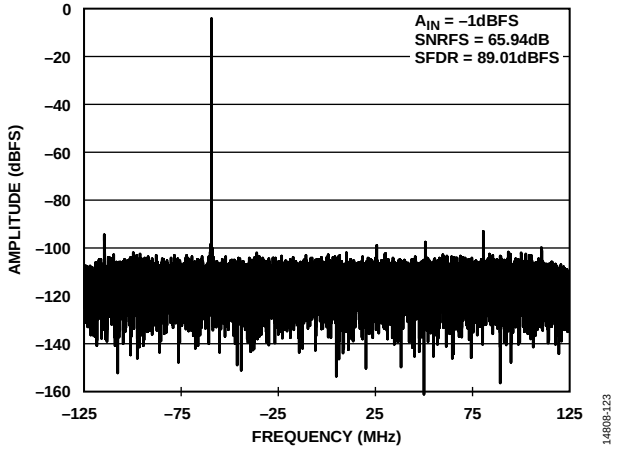

Figure 28. DDC Mode (Four DDCs; Decimate by 2; L = 2, M = 4, and F = 4) with f_{IN} = 305 MHz

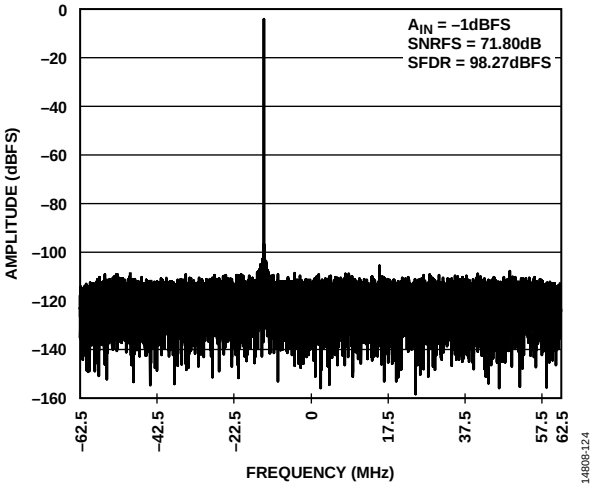

Figure 29. DDC Mode (Four DDCs; Decimate by 4; L = 1, M = 4, and F = 8) with f_{IN} = 305 MHz

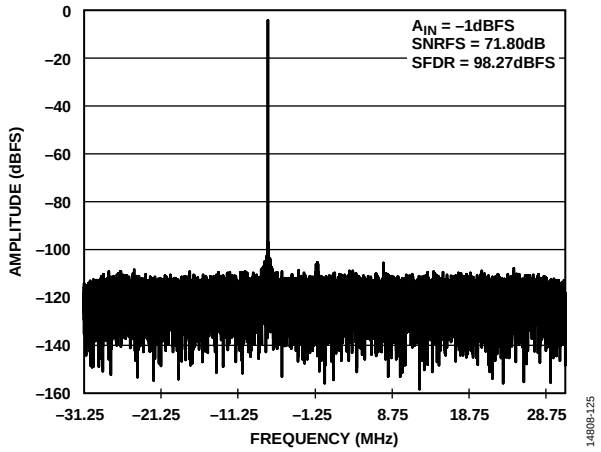

Figure 30. DDC Mode (Four DDCs; Decimate by 8; L = 1, M = 4, and F = 8) with f_{IN} = 305 MHz

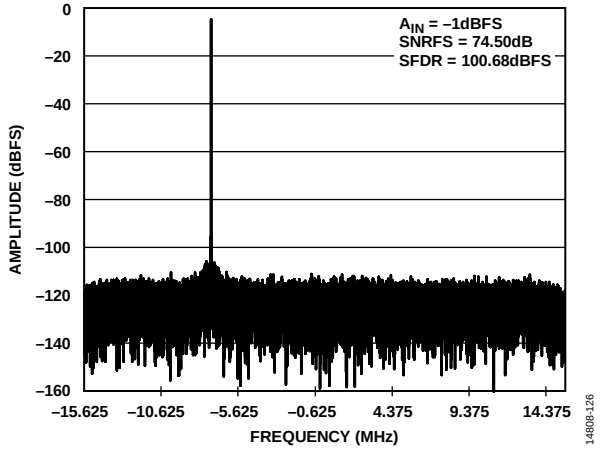

Figure 31. DDC Mode (Four DDCs, Decimate by 16, L = 1, M = 4, and F = 8) with f_{IN} = 305 MHz

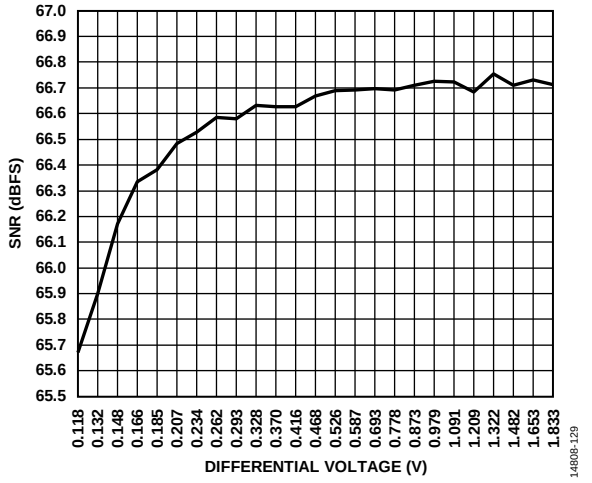

Figure 32. SNR vs. Differential Voltage (Clock Amplitude), f_{IN} = 155.3 MHz

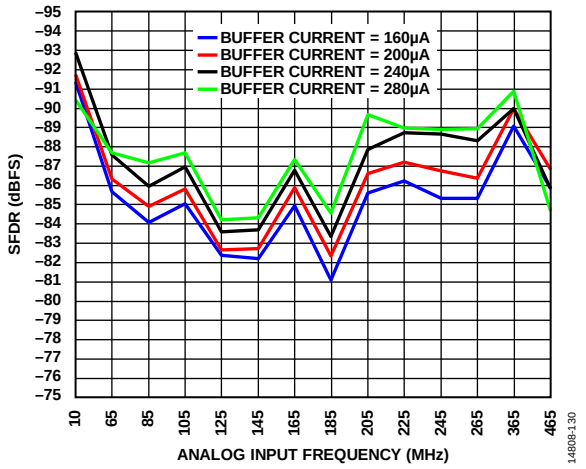

Figure 33. SFDR vs. Analog Input Frequency with Different Buffer Current Settings (First and Second Nyquist Zones)

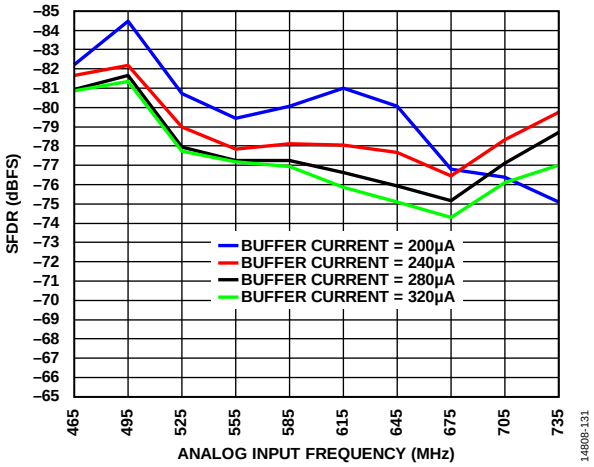

Figure 34. SFDR vs. Analog Input Frequency with Different Buffer Current Settings (Third Nyquist Zone)

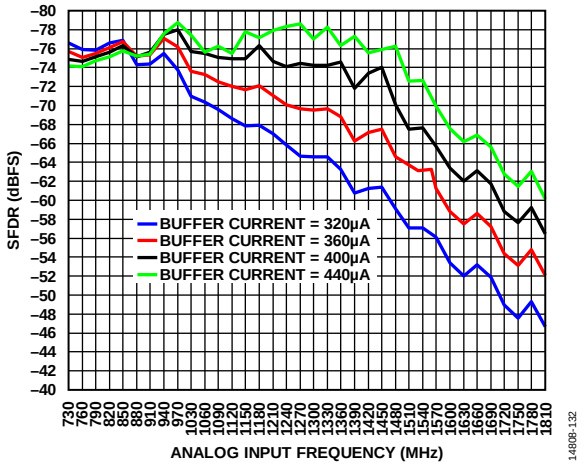

Figure 35. SFDR vs. Analog Input Frequency with Different Buffer Current Settings (Fourth Nyquist Zone)

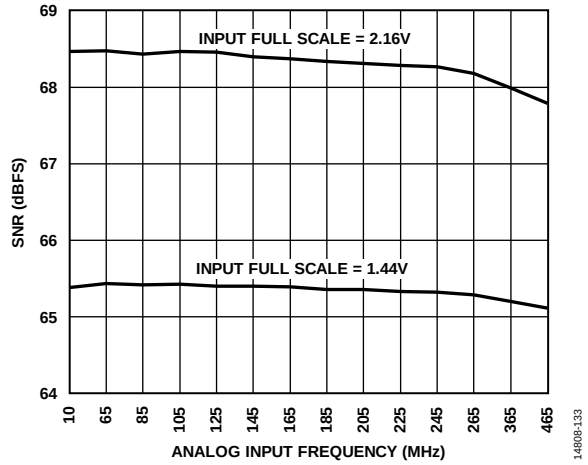

Figure 36. SNR vs. Analog Input Frequency with Different Analog Input Full Scales (First and Second Nyquist Zones)

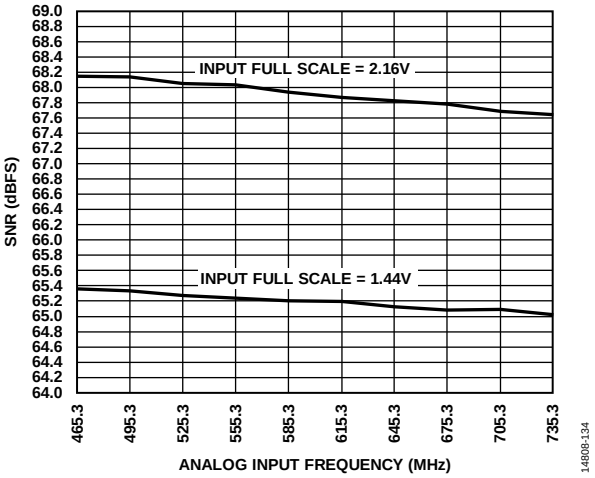

Figure 37. SNR vs. Analog Input Frequency with Different Analog Input Full Scales (Third Nyquist Zone)

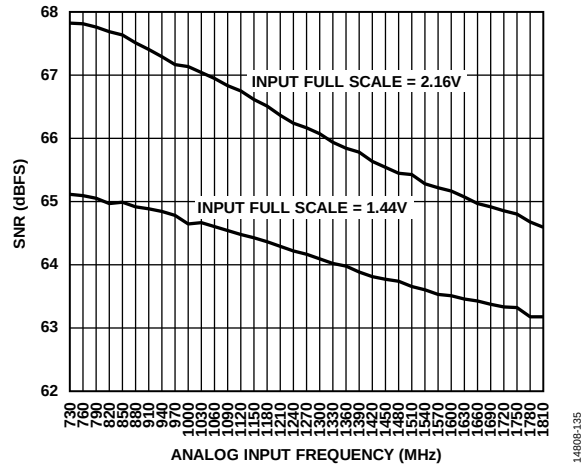

Figure 38. SNR vs. Analog Input Frequency with Different Analog Input Full Scales (Fourth Nyquist Zone)

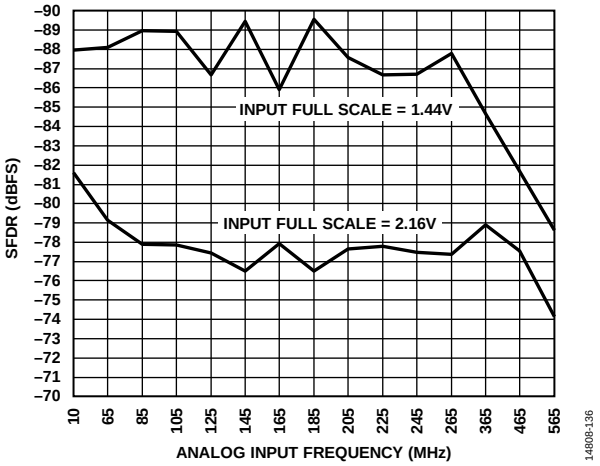

Figure 39. SFDR vs. Analog Input Frequency with Different Analog Input Full Scales (First and Second Nyquist Zones)

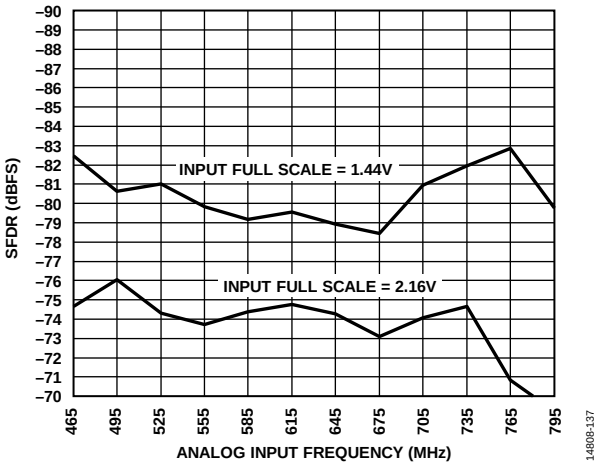

Figure 40. SFDR vs. Analog Input Frequency with Different Analog Input Full Scales (Third Nyquist Zone)

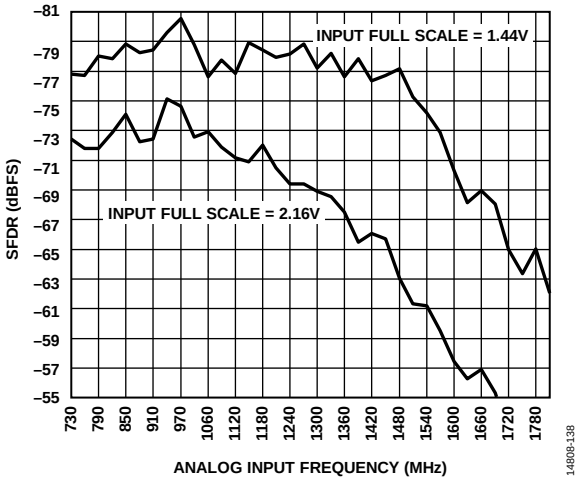

Figure 41. SFDR vs. Analog Input Frequency with Different Analog Input Full Scales (Fourth Nyquist Zone)

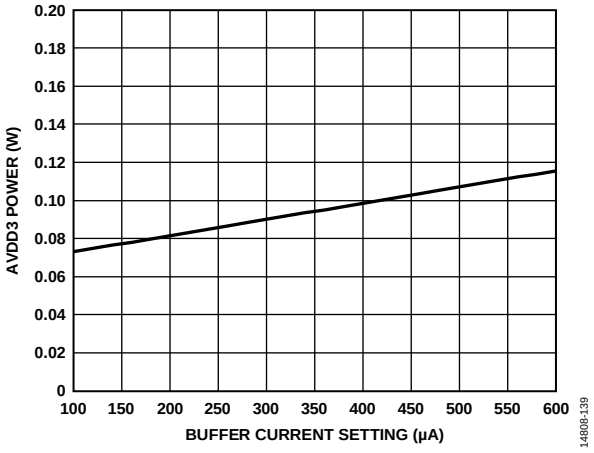

Figure 42. AVDD3 Power vs. Buffer Current Setting

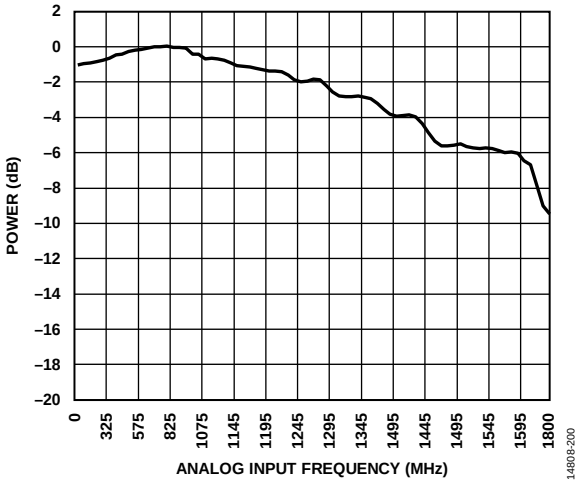

Figure 43. Full Power Bandwidth

EQUIVALENT CIRCUITS

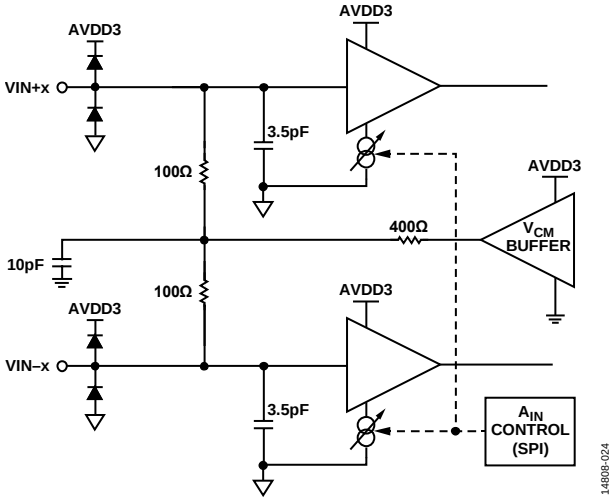

Figure 44. Analog Inputs

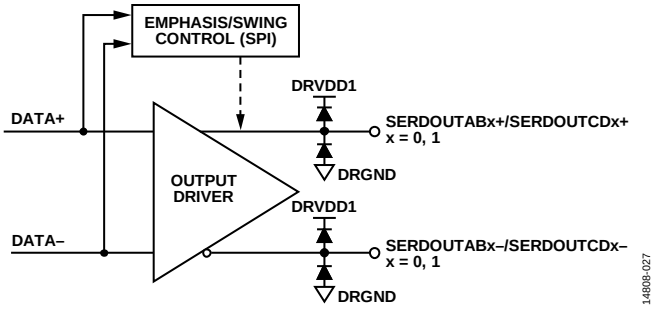

Figure 47. Digital Outputs

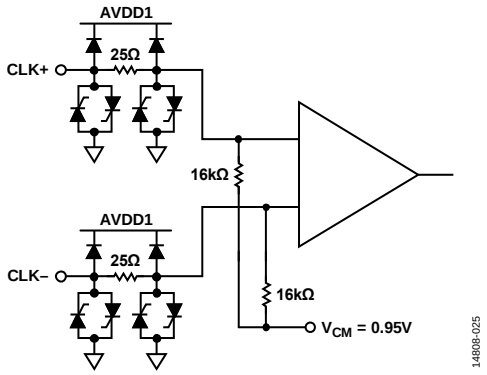

Figure 45. Clock Inputs

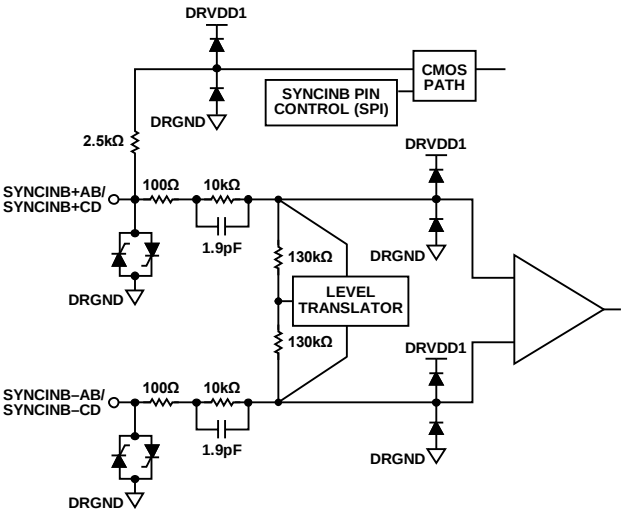

Figure 48. SYNCINB±AB, SYNCINB±CD Inputs

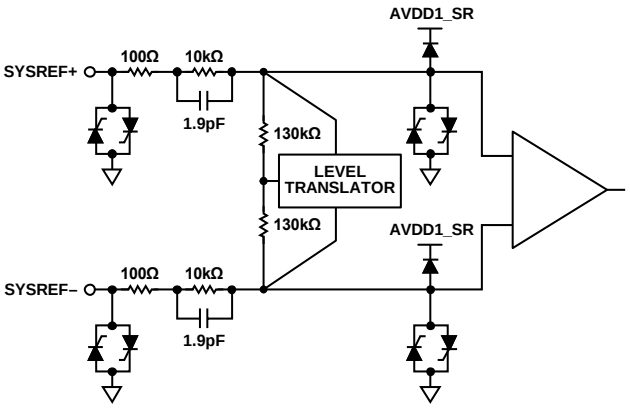

Figure 46. SYSREF± Inputs

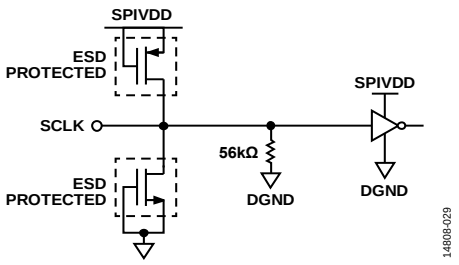

Figure 49. SCLK Input

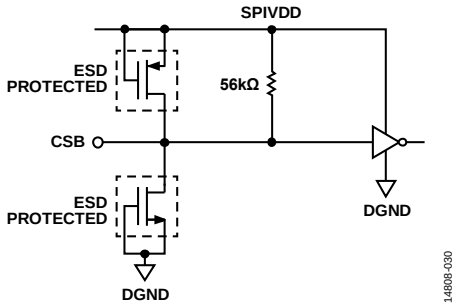

Figure 50. CSB Input

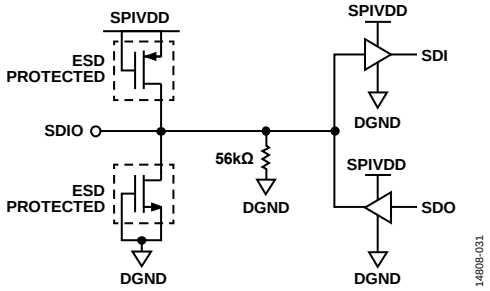

Figure 51. SDIO Input

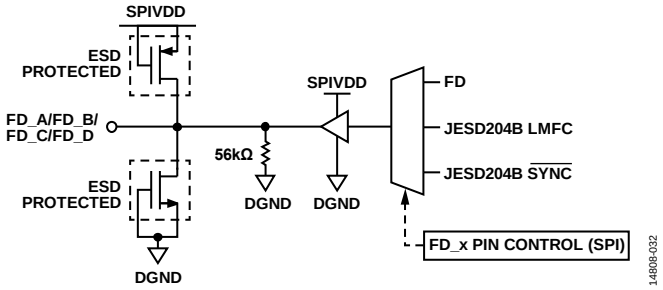

Figure 52. FD_A/FD_B/FD_C/FD_D Outputs

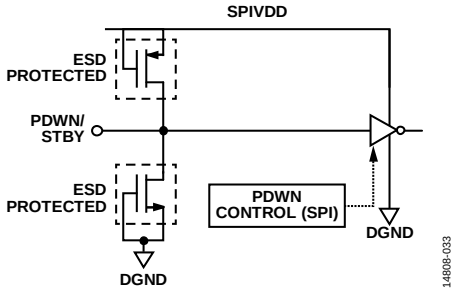

Figure 53. PDWN/STBY Input

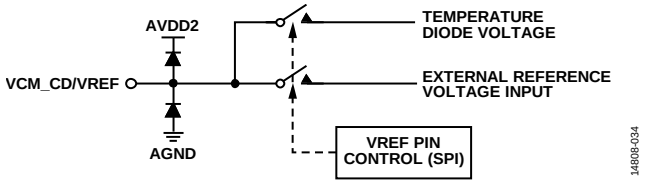

Figure 54. VCM_CD/VREF Input/Output

THEORY OF OPERATION

ADC ARCHITECTURE

The architecture of the AD9694 consists of an input buffered pipelined ADC. The input buffer is designed to provide a 200 Ω termination impedance to the analog input signal. The equivalent circuit diagram of the analog input termination is shown in Figure 44.

The input buffer provides a linear high input impedance (for ease of drive) and reduces kickback from the ADC. The buffer is optimized for high linearity, low noise, and low power. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with the preceding samples at the same time. Sampling occurs on the rising edge of the clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9694 is a differential buffer with an internal common-mode voltage of 1.34 V. The clock signal alternately switches the input circuit between sample mode and hold mode. Either a differential capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This configuration ultimately creates a low-pass filter at the input, which limits unwanted broadband noise. See Figure 55 and Figure 56 for details on input network recommendations.

For best dynamic performance, the source impedances driving VIN+x and VIN−x must be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates a differential reference that defines the span of the ADC core.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. In the case of the AD9694, the available span is programmable through the SPI port from 1.44 V p-p to 2.16 V p-p differential, with 1.80 V p-p differential being the default.

Dither

The AD9694 has internal on-chip dither circuitry that improves the ADC linearity and SFDR, particularly at smaller signal levels. A known but random amount of white noise is injected into the input of the AD9694. This dither improves the small signal linearity within the ADC transfer function and is precisely subtracted out digitally. The dither is turned on by default and does not reduce the ADC input dynamic range. The data sheet specifications and limits are obtained with the dither turned on. The dither can be disabled using SPI writes to Register 0x0922. Disabling the dither can slightly improve the SNR (by about 0.2 dB) at the expense of the small signal SFDR.

Differential Input Configurations

There are several ways to drive the AD9694, either actively or passively. However, optimum performance is achieved by driving the analog input differentially.

For applications where SNR and SFDR are key parameters, differential transformer coupling is the recommended input configuration (see Figure 55 and Figure 56) because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD9694.

For low to midrange frequencies, a double balun or double transformer network (see Figure 55) is recommended for optimum performance of the AD9694. For higher frequencies in the third or fourth Nyquist zones, remove some of the front-end passive components to ensure wideband operation (see Figure 56).

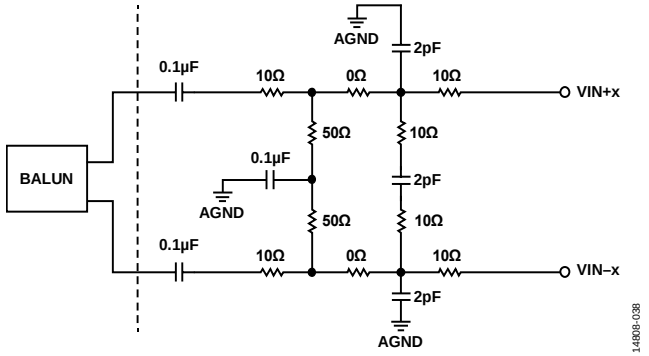

Figure 55. Differential Transformer Coupled Configuration for First and Second Nyquist Frequencies

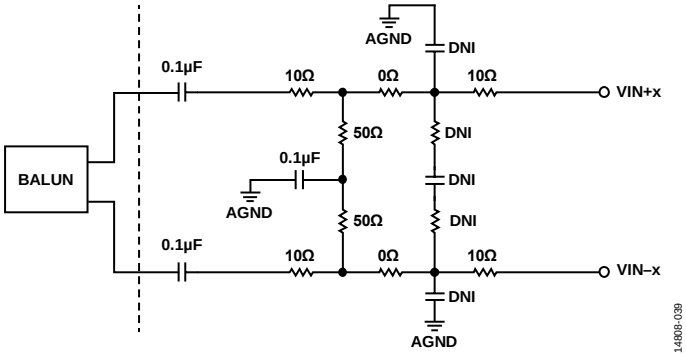

Figure 56. Differential Transformer Coupled Configuration for Third and Fourth Nyquist Zones

Input Common Mode

The analog inputs of the AD9694 are internally biased to the common mode as shown in Figure 57.

For dc-coupled applications, the recommended operation procedure is to export the common-mode voltage to the VCM_CD/VREF pin using the SPI writes listed in this section. The common-mode voltage must be set by the exported value to ensure proper ADC operation. Disconnect the internal common-mode buffer from the analog input using Register 0x1908.

When performing SPI writes for dc coupling operation, use the following register settings in order:

1. Set Register 0x1908, Bit 2 to 1 to disconnect the internal common-mode buffer from the analog input.
2. Set Register 0x18A6 to 0x00 to turn off the voltage reference.
3. Set Register 0x18E6 to 0x00 to turn off the temperature diode export.
4. Set Register 0x18E0 to 0x04.
5. Set Register 0x18E1 to 0x1C.
6. Set Register 0x18E2 to 0x14.
7. Set Register 0x18E3, Bit 6 to 0x01 to turn on the V_{CM} export.
8. Set Register 0x18E3, Bits[5:0] to the buffer current setting (copy the buffer current setting from Register 0x1A4C and Register 0x1A4D to improve the accuracy of the common-mode export).

Analog Input Controls and SFDR Optimization

The AD9694 offers flexible controls for the analog inputs, such as buffer current and input full-scale adjustment. All of the available controls are shown in Figure 57.

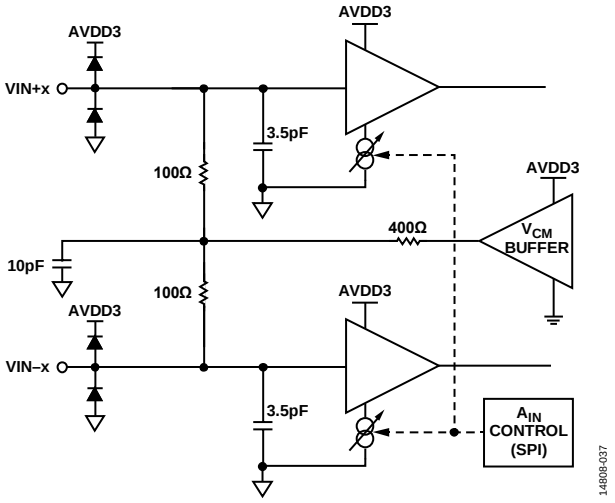

Figure 57. Analog Input Controls

Using Register 0x1A4C and Register 0x1A4D, the buffer currents on each channel can be scaled to optimize the SFDR over various input frequencies and bandwidths of interest. As the input buffer currents are set, the amount of current required by the AVDD3 supply changes. This relationship is shown in Figure 58. For a complete list of buffer current settings, see Table 39.

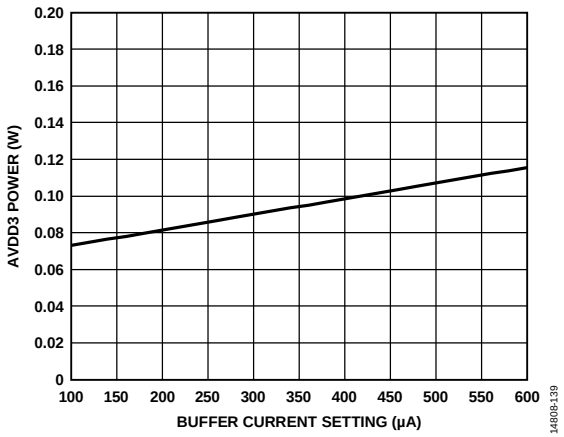

Figure 58. AVDD3 Power vs. Buffer Current Setting

In certain high frequency applications, the SFDR can be improved by reducing the full-scale setting.

Table 11 shows the recommended buffer current settings for the different analog input frequency ranges.

Table 11. SFDR Optimization for Input Frequencies

Nyquist Zone	Input Buffer Current Control Setting, Register 0x1A4C and Register 0x1A4D
First, Second, and Third Nyquist	240 µA (Register 0x1A4C, Bits[5:0] = Register 0x1A4D, Bits[5:0] = 01100)
Fourth Nyquist	400 µA (Register 0x1A4C, Bits[5:0] = Register 0x1A4D, Bits[5:0] = 10100)

Absolute Maximum Input Swing

The absolute maximum input swing allowed at the inputs of the AD9694 is 4.3 V p-p differential. Signals operating near or at this level can cause permanent damage to the ADC.

VOLTAGE REFERENCE

A stable and accurate 0.5 V voltage reference is built into the AD9694. This internal 0.5 V reference is used to set the full-scale input range of the ADC. The full-scale input range can be adjusted via Register 0x1910. For more information on adjusting the input swing, see Table 39. Figure 59 shows the block diagram of the internal 0.5 V reference controls.

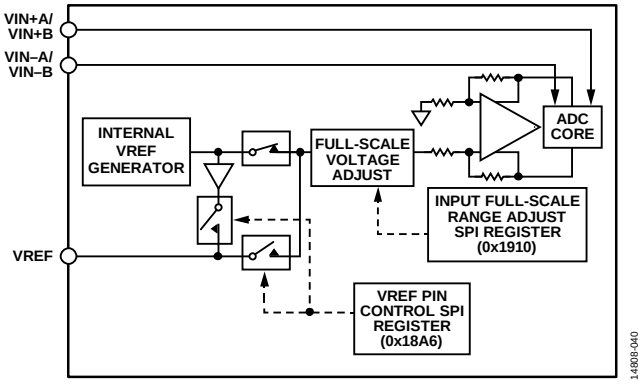

Figure 59. Internal Reference Configuration and Controls

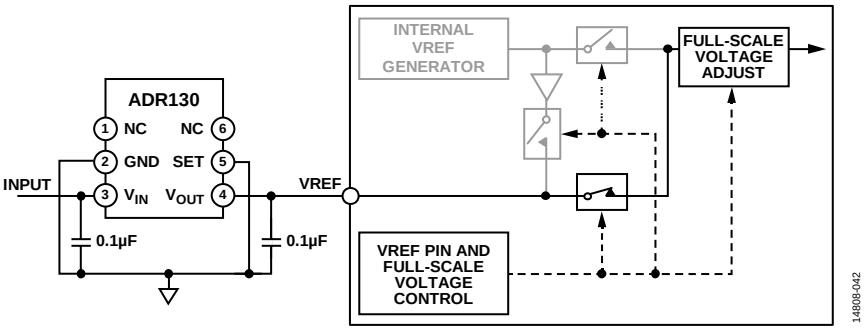

Figure 60. External Reference Using the ADR130

Register 0x18A6 enables the user to either use this internal 0.5 V reference, or to provide an external 0.5 V reference. When using an external voltage reference, provide a 0.5 V reference. The full-scale adjustment is made using the SPI, irrespective of the reference voltage. For more information on adjusting the full-scale level of the AD9694, refer to the Memory Map section.

The SPI writes required to use the external voltage reference, in order, are as follows:

1. Set Register 0x18E3 to 0x00 to turn off V_{CM} export.
2. Set Register 0x18E6 to 0x00 to turn off temperature diode export.
3. Set Register 0x18A6 to 0x01 to turn on the external voltage reference.

The use of an external reference can be necessary, in some applications, to enhance the gain accuracy of the ADC or to improve thermal drift characteristics.

The external reference must be a stable 0.5 V reference. The ADR130 is a sufficient option for providing the 0.5 V reference. Figure 60 shows how the ADR130 provides the external 0.5 V reference to the AD9694. The dashed lines show unused blocks within the AD9694 while using the ADR130 to provide the external reference.

DC OFFSET CALIBRATION

The AD9694 contains a digital filter to remove the dc offset from the output of the ADC. For ac-coupled applications, this filter can be enabled by setting Register 0x0701, Bit 7 to 1 and setting Register 0x073B, Bit 7 to 0. The filter computes the average dc signal, and it is digitally subtracted from the ADC output. As a result, the dc offset is improved to better than 70 dBFS at the output. Because the filter does not distinguish between the source of dc signals, this feature can be used when the signal content at dc is not of interest. The filter corrects dc up to ±512 codes and saturates beyond that.

CLOCK INPUT CONSIDERATIONS

For optimum performance, drive the AD9694 sample clock inputs (CLK+ and CLK−) with a differential signal. This signal is typically ac-coupled to the CLK+ and CLK− pins via a transformer or clock drivers. These pins are biased internally and require no additional biasing.

Figure 61 shows a preferred method for clocking the AD9694. The low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer.

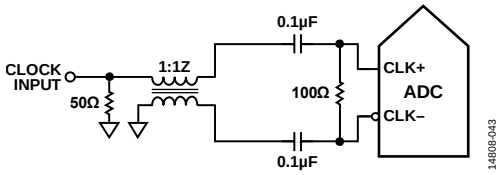

Figure 61. Transformer Coupled Differential Clock

Another option is to ac couple a differential CML or LVDS signal to the sample clock input pins, as shown in Figure 62 and Figure 63.

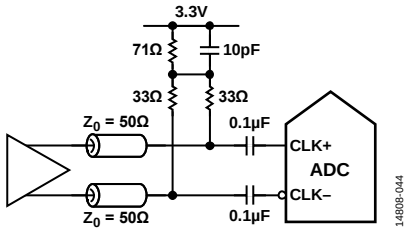

Figure 62. Differential CML Sample Clock

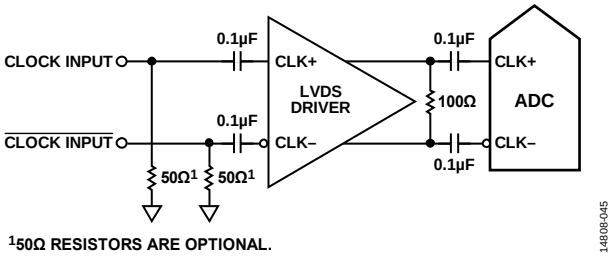

Figure 63. Differential LVDS Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. The AD9694 contains an internal clock divider and a duty cycle stabilizer (DCS). In applications where the clock duty cycle cannot be guaranteed to be 50%, a higher multiple frequency clock along with the usage of the clock divider is recommended. When it is not possible to provide a higher frequency clock, it is recommended to turn on the DCS. The output of the divider offers a 50% duty cycle, high slew rate (fast edge) clock signal to the internal ADC. The following SPI writes are required to turn on DCS (see the Memory Map section for more details on using this feature):

1. Write 0x81 to 0x011F.
2. Write 0x09 to 0x011C.
3. Write 0x09 to 0x011E.
4. Write 0x0B to 0x011C.
5. Write 0x0B to 0x011E.

Input Clock Divider

The AD9694 contains an input clock divider with the ability to divide the input clock by 1, 2, 4, or 8. The divider ratios can be selected using Register 0x0108 (see Figure 64).

In applications where the clock input is a multiple of the sample clock, care must be taken to program the appropriate divider ratio into the clock divider before applying the clock signal, which ensures that the current transients during device startup are controlled.

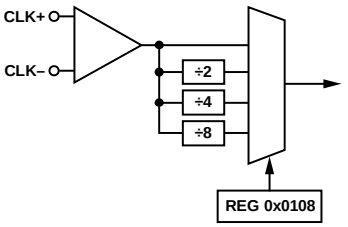

Figure 64. Clock Divider Circuit

The AD9694 clock divider can be synchronized using the external SYSREF± input. A valid SYSREF± causes the clock divider to reset to a programmable state. This synchronization feature allows multiple devices to have their clock dividers aligned to guarantee simultaneous input sampling.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR = -20 \times \log(2 \times \pi \times f_A \times t_J)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 65).

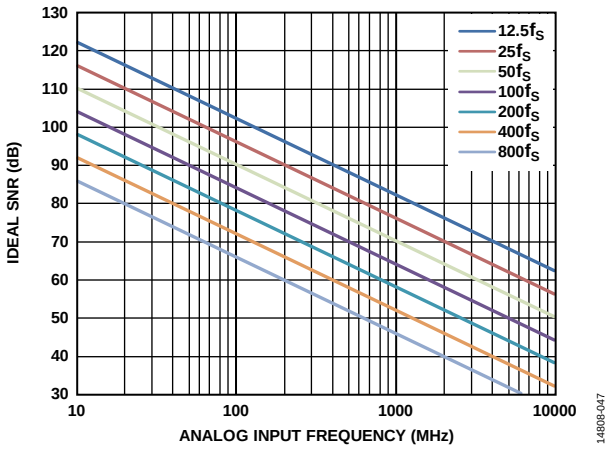

Figure 65. Ideal SNR vs. Analog Input Frequency over Jitter

Treat the clock input as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9694. Separate the power supplies for clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. If the clock is generated from another type of source (by gating, dividing, or other methods), retime the clock by the original clock at the last step. Refer to the AN-501 Application Note and the AN-756 Application Note for more in depth information about jitter performance as it relates to ADCs.

Figure 65 shows the estimated SNR of the AD9694 across input frequency for different clock induced jitter values. The SNR can be estimated by using the following equation:

$$SNR(\text{dBFS}) = -10\log\left(10^{\left(\frac{-SNR_{ADC}}{10}\right)} + 10^{\left(\frac{-SNR_{JITTER}}{10}\right)}\right)$$

Input Clock Detect

The AD9694 contains input clock detection circuitry to detect the signal on the input clock pins. If the clock amplitude or the sample rate is lower than the specified minimum value, the AD9694 enters power-down mode. When the input clock detect bit in Register 0x011B is set to 0, the input clock is not detected. See Register 0x011A and Register 0x011B for more details on the input clock detect feature.

Power-Down/Standby Mode

The AD9694 has a PDWN/STBY pin that configures the device in power-down or standby mode. The default operation is power-down. The PDWN/STBY pin is a logic high pin. When in power-down mode, the JESD204B link is disrupted. The power-down option can also be set via Register 0x003F and Register 0x0040.

In standby mode, the JESD204B link is not disrupted and transmits zeros for all converter samples. This state can be changed using Register 0x0571, Bit 7 to select /K/ characters.

Temperature Diode

The AD9694 contains a diode-based temperature sensor for measuring the temperature of the die. This diode can output a voltage and serve as a coarse temperature sensor to monitor the internal die temperature.

The temperature diode voltage can be output to the VCM_CD/VREF pin using the SPI. Use Register 0x18E6 to enable or disable the diode. Register 0x18E6 is a local register. Both cores must be selected in the pair index register (Register 0x0009 = 0x03) to enable the temperature diode readout. It is important to note that other voltages may be exported to the same pin at the same time, which can result in undefined behavior. Thus, to ensure a proper readout, switch off all other voltage exporting circuits as detailed as follows.

The SPI writes required to export the temperature diode are as follows (see Table 39 for more information):

1. Set Register 0x0009 to 0x03 to select both cores.
2. Set Register 0x18E3 to 0x00 to turn off V_{CM} export.
3. Set Register 0x18A6 to 0x00 to turn off voltage reference export.
4. Set Register 0x18E6 to 0x01 to turn on voltage export of the central 1× temperature diode. The typical voltage response of the temperature diode is shown in Figure 66. Although this voltage represents the die temperature, it is recommended to take measurements from a pair of diodes for improved accuracy. The next step explains how to enable the 20× diode.
5. Set Register 0x18E6 to 0x02 to turn on the second central temperature diode of the pair, which is 20× the size of the first. For the method using two diodes simultaneously to achieve a more accurate result, see the AN-1432 Application Note, *Practical Thermal Modeling and Measurements in High Power ICs*.

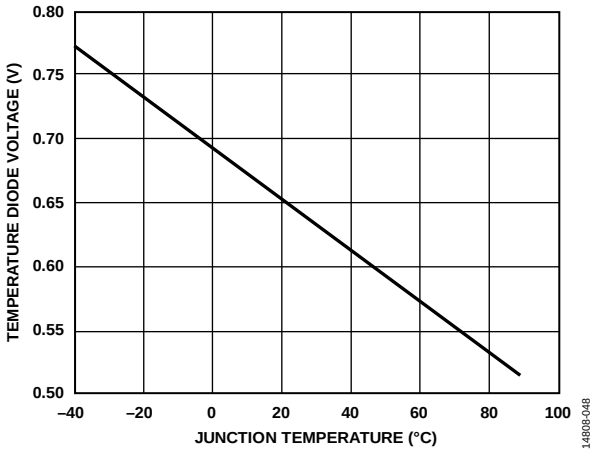

Figure 66. Temperature Diode Voltage vs. Junction Temperature

ADC OVERRANGE AND FAST DETECT

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overrange bit in the JESD204B outputs provides information on the state of the analog input that is of limited usefulness. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip actually occurs. In addition, because input signals can have significant slew rates, the latency of this function is of major concern. Highly pipelined converters can have significant latency. The AD9694 contains fast detect circuitry for individual channels to monitor the threshold and to assert the FD_A, FD_B, FD_C, and FD_D pins.

ADC OVERRANGE

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange indicator can be embedded within the JESD204B link as a control bit (when CSB > 0). The latency of this overrange indicator matches the sample latency.

FAST THRESHOLD DETECTION (FD_A, FD_B, FD_C, AND FD_D)

The fast detect (FD) bits in Register 0x0040 are immediately set whenever the absolute value of the input signal exceeds the programmable upper threshold level. The FD bits are cleared only when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time. This feature provides hysteresis and prevents the FD bits from excessively toggling.

The operation of the upper threshold and lower threshold registers, along with the dwell time registers, is shown in Figure 67.

The FD indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold registers, located at Register 0x0247 and Register 0x0248. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of 30 clock cycles (maximum). The approximate upper threshold magnitude is defined by

$$\textit{Upper Threshold Magnitude}\ (\text{dBFS}) = 20\log\left(\textit{Threshold Magnitude}/2^{13}\right)$$

The FD indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers, located at Register 0x0249 and Register 0x024A. The fast detect lower threshold register is a 13-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency, but is accurate in terms of converter resolution. The lower threshold magnitude is defined by

$$\textit{Lower Threshold Magnitude}\ (\text{dBFS}) = 20\log\left(\textit{Threshold Magnitude}/2^{13}\right)$$

For example, to set an upper threshold of −6 dBFS, write 0xFFF to Register 0x0247 and Register 0x0248. To set a lower threshold of −10 dBFS, write 0xA1D to Register 0x0249 and Register 0x024A.

The dwell time can be programmed from 1 to 65,535 sample clock cycles by placing the desired value in the fast detect dwell time registers, located at Register 0x024B and Register 0x024C. See the Memory Map section (Register 0x0040, and Register 0x0245 to Register 0x024C in Table 39) for more details.

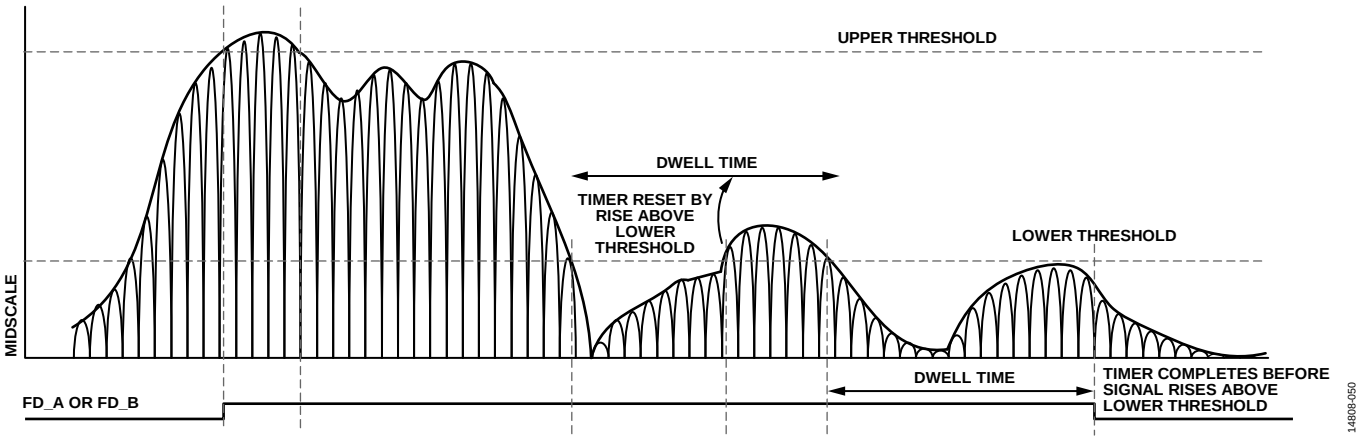

Figure 67. Threshold Settings for the FD_A and FD_B Signals

SIGNAL MONITOR

The signal monitor block provides additional information about the signal being digitized by the ADC. The signal monitor computes the peak magnitude of the digitized signal. This information can be used to drive an AGC loop to optimize the range of the ADC in the presence of real-world signals.

The results of the signal monitor block can be obtained either by reading back the internal values from the SPI port or by embedding the signal monitoring information into the JESD204B interface as special control bits. A global, 24-bit programmable period controls the duration of the measurement. Figure 68 shows the simplified block diagram of the signal monitor block.

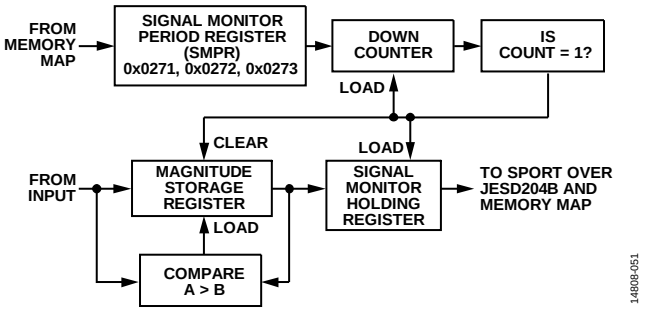

Figure 68. Signal Monitor Block

The peak detector captures the largest signal within the observation period. The detector only observes the magnitude of the signal. The resolution of the peak detector is a 13-bit value, and the observation period is 24 bits and represents converter output samples. The peak magnitude can be derived by using the following equation:

$$Peak\ Magnitude\ (\text{dBFS}) = 20\log(Peak\ Detector\ Value/2^{13})$$

The magnitude of the input port signal is monitored over a programmable time period, which is determined by the signal monitor period register (SMPR). The peak detector function is enabled by setting Bit 1 of Register 0x0270 in the signal monitor control register. The 24-bit SMPR must be programmed before activating this mode.

After enabling peak detection mode, the value in the SMPR is loaded into a monitor period timer, which decrements at the decimated clock rate. The magnitude of the input signal is compared with the value in the internal magnitude storage register (not accessible to the user), and the greater of the two is updated as the current peak level. The initial value of the magnitude storage register is set to the current ADC input signal magnitude. This comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the 13-bit peak level value is transferred to the signal monitor holding register, which can be read through the memory map or output through the SPORT over the JESD204B interface. The monitor period timer is reloaded with the value in the SMPR, and the countdown restarts. In addition, the magnitude of the first input sample is updated in the magnitude storage register, and the comparison and update procedure, as explained in the Fast Threshold Detection (FD_A, FD_B, FD_C, and FD_D) section, continues.

SPORT OVER JESD204B

The signal monitor data can also be serialized and sent over the JESD204B interface as control bits. These control bits must be deserialized from the samples to reconstruct the statistical data. The signal control monitor function is enabled by setting Bit 0 of Register 0x0279 and Bit 1 of Register 0x027A. Figure 69 shows two different example configurations for the signal monitor control bit locations inside the JESD204B samples. A maximum of three control bits can be inserted into the JESD204B samples; however, only one control bit is required for the signal monitor. Control bits are inserted from MSB to LSB. If only one control bit is to be inserted (CS = 1), only the most significant control bit is used (see thed Example Configuration 1 and the Example Configuration 2 in Figure 69). To select the SPORT over JESD204B (signal monitor) option, program Register 0x0559, Register 0x055A, and Register 0x058F. See Table 39 for more information on setting these bits.

Figure 70 shows the 25-bit frame data that encapsulates the peak detector value. The frame data is transmitted MSB first with five 5-bit subframes. Each subframe contains a start bit that can be used by a receiver to validate the deserialized data. Figure 71 shows the SPORT over JESD204B signal monitor data with a monitor period timer set to 80 samples.

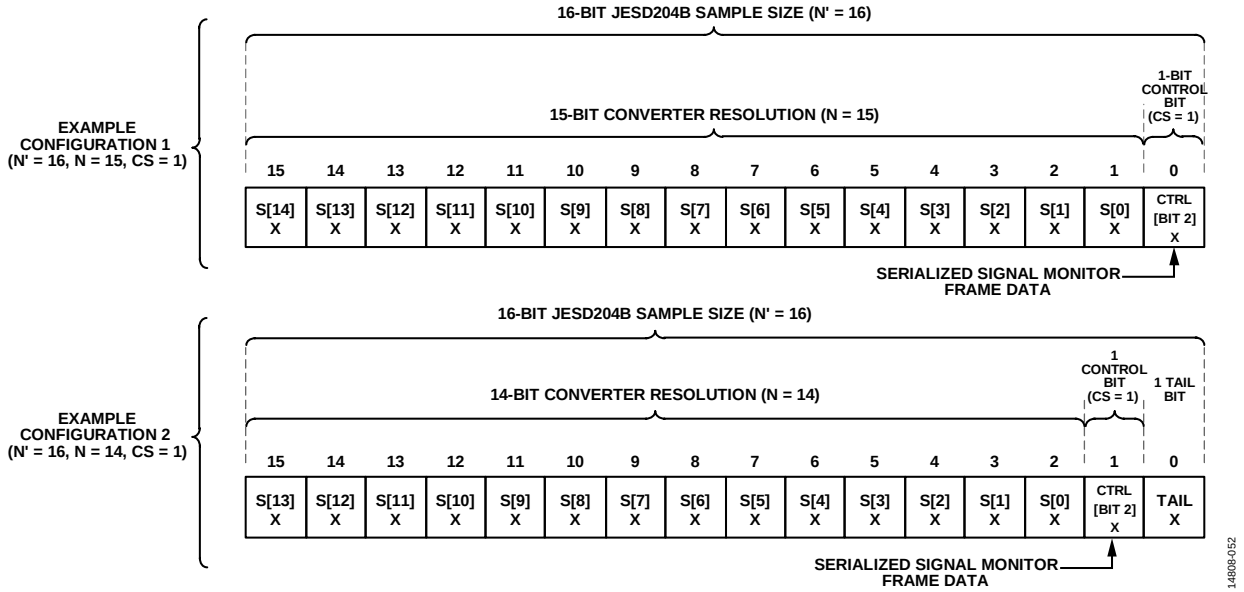

Figure 69. Signal Monitor Control Bit Locations

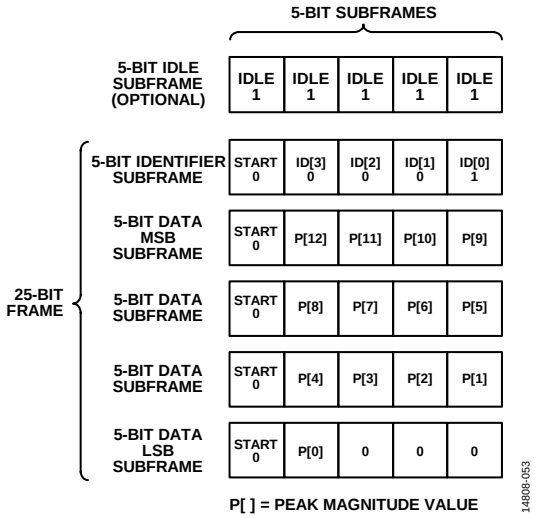

Figure 70. SPORT over JESD204B Signal Monitor Frame Data

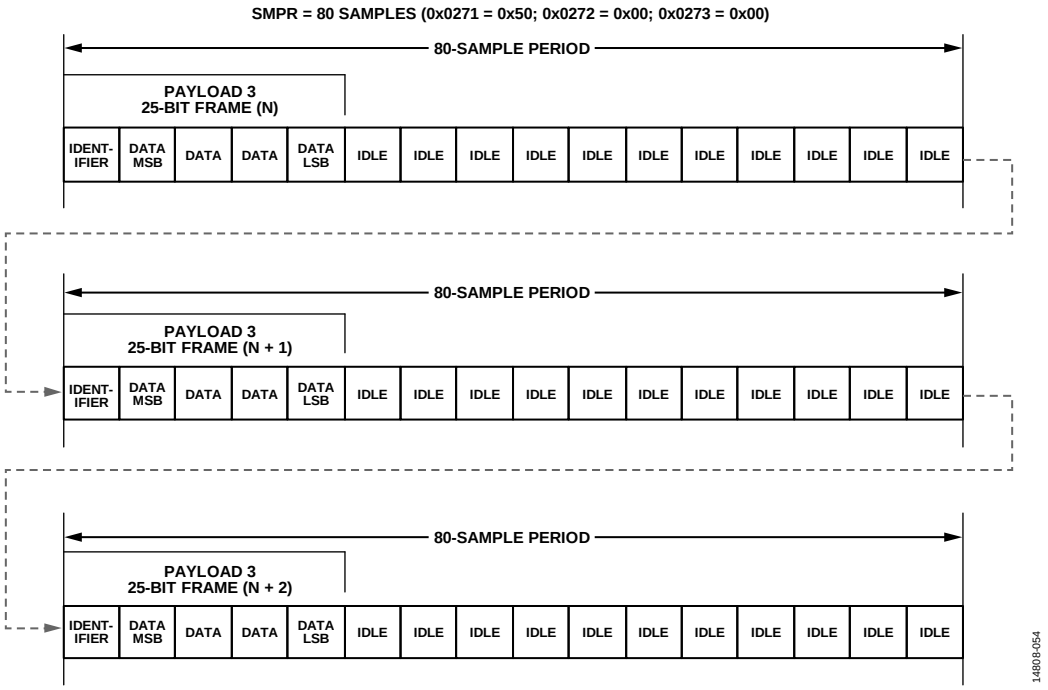

Figure 71. SPORT over JESD204B Signal Monitor Example with Period = 80 Samples

DIGITAL DOWNCONVERTER (DDC)

The AD9694 includes four digital downconverters (DDCs) that provide filtering and reduce the output data rate. This digital processing section includes an NCO, a half-band decimating filter, a finite impulse response (FIR filter, a gain stage, and a complex to real conversion stage. Each of these processing blocks has control lines that allow it to be independently enabled and disabled to provide the desired processing function. Each pair of ADC channels has two DDCs (DDC0 and DDC1) for a total of four DDCs. The digital downconverter can be configured to output either real data or complex output data.

The DDCs output a 16-bit stream. To enable this operation, the converter number of bits, N, is set to a default value of 16, even though the analog core only outputs 14 bits. In full bandwidth operation, the ADC outputs are the 14-bit word followed by two zeros, unless the tail bits are enabled.

DDC I/Q INPUT SELECTION

The AD9694 has four ADC channels and four DDC channels. Each DDC channel has two input ports that can be paired to support both real and complex inputs through the I/Q crossbar mux. For real signals, both DDC input ports must select the same ADC channel (that is, DDC Input Port I = ADC Channel A and DDC Input Port Q = ADC Channel A). For complex signals, each DDC input port must select different ADC channels (that is, DDC Input Port I = ADC Channel A and DDC Input Port Q = ADC Channel B or DDC Input Port I = ADC Channel C and DDC Input Port Q = ADC Channel D).

The inputs to each DDC are controlled by the DDC input selection registers (Register 0x0311 and Register 0x0331) in conjunction with the pair index register (Register 0x0009). See Table 39 for information on how to configure the DDCs.

DDC I/Q OUTPUT SELECTION

Each DDC channel has two output ports that can be paired to support both real and complex outputs. For real output signals, only the DDC Output Port I is used (the DDC Output Port Q is invalid). For complex I/Q output signals, both DDC Output Port I and DDC Output Port Q are used.

The I/Q outputs to each DDC channel are controlled by the DDC x complex to real enable bit, Bit 3, in the DDC control registers (Register 0x0310 and Register 0x0330) in conjunction with the pair index register (Register 0x0009).

The Chip Q ignore bit in the chip mode register (Register 0x0200, Bit 5) controls the chip output muxing of all the DDC channels. When all DDC channels use real outputs, set this bit high to ignore all DDC Q output ports. When any of the DDC channels are set to use complex I/Q outputs, the user must clear this bit to use both DDC Output Port I and DDC Output Port Q. For more information, see Figure 80.

DDC GENERAL DESCRIPTION

The four DDC blocks are used to extract a portion of the full digital spectrum captured by the ADC(s). The DDC blocks are intended for IF sampling or oversampled baseband radios requiring wide bandwidth input signals.

Each DDC block contains the following signal processing stages:

- Frequency translation stage (optional)
- Filtering stage
- Gain stage (optional)
- Complex to real conversion stage (optional)

Frequency Translation Stage (Optional)

This stage consists of a 48-bit complex NCO and quadrature mixers that can be used for frequency translation of both real and complex input signals. This stage shifts a portion of the available digital spectrum down to baseband.

Filtering Stage

After shifting down to baseband, this stage decimates the frequency spectrum using a chain of up to four half-band low-pass filters for rate conversion. The decimation process lowers the output data rate, which in turn reduces the output interface rate.

Gain Stage (Optional)

To compensate for losses associated with mixing a real input signal down to baseband, this stage adds an additional 0 dB or 6 dB of gain.

Complex to Real Conversion Stage (Optional)

When real outputs are necessary, this stage converts the complex outputs back to real by performing an $f_S/4$ mixing operation plus a filter to remove the complex component of the signal.

Figure 72 shows the detailed block diagram of the DDCs implemented in the AD9694.

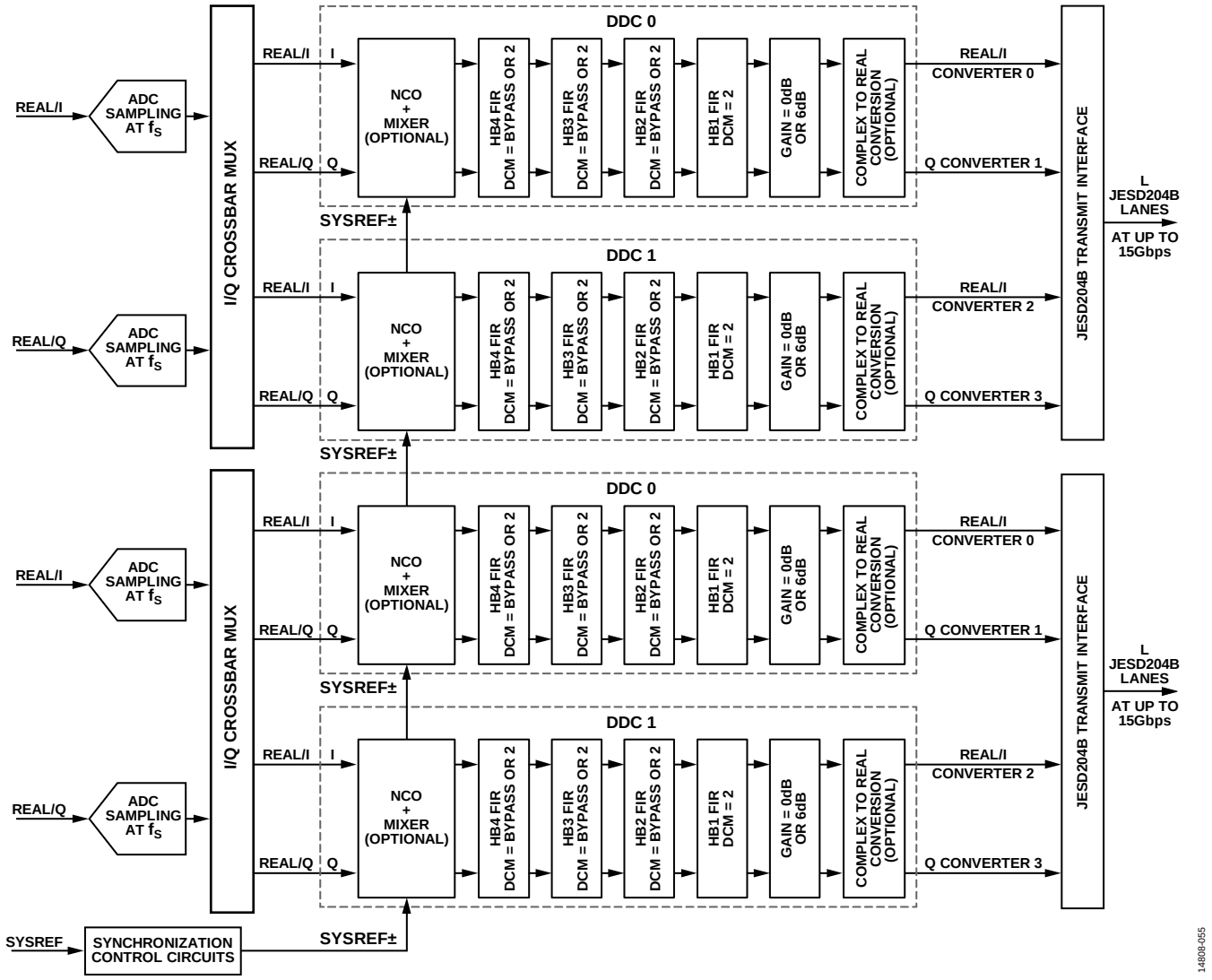

Figure 72. DDC Detailed Block Diagram

Figure 73 shows an example usage of one of the four DDC blocks with a real input signal and four half-band filters (HB4 + HB3 + HB2 + HB1). It shows both complex (decimate by 16) and real (decimate by 8) output options.

When DDCs have different decimation ratios, the chip decimation ratio register (Register 0x0201) must be set to the lowest decimation ratio of all the DDC blocks on a per pair basis in conjunction with the pair index register (Register 0x0009). In this scenario, samples of higher decimation ratio DDCs are repeated to match the chip decimation ratio sample rate. Whenever the NCO frequency is set or changed, the DDC soft reset must be issued. If the DDC soft reset is not issued, the output may potentially show amplitude variations.

Table 12 through Table 16 show the DDC samples when the chip decimation ratio is set to 1, 2, 4, 8, or 16, respectively. When DDCs have different decimation ratios, the chip decimation ratio must be set to the lowest decimation ratio of all the DDC channels. In this scenario, samples of higher decimation ratio DDCs are repeated to match the chip decimation ratio sample rate.

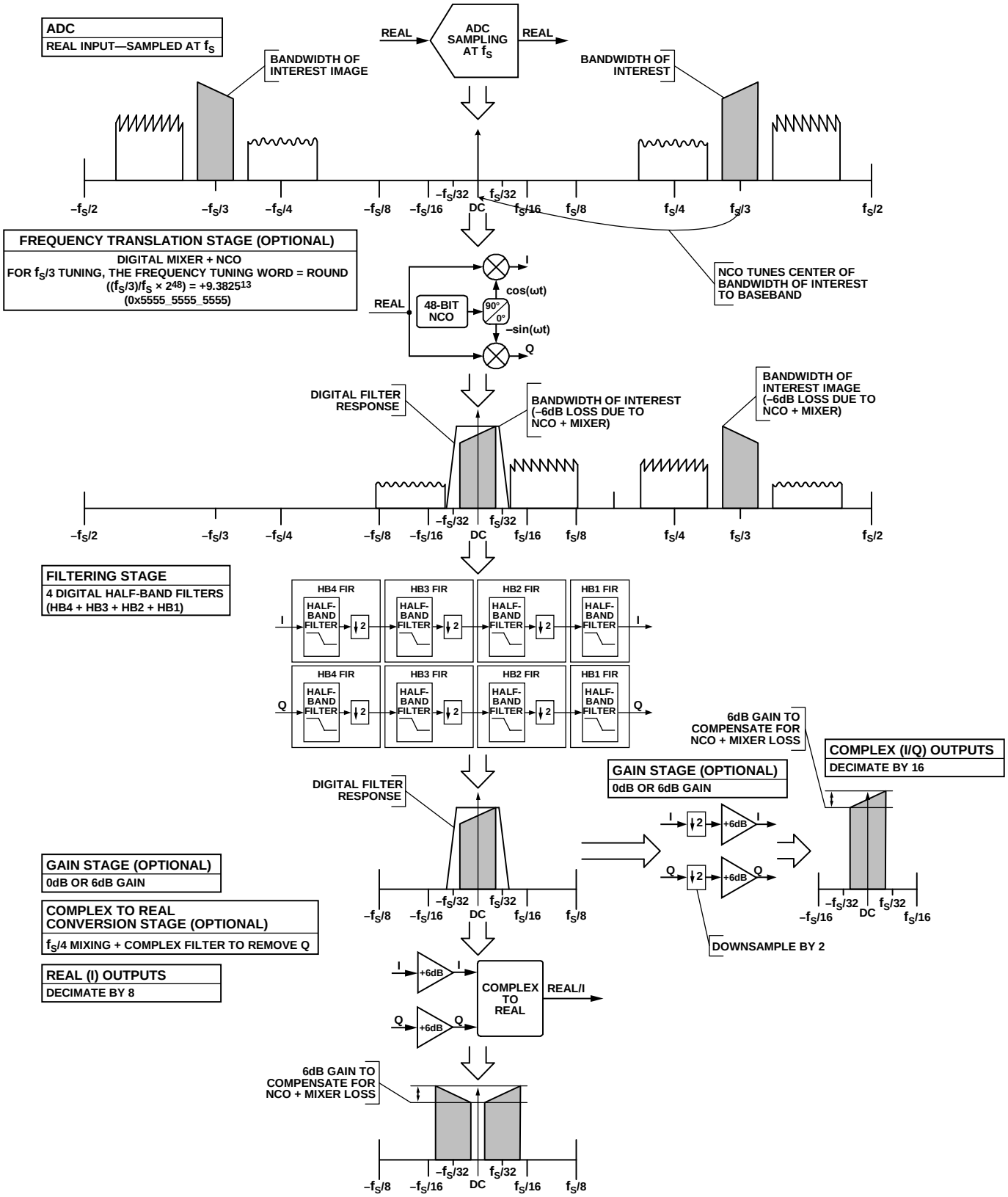

Figure 73. DDC Theory of Operation Example (Real Input, Decimate by 16)

Table 12. DDC Samples in Each JESD204B Link When Chip Decimation Ratio = 1

Real (I) Output (Complex to Real Enabled)				Complex (I/Q) Outputs (Complex to Real Disabled)			
HB1 FIR (DCM[1] = 1)	HB2 FIR + HB1 FIR (DCM[1] = 2)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB1 FIR (DCM[1] = 2)	HB2 FIR + HB1 FIR (DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N	N	N	N	N	N	N	N
N + 1	N	N	N	N	N	N	N
N + 2	N + 1	N	N	N + 1	N	N	N
N + 3	N + 1	N	N	N + 1	N	N	N
N + 4	N + 2	N + 1	N	N + 2	N + 1	N	N
N + 5	N + 2	N + 1	N	N + 2	N + 1	N	N
N + 6	N + 3	N + 1	N	N + 3	N + 1	N	N
N + 7	N + 3	N + 1	N	N + 3	N + 1	N	N
N + 8	N + 4	N + 2	N + 1	N + 4	N + 2	N + 1	N
N + 9	N + 4	N + 2	N + 1	N + 4	N + 2	N + 1	N
N + 10	N + 5	N + 2	N + 1	N + 5	N + 2	N + 1	N
N + 11	N + 5	N + 2	N + 1	N + 5	N + 2	N + 1	N
N + 12	N + 6	N + 3	N + 1	N + 6	N + 3	N + 1	N
N + 13	N + 6	N + 3	N + 1	N + 6	N + 3	N + 1	N
N + 14	N + 7	N + 3	N + 1	N + 7	N + 3	N + 1	N
N + 15	N + 7	N + 3	N + 1	N + 7	N + 3	N + 1	N
N + 16	N + 8	N + 4	N + 2	N + 8	N + 4	N + 2	N + 1
N + 17	N + 8	N + 4	N + 2	N + 8	N + 4	N + 2	N + 1
N + 18	N + 9	N + 4	N + 2	N + 9	N + 4	N + 2	N + 1
N + 19	N + 9	N + 4	N + 2	N + 9	N + 4	N + 2	N + 1
N + 20	N + 10	N + 5	N + 2	N + 10	N + 5	N + 2	N + 1
N + 21	N + 10	N + 5	N + 2	N + 10	N + 5	N + 2	N + 1
N + 22	N + 11	N + 5	N + 2	N + 11	N + 5	N + 2	N + 1
N + 23	N + 11	N + 5	N + 2	N + 11	N + 5	N + 2	N + 1
N + 24	N + 12	N + 6	N + 3	N + 12	N + 6	N + 3	N + 1
N + 25	N + 12	N + 6	N + 3	N + 12	N + 6	N + 3	N + 1
N + 26	N + 13	N + 6	N + 3	N + 13	N + 6	N + 3	N + 1
N + 27	N + 13	N + 6	N + 3	N + 13	N + 6	N + 3	N + 1
N + 28	N + 14	N + 7	N + 3	N + 14	N + 7	N + 3	N + 1
N + 29	N + 14	N + 7	N + 3	N + 14	N + 7	N + 3	N + 1
N + 30	N + 15	N + 7	N + 3	N + 15	N + 7	N + 3	N + 1
N + 31	N + 15	N + 7	N + 3	N + 15	N + 7	N + 3	N + 1

[1] DCM means decimation.

Table 13. DDC Samples in Each JESD204B Link When Chip Decimation Ratio = 2

Real (I) Output (Complex to Real Enabled)			Complex (I/Q) Outputs (Complex to Real Disabled)			
HB2 FIR + HB1 FIR (DCM[1] = 2)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB1 FIR (DCM[1] = 2)	HB2 FIR + HB1 FIR (DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N	N	N	N	N	N	N
N + 1	N	N	N + 1	N	N	N
N + 2	N + 1	N	N + 2	N + 1	N	N
N + 3	N + 1	N	N + 3	N + 1	N	N
N + 4	N + 2	N + 1	N + 4	N + 2	N + 1	N
N + 5	N + 2	N + 1	N + 5	N + 2	N + 1	N
N + 6	N + 3	N + 1	N + 6	N + 3	N + 1	N
N + 7	N + 3	N + 1	N + 7	N + 3	N + 1	N
N + 8	N + 4	N + 2	N + 8	N + 4	N + 2	N + 1
N + 9	N + 4	N + 2	N + 9	N + 4	N + 2	N + 1

Real (I) Output (Complex to Real Enabled)			Complex (I/Q) Outputs (Complex to Real Disabled)			
HB2 FIR + HB1 FIR (DCM[1] = 2)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB1 FIR (DCM[1] = 2)	HB2 FIR + HB1 FIR (DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N + 10	N + 5	N + 2	N + 10	N + 5	N + 2	N + 1
N + 11	N + 5	N + 2	N + 11	N + 5	N + 2	N + 1
N + 12	N + 6	N + 3	N + 12	N + 6	N + 3	N + 1
N + 13	N + 6	N + 3	N + 13	N + 6	N + 3	N + 1
N + 14	N + 7	N + 3	N + 14	N + 7	N + 3	N + 1
N + 15	N + 7	N + 3	N + 15	N + 7	N + 3	N + 1

[1] DCM means decimation.

Table 14. DDC Samples in Each JESD204B Link When Chip Decimation Ratio = 4

Real (I) Output (Complex to Real Enabled)		Complex (I/Q) Outputs (Complex to Real Disabled)		
HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB2 FIR + HB1 FIR (DCM[1] = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N	N	N	N	N
N + 1	N	N + 1	N	N
N + 2	N + 1	N + 2	N + 1	N
N + 3	N + 1	N + 3	N + 1	N
N + 4	N + 2	N + 4	N + 2	N + 1
N + 5	N + 2	N + 5	N + 2	N + 1
N + 6	N + 3	N + 6	N + 3	N + 1
N + 7	N + 3	N + 7	N + 3	N + 1

[1] DCM means decimation.

Table 15. DDC Samples in Each JESD204B Link When Chip Decimation Ratio = 8

Real (I) Output (Complex to Real Enabled)	Complex (I/Q) Outputs (Complex to Real Disabled)	
HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
N	N	N
N + 1	N + 1	N
N + 2	N + 2	N + 1
N + 3	N + 3	N + 1
N + 4	N + 4	N + 2
N + 5	N + 5	N + 2
N + 6	N + 6	N + 3
N + 7	N + 7	N + 3

[1] DCM means decimation.

Table 16. DDC Samples in Each JESD204B Link When Chip Decimation Ratio = 16

Real (I) Output (Complex to Real Enabled)	Complex (I/Q) Outputs (Complex to Real Disabled)
HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM[1] = 16)
Not applicable	N
Not applicable	N + 1
Not applicable	N + 2
Not applicable	N + 3

[1] DCM means decimation.

For example, if the chip decimation ratio is set to decimate by 4, DDC 0 is set to use the HB2 + HB1 filters (complex outputs, decimate by 4) and DDC 1 is set to use the HB4 + HB3 + HB2 + HB1 filters (real outputs, decimate by 8). DDC 1 repeats its output data two times for every one DDC 0 output. The resulting output samples are shown in Table 17.

Table 17. DDC Output Samples in Each JESD204B Link When Chip DCM[1] = 4, DDC 0 DCM[1] = 4 (Complex), and DDC 1 DCM[1] = 8 (Real)

	DDC 0		DDC 1	
DDC Input Samples	**Output Port I**	**Output Port Q**	**Output Port I**	**Output Port Q**
N	I0 (N)	Q0 (N)	I1 (N)	Not applicable
N + 1				
N + 2				
N + 3				
N + 4	I0 (N + 1)	Q0 (N + 1)		
N + 5				
N + 6				
N + 7				
N + 8	I0 (N + 2)	Q0 (N + 2)	I1 (N + 1)	Not applicable
N + 9				
N + 10				
N + 11				
N + 12	I0 (N + 3)	Q0 (N + 3)		
N + 13				
N + 14				
N + 15				

[1] DCM means decimation.

FREQUENCY TRANSLATION

OVERVIEW

Frequency translation is accomplished by using a 48-bit complex NCO with a digital quadrature mixer. This stage translates either a real or complex input signal from an IF to a baseband complex digital output (carrier frequency = 0 Hz).

The frequency translation stage of each DDC can be controlled individually and supports four different IF modes using Bits[5:4] of the DDC control registers (Register 0x0310 and Register 0x0330) in conjunction with the pair index register (Register 0x0009). These IF modes are

- Variable IF mode
- 0 Hz IF or zero IF (ZIF) mode
- $f_S/4$ Hz IF mode
- Test mode

Variable IF Mode

The NCO and mixers are enabled. NCO output frequency can be used to digitally tune the IF frequency.

0 Hz IF (ZIF) Mode

The mixers are bypassed, and the NCO is disabled.

$f_S/4$ Hz IF Mode

The mixers and the NCO are enabled in special downmixing by $f_S/4$ mode to save power.

Test Mode

Input samples are forced to 0.9599 to positive full scale. The NCO is enabled. This test mode allows the NCOs to directly drive the decimation filters.

Figure 74 and Figure 75 show examples of the frequency translation stage for both real and complex inputs.

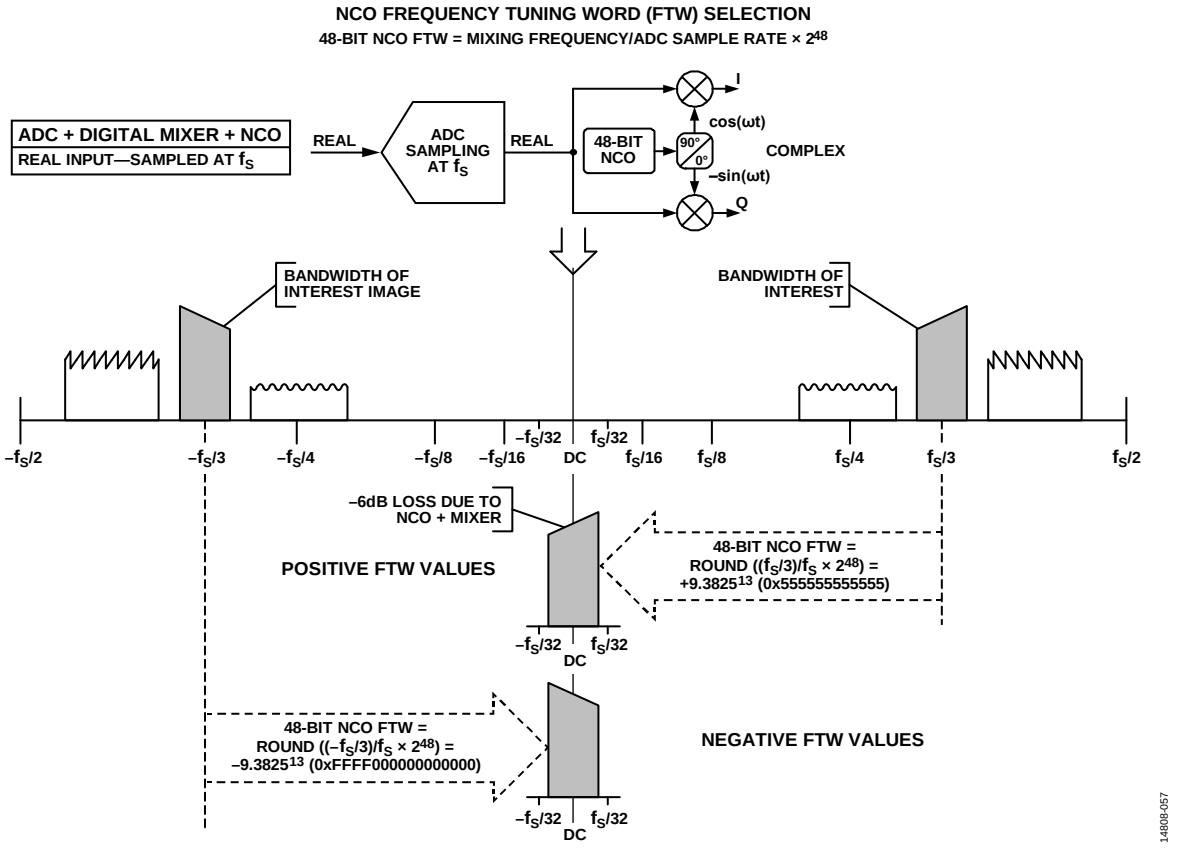

Figure 74. DDC NCO Frequency Tuning Word Selection—Real Inputs

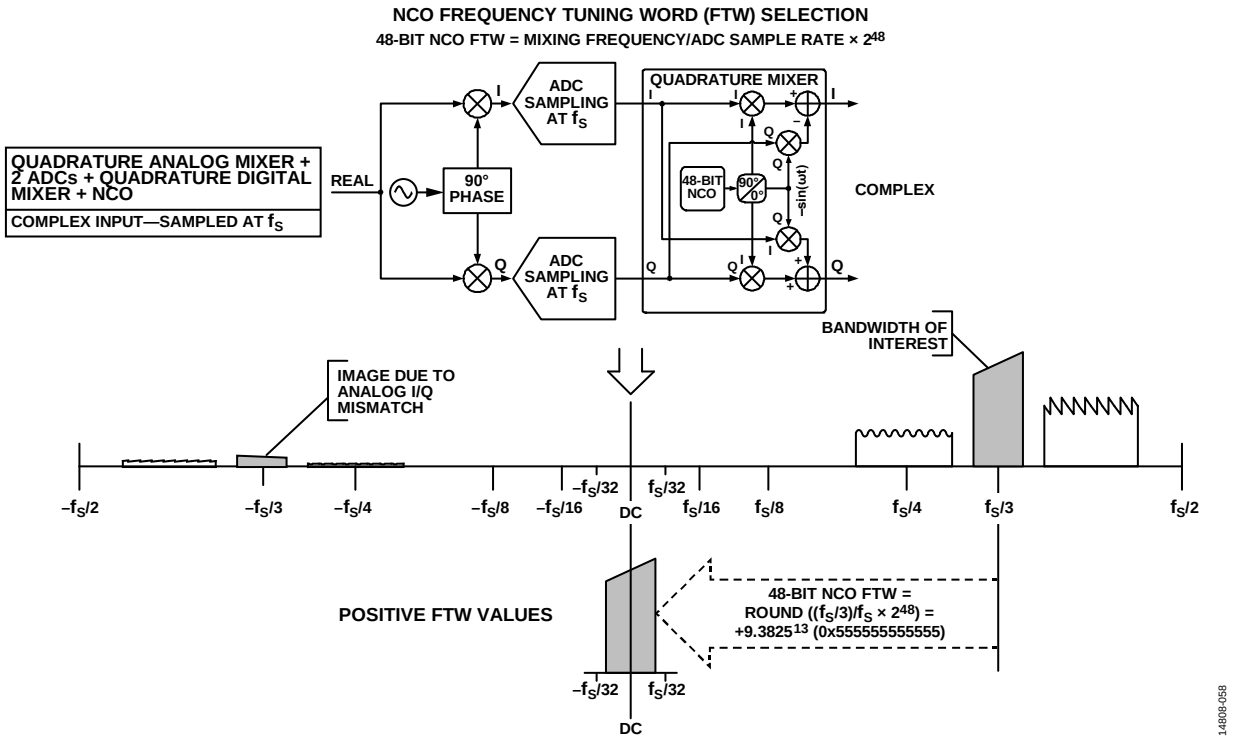

Figure 75. DDC NCO Frequency Tuning Word Selection—Complex Inputs

DDC NCO AND MIXER LOSS AND SFDR

When mixing a real input signal down to baseband, 6 dB of loss is introduced in the signal due to filtering of the negative image. An additional 0.05 dB of loss is introduced by the NCO. The total loss of a real input signal mixed down to baseband is 6.05 dB. For this reason, it is recommended that the user compensate for this loss by enabling the 6 dB of gain in the gain stage of the DDC to recenter the dynamic range of the signal within the full scale of the output bits.

When mixing a complex input signal down to baseband, the maximum value that each I/Q sample can reach is 1.414 × full scale after it passes through the complex mixer. To avoid over-range of the I/Q samples and to keep the data bit widths aligned with real mixing, 3.06 dB of loss is introduced in the mixer for complex signals. An additional 0.05 dB of loss is introduced by the NCO. The total loss of a complex input signal mixed down to baseband is −3.11 dB.

The worst case spurious signal from the NCO is greater than 102 dBc SFDR for all output frequencies.

NUMERICALLY CONTROLLED OSCILLATOR

The AD9694 has a 48-bit NCO for each DDC that enables the frequency translation process. The NCO allows the input spectrum to be tuned to dc, where it can be effectively filtered by the subsequent filter blocks to prevent aliasing. The NCO can be set up by providing a frequency tuning word (FTW) and a phase offset word (POW).

Setting Up the NCO FTW and POW

The NCO frequency value is given by the 32-bit twos complement number entered in the NCO FTW. Frequencies between $-f_S/2$ and $+f_S/2$ ($f_S/2$ excluded) are represented using the following frequency words:

- 0x800 represents a frequency of $-f_S/2$.
- 0x000 represents dc (frequency is 0 Hz).
- 0x7FF represents a frequency of $+f_S/2 - f_S/2^{12}$.

The NCO frequency tuning word can be calculated using the following equation:

$$NCO\_FTW = \text{round}\left(2^{48}\frac{\text{mod}(f_C, f_S)}{f_S}\right)$$

where:
NCO_FTW is a 48-bit twos complement number representing the NCO FTW.
f_C is the desired carrier frequency in Hz.
f_S is the AD9694 sampling frequency (clock rate) in Hz.
round( ) is a rounding function. For example, round(3.6) = 4 and for negative numbers, round(−3.4) = −3.
mod( ) is a remainder function. For example, mod(110,100) = 10 and for negative numbers, mod(−32,10) = −2.

This equation applies to the aliasing of signals in the digital domain (that is, aliasing introduced when digitizing analog signals).

For example, if the ADC sampling frequency (f_S) is 500 MSPS and the carrier frequency (f_C) is 140.312 MHz, then

$$NCO\_FTW = \text{round}\left(2^{48}\frac{\text{mod}(140.312,500)}{500}\right) = 7.89886 \times 10^{13}\ \text{Hz}$$

This, in turn, converts to 0x47D in the 12-bit twos complement representation for NCO_FTW. The actual carrier frequency, f_{C_ACTUAL}, is calculated based on the following equation:

$$f_{C\_ACTUAL} = \frac{NCO\_FTW \times f_S}{2^{48}} = 140.312\ \text{MHz}$$

A 48-bit POW is available for each NCO to create a known phase relationship between multiple AD9694 chips or individual DDC channels inside one AD9694 chip.

Use the following procedure to update the FTW and/or POW registers to ensure proper operation of the NCO:

1. Write to the FTW registers for all the DDCs.
2. Write to the POW registers for all the DDCs.
3. Synchronize the NCOs either through the DDC NCO soft reset bit (Register 0x0300, Bit 4), which is accessible through the SPI or through the assertion of the SYSREF± pin.

It is important to note that the NCOs must be synchronized either through the SPI or through the SYSREF± pin after all writes to the FTW or POW registers are complete. This step is necessary to ensure the proper operation of the NCO.

NCO Synchronization

Each NCO contains a separate phase accumulator word (PAW). The initial reset value of each PAW is set to zero and the phase increment value of each PAW is determined by the FTW. The POW is added to the PAW to produce the instantaneous phase of the NCO. See the Setting Up the NCO FTW and POW section for more information.

Use the following two methods to synchronize multiple PAWs within the chip:

- Using the SPI. Use the DDC NCO soft reset bit in the DDC synchronization control register (Register 0x0300, Bit 4) to reset all the PAWs in the chip, which is accomplished by setting the DDC NCO soft reset bit high and then setting this bit low. This method can only be used to synchronize DDC channels within the same pair (A/B or C/D) of a AD9694 chip.
- Using the SYSREF± pin. When the SYSREF± pin is enabled in the SYSREF± control registers (Register 0x0120 and Register 0x0121) and the DDC synchronization is enabled in the DDC synchronization control register (Register 0x0300, Bits[1:0]), any subsequent SYSREF± event resets all the PAWs in the chip. This method can be used to synchronize DDC channels within the same AD9694 chip or DDC channels within separate AD9694 chips.

Mixer

The NCO is accompanied by a mixer. The NCO mixer operation is similar to that of an analog quadrature mixer. It performs the downconversion of input signals (real or complex) by using the NCO frequency as a local oscillator. For real input signals, this mixer performs a real mixer operation (with two multipliers). For complex input signals, the mixer performs a complex mixer operation (with four multipliers and two adders). The mixer adjusts its operation based on the input signal (real or complex) provided to each individual channel. The selection of real or complex inputs can be controlled individually for each DDC block using Bit 7 of the DDC control registers (Register 0x0310 and Register 0x0330) in conjunction with the pair index register (Register 0x0009).

FIR FILTERS

OVERVIEW

Four sets of decimate by 2, low-pass, half-band, finite impulse response (FIR) filters (labeled HB1 FIR, HB2 FIR, HB3 FIR, and HB4 FIR in Figure 72) follow the frequency translation stage. After the carrier of interest is tuned down to dc (carrier frequency = 0 Hz), these filters efficiently lower the sample rate, while providing sufficient alias rejection from unwanted adjacent carriers around the bandwidth of interest.

HB1 FIR is always enabled and cannot be bypassed in DDC mode. The HB2, HB3, and HB4 FIR filters are optional and can be bypassed for higher output sample rates.

Table 18 shows the different bandwidths selectable by including different half-band filters. In all cases, the DDC filtering stage on the AD9694 provides <−0.001 dB of pass-band ripple and >100 dB of stop band alias rejection.

Table 19 shows the amount of stop band alias rejection for multiple pass-band ripple/cutoff points. The decimation ratio of the filtering stage of each DDC can be controlled individually through Bits[1:0] of the DDC control registers (Register 0x0310 and Register 0x0330) in conjunction with the pair index register (Register 0x0009).

Table 18. DDC Filter Characteristics

	Real Output		Complex (I/Q) Output					
Half-Band Filter Selection	**Decimation Ratio**	**Output Sample Rate (MSPS)**	**Decimation Ratio**	**Output Sample Rate (MSPS)**	**Alias Protected Bandwidth (MHz)**	**Ideal SNR Improvement[1] (dB)**	**Pass-Band Ripple (dB)**	**Alias Rejection (dB)**
HB1	1	500	2	250 (I) + 250 (Q)	200	1	<−0.0001	>100
HB1 + HB2	2	250	4	125 (I) + 125 (Q)	100	4		
HB1 + HB2 + HB3	4	125	8	62.5 (I) + 62.5 (Q)	50	7		
HB1 + HB2 + HB3 + HB4	8	62.5	16	31.25 (I) + 31.25 (Q)	25	10		

[1] Ideal SNR improvement due to oversampling and filtering = 10log(bandwidth/(f_S/2)).

Table 19. DDC Filter Alias Rejection

Alias Rejection (dB)	Pass-Band Ripple/Cutoff Point (dB)	Alias Protected Bandwidth for Real (I) Outputs[1]	Alias Protected Bandwidth for Complex (I/Q) Outputs
>100	<−0.0001	<40% × f_{OUT}	<80% × f_{OUT}
95	<−0.0002	<40.12% × f_{OUT}	<80.12% × f_{OUT}
90	<−0.0003	<40.23% × f_{OUT}	<80.46% × f_{OUT}
85	<−0.0005	<40.36% × f_{OUT}	<80.72% × f_{OUT}
80	<−0.0009	<40.53% × f_{OUT}	<81.06% × f_{OUT}
25.07	−0.5	45.17% × f_{OUT}	90.34% × f_{OUT}
19.3	−1.0	46.2% × f_{OUT}	92.4% × f_{OUT}
10.7	−3.0	48.29% × f_{OUT}	96.58% × f_{OUT}

[1] f_{OUT} = ADC input sample rate ÷ DDC decimation.

HALF-BAND FILTERS

The AD9694 offers four half-band filters to enable digital signal processing of the ADC converted data. These half-band filters are bypassable and can be individually selected.

HB4 Filter

The first decimate by 2, half-band, low-pass, FIR filter (HB4) uses an 11-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB4 filter is only used when complex outputs (decimate by 16) or real outputs (decimate by 8) are enabled; otherwise, it is bypassed. Table 20 and Figure 76 show the coefficients and response of the HB4 filter.

Table 20. HB4 Filter Coefficients

HB4 Coefficient Number	Normalized Coefficient	Decimal Coefficient (15-Bit)
C1, C11	0.006042	99
C2, C10	0	0
C3, C9	−0.049377	−809
C4, C8	0	0
C5, C7	0.293334	4806
C6	0.500000	8192

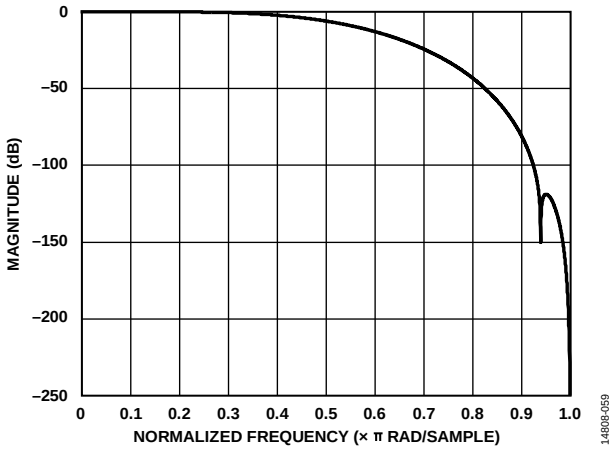

Figure 76. HB4 Filter Response

HB3 Filter

The second decimate by 2, half-band, low-pass, FIR filter (HB3) uses an 11-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB3 filter is only used when complex outputs (decimate by 8 or 16) or real outputs (decimate by 4 or 8) are enabled; otherwise, it is bypassed. Table 21 and Figure 77 show the coefficients and response of the HB3 filter.

Table 21. HB3 Filter Coefficients

HB3 Coefficient Number	Normalized Coefficient	Decimal Coefficient (17-Bit)
C1, C11	0.006638	435
C2, C10	0	0
C3, C9	−0.051055	−3346
C4, C8	0	0
C5, C7	0.294418	19,295
C6	0.500000	32,768

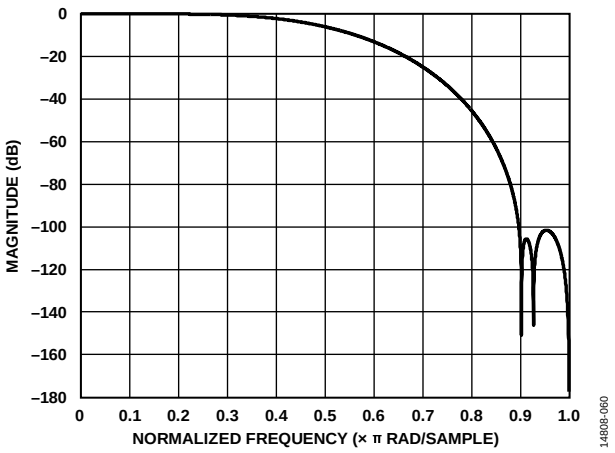

Figure 77. HB3 Filter Response

HB2 Filter

The third decimate by 2, half-band, low-pass, FIR filter (HB2) uses a 19-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption.

The HB2 filter is only used when complex or real outputs (decimate by 4, 8, or 16) is enabled; otherwise, it is bypassed.

Table 22 and Figure 78 show the coefficients and response of the HB2 filter.

Table 22. HB2 Filter Coefficients

HB2 Coefficient Number	Normalized Coefficient	Decimal Coefficient (18-Bit)
C1, C19	0.000671	88
C2, C18	0	0
C3, C17	−0.005325	−698
C4, C16	0	0
C5, C15	0.022743	2981
C6, C14	0	0
C7, C13	−0.074181	−9723
C8, C12	0	0
C9, C11	0.306091	40,120
C10	0.500000	65,536

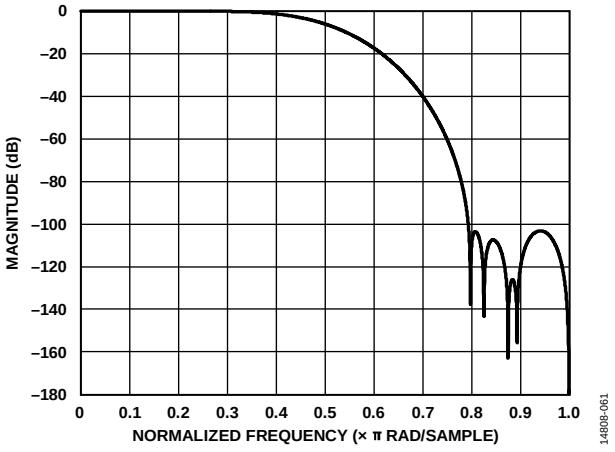

Figure 78. HB2 Filter Response

HB1 Filter

The fourth and final decimate by 2, half-band, low-pass, FIR filter (HB1) uses a 63-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB1 filter is always enabled and cannot be bypassed. Table 23 and Figure 79 show the coefficients and response of the HB1 filter.

Table 23. HB1 Filter Coefficients

HB1 Coefficient Number	Normalized Coefficient	Decimal Coefficient (20-Bit)
C1, C63	−0.000019	−10
C2, C62	0	0
C3, C61	0.000072	38
C4, C60	0	0
C5, C59	−0.000194	−102
C6, C58	0	0
C7, C57	0.000442	232
C8, C56	0	0
C9, C55	−0.000891	−467
C10, C54	0	0
C11, C53	0.001644	862
C12, C52	0	0
C13, C51	−0.002840	−1489
C14, C50	0	0
C15, C49	0.004653	2440
C16, C48	0	0
C17, C47	−0.007311	−3833
C18, C46	0	0
C19, C45	0.011121	5831
C20, C44	0	0
C21, C43	−0.016553	−8679
C22, C42	0	0
C23, C41	0.024420	12,803
C24, C40	0	0
C25, C39	−0.036404	−19,086
C26, C38	0	0
C27, C37	0.056866	29,814
C28, C36	0	0
C29, C35	−0.101892	−53,421
C30, C34	0	0
C31, C33	0.316883	166,138
C32	0.500000	262,144

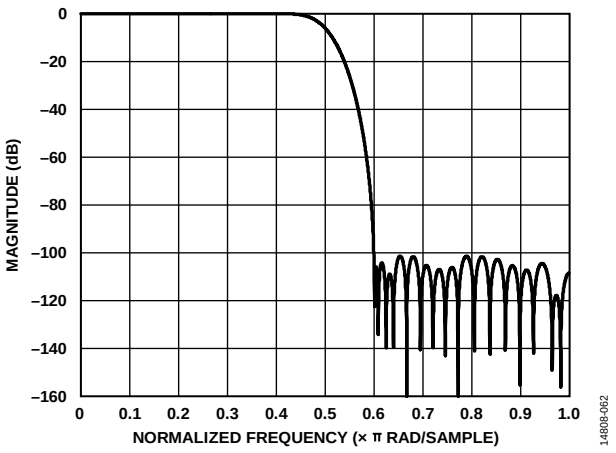

Figure 79. HB1 Filter Response

DDC GAIN STAGE

Each DDC contains an independently controlled gain stage. The gain is selectable as either 0 dB or 6 dB. When mixing a real input signal down to baseband, it is recommended that the user enable the 6 dB of gain to recenter the dynamic range of the signal within the full scale of the output bits.

When mixing a complex input signal down to baseband, the mixer has already recentered the dynamic range of the signal within the full scale of the output bits, and no additional gain is necessary. However, the optional 6 dB gain compensates for low signal strengths. The downsample by 2 portion of the HB1 FIR filter is bypassed when using the complex to real conversion stage.

DDC COMPLEX TO REAL CONVERSION

Each DDC contains an independently controlled complex to real conversion block. The complex to real conversion block reuses the last filter (HB1 FIR) in the filtering stage and an $f_S/4$ complex mixer to upconvert the signal. After upconverting the signal, the Q portion of the complex mixer is no longer needed and is dropped.

Figure 80 shows a simplified block diagram of the complex to real conversion.

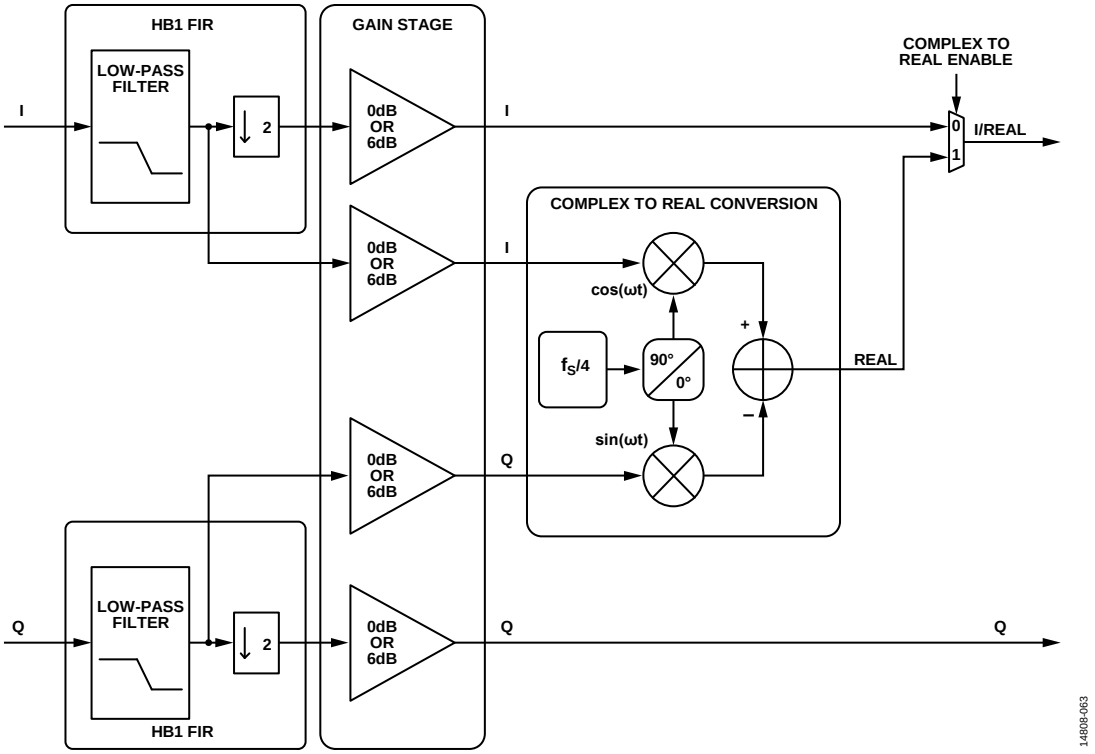

Figure 80. Complex to Real Conversion Block

DDC EXAMPLE CONFIGURATIONS

Table 24 describes the register settings for multiple DDC example configurations.

Table 24. DDC Example Configurations

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings[2]
One DDC	2	Complex	Complex	40% × f_S	2	Register 0x0009 = 0x01, 0x02, or 0x03 (pair selection) Register 0x0200 = 0x01 (one DDC; I/Q selected) Register 0x0201 = 0x01 (chip decimate by 2) Register 0x0310 = 0x83 (complex mixer; 0 dB gain; variable IF; complex outputs; HB1 filter) Register 0x0311 = 0x04 (DDC I input = ADC Channel A/Channel C; DDC Q input = ADC Channel B/Channel D Register 0x0314, Register 0x0315, Register 0x0316, Register 0x0317, Register 0x0318, Register 0x031A, Register 0x031D, Register 0x031E, Register 0x031F, Register 0x0320, Register 0x0321, Register 0x0322 = FTW and POW set as required by application for DDC 0
One DDC	4	Complex	Complex	20% × f_S	2	Register 0x0009 = 0x01, 0x02, or 0x03 (pair selection) Register 0x0200 = 0x01 (one DDC; I/Q selected) Register 0x0201 = 0x02 (chip decimate by 4) Register 0x0310 = 0x80 (complex mixer; 0 dB gain; variable IF; complex outputs; HB2 + HB1 filters)

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings[2]
						Register 0x0311 = 0x04 (DDC I input = ADC Channel A/C; DDC Q input = ADC Channel B/ Channel D) Register 0x0314, Register 0x0315, Register 0x0316, Register 0x0317, Register 0x0318, Register 0x031A, Register 0x031D, Register 0x031E, Register 0x031F, Register 0x0320, Register 0x0321, Register 0x0322 = FTW and POW set as required by application for DDC 0
Two DDCs	2	Real	Real	20% × f_S	2	Register 0x0009 = 0x01, 0x02, or 0x03 (pair selection) Register 0x0200 = 0x22 (two DDCs; I only selected) Register 0x0201 = 0x01 (chip decimate by 2) Register 0x0310, Register 0x0330 = 0x48 (real mixer; 6 dB gain; variable IF; real output; HB2 + HB1 filters) Register 0x0311 = 0x00 (DDC 0 I input = ADC Channel A/Channel C; DDC 0 Q input = ADC Channel A/Channel C) Register 0x0331 = 0x05 (DDC 1 I input = ADC Channel B/Channel D; DDC 1 Q input = ADC Channel B/Channel D Register 0x0314, Register 0x0315, Register 0x0316, Register 0x0317, Register 0x0318, Register 0x031A, Register 0x031D, Register 0x031E, Register 0x031F, Register 0x0320, Register 0x0321, Register 0x0322 = FTW and POW set as required by application for DDC 0 Register 0x0334, Register 0x0335, Register 0x0336, Register 0x0337, Register 0x0338, Register 0x033A, Register 0x033D, Register 0x033E, Register 0x033F, Register 0x0340, Register 0x0341, Register 0x0342 = FTW and POW set as required by application for DDC 1
Two DDCs	2	Complex	Complex	40% × f_S	4	Register 0x0009 = 0x01, 0x02, or 0x03 (pair selection) Register 0x0200 = 0x22 (two DDCs; I only selected) Register 0x0201 = 0x01 (chip decimate by 2) Register 0x0310, Register 0x0330 = 0x4B (complex mixer; 6 dB gain; variable IF; complex output; HB1 filter) Register 0x0311, Register 0x0331 = 0x04 (DDC 0 I input = ADC Channel A/Channel C; DDC 0 Q input = ADC Channel B/Channel D) Register 0x0314, Register 0x0315, Register 0x0316, Register 0x0317, Register 0x0318, Register 0x031A, Register 0x031D, Register 0x031E, Register 0x031F, Register 0x0320, Register 0x0321, Register 0x0322 = FTW and POW set as required by application for DDC 0 Register 0x0334, Register 0x0335, Register 0x0336, Register 0x0337, Register 0x0338, Register 0x033A, Register 0x033D, Register 0x033E, Register 0x033F, Register 0x0340, Register 0x0341, Register 0x0342 = FTW and POW set as required by application for DDC 1

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings[2]
Two DDCs	4	Complex	Complex	20% × f_S	4	Register 0x0009 = 0x01, 0x02, or 0x03 (pair selection) Register 0x0200 = 0x02 (two DDCs; I/Q selected) Register 0x0201 = 0x02 (chip decimate by 4) Register 0x0310, Register 0x0330 = 0x80 (complex mixer; 0 dB gain; variable IF; complex outputs; HB2 + HB1 filters) Register 0x0311, Register 0x0331 = 0x04 (DDC I input = ADC Channel A/Channel C; DDC Q input = ADC Channel B/Channel D) Register 0x0314, Register 0x0315, Register 0x0316, Register 0x0317, Register 0x0318, Register 0x031A, Register 0x031D, Register 0x031E, Register 0x031F, Register 0x0320, Register 0x0321, Register 0x0322 = FTW and POW set as required by application for DDC 0 Register 0x0334, Register 0x0335, Register 0x0336, Register 0x0337, Register 0x0338, Register 0x033A, Register 0x033D, Register 0x033E, Register 0x033F, Register 0x0340, Register 0x0341, Register 0x0342 = FTW and POW set as required by application for DDC 1
Two DDCs	4	Complex	Real	10% × f_S	2	Register 0x0009 = 0x01, 0x02, or 0x03 (pair selection) Register 0x0200 = 0x22 (two DDCs; I only selected) Register 0x0201 = 0x02 (chip decimate by 4) Register 0x0310, Register 0x0330 = 0x89 (complex mixer; 0 dB gain; variable IF; real output; HB3 + HB2 + HB1 filters) Register 0x0311, Register 0x0331 = 0x04 (DDC I input = ADC Channel A/Channel C; DDC Q input = ADC Channel B/Channel D) Register 0x0314, Register 0x0315, Register 0x0316, Register 0x0317, Register 0x0318, Register 0x031A, Register 0x031D, Register 0x031E, Register 0x031F, Register 0x0320, Register 0x0321, Register 0x0322 = FTW and POW set as required by application for DDC 0 Register 0x0334, Register 0x0335, Register 0x0336, Register 0x0337, Register 0x0338, Register 0x033A, Register 0x033D, Register 0x033E, Register 0x033F, Register 0x0340, Register 0x0341, Register 0x0342 = FTW and POW set as required by application for DDC 1
Two DDCs	4	Real	Real	10% × f_S	2	Register 0x0009 = 0x01, 0x02, or 0x03 (pair selection) Register 0x0200 = 0x22 (two DDCs; I only selected) Register 0x0201 = 0x02 (chip decimate by 4) Register 0x0310, Register 0x0330 = 0x49 (real mixer; 6 dB gain; variable IF; real output; HB3 + HB2 + HB1 filters) Register 0x0311 = 0x00 (DDC 0 I input = ADC Channel A/Channel C; DDC 0 Q input = ADC Channel A/Channel C)

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings[2]
						Register 0x0331 = 0x05 (DDC 1 I input = ADC Channel B/Channel D; DDC 1 Q input = ADC Channel B/Channel D) Register 0x0314, Register 0x0315, Register 0x0316, Register 0x0317, Register 0x0318, Register 0x031A, Register 0x031D, Register 0x031E, Register 0x031F, Register 0x0320, Register 0x0321, Register 0x0322 = FTW and POW set as required by application for DDC 0 Register 0x0334, Register 0x0335, Register 0x0336, Register 0x0337, Register 0x0338, Register 0x033A, Register 0x033D, Register 0x033E, Register 0x033F, Register 0x0340, Register 0x0341, Register 0x0342 = FTW and POW set as required by application for DDC 1
Two DDCs	4	Real	Complex	20% × f_S	4	Register 0x0009 = 0x01, 0x02, or 0x03 (pair selection) Register 0x0200 = 0x02 (two DDCs; I/Q selected) Register 0x0201 = 0x02 (chip decimate by 4) Register 0x0310, Register 0x0330 = 0x40 (real mixer; 6 dB gain; variable IF; complex output; HB2 + HB1 filters) Register 0x0311 = 0x00 (DDC 0 I input = ADC Channel A/Channel C; DDC 0 Q input = ADC Channel A/Channel C) Register 0x0331 = 0x05 (DDC 1 I input = ADC Channel B/Channel D; DDC 1 Q input = ADC Channel B/Channel D) Register 0x0314, Register 0x0315, Register 0x0316, Register 0x0317, Register 0x0318, Register 0x031A, Register 0x031D, Register 0x031E, Register 0x031F, Register 0x0320, Register 0x0321, Register 0x0322 = FTW and POW set as required by application for DDC 0 Register 0x0334, Register 0x0335, Register 0x0336, Register 0x0337, Register 0x0338, Register 0x033A, Register 0x033D, Register 0x033E, Register 0x033F, Register 0x0340, Register 0x0341, Register 0x0342 = FTW and POW set as required by application for DDC 1
Two DDCs	8	Real	Real	5% × f_S	2	Register 0x0009 = 0x01, 0x02, or 0x03 (pair selection) Register 0x0200 = 0x22 (two DDCs; I only selected) Register 0x0201 = 0x03 (chip decimate by 8) Register 0x0310, Register 0x0330 = 0x4A (real mixer; 6 dB gain; variable IF; real output; HB4 + HB3 + HB2 + HB1 filters) Register 0x0311 = 0x00 (DDC 0 I input = ADC Channel A/Channel C; DDC 0 Q input = ADC Channel A/Channel C) Register 0x0331 = 0x05 (DDC 1 I input = ADC Channel B/Channel D; DDC 1 Q input = ADC Channel B/Channel D)

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings[2]
						Register 0x0314, Register 0x0315, Register 0x0316, Register 0x0317, Register 0x0318, Register 0x031A, Register 0x031D, Register 0x031E, Register 0x031F, Register 0x0320, Register 0x0321, Register 0x0322 = FTW and POW set as required by application for DDC 0 Register 0x0334, Register 0x0335, Register 0x0336, Register 0x0337, Register 0x0338, Register 0x033A, Register 0x033D, Register 0x033E, Register 0x033F, Register 0x0340, Register 0x0341, Register 0x0342 = FTW and POW set as required by application for DDC 1

[1] f_S is the ADC sample rate. Bandwidths listed are <−0.001 dB of pass-band ripple and >100 dB of stop band alias rejection.
[2] The NCOs must be synchronized either through the SPI or through the SYSREF± pin after all writes to the FTW or POW registers have completed. This synchronization is necessary to ensure the proper operation of the NCO. See the NCO Synchronization section for more information.

DIGITAL OUTPUTS

INTRODUCTION TO THE JESD204B INTERFACE

The AD9694 digital outputs are designed to the JEDEC standard, JESD204B, serial interface for data converters. JESD204B is a protocol to link the AD9694 to a digital processing device over a serial interface with lane rates of up to 15 Gbps. The benefits of the JESD204B interface over LVDS include a reduction in required board area for data interface routing, and an ability to enable smaller packages for converter and logic devices.

SETTING UP THE AD9694 DIGITAL INTERFACE

The following SPI writes are required for the AD9694 at startup and each time the ADC is reset (datapath reset, soft reset, link power-down/power-up, or hard reset):

1. Write 0x4F to Register 0x1228.
2. Write 0x0F to Register 0x1228.
3. Write 0x04 to Register 0x1222.
4. Write 0x00 to Register 0x1222.
5. Write 0x08 to Register 0x1262.
6. Write 0x00 to Register 0x1262.

The JESD204B data transmit blocks, JTX, assemble the parallel data from the ADC into frames and uses 8-bit/10-bit encoding as well as optional scrambling to form serial output data. Lane synchronization is supported through the use of special control characters during the initial establishment of the link. Additional control characters are embedded in the data stream to maintain synchronization thereafter. A JESD204B receiver is required to complete the serial link. For additional details on the JESD204B interface, refer to the JESD204B standard.

The JESD204B data transmit blocks in the AD9694 map up to two physical ADCs or up to four virtual converters (when the DDCs are enabled) over each of the two JESD204B links. Each link can be configured to use one or two JESD204B lanes for up to a total of four lanes for the AD9694 chip. The JESD204B specification refers to a number of parameters to define the link, and these parameters must match between the JESD204B transmitter (the AD9694 output) and the JESD204B receiver (the logic device input). The JESD204B outputs of the AD9694 function effectively as two individual JESD204B links. The two JESD204B links can be synchronized if desired using the SYSREF± input.

Each JESD204B link is described according to the following parameters:

- L is the number of lanes per converter device (lanes per link) (AD9694 value = 1 or 2)
- M is the number of converters per converter device (virtual converters per link) (AD9694 value = 1, 2, or 4)
- F is the number of octets per frame (AD9694 value = 1, 2, 4, or 8)
- N′ is the number of bits per sample (JESD204B word size) (AD9694 value = 8 or 16)
- N is the converter resolution (AD9694 value = 7 to 16)
- CS is the number of control bits per sample (AD9694 value = 0, 1, 2, or 3)
- K is the number of frames per multiframe (AD9694 value = 4, 8, 12, 16, 20, 24, 28, or 32)
- S is the samples transmitted per single converter per frame cycle (AD9694 value is set automatically based on L, M, F, and N′)
- HD is high density mode (AD9694 value is set automatically based on L, M, F, and N′)
- CF is the number of control words per frame clock cycle per converter device (AD9694 value = 0)

Figure 81 shows a simplified block diagram of the AD9694 JESD204B link. By default, the AD9694 is configured to use four converters and four lanes. The Converter A and Converter B data is output to SERDOUTAB0± and SERDOUTAB1±, and the Converter C and Converter D data is output to SERDOUTCD0± and SERDOUTCD1±. The AD9694 allows other configurations, such as combining the outputs of each pair of converters into a single lane, or changing the mapping of the digital output paths. These modes are set up via a quick configuration register in the SPI register map, including additional customizable options.

By default in the AD9694, the 14-bit converter word from each converter is separated into two octets (eight bits of data). Bit 13 (MSB) through Bit 6 are in the first octet. The second octet contains Bit 5 through Bit 0 (LSB) and two tail bits. The tail bits can be configured as zeros or a pseudorandom number sequence. The tail bits can also be replaced with control bits indicating overrange, SYSREF±, or fast detect output. Control bits are filled and inserted MSB first such that enabling CS = 1 activates Control Bit 2, enabling CS = 2 activates Control Bit 2 and Control Bit 1, and enabling CS = 3 activates Control Bit 2, Control Bit 1, and Control Bit 0.

The two resulting octets can be scrambled. Scrambling is optional; however, it is recommended to avoid spectral peaks when transmitting similar digital data patterns. The scrambler uses a self synchronizing, polynomial-based algorithm defined by the equation $1 + x^{14} + x^{15}$. The descrambler in the receiver is a self synchronizing version of the scrambler polynomial.

The two octets are then encoded with an 8-bit/10-bit encoder. The 8-bit/10-bit encoder works by taking eight bits of data (an octet) and encoding them into a 10-bit symbol. Figure 82 shows how the 14-bit data is taken from the ADC, the tail bits are added, the two octets are scrambled, and how the octets are encoded into two 10-bit symbols. Figure 82 shows the default data format.

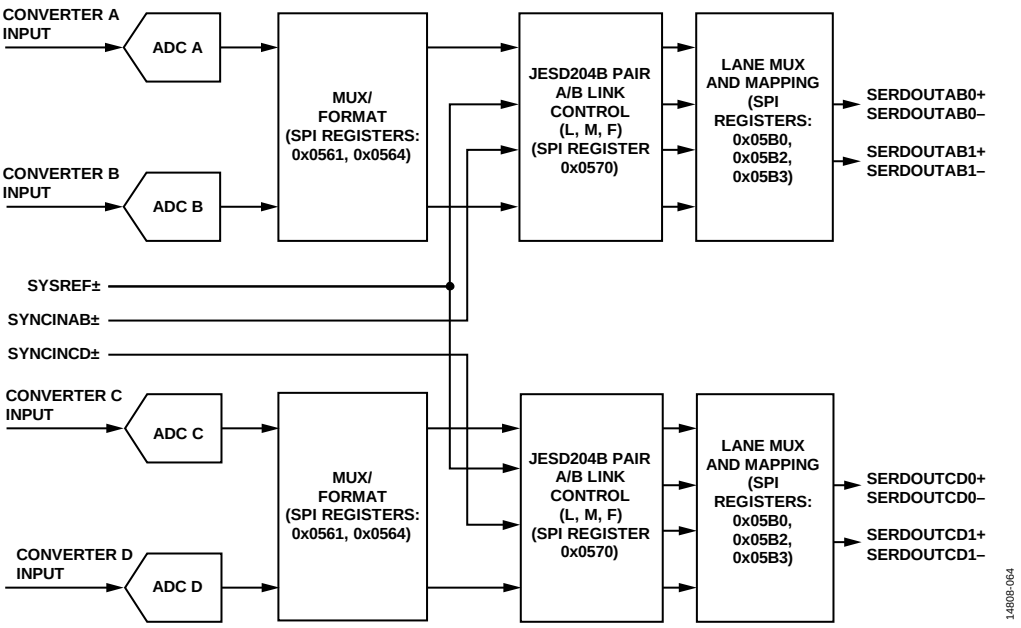

Figure 81. Transmit Link Simplified Block Diagram Showing Full Bandwidth Mode (Register 0x0200 = 0x00)

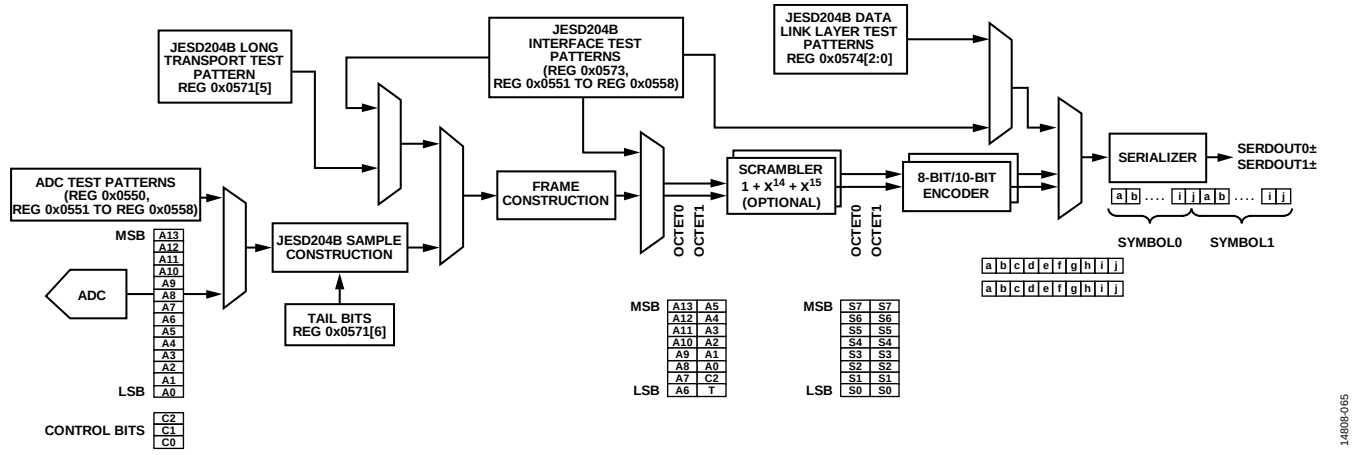

Figure 82. ADC Output Data Path Showing Data Framing

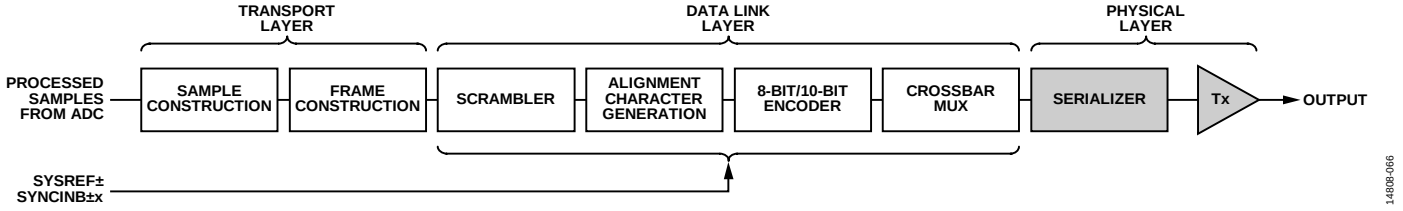

Figure 83. Data Flow

FUNCTIONAL OVERVIEW

The block diagram in Figure 83 shows the flow of data through each of the two JESD204B links from the sample input to the physical output. The processing can be divided into layers that are derived from the open source initiative (OSI) model widely used to describe the abstraction layers of communications systems. These layers are the transport layer, data link layer, and physical layer (serializer and output driver).

Transport Layer

The transport layer handles packing the data (consisting of samples and optional control bits) into JESD204B frames that are mapped to 8-bit octets. These octets are sent to the data link layer. The transport layer mapping is controlled by rules derived from the link parameters. Tail bits are added to fill gaps where required. Use the following equation to determine the number of tail bits within a sample (JESD204B word):

$$T = N' - N - CS$$

Data Link Layer

The data link layer is responsible for the low level functions of passing data across the link. These functions include optionally scrambling the data, inserting control characters for multichip synchronization, lane alignment, or monitoring, and encoding 8-bit octets into 10-bit symbols. The data link layer is also responsible for sending the initial lane alignment sequence (ILAS), which contains the link configuration data used by the receiver to verify the settings in the transport layer.

Physical Layer (PHY)

The physical layer consists of the high speed circuitry clocked at the serial clock rate. In this layer, parallel data is converted into one, two, or four lanes of high speed differential serial data.

JESD204B LINK ESTABLISHMENT

The AD9694 JESD204B transmitter (Tx) interface operates in Subclass 1 as defined in the JEDEC Standard 204B (July 2011 specification). The link establishment process is divided into the following steps: code group synchronization and SYNCINB±AB/ SYNCINB±CD, initial lane alignment sequence, and user data and error correction.

Code Group Synchronization (CGS) and SYNCINB±x

The CGS is the process by which the JESD204B receiver finds the boundaries between the 10-bit symbols in the stream of data. During the CGS phase, the JESD204B transmit block transmits /K28.5/ characters. The receiver must locate /K28.5/ characters in its input data stream using clock and data recovery (CDR) techniques.

The receiver issues a synchronization request by asserting the SYNCINB±AB and SYNCINB±CD pins of the AD9694 low. The JESD204B Tx then begins sending /K/ characters. After the receiver synchronizes, it waits for the correct reception of at least four consecutive /K/ symbols. It then deasserts SYNCINB±AB and SYNCINB±CD. The AD9694 then transmits an ILAS on the following local multiframe clock (LMFC) boundary.

For more information on the code group synchronization phase, refer to the JEDEC Standard JESD204B, July 2011, Section 5.3.3.1.

The SYNCINB±AB and SYNCINB±CD pin operation can also be controlled by the SPI. The SYNCINB±AB and SYNCINB±CD signals are differential LVDS mode signals by default, but can also be driven single-ended. For more information on configuring the SYNCINB±AB and SYNCINB±CD pin operation, refer to Register 0x0572.

Initial Lane Alignment Sequence (ILAS)

The ILAS phase follows the CGS phase and begins on the next LMFC boundary. The ILAS consists of four multiframes, with an /R/ character marking the beginning and an /A/ character marking the end. The ILAS begins by sending an /R/ character followed by 0 to 255 ramp data for one multiframe. On the second multiframe, the link configuration data is sent, starting with the third character. The second character is a /Q/ character to confirm that the link configuration data follows. All undefined data slots are filled with ramp data. The ILAS sequence is never scrambled.

The ILAS sequence construction is shown in Figure 84. The four multiframes include the following:

- Multiframe 1. Begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 2. Begins with an /R/ character followed by a /Q/ (/K28.4/) character, followed by link configuration parameters over 14 configuration octets (see Table 25) and ends with an /A/ character. Many of the parameter values are of the value − 1 notation.
- Multiframe 3. Begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 4. Begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).

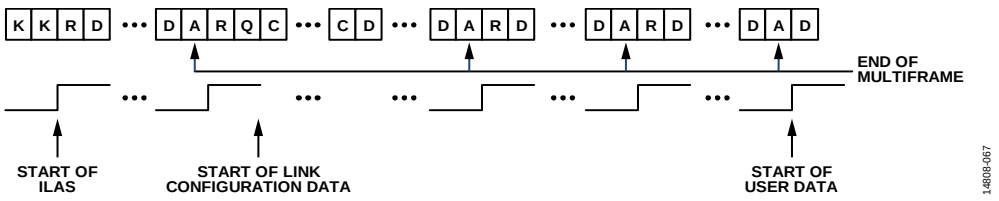

Figure 84. Initial Lane Alignment Sequence

User Data and Error Detection

After the initial lane alignment sequence is complete, the user data is sent. Normally, within a frame, all characters are considered user data. However, to monitor the frame clock and multiframe clock synchronization, there is a mechanism for replacing characters with /F/ or /A/ alignment characters when the data meets certain conditions. These conditions are different for unscrambled and scrambled data. The scrambling operation is enabled by default, but it may be disabled using the SPI.

For scrambled data, any 0xFC character at the end of a frame is replaced by an /F/, and any 0xFD character at the end of a multiframe is replaced with an /A/. The JESD204B receiver (Rx) checks for /F/ and /A/ characters in the received data stream and verifies that they only occur in the expected locations. If an unexpected /F/ or /A/ character is found, the receiver handles the situation by using dynamic realignment or asserting the SYNCINB±x signal for more than four frames to initiate a resynchronization. For unscrambled data, if the final character of two subsequent frames are equal, the second character is replaced with an /F/ if it is at the end of a frame, and an /A/ if it is at the end of a multiframe.

Insertion of alignment characters can be modified using the SPI. The frame alignment character insertion (FACI) is enabled by default. More information on the link controls is available in the Memory Map section, Register 0x0571.

8-Bit/10-Bit Encoder

The 8-bit/10-bit encoder converts 8-bit octets into 10-bit symbols and inserts control characters into the stream when needed. The control characters used in JESD204B are shown in Table 25. The 8-bit/10-bit encoding ensures that the signal is dc balanced by using the same number of ones and zeros across multiple symbols.

The 8-bit/10-bit interface has options that can be controlled via the SPI. These operations include bypass and invert. These options are intended to be troubleshooting tools for the verification of the digital front end (DFE). Refer to the Memory Map section, Register 0x0572, Bits[2:1] for information on configuring the 8-bit/10-bit encoder.

PHYSICAL LAYER (DRIVER) OUTPUTS

Digital Outputs, Timing, and Controls

The AD9694 physical layer consists of drivers that are defined in the JEDEC Standard JESD204B, July 2011. The differential digital outputs are powered up by default. The drivers use a dynamic 100 Ω internal termination to reduce unwanted reflections.

Place a 100 Ω differential termination resistor at each receiver input to result in a nominal 300 mV p-p swing at the receiver (see Figure 85). Alternatively, single-ended 50 Ω termination can be used. When single-ended termination is used, the termination voltage is DRVDD1/2. Otherwise, 0.1 µF ac coupling capacitors can be used to terminate to any single-ended voltage.

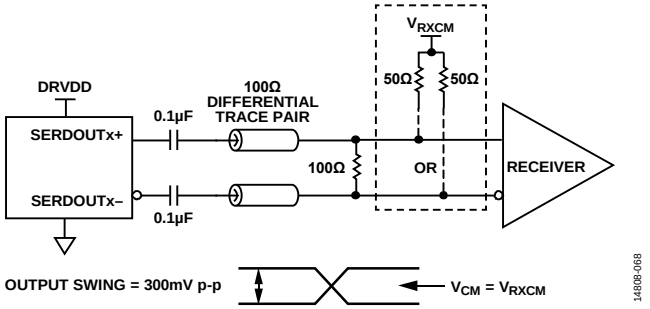

Figure 85. AC-Coupled Digital Output Termination Example

The AD9694 digital outputs can interface with custom ASICs and FPGA receivers, providing superior switching performance in noisy environments. Single point to point network topologies are recommended with a single differential 100 Ω termination resistor placed as close to the receiver inputs as possible. The common mode of the digital output automatically biases itself to half the DRVDD1 supply of 1.25 V (V_{CM} = 0.6 V). See Figure 86 for dc coupling the outputs to the receiver logic.

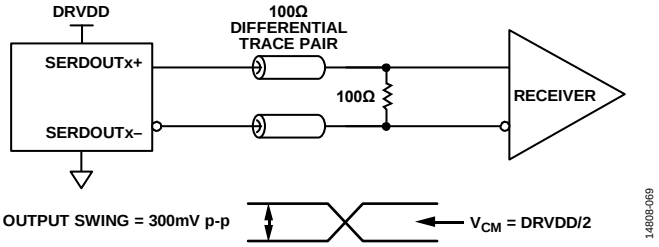

Figure 86. DC-Coupled Digital Output Termination Example

Table 25. AD9694 Control Characters Used in JESD204B

Abbreviation	Control Symbol	8-Bit Value	10-Bit Value, RD[1] = −1	10-Bit Value, RD[1] = +1	Description
/R/	/K28.0/	000 11100	001111 0100	110000 1011	Start of multiframe
/A/	/K28.3/	011 11100	001111 0011	110000 1100	Lane alignment
/Q/	/K28.4/	100 11100	001111 0100	110000 1101	Start of link configuration data
/K/	/K28.5/	101 11100	001111 1010	110000 0101	Group synchronization
/F/	/K28.7/	111 11100	001111 1000	110000 0111	Frame alignment

[1] RD means running disparity.

If there is no far end receiver termination, or if there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than six inches, and that the differential output traces be close together and at equal lengths.

Figure 87 through Figure 89 show examples of the digital output data eye, time interval error (TIE) jitter histogram, and bathtub curve for one AD9694 lane running at 15 Gbps. The format of the output data is twos complement by default. To change the output data format, see the Memory Map section (Register 0x0561 in Table 39).

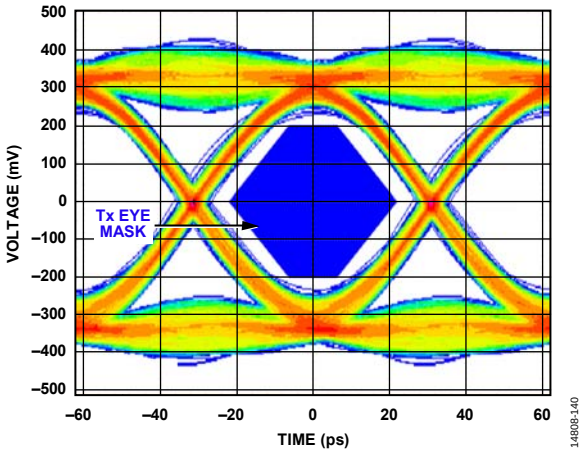

Figure 87. Digital Outputs Data Eye Diagram; External 100 Ω Terminations at 15 Gbps

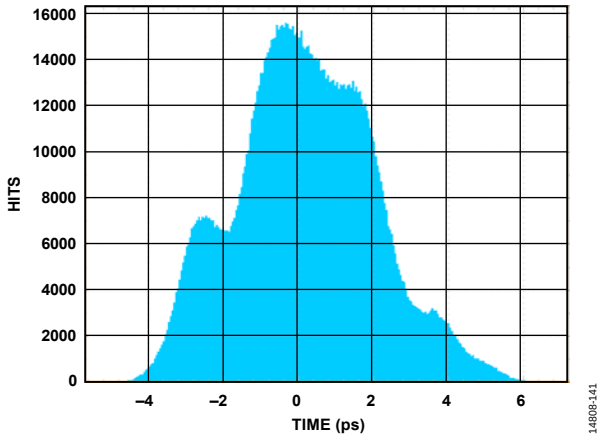

Figure 88. Digital Outputs Histogram; External 100 Ω Terminations at 15 Gbps

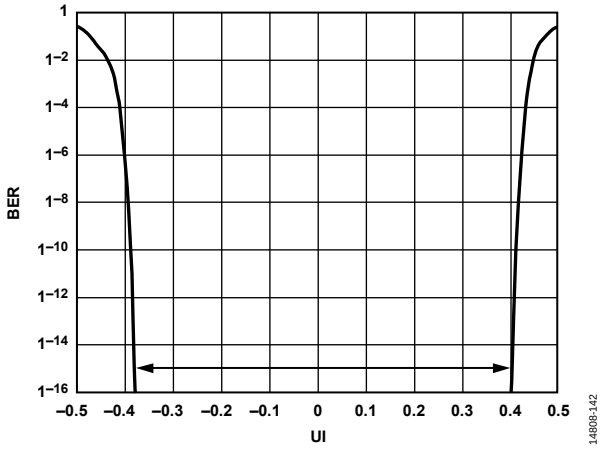

Figure 89. Digital Outputs Bathtub Curve; External 100 Ω Terminations at 15 Gbps

De-Emphasis

De-emphasis enables the receiver eye diagram mask to be met in conditions where the interconnect insertion loss does not meet the JESD204B specification. Use the de-emphasis feature only when the receiver is unable to recover the clock due to excessive insertion loss. Under normal conditions, it is disabled to conserve power. Additionally, enabling and setting too high a de-emphasis value on a short link can cause the receiver eye diagram to fail. Use the de-emphasis setting with caution because it may increase electromagnetic interference (EMI). See the Memory Map section (Register 0x05C4 and Register 0x05C6 in Table 39) for more details.

Phase-Locked Loop (PLL)

The PLL generates the serializer clock, which operates at the JESD204B lane rate. The status of the PLL lock can be checked in the PLL lock status bit (Register 0x056F, Bit 7). This read only bit alerts the user when the PLL has achieved a lock for the specific setup. The JESD204B lane rate control bits, Bits[7:4] of Register 0x056E, must be set to correspond with the lane rate.

JESD204B Tx CONVERTER MAPPING

To support the different chip operating modes, the AD9694 design treats each sample stream (real or I/Q) as originating from separate virtual converters. The I/Q samples are always mapped in pairs with the I samples mapped to the first virtual converter and the Q samples mapped to the second virtual converter. With this transport layer mapping, the number of virtual converters are the same whether a single real converter is used along with a digital downconverter block producing I/Q outputs, or an analog downconversion is used with two real converters producing I/Q outputs.

Figure 90 shows a block diagram of the two scenarios described for I/Q transport layer mapping.

The JESD204B Tx block for AD9694 supports up to four DDC blocks. Each DDC block outputs either two sample streams (I/Q) for the complex data components (real + imaginary), or one sample stream for real (I) data. The JESD204B interface can be configured to use up to eight virtual converters depending on the DDC configuration. Figure 91 shows the virtual converters and their relationship to the DDC outputs when complex outputs are used. Table 26 shows the virtual converter mapping for each chip application mode when channel swapping is disabled.

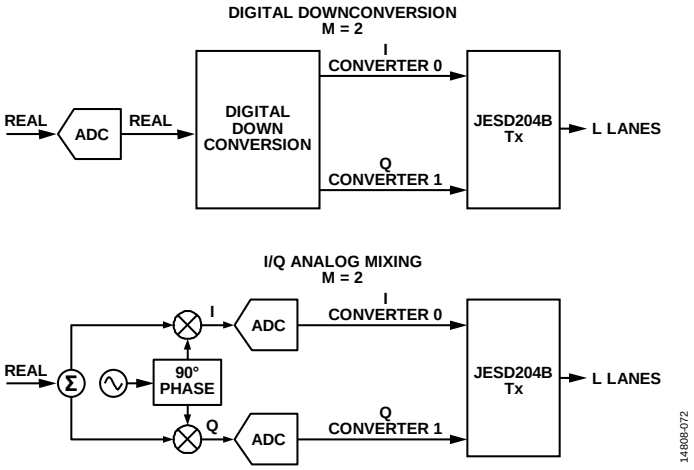

Figure 90. I/Q Transport Layer Mapping

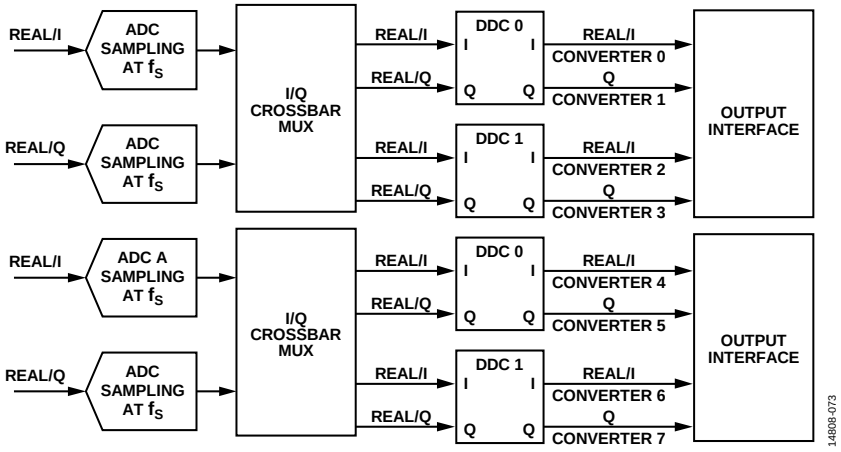

Figure 91. DDCs and Virtual Converter Mapping

CONFIGURING THE JESD204B LINK

The AD9694 has two JESD204B links. The device offers an easy way to set up the JESD204B link through the JESD204B JTX quick configuration register (Register 0x570). One link consists of the SERDOUTAB0± and SERDOUTAB1± serial outputs and the second link consists of the SERDOUTCD0± and SERDOUTCD1± serial outputs. The basic parameters that determine the link setup are

- Number of lanes per link (L)
- Number of converters per link (M)
- Number of octets per frame (F)

If the internal DDCs are used for on-chip digital processing, M represents the number of virtual converters. The virtual converter mapping setup is shown in Figure 91.

The maximum lane rate allowed by the JESD204B specification is 15 Gbps. The lane line rate is related to the JESD204B parameters using the following equation:

$$Lane\ Line\ Rate = \frac{M \times N' \times \left(\frac{10}{8}\right) \times f_{OUT}}{L}$$

where:

$$f_{OUT} = \frac{f_{ADC\_CLOCK}}{Decimation\ Ratio}$$

The decimation ratio (DCM) is the parameter programmed in Register 0x0201.

Use the following steps to configure the output:

1. Power down the link.
2. Select the quick configuration options.
3. Configure any detailed options.
4. Set the output lane mapping (optional).
5. Set additional driver configuration options (optional).
6. Power up the link.

If the lane line rate calculated is less than 6.75 Gbps, select the low line rate option by programming a value of 0x10 to Register 0x056E.

Table 27 and Table 28 show the JESD204B output configurations supported for both N′ = 16 and N′ = 8 for a given number of virtual converters. Take care to ensure that the serial line rate for a given configuration is within the supported range of 1.6875 Gbps to 15 Gbps.

See the Example 1: Full Bandwidth Mode section and the Example 2: ADC with DDC Option (Two ADCs Plus Two DDCs in Each Pair) section for two examples describing which JESD204B transport layer settings are valid for a given chip mode.

Table 26. Virtual Converter Mapping (Per Link)

Number of Virtual Converters Supported	Chip Application Mode (Register 0x0200, Bits[3:0])	Chip Q Ignore (Register 0x0200, Bit 5)	Virtual Converter Mapping			
			0	1	2	3
1 to 2	Full bandwidth mode (0x0)	Real or complex (0x0)	ADC A/ADC C samples	ADC B/ADC D samples	Unused	Unused
1	One DDC mode (0x1)	Real (I only) (0x1)	DDC 0 I samples	Unused	Unused	Unused
2	One DDC mode (0x1)	Complex (I/Q) (0x0)	DDC 0 I samples	DDC 0 Q samples	Unused	Unused
2	Two DDC mode (0x2)	Real (I only) (0x1)	DDC 0 I samples	DDC 1 I samples	Unused	Unused
4	Two DDC mode (0x2)	Complex (I/Q) (0x0)	DDC 0 I samples	DDC 0 Q samples	DDC 1 I samples	DDC 1 Q samples

Table 27. JESD204B Output Configurations for N′ = 16 (Per Link)

Number of Virtual Converters Supported (Same Value as M)	JESD204B JTX Quick Configuration (Register 0x0570)	JESD204B Serial Lane Rate[1]	JESD204B Transport Layer Settings[2]								
			L	M	F	S	HD	N	N′	CS	K[3]
1	0x01	20 × f_{OUT}	1	1	2	1	0	8 to 16	16	0 to 3	Only valid K values that are divisible by 4 are supported
	0x40	10 × f_{OUT}	2	1	1	1	1	8 to 16	16	0 to 3	
	0x41	10 × f_{OUT}	2	1	2	2	0	8 to 16	16	0 to 3	
2	0x0A	40 × f_{OUT}	1	2	4	1	0	8 to 16	16	0 to 3	
	0x49	20 × f_{OUT}	2	2	2	1	0	8 to 16	16	0 to 3	
4	0x13	80 × f_{OUT}	1	4	8	1	0	8 to 16	16	0 to 3	
	0x52	40 × f_{OUT}	2	4	4	1	0	8 to 16	16	0 to 3	

[1] f_{OUT} (output sample rate) is the ADC sample rate/chip decimation ratio. The JESD204B serial line rate must be ≥1687.5 Mbps and ≤15,000 Mbps. When the serial lane rate is ≤15 Gbps and >13.5 Gbps, set Bits[7:4] to 0x3 in Register 0x056E. When the serial lane rate is ≤13.5 Gbps and > 6.75 Gbps, set Bits[7:4] to 0x0 in Register 0x056E. When the serial lane rate is ≤ 6.75 Gbps and >3.375 Gbps, set Bits[7:4] to 0x1 in Register 0x056E. When the serial lane rate is ≤3.375 Gbps and ≥1687.5 Mbps, set Bits[7:4] to 0x5 in Register 0x056E.
[2] JESD204B transport layer descriptions are as described in the Setting Up the AD9694 Digital Interface section.
[3] For F = 1, K = 20, 24, 28, and 32. For F = 2, K = 12, 16, 20, 24, 28, and 32. For F = 4, K = 8, 12, 16, 20, 24, 28, and 32. For F = 8 and F = 16, K = 4, 8, 12, 16, 20, 24, 28, and 32.

Table 28. JESD204B Output Configurations for N′ = 8 (Per Link)

Number of Virtual Converters Supported (Same Value as M)	JESD204B Quick Configuration (Register 0x0570)	Serial Lane Rate[1]	JESD204B Transport Layer Settings[2]								
			L	M	F	S	HD	N	N′	CS	K[3]
1	0x00	10 × f_{OUT}	1	1	1	1	0	7 to 8	8	0 to 1	Only valid K values which are divisible by 4 are supported
	0x01	10 × f_{OUT}	1	1	2	2	0	7 to 8	8	0 to 1	
	0x40	5 × f_{OUT}	2	1	1	2	0	7 to 8	8	0 to 1	
	0x41	5 × f_{OUT}	2	1	2	4	0	7 to 8	8	0 to 1	
	0x42	5 × f_{OUT}	2	1	4	8	0	7 to 8	8	0 to 1	
2	0x09	20 × f_{OUT}	1	2	2	1	0	7 to 8	8	0 to 1	
	0x48	10 × f_{OUT}	2	2	1	1	0	7 to 8	8	0 to 1	
	0x49	10 × f_{OUT}	2	2	2	2	0	7 to 8	8	0 to 1	

[1] f_{OUT} = output sample rate is the ADC sample rate/chip decimation ratio. The JESD204B serial line rate must be ≥1687.5 Mbps and ≤15,000 Mbps. When the serial lane rate is ≤15 Gbps and >13.5 Gbps, set Bits[7:4] to 0x3 in Register 0x056E. When the serial lane rate is ≤13.5 Gbps and > 6.75 Gbps, set Bits[7:4] to 0x0 in Register 0x056E. When the serial lane rate is ≤6.75 Gbps and >3.375 Gbps, set Bits[7:4] to 0x1 in Register 0x056E. When the serial lane rate is ≤3.375 Gbps and ≥1687.5 Mbps, set Bits[7:4] to 0x5 in Register 0x056E.
[2] JESD204B transport layer descriptions are as described in the Setting Up the AD9694 Digital Interface section.
[3] For F = 1, K = 20, 24, 28, and 32. For F = 2, K = 12, 16, 20, 24, 28, and 32. For F = 4, K = 8, 12, 16, 20, 24, 28, and 32. For F = 8 and F = 16, K = 4, 8, 12, 16, 20, 24, 28, and 32.

Example 1: Full Bandwidth Mode

In this example, the chip application mode is full bandwidth mode (see Figure 92), as follows:

- Two 14-bit converters at 500 MSPS
- Full bandwidth application layer mode
- No decimation

The JESD204B output configuration is as follows:

- Two virtual converters required (see Table 27)
- Output sample rate (f_{OUT}) = 500/1 = 500 MSPS

The JESD204B supported output configurations (see Table 27) include the following:

- N′ = 16 bits
- N = 16 bits
- L = 2, M = 2, and F = 2 (quick configuration = 0x48)
- CS = 0 to 2
- K = 32
- Output serial line rate = 10 Gbps per lane

Example 2: ADC with DDC Option (Two ADCs Plus Two DDCs in Each Pair)

In this example, the chip application mode is two-DDC mode. (see Figure 93), as follows:

- Two 14-bit converters at 500 MSPS
- Two DDC application layer mode with complex outputs (I/Q)
- Chip decimation ratio = 4
- DDC decimation ratio = 4 (see Table 27)

The JESD204B output configuration is as follows:

- Virtual converters required = 4 (see Table 27)
- Output sample rate (f_{OUT}) = 500/4 = 125 MSPS
- N′ = 16 bits
- N = 14 bits
- L = 1, M = 4, and F = 8 (quick configuration = 0x13)
- CS = 0 to 1
- K = 32
- Output serial line rate = 10 Gbps per lane (L = 1) or 5 Gbps per lane (L = 2)

For L = 1, set Register 0x056E, Bits[7:4] to 0x1. For L = 2, set Register 0x056E, Bits[7:4] to 0x5.

Example 2 shows the flexibility in the digital and lane configurations for the AD9694. The sample rate is 500 MSPS, but the outputs are all combined in either one or two lanes, depending on the input/output speed capability of the receiving device.

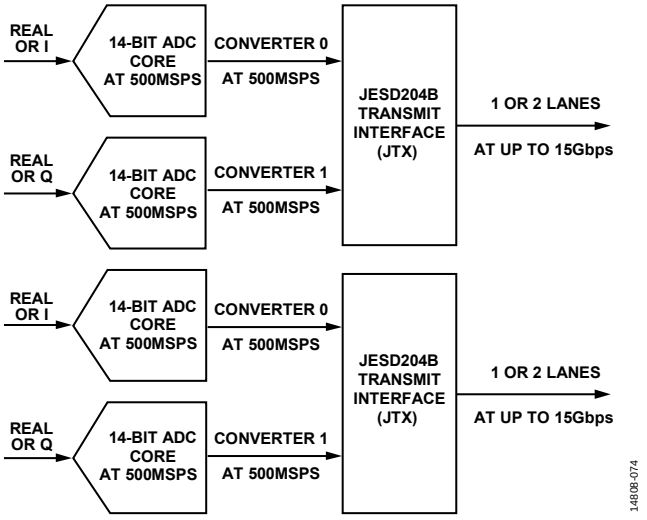

Figure 92. Full Bandwidth Mode

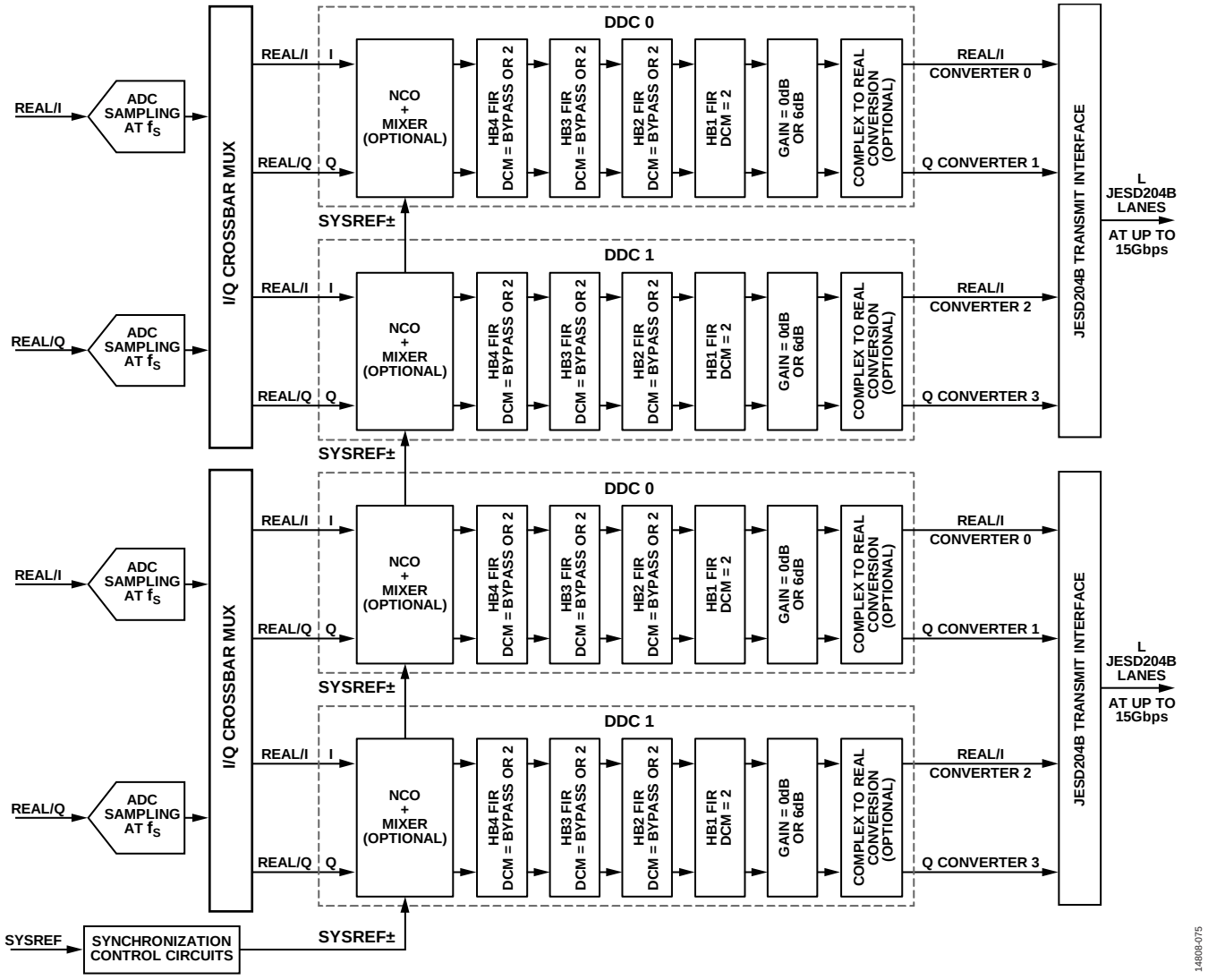

Figure 93. Two ADCs Plus Two DDCs Mode in Each Pair

LATENCY

END TO END TOTAL LATENCY

Total latency in the AD9694 is dependent on the chip application mode and the JESD204B configuration. For any given combination of these parameters, the latency is deterministic, however, the value of this deterministic latency must be calculated as described in the Example Latency Calculations section.

Table 29 shows the combined latency through the ADC and DSP for the different chip application modes supported by the AD9694. Table 30 shows the latency through the JESD204B block for each application mode based on the M/L ratio. For both Table 29 and Table 30, latency is typical and is in units of the encode clock. The latency through the JESD204B block does not depend on the output data type (real or complex). Therefore, data type is not included in Table 30.

To determine the total latency, select the appropriate ADC + DSP latency from Table 29 and add it to the appropriate JESD204B latency from Table 30. Example calculations are provided in the following section.

EXAMPLE LATENCY CALCULATIONS

Example Configuration 1

In this example, the ADC application mode is full bandwidth with the following conditions:

- Real outputs
- L = 4, M = 2, F = 1, S = 1 (JESD204B mode)
- M/L ratio = 0.5

Latency = 31 + 25 = 56 encode clocks

Example Configuration 2

In this example, the ADC application mode is decimate by 4, DCM4, with the following conditions:

- Complex outputs
- L = 4, M = 2, F = 1, S = 1 (JESD204B mode)
- M/L ratio = 0.5

Latency = 162 + 88 = 250 encode clocks

LMFC REFERENCED LATENCY

Some FPGA vendors may require the end user to know the LMFC referenced latency to make the appropriate deterministic latency adjustments. If they are required, the latency values in Table 29 and Table 30 can be used for the analog input to LMFC latency value and the LMFC to data output latency value.

Table 29. Latency Through the ADC + DSP Blocks (Number of Sample Clocks)

Chip Application Mode[1]	Enabled Filters	ADC and DSP Latency
Full Bandwidth	Not applicable	31
DCM1 (real) DCM2 (complex)	HB1	94
DCM2 (real) DCM4 (complex)	HB2 + HB1	162
DCM4-real DCM8 (complex)	HB3 +HB2 + HB1	292
DCM8 (real) DCM16 (complex)	HB4 + HB3 + HB2 + HB1	548

[1] DCMx indicates the decimation ratio.

Table 30. Latency Through JESD204B Block (Number of Sample Clocks)

	M/L Ratio[1, 2]				
Chip App Mode	**0.5**	**1**	**2**	**4**	**8**
Full BW	25	14	7	4	2
DCM1	25	14	7	N/A	N/A
DCM2	46	27	14	7	N/A
DCM4	88	50	27	14	7
DCM8	172	96	50	27	14
DCM16	339[3, 4]	188[3]	96[3]	50[d]	27[3]

[1] M/L ratio is the number of converters divided by the number of lanes for the configuration.
[2] N/A means not applicable, indicating the application mode is not supported at the M/L ratio listed.
[3] Indicates the application mode at the M/L ratio listed is only supported in complex output mode.
[4] Indicates the application mode at the M/L ratio listed is only supported in real output mode.

DETERMINISTIC LATENCY

Both ends of the JESD204B link contain various clock domains distributed throughout each system. Data traversing from one clock domain to a different clock domain can lead to ambiguous delays in the JESD204B link. These ambiguities lead to nonrepeatable latencies across the link from one power cycle or link reset to the next. Section 6 of the JESD204B specification addresses the issue of deterministic latency with mechanisms defined as Subclass 1 and Subclass 2.

The AD9694 supports JESD204B Subclass 0 and Subclass 1 operation. Register 0x0590, Bits[7:5] set the subclass mode for the AD9694 and its default is set for Subclass 1 operating mode (Register 0x590, Bits[7:5] = 001. If deterministic latency is not a system requirement, Subclass 0 operation is recommended and the SYSREF± signal may not be required. Even in Subclass 0 mode, the SYSREF± signal may be required in an application where multiple AD9694 devices need to be synchronized with each other (for more information, see the Timestamp Mode section).

SUBCLASS 0 OPERATION

If there is no requirement for multichip synchronization while operating in Subclass 0 mode (Register 0x590, Bits[7:5] = 000), the SYSREF± input can be left disconnected. In this mode, the relationship of the JESD204B clocks between the JESD204B transmitter and receiver are arbitrary but does not affect the ability of the receiver to capture and align the lanes within the link.

SUBCLASS 1 OPERATION

The JESD204B protocol organizes data samples into octets, frames and multiframes, as described in the Transport Layer section. The LMFC is synchronous with the beginnings of these multiframes. In Subclass 1 operation, the SYSREF± signal is used to synchronize the LMFCs for each device in a link or across multiple links (within the AD9694, SYSREF± also synchronizes the internal sample dividers); see Figure 94. The JESD204B receiver uses the multiframe boundaries and buffering to achieve consistent latency across lanes (or even multiple devices), and to achieve a fixed latency between power cycles and link reset conditions.

Deterministic Latency Requirements

Several key factors are required for achieving deterministic latency in a JESD204B Subclass 1 system.

- SYSREF± signal distribution skew within the system must be less than the desired uncertainty for the system.
- SYSREF± setup and hold time requirements must be met for each device in the system.
- The total latency variation across all lanes, links and devices must be ≤1 LMFC (t_{LMFC}) period (see Figure 94). This total latency includes both variable delays and the variation in fixed delays from lane to lane, link to link, and device to device in the system.

Setting Deterministic Latency Registers

The JESD204B receive buffer in the logic device buffers data starting on the LMFC boundary. If the total link latency in the system is near an integer multiple of the LMFC period, it is possible that from one power cycle to the next, the data arrival time at the receive buffer may overlap an LMFC boundary. To ensure deterministic latency in this case, a phase adjustment of the LMFC at either the transmitter or receiver must be performed. Typically, adjustments to accommodate the receive buffer are made to the LMFC of the receiver. In the AD9694, this adjustment can be made using the JTX LMFC offset register (Register 0x0578, Bits[4:0]). This register delays the LMFC in frame clock increments, depending on the F parameter (number of octets per lane per frame). For F = 1, every fourth setting (0, 4, 8, …) results in a one-frame clock shift. For F = 2, every other setting (0, 2, 4, …) results in a one-frame clock shift. For all other values of F, each setting results in a one-frame clock shift. Figure 95 shows that, when the link latency is near an LMFC boundary, the local LMFC of the AD9694 can be delayed to delay the data arrival time at the receiver. Figure 96 shows how the LMFC of the receiver is delayed to accommodate the receive buffer timing. Consult the applicable JESD204B receiver user guide for details on making this adjustment.

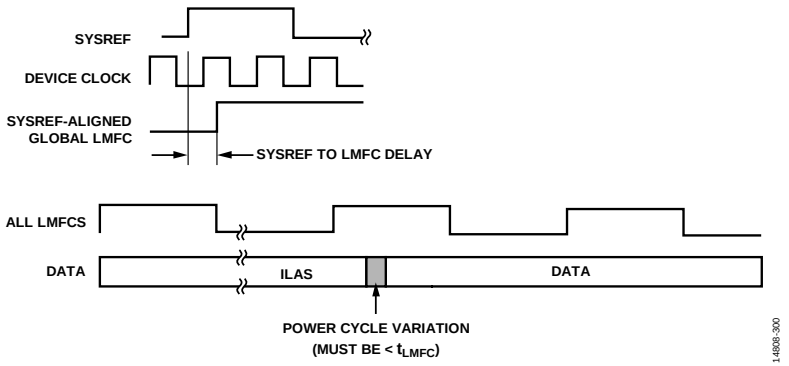

Figure 94. SYSREF and LMFC

If the total latency in the system is not near an integer multiple of the LMFC period or if the appropriate adjustments have been made to the LMFC phase at the clock source, it is still possible to have variable latency from one power cycle to the next. In this case, check whether the setup and hold time requirements for the SYSREF± are not being met, by reading the SYSREF± setup/hold monitor register (Register 0x0128). This function is fully described in the SYSREF± Setup/Hold Window Monitor section.

If reading Register 0x0128 indicates a timing issue, a couple of adjustments can made in the AD9694, as follows:

- Change the SYSREF± level that is used for alignment using the SYSREF± transition select bit (Register 0x0120, Bit 4).
- Change the edge of CLK± that is used to capture SYSREF± using the CLK± edge select bit (Register 0x0120, Bit 3).

Both of these options are described in the SYSREF± Control Features section. If neither of these measures help achieve an acceptable setup and hold time, adjusting the phase of SYSREF± and/or the device clock (CLK±) may be required.

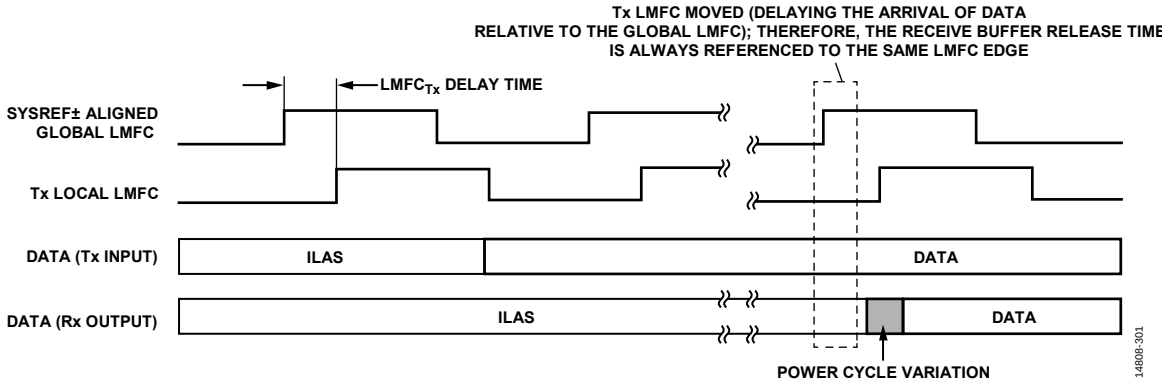

Figure 95. Adjusting the JESD204B Tx LMFC in the AD9694

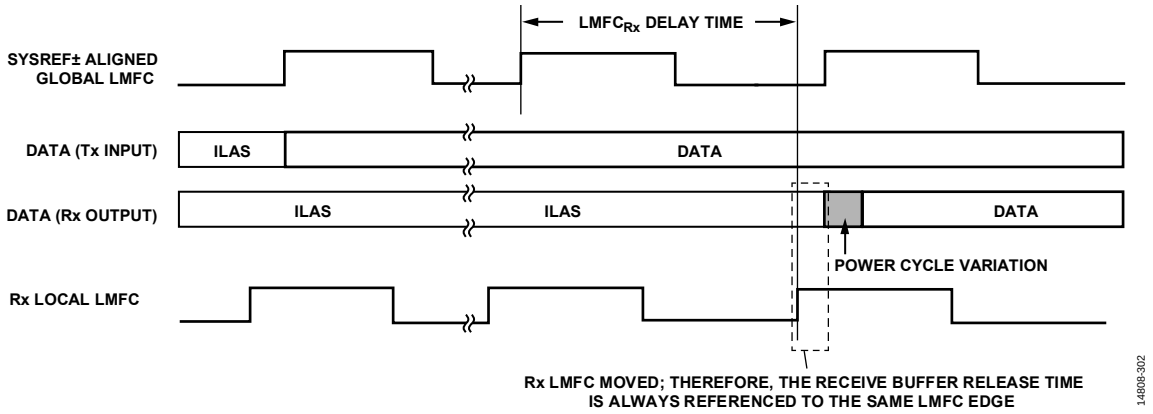

Figure 96. Adjusting the JESD204B Rx LMFC in the Logic Device

MULTICHIP SYNCHRONIZATION

The flowchart in Figure 98 describes the internal mechanism for multichip synchronization in the AD9694. There are two methods by which multichip synchronization can take place as determined by the synchronization mode bit in Register 0x1FF, Bit 0. Each method involves different applications of the SYSREF± signal.

NORMAL MODE

The default state of the synchronization mode bit is 0x0, which configures the AD9694 for sample chip synchronization. The JESD204B standard specifies the use of SYSREF± to provide for deterministic latency within a single link. This same concept, when applied to a system with multiple converters and logic devices, can also provide multichip synchronization. In Figure 98, this synchronization mode is referred to as normal mode. Following the process outlined in Figure 98 ensures that the AD9694 is configured appropriately. Users are recommended to consult the user intellectual property guide of the logic devices to ensure the JESD204B receivers are configured appropriately.

TIMESTAMP MODE

For all AD9694 full bandwidth operating modes, the SYSREF± input can also be used to timestamp samples. Timestamping is another method by which multiple channels and multiple devices can achieve synchronization. This timestamping is especially effective when synchronizing multiple devices to one or more logic devices. The logic devices simply buffer the data streams, identify the timestamped samples, and align them. When the synchronization mode bit (Register 0x01FF, Bit 0) is set to 0x1, the timestamp method is used for synchronization of multiple channels and/or devices. In this mode, SYSREF± resets the sample dividers and the JESD204B clocking. When the synchronization mode is set to 0x1, the clocks are not reset; instead, the coinciding sample is timestamped using JESD204B control bits of that sample. To operate in timestamp mode, the following additional settings are necessary:

- Continuous or N shot SYSREF± enabled (Register 0x0120, Bits[2:1] = 1 or 2 decimal)
- At least one control bit must be enabled (Register 0x58F, Bits[7:6] = 1, 2, or 3 decimal)
- Set the function for one of the control bits to SYSREF±, as follows:
  - Register 0x0559, Bits[2:0] = 5 if using Control Bit 0
  - Register 0x0559, Bits[6:4] = 5 if using Control Bit 1
  - Register 0x055A, Bits[2:0] = 5 if using Control Bit 2

Figure 97 shows how the input sample coincident with SYSREF± is timestamped and ultimately output from the ADC. In this example, there are two control bits and Control Bit 0 indicates which sample was coincident with the SYSREF± rising edge. The pipeline latencies for each channel are identical. If so desired, the SYSREF± timestamp delay register (Register 0x0123) can be used to adjust the timing of the sample that is timestamped.

Time stamping is not supported by any AD9694 operating modes that use decimation.

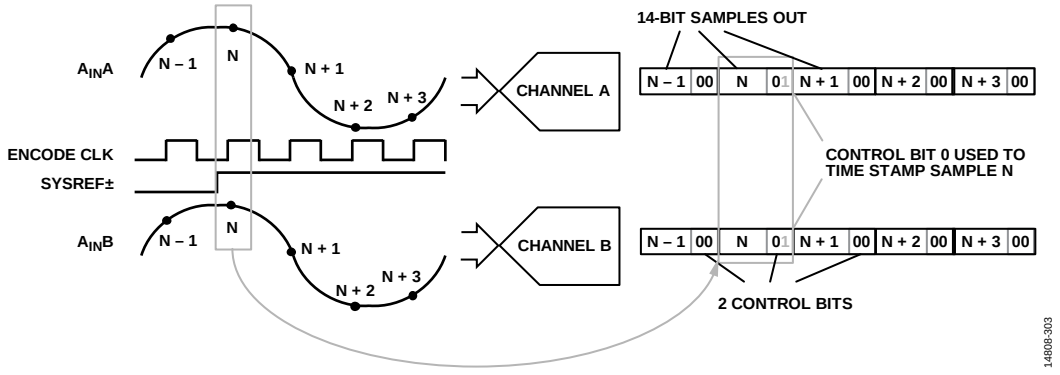

Figure 97. Timestamping—CS = 2 (Register 0x058F, Bits[7:6] = 2 Decimal), Control Bit 0 is SYSREF± (Register 0x0559, Bits[2:0] = 5 Decimal)

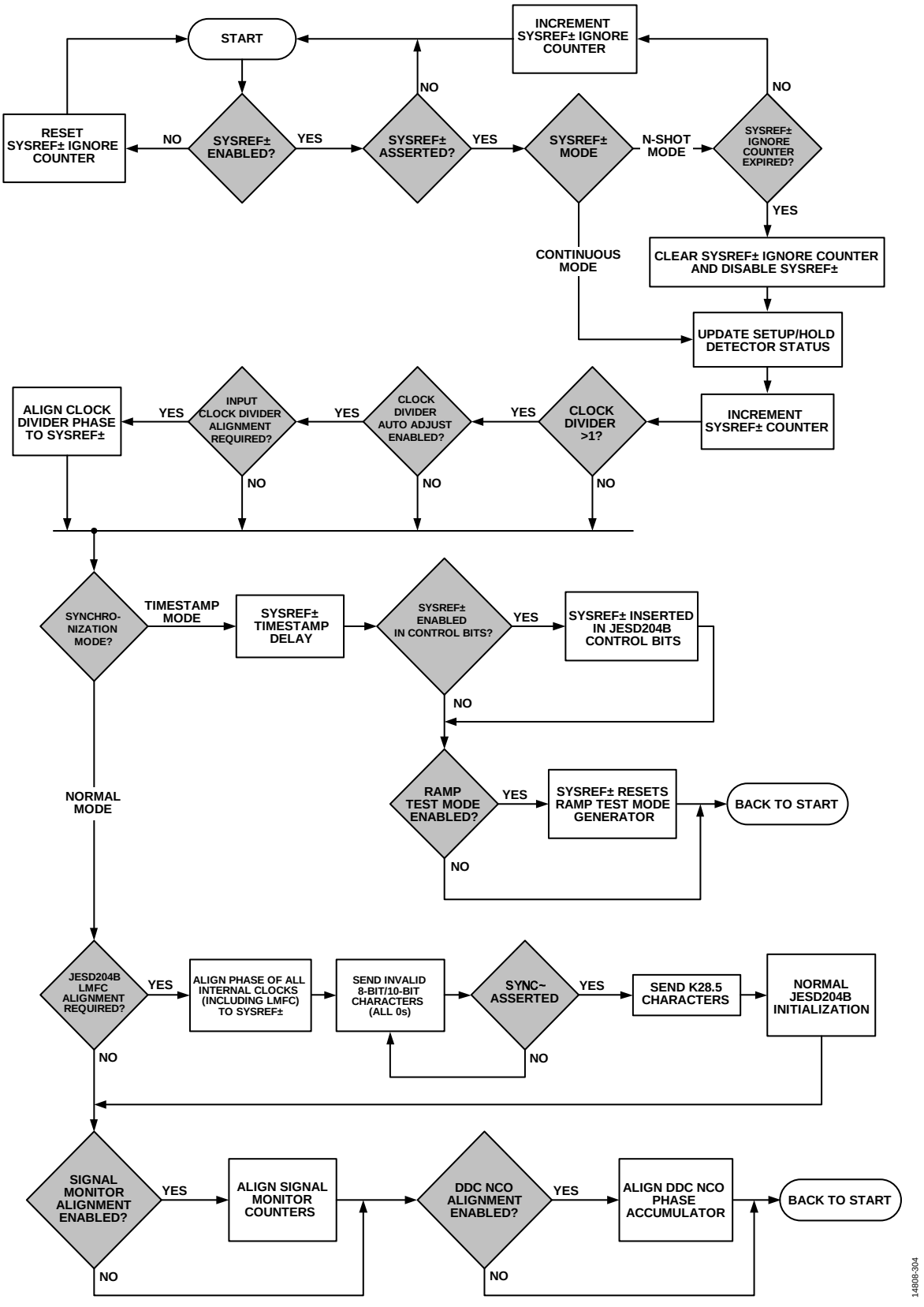

Figure 98. SYSREF± Capture Scenarios and Multichip Synchronization

SYSREF± INPUT

The SYSREF± input signal is used as a high accuracy system reference for deterministic latency and multichip synchronization. The AD9694 accepts a single-shot or periodic input signal. The SYSREF± mode select bits (Register 0x0120, Bits[2:1]) select the input signal type and serves to activate the SYSREF± state machine when set. If in single (or N) shot mode (Register 0x0120, Bits[2:1] = 2 decimal), the SYSREF± mode select bit self clears after the appropriate SYSREF± transition is detected. The pulse width must have a minimum width of two CLK± periods. If the clock divider (Register 0x010B, Bits[2:0]) is set to a value other than divide by 1, multiply this minimum pulse width requirement by the divide ratio (for example, if set to divide by 8, the minimum pulse width is 16 CLK± cycles). When using a continuous SYSREF± signal (Register 0x0120, Bits[2:1] = 1 decimal), the period of the SYSREF± signal must be an integer multiple of the LMFC. LMFC can be derived using the formula:

$$LMFC = ADC\ clock/S \times K$$

where:
S is the JESD204B parameter for the number of samples per converter.
K is the JESD204B parameter for the number of frames per multiframe.

Continuous SYSREF± signal is generally not recommended because the periodic SYSREF± signal may couple with the sampling path, creating spurs in the spectrum.

The input clock divider, DDCs, signal monitor block, and JESD204B link are all synchronized using the SYSREF± input when in sample synchronization mode (normal mode) (Register 0x01FF, Bit 0 = 0x0. The SYSREF± input can also be used to timestamp an ADC sample or provide a mechanism for synchronizing multiple AD9694 devices in a system. For the highest level of timing accuracy, SYSREF± must meet setup and hold requirements relative to the CLK± input. Several features in the AD9694 can be used to ensure these requirements are met. These features are described in the SYSREF± Control Features section.

SYSREF± Control Features

SYSREF± is used, together with the input clock (CLK±), as part of a source synchronous timing interface, and requires setup and hold timing requirements of −44.8 ps and 64.4 ps relative to CLK± (see Figure 99). The AD9694 has three features that aid customers in meeting these requirements.

First, the SYSREF± sample event can be defined as either a synchronous low to high transition or synchronous high to low transition.

Second, the AD9694 allows the SYSREF± signal to be sampled using either the rising edge or falling edge of the input clock. Figure 99, Figure 100, Figure 101 and Figure 102 show all four possible combinations.

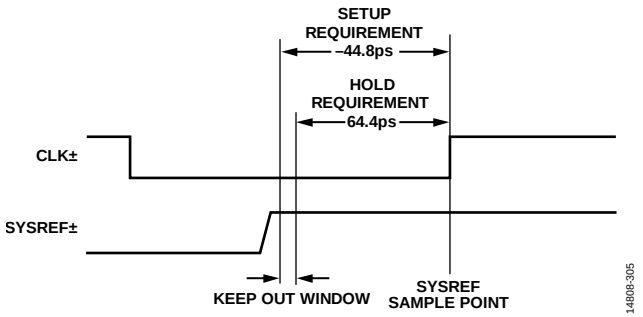

Figure 99. SYSREF± Setup and Hold Time Requirements. SYSREF± Low to High Transition Using Rising Edge Clock (Default)

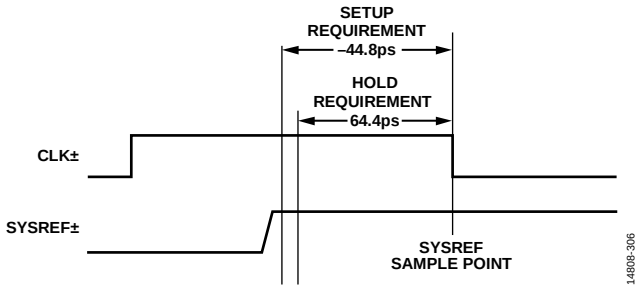

Figure 100. SYSREF± Low to High Transition Using Falling Edge Clock Capture (Register 0x0120, Bit 4 = 1'b0, Register 0x0120, Bit 3 = 1'b1)

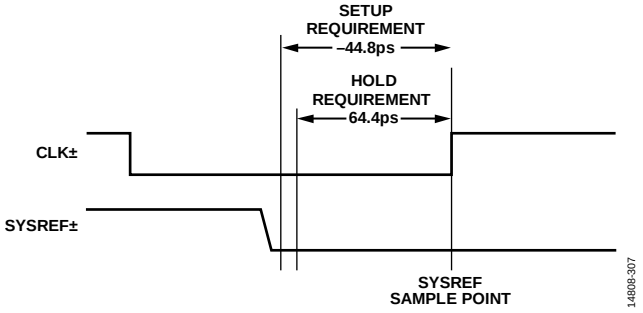

Figure 101. SYSREF± High to Low Transition Using Rising Edge Clock Capture (Register 0x0120, Bit 4 = 1'b1, Register 0x0120, Bit 3 = 1'b0)

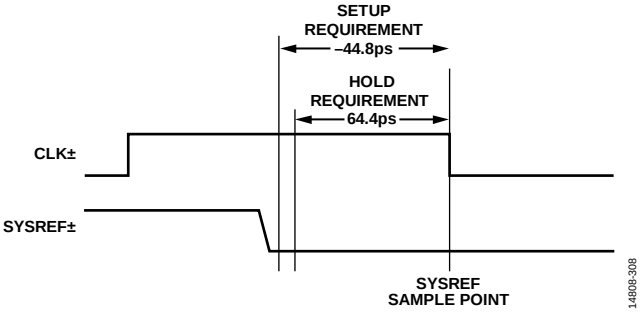

Figure 102. SYSREF± High to Low Transition Using Falling Edge Clock Capture (Register 0x0120, Bit 4 = 1'b1, Register 0x0120, Bit 3 = 1'b1)

Third, the AD9694 has the ability to ignore a programmable number (up to 16) of SYSREF± events (the SYSREF± ignore feature is enabled by setting the SYSREF± mode register (Register 0x0120, Bits[2:1]) to 2'b10, N shot mode). This feature is useful to handle periodic SYSREF± signals that need time to settle after startup. Ignoring SYSREF± until the clocks in the system have settled can avoid an inaccurate SYSREF± trigger. Figure 103 shows an example of the SYSREF± ignore feature when ignoring three SYSREF± events.

SYSREF± SETUP/HOLD WINDOW MONITOR

To ensure a valid SYSREF signal capture, the AD9694 has a SYSREF± setup/hold window monitor. This feature allows the system designer to determine the location of the SYSREF± signals relative to the CLK± signals by reading back the amount of setup/hold margin on the interface through the memory map. Figure 104 and Figure 105 show the setup and hold status values for different phases of SYSREF±. The setup detector returns the status of the SYSREF± signal before the CLK± edge, and the hold detector returns the status of the SYSREF signal after the CLK± edge. Register 0x0128 stores the status of SYSREF± and lets the user know if the SYSREF± signal is captured by the ADC.

Table 31 shows the description of the contents of Register 0x128 and how to interpret them.

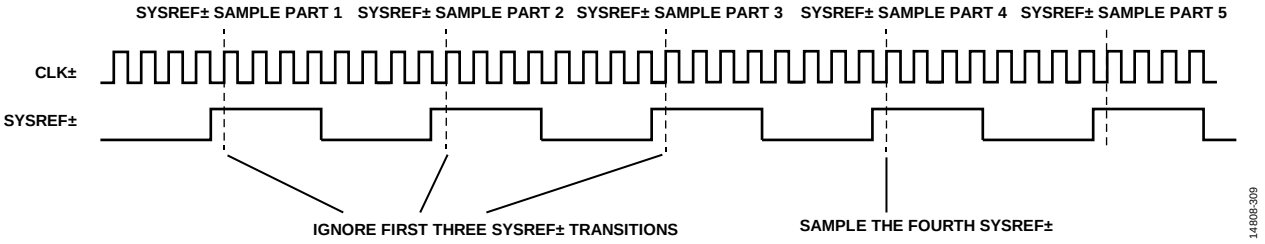

Figure 103. SYSREF± Ignore Example (SYSREF± N Shot Ignore Counter Select, Register 0x0121, Bits[3:0] = 3 Decimal)

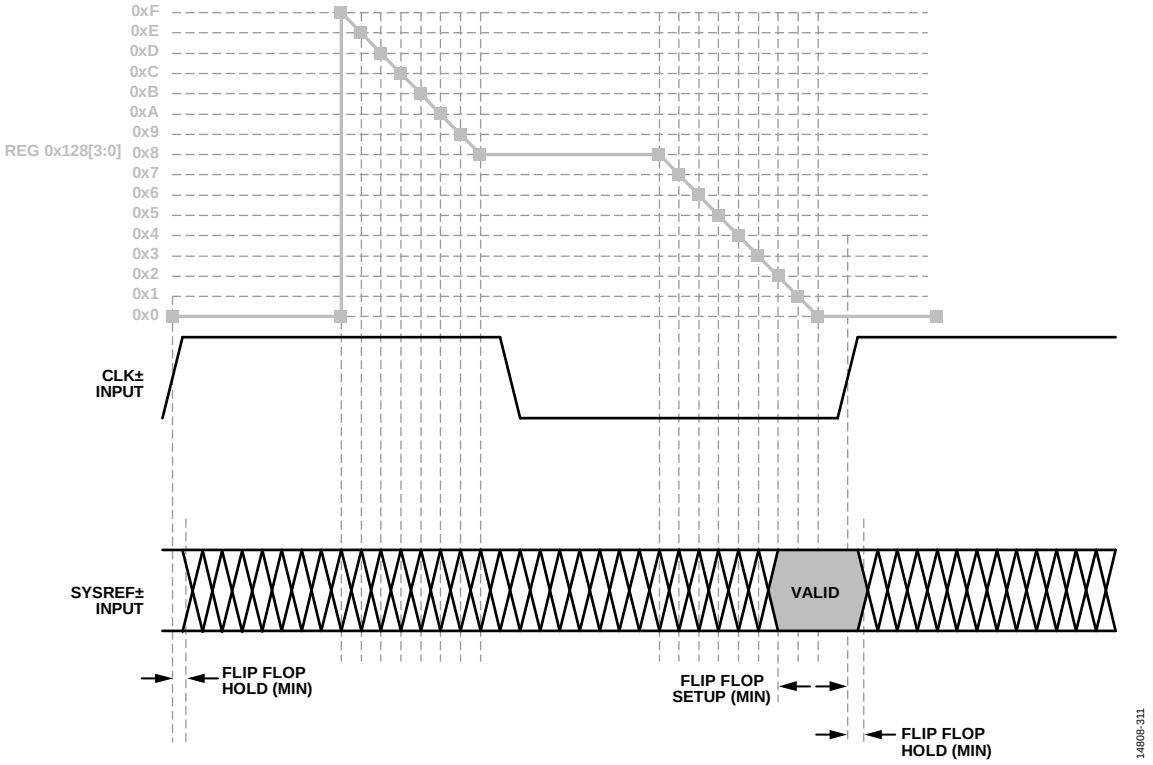

Figure 104. SYSREF± Setup Detector

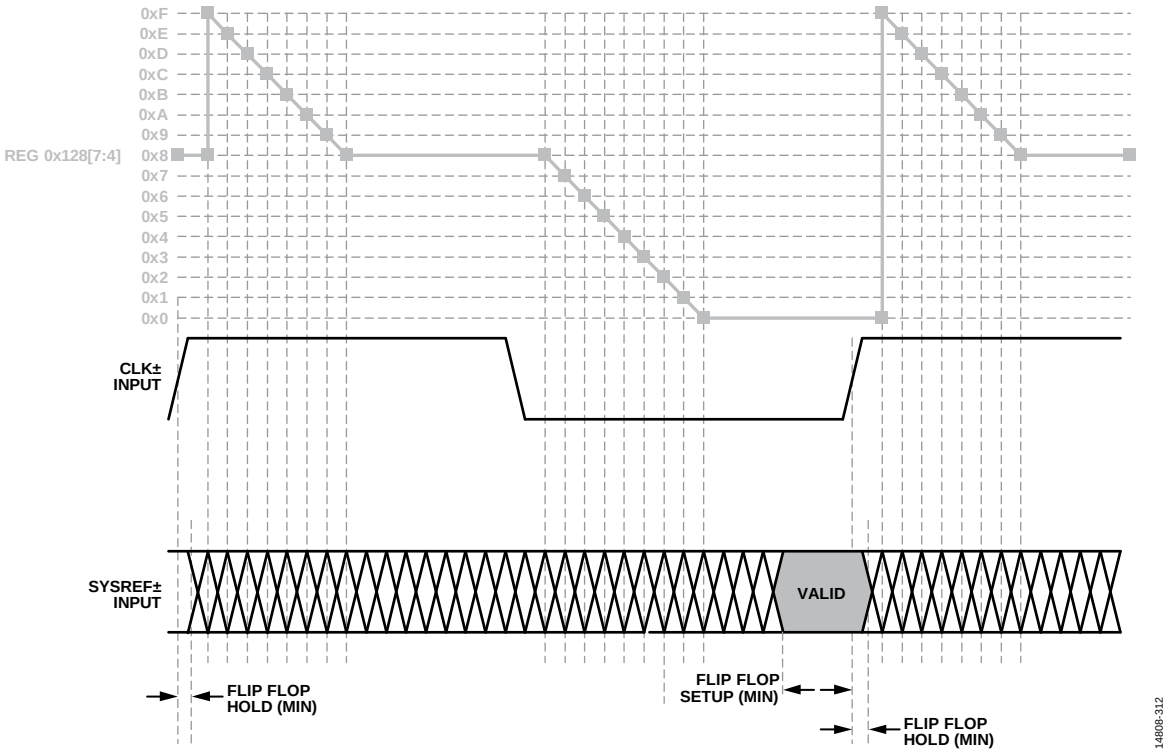

Figure 105. SYSREF± Hold Detector

Table 31. SYSREF± Setup/Hold Monitor, Register 0x0128

Register 0x0128, Bits[7:4] Hold Status	Register 0x0128, Bits[3:0] Setup Status	Description
0x0	0x0 to 0x7	Possible setup error. The smaller this number, the smaller the setup margin.
0x0 to 0x8	0x8	No setup or hold error (best hold margin).
0x8	0x9 to 0xF	No setup or hold error (best setup and hold margin).
0x8	0x0	No setup or hold error (best setup margin).
0x9 to 0xF	0x0	Possible hold error. The larger this number, the smaller the hold margin.
0x0	0x0	Possible setup or hold error.

TEST MODES

ADC TEST MODES

The AD9694 has various test options that aid in the system level implementation. The AD9694 has ADC test modes that are available in Register 0x0550. These test modes are described in Table 32. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks, and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not. The pseudorandom noise (PN) generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x0550. These tests can be performed with or without an analog signal (if present, the analog signal is ignored); however, they do require an encode clock.

If the application mode is set to select a DDC mode of operation, the test modes must be enabled for each DDC enabled. The test patterns can be enabled via Bit 2 and Bit 0 of Register 0x0327 and Register 0x0347, depending on which DDC(s) are selected. The I data uses the test patterns selected for Channel A, and the Q data uses the test patterns selected for Channel B. For DDC3 only, the I data uses the test patterns from Channel A, and the Q data does not output test patterns. For more information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Table 32. ADC Test Modes

Output Test Mode Bit Sequence	Pattern Name	Expression	Default/ Seed Value	Sample (N, N + 1, N + 2, …)
0000	Off (default)	Not applicable	Not applicable	Not applicable
0001	Midscale short	00 0000 0000 0000	Not applicable	Not applicable
0010	Positive full-scale short	01 1111 1111 1111	Not applicable	Not applicable
0011	Negative full-scale short	10 0000 0000 0000	Not applicable	Not applicable
0100	Checkerboard	10 1010 1010 1010	Not applicable	0x1555, 0x2AAA, 0x1555, 0x2AAA, 0x1555
0101	PN sequence long	$x^{23} + x^{18} + 1$	0x3AFF	0x3FD7, 0x0002, 0x26E0, 0x0A3D, 0x1CA6
0110	PN sequence short	$x^9 + x^5 + 1$	0x0092	0x125B, 0x3C9A, 0x2660, 0x0c65, 0x0697
0111	One-word/zero-word toggle	11 1111 1111 1111	Not applicable	0x0000, 0x3FFF, 0x0000, 0x3FFF, 0x0000
1000	User input	Register 0x0551 to Register 0x0558	Not applicable	User Pattern 1, Bits[15:2], User Pattern 2, Bits[15:2], User Pattern 3, Bits[15:2], User Pattern 4, Bits[15:2], User Pattern 1, Bits[15:2] … for repeat mode User Pattern 1, Bits[15:2], User Pattern 2, Bits[15:2], User Pattern 3, Bits[15:2], User Pattern 4, Bits[15:2], 0x0000 … for single mode
1111	Ramp output	(x) % 2^{14}	Not applicable	(x) % 2^{14}, (x +1) % 2^{14}, (x +2) % 2^{14}, (x +3) % 2^{14}

JESD204B BLOCK TEST MODES

In addition to the ADC pipeline test modes, the AD9694 also has flexible test modes in the JESD204B block. These test modes are listed in Register 0x0573 and Register 0x0574. These test patterns can be injected at various points along the output data path. These test injection points are shown in Figure 82. Table 33 describes the various test modes available in the JESD204B block. For the AD9694, a transition from test modes (Register 0x0573 ≠ 0x00) to normal mode (Register 0x0573 = 0x00) requires an SPI soft reset. This reset is performed by writing 0x81 to Register 0x0000 (self cleared).

Transport Layer Sample Test Mode

The transport layer samples are implemented in the AD9694 as defined by Section 5.1.6.3 in the JEDEC JESD204B specification. These tests are shown in Register 0x0571, Bit 5. The test pattern is equivalent to the raw samples from the ADC.

Interface Test Modes

The interface test modes are described in Register 0x0573, Bits[3:0]. These test modes are also explained in Table 33. The interface tests can be injected at various points along the data. See Figure 82 for more information on the test injection points. Register 0x0573, Bits[5:4] show where these tests are injected.

Table 34, Table 35, and Table 36 show examples of some of the test modes when injected at the JESD204B sample input, physical layer (PHY) 10-bit input, and scrambler 8-bit input. In Table 34 through Table 36, UPx represents the user pattern control bits from the customer register map.

Data Link Layer Test Modes

The data link layer test modes are implemented in the AD9694 as defined by Section 5.3.3.8.2 in the JEDEC JESD204B specification. These tests are shown in Register 0x0574, Bits[2:0]. Test patterns inserted at the data link layer are useful for verifying the functionality of the data link layer. When the data link layer test modes are enabled, disable SYNCINB±x by writing 0xC0 to Register 0x0572.

Table 33. JESD204B Interface Test Modes

Output Test Mode Bit Sequence	Pattern Name	Expression	Default
0000	Off (default)	Not applicable	Not applicable
0001	Alternating checker board	0x5555, 0xAAAA, 0x5555, …	Not applicable
0010	1/0 word toggle	0x0000, 0xFFFF, 0x0000, …	Not applicable
0011	31-bit PN sequence	$x^{31} + x^{28} + 1$	0x0003AFFF
0100	23-bit PN sequence	$x^{23} + x^{18} + 1$	0x003AFF
0101	15-bit PN sequence	$x^{15} + x^{14} + 1$	0x03AF
0110	9-bit PN sequence	$x^{9} + x^{5} + 1$	0x092
0111	7-bit PN sequence	$x^{7} + x^{6} + 1$	0x07
1000	Ramp output	(x) % 2^{16}	Ramp size depends on test injection point
1110	Continuous/repeat user test	Register 0x0551 to Register 0x0558	User Pattern 1 to User Pattern 4, then repeat
1111	Single user test	Register 0x0551 to Register 0x0558	User Pattern 1 to User Pattern 4, then zeros

Table 34. JESD204B Sample Input for M = 2, S = 2, N' = 16 (Register 0x0573, Bits[5:4] = 2'b00)

Frame Number	Converter Number	Sample Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	9-Bit PN	23-Bit PN	User Repeat	User Single
0	0	0	0x5555	0x0000	(x) % 2^{16}	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	0	1	0x5555	0x0000	(x) % 2^{16}	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	1	0	0x5555	0x0000	(x) % 2^{16}	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	1	1	0x5555	0x0000	(x) % 2^{16}	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
1	0	0	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	0	1	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	1	0	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	1	1	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
2	0	0	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	0	1	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	1	0	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	1	1	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
3	0	0	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	0	1	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]

Frame Number	Converter Number	Sample Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	9-Bit PN	23-Bit PN	User Repeat	User Single
3	1	0	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	1	1	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
4	0	0	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	0	1	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	1	0	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	1	1	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000

Table 35. Physical Layer 10-Bit Input (Register 0x0573, Bits[5:4] = 2'b01)

10-Bit Symbol Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	9-Bit PN	23-Bit PN	User Repeat	User Single
0	0x155	0x000	(x) % 2^{10}	0x125	0x3FD	UP1[15:6]	UP1[15:6]
1	0x2AA	0x3FF	(x + 1) % 2^{10}	0x2FC	0x1C0	UP2[15:6]	UP2[15:6]
2	0x155	0x000	(x + 2) % 2^{10}	0x26A	0x00A	UP3[15:6]	UP3[15:6]
3	0x2AA	0x3FF	(x + 3) % 2^{10}	0x198	0x1B8	UP4[15:6]	UP4[15:6]
4	0x155	0x000	(x + 4) % 2^{10}	0x031	0x028	UP1[15:6]	0x000
5	0x2AA	0x3FF	(x + 5) % 2^{10}	0x251	0x3D7	UP2[15:6]	0x000
6	0x155	0x000	(x + 6) % 2^{10}	0x297	0x0A6	UP3[15:6]	0x000
7	0x2AA	0x3FF	(x + 7) % 2^{10}	0x3D1	0x326	UP4[15:6]	0x000
8	0x155	0x000	(x + 8) % 2^{10}	0x18E	0x10F	UP1[15:6]	0x000
9	0x2AA	0x3FF	(x + 9) % 2^{10}	0x2CB	0x3FD	UP2[15:6]	0x000
10	0x155	0x000	(x + 10) % 2^{10}	0x0F1	0x31E	UP3[15:6]	0x000
11	0x2AA	0x3FF	(x + 11) % 2^{10}	0x3DD	0x008	UP4[15:6]	0x000

Table 36. Scrambler 8-Bit Input (Register 0x0573, Bits[5:4] = 2'b10)

8-Bit Octet Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	9-Bit PN	23-Bit PN	User Repeat	User Single
0	0x55	0x00	(x) % 2^{8}	0x49	0xFF	UP1[15:9]	UP1[15:9]
1	0xAA	0xFF	(x + 1) % 2^{8}	0x6F	0x5C	UP2[15:9]	UP2[15:9]
2	0x55	0x00	(x + 2) % 2^{8}	0xC9	0x00	UP3[15:9]	UP3[15:9]
3	0xAA	0xFF	(x + 3) % 2^{8}	0xA9	0x29	UP4[15:9]	UP4[15:9]
4	0x55	0x00	(x + 4) % 2^{8}	0x98	0xB8	UP1[15:9]	0x00
5	0xAA	0xFF	(x + 5) % 2^{8}	0x0C	0x0A	UP2[15:9]	0x00
6	0x55	0x00	(x + 6) % 2^{8}	0x65	0x3D	UP3[15:9]	0x00
7	0xAA	0xFF	(x + 7) % 2^{8}	0x1A	0x72	UP4[15:9]	0x00
8	0x55	0x00	(x + 8) % 2^{8}	0x5F	0x9B	UP1[15:9]	0x00
9	0xAA	0xFF	(x + 9) % 2^{8}	0xD1	0x26	UP2[15:9]	0x00
10	0x55	0x00	(x + 10) % 2^{8}	0x63	0x43	UP3[15:9]	0x00
11	0xAA	0xFF	(x + 11) % 2^{8}	0xAC	0xFF	UP4[15:9]	0x00

SERIAL PORT INTERFACE

The AD9694 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the Serial Control Interface Standard (Rev. 1.0).

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 37). The SCLK (serial clock) pin is used to synchronize the read and write data presented from and to the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 37. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input, which is used to synchronize serial interface, reads, and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that gates the read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 4 and Table 7.

Other modes involving the CSB pin are available. The CSB pin can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB can stall high between bytes to allow additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This bit allows the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first mode is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the Serial Control Interface Standard (Rev. 1.0).

HARDWARE INTERFACE

The pins described in Table 37 comprise the physical interface between the user programming device and the serial port of the AD9694. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9694 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 38 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the Serial Control Interface Standard (Rev. 1.0). The AD9694 device specific features are described in the Memory Map section.

Table 38. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode.
Clock	Allows the user to access the clock divider via the SPI.
DDC	Allows the user to set up decimation filters for different applications.
Test Input/Output	Allows the user to set test modes to have known data on output bits.
Output Mode	Allows the user to set up outputs.
Serializer/Deserializer (SERDES) Output Setup	Allows the user to vary SERDES settings such as swing and emphasis.

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is divided into four sections: the Analog Devices SPI registers (Register 0x0000 to Register 0x000D and Register 0x18A6 to Register 0x1A4D, the ADC function registers (Register 0x003F to Register 0x027A, Register 0x0701, and Register 0x073B), the DDC function registers (Register 0x0300 to Register 0x0347), and the digital outputs and test modes registers (Register 0x0550 to Register 0x1262).

Table 39 (see the Memory Map section) documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x0561, the output sample mode register, has a hexadecimal default value of 0x01. This default value means that Bit 0 = 1, and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see Table 39.

Unassigned and Reserved Locations

All address and bit locations that are not included in Table 39 are not currently supported for this device. Write unused bits of a valid address location with 0s unless the default value is set otherwise. Writing to these locations is required only when part of an address location is unassigned (for example, Address 0x0561). If the entire address location is open (for example, Address 0x0013), do not write to this address location.

Default Values

After the AD9694 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 39.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."
- X denotes a don't care bit.

ADC Pair Addressing

The AD9694 functionally operates as two pairs of dual IF receiver channels. There are two ADCs and two DDCs in each pair making for a total of four of each for the AD9694 device. To access the SPI registers for each pair, the pair index must be written in Register 0x0009. The pair index register must be written prior to any other SPI write to the AD9694.

Channel Specific Registers

Some channel setup functions, such as the fast detect control (Register 0x0247), can be programmed to a different value for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 39 as local. These local registers and bits can be accessed by setting the appropriate Channel A/Channel C or Channel B/Channel D bits in Register 0x0008. The particular channel that is addressed is dependent upon the pair selection written to Register 0x0009. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, set only Channel A/Channel C or Channel B/Channel D to read one of the two registers. If both bits are set during an SPI read cycle, the device returns the value for Channel A. If both pairs and both channels are selected via Register 0x0009 and Register 0x0008, the device returns the value for Channel A.

The names of the registers listed Table 39 are prefixed with either global map, channel map, JESD204B map, or pair map. Registers in the pair map and JESD204B map apply to a pair of channels, either Pair A/B or Pair C/D. To write registers in the pair map and JESD204B map, the pair index register (Register 0x0009) must be written to address the appropriate pair. The SPI Configuration A (Register 0x0000), SPI Configuration B (Register 0x0001), and pair index (Register 0x0009) registers are the only registers that reside in the global map. Registers in the channel map are local to each channel: Channel A, Channel B, Channel C, or Channel D. To write registers in the channel map, the pair index register (Register 0x0009) must be written first to address the desired pair (Pair A/B or Pair C/D) followed by writing the device index register (Register 0x0008) to select the desired channel (Channel A/Channel C or Channel B/Channel D).

For example, to write Channel A to a test mode (set by Register 0x0550), first write 0x01 to Register 0x0009 to select Pair A/B, followed by writing 0x01 to Register 0x0008 to select Channel A. Then, write Register 0x0550 to the value for the desired test mode. To write all channels to a test mode (set by Register 0x0550), first write Register 0x0009 to a value of 0x03 to select both Pair A/B and Pair C/D, followed by writing Register 0x0008 to a value of 0x03 to select Channel A, Channel B, Channel C, and Channel D. Next, write Register 0x0550 to the value for the desired test mode.

SPI Soft Reset

After issuing a soft reset by programming 0x81 to Register 0x0000, the AD9694 requires 5 ms to recover. When programming the AD9694 for application setup, ensure that an adequate delay is programmed into the firmware after asserting the soft reset and before starting the device setup.

MEMORY MAP REGISTER TABLE—DETAILS

All address locations that are not included in Table 39 are not currently supported for this device and must not be written.

Table 39. Memory Map Details

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0000	Global map SPI Configuration A	7	Soft reset (self clearing)		When a soft reset is issued, the user must wait 5 ms before writing to any other register. This wait provides sufficient time for the boot loader to complete.	0x0	R/W
				0	Do nothing.		
				1	Reset the SPI and registers (self clearing).		
		6	LSB first mirror			0x0	R/W
				1	LSB shifted first for all SPI operations.		
				0	MSB shifted first for all SPI operations.		
		5	Address ascension mirror			0x0	R/W
				0	Multibyte SPI operations cause addresses to auto-increment.		
				1	Multibyte SPI operations cause addresses to auto-increment.		
		4	Reserved		Reserved.	0x0	R
		3	Reserved		Reserved.	0x0	R
		2	Address ascension			0x0	R/W
				0	Multibyte SPI operations cause addresses to auto-increment.		
				1	Multibyte SPI operations cause addresses to auto-increment.		
		1	LSB first			0x0	R/W
				1	MSB shifted first for all SPI operations.		
				0	MSB shifted first for all SPI operations.		
		0	Soft reset (self clearing)		When a soft reset is issued, the user must wait 5 ms before writing to any other register. This wait provides sufficient time for the boot loader to complete.	0x0	R/W
				0	Do nothing.		
				1	Reset the SPI and registers (self clearing).		
0x0001	Global map SPI Configuration B	7	Single instruction			0x0	R/W
				0	SPI streaming enabled.		
				1	Streaming (multibyte read/write) is disabled. Only one read or write operation is performed regardless of the state of the CSB line.		
		[6:2]	Reserved		Reserved.	0x0	R
		1	Datapath soft reset (self clearing)			0x0	R/W
				0	Normal operation.		
				1	Datapath soft reset (self clearing)		
		0	Reserved		Reserved.	0x0	R
0x0002	Channel map chip configuration	[7:2]	Reserved		Reserved.	0x0	R
		[1:0]	Channel power modes		Channel power modes.	0x0	R/W
				00	Normal mode (power up).		

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
				10	Standby mode. The digital data path clocks are disabled, the JESD204B interface is enabled, and the outputs are enabled.		
				11	Power-down mode. The digital data path clocks are disabled, the digital data path is held in reset, the JESD204B interface is disabled, and the outputs are disabled.		
0x0003	Pair map chip type	[7:0]	CHIP_TYPE		Chip type.	0x3	R
				0x3	High speed ADC.		
0x0004	Pair map chip ID LSB	[7:0]	CHIP_ID		Chip ID.	0xDB	R
0x0006	Pair map chip grade	[7:4]	CHIP_SPEED_GRADE		Chip speed grade.	0x0	R
				0101	500 MHz.		
		[3:0]	Reserved		Reserved.	0x0	R
0x0008	Pair map device index	[7:2]	Reserved		Reserved.	0x0	R
		1	Channel B/D			0x1	R/W
				0	ADC Core B/D does not receive the next SPI command.		
				1	ADC Core B/D receives the next SPI command.		
		0	Channel A/C			0x1	R/W
				0	ADC Core A/C does not receive the next SPI command.		
				1	ADC Core A/C receives the next SPI command.		
0x0009	Global map pair index	[7:2]	Reserved		Reserved.	0x0	R
		1	Pair C/D			0x1	R/W
				0	ADC Pair C/D does not receive the next read/write command from the SPI interface.		
				1	ADC Pair C/D does not receive the next read/write command from the SPI interface.		
		0	Pair A/B			0x1	R/W
				0	ADC Pair A/B does not receive the next read/write command from the SPI interface.		
				1	ADC Pair A/B does receive the next read/write command from the SPI interface.		
0x000A	Pair map scratch pad	[7:0]	Scratch pad		Chip scratch pad register. Used to provide a consistent memory location for software debug.	0x7	R/W
0x000B	Pair map SPI revision	[7:0]	SPI_REVISION		SPI revision register. (0x01 = Revision 1.0)	0x1	R
				00000001	Revision 1.0.		
0x000C	Pair map vendor ID LSB	[7:0]	CHIP_VENDOR_ID[7:0]		Vendor ID.	0x56	R
0x000D	Pair map vendor ID MSB	[7:0]	CHIP_VENDOR_ID[15:8]		Vendor ID.	0x4	R
0x003F	Channel map chip power-down pin	7	PDWN/STBY disable		Used in conjunction with Register 0x0040.	0x0	R/W
				0	Power-down pin (PDWN/STBY) enabled. Global pin control selection enabled (default).		

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
				1	Power-down pin (PDWN/STBY) disabled/ignored. Global pin control selection ignored.		
		[6:0]	Reserved		Reserved.	0x0	R
0x0040	Pair Map Chip Pin Control 1	[7:6]	PDWN/STBY function			0x0	R/W
				00	Power-down pin. Assertion of the external power-down pin (PDWN/STBY) causes the chip to enter full power-down mode.		
				01	Standby pin. Assertion of the external power-down (PDWN/STBY) causes the chip to enter standby mode.		
				10	Pin disabled. Assertion of the external power-down pin (PDWN/STBY) is ignored.		
		[5:3]	Fast Detect B/D (FD_B/FD_D)			0x7	R/W
				000	Fast Detect B/D output.		
				001	JESD204B LMFC output.		
				010	JESD204B internal SYNC~ output.		
				111	Disabled (configured as input with weak pull-down resistor.		
		[2:0]	Fast Detect A/C (FD_A/FD_C)			0x7	R/W
				000	Fast Detect A/C output.		
				001	JESD204B LMFC output.		
				010	JESD204B internal SYNC~ output.		
				111	Disabled (configured as input with weak pull-down resistor.		
0x0108	Pair map clock divider control	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Clock divider			0x1	R/W
				000	Divide by 1.		
				001	Divide by 2.		
				011	Divide by 4.		
				111	Divide by 8.		
0x0109	Channel map clock divider phase	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Clock divider phase offset			0x0	R/W
				0000	0 input clock cycles delayed.		
				0001	½ input clock cycles delayed (invert clock).		
				0010	1 input clock cycle delayed.		
				0011	1 ½ input clock cycles delayed.		
				0100	2 input clock cycles delayed.		
				0101	2 ½ input clock cycles delayed.		
				0110	3 input clock cycles delayed.		
				0111	3 ½ input clock cycles delayed.		
				1000	4 input clock cycles delayed.		
				1001	4 ½ input clock cycles delayed.		
				1010	5 input clock cycles delayed.		
				1011	5 ½ input clock cycles delayed.		
				1100	6 input clock cycles delayed.		
				1101	6 ½ input clock cycles delayed.		
				1110	7 input clock cycles delayed.		
				1111	7 ½ input clock cycles delayed.		

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x010A	Pair map clock divider SYSREF± control	7	Clock divider autophase adjust			0x0	R/W
				0	Clock divider phase is not changed by SYSREF± (disabled).		
				1	Clock divider phase is automatically adjusted by SYSREF± (enabled).		
		[6:4]	Reserved		Reserved.	0x0	R
		[3:2]	Clock divider negative skew window			0x0	R/W
				00	No negative skew: SYSREF± must be captured accurately.		
				01	½ device clocks of negative skew.		
				10	1 device clock of negative skew.		
				11	1 ½ device clocks of negative skew.		
		[1:0]	Clock divider positive skew window			0x0	R/W
				00	No positive skew: SYSREF± must be captured accurately.		
				01	½ device clocks of positive skew.		
				10	1 device clock of positive skew.		
				11	1 ½ device clocks of positive skew.		
0x0110	Pair map clock delay control	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Clock delay mode select		Clock delay mode select. Used in conjunction with Register 0x0111 and Register 0x0112.	0x0	R/W
				000	No clock delay.		
				001	Reserved.		
				010	Fine delay: only Delay Step 0 to Delay Step 16 valid.		
				011	Fine delay (lowest jitter): only Delay Step 0 to Delay Step 16 valid.		
				100	Fine delay: all 192 delay steps valid.		
				101	Reserved (same as 100).		
				110	Fine delay enabled (all 192 delay steps valid); super fine delay enabled (all 128 delay steps valid).		
0x0111	Channel map clock super fine delay	[7:0]	Clock super fine delay adjust		Clock super fine delay adjust: this is an unsigned control to adjust the super fine sample clock delay in 0.25 ps steps. 0x00 = 0 delay steps. … 0x08 = 8 delay steps. … 0x80 = 128 delay steps.	0x0	R/W
0x0112	Channel map clock fine delay	[7:0]	Clock fine delay adjust		Clock fine delay adjust: this is an unsigned control to adjust the fine sample clock skew in 1.725 ps steps. 0x00 = 0 delay steps. … 0x08 = 8 delay steps. … 0xC0 = 192 delay steps.	0xC0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x011A	Clock detection control	[7:5]	Reserved		Reserved.	0x0	R/W
		[4:3]	Clock detection threshold		Clock detection threshold.	0x1	R/W
				01	Threshold 1 for sample rate ≥ 300 MSPS		
				11	Threshold 2 for sample rate < 300 MSPS		
		[2:0]	Reserved		Reserved	0x1	R/W
0x011B	Pair map clock status	[7:1]	Reserved		Reserved.	0x0	R
		0	Input clock detect		Clock detection status	0x0	R
				0	Input clock not detected.		
				1	Input clock detected/locked.		
0x011C	Clock DCS Control 1	[7:3]	Reserved		Reserved	0x1	R/W
		1	Clock DCS 1 enable	0	DCS 1 bypassed.	0x0	R/W
				1	DCS 1 enabled.		
		0	Clock DCS 1 power-up	0	DCS 1 powered down	0x0	R/W
				1	DCS 1 powered up. The DCS must be powered up before being enabled.		
0x011E	Clock DCS Control 2 (this register needs to be set to the value same as DCS Control 1)	[7:3]	Reserved		Reserved	0x11	R/W
		1	Clock DCS 2 enable	0	DCS 2 bypassed.	0x0	R/W
				1	DCS 2 enabled.		
		0	Clock DCS 2 power-up	0	DCS 2 powered down.	0x0	R/W
				1	DCS 2 powered up. The DCS must be powered up before being enabled.		
0x011F	Clock DCS Control 3	[7:0]	Clock DCS 3 enable	0x84	DCS 3 bypassed.	0x84	R/W
				0x81	DCS 3 enabled.		
0x0120	Pair map SYSREF Control 1	7	Reserved		Reserved.	0x0	R
		6	SYSREF± flag reset			0x0	R/W
				0	Normal flag operation.		
				1	SYSREF± flags held in reset (setup/hold error flags cleared).		
		5	Reserved		Reserved.	0x0	R
		4	SYSREF± transition select			0x0	R/W
				0	SYSREF± is valid on low to high transitions using selected CLK± edge. When changing this setting, SYSREF± mode select must be set to disabled.		
				1	SYSREF± is valid on high to low transitions using selected CLK± edge. When changing this setting, SYSREF± mode select must be set to disabled.		
		3	CLK± edge select			0x0	R/W
				0	Captured on rising edge of CLK± input.		
				1	Captured on falling edge of CLK± input.		
		[2:1]	SYSREF± mode select			0x0	R/W
				00	Disabled.		
				01	Continuous.		
				10	N shot.		
		0	Reserved		Reserved.	0x0	R

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0121	Pair map SYSREF Control 2	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	SYSREF± N shot ignore counter select			0x0	R/W
				0000	Next SYSREF± only (do not ignore).		
				0001	Ignore the first SYSREF± transition.		
				0010	Ignore the first two SYSREF± transitions.		
				0011	Ignore the first three SYSREF± transitions.		
				0100	Ignore the first four SYSREF± transitions.		
				0101	Ignore the first five SYSREF± transitions.		
				0110	Ignore the first six SYSREF± transitions.		
				0111	Ignore the first seven SYSREF± transitions.		
				1000	Ignore the first eight SYSREF± transitions.		
				1001	Ignore the first nine SYSREF± transitions.		
				1010	Ignore the first 10 SYSREF± transitions.		
				1011	Ignore the first 11 SYSREF± transitions.		
				1100	Ignore the first 12 SYSREF± transitions.		
				1101	Ignore the first 13 SYSREF± transitions.		
				1110	Ignore the first 14 SYSREF± transitions.		
				1111	Ignore the first 15 SYSREF± transitions.		
0x0123	Pair map SYSREF Control 4	7	Reserved		Reserved.	0x0	R
		[6:0]	SYSREF± timestamp delay, Bits[6:0]		SYSREF± timestamp delay (in converter sample clock cycles). 0: 0 sample clock cycle delay). 1: 1 sample clock cycle delay. … 127: 127 sample clock cycle delay.	0x40	R/W
0x0128	Pair map SYSREF Status 1	[7:4]	SYSREF± hold status, Bits[7:4]		SYSREF± hold status. See Table 31 for more information.	0x0	R
		[3:0]	SYSREF± setup status, Bits[3:0]		SYSREF± setup status. See Table 31 for more information.	0x0	R
0x0129	Pair map SYSREF Status 2	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Clock divider phase when SYSREF± was captured		SYSREF± divider phase. Represents the phase of the divider when SYSREF± was captured. 0000 = in phase. 0001 = SYSREF± is ½ cycle delayed from clock. 0010 = SYSREF± is 1 cycle delayed from clock. 0011 = 1½ input clock cycles delayed. 0100 = 2 input clock cycles delayed. 0101 = 2½ input clock cycles delayed. … 1111 = 7½ input clock cycles delayed.	0x0	R
0x012A	Pair map SYSREF Status 3	[7:0]	SYSREF counter, Bits[7:0] increments when a SYSREF± is captured		SYSREF± count. Running counter that increments whenever a SYSREF± event is captured. Reset by Register 0x0120, Bit 6. Wraps around at 255. Read these bits only while Register 0x0120, Bits[2:1] is set to disabled.	0x0	R

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x01FF	Pair map chip sync	[7:1]	Reserved		Reserved.	0x0	R
		0	Synchronization mode			0x0	R/W
				0x0	Sample synchronization mode. SYSREF± signal resets all internal sample dividers. Use this mode when synchronizing multiple chips as specified in the JESD204B standard. If the phase of any of the dividers needs to change, the JESD204B link goes down.		
				0x1	Partial synchronization/timestamp mode. SYSREF± signal does not reset sample internal dividers. In this mode, the JESD204B link, the signal monitor, the parallel interface clocks are not affected by the SYSREF± signal. The SYSREF± signal simply timestamps a sample as it passes through the ADC.		
0x0200	Pair map chip mode	[7:6]	Reserved		Reserved.	0x0	R/W
		5	Chip Q ignore		Chip real (I) only selection.	0x0	R/W
				0	Both real (I) and complex (Q) selected.		
				1	Only real (I) selected. Complex (Q) is ignored.		
		4	Reserved		Reserved.	0x0	R
		[3:0]	Chip application mode			0x0	R/W
				0000	Full bandwidth mode.		
				0001	One DDC mode (DDC 0 only).		
				0010	Two DDC mode (DDC 0 and 1 only).		
0x0201	Pair map chip decimation ratio	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Chip decimation ratio select		Chip decimation ratio.	0x0	R/W
				000	Decimate by 1 (full sample rate).		
				001	Decimate by 2.		
				010	Decimate by 4.		
				011	Decimate by 8.		
				100	Decimate by 16.		
0x0228	Channel map custom offset	[7:0]	Offset adjust in LSBs from +127 to −128		Digital data path offset. Twos complement offset adjustment aligned with least significant converter resolution bit.	0x0	R/W
0x0245	Channel map fast detect control	[7:4]	Reserved		Reserved.	0x0	R
		3	Force FD_A/FD_B/FD_C/FD_D pins			0x0	R/W
				0	Normal operation of fast detect pin.		
				1	Force a value on fast detect pin (see Bit 2).		
		2	Force value of FD_A/FD_B/FD_C/FD_D pins (if force pins is true, this value is output on FD_x pins)		The fast detect output pin for this channel is set to this value when the output is forced.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	Enable fast detect output			0x0	R/W
				0	Fine fast detect disabled.		
				1	Fine fast detect enabled.		
0x0247	Channel map fast detect upper threshold LSB	[7:0]	Fast detect upper threshold, Bits[7:0]		LSBs of fast detect upper threshold. 8 LSBS of the programmable 13-bit upper threshold that is compared to the fine ADC magnitude.	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0248	Channel map fast detect upper threshold MSB	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Fast detect upper threshold, Bits[12:8]		LSBs of fast detect upper threshold. 8 LSBS of the programmable 13-bit upper threshold that is compared to the fine ADC magnitude.	0x0	R/W
0x0249	Channel map fast detect lower threshold LSB	[7:0]	Fast detect lower threshold, Bits[7:0]		LSBs of fast detect lower threshold. 8 LSBS of the programmable 13-bit lower threshold that is compared to the fine ADC magnitude.	0x0	R/W
0x024A	Channel map fast detect lower threshold MSB	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Fast detect lower threshold, Bits[12:8]		LSBs of fast detect lower threshold. 8 LSBS of the programmable 13-bit lower threshold that is compared to the fine ADC magnitude.	0x0	R/W
0x024B	Channel map fast detect dwell time LSB	[7:0]	Fast detect dwell time, Bits[7:0]		LSBs of fast detect dwell time counter target. This is a load value for a 16-bit counter that determines how long the ADC data must remain below the lower threshold before the FD_x pins are reset to 0.	0x0	R/W
0x024C	Channel map fast detect dwell time MSB	[7:0]	Fast detect dwell time, Bits[15:8]		LSBs of fast detect dwell time counter target. This is a load value for a 16-bit counter that determines how long the ADC data must remain below the lower threshold before the FD_x pins are reset to 0.	0x0	R/W
0x026F	Pair map signal monitor sync control	[7:2]	Reserved		Reserved.	0x0	R
		1	Reserved		Reserved.	0x0	R/W
		0	Signal monitor synchronization mode	0 1	Synchronization disabled. Only the next valid edge of the SYSREF± pin is used to synchronize the signal monitor block. Subsequent edges of the SYSREF± pin are ignored. When the next SYSREF± is received, this bit is cleared. The SYSREF± input pin must be enabled to synchronize the signal monitor blocks.	0x0	R/W
0x0270	Channel map signal monitor control	[7:2]	Reserved		Reserved.	0x0	R
		1	Peak detector	0 1	Peak detector disabled. Peak detector enabled.	0x0	R/W
		0	Reserved		Reserved.	0x0	R
0x0271	Channel Map Signal Monitor Period 0	[7:0]	Signal monitor period, Bits[7:0]		This 24-bit value sets the number of output clock cycles over which the signal monitor performs its operation. Bit 0 is ignored.	0x80	R/W
0x0272	Channel Map Signal Monitor Period 1	[7:0]	Signal monitor period, Bits[15:8]		This 24-bit value sets the number of output clock cycles over which the signal monitor performs its operation. Bit 0 is ignored.	0x0	R/W
0x0273	Channel Map Signal Monitor Period 2	[7:0]	Signal monitor period, Bits[23:16]		This 24-bit value sets the number of output clock cycles over which the signal monitor performs its operation. Bit 0 is ignored.	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0274	Channel map signal monitor status control	[7:5]	Reserved		Reserved.	0x0	R
		4	Result update			0x0	R/W
				1	Status update based on Bits[2:0] (self clearing).		
		3	Reserved		Reserved.	0x0	R
		[2:0]	Result selection			0x1	R/W
				001	Peak detector placed on status readback signals.		
0x0275	Channel Map Signal Monitor Status 0	[7:0]	Signal monitor result, Bits[7:0]		Signal monitor status result. This 20-bit value contains the status result calculated by the signal monitor block. The content is dependent on the Register 0x0274, Bits[2:0] bit settings.	0x0	R
0x0276	Channel Map Signal Monitor Status 1	[7:0]	Signal monitor result, Bits[15:8]		Signal monitor status result. This 20-bit value contains the status result calculated by the signal monitor block. The content is dependent on the Register 0x0274, Bits[2:0] bit settings.	0x0	R
0x0277	Channel Map Signal Monitor Status 2	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Signal monitor result, Bits[19:16]		Signal monitor status result. This 20-bit value contains the status result calculated by the signal monitor block. The content is dependent on the Register 0x0274, Bits[2:0] bit settings.	0x0	R
0x0278	Channel map signal monitor status frame counter	[7:0]	Period count result, Bits[7:0]		Signal monitor frame counter status bits. Frame counter increments whenever the period counter expires.	0x0	R
0x0279	Channel map signal monitor serial framer control	[7:2]	Reserved		Reserved.	0x0	R
		1	Reserved		Reserved.	0x0	R/W
		0	Signal monitor SPORT over JESD204B enable			0x0	R/W
				0	Disabled.		
				1	Enabled.		
0x027A	SPORT over JESD204B input selection (local)	[7:6]	Reserved		Reserved.	0x0	R
		1	SPORT over JESD204B input selection		Signal monitor serial framer input selection. When each individual bit is a 1, the corresponding signal statistics information is sent within the frame.	0x1	R/W
				0	Disabled.		
				1	Peak detector data inserted in serial frame.		
		0	Reserved			0x0	R
0x0300	Pair map DDC sync control	7	Reserved		Reserved.	0x0	R/W
		6	Reserved		Reserved.	0x0	R/W
		5	Reserved		Reserved.	0x0	R
		4	DDC NCO soft reset		This bit can be used to synchronize all the NCOs inside the DDC blocks.	0x0	R/W
				0	Normal operation.		
				1	DDC held in reset.		
		[3:2]	Reserved		Reserved.	0x0	R
		1	DDC next sync		The SYSREF± pin must be an integer multiple of the NCO frequency for this function to operate correctly in continuous mode.	0x0	R/W
				0	Continuous mode.		

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
				1	Only the next valid edge of the SYSREF± pin is used to synchronize the NCO in the DDC block. Subsequent edges of the SYSREF± pin are ignored. When the next SYSREF± edge is found, the DDC synchronization enable bit is cleared.		
		0	DDC synchronization mode		The SYSREF± input pin must be enabled to synchronize the DDCs.	0x0	R/W
				0	Synchronization Disabled.		
				1	If DDC next sync == 1, only the next valid edge of the SYSREF± pin is used to synchronize the NCO in the DDC block. Subsequent edges of the SYSREF± pin are ignored. When the next SYSREF± edge is received, this bit is cleared.		
0x0310	Pair map DDC 0 control	7	DDC 0 mixer select			0x0	R/W
				0	Real mixer (I and Q inputs must be from the same real channel).		
				1	Complex mixer (I and Q must be from separate, real and imaginary quadrature ADC receive channels—analog demodulator).		
		6	DDC 0 gain select		Gain can be used to compensate for the 6 dB loss associated with mixing an input signal down to baseband and filtering out its negative component.	0x0	R/W
				0	0 dB gain.		
				1	6 dB gain (multiply by 2).		
		[5:4]	DDC 0 IF mode			0x0	R/W
				00	Variable IF mode.		
				01	0 Hz IF mode.		
				10	$f_S/4$ Hz IF mode.		
				11	Test mode.		
		3	DDC 0 complex to real enable			0x0	R/W
				0	Complex (I and Q) outputs contain valid data.		
				1	Real (I) output only. Complex to real enabled. Uses extra $f_S/4$ mixing to convert to real.		
		2	Reserved		Reserved.	0x0	R
		[1:0]	DDC 0 decimation rate select		Decimation filter selection.	0x0	R/W
				11	HB1 filter selection: decimate by 1 (real outputs (complex to real enabled)) or decimate by 2 (complex outputs (complex to real disabled)).		
				00	HB2 + HB1 filter selection: decimate by 2 (real outputs (complex to real enabled)) or decimate by 4 ((complex outputs (complex to real disabled)).		
				01	HB3 + HB2 + HB1 filter selection: decimate by 4 (real outputs (complex to real enabled)) or decimate by 8 (complex outputs (complex to real disabled)).		
				10	HB4 + HB3 + HB2 + HB1 filter selection: decimate by 8 (real outputs (complex to real enabled)) or decimate by 16 (complex outputs (complex to real disabled)).		

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0311	Pair Map DDC 0 input select	[7:3]	Reserved		Reserved.	0x0	R
		2	DDC 0 Q input select			0x0	R/W
				0	Channel A/Channel C.		
				1	Channel B/Channel D.		
		1	Reserved		Reserved.	0x0	R
		0	DDC 0 I input select			0x0	R/W
				0	Channel A.		
				1	Channel B.		
0x0314	Pair Map DDC 0 Phase Increment 0	[7:0]	DDC 0 NCO frequency value, twos complement, Bits[7:0]		NCO phase increment value; twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0315	Pair Map DDC 0 Phase Increment 1	[7:0]	DDC 0 NCO frequency value, twos complement, Bits[15:8]		NCO phase increment value; twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0316	Pair Map DDC 0 Phase Increment 2	[7:0]	DDC 0 NCO frequency value, twos complement, Bits[23:16]		NCO phase increment value; twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0317	Pair Map DDC 0 Phase Increment 3	[7:0]	DDC 0 NCO frequency value, twos complement, Bits[31:24]		NCO phase increment value; twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0318	Pair Map DDC 0 Phase Increment 4	[7:0]	DDC 0 NCO frequency value, twos complement, Bits[39:32]		NCO phase increment value; twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x031A	Pair Map DDC 0 Phase Increment 5	[7:0]	DDC 0 NCO frequency value, twos complement, Bits[47:40]		NCO phase increment value; twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x031D	Pair Map DDC 0 Phase Offset 0	[7:0]	DDC 0 NCO phase value, twos complement, Bits[7:0]		Twos complement phase offset value for the NCO.	0x0	R/W
0x031E	Pair Map DDC 0 Phase Offset 1	[7:0]	DDC 0 NCO phase value, twos complement, Bits[15:8]		Twos complement phase offset value for the NCO.	0x0	R/W
0x031F	Pair Map DDC 0 Phase Offset 2	[7:0]	DDC 0 NCO phase value, twos complement, Bits[23:16]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0320	Pair Map DDC 0 Phase Offset 3	[7:0]	DDC 0 NCO phase value, twos complement, Bits[31:24]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0321	Pair Map DDC 0 phase Offset 4	[7:0]	DDC 0 NCO phase value, twos complement, Bits[39:32]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0322	Pair Map DDC 0 Phase Offset 5	[7:0]	DDC 0 NCO phase value, twos complement, Bits[47:40]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0327	Pair Map DDC 0 test enable	[7:3]	Reserved		Reserved.	0x0	R
		2	DDC 0 Q output test mode enable		Q samples always use Test Mode B/D block.	0x0	R/W
				0	Test mode disabled.		
				1	Test mode enabled.		
		1	Reserved		Reserved.	0x0	R

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	DDC 0 I output test mode enable		I samples always use Test Mode A/C block.	0x0	R/W
				0	Test mode disabled.		
				1	Test mode enabled.		
0x0330	Pair Map DDC 1 control	7	DDC 1 mixer select			0x0	R/W
				0	Real mixer (I and Q inputs must be from the same real channel).		
				1	Complex mixer (I and Q must be from separate real and imaginary quadrature ADC receive channels—analog demodulator).		
		6	DDC 1 gain select		Gain can be used to compensates for the 6 dB loss associated with mixing an input signal down to baseband and filtering out its negative component.	0x0	R/W
				0	0 dB gain.		
				1	6 dB gain (multiply by 2).		
		[5:4]	DDC 1 IF mode			0x0	R/W
				00	Variable IF mode.		
				01	0 Hz IF mode.		
				10	$f_S/4$ Hz IF mode.		
				11	Test mode.		
		3	DDC 1 complex to real enable			0x0	R/W
				0	Complex (I and Q) outputs contain valid data.		
				1	Real (I) output only. Complex to real enabled. Uses extra $f_S/4$ mixing to convert to real.		
		2	Reserved		Reserved.	0x0	R
		[1:0]	DDC 1 decimation rate select		Decimation filter selection.	0x0	R/W
				11	HB1 filter selection: decimate by 1 (real outputs (complex to real enabled)) or decimate by 2 (complex outputs (complex to real disabled)).		
				00	HB2 + HB1 filter selection: decimate by 2 (real outputs (complex to real enabled)) or decimate by 4 ((complex outputs (complex to real disabled)).		
				01	HB3 + HB2 + HB1 filter selection: decimate by 4 (real outputs (complex to real enabled)) or decimate by 8 (complex outputs (complex to real disabled)).		
				10	HB4 + HB3 + HB2 + HB1 filter selection: decimate by 8 (real outputs (complex to real enabled)) or decimate by 16 (complex outputs (complex to real disabled)).		
0x0331	Pair Map DDC 1 input select	[7:3]	Reserved		Reserved.	0x0	R
		2	DDC 1 Q input select			0x1	R/W
				0	Channel A/Channel C.		
				1	Channel B/Channel D.		
		1	Reserved		Reserved.	0x0	R
		0	DDC 1 I input select			0x1	R/W
				0	Channel A.		
				1	Channel B.		

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0334	Pair Map DDC 1 Phase Increment 0	[7:0]	DDC 1 NCO frequency value, twos complement, Bits[7:0]		NCO phase increment value. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0335	Pair Map DDC 1 Phase Increment 1	[7:0]	DDC 1 NCO frequency value, twos complement, Bits[15:8]		NCO phase increment value. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0336	Pair Map DDC 1 Phase Increment 2	[7:0]	DDC 1 NCO frequency value, twos complement, Bits[23:16]		NCO phase increment value. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0337	Pair Map DDC 1 Phase Increment 3	[7:0]	DDC 1 NCO frequency value, twos complement, Bits[31:24]		NCO phase increment value. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0338	Pair Map DDC 1 Phase Increment 4	[7:0]	DDC 1 NCO frequency value, twos complement, Bits[39:32]		NCO phase increment value. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x033A	Pair Map DDC 1 Phase Increment 5	[7:0]	DDC 1 NCO frequency value, twos complement, Bits[47:40]		NCO phase increment value. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x033D	Pair Map DDC 1 Phase Offset 0	[7:0]	DDC 1 NCO phase value, twos complement, Bits[7:0]		Twos complement phase offset value for the NCO.	0x0	R/W
0x033E	Pair Map DDC 1 Phase Offset 1	[7:0]	DDC 1 NCO phase value, twos complement, Bits[15:8]		Twos complement phase offset value for the NCO.	0x0	R/W
0x033F	Pair Map DDC 1 Phase Offset 2	[7:0]	DDC 1 NCO phase value, twos complement, Bits[23:16]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0340	Pair Map DDC 1 Phase Offset 3	[7:0]	DDC 1 NCO phase value, twos complement, Bits[31:24]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0341	Pair Map DDC 1 Phase Offset 4	[7:0]	DDC 1 NCO phase value, twos complement, Bits[39:32]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0342	Pair Map DDC 1 Phase Offset 5	[7:0]	DDC 1 NCO phase value, twos complement, Bits[47:40]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0347	Pair Map DDC 1 test enable	[7:3]	Reserved		Reserved.	0x0	R
		2	DDC 1 Q output test mode enable		Q samples always use Test Mode B/Test Mode D block.	0x0	R/W
				0	Test mode disabled.		
				1	Test mode enabled.		
		1	Reserved		Reserved.	0x0	R
		0	DDC 1 I output test mode enable		I samples always use Test Mode A/Test Mode C block.	0x0	R/W
				0	Test mode disabled.		
				1	Test mode enabled.		
0x0550	Channel map test mode control	7	User pattern selection			0x0	R/W
				0	Continuous repeat.		
				1	Single pattern.		
		6	Reserved		Reserved.	0x0	R

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		5	Reset pseudorandom long generator			0x0	R/W
				0	Long PN enabled.		
				1	Long PN held in reset.		
		4	Reset PN short gen			0x0	R/W
				0	Short PN enabled.		
				1	Short PN held in reset.		
		[3:0]	Test mode selection			0x0	R/W
				0000	Off—normal operation.		
				0001	Midscale short.		
				0010	Positive full scale.		
				0011	Negative full scale.		
				0100	Alternating checkerboard.		
				0101	PN sequence—long.		
				0110	PN sequence—short.		
				0111	1/0 word toggle.		
				1000	User pattern test mode (used with the test mode pattern selection and the User Pattern 1 through User Pattern 4 registers)		
				1111	Ramp output.		
0x0551	Pair map User Pattern 1 LSB	[7:0]	User Pattern 1, Bits[7:0]		User Test Pattern 1 least significant byte.	0x0	R/W
0x0552	Pair map User Pattern 1 MSB	[7:0]	User Pattern 1, Bits[15:8]		User Test Pattern 1 most significant byte.	0x0	R/W
0x0553	Pair map User Pattern 2 LSB	[7:0]	User Pattern 2, Bits[7:0]		User Test Pattern 2 least significant byte.	0x0	R/W
0x0554	Pair map User Pattern 2 MSB	[7:0]	User Pattern 2, Bits[15:8]		User Test Pattern 2 most significant byte.	0x0	R/W
0x0555	Pair map User Pattern 3 LSB	[7:0]	User Pattern 3, Bits[7:0]		User Test Pattern 3 least significant byte.	0x0	R/W
0x0556	Pair map User Pattern 3 MSB	[7:0]	User Pattern 3, Bits[15:8]		User Test Pattern 3 most significant byte.	0x0	R/W
0x0557	Pair map User Pattern 4 LSB	[7:0]	User Pattern 4, Bits[7:0]		User Test Pattern 4 least significant byte.	0x0	R/W
0x0558	Pair map User Pattern 4 MSB	[7:0]	User Pattern 4, Bits[15:8]		User Test Pattern 4 most significant byte.	0x0	R/W
0x0559	Pair map Output Control Mode 0	7	Reserved		Reserved.	0x0	R
		[6:4]	Converter Control Bit 1 selection			0x0	R/W
				000	Tie low (1'b0).		
				001	Overrange bit.		
				010	Signal monitor (SMON) bit.		
				011	Fast detect (FD) bit.		
				100	Reserved.		
				101	SYSREF±.		
				110	Reserved.		
				111	Reserved.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	Converter Control Bit 0 selection			0x0	R/W
				000	Tie low (1'b0).		
				001	Overrange bit.		
				010	Signal monitor (SMON) bit.		
				011	Fast detect (FD) bit.		

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
				101	SYSREF±.		
				100	Reserved.		
				110	Reserved.		
				111	Reserved.		
0x055A	Pair map Output Control Mode 1	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Converter control Bit 2 selection			0x1	R/W
				000	Tie low (1'b0).		
				001	Overrange bit.		
				010	Signal monitor (SMON) bit.		
				011	Fast detect (FD) bit.		
				100	Reserved.		
				101	SYSREF±.		
				110	Reserved.		
				111	Reserved.		
0x0561	Pair map output sample mode	[7:3]	Reserved		Reserved.	0x0	R
		2	Sample invert			0x0	R/W
				0	ADC sample data is not inverted.		
				1	ADC sample data is inverted.		
		[1:0]	Data format select			0x1	R/W
				00	Offset binary.		
				01	Twos complement (default).		
0x0564	Pair map output channel select	[7:2]	Reserved		Reserved.	0x0	R
		1	Reserved		Reserved.	0x0	R/W
		0	Converter channel swap control			0x0	R/W
				0	Normal channel ordering.		
				1	Channel swap enabled.		
0x056E	JESD204B map PLL control	[7:4]	JESD204B lane rate control			0x0	R/W
				0000	Lane rate = 6.75 Gbps to 13.5 Gbps.		
				0001	Lane rate = 3.375 Gbps to 6.75 Gbps.		
				0011	Lane rate = 13.5 Gbps to 15 Gbps.		
				0101	Lane rate = 1.6875 Gbps to 3.375 Gbps.		
		[3:0]	Reserved		Reserved.	0x0	R
0x056F	JESD204B map PLL STATUS	7	PLL lock status			0x0	R
				0	Not locked.		
				1	Locked.		
		[6:4]	Reserved		Reserved.	0x0	R
		3	Reserved		Reserved.	0x0	R
		[2:0]	Reserved		Reserved.	0x0	R
0x0570	JESD204B map JTX quick configuration	[7:6]	Quick Configuration L		Number of lanes (L) = $2^{0x0570[7:6]}$.	0x1	R/W
				0	L = 1.		
				1	L = 2.		
		[5:3]	Quick Configuration M		Number of converters (M) = $2^{0x0570[5:3]}$.	0x1	R/W
				0	M = 1.		
				1	M = 2.		
				10	M = 4.		
		[2:0]	Quick Configuration F		Number of octets/frame (F) = $2^{0x0570[2:0]}$.	0x1	R/W
				0	F = 1.		
				1	F = 2.		
				10	F = 4.		
				11	F = 8.		

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0571	JESD204B map JTX Link Control 1	7	Standby mode	0 1	Standby mode forces zeros for all converter samples. Standby mode forces code group synchronization (/K28.5/ characters).	0x0	R/W
		6	Tail bit (t) PN	0 1	Disable. Enable.	0x0	R/W
		5	Long transport layer test	0 1	JESD204B test samples disabled. JESD204B test samples enabled—long transport layer test sample sequence (as specified in JESD204B Section 5.1.6.3) sent on all link lanes.	0x0	R/W
		4	Lane synchronization	0 1	Disable FACI uses /K28.7/. Enable FACI uses /K28.3/ and /K28.7/.	0x1	R/W
		[3:2]	ILAS sequence mode	00 01 11	Initial lane alignment sequence disabled— (JESD204B 5.3.3.5). Initial lane alignment sequence enabled— (JESD204B 5.3.3.5). Initial lane alignment t sequence always on test mode—JESD204B data link layer test mode where repeated lane alignment sequence (as specified in JESD204B Section 5.3.3.8.2) sent on all lanes.	0x1	R/W
		1	FACI	0 1	Frame alignment character insertion enabled (JESD204B 5.3.3.4). Frame alignment character insertion disabled—for debug only (JESD204B 5.3.3.4).	0x0	R/W
		0	Link control	0 1	JESD204B serial transmit link enabled. Transmission of the /K28.5/ characters for code group synchronization is controlled by the SYNCINB±x pin. JESD204B serial transmit link powered down (held in reset and clock gated).	0x0	R/W
0x0572	JESD204B map JTX Link Control 2	[7:6]	SYNCINB±x pin control	00 10 11	Normal mode. Ignore SYNCINB±x (force CGS). Ignore SYNCINB±x (force ILAS/user data).	0x0	R/W
		5	SYNCINB±x pin invert	0 1	SYNCINB±x pin not inverted. SYNCINB±x pin inverted.	0x0	R/W
		4	SYNCINB±x pin type	0 1	LVDS differential pair SYNC~ input. CMOS single-ended SYNC~ input.	0x0	R/W
		3	Reserved		Reserved.	0x0	R

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		2	8-bit/10-bit bypass			0x0	R/W
				0	8-bit/10-bit enabled.		
				1	8-bit/10-bit bypassed (most significant two bits are 0).		
		1	8-bit/10-bit invert			0x0	R/W
				0	Normal.		
				1	Invert abcdefghij symbols.		
		0	Reserved		Reserved.	0x0	R/W
0x0573	JESD204B map JTX Link Control 3	[7:6]	Checksum mode			0x0	R/W
				00	Checksum is the sum of all 8-bit registers in the link configuration table.		
				01	Checksum is the sum of all individual link configuration fields (LSB aligned).		
				10	Checksum is disabled (set to zero). For test purposes only.		
				11	Unused.		
		[5:4]	Test injection point			0x0	R/W
				0	N' sample input.		
				1	10-bit data at 8-bit/10-bit output (for PHY testing).		
				10	8-bit data at scrambler input.		
		[3:0]	JESD204B test mode patterns			0x0	R/W
				0	Normal operation (test mode disabled).		
				1	Alternating checkerboard.		
				10	1/0 word toggle.		
				11	31-bit PN sequence: $x^{31} + x^{28} + 1$.		
				100	23-bit PN sequence: $x^{23} + x^{18} + 1$.		
				101	15-bit PN sequence: $x^{15} + x^{14} + 1$.		
				110	9-bit PN sequence: $x^9 + x^5 + 1$.		
				111	7-bit PN sequence: $x^7 + x^6 + 1$.		
				1000	Ramp output.		
				1110	Continuous/repeat user test.		
				1111	Single user test.		
0x0574	JESD204B map JTX Link Control 4	[7:4]	ILAS delay			0x0	R/W
				0	Transmit ILAS on first LMFC after SYNCINB±x is deasserted.		
				1	Transmit ILAS on second LMFC after SYNCINB±x is deasserted.		
				10	Transmit ILAS on third LMFC after SYNCINB±x is deasserted.		
				11	Transmit ILAS on fourth LMFC after SYNCINB±x is deasserted.		
				100	Transmit ILAS on fifth LMFC after SYNCINB±x is deasserted.		
				101	Transmit ILAS on sixth LMFC after SYNCINB±x is deasserted.		
				110	Transmit ILAS on seventh LMFC after SYNCINB±x is deasserted.		
				111	Transmit ILAS on eighth LMFC after SYNCINB±x is deasserted.		
				1000	Transmit ILAS on ninth LMFC after SYNCINB±x is deasserted.		
				1001	Transmit ILAS on 10th LMFC after SYNCINB±x is deasserted.		

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
				1010	Transmit ILAS on 11th LMFC after SYNCINB±x is deasserted.		
				1011	Transmit ILAS on 12th LMFC after SYNCINB±x is deasserted.		
				1100	Transmit ILAS on 13th LMFC after SYNCINB±x is deasserted.		
				1101	Transmit ILAS on 14th LMFC after SYNCINB± is deasserted.		
				1110	Transmit ILAS on 15th LMFC after SYNCINB±x is deasserted.		
				1111	Transmit ILAS on 16th LMFC after SYNCINB±x is deasserted.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	Link layer test mode			0x0	R/W
				000	Normal operation (link layer test mode disabled).		
				001	Continuous sequence of /D21.5/ characters.		
				010	Reserved.		
				011	Reserved.		
				100	Modified RPAT test sequence.		
				101	JSPAT test sequence.		
				110	JTSPAT test sequence.		
				111	Reserved.		
0x0578	JESD204B map JTX LMFC offset	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	LMFC phase offset value		Local multiframe clock (LMFC) phase offset value. Reset value for LMFC phase counter when SYSREF± is asserted. Used for deterministic delay applications.	0x0	R/W
0x0580	JESD204B map JTX DID configuration	[7:0]	JESD204B Tx DID value		JESD204x serial device identification (DID) number.	0x0	R/W
0x0581	JESD204B map JTX BID configuration	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	JESD204B Tx BID value		JESD204x serial bank identification (BID) number (extension to DID).	0x0	R/W
0x0583	JESD204B map JTX LID 0 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 0 LID value		JESD204x serial lane identification (LID) number for Lane 0.	0x0	R/W
0x0585	JESD204B map JTX LID 1 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 1 LID value		JESD204x serial lane identification (LID) number for Lane 1.	0x2	R/W
0x058B	JESD204B map JTX SCR L configuration	7	JESD204B scrambling (SCR)			0x1	R/W
				0	JESD204x scrambler disabled (SCR = 0).		
				1	JESD204x scrambler enabled (SCR = 1).		
		[6:5]	Reserved		Reserved.	0x0	R
		[4:0]	JESD204B lanes (L)			0x1	R
				0x0	One lane per link (L = 1).		
				0x1	Two lanes per link (L = 2).		
0x058C	JESD204B map JTX F configuration	[7:0]	Number of octets per frame (F)		Number of octets per frame, F = Register 0x058C, Bits[7:0] + 1.	0x1	R

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x058D	JESD204B map JTX K configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Number of frames per multiframe (K)		JESD204x number of frames per multiframe (K = Register 0x058D, Bits[4:0] + 1). Only values where F × K, which are divisible by 4, can be used.	0x1F	R/W
				00011	K = 4.		
				00111	K = 8.		
				01100	K = 12.		
				01111	K = 16.		
				10011	K = 20.		
				10111	K = 24.		
				11011	K = 28.		
				11111	K = 32.		
0x058E	JESD204B map JTX M configuration	[7:0]	Number of converters per link			0x1	R
				00000000	Link connected to one virtual converter (M = 1).		
				00000001	Link connected to two virtual converters (M = 2).		
				00000011	Link connected to four virtual converters (M = 4).		
0x058F	JESD204B map JTX CS N configuration	[7:6]	Number of control bits (CS) per sample			0x0	R/W
				00	No control bits (CS = 0).		
				01	One control bit (CS = 1), Control Bit 2 only.		
				10	Two control bits (CS = 2), Control Bit 2 and Control Bit 1 only.		
				11	Three control bits (CS = 3), all control bits (Control Bit 2, Control Bit 1, and Control Bit 0).		
		5	Reserved		Reserved.	0x0	R
		[4:0]	ADC converter resolution (N)			0xF	R/W
				00110	N = 7-bit resolution.		
				00111	N = 8-bit resolution.		
				01000	N = 9-bit resolution.		
				01001	N = 10-bit resolution.		
				01010	N = 11-bit resolution.		
				01011	N = 12-bit resolution.		
				01100	N = 13-bit resolution.		
				01101	N = 14-bit resolution.		
				01110	N = 15-bit resolution.		
				01111	N = 16-bit resolution.		
0x0590	JESD204B map JTX Subclass Version NP configuration	[7:5]	Subclass support			0x1	R/W
				000	Subclass 0.		
				001	Subclass 1.		
		[4:0]	ADC number of bits per sample (N')			0xF	R/W
				00111	N' = 8.		
				01111	N' = 16.		
0x0591	JESD204B map JTX S configuration	[7:5]	Reserved		Reserved.	0x1	R
		[4:0]	Samples per converter frame cycle (S)		Samples per converter frame cycle (S = Register 0x0591, Bits[4:0] + 1).	0x0	R

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0592	JESD204B map JTX HD CF configuration	7	HD value	0 1	High density format disabled. High density format enabled.	0x0	R
		[6:5]	Reserved		Reserved.	0x0	R
		[4:0]	Control words per frame clock cycle per link (CF)		Number of control words per frame clock cycle per link (CF = Register 0x0592, Bits[4:0]).	0x0	R
0x05A0	JESD204B map JTX Checksum 0 configuration	[7:0]	Checksum 0 checksum value for SERDOUTx0±		Serial checksum value for Lane 0. Automatically calculated for each lane. SUM(all link configuration parameters for Lane 0) % 256.	0xC3	R
0x05A1	JESD204B map JTX Checksum 1 configuration	[7:0]	Checksum 1 checksum value for SERDOUTx1±		Serial Checksum Value for Lane 1. Automatically calculated for each lane. SUM(all link configuration parameters for Lane 1) % 256.	0xC4	R
0x05B0	SERDOUTx0±/ SERDOUTx1± lane power-down	7	Reserved		Reserved.	0x1	R/W
		6	Reserved		Reserved.	0x1	R/W
		5	Reserved		Reserved.	0x1	R/W
		4	Reserved		Reserved.	0x1	R/W
		3	Reserved		Reserved.	0x1	R/W
		2	SERDOUTx1± Lane 1 power-down		Physical Lane 1 force power-down.	0x0	R/W
		1	Reserved		Reserved.	0x1	R/W
		0	SERDOUTx0± Lane 0 power-down		Physical Lane 0 force power-down.	0x0	R/W
0x05B2	JESD204B map JTX lane Assignment 1	7	Reserved		Reserved.	0x0	R
		[6:4]	Reserved		Reserved.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUTx0± lane assignment	0 1 10 11	Logical Lane 0 (default). Logical Lane 1. Logical Lane 2. Logical Lane 3.	0x0	R/W
0x05B3	JESD204B map JTX lane Assignment 2	7	Reserved		Reserved.	0x0	R
		[6:4]	Reserved		Reserved.	0x1	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUTx1± lane assignment	0 1 10 11	Logical Lane 0. Logical Lane 1 (default). Logical Lane 2. Logical Lane 3.	0x1	R/W
0x05C0	JESD204B map JESD204B serializer drive adjust	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Swing voltage SERDOUTx0±	0 1	1.0 × DRVDD1 (differential). 0.850 × DRVDD1 (differential).	0x1	R/W
0x05C1	JESD204B map JESD204B serializer drive adjust	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Swing voltage SERDOUTx1±	0 1	1.0 × DRVDD1 (differential). 0.850 × DRVDD1 (differential).	0x1	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x05C4	JESD204B serializer preemphasis selection register for Logical Lane 0	7	Post tap enable	0 1	Disable. Enable.	0x0	R/W
		[6:4]	Sets post tab level	0 1 10 11 100	0 dB (recommended when insertion loss = 0 dB to 4 dB when voltage swing setting is 0). 3 dB (recommended when insertion loss = 4 dB to 9 dB when voltage swing setting is 0). 6 dB (recommended when insertion loss = 9 dB to 14 dB when voltage swing setting is 0). 9 dB (recommended when insertion loss > 14 dB when voltage swing setting is 0). 12 dB.	0x0	R/W
		[3:0]	Reserved		Reserved.	0x0	R
0x05C6	JESD204B serializer preemphasis selection register for Logical Lane 1	7	Post tap polarity	0 1	Disable. Enable.	0x0	R/W
		[6:4]	Sets post tab level	0 1 10 11 100	0 dB (recommended when insertion loss = 0 dB to 4 dB when voltage swing setting is 0). 3 dB (recommended when insertion loss = 4 dB to 9 dB when voltage swing setting is 0). 6 dB (recommended when insertion loss = 9 dB to 14 dB when voltage swing setting is 0). 9 dB (recommended when insertion loss > 14 dB when voltage swing setting is 0). 12 dB.	0x0	R/W
		[3:0]	Reserved		Reserved.	0x0	R
0x0922	Large dither control	[7:0]	Large dither control	1110000 1110001	Enable. Disable.	0x70	R/W
0x1222	PLL calibration	[7:0]	PLL calibration	 0x00 0x04	PLL calibration. Normal operation. PLL calibration	0x0	R/W
0x1228	JESD204B start-up circuit reset	[7:0]	JESD204B start-up circuit reset	 0x0F 0x4F	JESD204B start-up circuit reset. Normal operation. Start-up circuit reset.	0xF	R/W
0x1262	PLL loss of lock control		PLL loss of lock control	 0x00 0x08	PLL loss of lock control. Normal operation. Clear loss of lock.	0x0	R/W
0x0701	DC offset calibration control	[7:0]	DC offset calibration control	0x06 0x86	Disable dc offset calibration. Enable dc offset calibration.	0x06	R/W
0x073B	DC Offset Calibration Control 2 (local)	7	DC Offset Calibration Enable 2	0 1	Enabled (must set to 0 when Register 0x0701, Bit 7 = 1). Disabled (must set to 1 when Register 0x0701, Bit 7 = 0).	0x1	R/W
		[6:0]	Reserved	111111	Reserved.	0x3F	R
0x18A6	Pair map VREF control	[7:5]	Reserved		Reserved.	0x0	R
		4	Reserved		Reserved.	0x0	R/W
		[3:1]	Reserved		Reserved.	0x0	R
		0	VREF control	0 1	Internal reference. External reference.	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x18E0	External V_{CM} Buffer Control 1	[7:0]	External V_{CM} Buffer Control 1		See the Input Common Mode section for details.	0x0	R/W
0x18E1	External V_{CM} Buffer Control 2	[7:0]	External V_{CM} Buffer Control 2		See the Input Common Mode section for details.	0x0	R/W
0x18E2	External V_{CM} Buffer Control 3	[7:0]	External V_{CM} Buffer Control 3		See the Input Common Mode section for details.	0x0	R/W
0x18E3	External V_{CM} buffer control	7	Reserved		Reserved.	0x0	R/W
		6	External V_{CM} buffer	1 0	Enable. Disable.	0x0	R/W
		[5:0]	External V_{CM} buffer current setting		See the Input Common Mode section for details.	0x0	R/W
0x18E6	Temperature diode export	[7:1]	Reserved		Reserved.	0x0	R/W
		0	Temperature diode export	1 0	Enable. Disable.	0x0	R/W
0x1908	Channel map analog input control	[7:6]	Reserved		Reserved.	0x0	R
		[5:4]	Reserved		Reserved.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		2	Analog input dc coupling control	 0 1	Analog input dc coupling control. AC coupling. DC coupling.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	Reserved		Reserved.	0x0	R/W
0x1910	Channel map input full-scale range	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Input full-scale control	0000 1010 1011 1100 1101 1110 1111 Reserved.	2.16 V p-p. 1.44 V p-p. 1.56 V p-p. 1.68 V p-p. 1.80 V p-p. 1.92 V p-p. 2.04 V p-p.	0xD	R/W
0x1A4C	Channel map Buffer Control 1	[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	Buffer Control 1	00110 01000 01010 01100 01110 10000 10010 10100 10110	120 µA. 160 µA. 200 µA. 240 µA. 280 µA. 320 µA. 360 µA. 400 µA. 440 µA.	0xC	R/W
0x1A4D	Channel map Buffer Control 2	[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	Buffer Control 2	00110 01000 01010 01100 01110 10000 10010 10100 10110	120 µA. 160 µA. 200 µA. 240 µA. 280 µA. 320 µA. 360 µA. 400 µA. 440 µA.	0xC	R/W

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

The AD9694 must be powered by the following seven supplies: AVDD1 = AVDD1_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, and SPIVDD = 1.8 V. For applications requiring an optimal high power efficiency and low noise performance, it is recommended that the ADP5054 quad switching regulator be used to convert the 6.0 V or 12 V input rails to intermediate rails (1.3 V, 2.4 V, and 3.0 V). These intermediate rails are then postregulated by very low noise, low dropout (LDO) regulators (such as the ADP1762, ADP7159, ADP151, and ADP7118). Figure 106 shows the recommended power supply scheme for AD9694.

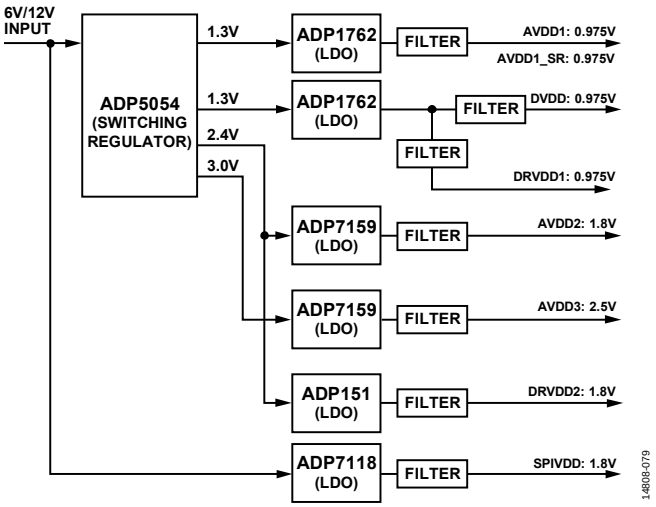

Figure 106. High Efficiency, Low Noise Power Solution for the AD9694

It is not necessary to split all of these power domains in all cases. The recommended solution shown in Figure 106 provides the lowest noise, highest efficiency power delivery system for the AD9694. If only one 0.975 V supply is available, route to AVDD1 first and then tap it off and isolate it with a ferrite bead or a filter choke, preceded by decoupling capacitors for AVDD1_SR, DVDD, and DRVDD1, in that order. The user can employ several different decoupling capacitors to cover both high and low frequencies. These capacitors must be placed close to the point of entry at the PCB level and close to the devices, with minimal trace lengths.

EXPOSED PAD THERMAL HEAT SLUG RECOMMENDATIONS

It is required that the exposed pad on the underside of the ADC be connected to AGND to achieve the best electrical and thermal performance of the AD9694. Connect an exposed continuous copper plane on the PCB to the AD9694 exposed pad, Pin 0. The copper plane must have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias must be solder filled or plugged. The number of vias and the fill determine the resultant θ_{JA} measured on the board, which is shown in Table 9.

See Figure 107 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

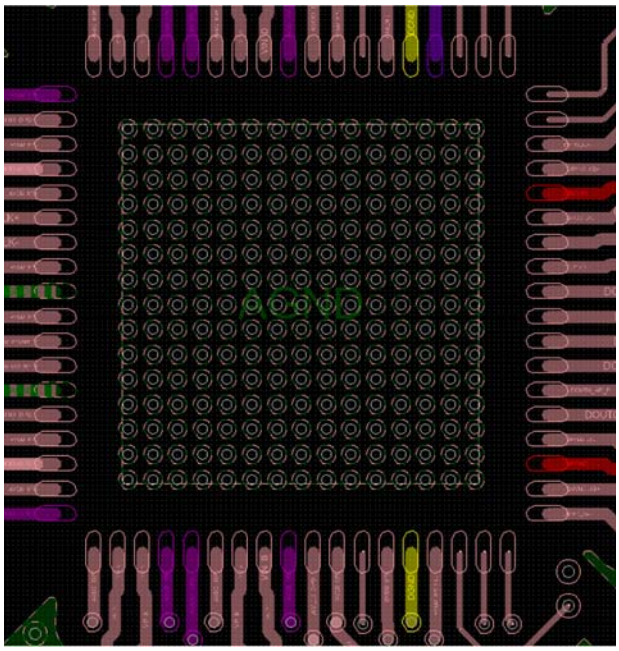

Figure 107. Recommended PCB Layout of Exposed Pad for the AD9694

AVDD1_SR (PIN 64) AND AGND_SR (PIN 63 AND PIN 67)

AVDD1_SR (Pin 64) and AGND_SR (Pin 63 and Pin 67) can provide a separate power supply node to the SYSREF± circuits of AD9694. If running in Subclass 1, the AD9694 can support periodic one-shot or gapped signals. To minimize the coupling of this supply into the AVDD1 supply node, adequate supply bypassing is required.

OUTLINE DIMENSIONS

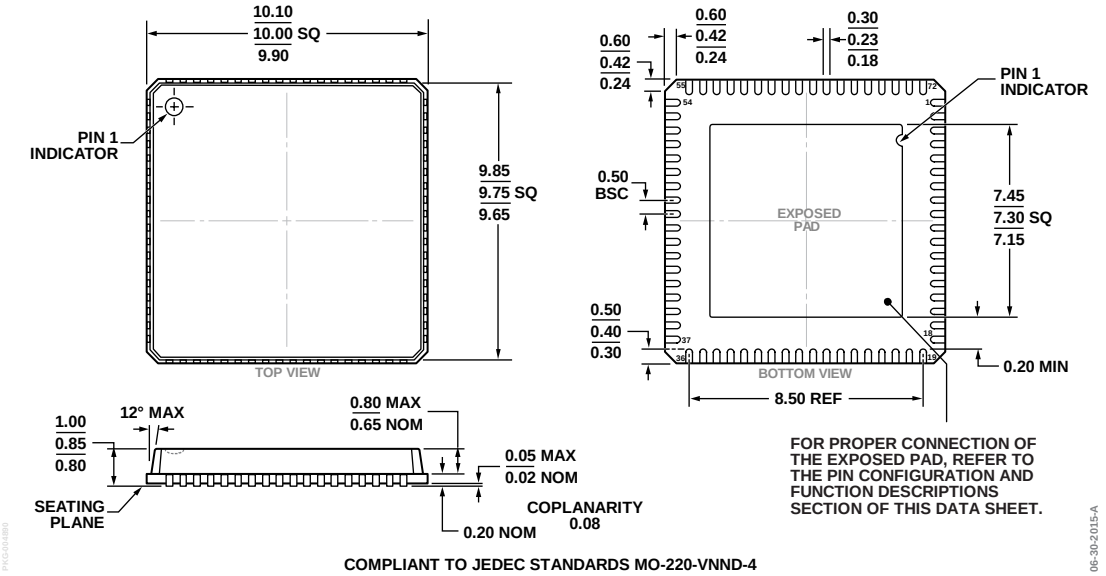

Figure 108. 72-Lead Lead Frame Chip Scale Package [LFCSP]
10 mm × 10 mm Body and 0.85 mm Package Height
(CP-72-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Junction Temperature Range	Package Description	Package Option
AD9694BCPZ-500	−40°C to +105°C	72-Lead Lead Frame Chip Scale Package [LFCSP]	CP-72-10
AD9694BCPZRL7-500	−40°C to +105°C	72-Lead Lead Frame Chip Scale Package [LFCSP]	CP-72-10
AD9694-500EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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