30 V, Low Noise, Rail-to-Rail Input/Output, Low Power Operational Amplifiers

Data Sheet

ADA4084-1/ADA4084-2/ADA4084-4

FEATURES

Rail-to-rail input/output
Low power: 0.625 mA typical per amplifier at ±15 V
Gain bandwidth product: 15.9 MHz at A_V = 100 typical
Unity-gain crossover: 9.9 MHz typical
−3 dB closed-loop bandwidth: 13.9 MHz typical at ±15 V
Low offset voltage: 100 µV maximum (SOIC)
Unity-gain stable
High slew rate: 4.6 V/µs typical
Low noise: 3.9 nV/√Hz typical at 1 kHz
Long-term offset voltage drift (10,000 hours): 3 µV typical
Temperature hysteresis: 4 µV typical

APPLICATIONS

Battery-powered instrumentation
High-side and low-side sensing
Power supply control and protection
Telecommunications
Digital-to-analog converter (DAC) output amplifiers
Analog-to-digital converter (ADC) input buffers

PIN CONNECTION DIAGRAM

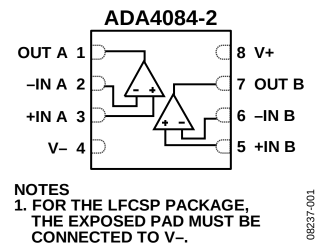

Figure 1. ADA4084-2, 8-Lead LFCSP (CP); for Additional Packages and Models, See the Pin Configurations and Function Descriptions Section

GENERAL DESCRIPTION

The ADA4084-1 (single), ADA4084-2 (dual), and ADA4084-4 (quad) are single-supply, 10 MHz bandwidth amplifiers featuring rail-to-rail inputs and outputs. They are guaranteed to operate from +3 V to +30 V (or ±1.5 V to ±15 V).

These amplifiers are well suited for single-supply applications requiring both ac and precision dc performance. The combination of wide bandwidth, low noise, and precision makes the ADA4084-1/ADA4084-2/ADA4084-4 useful in a wide variety of applications, including filters and instrumentation.

Other applications for these amplifiers include portable telecom-munications equipment, power supply control and protection, and use as amplifiers or buffers for transducers with wide output ranges. Sensors requiring a rail-to-rail input amplifier include Hall effect, piezoelectric, and resistive transducers.

The ability to swing rail to rail at both the input and output enables designers to build multistage filters in single-supply systems and to maintain high signal-to-noise ratios.

The ADA4084-1/ADA4084-2/ADA4084-4 are specified over the industrial temperature range of −40°C to +125°C.

The single ADA4084-1 is available in the 5-lead SOT-23 and 8-lead SOIC; the dual ADA4084-2 is available in the 8-lead SOIC, 8-lead MSOP, and 8-lead LFCSP surface-mount packages; and the ADA4084-4 is offered in the 14-lead TSSOP and 16-lead LFCSP.

The ADA4084-1/ADA4084-2/ADA4084-4 are members of a growing series of high voltage, low noise op amps offered by Analog Devices, Inc. (see Table 1).

Table 1. Low Noise Op Amps

Single	Dual	Quad	Voltage Noise
AD8597	AD8599		1.1 nV/Hz
ADA4004-1	ADA4004-2	ADA4004-4	1.8 nV/Hz
AD8675	AD8676		2.8 nV/Hz rail-to-rail output
AD8671	AD8672	AD8674	2.8 nV/Hz
OP27, OP37			3.2 nV/Hz
ADA4084-1	ADA4084-2	ADA4084-4	3.9 nV/Hz rail-to-rail input/output

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TABLE OF CONTENTS

REVISION HISTORY

5/2017—Rev. H to Rev. I

Changed CP-8-12 to CP-8-11 ... Throughout
Changed CP-16-26 to CP-16-17 ... Throughout
Changes to Features Section ... 1
Added Long-Term Drift Section, Temperature Hysteresis Section, Figure 112, Figure 113, and Figure 114; Renumbered Sequentially ... 32
Updated Outline Dimensions ... 34
Changes to Ordering Guide ... 36

8/2015—Rev. G to Rev. H

Added 5-Lead SOT-23 ... Universal
Changes to Pin Connection Diagram Section, Figure 1, and General Description Section ... 1
Deleted Figure 3; Renumbered Sequentially ... 1
Changes to Large Signal Voltage Gain Parameter, Table 2 ... 4
Changes to Large Signal Voltage Gain Parameter, Table 3 ... 5
Changes to Large Signal Voltage Gain Parameter, Table 4 ... 6
Changes to Table 6 ... 7
Moved Figure 3 ... 8
Added Pin Configurations and Function Descriptions Section, Figure 4, Figure 5, Table 7, Table 8, and Table 9; Renumbered Sequentially ... 8
Added Figure 6, Figure 7, Figure 8, Table 10, and Table 11 ... 9
Moved Figure 9 ... 10
Added Table 12 ... 10
Added Figure 11 and Figure 15 ... 11
Added Figure 42 and Figure 46 ... 17
Added Figure 73 and Figure 77 ... 23
Updated Outline Dimensions ... 32
Changes to Ordering Guide ... 35

6/2015—Rev. F to Rev. G

Changes to Figure 96 and Figure 97 ... 24

1/2015—Rev. E to Rev. F

Moved Revision History ... 3
Changes to Table 5 ... 7
Changes to Ordering Guide ... 29

7/2014—Rev. D to Rev. E

Added ADA4084-1 ... Universal
Added Figure 1; Renumbered Sequentially ... 1
Changes to Output Voltage High Parameter, Table 2 ... 3
Changes to Current Noise Density Parameter, Table 3 ... 4
Changes to Current Noise Density Parameter, Table 4 ... 5
Changes to Figure 8 Caption, and Figure 9 to Figure 11 ... 7
Changes to Figure 13 ... 8
Changes to Figure 21 ... 9
Added Figure 31; Renumbered Sequentially ... 11
Changes to Figure 30 Caption, and Figure 32 to Figure 34 ... 11
Changes to Figure 36 Caption to Figure 39 Caption ... 12
Changes to Figure 50 ... 14
Added Figure 60 ... 16
Changes to Figure 59 Caption, Figure 62, and Figure 63 ... 16
Changes to Figure 65 Caption to Figure 68 Caption ... 17
Changes to Figure 79 ... 19
Added Figure 89 ... 21
Changes to Figure 88 Caption, Figure 91 Caption, and Figure 92 Caption ... 21
Changes to Ordering Guide ... 28

11/2013—Rev. C to Rev. D

Added 14-Lead TSSOP and 16-Lead LFCSP Packages....... Universal
Added ADA4084-4.. Universal
Change to Features Section and Applications Section 1
Added Figure 2 and Figure 3; Renumbered Sequentially 1
Changes to Table 2 3
Changes to Table 3 4
Changes to Table 4 5
Changes to Table 5 and Table 6 6
Changes to Typical Performance Characteristics Section 7
Updated Outline Dimensions 27
Changes to Ordering Guide 28

4/2013—Rev. B to Rev. C

Changes to Figure 48 Caption 15
Updated Outline Dimensions 25

6/2012—Rev. A to Rev. B

Added LFCSP Package.. Universal
Changes to Figure 1 1
Changes to Output Voltage High Parameter, Table 4 5
Added Figure 5 and Figure 7, Renumbered Sequentially 7
Added Figure 30 and Figure 32 12
Added Figure 55 and Figure 57 17
Added Startup Characteristics Section 23
Moved Figure 78 23
Changes to Output Phase Reversal Section and Comparator Operation Section 24
Updated Outline Dimensions 25
Changes to Ordering Guide 26

2/2012—Rev. 0 to Rev. A

Changes to Data Sheet Title 1
Changes to Voltage Range in General Description 1
Changes to Supply Current/Amplifier Parameter, Table 2 3
Changes to Common-Mode Rejection Ratio Parameter, Table 3 .. 4
Changes to Common-Mode Rejection Ratio Parameter, Table 4 .. 5
Changes to Figure 2 6
Changes to Figure 24 10
Changes to Figure 32 12
Changes to Figure 47 14
Changes to Figure 55 16
Changes to Figure 62 17
Changes to Figure 73 20

10/2011—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{SY} = 3 V, V_{CM} = 1.5 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	SOIC package		20	100	µV
		−40°C ≤ T_A ≤ +125°C			200	µV
		SOT-23, MSOP, TSSOP packages		50	130	µV
		−40°C ≤ T_A ≤ +125°C			250	µV
		ADA4084-2 LFCSP package		80	200	µV
		−40°C ≤ T_A ≤ +125°C			300	µV
Offset Voltage Drift	Δt/ΔT	−40°C ≤ T_A ≤ +125°C		0.5	1.75	µV/°C
Offset Voltage Matching		T_A = 25°C			150	µV
		ADA4084-4 LFCSP package			200	µV
Input Bias Current	I_B			140	250	nA
		−40°C ≤ T_A ≤ +125°C			400	nA
Input Offset Current	I_{OS}			5	25	nA
		−40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3 V	64	88		dB
		−40°C ≤ T_A ≤ +125°C	60			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.5 V ≤ V_{OUT} ≤ 2.5 V	100	104		dB
		−40°C ≤ T_A ≤ +125°C	97			dB
Input Impedance						
Differential				100‖1.1		kΩ‖pF
Common Mode				80‖2.9		MΩ‖pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	2.90	2.95		V
		−40°C ≤ T_A ≤ +125°C	2.80			V
		R_L = 2 kΩ to V_{CM}	2.85	2.9		V
		−40°C ≤ T_A ≤ +125°C	2.70			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		10	20	mV
		−40°C ≤ T_A ≤ +125°C			40	mV
		R_L = 2 kΩ to V_{CM}		20	30	mV
		−40°C ≤ T_A ≤ +125°C			50	mV
Short-Circuit Current	I_{SC}			−17/+10		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = 1		0.1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±1.25 V to ±1.75 V	100	110		dB
		−40°C ≤ T_A ≤ +125°C	90			dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA		0.565	0.650	mA
		−40°C ≤ T_A ≤ +125°C			0.950	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	2.0	2.6		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		15.4		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		8.08		MHz
Phase Margin	$Φ_M$			86		Degrees
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = 1, V_{IN} = 5 mV p-p		12.3		MHz
Settling Time	t_S	A_V = 10, V_{IN} = 2 V p-p, 0.1%		4		µs
Total Harmonic Distortion Plus Noise	THD + N	V_{IN} = 300 mV rms, R_L = 2 kΩ, f = 1 kHz		0.009		%
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.14		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		3.9		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.55		pA/√Hz

V_{SY} = ±5.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	SOIC package		30	100	μV
		−40°C ≤ T_A ≤ +125°C			200	μV
		SOT-23, MSOP, TSSOP packages		60	130	μV
		−40°C ≤ T_A ≤ +125°C			250	μV
		ADA4084-2 LFCSP package		90	200	μV
		−40°C ≤ T_A ≤ +125°C			300	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.5	1.75	μV/°C
Offset Voltage Matching		T_A = 25°C			150	μV
		ADA4084-4 LFCSP package			200	μV
Input Bias Current	I_B			140	250	nA
		−40°C ≤ T_A ≤ +125°C			400	nA
Input Offset Current	I_{OS}			5	25	nA
		−40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			−5		+5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±4 V, −40°C ≤ T_A ≤ +125°C	106	124		dB
		V_{CM} = ±5 V	76			dB
		V_{CM} = ±5 V, −40°C ≤ T_A ≤ +125°C	70			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, −4 V ≤ V_{OUT} ≤ 4 V	108	112		dB
		−40°C ≤ T_A ≤ +125°C	103			dB
Input Impedance						
Differential				100‖1.1		kΩ‖pF
Common Mode				200‖2.5		MΩ‖pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	4.9	4.95		V
		−40°C ≤ T_A ≤ +125°C	4.8			V
		R_L = 2 kΩ to V_{CM}	4.8	4.85		V
		−40°C ≤ T_A ≤ +125°C	4.7			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		−4.95	−4.9	V
		−40°C ≤ T_A ≤ +125°C			−4.8	V
		R_L = 2 kΩ to V_{CM}		−4.95	−4.8	V
		−40°C ≤ T_A ≤ +125°C			−4.7	V
Short-Circuit Current	I_{SC}			−24/+17		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = 1		0.1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±2 V to ±18 V	110	120		dB
		−40°C ≤ T_A ≤ +125°C	105			dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA		0.595	0.700	mA
		−40°C ≤ T_A ≤ +125°C			1.00	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ to V_{CM}	2.4	3.7		V/μs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		15.9		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		9.6		MHz
Phase Margin	Φ_M			85		Degrees
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = 1, V_{IN} = 5 mV p-p		13.9		MHz
Settling Time	t_S	A_V = 10, V_{IN} = 8 V p-p, 0.1%		4		μs
Total Harmonic Distortion Plus Noise	THD + N	V_{IN} = 2 V rms, R_L = 2 kΩ, f = 1 kHz		0.003		%
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.14		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		3.9		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.55		pA/√Hz

V_{SY} = ±15.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	SOIC package		40	100	µV
		−40°C ≤ T_A ≤ +125°C			200	µV
		SOT-23, MSOP, TSSOP packages		70	130	µV
		−40°C ≤ T_A ≤ +125°C			250	µV
		ADA4084-2 LFCSP package		100	200	µV
		−40°C ≤ T_A ≤ +125°C			300	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.5	1.75	µV/°C
Offset Voltage Matching		T_A = 25°C			150	µV
		ADA4084-4 LFCSP package			200	µV
Input Bias Current	I_B			140	250	nA
		−40°C ≤ T_A ≤ +125°C			400	nA
Input Offset Current	I_{OS}			5	25	nA
		−40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			−15		+15	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±14 V, −40°C ≤ T_A ≤ +125°C	106	124		dB
		V_{CM} = ±15 V	85			dB
		V_{CM} = ±15 V, −40°C ≤ T_A ≤ +125°C	80			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, −13.5 V ≤ V_{OUT} ≤ +13.5 V	110	117		dB
		−40°C ≤ T_A ≤ +125°C	105			dB
Input Impedance						
Differential				100‖1.1		kΩ‖pF
Common Mode				200‖2.5		MΩ‖pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	14.85	14.9		V
		−40°C ≤ T_A ≤ +125°C	14.8			V
		R_L = 2 kΩ to V_{CM}	14.5	14.6		V
		−40°C ≤ T_A ≤ +125°C	14.0			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		−14.95	−14.9	V
		−40°C ≤ T_A ≤ +125°C			−14.8	V
		R_L = 2 kΩ to V_{CM}		−14.9	−14.8	V
		−40°C ≤ T_A ≤ +125°C			−14.7	V
Short-Circuit Current	I_{SC}			±30		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +1		0.1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±2 V to ±18 V	110	120		dB
		−40°C ≤ T_A ≤ +125°C	105			dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA		0.625	0.750	mA
		−40°C ≤ T_A ≤ +125°C			1.050	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	2.4	4.6		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		15.9		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		9.9		MHz
Phase Margin	Φ_M			86		Degrees
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = 1, V_{IN} = 5 mV p-p		13.9		MHz
Settling Time	t_S	A_V = 10, V_{IN} = 10 V p-p, 0.1%		4		µs
Total Harmonic Distortion Plus Noise	THD + N	V_{IN} = 5 V rms, R_L = 2 kΩ, f = 1 kHz		0.003		%
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.1		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		3.9		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.55		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	$V- \leq V_{IN} \leq V+$
Differential Input Voltage[1]	±0.6 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C
ESD	
Human Body Model[2]	4.5 kV
Machine Model[3]	200 V
Field-Induced Charged-Device Model (FICDM)[4]	1.25 kV

[1] For input differential voltages greater than 0.6 V, limit the input current to less than 5 mA to prevent degradation or destruction of the input devices.
[2] Applicable standard: MIL-STD-883, Method 3015.7.
[3] Applicable standard: JESD22-A115-A (ESD machine model standard of JEDEC).
[4] Applicable standard: JESD22-C101-C (ESD FICDM standard of JEDEC).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device soldered on a 4-layer JEDEC standard printed circuit board (PCB) with zero airflow.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead SOT-23 (RJ-5)	219.4	155.6	°C/W
8-Lead SOIC_N (R-8)	121	43	°C/W
8-Lead MSOP (RM-8)	142	45	°C/W
8-Lead LFCSP (CP-8-11)[1, 3]	84	40	°C/W
14-Lead TSSOP (RU-14)	112	43	°C/W
16-Lead LFCSP (CP-16-17)[2, 3]	55	30	°C/W

[1] Values are based on 4-layer (2S2P) JEDEC standard PCB, with four thermal vias. Exposed pad soldered to PCB.
[2] Values are based on 4-layer (2S2P) JEDEC standard PCB, with nine thermal vias. Exposed pad soldered to PCB.
[3] θ_{JC} measured on top of package.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

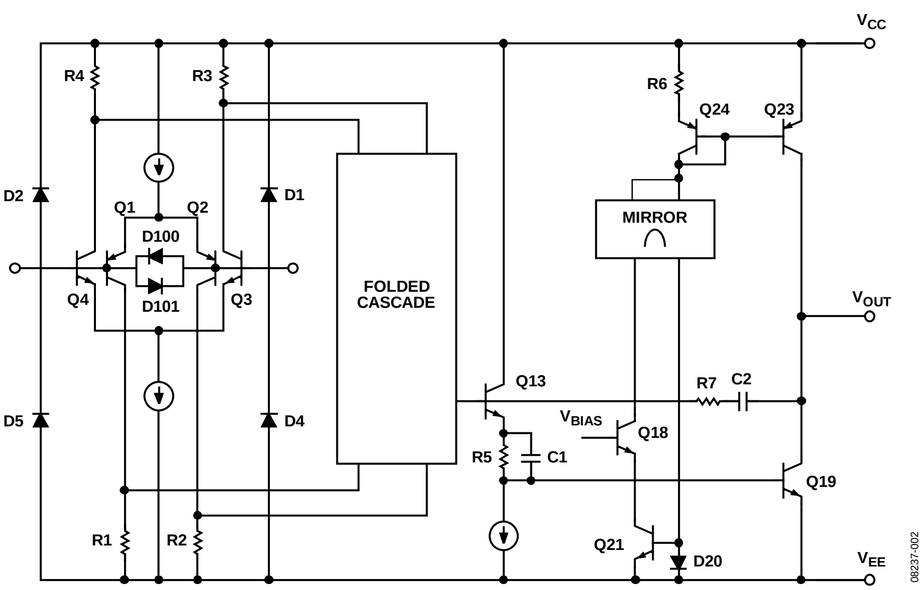

Figure 2. Simplified Schematic

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

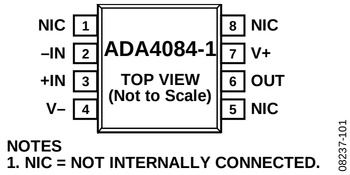

Figure 3. ADA4084-1, 8-Lead SOIC (R)

Table 7. 8-Lead SOIC, ADA4084-1 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NIC	Not Internally Connected
2	−IN	Negative Input
3	+IN	Positive Input
4	V−	Negative Supply
5	NIC	Not Internally Connected
6	OUT	Output
7	V+	Positive Supply
8	NIC	Not Internally Connected

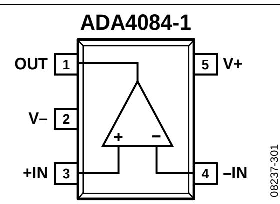

Figure 4. ADA4084-1, 5-Lead SOT-23 (RJ)

Table 8. 5-Lead SOT-23, ADA4084-1 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT	Output
2	V−	Negative Supply
3	+IN	Positive Input
4	−IN	Negative Input
5	V+	Positive Supply

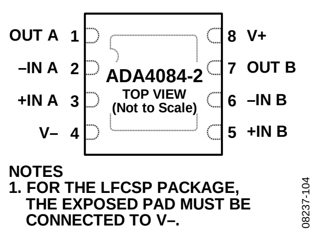

Figure 5. ADA4084-2, 8-Lead LFCSP (CP)

Table 9. 8-Lead LFCSP, ADA4084-2 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A
2	−IN A	Negative Input, Channel A
3	+IN A	Positive Input, Channel A
4	V−	Negative Supply
5	+IN B	Positive Input, Channel B
6	−IN B	Negative Input, Channel B
7	OUT B	Output, Channel B
8	V+	Positive Supply
	EPAD	Exposed Pad. For the LFCSP package, the exposed pad must be connected to V−.

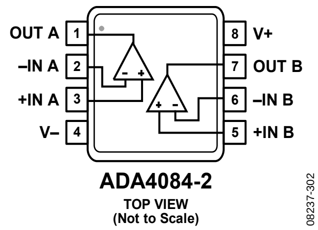

Figure 6. ADA4084-2, 8-Lead MSOP (RM)

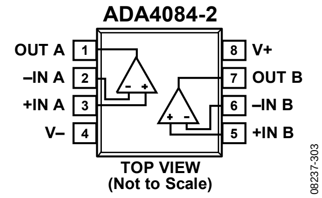

Figure 7. ADA4084-2, 8-Lead SOIC (R)

Table 10. 8-Lead MSOP, 8-Lead SOIC, ADA4084-2 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A
2	−IN A	Negative Input, Channel A
3	+IN A	Positive Input, Channel A
4	V−	Negative Supply
5	+IN B	Positive Input, Channel B
6	−IN B	Negative Input, Channel B
7	OUT B	Output, Channel B
8	V+	Positive Supply B

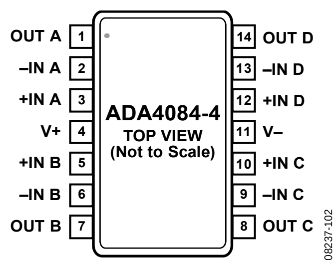

Figure 8. ADA4084-4, 14-Lead TSSOP (RU)

Table 11. 14-Lead TSSOP, ADA4804-4 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A
2	−IN A	Negative Input, Channel A
3	+IN A	Positive Input, Channel A
4	V+	Positive Supply
5	+IN B	Positive Input, Channel B
6	−IN B	Negative Input, Channel B
7	OUT B	Output, Channel B
8	OUT C	Output, Channel C
9	−IN C	Negative Input, Channel C
10	+IN C	Positive Input, Channel C
11	V−	Negative Supply
12	+IN D	Positive Input, Channel D
13	−IN D	Negative Input, Channel D
14	OUT D	Output, Channel D

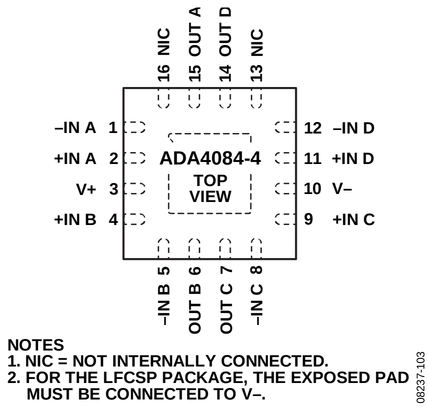

Figure 9. ADA4084-4, 16-Lead LFCSP (CP)

Table 12. 16-Lead LFCSP, ADA4084-4 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	–IN A	Negative Input Channel A
2	+IN A	Positive Input, Channel A
3	V+	Positive Supply
4	+IN B	Positive Input, Channel B
5	–IN B	Negative Input, Channel B
6	OUT B	Output, Channel B
7	OUT C	Output, Channel C
8	–IN C	Negative Input, Channel C
9	+IN C	Positive Input, Channel C
10	V–	Negative Supply
11	+IN D	Positive Input, Channel D
12	–IN D	Negative Input, Channel D
13	NIC	Not Internally Connected
14	OUT D	Output, Channel D
15	OUT A	Output, Channel A
16	NIC	Not Internally Connected

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

±1.5 V CHARACTERISTICS

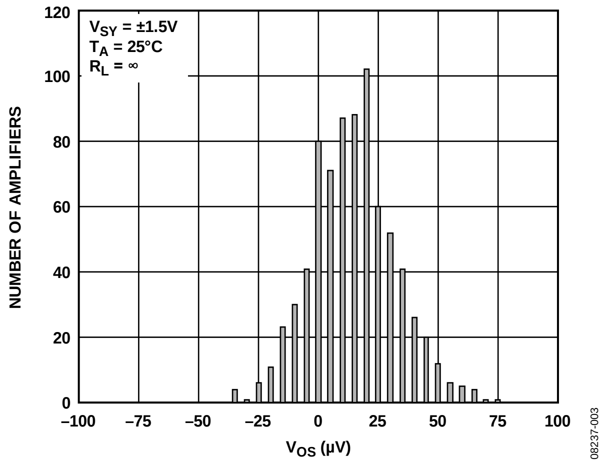

Figure 10. Input Offset Voltage (V_{OS}) Distribution, SOIC

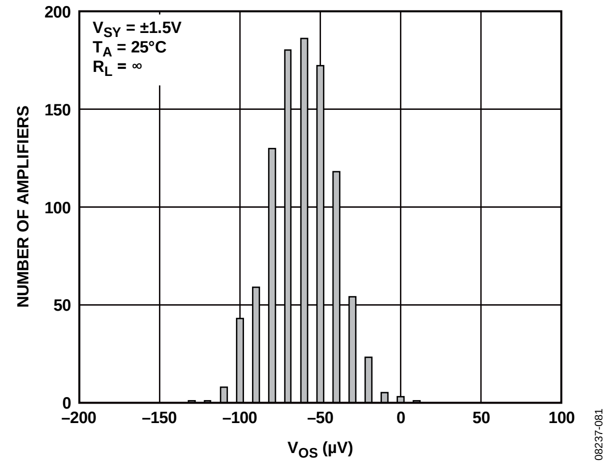

Figure 13. Input Offset Voltage (V_{OS}) Distribution, LFCSP

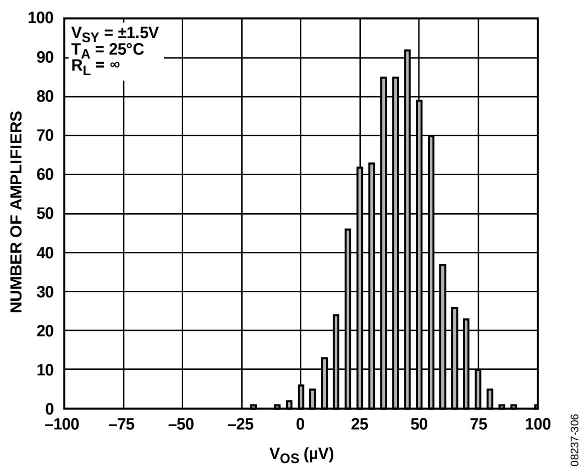

Figure 11. Input Offset Voltage (V_{OS}) Distribution, SOT-23

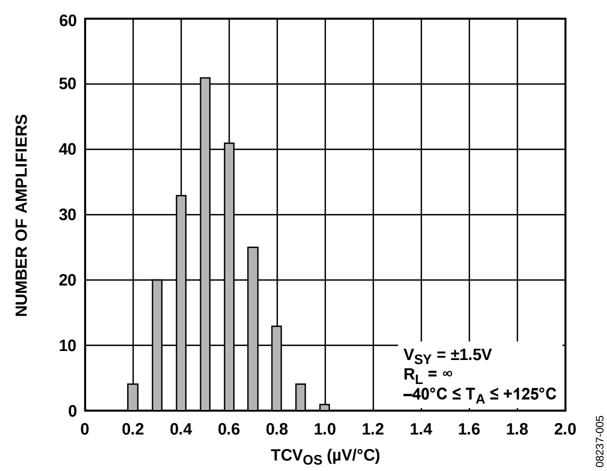

Figure 14. TCV_{OS} Distribution, SOIC, MSOP, and TSSOP

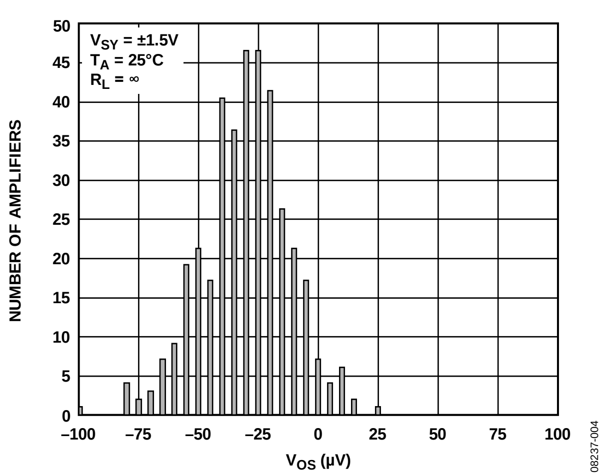

Figure 12. Input Offset Voltage (V_{OS}) Distribution, MSOP and TSSOP

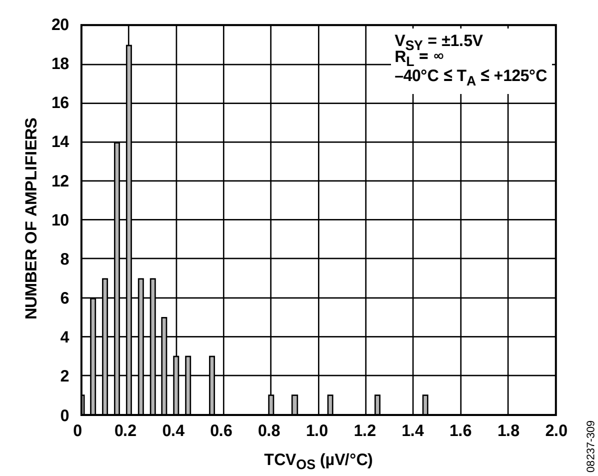

Figure 15. TCV_{OS} Distribution, SOT-23

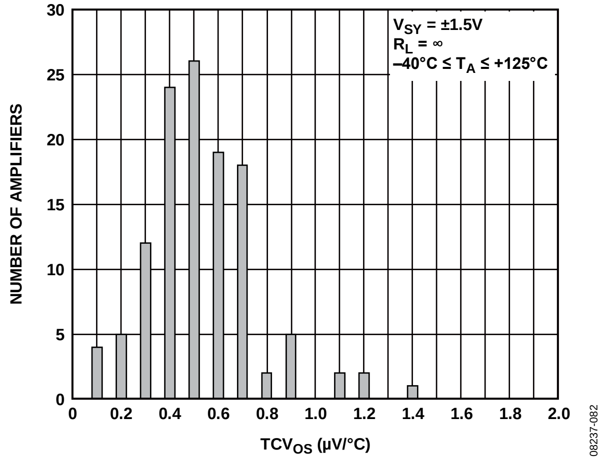

Figure 16. TCV_{OS} Distribution, LFCSP

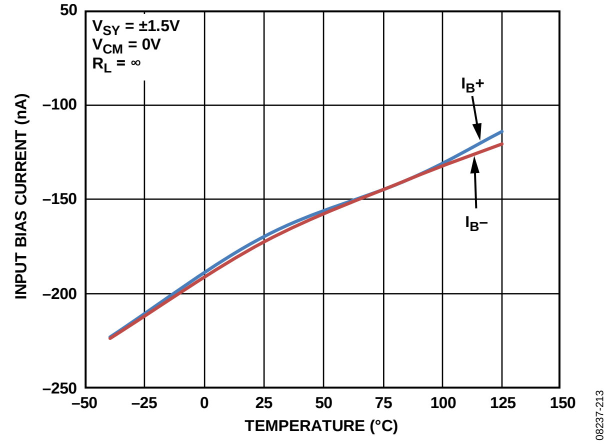

Figure 19. Input Bias Current vs. Temperature

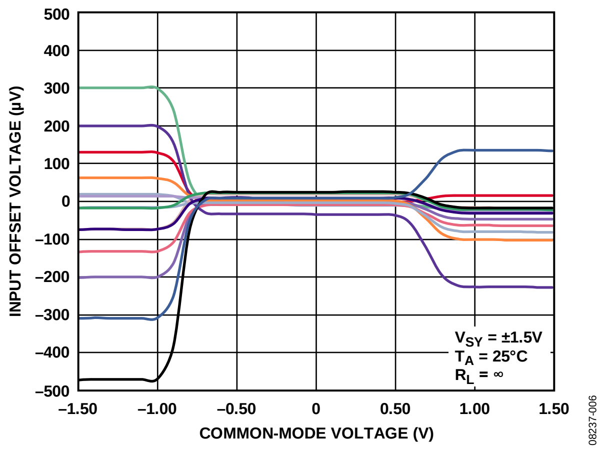

Figure 17. Input Offset Voltage vs. Common-Mode Voltage

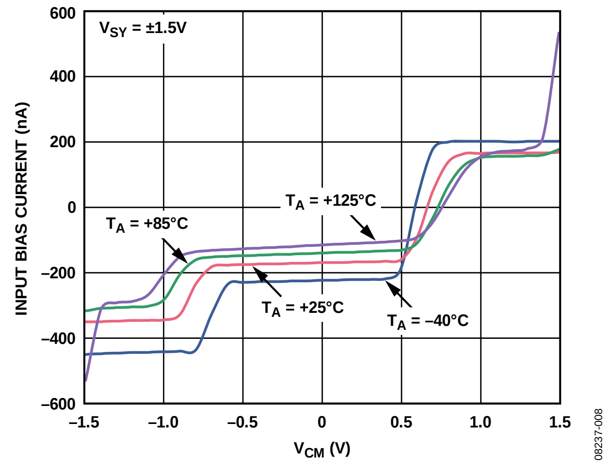

Figure 20. Input Bias Current vs. V_{CM} for Various Temperatures

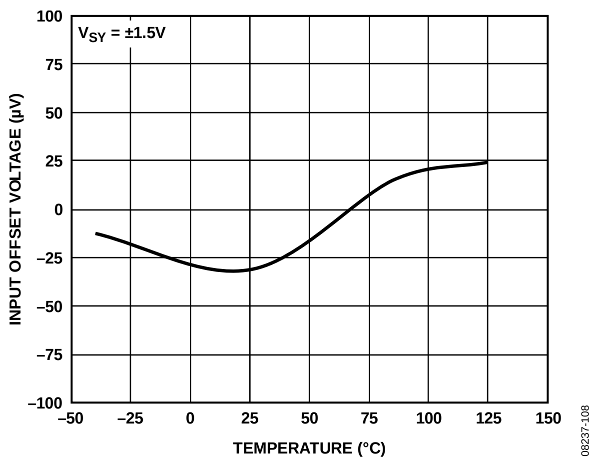

Figure 18. Input Offset Voltage vs. Temperature

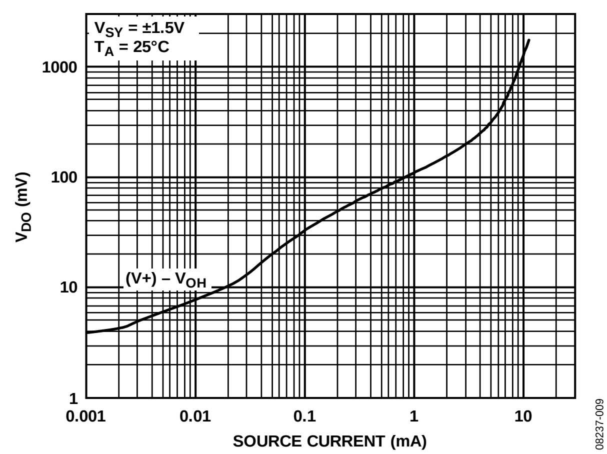

Figure 21. Dropout Voltage (V_{DO}) vs. Source Current

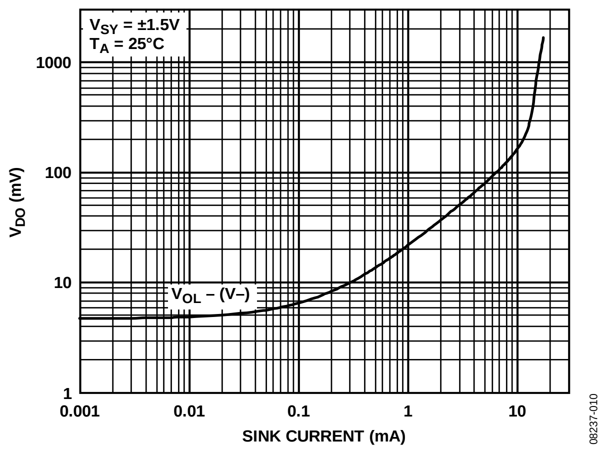

Figure 22. Dropout Voltage (V_{DO}) vs. Sink Current

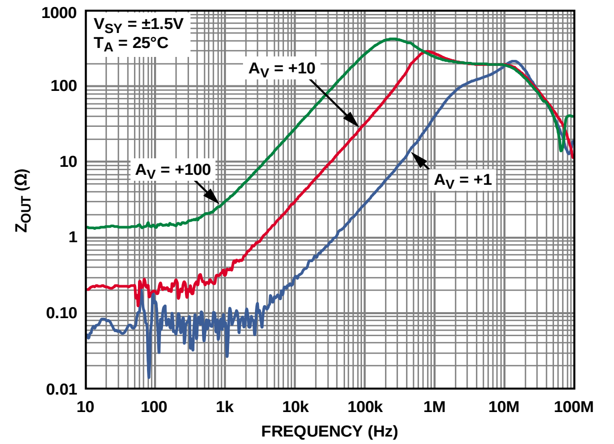

Figure 25. Output Impedance (Z_{OUT}) vs. Frequency

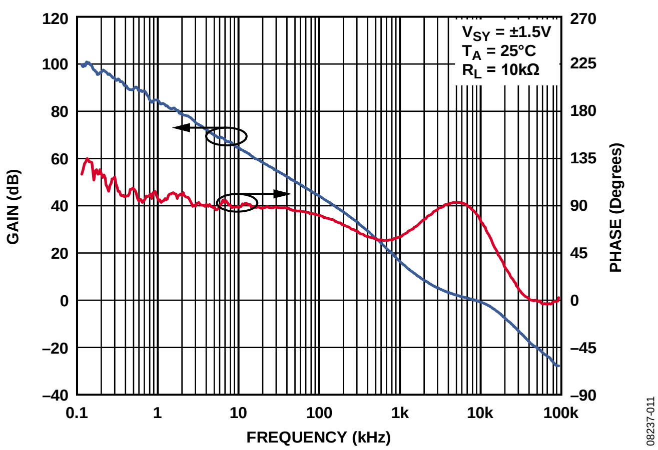

Figure 23. Open-Loop Gain and Phase vs. Frequency

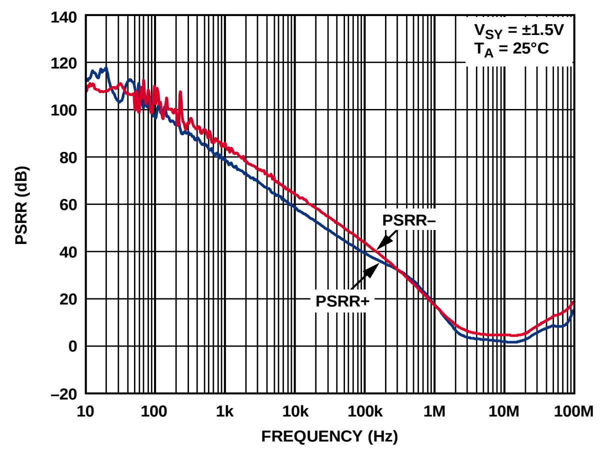

Figure 26. PSRR vs. Frequency

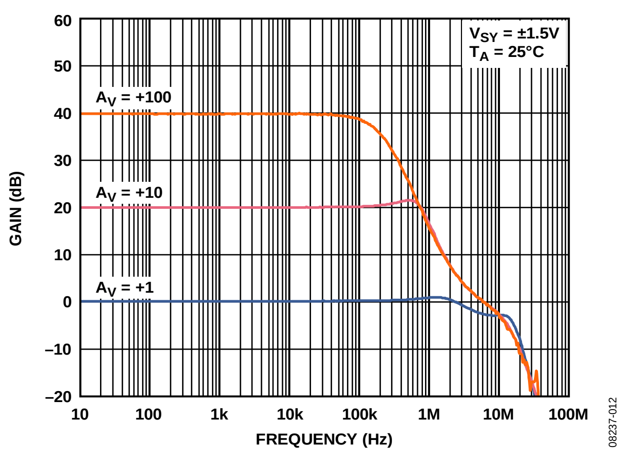

Figure 24. Closed-Loop Gain vs. Frequency

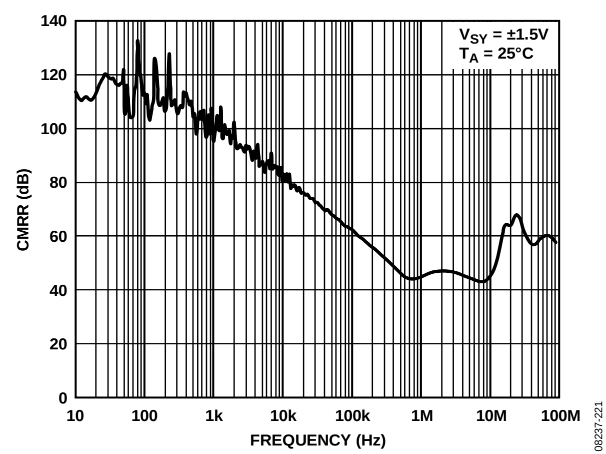

Figure 27. CMRR vs. Frequency

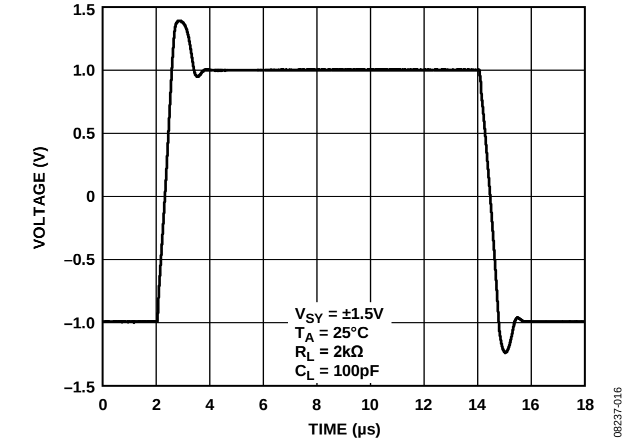

Figure 28. Large Signal Transient Response

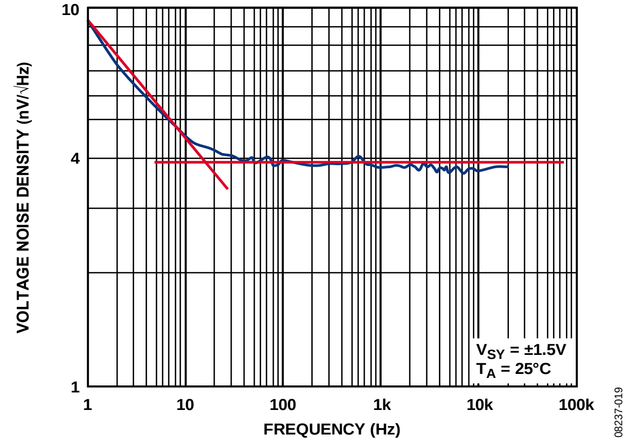

Figure 31. Voltage Noise Density vs. Frequency

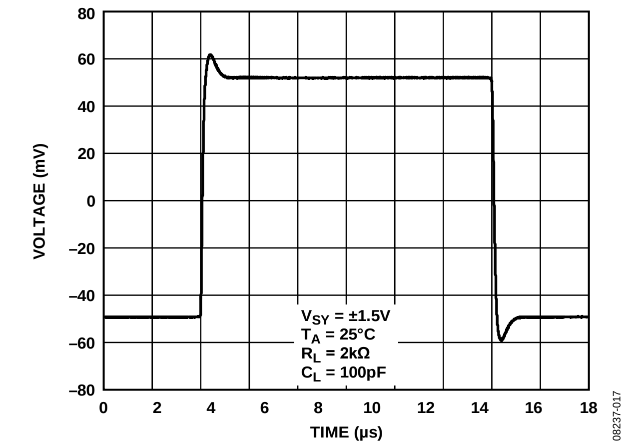

Figure 29. Small Signal Transient Response

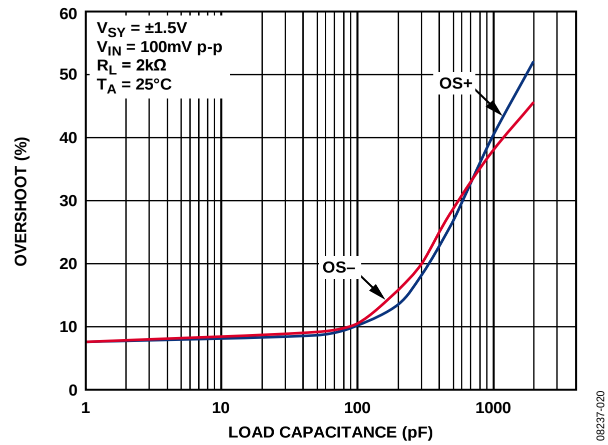

Figure 32. Overshoot vs. Load Capacitance

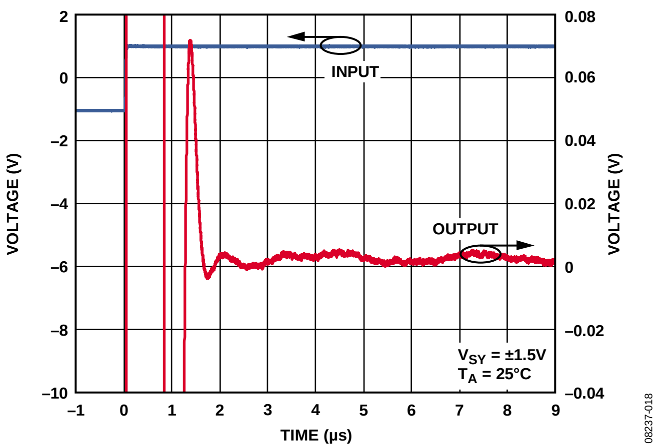

Figure 30. Settling Time

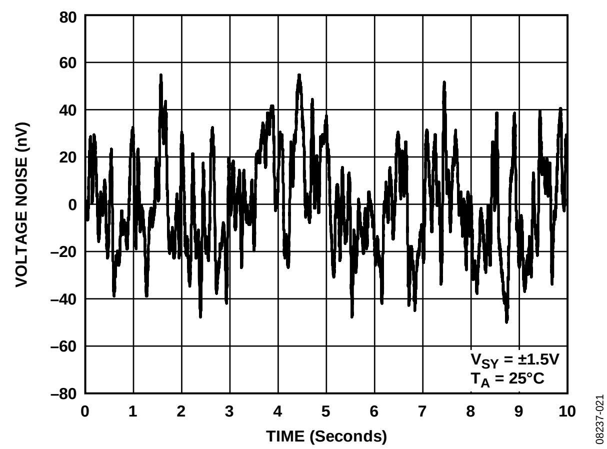

Figure 33. Voltage Noise, 0.1 Hz to 10 Hz

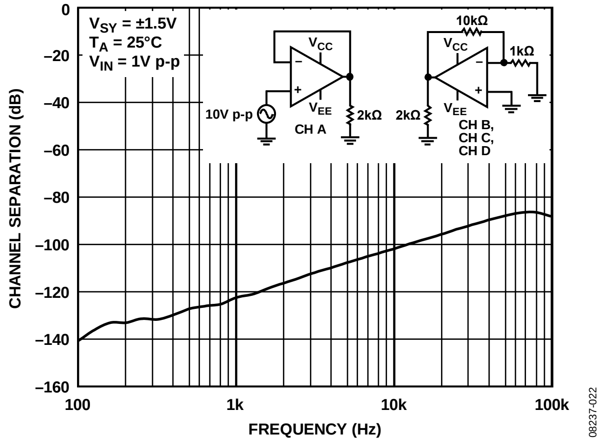

Figure 34. Channel Separation vs. Frequency

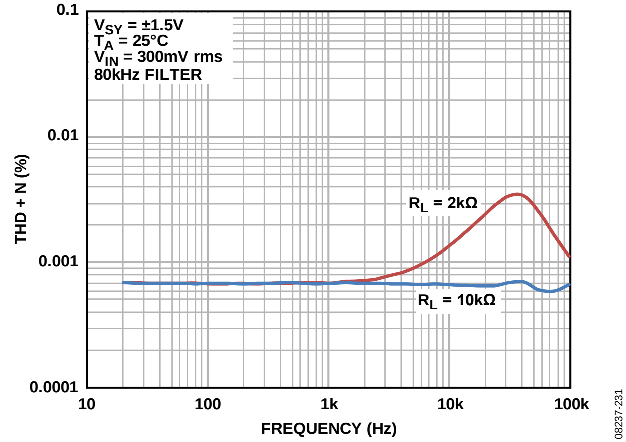

Figure 37. THD + N vs. Frequency, 80 kHz Filter

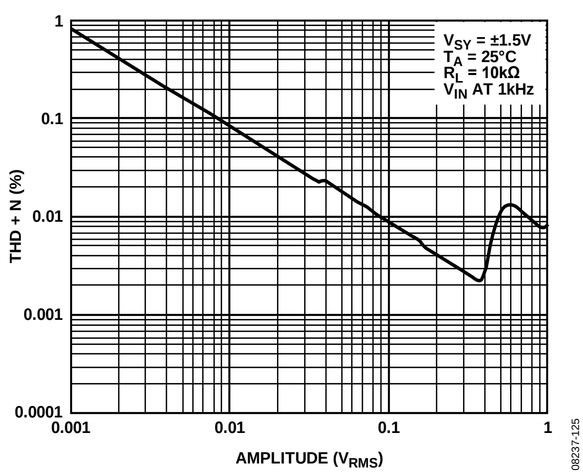

Figure 35. THD + N vs. Amplitude

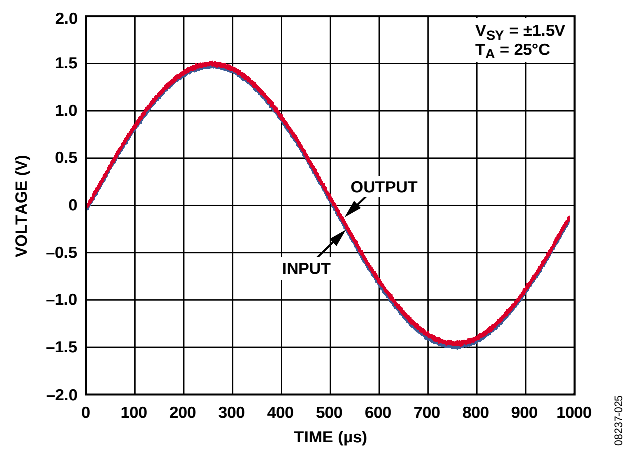

Figure 38. No Phase Reversal

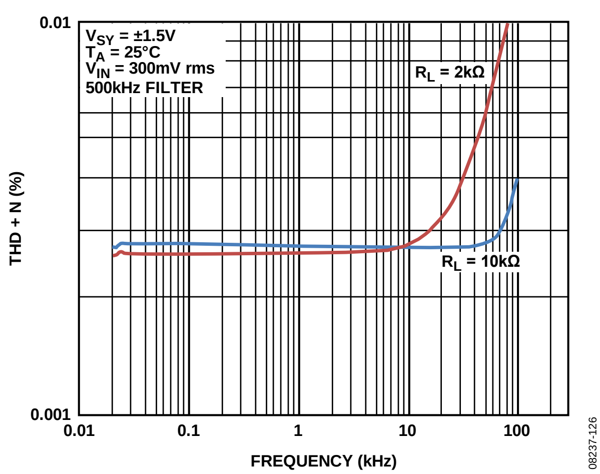

Figure 36. THD + N vs. Frequency, 500 kHz Filter

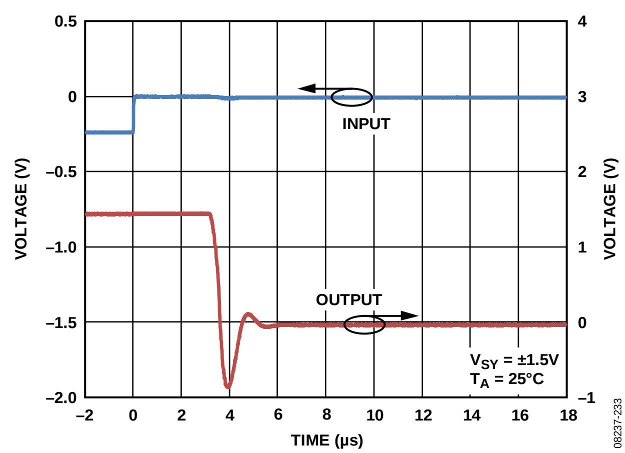

Figure 39. Positive 50% Overload Recovery

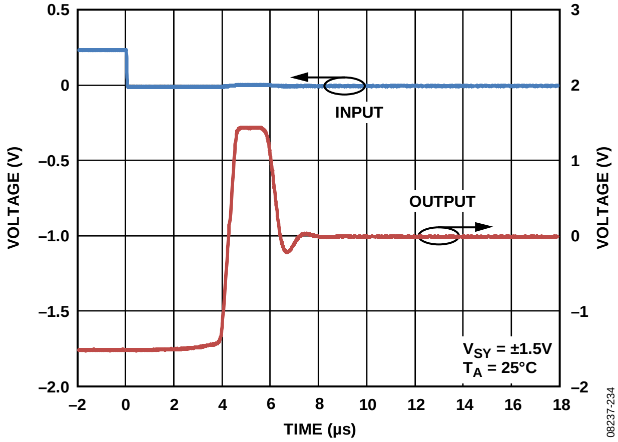

Figure 40. Negative 50% Overload Recovery

±5 V CHARACTERISTICS

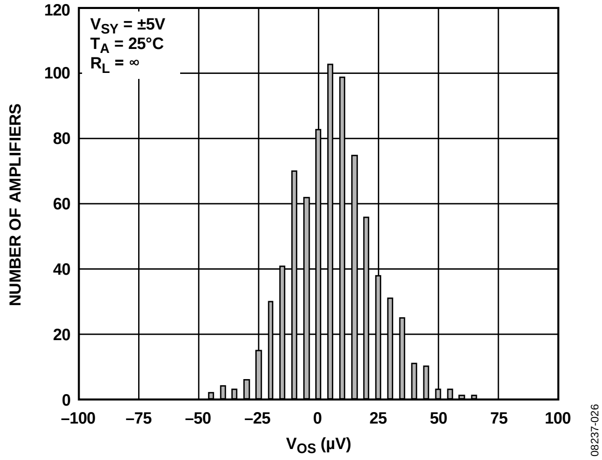

Figure 41. Input Offset Voltage (V_{OS}) Distribution, SOIC

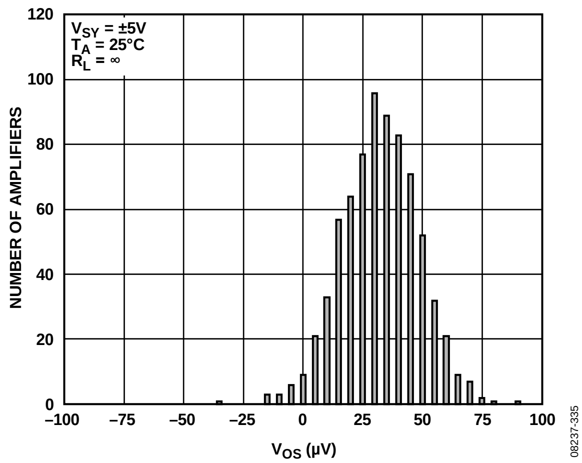

Figure 42. Input Offset Voltage (V_{OS}) Distribution, SOT-23

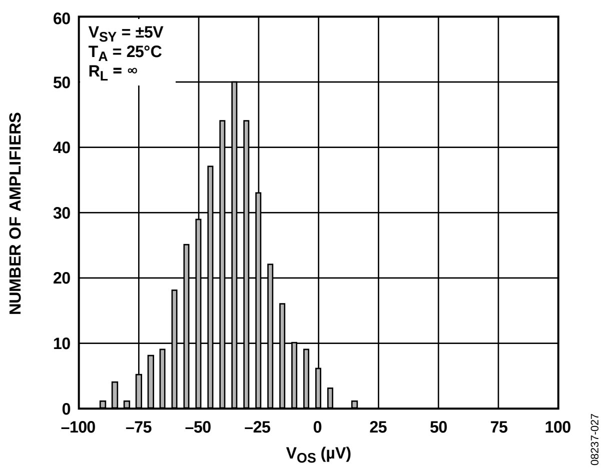

Figure 43. Input Offset Voltage (V_{OS}) Distribution, MSOP and TSSOP

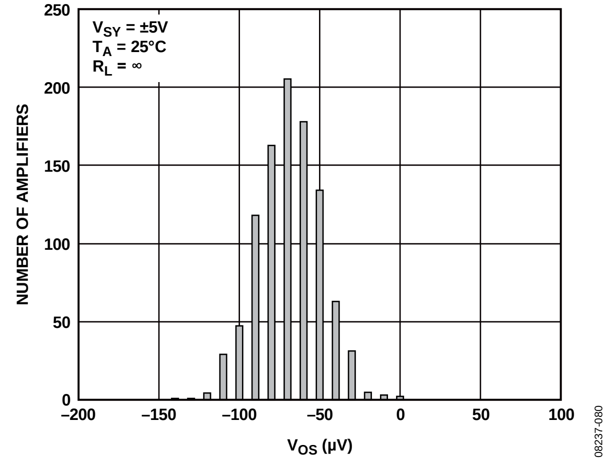

Figure 44. Input Offset Voltage (V_{OS}) Distribution, LFCSP

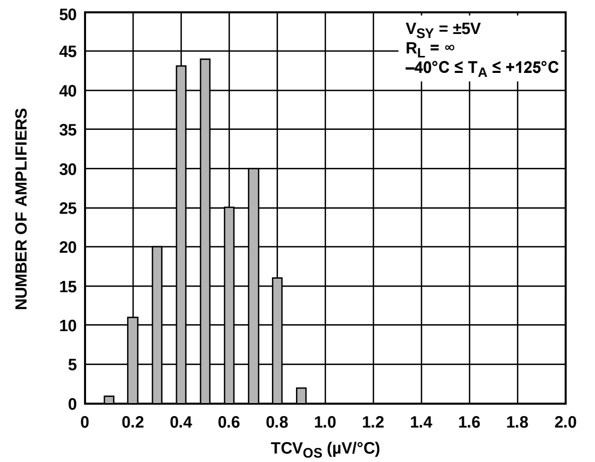

Figure 45. TCV_{OS} Distribution, SOIC, MSOP, and TSSOP

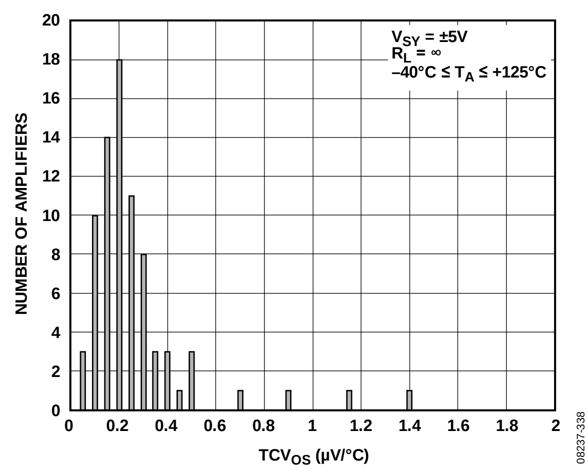

Figure 46. TCV_{OS} Distribution for SOT-23

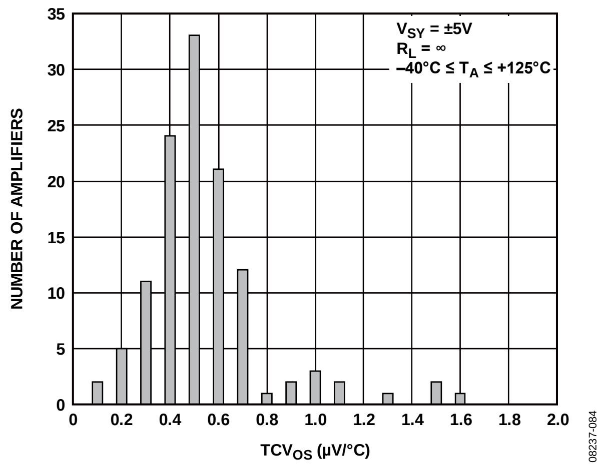

Figure 47. TCV_{OS} Distribution, LFCSP

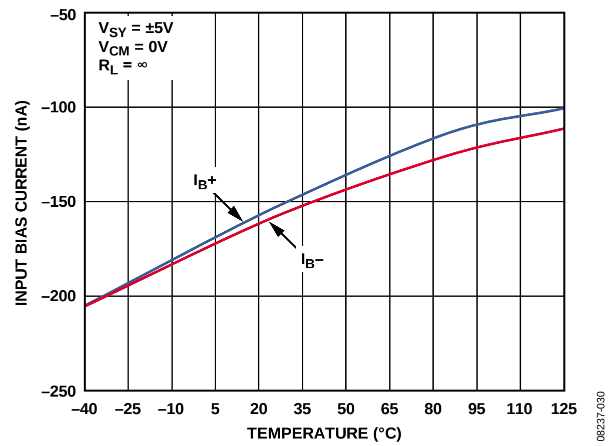

Figure 50. Input Bias Current vs. Temperature

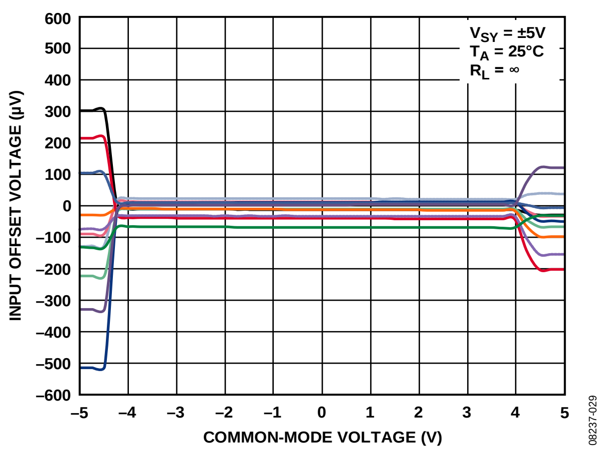

Figure 48. Input Offset Voltage vs. Common-Mode Voltage

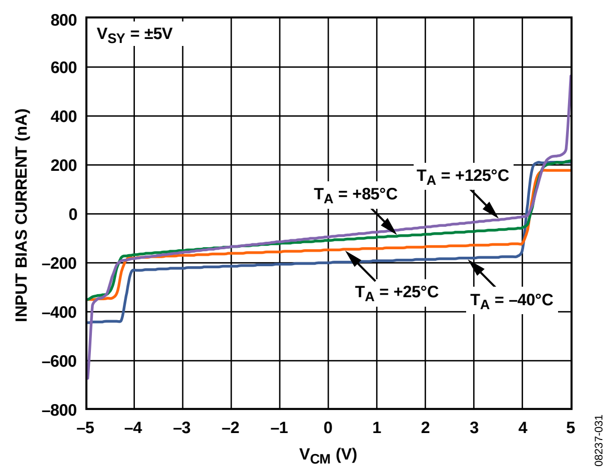

Figure 51. Input Bias Current vs. V_{CM} for Various Temperatures

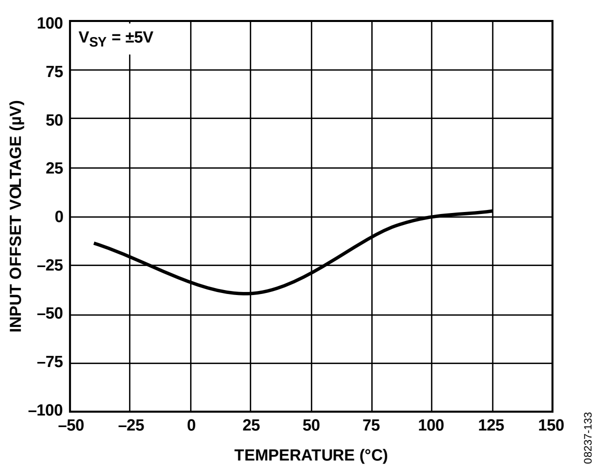

Figure 49. Input Offset Voltage vs. Temperature

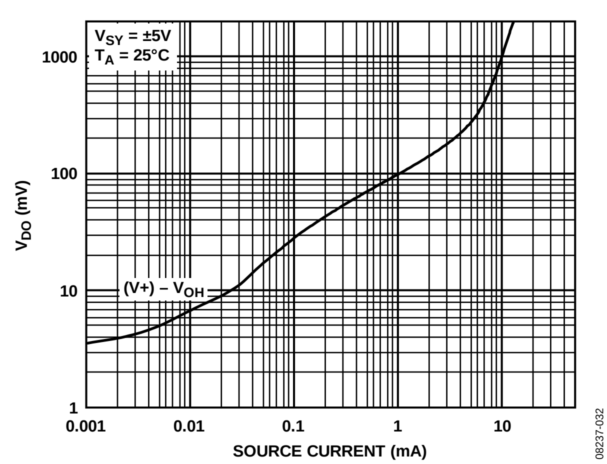

Figure 52. Dropout Voltage (V_{DO}) vs. Source Current

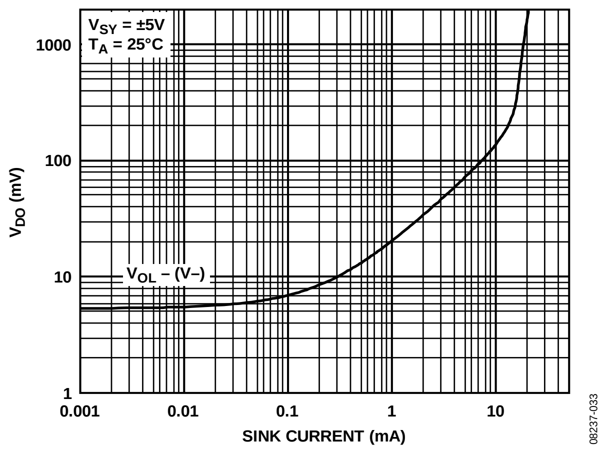

Figure 53. Dropout Voltage (V_{DO}) vs. Sink Current

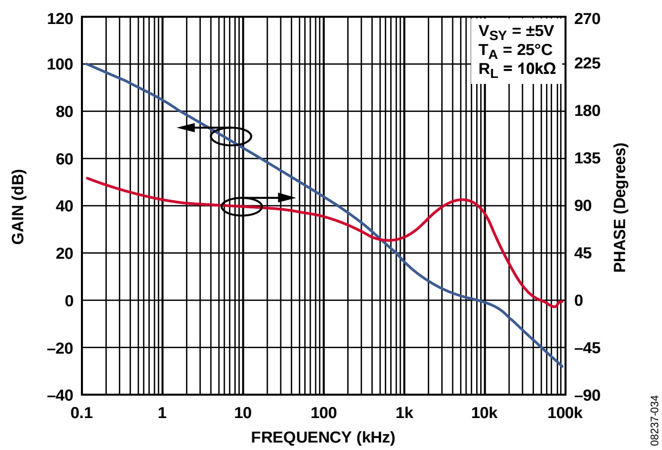

Figure 54. Open-Loop Gain and Phase vs. Frequency

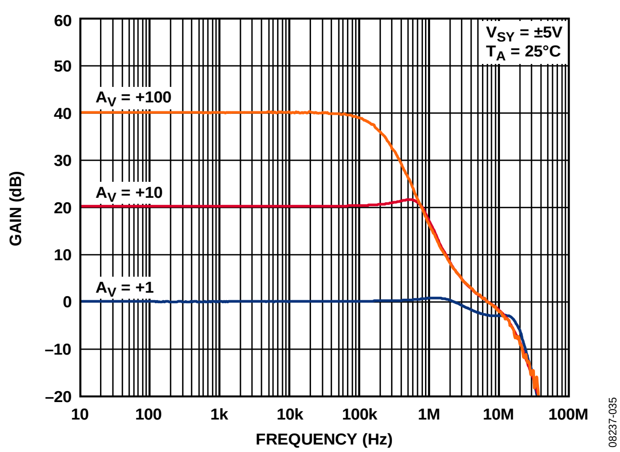

Figure 55. Closed-Loop Gain vs. Frequency

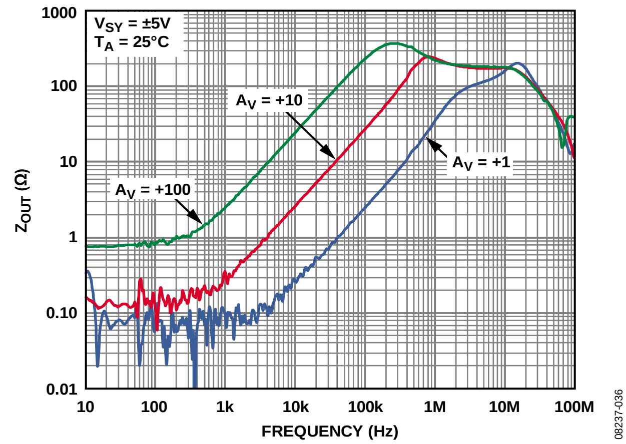

Figure 56. Output Impedance (Z_{OUT}) vs. Frequency

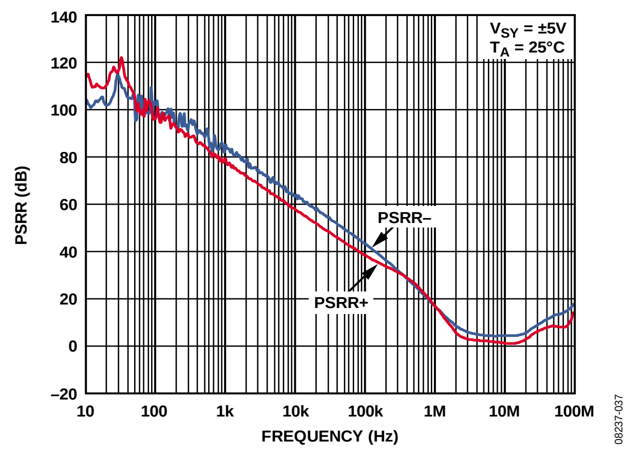

Figure 57. PSRR vs. Frequency

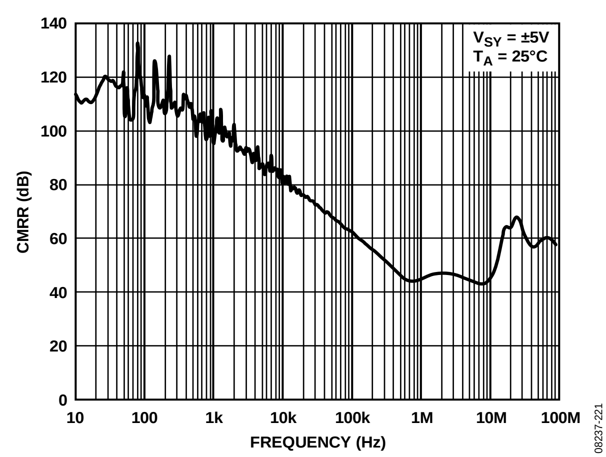

Figure 58. CMRR vs. Frequency

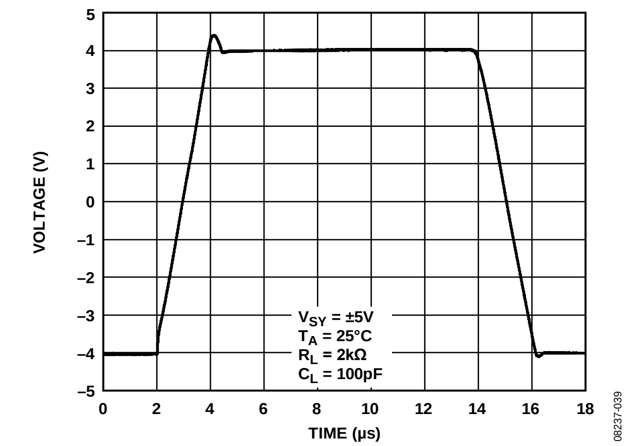

Figure 59. Large Signal Transient Response

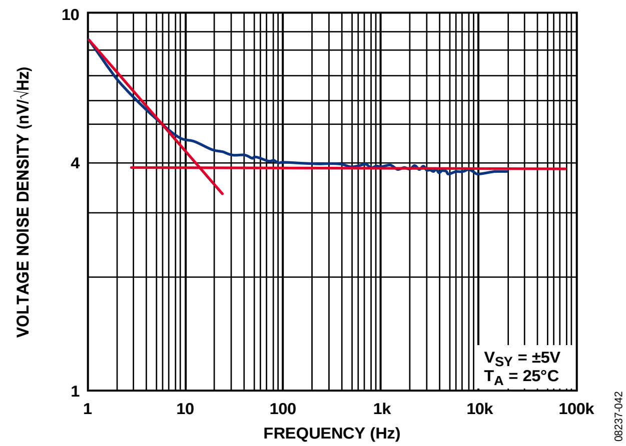

Figure 62. Voltage Noise Density vs. Frequency

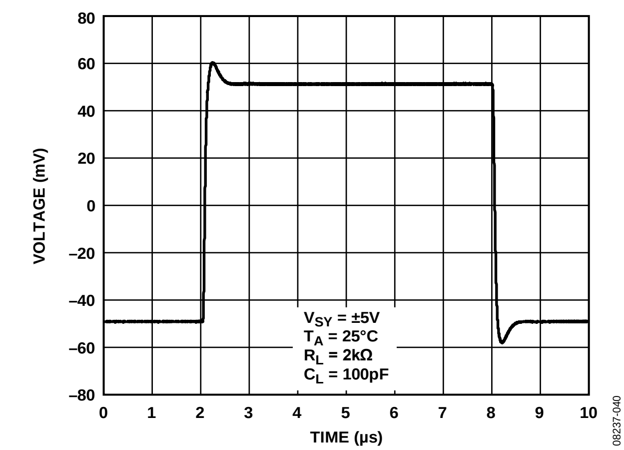

Figure 60. Small Signal Transient Response

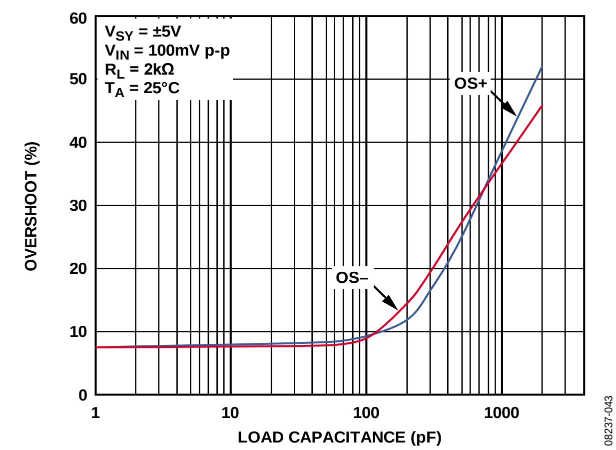

Figure 63. Overshoot vs. Load Capacitance

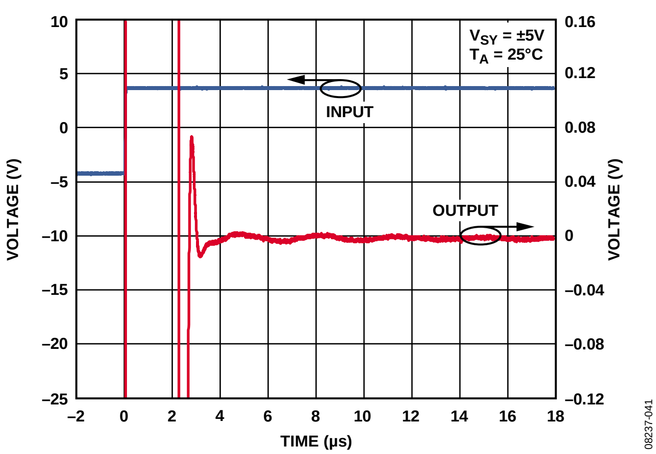

Figure 61. Settling Time

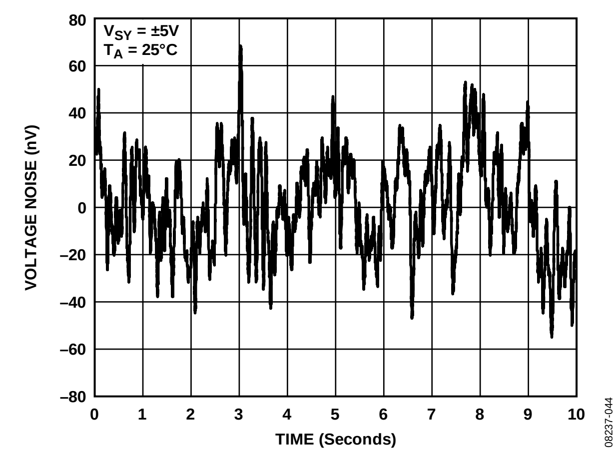

Figure 64. Voltage Noise, 0.1 Hz to 10 Hz

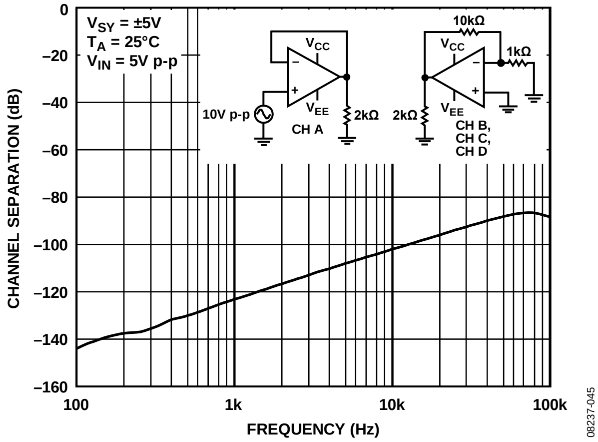

Figure 65. Channel Separation vs. Frequency

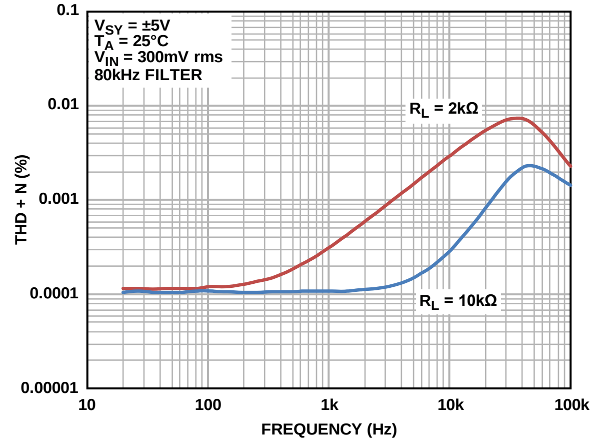

Figure 68. THD + N vs. Frequency, 80 kHz Filter

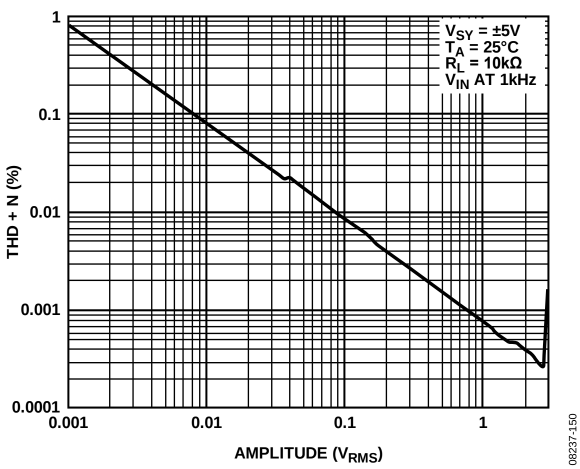

Figure 66. THD + N vs. Amplitude

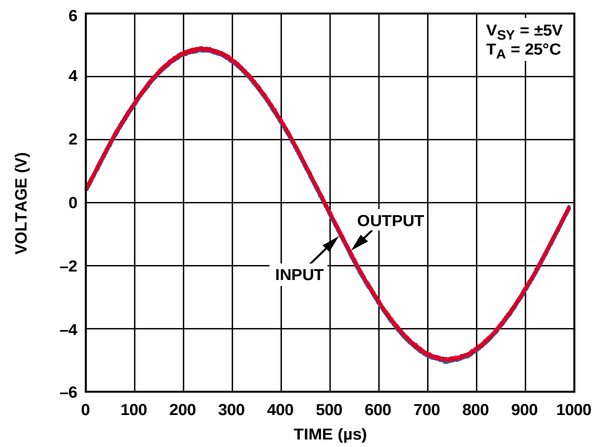

Figure 69. No Phase Reversal

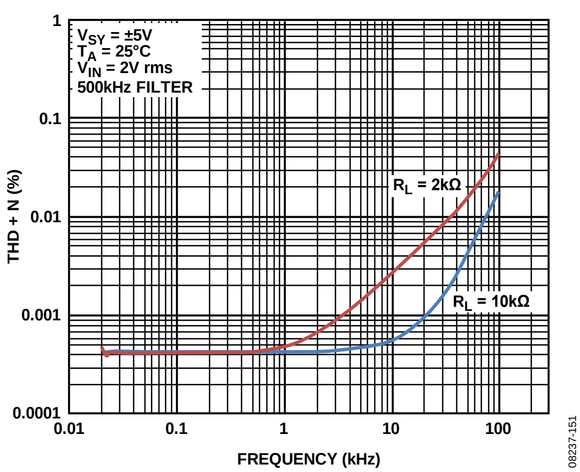

Figure 67. THD + N vs. Frequency, 500 kHz Filter

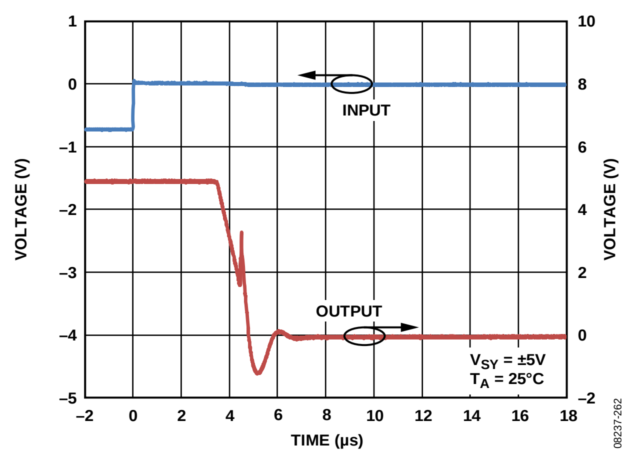

Figure 70. Positive 50% Overload Recovery

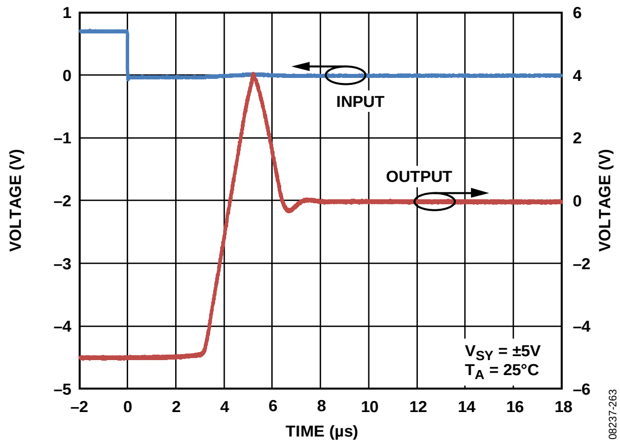

Figure 71. Negative 50% Overload Recovery

±15 V CHARACTERISTICS

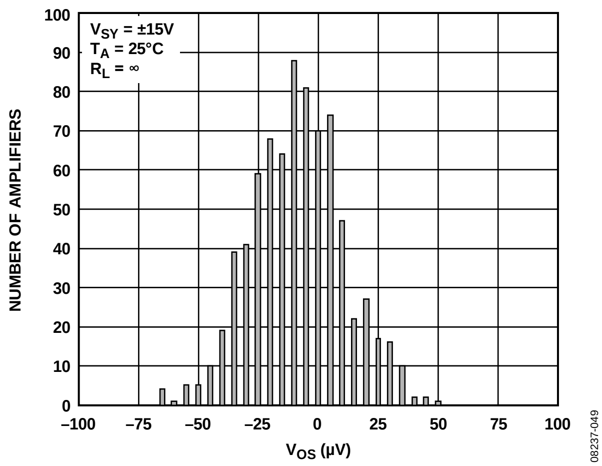

Figure 72. Input Offset Voltage (V_{OS}) Distribution, SOIC

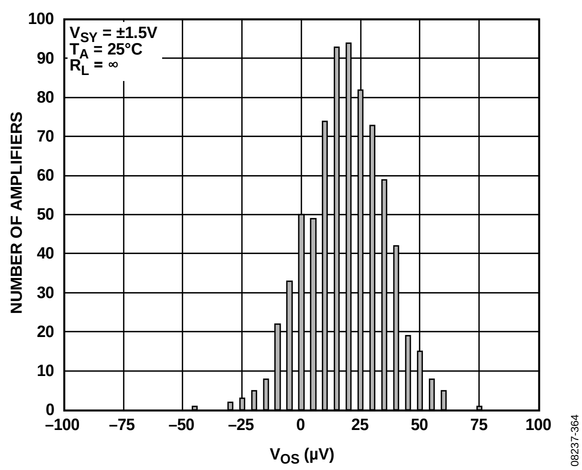

Figure 73. Input Offset Voltage (V_{OS}) Distribution, SOT-23

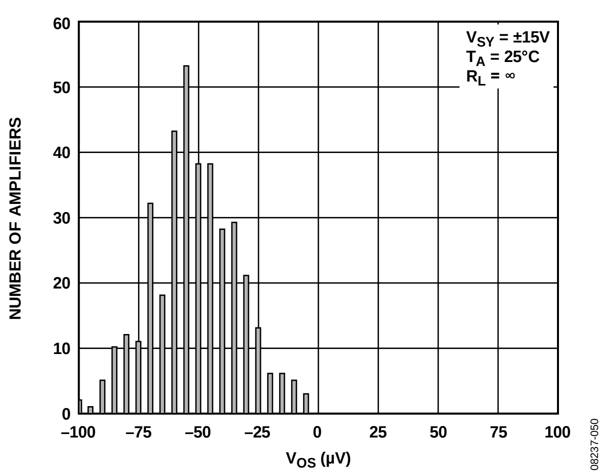

Figure 74. Input Offset Voltage (V_{OS}) Distribution, MSOP and TSSOP

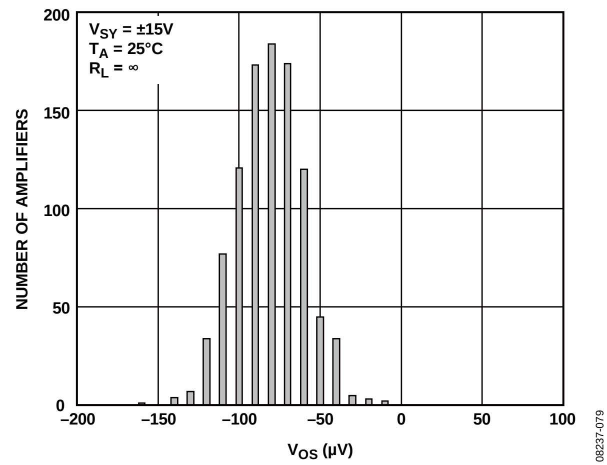

Figure 75. Input Offset Voltage (V_{OS}) Distribution, LFCSP

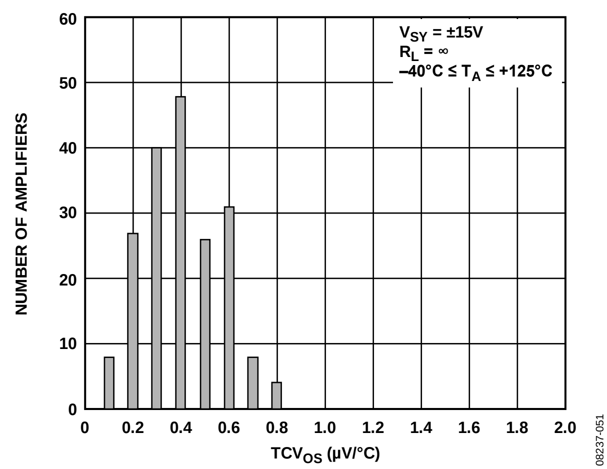

Figure 76. TCV_{OS} Distribution, SOIC, MSOP, and TSSOP

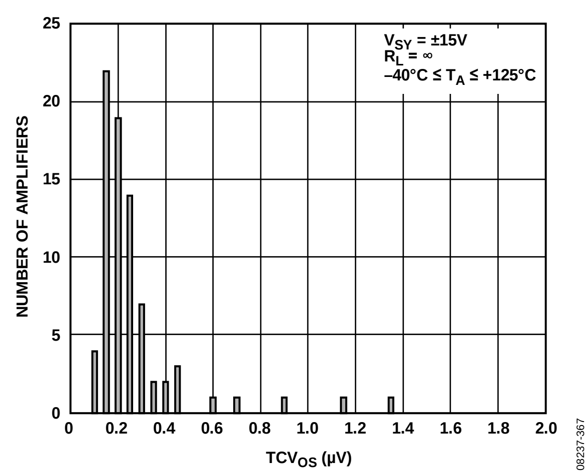

Figure 77. TCV_{OS} Distribution, SOT-23

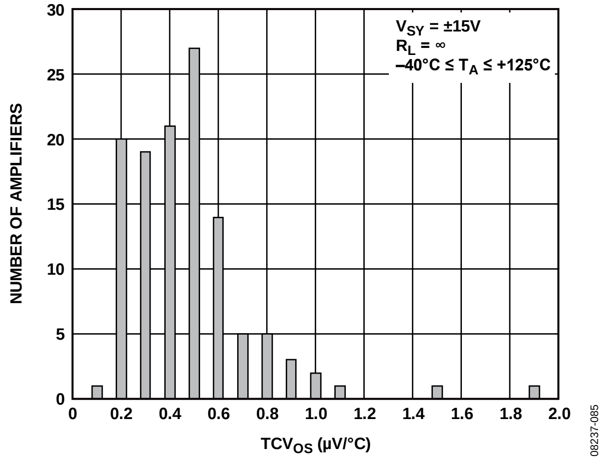

Figure 78. TCV$_{OS}$ Distribution, LFCSP

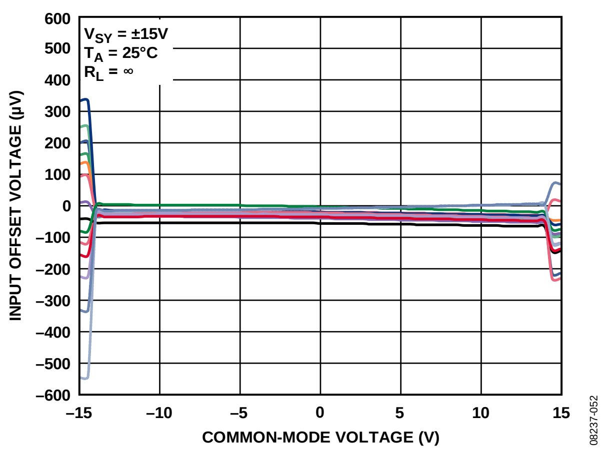

Figure 79. Input Offset Voltage vs. Common-Mode Voltage

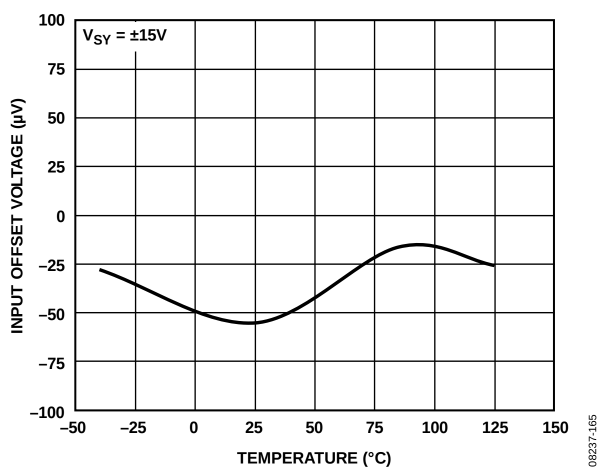

Figure 80. Input Offset Voltage vs. Temperature

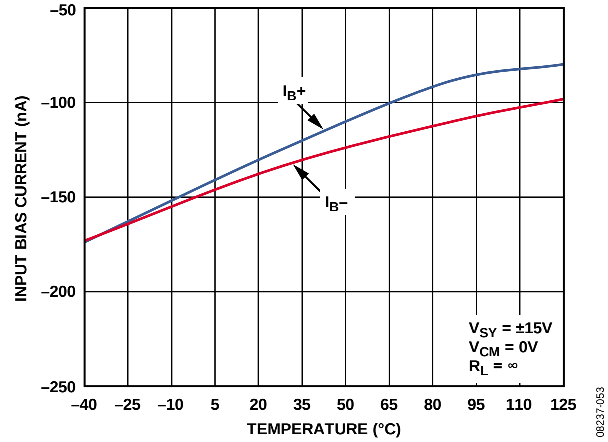

Figure 81. Input Bias Current vs. Temperature

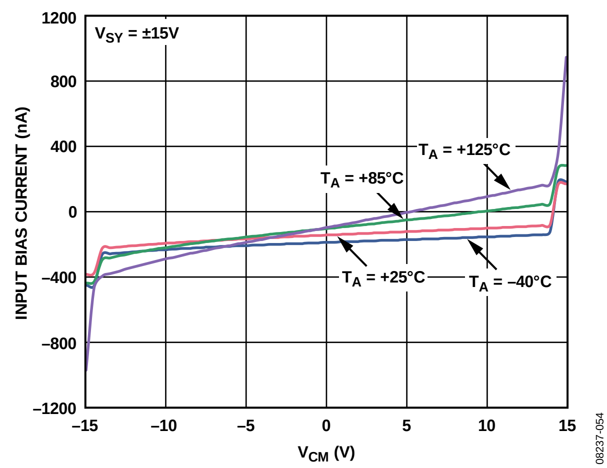

Figure 82. Input Bias Current vs. V$_{CM}$ for Various Temperatures

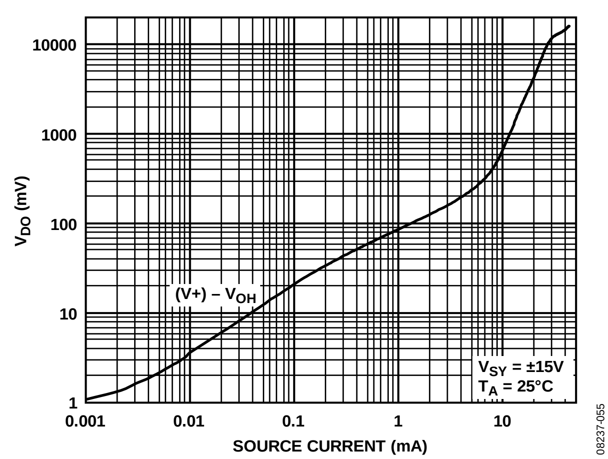

Figure 83. Dropout Voltage (V$_{DO}$) vs. Source Current

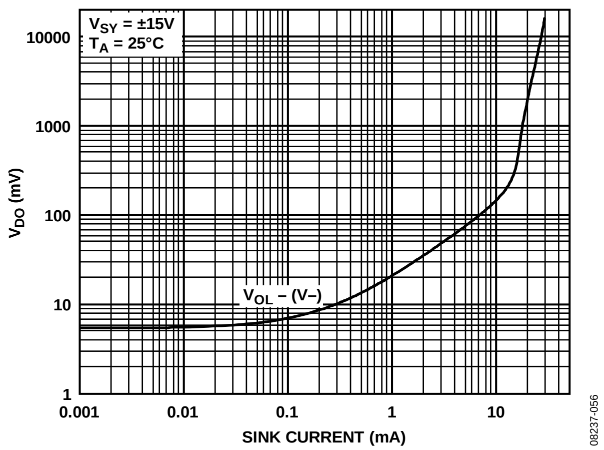

Figure 84. Dropout Voltage (V_{DO}) vs. Sink Current

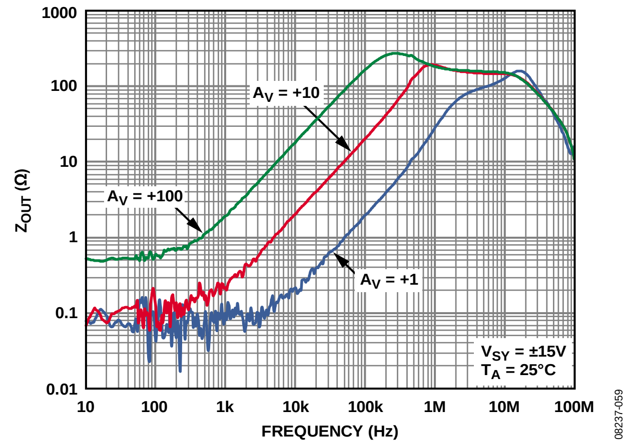

Figure 87. Output Impedance (Z_{OUT}) vs. Frequency

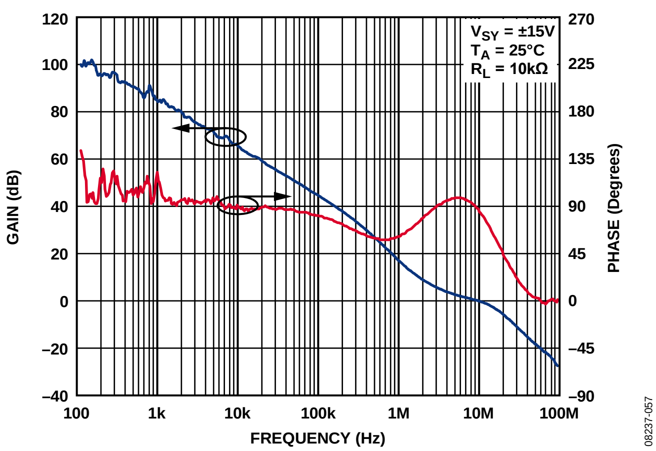

Figure 85. Open-Loop Gain and Phase vs. Frequency

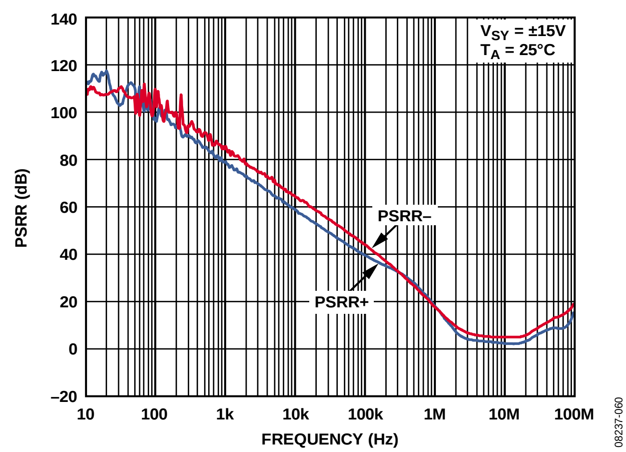

Figure 88. PSRR vs. Frequency

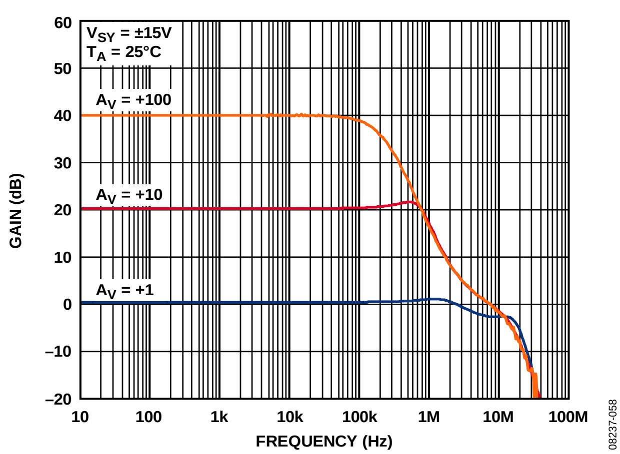

Figure 86. Closed-Loop Gain vs. Frequency

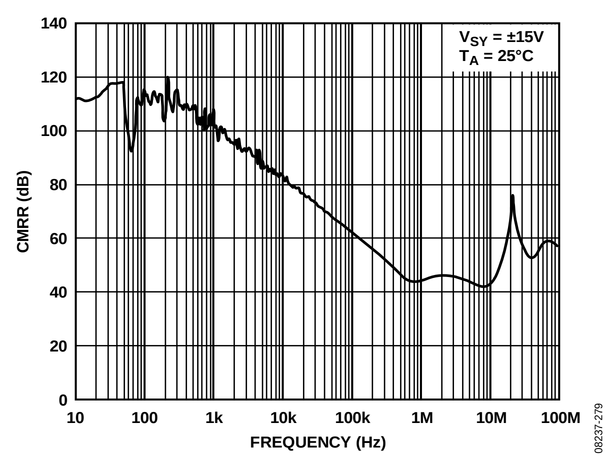

Figure 89. CMRR vs. Frequency

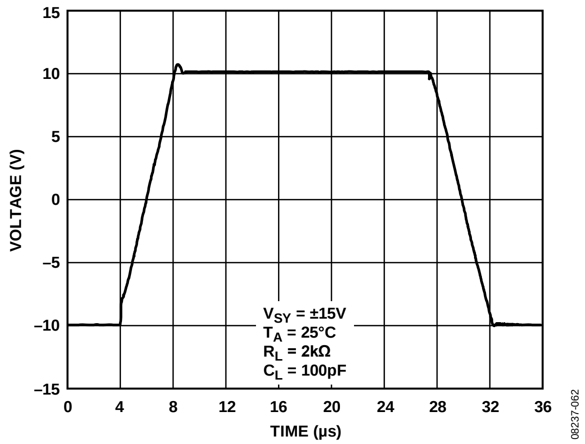

Figure 90. Large Signal Transient Response

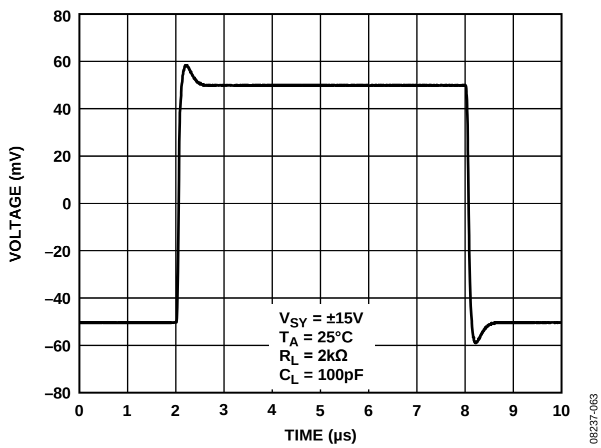

Figure 91. Small Signal Transient Response

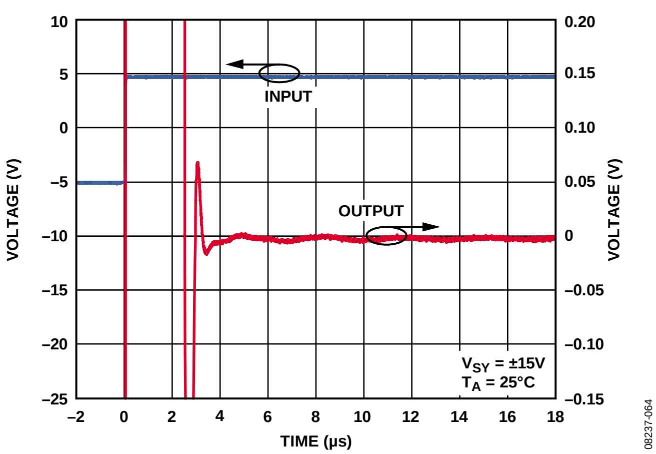

Figure 92. Settling Time

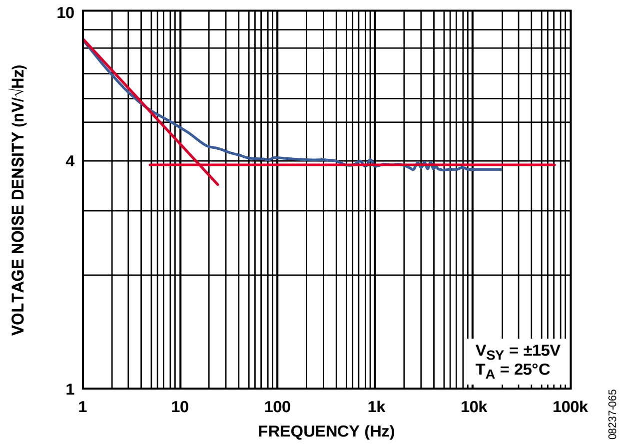

Figure 93. Voltage Noise Density vs. Frequency

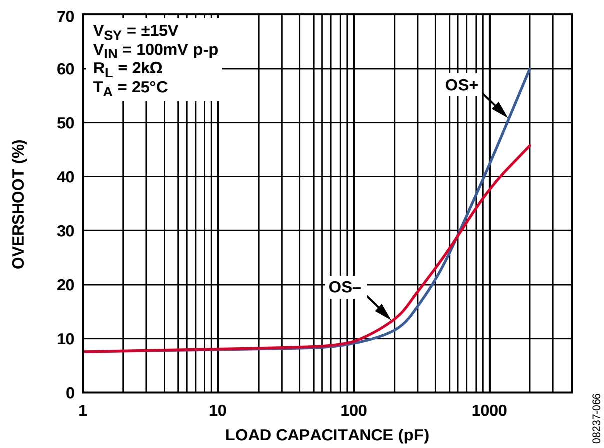

Figure 94. Overshoot vs. Load Capacitance

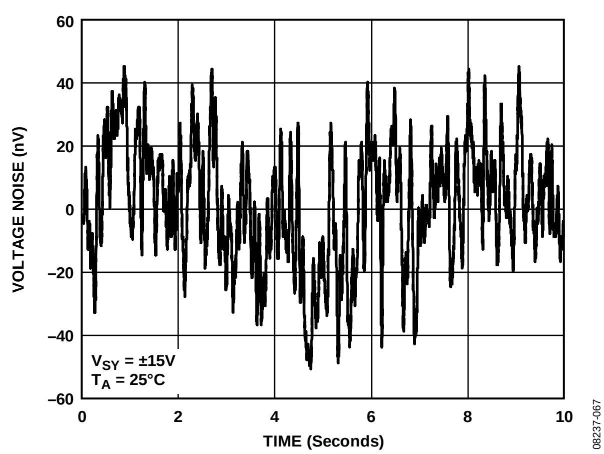

Figure 95. Voltage Noise 0.1 Hz to 10 Hz

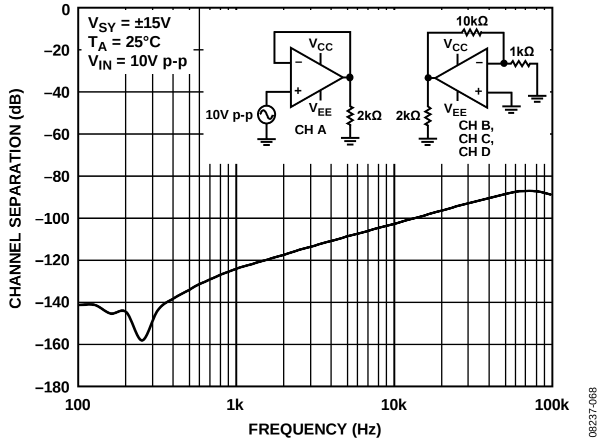

Figure 96. Channel Separation vs. Frequency

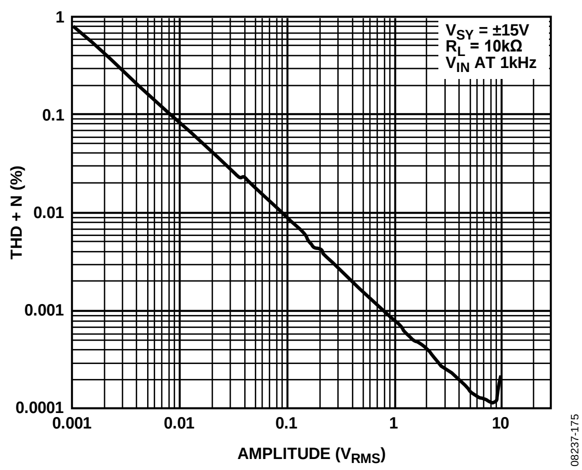

Figure 97. THD + N vs. Amplitude

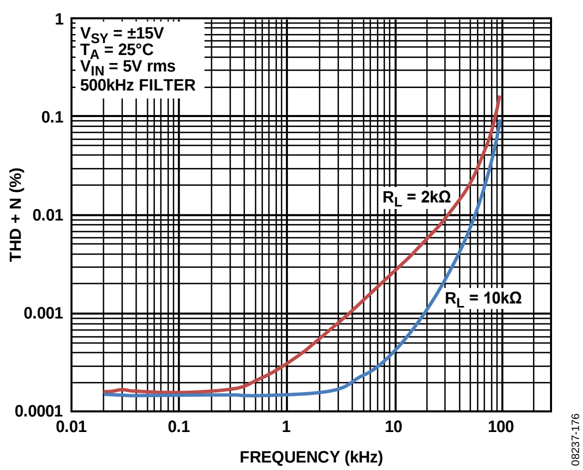

Figure 98. THD + N vs. Frequency, 500 kHz Filter

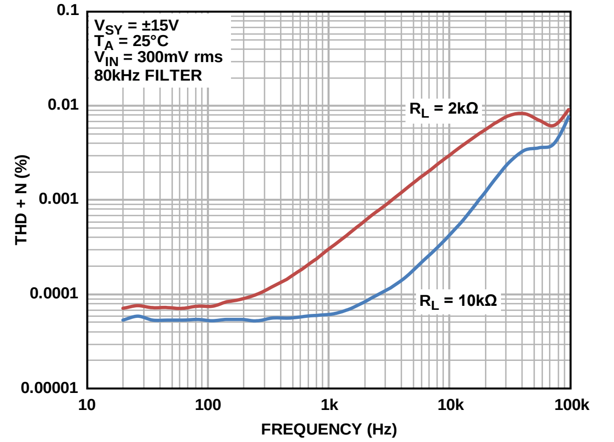

Figure 99. THD + N vs. Frequency, 80 kHz Filter

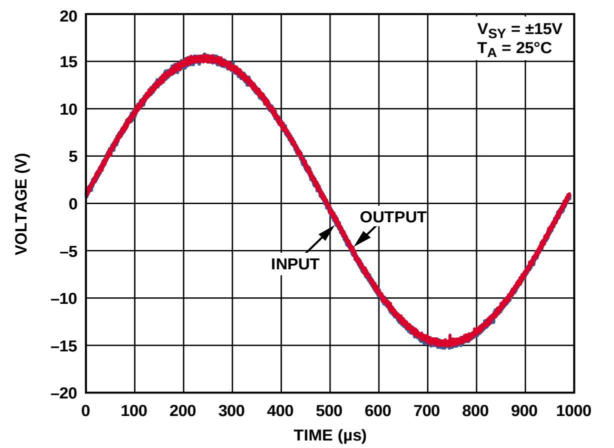

Figure 100. No Phase Reversal

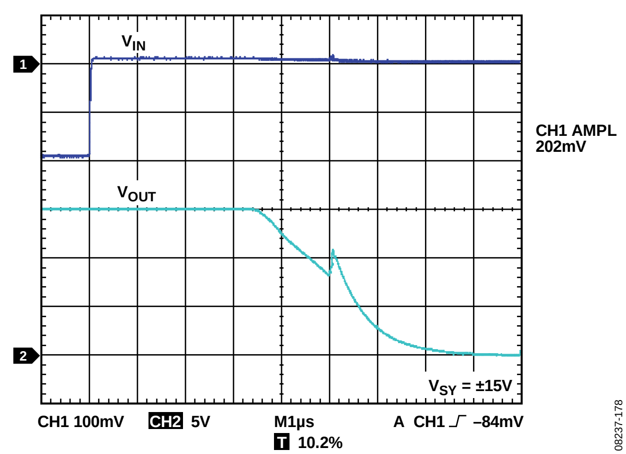

Figure 101. Positive 50% Overload Recovery

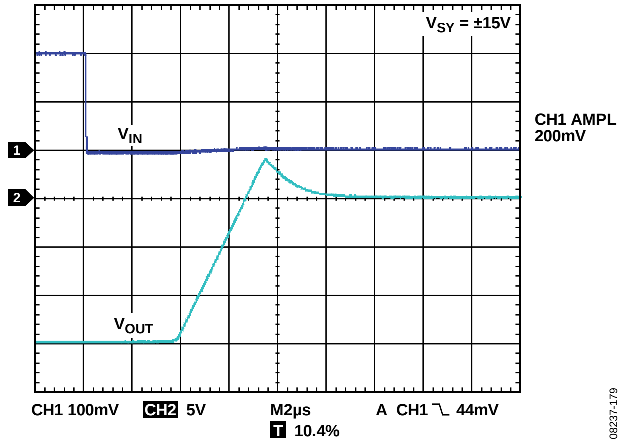

Figure 102. Negative 50% Overload Recovery

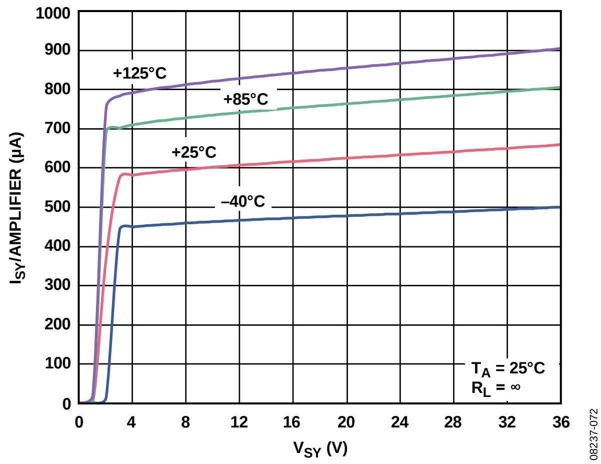

Figure 103. Supply Current (I_{SY}) per Amplifier vs. Supply Voltage (V_{SY}) for Various Temperatures

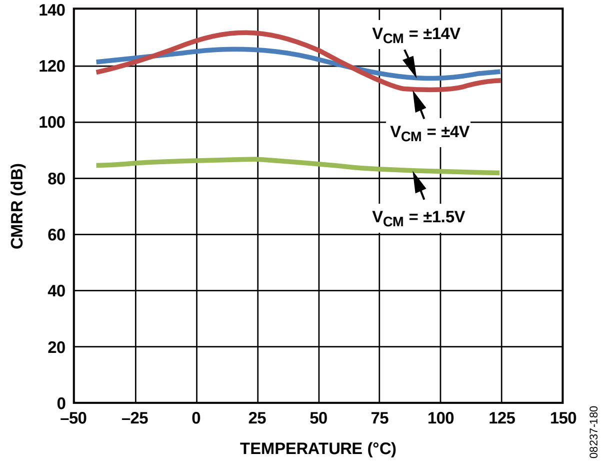

Figure 104. CMRR vs. Temperature

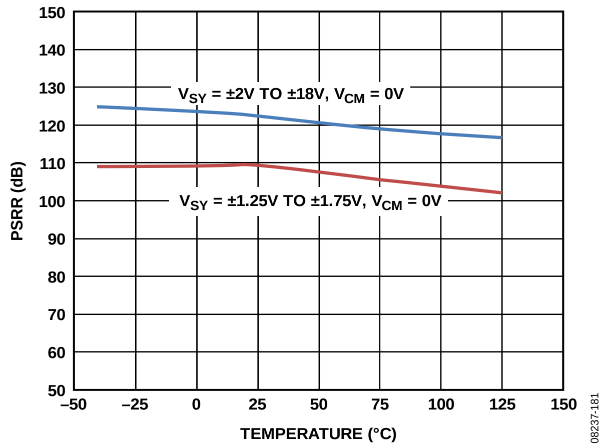

Figure 105. PSRR vs. Temperature

APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION

The ADA4084-1/ADA4084-2/ADA4084-4 devices are precision single-supply, rail-to-rail operational amplifiers. Intended for portable instrumentation, the ADA4084-1/ADA4084-2/ADA4084-4 devices combine the attributes of precision, wide bandwidth, and low noise, making them an ideal choice in single-supply applications that require both ac and precision dc performance. Other low supply voltage applications for which the ADA4084-1/ADA4084-2/ADA4084-4 devices are well suited include active filters, audio microphone preamplifiers, power supply control, and telecommunications. To combine all of these attributes with rail-to-rail input/output operation, novel circuit design techniques are used.

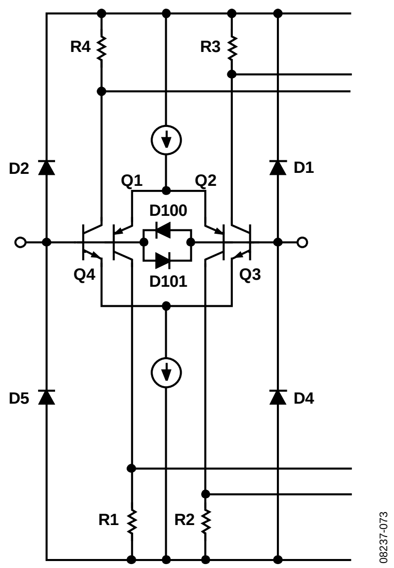

Figure 106. Equivalent Input Circuit

For example, Figure 106 illustrates a simplified equivalent circuit for the input stage of the ADA4084-1/ADA4084-2/ADA4084-4. It comprises a PNP differential pair, Q1 and Q2, and an NPN differential pair, Q3 and Q4, operating concurrently. Diode D100 and Diode D101 serve to clamp the applied differential input voltage to the ADA4084-1/ADA4084-2/ADA4084-4, thereby protecting the input transistors against Zener breakdown of the emitter-base junctions. Input stage voltage gains are kept low for input rail-to-rail operation. The two pairs of differential output voltages are connected to the second stage of the ADA4084-1/ADA4084-2/ADA4084-4, which is a modified compound folded cascade gain stage. It is also in the second gain stage that the two pairs of differential output voltages are combined into a single-ended output signal voltage used to drive the output stage.

A key issue in the input stage is the behavior of the input bias currents over the input common-mode voltage range. Input bias currents in the ADA4084-1/ADA4084-2/ADA4084-4 are the arithmetic sum of the base currents in Q1 and Q4 and in Q2 and Q3. As a result of this design approach, the input bias currents in the ADA4084-1/ADA4084-2/ADA4084-4 not only exhibit different amplitudes, but they also exhibit different polarities. This effect is best shown in Figure 19, Figure 20, Figure 50, Figure 51, Figure 81, and Figure 82. It is, therefore, important that the effective source impedances that are connected to the ADA4084-1/ADA4084-2/ADA4084-4 inputs be balanced for optimum dc and ac performance.

To achieve rail-to-rail output, the ADA4084-1/ADA4084-2/ADA4084-4 output stage design employs a unique topology for both sourcing and sinking current. This circuit topology is shown in Figure 107. The output stage is voltage driven from the second gain stage. The signal path through the output stage is inverting; that is, for positive input signals, Q13 provides the base current drive to Q19 so that it conducts (sinks) current. For negative input signals, the signal path via Q18 to the mirror to Q24 provides the base current drive for Q23 to conduct (source) current. Both transistors provide output current until they are forced into saturation.

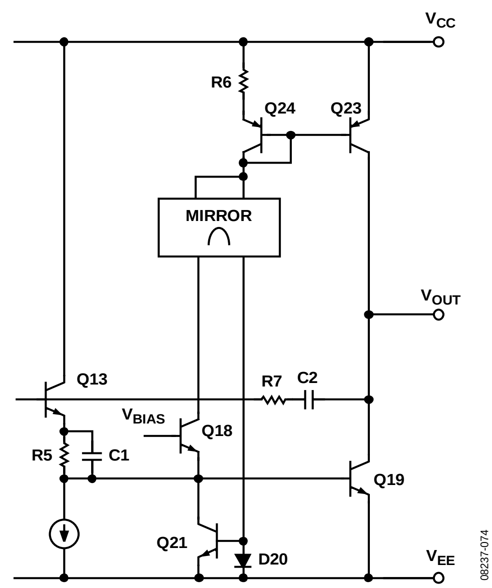

Figure 107. Equivalent Output Circuit

Thus, the saturation voltage of the output transistors sets the limit on the ADA4084-1/ADA4084-2/ADA4084-4 maximum output voltage swing. Output short-circuit current limiting is determined by the maximum signal current into the base of Q13 from the second gain stage. The output stage also exhibits voltage gain. This is accomplished by the use of common-emitter amplifiers, and, as a result, the voltage gain of the output stage (thus, the open-loop gain of the device) exhibits a dependence on the total load resistance at the output of the ADA4084-1/ADA4084-2/ADA4084-4.

START-UP CHARACTERISTICS

The ADA4084-1/ADA4084-2/ADA4084-4 are specified to operate from 3 V to 30 V (±1.5 V to ±15 V) under nominal power supplies. During power-up as the supply voltage increases from 0 V to the nominal power supply voltage, the supply current (I_{SY}) increases as well, to the point at which it stabilizes and the amplifier is ready to operate. The stabilization varies with temperature, as shown in Figure 103. For example, at −40°C, it requires a higher voltage and stabilizes at a lower supply current than at hot temperatures. At hot temperatures, it requires a lower voltage but stabilizes at a higher current. In all cases, the ADA4084-1/ ADA4084-2/ADA4084-4 are specified to start up and operate at a minimum of 3 V under all temperature conditions.

INPUT PROTECTION

As with any semiconductor device, if conditions exist where the applied input voltages to the device exceed either supply voltage, the input overvoltage I-to-V characteristic of the device must be considered. When an overvoltage occurs, the amplifier may be damaged, depending on the magnitude of the applied voltage and the magnitude of the fault current.

The D1, D2, D4, and D5 diodes conduct when the input common-mode voltage exceeds either supply pin by a diode drop. This diode drop voltage varies with temperature and is in the range of 0.3 V to 0.8 V. As shown in the simplified equivalent input circuit of Figure 106, the ADA4084-1/ADA4084-2/ADA4084-4 do not have any internal current limiting resistors; thus, fault currents can quickly rise to damaging levels.

This input current is not inherently damaging to the device, provided that it is limited to 5 mA or less. If a fault condition causes more than 5 mA to flow, add an external series resistor at the expense of additional thermal noise. Figure 108 shows a typical noninverting configuration for an overvoltage protected amplifier, where the series resistance (R1) is chosen, such that

$$R1 = \frac{V_{IN(MAX)} - V_{SUPPLY}}{5\text{ mA}}$$

For example, a 1 kΩ resistor protects the ADA4084-1/ADA4084-2/ ADA4084-4 against input signals up to 5 V above and below the supplies. Note that the thermal noise of a 1 kΩ resistor at room temperature is 4 nV/√Hz, which exceeds the voltage noise of the ADA4084-1/ADA4084-2/ADA4084-4. For other configurations in which both inputs are used, add a series resistor to limit the input current. To ensure optimum dc and ac performance, balance the source impedance levels.

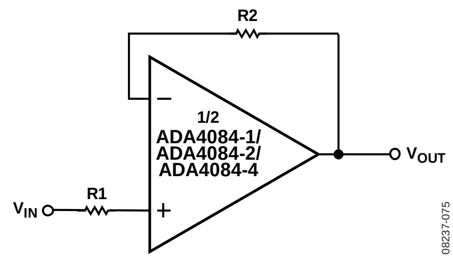

Figure 108. Resistance in Series with the Input Limits Overvoltage Currents to Safe Values

To protect the Q1/Q2 and Q3/Q4 pairs from large differential voltages that may result in Zener breakdown of the emitter-base junction, D100 and D101 are connected between the two inputs. This precludes operation as a comparator. For a more complete description, see the MT-035 Tutorial, *Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues*; the MT-083 Tutorial, *Comparators*; the MT-084 Tutorial, *Using Op Amps as Comparators*; and the AN-849 Application Note, *Using Op Amps as Comparators*.

OUTPUT PHASE REVERSAL

Some operational amplifiers designed for single-supply operation exhibit an output voltage phase reversal when their inputs are driven beyond their useful common-mode range. Typically, for single-supply bipolar op amps, the negative supply determines the lower limit of their common-mode range. With these devices, external clamping diodes, with the anode connected to ground and the cathode to the inputs, prevent input signal excursions from exceeding the negative supply of the device (that is, GND), preventing a condition that causes the output voltage to change phase. JFET input amplifiers can also exhibit phase reversal, and, if so, a series input resistor is usually required to prevent it.

The ADA4084-1/ADA4084-2/ADA4084-4 are free from reasonable input voltage range restrictions, provided that input voltages no greater than the supply voltages are applied (see Figure 38, Figure 69, and Figure 100).

Although device output does not change phase, large currents can flow through the input protection diodes. Therefore, apply the technique recommended in the Input Protection section to those applications where the likelihood of input voltages exceeding the supply voltages is high.

DESIGNING LOW NOISE CIRCUITS IN SINGLE-SUPPLY APPLICATIONS

In single-supply applications, devices like the ADA4084-1/ ADA4084-2/ADA4084-4 extend the dynamic range of the application through the use of rail-to-rail operation. Referring to the op amp noise model circuit configuration illustrated in Figure 109, the expression for the total equivalent input noise voltage of an amplifier for a source resistance level, R_S, is given by

$$e_{nT} = \sqrt{2\left[(e_{nR})^2 + (i_{nOA} \times R_S)^2\right] + (e_{nOA})^2} \text{, units in } \frac{V}{\sqrt{Hz}}$$

where:
$(e_{nR})^2$ is the source resistance thermal noise voltage power (4kTR).
k is the Boltzmann's constant, 1.38×10^{-23} J/K.
T is the ambient temperature in Kelvin of the circuit, 273.15 + T_A (°C).
$(i_{nOA})^2$ is the op amp equivalent input noise current spectral power (1 Hz bandwidth).
$R_S = 2R$, the effective, or equivalent, circuit source resistance.
$(e_{nOA})^2$ is the op amp equivalent input noise voltage spectral power (1 Hz bandwidth).

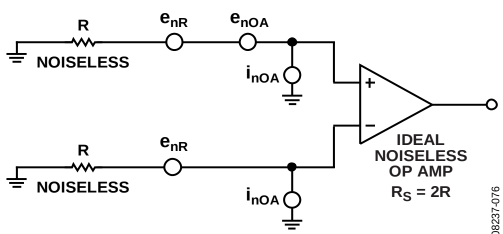

Figure 109. Op Amp Noise Circuit Model Used to Determine Total Circuit Equivalent Input Noise Voltage and Noise Figure

As a design aid, Figure 110 shows the equivalent thermal noise of the ADA4084-1/ADA4084-2/ADA4084-4 vs. the total source resistance. Note that for source resistance less than 1 kΩ, the equivalent input noise voltage of the ADA4084-1/ADA4084-2/ ADA4084-4 is dominant.

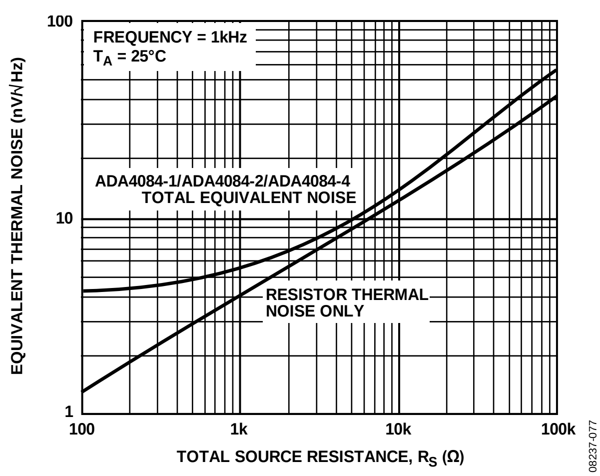

Figure 110. Equivalent Thermal Noise vs. Total Source Resistance

Because circuit SNR is the critical parameter in the final analysis, the noise behavior of a circuit is sometimes expressed in terms of its noise figure (NF). The noise figure is defined as the ratio of the signal-to-noise output of a circuit to its signal-to-noise input.

Noise figure is generally used for RF and microwave circuit analysis in a 50 Ω system. This is not very useful for op amp circuits where the input and output impedances can vary greatly. For a more complete description of noise figure, see the MT-052 Tutorial, *Op Amp Noise Figure: Don't be Misled.*

Signal levels in the application invariably increase to maximize circuit SNR, which is not an option in low voltage, single-supply applications.

Therefore, to achieve optimum circuit SNR in single-supply applications, choose an operational amplifier with the lowest equivalent input noise voltage, along with source resistance levels that are consistent with maintaining low total circuit noise.

COMPARATOR OPERATION

Although op amps are quite different from comparators, occasionally an unused section of a dual or a quad op amp can be used as a comparator; however, this is not recommended for any rail-to-rail output op amps. For rail-to-rail output op amps, the output stage is generally a ratioed current mirror with bipolar or MOSFET transistors. With the device operating open-loop, the second stage increases the current drive to the ratioed mirror to close the loop. However, the loop cannot close, which results in an increase in supply current. With the op amp configured as a comparator, the supply current can be significantly higher (see Figure 111). Configure an unused section as a voltage follower with the noninverting input connected to a voltage within the input voltage range. The ADA4084-1/ADA4084-2/ADA4084-4 have unique second stage and output stage designs that greatly reduce the excess supply current when the op amp is operating open-loop.

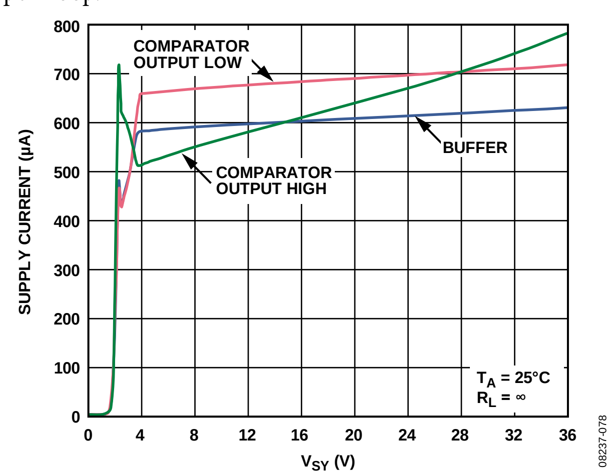

Figure 111. Supply Current vs. Supply Voltage (V_{SY})

LONG-TERM DRIFT

The stability of a precision signal path over its lifetime or between calibration procedures is dependent on the long-term stability of the analog components in the path, such as op amps, references, and data converters. To help system designers predict the long-term drift of circuits that use the ADA4084-1/ ADA4084-2/ADA4084-4, Analog Devices measured the offset voltage of multiple units for 10,000 hours (more than 13 months) using a high precision measurement system, including an ultrastable oil bath. To replicate real-world system performance, the devices under test (DUTs) were soldered onto an FR4 PCB using a standard reflow profile (as defined in the JEDEC J-STD-020D standard), as opposed to testing them in sockets. This manner of testing is important because expansion and contraction of the PCB can apply stress to the integrated circuit (IC) package and contribute to shifts in the offset voltage.

The ADA4084-1/ADA4084-2/ADA4084-4 have extremely low long-term drift, as shown in Figure 112. The red, blue, and green traces show sample units. Note that the mean drift of the ADA4084-1/ADA4084-2/ADA4084-4 over 10,000 hours is less than 3 µV, or less than 3% of their maximum specified offset voltage of 100 µV at room temperature.

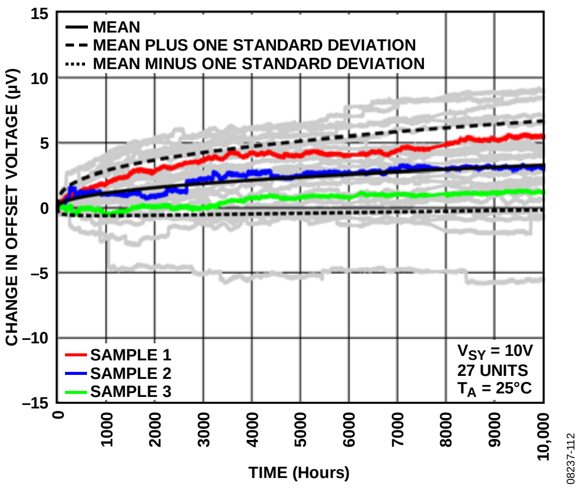

Figure 112. Measured Long-Term Drift of the ADA4084-1/ADA4084-2/ ADA4084-4 Offset Voltage over 10,000 Hours

TEMPERATURE HYSTERESIS

In addition to stability over time as described in the Long-Term Drift section, it is useful to know the temperature hysteresis, that is, the stability vs. cycling of temperature. Hysteresis is an important parameter because it tells the system designer how closely the signal returns to its starting amplitude after the ambient temperature changes and subsequent return to room temperature. Figure 113 shows the change in input offset voltage as the temperature cycles three times from room temperature to +125°C to −40°C and back to room temperature. The dotted line is an initial preconditioning cycle to eliminate the original temperature-induced offset shift from exposure to production solder reflow temperatures. In the three full cycles, the offset hysteresis is typically only 4 µV, or 2% of its 200 µV maximum offset voltage over the full operating temperature range. The histogram in Figure 114 shows that the hysteresis is larger when the device is cycled through only a half cycle, from room temperature to 125°C and back to room temperature.

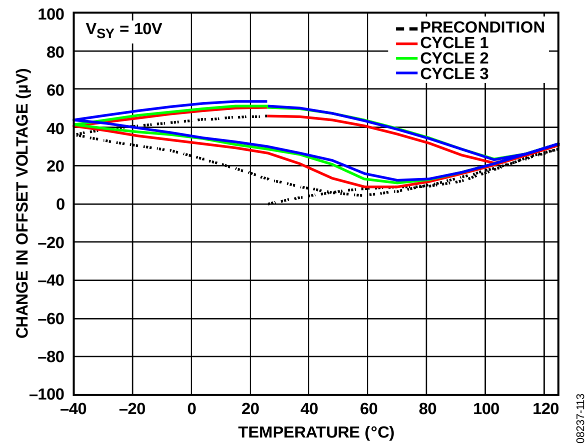

Figure 113. Change in Offset Voltage over Three Full Temperature Cycles

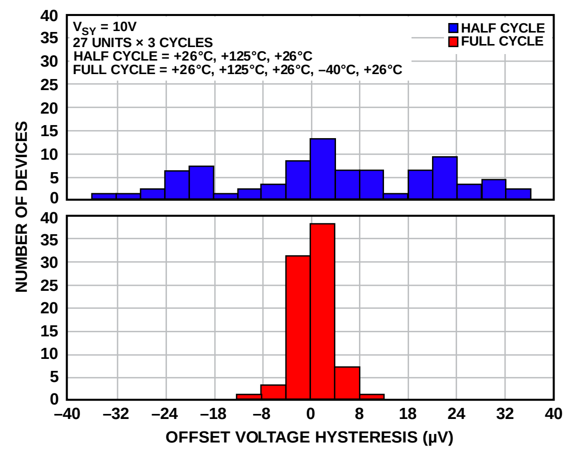

Figure 114. Histogram Showing the Temperature Hysteresis of the Offset Voltage over Three Full Cycles and over Three Half Cycles

OUTLINE DIMENSIONS

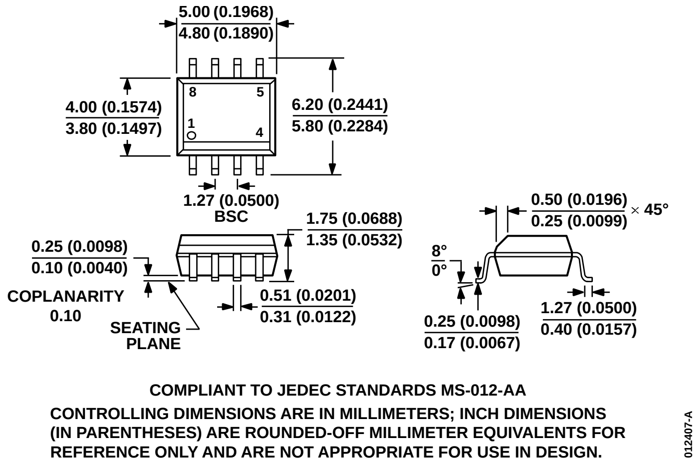

Figure 115. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

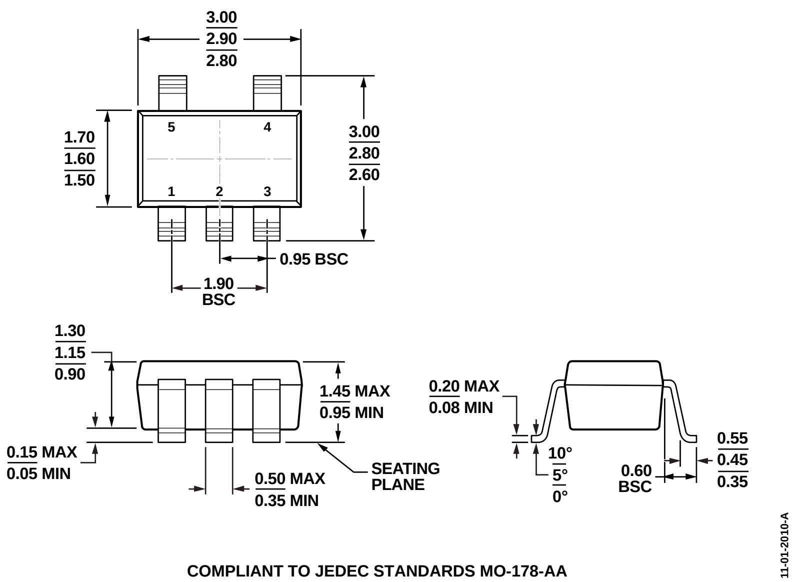

Figure 116. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters

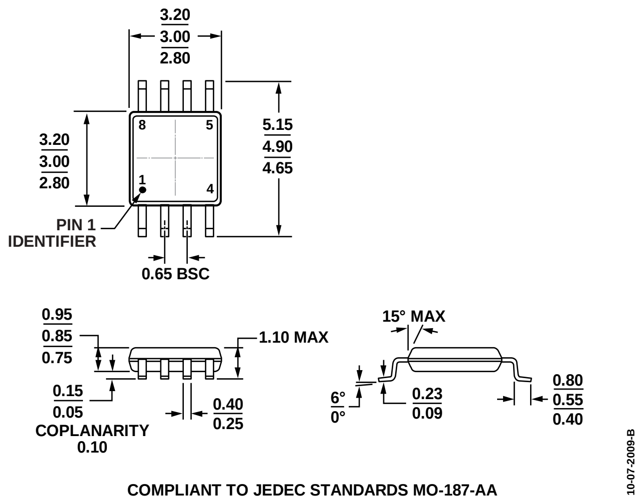

Figure 117. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

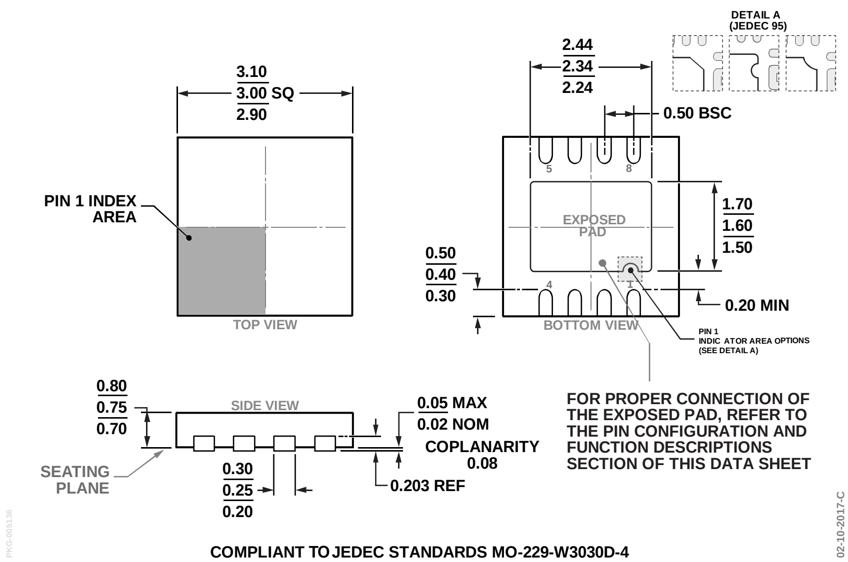

Figure 118. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-11)
Dimensions shown in millimeters

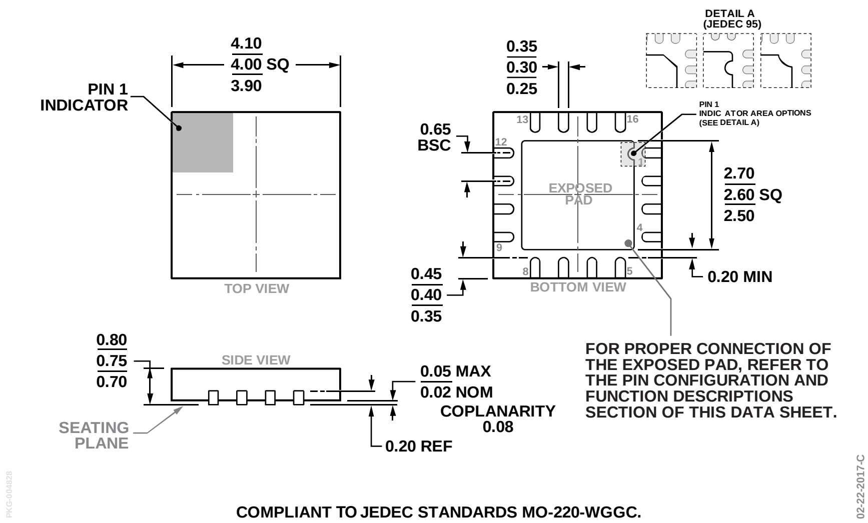

Figure 119. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 075 mm Package Height
(CP-16-17)
Dimensions shown in millimeters

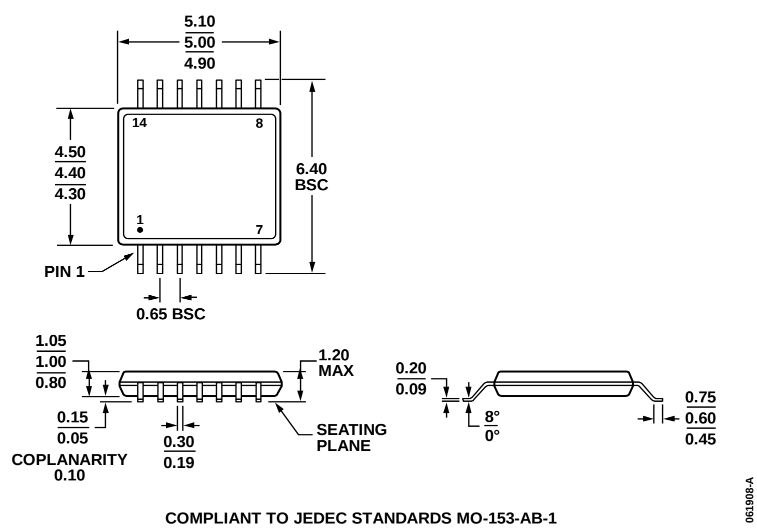

Figure 120. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4084-1ARZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4084-1ARZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4084-1ARZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4084-1ARJZ-R2	−40°C to +125°C	5-Lead Small Outline Transistor Package [SOT-23]	RJ-5	A38
ADA4084-1ARJZ-R7	−40°C to +125°C	5-Lead Small Outline Transistor Package [SOT-23]	RJ-5	A38
ADA4084-1ARJZ-RL	−40°C to +125°C	5-Lead Small Outline Transistor Package [SOT-23]	RJ-5	A38
ADA4084-2ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2Q
ADA4084-2ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2Q
ADA4084-2ARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2Q
ADA4084-2ARZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4084-2ARZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4084-2ARZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4084-2ACPZ-R7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-11	A2Q
ADA4084-2ACPZ-RL	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-11	A2Q
ADA4084-4ACPZ-R7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-17	
ADA4084-4ACPZ-RL	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-17	
ADA4084-4ARUZ	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	
ADA4084-4ARUZ-RL	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14	

[1] Z = RoHS Compliant Part.

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