ANALOG DEVICES

50 V, 130 kHz, 32.5 µA, Robust, Over-The-Top Precision Op Amp

Data Sheet **ADA4097-1**

FEATURES

Ultrawide common-mode input range: $-V_S - 0.1$ V to $-V_S + 70$ V
Wide power supply voltage range: +3 V to +50 V (to ±25 V for PSRR)
Low power supply current: 32.5 µA (typical)
Low input offset voltage: ±60 µV maximum
Low input offset voltage drift: ±1 µV/°C maximum (B grade)
Low input voltage noise
6 Hz typical 1/f noise corner
1000 nV p-p typical at 0.1 Hz to 10 Hz
GBP: 130 kHz typical for f_{TEST} = 250 Hz
Slew rate: 0.1 V/µs typical at ΔV_{OUT} = 4 V
Low power supply current shutdown: 20 µA maximum
Low input offset current: ±300 pA maximum
Large signal voltage gain: 120 dB minimum for ΔV_{OUT} = 4 V
CMRR: 120 dB minimum at V_{CM} = −0.1 V to +70 V
PSRR: 123 dB minimum at V_{SY} = +3 V to ±25 V
Input overdrive tolerant with no phase reversal
±2 kV HBM and ±1.25 kV FICDM
Wide temperature range: −55°C to +150°C (H grade)
6-lead TSOT package

APPLICATIONS

Industrial sensor conditioning
Supply current sensing
Battery and power supply monitoring
Front-end amplifiers in abusive environments
4 mA to 20 mA transmitters

GENERAL DESCRIPTION

The ADA4097-1 is a robust, precision, rail-to-rail input and output operational amplifier (op amp) with inputs that operate from $-V_S$ to $+V_S$ and beyond, which is referred to in this data sheet as Over-The-Top™. The device features offset voltages of <60 µV, input bias currents (I_B) of <0.3 nA, and can operate on single or split supplies that range from 3 V to 50 V. The ADA4097-1 draws 32.5 µA of supply current.

The ADA4097-1 Over-The-Top input stage has robust input protection features for abusive environments. The inputs can tolerate up to 80 V of differential voltage without damage or degradation to dc accuracy. The operating common-mode input range extends from rail-to-rail and beyond, up to 70 V > $-V_S$, independent of the $+V_S$ supply.

The ADA4097-1 is unity-gain stable and can drive loads requiring up to 20 mA. The device can also drive capacitive loads as large as 200 pF. The amplifier is available with low power shutdown.

The ADA4097-1 is available in a standard, 6-lead, thin small outline transistor (TSOT) package.

TYPICAL APPLICATION CIRCUIT

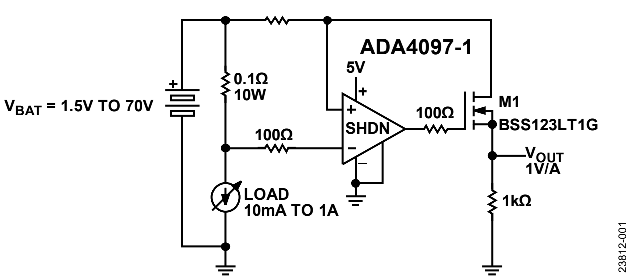

Figure 1. 1 V/A Over-The-Top Current Sense Application (V_{BAT} Is the Battery Voltage.)

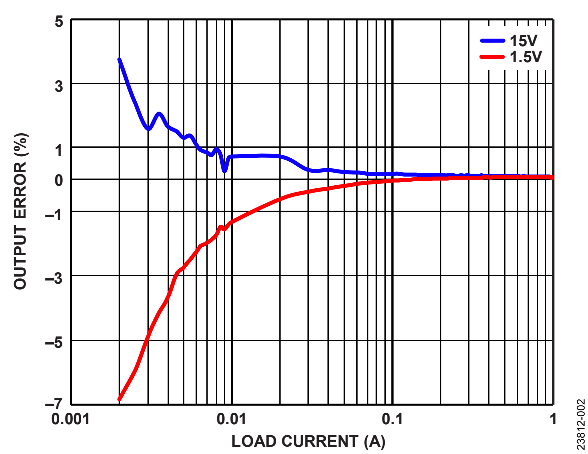

Figure 2. Output Error vs. Load Current

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Typical Application Circuit ... 1
Revision History ... 2
Specifications ... 3
5 V Supply ... 3
±15 V Supply ... 5
Absolute Maximum Ratings ... 8
Maximum Power Dissipation ... 8
Thermal Resistance ... 8
Electrostatic Discharge (ESD) Ratings ... 8
ESD Caution ... 8
Pin Configuration and Function Descriptions ... 9
Typical Performance Characteristics ... 10
Theory of Operation ... 18
Input Protection ... 19
Over-The-Top Operation Considerations ... 19
Output ... 20
Shutdown Pin (SHDN) ... 20
Applications Information ... 21
Large Resistor Gain Operation ... 21
Recommended Values for Various Gains ... 21
Noise ... 22
Distortion ... 22
Power Dissipation and Thermal Shutdown ... 23
Circuit Layout Considerations ... 23
Power Supply Bypassing ... 23
Grounding ... 24
ESD Protection when Powered ... 24
Related Products ... 24
Typical Applications ... 25
Outline Dimensions ... 27
Ordering Guide ... 27

REVISION HISTORY

5/2021—Revision 0: Initial Version

SPECIFICATIONS

5 V SUPPLY

Common-mode voltage (V_{CM}) = 2.5 V, SHDN pin is open, load resistance (R_L) = 499 kΩ to midsupply, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	B Grade Min	B Grade Typ	B Grade Max	H Grade Min	H Grade Typ	H Grade Max	Unit
DC PERFORMANCE								
Input Offset Voltage (V_{OS})[1]	0.25 V < V_{CM} < 3.5 V		±20	±60		±20	±60	µV
	Minimum temperature (T_{MIN}) < T_A < maximum temperature (T_{MAX})			±130			±160	µV
	0.25 V < V_{CM} < 70 V		±30	±60		±30	±60	µV
	T_{MIN} < T_A < T_{MAX}			±160			±185	µV
	−0.1 V < V_{CM} < +70 V		±30	±60		±30	±60	µV
	T_{MIN} < T_A < T_{MAX}			±400			±450	µV
Input Offset Voltage Drift[2]	T_{MIN} < T_A < T_{MAX}		±0.1	±1		±0.1	±1.5	µV/°C
Input Bias Current (I_B)			±0.1	±0.3		±0.1	±0.3	nA
	T_{MIN} < T_A < T_{MAX}			±10			±25	nA
	V_{CM} = 70 V, Over-The-Top	0.25	0.8	1.5	0.25	0.8	1.5	µA
	T_{MIN} < T_A < T_{MAX}	0.175		2.25	0.125		2.5	µA
	0 V < V_{CM} < 70 V, V_{SY} = 0 V		0.001	1		0.001	1	µA
	T_{MIN} < T_A < T_{MAX}			10			10	µA
Input Offset Current (I_{OS})			±100	±300		±100	±300	pA
	T_{MIN} < T_A < T_{MAX}			±5			±10	nA
	V_{CM} = 70 V, Over-The-Top[3]		±0.025	±0.065		±0.025	±0.065	µA
	T_{MIN} < T_A < T_{MAX}			±0.095			±0.15	µA
Common-Mode Rejection Ratio (CMRR)	V_{CM} = −0.1 V to +70 V	120	145		120	145		dB
	T_{MIN} < T_A < T_{MAX}	104			103			dB
	V_{CM} = 0.25 V to 3.5 V	115	134		115	134		dB
	T_{MIN} < T_A < T_{MAX}	110			107			dB
Common-Mode Input Range	Guaranteed by CMRR tests	−0.1		+70	−0.1		+70	V
Large Signal Voltage Gain (A_{OL})	Delta output voltage (ΔV_{OUT}) = 4 V	120	140		120	140		dB
	T_{MIN} < T_A < T_{MAX}	114			112			dB
	ΔV_{OUT} = 4 V, R_L = 10 kΩ	100	108		100	108		dB
	T_{MIN} < T_A < T_{MAX}	94			90			dB
NOISE PERFORMANCE								
Input Voltage Noise	Frequency (f) = 0.1 Hz to 10 Hz		1000			1000		nV p-p
	1/f noise corner		6			6		Hz
	f = 100 Hz		53			53		nV/√Hz
Over-The-Top	f = 100 Hz, V_{CM} > 5 V		65			65		nV/√Hz
Input Current Noise	f = 100 Hz		0.05			0.05		pA/√Hz
Over-The-Top	f = 100 Hz, V_{CM} > 5 V		0.5			0.5		pA/√Hz
DYNAMIC PERFORMANCE								
Slew Rate	ΔV_{OUT} = 4 V	0.025	0.1		0.025	0.1		V/µs
	T_{MIN} < T_A < T_{MAX}	0.018			0.015			V/µs
Gain Bandwidth Product (GBP)	Test frequency (f_{TEST}) = 250 Hz	120	130		120	130		kHz
	T_{MIN} < T_A < T_{MAX}	100			100			kHz

Parameter	Test Conditions/Comments	B Grade			H Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
Phase Margin			58			58		Degrees
1% Settling Time	$\Delta V_{OUT} = \pm 2$ V		70			70		µs
0.1% Settling Time	$\Delta V_{OUT} = \pm 2$ V		100			100		µs
Total Harmonic Distortion Plus Noise (THD + N)	f = 1 kHz, V_{OUT} = 2 V p-p, R_L = 10 kΩ, bandwidth = 80 kHz		0.05			0.05		%
INPUT CHARACTERISTICS								
Input Resistance	Differential mode		10			10		MΩ
	Common mode		>1			>1		GΩ
Over-The-Top	Differential mode, $V_{CM} > 5$ V		60			60		kΩ
	Common mode, $V_{CM} > 5$ V		>1			>1		GΩ
Input Capacitance	Differential mode		1			1		pF
	Common mode		3			3		pF
SHDN PIN								
Input Logic Low	Amplifier active, SHDN pin voltage (V_{SHDN}) < $-V_S + 0.5$ V, $T_{MIN} < T_A < T_{MAX}$			$-V_S + 0.5$			$-V_S + 0.5$	V
Input Logic High	Amplifier shutdown, $V_{SHDN} > -V_S + 1.5$ V, $T_{MIN} < T_A < T_{MAX}$	$-V_S + 1.5$			$-V_S + 1.5$			V
Response Time	Amplifier active to shutdown		2.5			2.5		µs
	Amplifier shutdown to active		100			100		µs
Pull-Down Current	$V_{SHDN} = -V_S + 0.5$ V, $T_{MIN} < T_A < T_{MAX}$		0.6	3		0.6	3	µA
	$V_{SHDN} = -V_S + 1.5$ V, $T_{MIN} < T_A < T_{MAX}$		0.3	2.5		0.3	2.5	µA
OUTPUT CHARACTERISTICS								
Output Voltage Swing Low	Overdrive voltage (V_{OD}[4]) = 30 mV, no load		15	40		15	40	mV
	$T_{MIN} < T_A < T_{MAX}$			45			50	mV
	V_{OD} = 30 mV, sink current (I_{SINK}) = 5 mA		240	325		240	325	mV
	$T_{MIN} < T_A < T_{MAX}$			380			400	mV
Output Voltage Swing High	V_{OD} = 30 mV, no load		2.5	5		2.5	5	mV
	$T_{MIN} < T_A < T_{MAX}$			10			15	mV
	V_{OD} = 30 mV, source current (I_{SOURCE}) = 5 mA		570	700		570	700	mV
	$T_{MIN} < T_A < T_{MAX}$			1000			1100	mV
Short-Circuit Current	I_{SOURCE}	20	30		20	30		mA
	$T_{MIN} < T_A < T_{MAX}$	10			6			mA
	I_{SINK}	35	40		35	40		mA
	$T_{MIN} < T_A < T_{MAX}$	10			6			mA
Output Pin Leakage During Shutdown	$V_{SHDN} = -V_S + 1.5$ V		±5	±100		±5	±100	nA
	$T_{MIN} < T_A < T_{MAX}$			±10			±10	µA

Parameter	Test Conditions/Comments	B Grade Min	B Grade Typ	B Grade Max	H Grade Min	H Grade Typ	H Grade Max	Unit
POWER SUPPLY								
Maximum Operating Voltage[5]				50			50	V
Voltage Range (V_{SY})	Guaranteed by power supply rejection ratio (PSRR)	3		50	3		50	V
Supply Current	Amplifier active		32.5	36		32.5	36	µA
	$T_{MIN} < T_A < T_{MAX}$			55			60	µA
	Amplifier shutdown, $V_{SHDN} = -V_S + 1.5$ V		12	20		12	20	µA
	$T_{MIN} < T_A < T_{MAX}$			22.5			22.5	µA
PSRR	V_{SY} = +3 V to ±25 V	123	145		123	145		dB
	$T_{MIN} < T_A < T_{MAX}$	120			120			dB
THERMAL SHUTDOWN[6]								
Temperature	T_J		175			175		°C
Hysteresis			20			20		°C
Operating Temperature	T_A	−40		+125	−55		+150	°C

[1] Thermoelectric voltages present in the high speed production test limit the measurement accuracy of this parameter. The limits shown in Table 1 are determined by test capability and are not necessarily indicative of actual device performance.
[2] Offset voltage drift is guaranteed through lab characterization and is not production tested.
[3] Test accuracy is limited by high speed production test equipment repeatability. Bench measurements indicate that the input offset current in Over-The-Top configuration is typically controlled to under 50 nA at +25°C and 100 nA over the −55°C < T_A < +150°C temperature range.
[4] V_{OD} is +30 mV for V_{OUT} high and −30 mV for V_{OUT} low.
[5] Maximum operating voltage is limited by the time-dependent dielectric breakdown (TDDB) of the on-chip capacitor oxides. The amplifier tolerates temporary transient overshoot up to the specified absolute maximum rating, but the dc supply voltage must be limited to the maximum operating voltage.
[6] Thermal shutdown is lab characterized only and is not tested in production.

±15 V SUPPLY

V_{CM} = 0 V, SHDN pin is open, R_L = 499 kΩ to ground, and T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	B Grade Min	B Grade Typ	B Grade Max	H Grade Min	H Grade Typ	H Grade Max	Unit
DC PERFORMANCE								
V_{OS}[1]			±20	±60		±20	±60	µV
	$T_{MIN} < T_A < T_{MAX}$			±150			±175	µV
	V_{SY} = ±25 V		±20	±60		±20	±60	µV
	$T_{MIN} < T_A < T_{MAX}$			±150			±175	µV
Input Offset Voltage Drift[2]	$T_{MIN} < T_A < T_{MAX}$		±0.1	±1		±0.1	±1.5	µV/°C
I_B			±0.1	±0.3		±0.1	±0.3	nA
	$T_{MIN} < T_A < T_{MAX}$			±10			±25	nA
	V_{SY} = ±25 V		±0.1	±0.3		±0.1	±0.3	nA
	$T_{MIN} < T_A < T_{MAX}$			±10			±25	nA
I_{OS}			±0.1	±0.3		±0.1	±0.3	nA
	$T_{MIN} < T_A < T_{MAX}$			±5			±10	nA
	V_{SY} = ±25 V		±0.1	±0.3		±0.1	±0.3	nA
	$T_{MIN} < T_A < T_{MAX}$			±5			±10	nA

Parameter	Test Conditions/Comments	B Grade Min	B Grade Typ	B Grade Max	H Grade Min	H Grade Typ	H Grade Max	Unit
CMRR	V_{CM} = −14.75 V to +13.5 V	117	135		117	135		dB
	$T_{MIN} < T_A < T_{MAX}$	109			109			dB
	V_{CM} = −15.1 V to +13.5 V	117	135		117	135		dB
	$T_{MIN} < T_A < T_{MAX}$	99			95			dB
	V_{CM} = −15.1 V to +55 V	117	140		117	140		dB
	$T_{MIN} < T_A < T_{MAX}$	103			103			dB
Common-Mode Input Range	Guaranteed by CMRR tests	−15.1		+55	−15.1		+55	V
A_{OL}	ΔV_{OUT} = 25 V	120	150		120	150		dB
	$T_{MIN} < T_A < T_{MAX}$	114			112			dB
	ΔV_{OUT} = 25 V, R_L = 10 kΩ	100	108		100	108		dB
	$T_{MIN} < T_A < T_{MAX}$	94			90			dB
NOISE PERFORMANCE								
Input Voltage Noise	f = 0.1 Hz to 10 Hz		1			1		µV p-p
	1/f noise corner		6			6		Hz
	f = 100 Hz		53			53		nV/√Hz
Over-The-Top	f = 100 Hz, V_{CM} > $+V_S$		65			65		nV/√Hz
Input Current Noise	f = 100 Hz		0.05			0.05		pA/√Hz
Over-The-Top	f = 100 Hz, V_{CM} > $+V_S$		0.5			0.5		pA/√Hz
DYNAMIC PERFORMANCE								
Slew Rate	ΔV_{OUT} = 25 V	0.03	0.1		0.03	0.1		V/µs
	$T_{MIN} < T_A < T_{MAX}$	0.02			0.015			V/µs
GBP	f_{TEST} = 250 Hz	125	130		125	130		kHz
	$T_{MIN} < T_A < T_{MAX}$	100			100			kHz
Phase Margin			59			59		Degrees
1% Settling Time	ΔV_{OUT} = ±2 V		70			70		µs
0.1% Settling Time	ΔV_{OUT} = ±2 V		100			100		µs
THD + N	f = 1 kHz, V_{OUT} = 5.6 V p-p, R_L = 10 kΩ, bandwidth = 80 kHz		0.1			0.1		%
INPUT CHARACTERISTICS								
Input Resistance	Differential mode		10			10		MΩ
	Common mode		>1			>1		GΩ
Input Capacitance	Differential mode		1			1		pF
	Common mode		3			3		pF
SHDN PIN								
Input Logic Low	Amplifier active, V_{SHDN} < $-V_S$ + 0.5 V			$-V_S$ + 0.5			$-V_S$ + 0.5	V
Input Logic High	Amplifier shutdown, V_{SHDN} > $-V_S$ + 1.5 V	$-V_S$ + 1.5			$-V_S$ + 1.5			V
Response Time	Amplifier active to shutdown		2.5			2.5		µs
	Amplifier shutdown to active		100			100		µs
Pull-Down Current	V_{SHDN} = $-V_S$ + 0.5 V, $T_{MIN} < T_A < T_{MAX}$		0.3	3		0.3	3	µA
	V_{SHDN} = $-V_S$ + 1.5 V, $T_{MIN} < T_A < T_{MAX}$		0.6	2.5		0.6	2.5	µA

Parameter	Test Conditions/Comments	B Grade Min	B Grade Typ	B Grade Max	H Grade Min	H Grade Typ	H Grade Max	Unit
OUTPUT CHARACTERISTICS								
Output Voltage Swing Low	V_{OD}[3] = 30 mV, no load		15	40		15	40	mV
	$T_{MIN} < T_A < T_{MAX}$			45			50	mV
	V_{OD} = 30 mV, I_{SINK} = 5 mA		240	325		240	325	mV
	$T_{MIN} < T_A < T_{MAX}$			380			400	mV
Output Voltage Swing High	V_{OD} = 30 mV, no load		2.5	10		2.5	10	mV
	$T_{MIN} < T_A < T_{MAX}$			15			20	mV
	V_{OD} = 30 mV, I_{SOURCE} = 5 mA		570	700		570	700	mV
	$T_{MIN} < T_A < T_{MAX}$			1000			1100	mV
Short-Circuit Current	I_{SOURCE}	20	30		20	30		mA
	$T_{MIN} < T_A < T_{MAX}$	10			6			mA
	I_{SINK}	35	45		35	45		mA
	$T_{MIN} < T_A < T_{MAX}$	10			6			mA
POWER SUPPLY								
Maximum Operating Voltage[4]				50			50	V
Voltage Range	Guaranteed by PSRR	3		50	3		50	V
Supply Current	Amplifier active		40	44		40	44	µA
	$T_{MIN} < T_A < T_{MAX}$			65			70	µA
	$V_{SY} = \pm 25$ V		42	48		42	48	µA
	$T_{MIN} < T_A < T_{MAX}$			70			75	µA
	Amplifier shutdown, $V_{SHDN} = -V_S + 1.5$ V		15	22.5		15	22.5	µA
	$T_{MIN} < T_A < T_{MAX}$			25			25	µA
PSRR	V_{SY} = 3 V to 50 V	123	145		123	145		dB
	$T_{MIN} < T_A < T_{MAX}$	120			120			dB
THERMAL SHUTDOWN[5]								
Temperature	T_J		175			175		°C
Hysteresis			20			20		°C
Operating Temperature	T_A	−40		+125	−55		+150	°C

[1] Thermoelectric voltages present in the high speed production test limit the measurement accuracy of this parameter. The limits shown in Table 2 are determined by test capability and are not necessarily indicative of actual device performance.
[2] Offset voltage drift is guaranteed through lab characterization and is not production tested.
[3] V_{OD} is +30 mV for V_{OUT} high and −30 mV for V_{OUT} low.
[4] Maximum operating voltage is limited by the TDDB of the on-chip capacitor oxides. The amplifier tolerates temporary transient overshoot up to the specified absolute maximum rating and the dc supply voltage must be limited to the maximum operating voltage.
[5] Thermal shutdown is lab characterized only and is not tested in production.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage[1]	
Transient	60 V
Continuous	50 V
Power Dissipation (P_D)	See Figure 3
Differential Input Voltage	±80 V
±IN Pin Voltage	
Continuous	−10 V to +80 V
Survival	−15 V to +80 V
±IN Pin Current	10 mA
SHDN Pin Voltage	−0.3 V to +60 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
T_J	175°C

[1] Maximum supply voltage is limited by the TDDB of the on-chip capacitor oxides. The amplifier tolerates temporary transient overshoot up to the specified transient maximum rating. The continuous operating supply voltage must be limited to no more than 50 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

T_J exceeding 125°C promotes accelerated aging. The ADA4097-1 demonstrates ±25 V supply operation beyond 1000 hours at T_A = 150°C.

MAXIMUM POWER DISSIPATION

The maximum safe P_D on the device is limited by the associated rise in either T_C or T_J on the die. At approximately T_C = 150°C, which is the glass transition temperature, the properties of the plastic changes. Exceeding this temperature limit, even temporarily, may change the stresses that the package exerts on the die, which permanently shifts the parametric performance of the ADA4097-1. Exceeding T_J = 175°C for an extended period may result in changes in the silicon devices and may potentially cause failure of the device.

The P_D on the package is the sum of the quiescent power dissipation and the power dissipated in the package due to the output load drive. The quiescent power is expressed as $V_{SY} \times I_{SY}$, where I_{SY} is the quiescent current.

The P_D due to the load drive depends on the application. The P_D due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing $θ_{JA}$. Additional metal that is directly in contact with the package leads from metal traces through vias, ground, and power planes reduces $θ_{JA}$.

Figure 3 shows the maximum P_D vs. T_A for the single and dual 6-lead TSOT packages on a JEDEC standard, 4-layer board, with $-V_S$ connected to a pad that is thermally connected to a printed circuit board (PCB) plane. $θ_{JA}$ values are approximations.

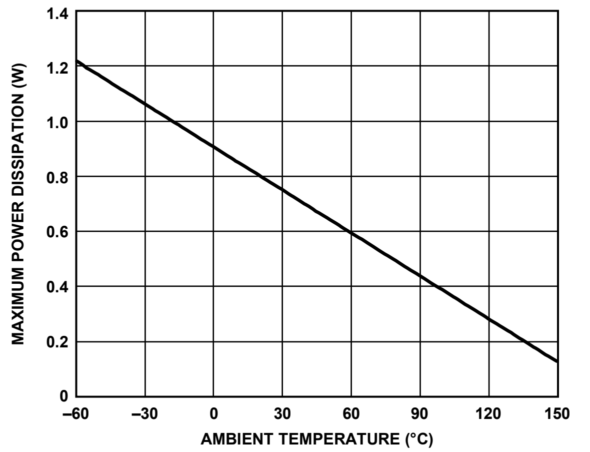


Figure 3. Maximum Power Dissipation vs. Ambient Temperature

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

$θ_{JA}$ is the junction to ambient thermal resistance.

Table 4. Thermal Resistance

Package Type	$θ_{JA}$	Unit
UJ-6	192	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

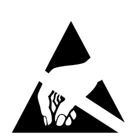
Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADA4097-1

Table 5. ADA4097-1, 6-Lead TSOT

ESD Model	Withstand Threshold	Class
HBM	±2 kV	3A
FICDM	±1.25 kV	3

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

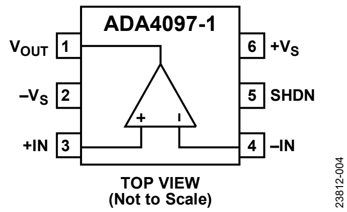


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{OUT}	Amplifier Output.
2	$-V_S$	Negative Power Supply. In single-supply applications, the $-V_S$ pin is normally soldered to a low impedance ground plane. In split-supply applications, bypass the $-V_S$ pin with a capacitance of at least 0.1 µF to a low impedance ground plane, as close to the $-V_S$ pin as possible.
3	+IN	Noninverting Input of the Amplifier.
4	−IN	Inverting Input of the Amplifier.
5	SHDN	Op Amp Shutdown. The threshold for shutdown is approximately 1 V above the negative supply. If the SHDN pin is not connected or hard tied to $-V_S$, the amplifier is active. If the SHDN pin is asserted high ($V_{SHDN} > -V_S + 1.5$ V), the amplifier is placed in a shutdown state, and the output of the amplifier goes to a high impedance state. If the SHDN pin is left unconnected, it is recommended to connect a small capacitor of 1 nF between the SHDN pin and the $-V_S$ pin to prevent signals from the −IN pin from capacitively coupling to the SHDN pin.
6	$+V_S$	Positive Power Supply. Bypass the $+V_S$ pin with a capacitance of at least 0.1 µF to a low impedance ground plane, as close to the $+V_S$ pin as possible.

TYPICAL PERFORMANCE CHARACTERISTICS

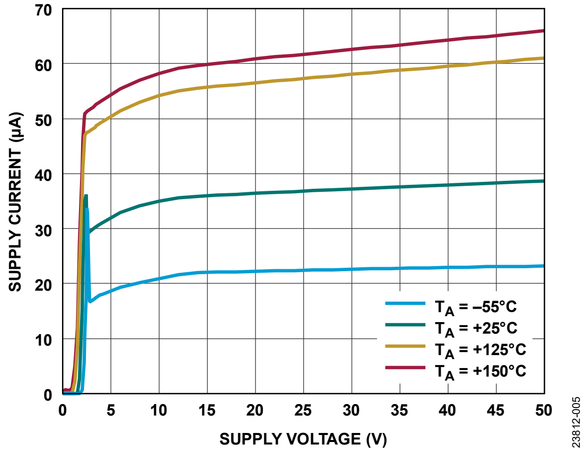


Figure 5. Supply Current vs. Supply Voltage

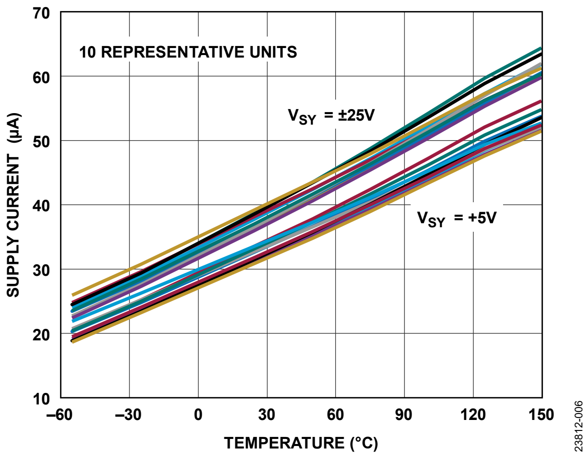


Figure 6. Supply Current vs. Temperature Across Various Supply Voltages

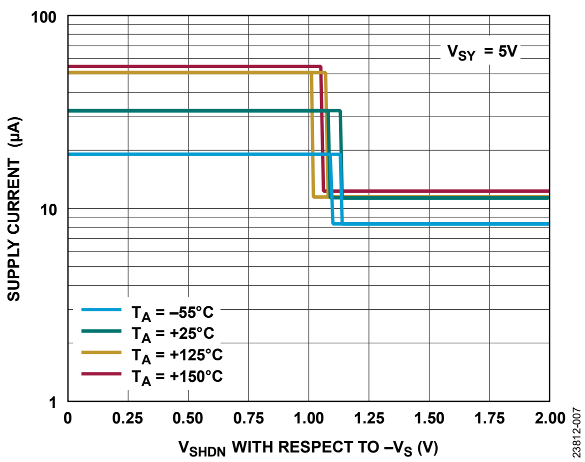


Figure 7. Supply Current vs. V_{SHDN} with Respect to $-V_S$

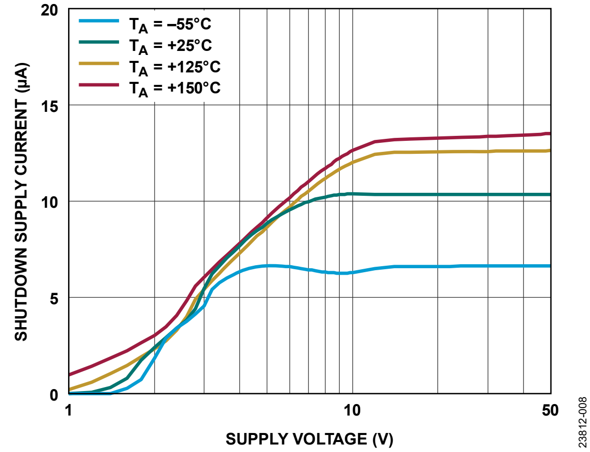


Figure 8. Shutdown Supply Current vs. Supply Voltage

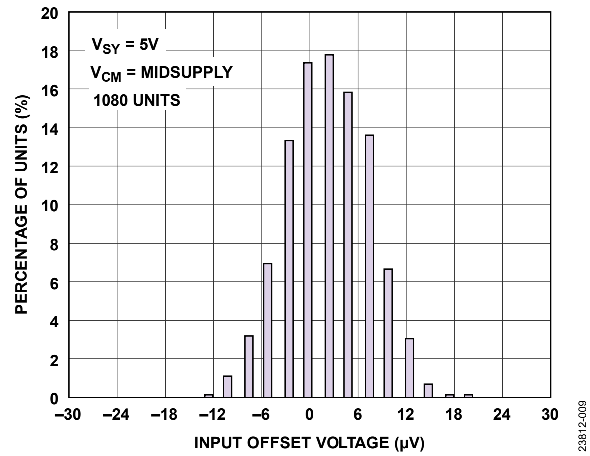


Figure 9. Typical Distribution of Input Offset Voltage, V_{SY} = 5 V

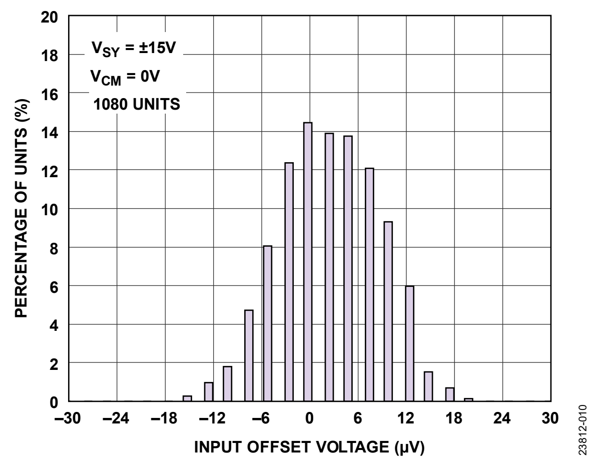


Figure 10. Typical Distribution of Input Offset Voltage with V_{SY} = ±15 V

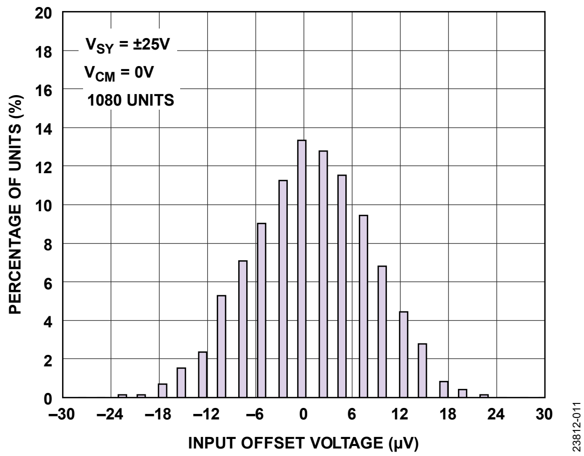


Figure 11. Typical Distribution of Input Offset Voltage with V_{SY} = ±25 V

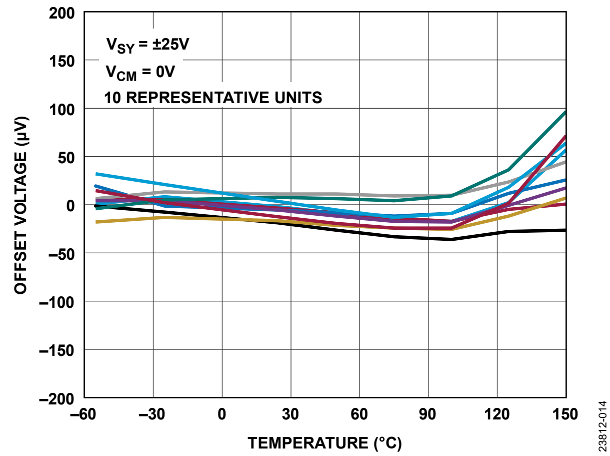


Figure 14. Offset Voltage vs. Temperature with V_{SY} = ±25 V

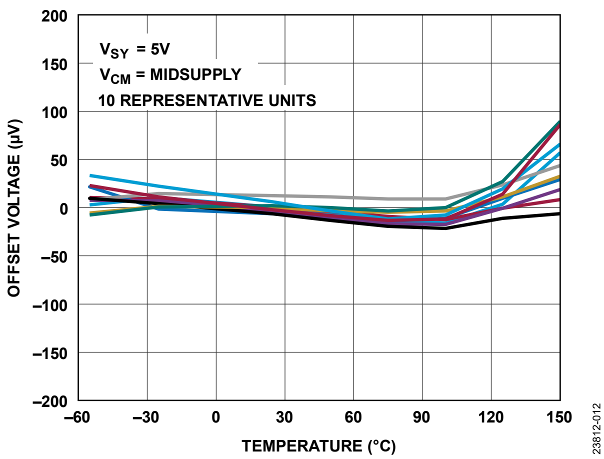


Figure 12. Midsupply Offset Voltage vs. Temperature with V_{SY} = 5 V

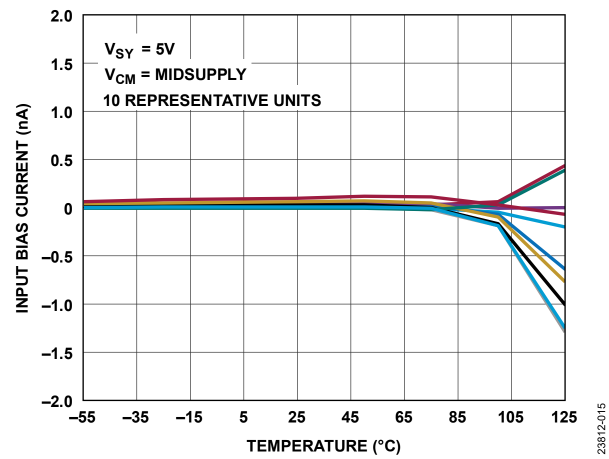


Figure 15. Midsupply Input Bias Current vs. Temperature with V_{SY} = 5 V

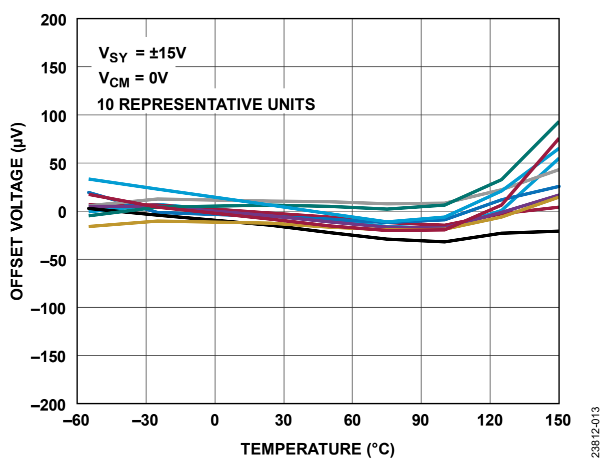


Figure 13. Offset Voltage vs. Temperature with V_{SY} = ±15 V

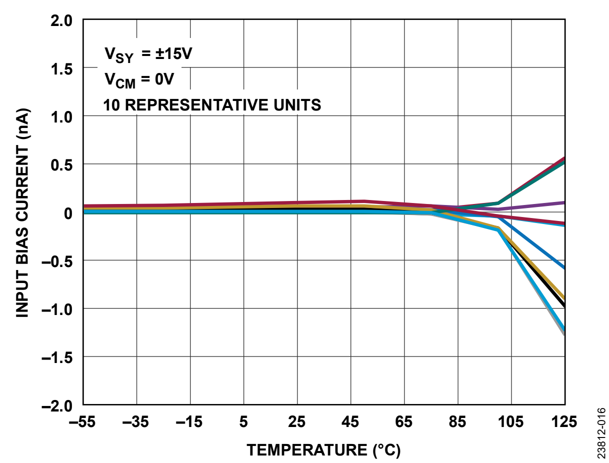


Figure 16. Input Bias Current vs. Temperature with V_{SY} = ±15 V

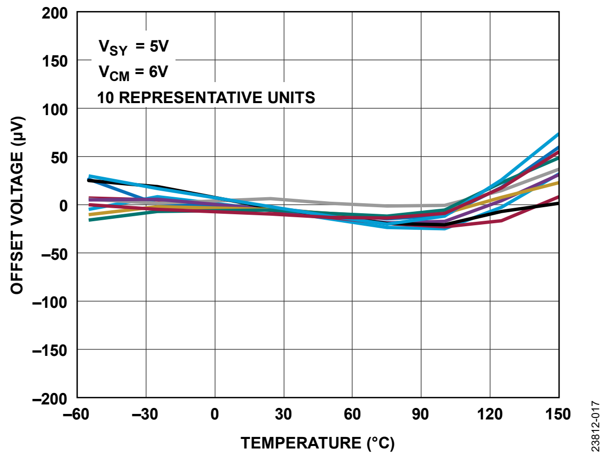


Figure 17. Offset Voltage vs. Temperature with V_{CM} = 6 V, Over-The-Top

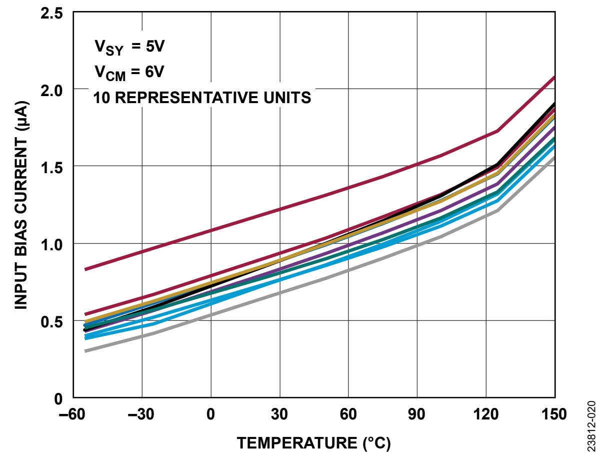


Figure 20. Input Bias Current vs. Temperature with V_{CM} = 6 V, Over-The-Top

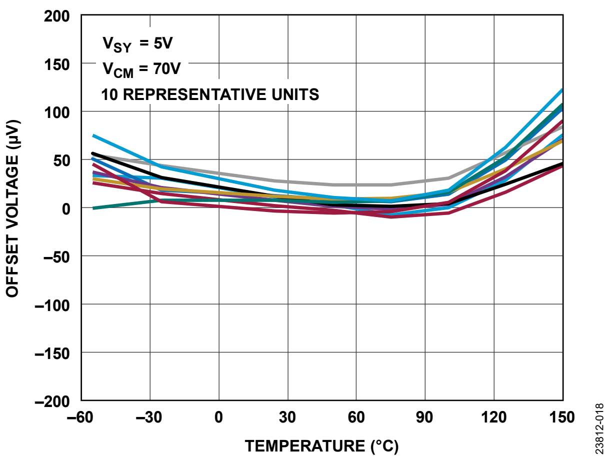


Figure 18. Offset Voltage vs. Temperature with V_{CM} = 70 V

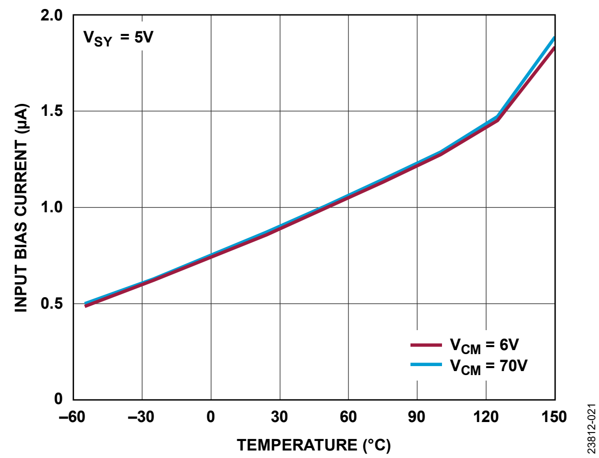


Figure 21. Input Bias Current vs. Temperature Across Various V_{CM}

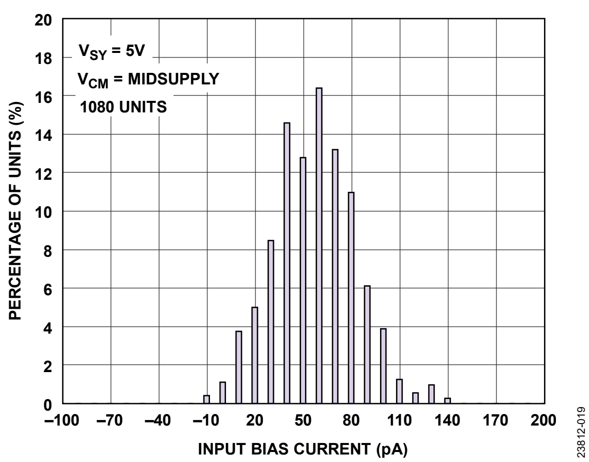


Figure 19. Typical Distribution of Input Bias Current, V_{SY} = 5 V

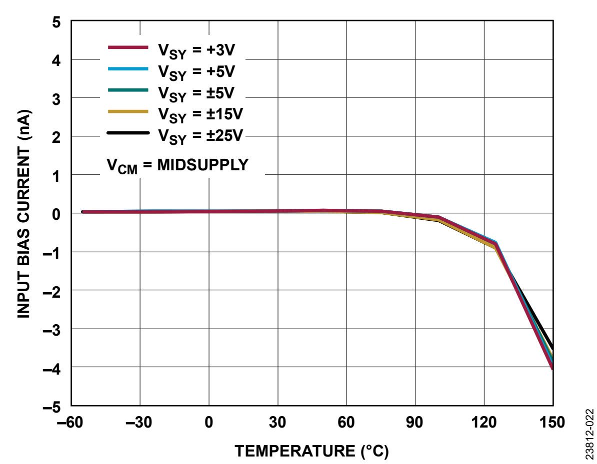


Figure 22. Input Bias Current vs. Temperature Across Various Supply Voltages

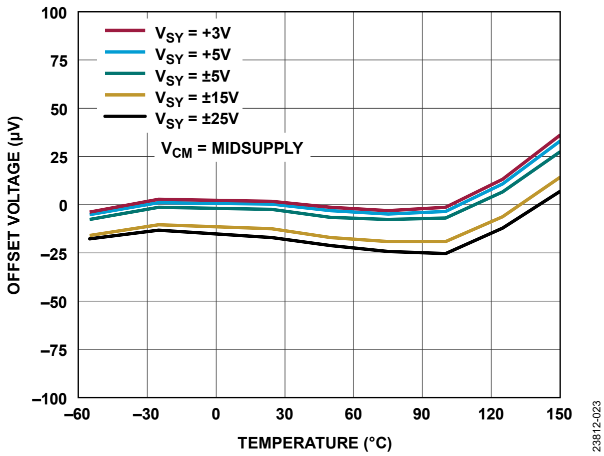


Figure 23. Offset Voltage vs. Temperature Across Various Supply Voltages

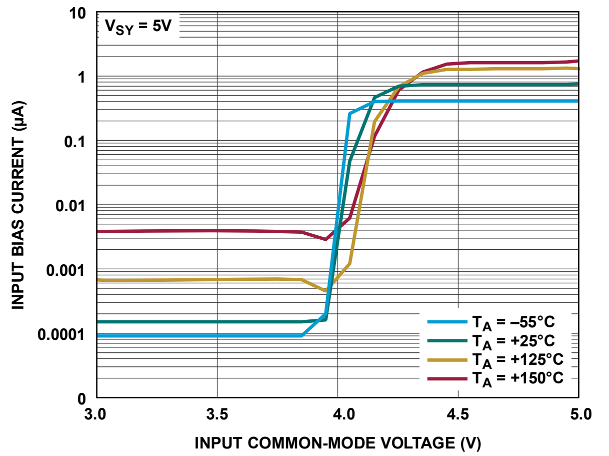


Figure 26. Input Bias Current vs. Input Common-Mode Voltage from Normal Operation to Over-The-Top Operation

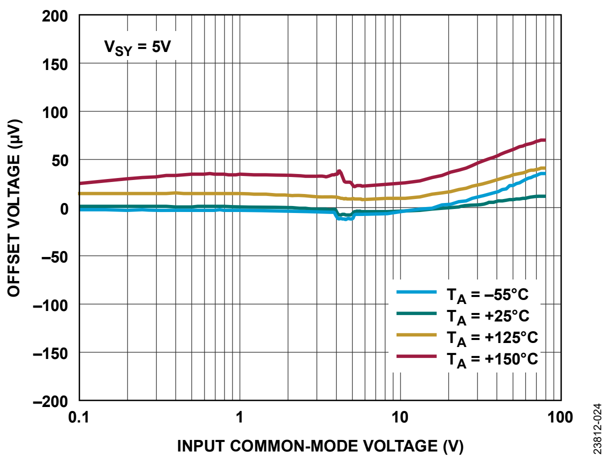


Figure 24. Offset Voltage vs. Input Common-Mode Voltage from Normal Operation to Over-The-Top Operation

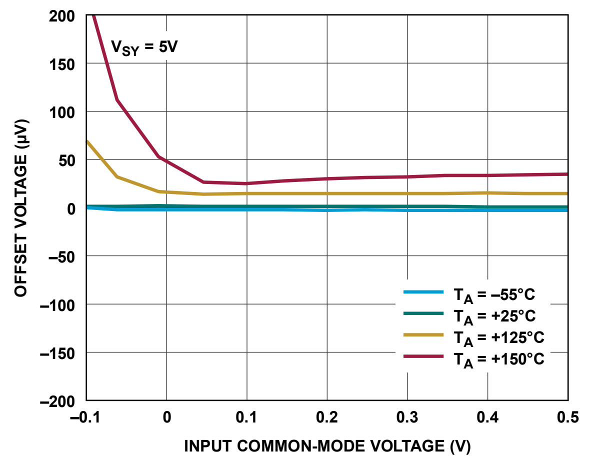


Figure 27. Offset Voltage vs. Input Common-Mode Voltage for Ground Sensing Applications

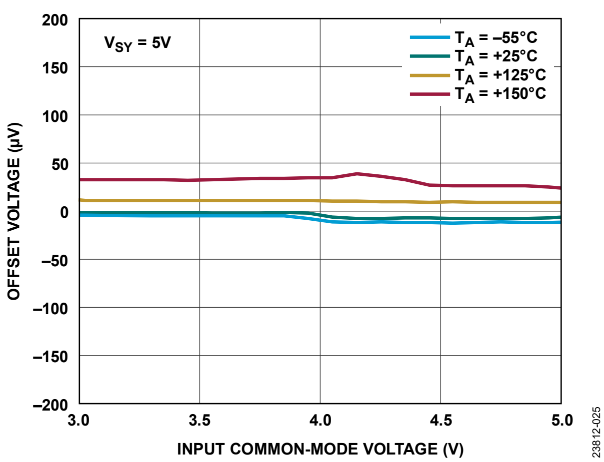


Figure 25. Offset Voltage vs. Input Common-Mode Voltage over the Input Common-Mode Range

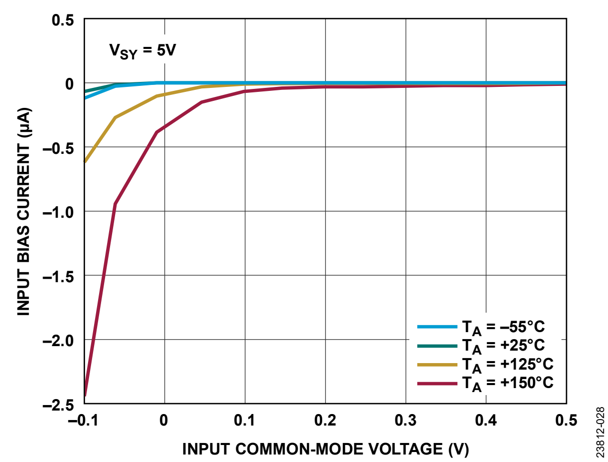


Figure 28. Input Bias Current vs. Input Common-Mode Voltage for Ground Sensing Applications

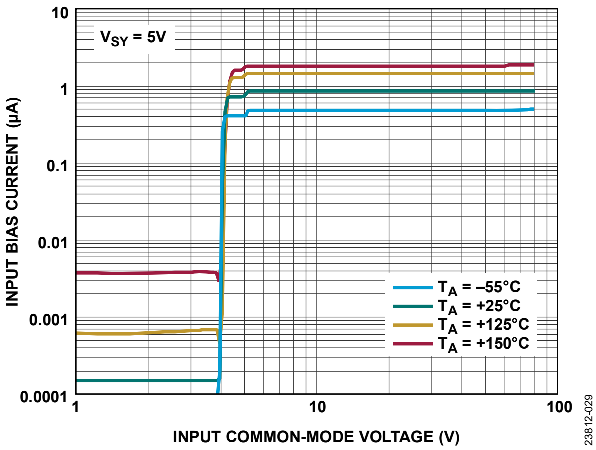


Figure 29. Input Bias Current vs. Input Common-Mode Voltage

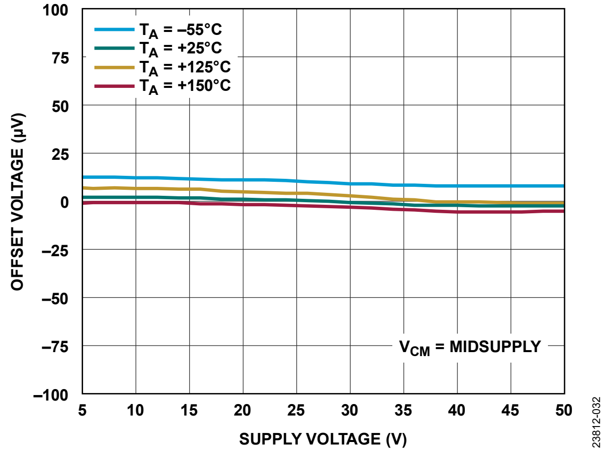


Figure 32. Offset Voltage vs. Supply Voltage

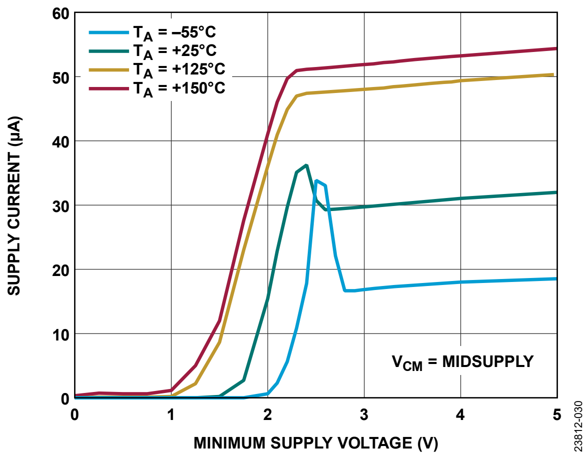


Figure 30. Supply Current vs. Minimum Supply Voltage

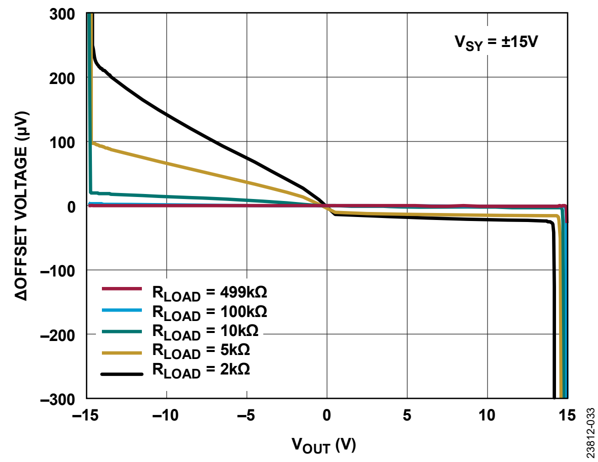


Figure 33. ΔOffset Voltage vs. V_{OUT} Across Various R_{LOAD}

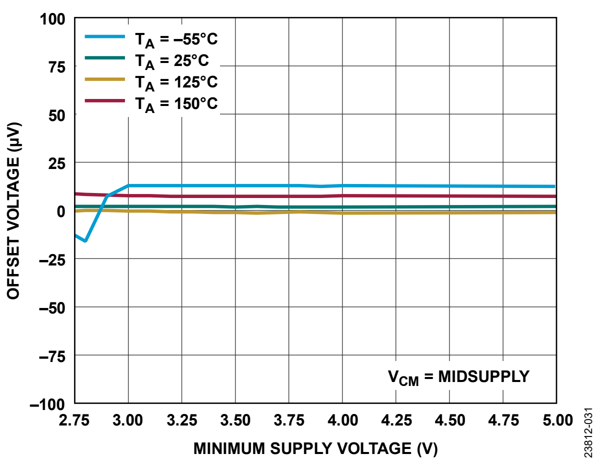


Figure 31. Offset Voltage vs. Minimum Supply Voltage

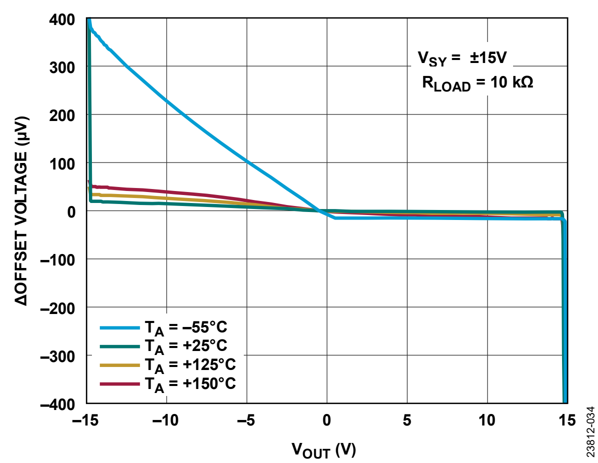


Figure 34. ΔOffset Voltage vs. V_{OUT} Across Various Temperatures

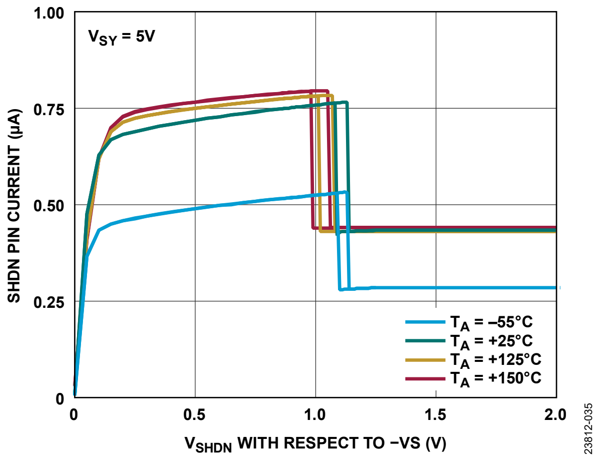


Figure 35. SHDN Pin Current (I_{SHDN}) vs. V_{SHDN} with Respect to $-V_S$ over Various Temperatures

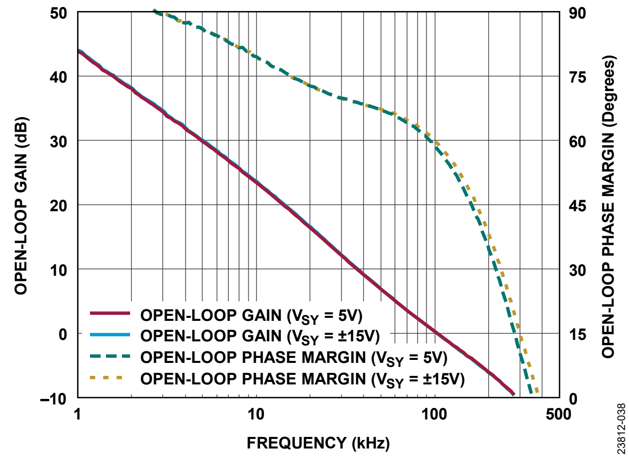


Figure 38. Open-Loop Gain and Open-Loop Phase Margin vs. Frequency

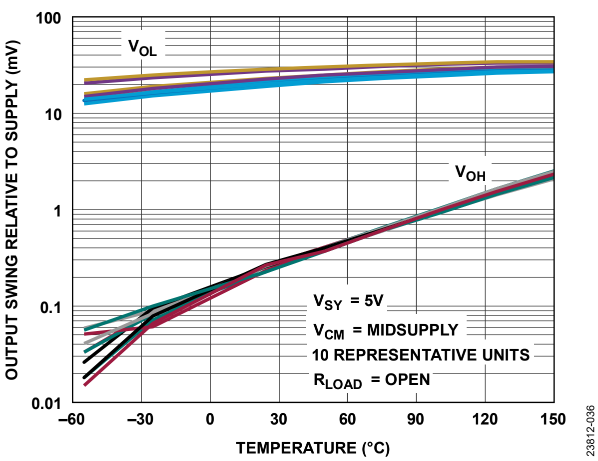


Figure 36. Output Swing Relative to Supply vs. Temperature

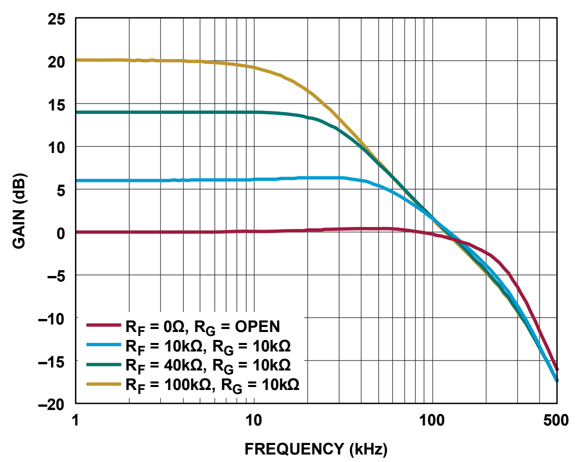


Figure 39. Noninverting Small Signal Frequency Response

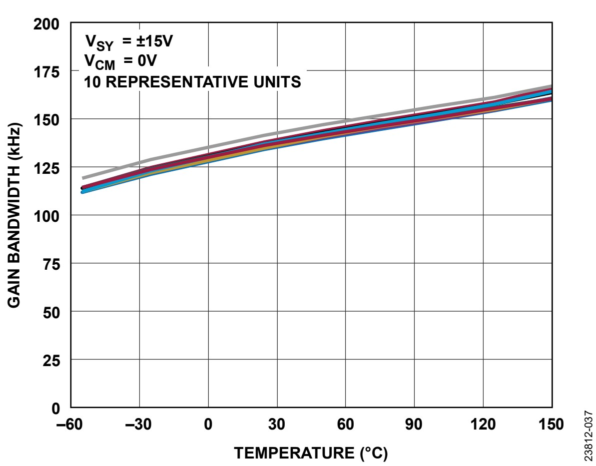


Figure 37. Gain Bandwidth vs. Temperature

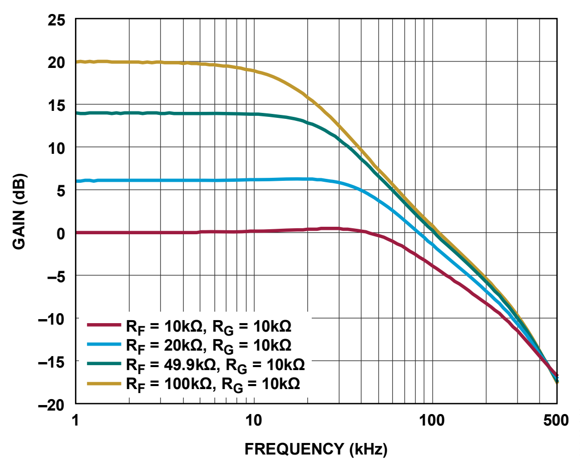


Figure 40. Inverting Small Signal Frequency Response

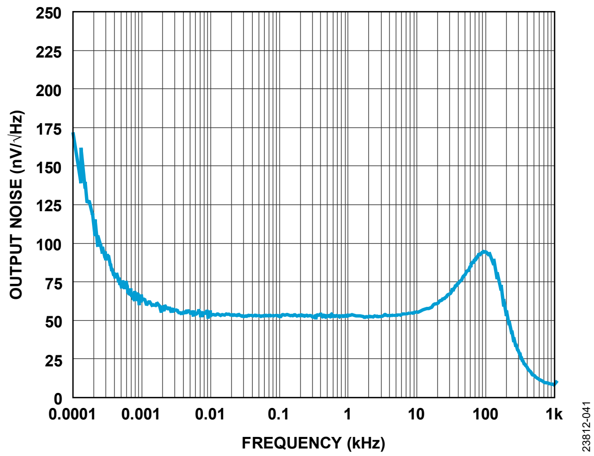


Figure 41. Output Noise vs. Frequency

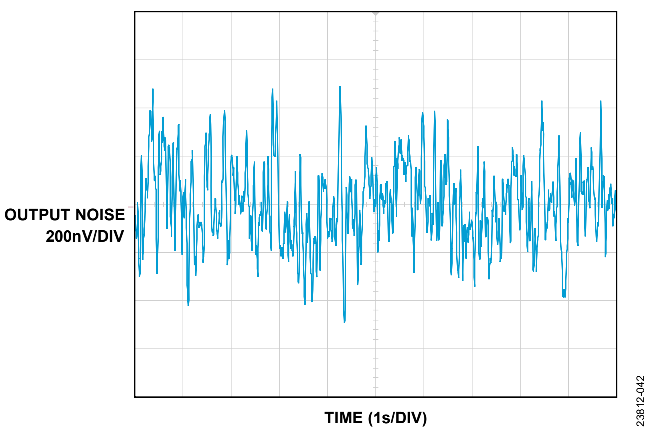


Figure 42. 0.1 Hz to 10 Hz Noise

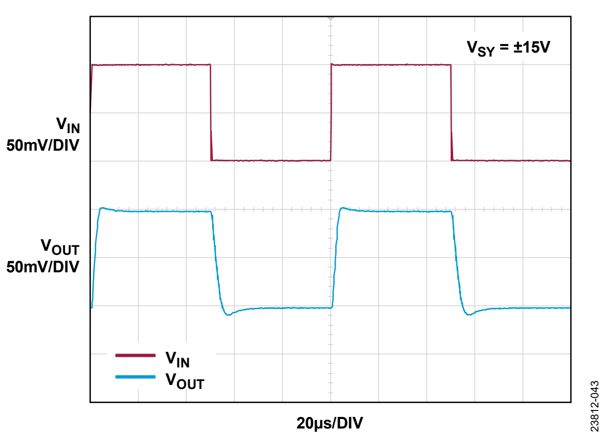


Figure 43. Unity-Gain Small Signal Step Response

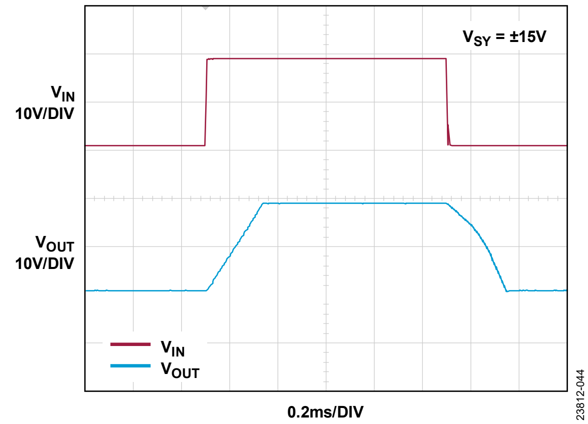


Figure 44. Unity-Gain Large Signal Step Response

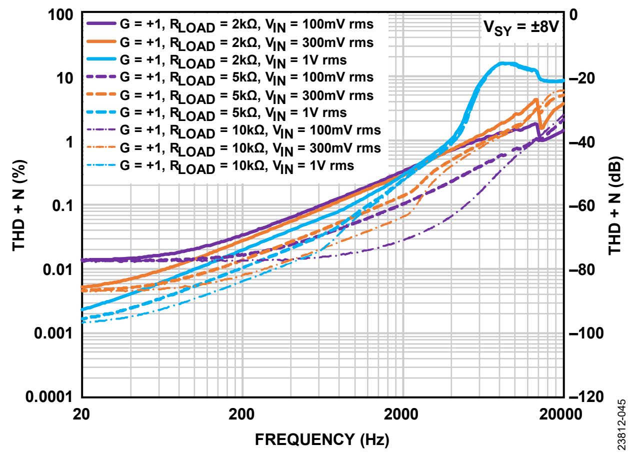


Figure 45. THD + N vs. Frequency over Load

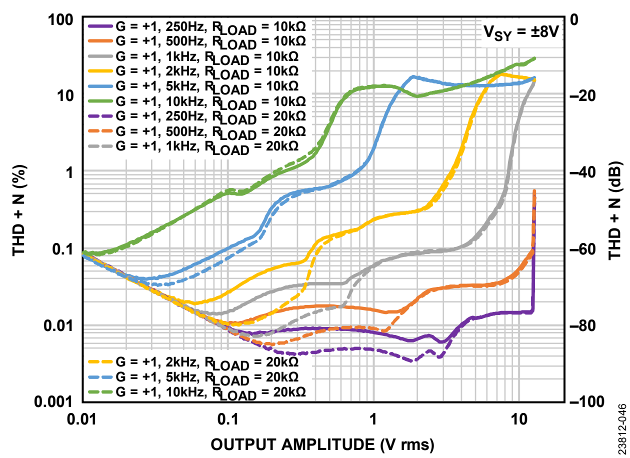


Figure 46. THD + N vs. Output Amplitude

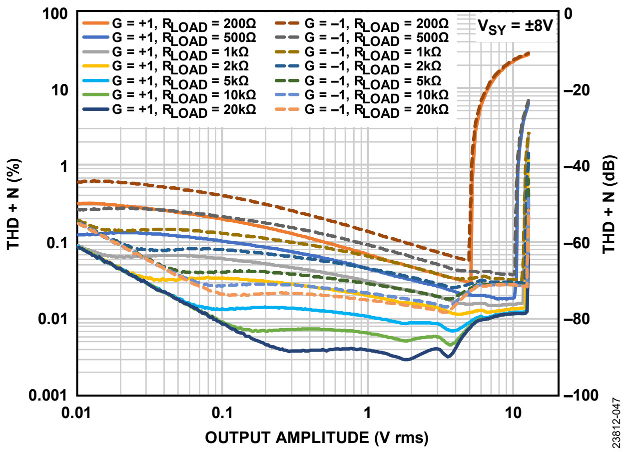


Figure 47. THD + N vs. Output Amplitude and Load

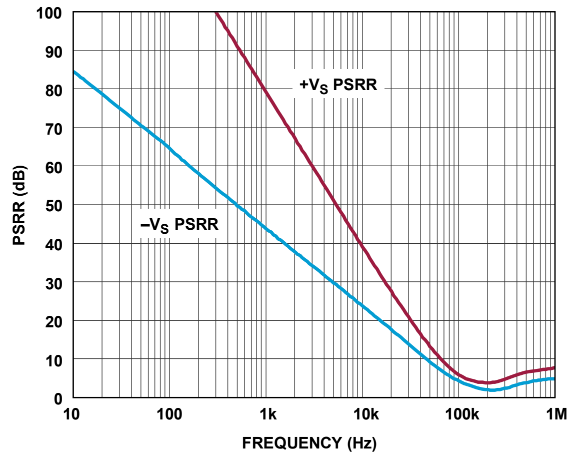


Figure 49. PSRR vs. Frequency

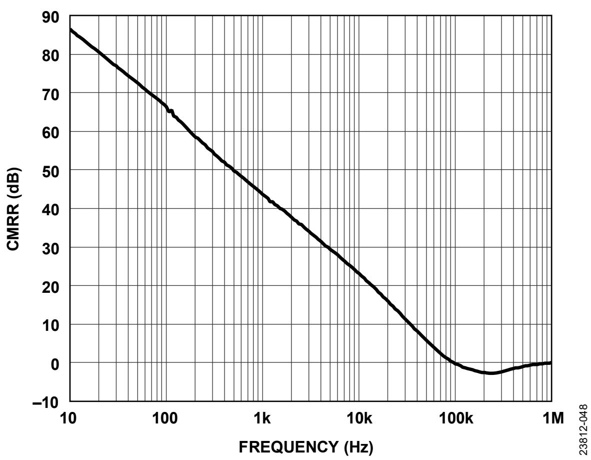


Figure 48. CMRR vs. Frequency

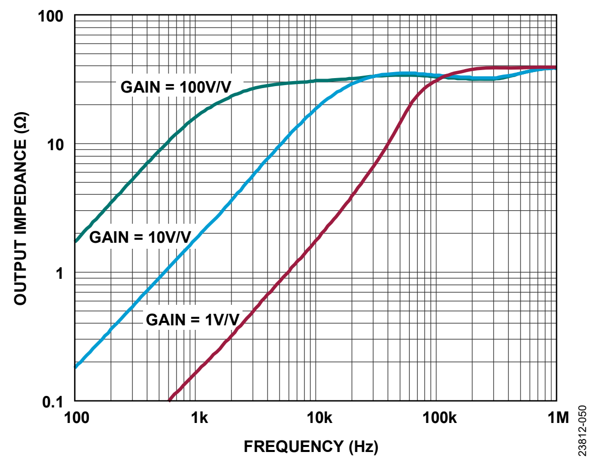


Figure 50. Output Impedance vs. Frequency

THEORY OF OPERATION

The ADA4097-1 is a robust, voltage feedback amplifier that combines unity-gain stability with low offset, low offset drift, and 53 nV/√Hz of input voltage noise. Figure 53 shows a simplified schematic of the device. The ADA4097-1 has two input stages: a common emitter differential input stage consisting of the Q1 and Q2 PNP transistors that operate with the inputs biased between $-V_S$ and 1 V below $+V_S$, and a common base input stage that consists of the Q3 to Q6 PNP transistors that operate when the common-mode input is biased $>+V_S - 1$ V. These input stages result in two distinct operating regions, as shown in Figure 51.

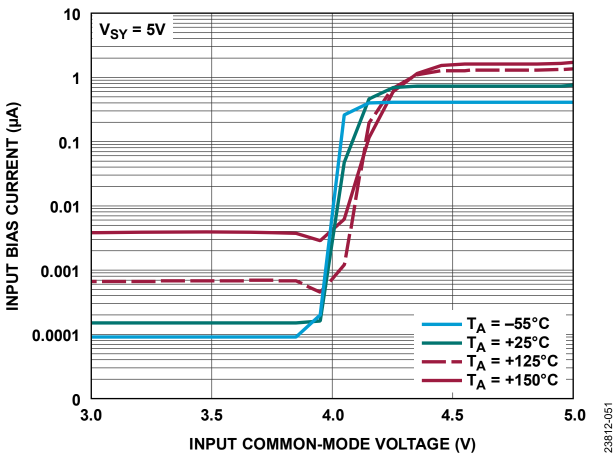


Figure 51. Input Bias Current vs. Input Common-Mode Voltage over Temperature, V_{SY} = 5 V

For common-mode input voltages that are approximately 1 V below the $+V_S$ supply, where Q1 and Q2 are active (see Figure 51), the common emitter PNP input stage is active and the input bias current is typically <0.3 nA. When the common-mode input is above $+V_S - 1$ V, the Q9 transistor turns on, which diverts bias current away from the common emitter differential input pair to the mirror that consists of M3 and M4. The current from M4 biases the common base differential input pair (Q3 to Q6). The Over-The-Top input pair operates in a common base configuration and the input bias current increases to ~0.8 µA. The offset voltages of both input stages are tightly trimmed and are specified in Table 1 and Table 2.

As the input common-mode transitions to the Over-The-Top region, the input CMRR degrades slightly when compared to the rest of the input common-mode range, as shown in Figure 52.

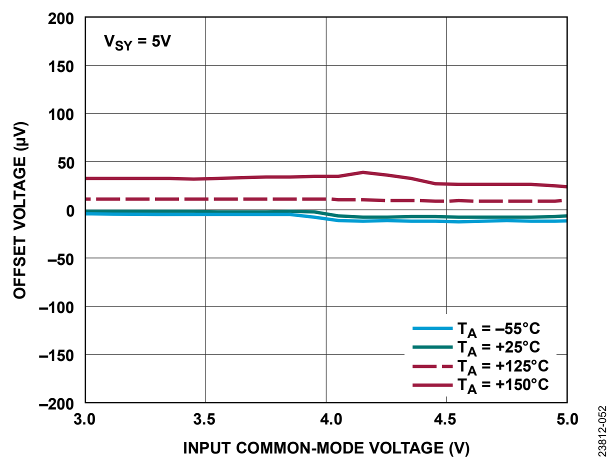


Figure 52 . Offset Voltage vs. Input Common-Mode Voltage over Temperature, V_{SY} = 5 V

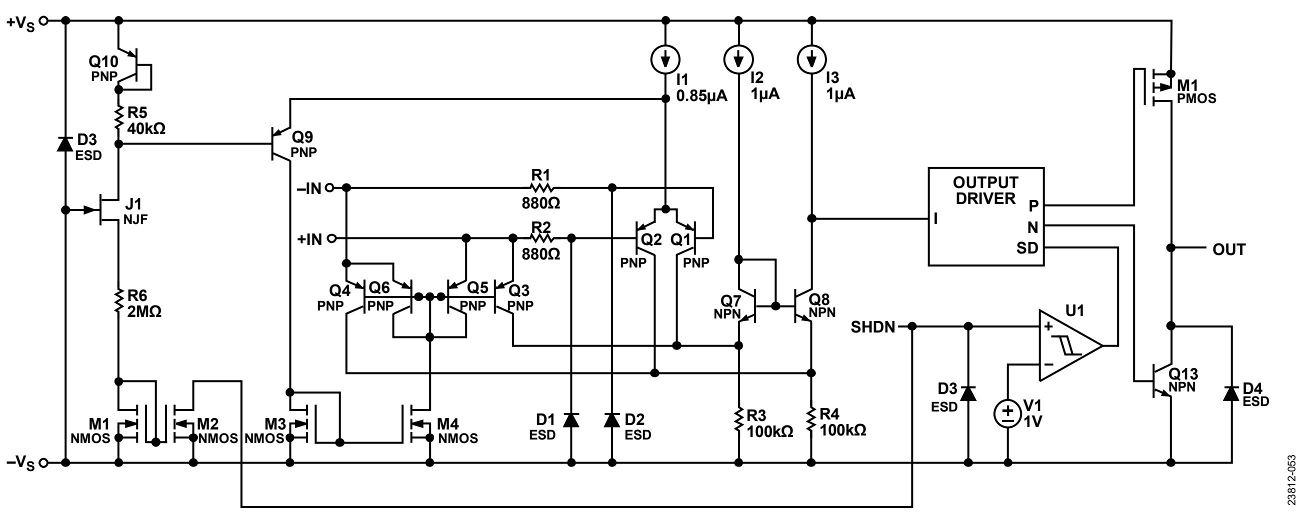


Figure 53. Simplified ADA4097-1 Schematic

INPUT PROTECTION

The inputs are protected against temporary voltage excursions to 15 V below $-V_S$ (see Figure 54) by internal 880 Ω resistors (see Figure 53). These resistors limit the current in the series D1 diode and D2 diode that are tied to the bases of the Q1 and Q2 transistors, respectively. Adding additional external series resistance extends the protection to >15 V below $-V_S$, at the cost of stability and added thermal noise. The input stage of the ADA4097-1 incorporates phase reversal protection to prevent the output from phase reversing for inputs below $-V_S$. The ADA4097-1 op amp does not have clamping diodes between the inputs and can be differentially overdriven up to 80 V without damage, inducing parametric shifts, or drawing appreciable input current. Figure 55 summarizes the input fault types that can be applied to the ADA4097-1 without compromising input integrity.

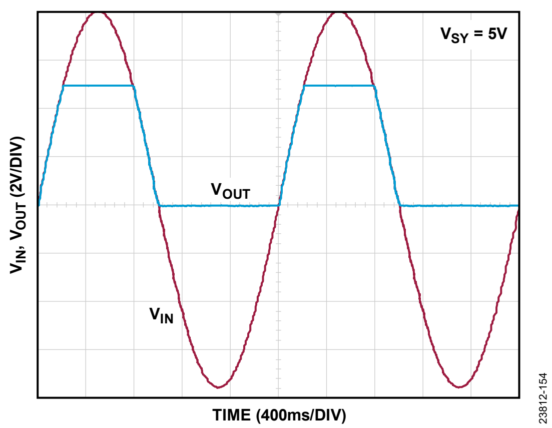


Figure 54. ADA4097-1 as Unity-Gain Buffer with Noninverting Input Driven Beyond the Supply (V_{SY} = 5 V)

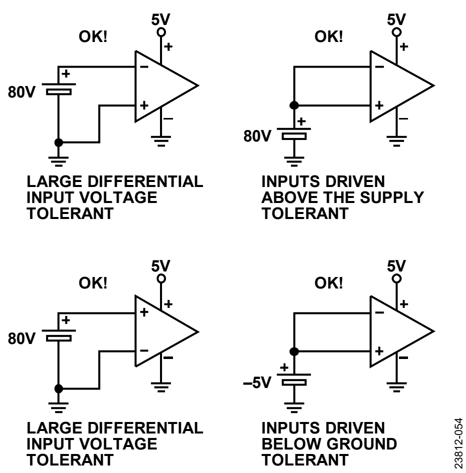


Figure 55. ADA4097-1 Fault Tolerant Conditions

OVER-THE-TOP OPERATION CONSIDERATIONS

When the ADA4097-1 input common-mode is biased near or >$+V_S$ supply, the amplifier operates in the Over-The-Top configuration. The differential input pair that controls amplifier operation is the common base pair, Q3 to Q6 (see Figure 53).

Input bias currents change from<±0.3 nA in normal operation to approximately 0.8 µA in Over-The-Top operation when the input stage transitions from common emitter to common base. The Over-The-Top input bias currents are well matched, and the associated offset is typically <50 nA. Ensure that the impedance connected to the inverting and noninverting inputs is well matched to avoid any input bias current induced voltage offsets.

Differential input impedance, R_{IN} (see Figure 56), decreases from >10 MΩ in normal operation to ~60 kΩ in Over-The-Top operation (see Table 1 and Table 2).

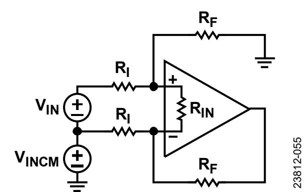


Figure 56. Difference Amplifier Configured for Normal Operation and Over-The-Top Operation (R_I Is a Gain Setting Resistor)

This R_{IN} resistance appears across the summing nodes in Over-The-Top operation due to the configuration of the common base input stage.

The R_{IN} value is derived from the specified I_B that flows to the op amp inputs, as expressed in the following equation:

$$R_{IN} = 2kT/(qI_B)$$

where:
k is Boltzmann's constant.
T is the operating temperature.
q is the charge of an electron.
I_B is the operating input bias current in Over-The-Top operation.

The inputs are biased proportional to absolute temperature. Therefore, R_{IN} is relatively constant with temperature. This resistance appears across the summing nodes of the amplifier, which is forced to 0 V differentially by the feedback action of the amplifier and can seem relatively harmless. However, depending on the configuration, this input resistance can boost the noise gain, lower overall amplifier loop gain and closed-loop bandwidth, and raise output noise. The singular benefit of this configuration is an increase in closed-loop amplifier stability.

In normal mode ($-V_S < V_{CM} < +V_S -1$ V), R_{IN} is typically large compared to the value of the gain setting resistors (R_F and R_I), and R_{IN} can be ignored.

In this case, the noise gain is defined by the following equation:

$$Noise\ Gain = 1 + R_F/R_I$$

When the amplifier transitions to Over-The-Top operation with the input common-mode biased near or above the $+V_S$ supply, consider the value of R_{IN}.

The noise gain of the amplifier increases as shown in the following equation:

$$Noise\ Gain_{OTT} = \left(\left(1 + \frac{R_F}{R_I \| R_{IN} + R_I \| R_F}\right) \times \left(1 + \frac{R_I \| R_F}{R_{IN}}\right)\right)$$

where $Noise\ Gain_{OTT}$ is the Over-The-Top noise gain.

The dc closed-loop gain remains mostly unaffected (R_F/R_I). However, the loop gain of the amplifier decreases, as expressed in the following equation:

$$\frac{A_{OL}}{1 + \frac{R_F}{R_I}} \text{ to } \frac{A_{OL}}{Noise\ Gain_{OTT}}$$

Likewise, the closed-loop bandwidth (BW_{CLOSED_LOOP}) of the amplifier changes going from normal operation to Over-The-Top operation.

In normal operation,

$$BW_{CLOSED\_LOOP} \approx \frac{GBP}{1 + \frac{R_F}{R_I}}$$

In Over-The-Top operation,

$$BW_{CLOSED\_LOOP} \approx \frac{GBP}{Noise\ Gain_{OTT}}$$

Output voltage noise density (e_{no}) is impacted when the device transitions from normal operation to Over-The-Top operation. Resistor noise is neglected in both modes of operation in the following equations.

In normal operation, neglecting resistor noise,

$$e_{no} \cong e_n \left(1 + \frac{R_F}{R_I}\right)$$

where e_n is input referred voltage noise density.

In Over-The-Top operation, neglecting resistor noise,

$$e_{no} \cong e_n \times Noise\ Gain_{OTT}$$

OUTPUT

The output of the ADA4097-1 can swing rail-to-rail to within 15 mV of the either supply with no load. The output can source 30 mA and sink 40 mA. The amplifier is internally compensated to drive at least 200 pF of C_{LOAD}. Adding a series resistance of 50 Ω between the output and larger capacitive loads extends the capacitive drive capability of the amplifier.

If the ADA4097-1 enters shutdown, the V_{OUT} pin appears as high impedance with two steering diodes connected to either supply. In this state, the output typically leaks <5 nA.

SHUTDOWN PIN (SHDN)

The ADA4097-1 has a dedicated SHDN pin to place the amplifier in a very low power shutdown state when asserted high. A logic high is defined by a voltage ≥1.5 V applied to the SHDN pin with respect to the $-V_S$ pin. In shutdown, the amplifier draws <20 µA of supply current (see Figure 7) and the V_{OUT} pin is placed in a high impedance state.

The SHDN pin can be driven beyond the $+V_S$ supply up to the absolute maximum voltage (60 V with respect to $-V_S$) and draws little current (<2.5 µA). For normal active amplifier operation, the SHDN pin can be floated or driven by an external voltage source low (within 0.5 V of $-V_S$). If the SHDN pin is left floating, an internal current source (~600 nA) pulls the SHDN pin to $-V_S$, which places the amplifier into a default, active amplifying state. Because of the close proximity of the −IN pin and SHDN pin, fast edges on the −IN pin may ac-couple to the adjacent high impedance SHDN pin, inadvertently placing the device in shutdown. If this scenario is a concern, add a 1 nF capacitor between the SHDN pin and the $-V_S$ pin.

Alternatively, the amplifier can be effectively placed in a low power state by removing $+V_S$. In this low power state, the inputs typically leak <1 nA with either ±IN pin biased between $-V_S$ and 70 V above $-V_S$. If the ±IN pins are taken below $-V_S$, they appear as a diode connected to the $-V_S$ supply in series with a resistance of 880 Ω. In this condition, limit the current to <10 mA.

Using an external source to drive the output beyond either $\pm V_S$ supply under shutdown conditions may produce unlimited current and may damage the device.

APPLICATIONS INFORMATION

LARGE RESISTOR GAIN OPERATION

The ADA4097-1 has approximately 3.5 pF of input capacitance.

The parallel combination of the R_F and R_G on the inverting input can combine with this input capacitance (C_{IN}) to form a pole that can reduce bandwidth, cause frequency response peaking, or produce oscillations (see Figure 58). To mitigate these consequences, place a feedback capacitor with a value of $C_F > C_{IN}(R_G/R_F)$ in parallel with R_F for summing node impedances >200 kΩ ($R_F||R_G$ > 200 kΩ). This capacitor placement cancels the input pole and optimizes dynamic performance (see Figure 57).

For applications where the noise gain is unity ($R_G \rightarrow \infty$), and the feedback resistor exceeds 200 kΩ, $C_F \geq C_{IN}$. Optimize PCB layouts to keep layout related summing node capacitance to an absolute minimum.

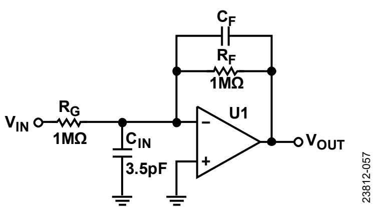


Figure 57. Inverting Gain Schematic

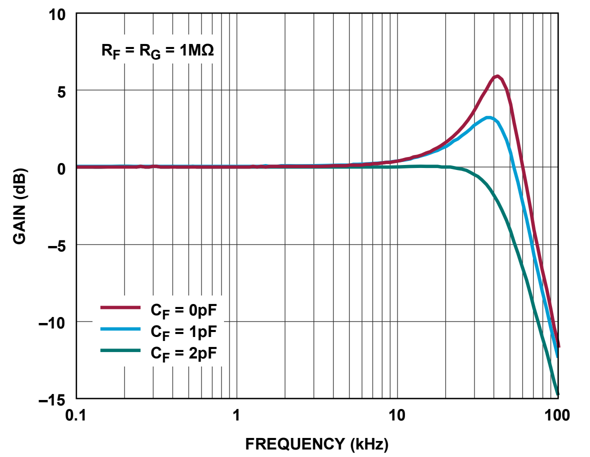


Figure 58. Inverting Gain of 1, Small Signal Frequency Response, $R_F = R_G = 1$ MΩ

RECOMMENDED VALUES FOR VARIOUS GAINS

Table 7 is a reference for determining various recommended gains and associated noise performance. The total impedance seen at the inverting input is kept to <200 kΩ for gains >1 to maintain ideal small signal bandwidth.

Table 7. Gains and Associated Recommended Resistor Values (T_A = 25°C)

Gain	R_F (kΩ)	R_G (kΩ)	C_F (pF)	Approximate −3 dB Frequency (kHz)	Total System Noise (nV/√Hz at 1 kHz), Referred to Input
+1	0	Not applicable	Not applicable	220	53
+2	10	10	0	80	54
+2	100	100	0	100	59.5
+5	10	40.2	0	33.5	53.2
+10	10	90	0	18	53.2
−1	10	10	0	87	108
−1	100	100	0	95	119
−1	1000	1000	2	55	215
−2	10	20	0	56	80
−5	10	49.9	0	29	64.2
−10	10	100	0	17	58.5

NOISE

To analyze the noise performance of an amplifier circuit, identify the noise sources, and then determine if each source has a significant contribution to the overall noise performance of the amplifier. To simplify the noise calculations, noise spectral densities (NSDs) are used rather than actual voltages, to leave bandwidth out of the expressions. NSD is generally expressed in nV/√Hz and is equivalent to the noise in a 1 Hz bandwidth.

The noise model shown in Figure 59 has six individual noise sources: the Johnson noise of the three resistors (R1 to R3), the op amp voltage noise, and the current noise ($I_{N\pm}$) in each input of the amplifier. Each noise source has its own contribution to the noise at the output. Noise is generally specified as referring to input (RTI), but it is often simpler to calculate the noise referred to the output (RTO), and then divide by the noise gain to obtain the RTI noise.

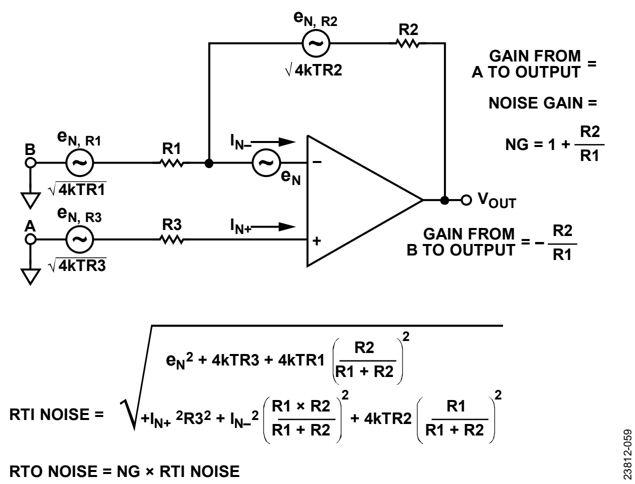


Figure 59. Op Amp Noise Analysis Model

Assuming $I_{N+} = I_{N-} = I_N$, the equation for RTI noise can be simplified to the following form:

$$RTI\ Noise = \sqrt{e_n^2 + e_{n,R}^2 + (I_N R_{EQ})^2}$$

$$e_{n,R} = \sqrt{4kTR_{EQ}}$$

$$R_{EQ} = R3 + R1||R2$$

where:
e_n is the op amp voltage noise.
$e_{n,R}$ is the thermal noise contribution of the surrounding R1 to R3 resistors.
R_{EQ} is the equivalent input resistance.
k is Boltzmann's constant (1.38×10^{-23} J/K).
T is the absolute temperature in Kelvin.

A 50 Ω resistor generates a Johnson noise of 1 nV/√Hz at 25°C.

For optimal performance, the lower bound of resistance in a feedback network is determined by the amount of quiescent power and distortion that can be tolerated. The upper bound is determined by the resistor and current noise density. The ADA4097-1 has an e_n of 53 nV/√Hz.

If resistor and current noise contributions are less than half this value, the e_n introduced by the op amp dominates and provides optimal noise performance of the device.

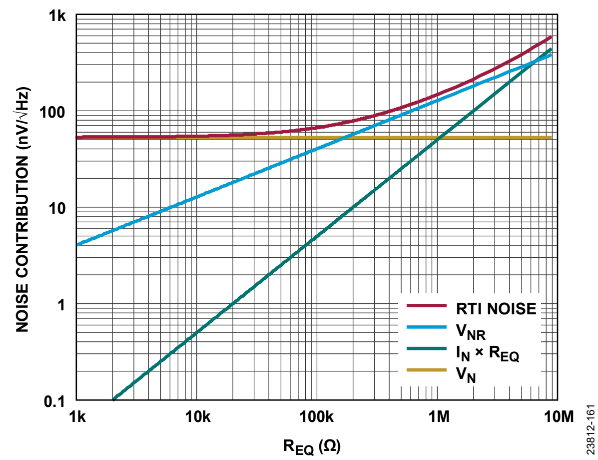


Figure 60. Noise Contributions vs. Equivalent Input Resistance

For the ADA4097-1, this lower bound of resistance in the feedback network is about 40 kΩ. For the amplifier configuration shown in Figure 59, R_{EQ} < 40 kΩ provides stable noise performance. If noise performance is not important, e_n is typically fixed for a given T_A, $e_{n,R}$ increases with the square root of the resistor value, and the $I_N \times R_{EQ}$ resistance increases linearly, but does not impact total noise until it approaches the value of $e_{n,R}$. With R_{EQ} < ~6 MΩ, $e_{n,R}$ is larger than $I_N \times R_{EQ}$. A safe value for R_{EQ} < 2 MΩ to ensure that I_N is not the majority contributor to total noise seen by the input.

Figure 60 shows the noise contributions for the range of resistance values discussed in this section.

DISTORTION

There are two main contributors of distortion in op amps: output crossover distortion as the output transitions from sourcing to sinking, and distortion caused by nonlinear common-mode rejection. If the op amp is operating in an inverting configuration, there is no common-mode induced distortion. If the op amp is operating in the noninverting configurations within the normal input common-mode range ($-V_S$ to $+V_S$ − 1 V), distortion is acceptable. When the inputs transition from normal to Over-The-Top operation or vice versa, a significant degradation occurs in linearity due to the change of input circuitry.

As R_L decreases, distortion increases due to a net decrease in loop gain and greater signal swings internal to the amplifier that are necessary to drive the load. The lowest distortion can be achieved with the ADA4097-1 operating in Class A operation in an inverting configuration, with the input common-mode biased at midsupply.

POWER DISSIPATION AND THERMAL SHUTDOWN

The ADA4097-1 can drive heavy loads on power supplies up to ±25 V. Therefore, ensure that T_J on the integrated circuit does not exceed 175°C. The ADA4097-1 is housed in a 6-lead TSOT package (θ_{JA} = 192°C/W).

Junction temperatures exceeding 125°C promote accelerated aging. Reliability of the ADA4097-1 may be impaired if the junction temperature exceeds 175°C. If the junction temperature exceeds 175°C, the ADA4097-1 has a final safety measure in the form of a thermal shutdown that shuts off the output stage and reduces the internal device currents. When this thermal shutdown function triggers, the output remains disabled in a high impedance state until the junction temperature drops 20°C. Persistent heavy loads and elevated ambient temperatures can cause the ADA4097-1 to oscillate in and out of thermal shutdown depending on the power dissipated on the die, until the heavy load is removed (see Figure 61).

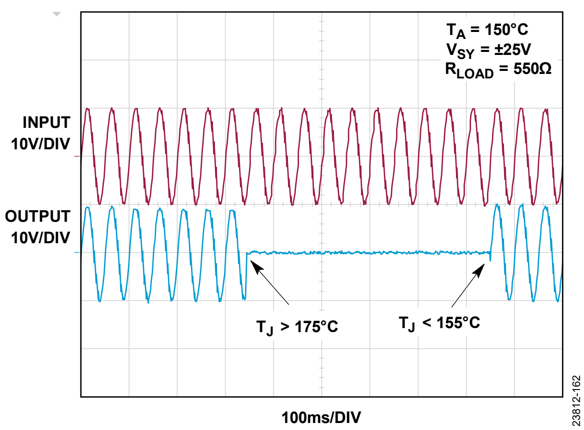


Figure 61. ADA4097-1 Cycling In and Out of Thermal Shutdown

It is not recommended to operate near the maximum junction temperature.

Typically, T_J can be estimated from T_A and the device power dissipation ($P_D \times \theta_{JA}$), as shown in the following equation:

$$T_J = T_A + P_D \times \theta_{JA}$$

The power dissipation in the IC varies as a function of supply voltage, the output voltage, and load resistance. For a given supply voltage, the worst case power dissipation ($P_{D(MAX)}$) in the IC occurs when the supply current is maximum, and the output voltage is at half of either supply voltage.

$$P_{D(MAX)} = V_s I_{s(MAX)} + \frac{\left(\frac{V_{SY}}{2}\right)^2}{R_L}$$

For a given supply voltage, use Figure 62 as a guide for estimating the minimum load resistance that the ADA4097-1 can drive for a given supply voltage and a given rise in junction temperature (ΔT_J). For example, to limit ΔT_J to 50°C, the load driven on the ±15 V supplies (+30 V total supply) must not be lower than 0.8 kΩ. It is assumed that θ_{JA} is 192°C/W.

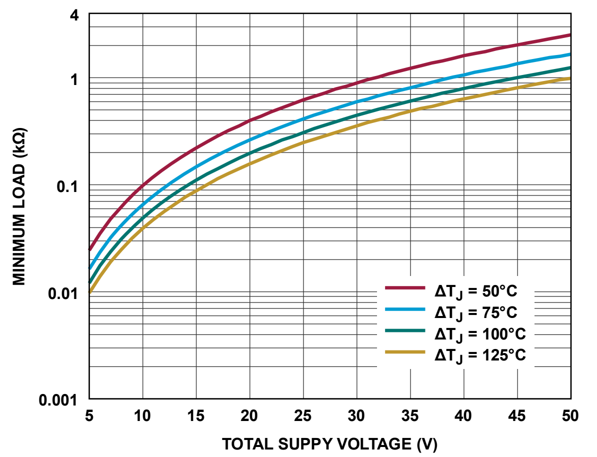


Figure 62. Minimum Load Resistance for Given ΔT_J and V_{SY}

CIRCUIT LAYOUT CONSIDERATIONS

Careful and deliberate attention to detail when laying out the ADA4097-1 boards yields optimal performance. Power supply bypassing, parasitic capacitance, and component selection all contribute to the overall performance of the amplifier.

POWER SUPPLY BYPASSING

On single supplies, solder the $-V_S$ supply pin directly to a low impedance ground plane. Bypass the $+V_S$ pin to a low impedance ground plane with a low effective series resistance (ESR) multilayer ceramic capacitor (MLCC) of 0.1 µF, typically, as close to the $\pm V_S$ supply pins as possible. When driving heavy loads, add 10 µF of supply capacitance. When using split supplies, these conditions are applicable to the $-V_S$ supply pin.

The ADA4097-1 has an internal current source of ~0.6 µA on the SHDN pin to pull the pin down to $-V_S$ and to place the amplifier in the default amplifying state. If the SHDN state is not required, hard tie the SHDN pin to the $-V_S$ pin. If the SHDN pin is left floating or driven by a source with significant source impedance (>100 Ω), bypass the $-V_S$ supply pin with a small, 1 nF capacitor to prevent stray signals from coupling on the SHDN pin, which can inadvertently trigger shutdown.

GROUNDING

Use ground and power planes where possible to reduce the resistance and inductance of the supply and ground returns. Place bypass capacitors as close as possible to the $\pm V_S$ supply pins, with the other ends connected to the ground plane. It is recommended to use a bypass capacitor of at least 0.1 µF when driving light loads (load currents < 100 µA), and more capacitance when driving heavier loads. Routing from the output to the load and return to the ground plane must have minimal loop area to keep inductance to a minimum.

ESD PROTECTION WHEN POWERED

ICs react to ESD strikes differently when unpowered vs. powered, which falls under IEC-61000-4-2 standards (see the Absolute Maximum Ratings section). A device that performs well under HBM conditions can perform poorly under International Electrotechnical Commission (IEC) conditions. The ADA4097-1 is thoroughly abused with ESD strikes under IEC conditions to create a front-end circuit protection scheme that protects the device if subjected to ESD strikes. Figure 63 and Figure 64 show two different protection schemes that extend the protection of the ADA4097-1 to ±8 kV ESD strikes.

Consider the following when selecting components:

- A component size of 0805 or larger to reduce chance of arc-over.
- Pulse withstanding, thick film resistors.
- C0G MLCC with a minimum rating of 100 V.
- Bidirectional, transient voltage suppression (TVS) diodes.

In the circuit shown in Figure 63, R1 is a 220 Ω, Panasonic, 0805, ERJ-P6 series, and C1 is a 100 pF, Yageo, 0805, 100 V, C0G/NPO.

ADVANTAGES	DISADVANTAGES
INEXPENSIVE (~5 CENTS)	R1 INTRODUCES THERMAL NOISE
SMALL FOOTPRINT	RC NETWORK LIMITS SPEED
MINIMAL LEAKAGE	NEED TO CAREFULLY CHARACTERIZE CAPACITOR
	NOT AS ROBUST AGAINST REPEATED STRIKES

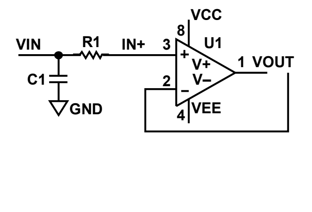


Figure 63. ESD Protection Circuit (RC Network)

In the circuit shown in Figure 64, R1 is a 220 Ω, Panasonic, 0805, ERJ-P6 series, and D1 is a Bourns CDSOD323-T36SC. An ESD varistor can be considered for D1.

For more information on system level ESD considerations, see the technical article, *When Good Electrons Go Bad: How to Protect Your Analog Front End*, on the Analog Devices, Inc., website.

RELATED PRODUCTS

Table 8 describes several alternative precision amplifiers that can also be considered for certain applications.

ADVANTAGES	DISADVANTAGES
INEXPENSIVE (20 TO 30 CENTS)	R1 INTRODUCES NOISE
SMALL FOOTPRINT	D1 HAS LEAKAGE CURRENT
VERY ROBUST	D1 HAS CAPACITANCE (5pF TO 300pF)

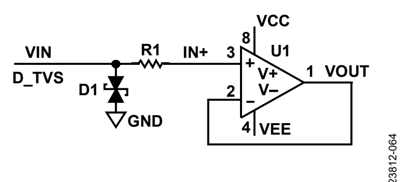


Figure 64. ESD Protection Circuit (R-TVS Network)

Table 8. ADA4097-1 Related Products

Model	V_{OS} (µV)	I_B (nA)	GBP (kHz)	e_n (nV/√Hz)	I_{SY} (µA)	Common-Mode Input Range (V)
ADA4097-1	60	0.3	130	53	33	$-V_S$ to $-V_S + 70$
ADA4098-1	30	0.7	1000	17	165	$-V_S$ to $-V_S + 70$
ADA4099-1	30	10	8000	7	1500	$-V_S$ to $-V_S + 70$
ADA4077-1	35	1	3900	7	500	$-V_S$ to $+V_S$
LT6015	50	5	3200	18	335	$-V_S$ to $-V_S + 76$
LT6014	60	0.4	1600	9.5	165	$-V_S$ to $+V_S$
LT1494	375	1	2.7	185	1.5	$-V_S$ to $-V_S + 36$
LT1490A	500	8	180	50	55	$-V_S$ to $-V_S + 44$

TYPICAL APPLICATIONS

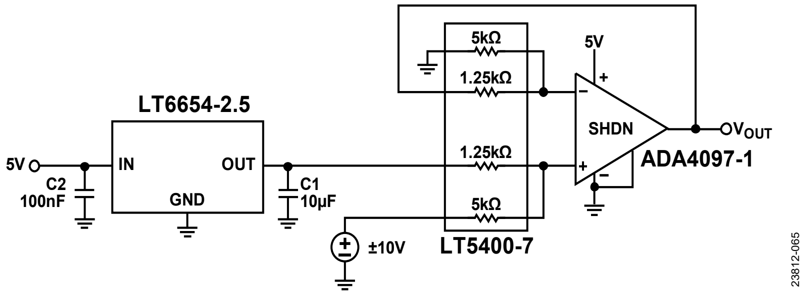


Figure 65. ±10 V to 0 V to +5 V Funnel Amplifier, High CMRR and ±80 V Input Protection via LT5400-7 Resistor Network

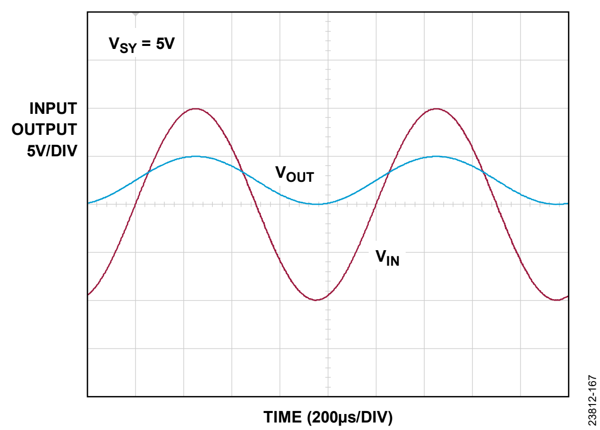


Figure 66. ±10 V to 0 V to +5 V Funnel Amplifier, Input and Output Voltages

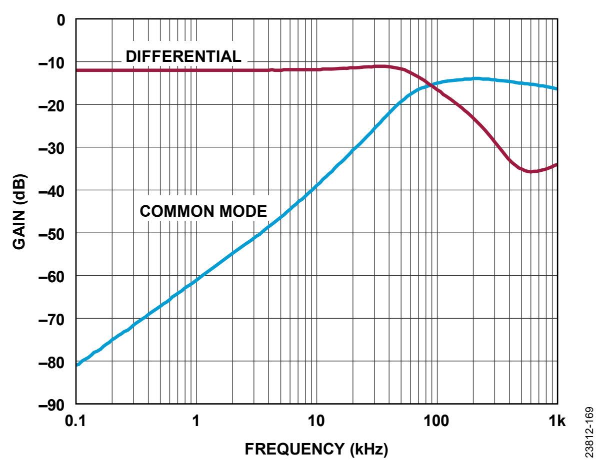


Figure 67. ±10 V to 0 V to +5 V Funnel Amplifier, System Gain

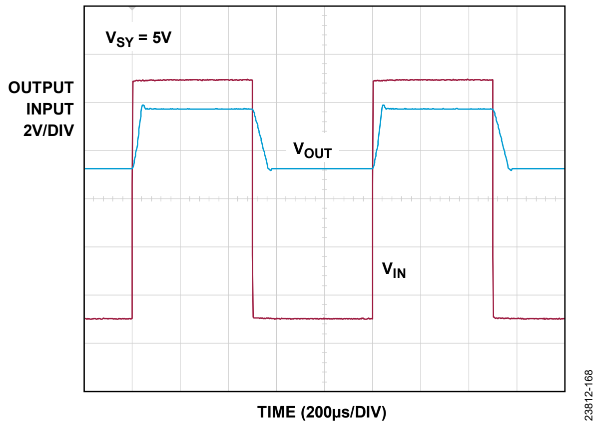


Figure 68. ±10 V to 0 V to +5 V Funnel Amplifier, Large Signal Pulse Response

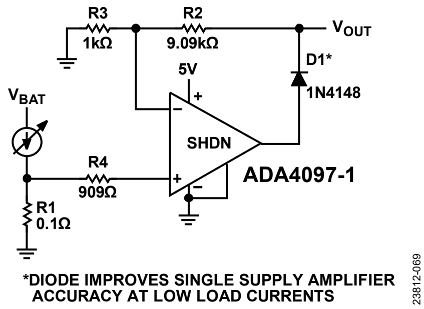


Figure 69. 1 V/A Low-Side Current Sense

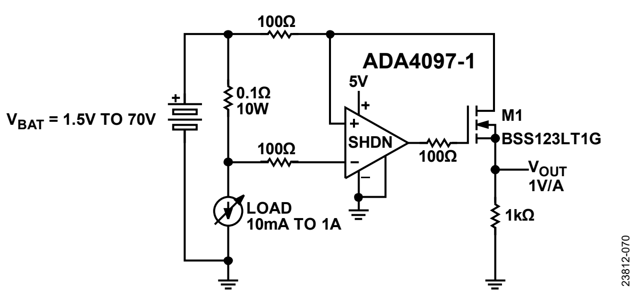


Figure 70. 1 V/A High-Side Current Sense

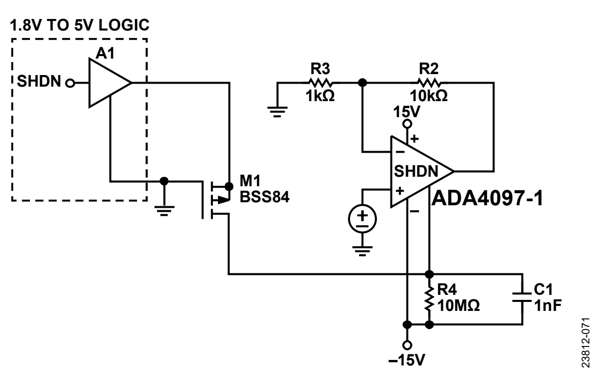


Figure 71. Microprocessor Control of SHDN Pin in Split Supply Applications

OUTLINE DIMENSIONS

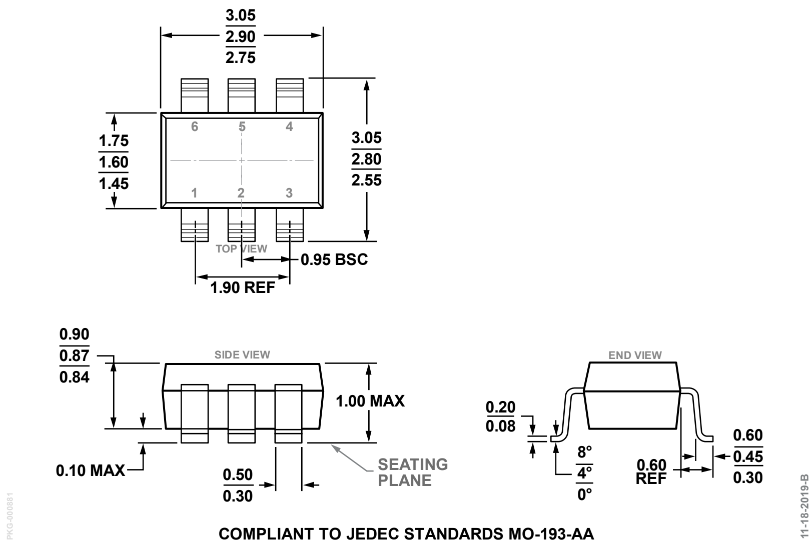


Figure 72. 6-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Marking Code
ADA4097-1BUJZ-R5	−40°C to +125°C	6-Lead TSOT	UJ-6	Y7K
ADA4097-1BUJZ-RL7	−40°C to +125°C	6-Lead TSOT	UJ-6	Y7K
ADA4097-1HUJZ-RL7	−55°C to +150°C	6-Lead TSOT	UJ-6	Y7L
EVAL-ADA4097-1HUJZ		Evaluation Board		

[1] Z = RoHS Compliant Part.