ANALOG DEVICES

Precision, Ultralow Noise, RRIO, Zero-Drift Op Amp

Data Sheet

ADA4528-1/ADA4528-2

FEATURES

Low offset voltage: 2.5 μV maximum
Low offset voltage drift: 0.015 μV/°C maximum
Low noise
- **5.6 nV/√Hz at f = 1 kHz, A_V = +100**
- **97 nV p-p at f = 0.1 Hz to 10 Hz, A_V = +100**

Open-loop gain: 130 dB minimum
CMRR: 135 dB minimum
PSRR: 130 dB minimum
Unity-gain crossover: 4 MHz
Gain bandwidth product: 3 MHz at A_V = +100
−3 dB closed-loop bandwidth: 6.2 MHz
Single-supply operation: 2.2 V to 5.5 V
Dual-supply operation: ±1.1 V to ±2.75 V
Rail-to-rail input and output
Unity-gain stable

APPLICATIONS

Thermocouple/thermopile
Load cell and bridge transducers
Precision instrumentation
Electronic scales
Medical instrumentation
Handheld test equipment

GENERAL DESCRIPTION

The ADA4528-1/ADA4528-2 are ultralow noise, zero-drift operational amplifiers featuring rail-to-rail input and output swing. With an offset voltage of 2.5 μV, offset voltage drift of 0.015 μV/°C, and typical noise of 97 nV p-p (0.1 Hz to 10 Hz, A_V = +100), the ADA4528-1/ADA4528-2 are well suited for applications in which error sources cannot be tolerated.

The ADA4528-1/ADA4528-2 have a wide operating supply range of 2.2 V to 5.5 V, high gain, and excellent CMRR and PSRR specifications, which make it ideal for applications that require precision amplification of low level signals, such as position and pressure sensors, strain gages, and medical instrumentation.

The ADA4528-1/ADA4528-2 are specified over the extended industrial temperature range (−40°C to +125°C). The ADA4528-1 and ADA4528-2 are available in 8-lead MSOP and 8-lead LFCSP packages.

For more information about the ADA4528-1/ADA4528-2, see the AN-1114 Application Note, *Lowest Noise Zero-Drift Amplifier Has 5.6 nV/√Hz Voltage Noise Density*.

PIN CONNECTION DIAGRAMS

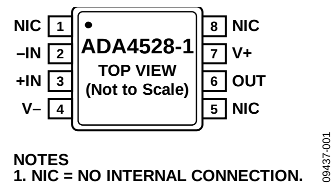

Figure 1. ADA4528-1 Pin Configuration, 8-Lead MSOP

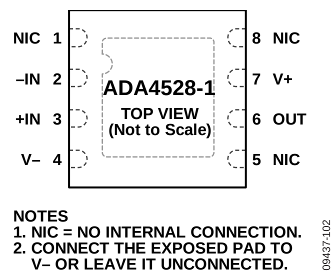

Figure 2. ADA4528-1 Pin Configuration, 8-Lead LFCSP

For ADA4528-2 pin connections and for more information about the pin connections for these products, see the Pin Configurations and Function Descriptions section.

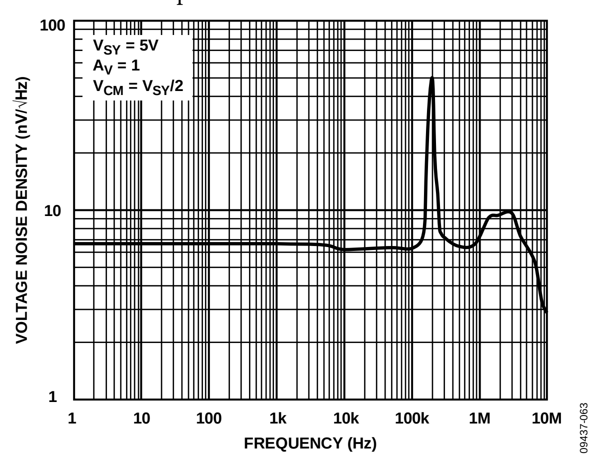

Figure 3. Voltage Noise Density vs. Frequency

Table 1. Analog Devices, Inc., Zero-Drift Op Amp Portfolio[1]

Type	Ultralow Noise	Micropower (<20 μA)	Low Power (<1 mA)	16 V Operating Voltage	30 V Operating Voltage
Single	ADA4528-1	ADA4051-1	AD8628	AD8638	ADA4638-1
			AD8538		
Dual	ADA4528-2	ADA4051-2	AD8629	AD8639	
			AD8539		
Quad			AD8630		

[1] See www.analog.com for the latest selection of zero-drift operational amplifiers.

Rev. F Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

8/2017—Rev. E to Rev. F

Deleted CP-8-19 ... Universal
Updated Outline Dimensions ... 24
Changes to Ordering Guide ... 25

6/2017—Rev. D to Rev. E

Deleted CP-8-12 ... Universal
Added CP-8-19 ... Universal
Updated Outline Dimensions ... 24
Changes to Ordering Guide ... 25

5/2013—Rev. C to Rev. D

Added 8-Lead LFCSP Package (CP-8-11) ... Universal
Changes to Table 5 ... 7
Added Figure 7, Renumbered Sequentially ... 8
Added Figure 62 and Figure 63 ... 19
Changes to Comparator Operation Section, Figure 68, Figure 69, Figure 70, and Figure 71 ... 21
Changes to Figure 72 ... 22
Added Figure 76 ... 24

9/2012—Rev. B to Rev. C

Changes to Features Section ... 1
Added Comparator Operation Section ... 21
Added Figure 65 to Figure 69; Renumbered Sequentially ... 21

7/2012—Rev. A to Rev. B

Added ADA4528-2 ... Universal
Changes to Features Section, Figure 1, Figure 2, and Table 1 ... 1
Added Pin Connection Diagrams Section and Figure 3; Renumbered Sequentially ... 1
Changes to Table 2 ... 3
Changes to Table 3 ... 5
Change to Endnote 1 of Table 4 and Thermal Resistance Section ... 7
Added Pin Configurations and Function Descriptions Section, Figure 4, Figure 5, and Table 6 ... 8
Added Figure 6 and Table 7 ... 9
Changes to Input Protection Section ... 19
Changes to Source Resistance Section and Caption of Figure 63 ... 20
Changes to Residual Voltage Ripple Section and Caption of Figure 64 ... 21
Changes to Ordering Guide ... 22

9/2011—Rev. 0 to Rev. A

Added 8-Lead LFCSP_WD Package ... Universal
Changes to General Description Section ... 1
Added Figure 2; Renumbered Sequentially ... 1
Changes to Offset Voltage, Offset Voltage Drift, Power Supply Rejection Ratio, and Settling Time to 0.1% Parameters, Table 2 ... 3
Changes to Thermal Resistance Section and Table 5 ... 5
Changes to Figure 41 and Figure 44 ... 12
Changes to Figure 45 and Figure 48 ... 13
Updated Outline Dimensions ... 18
Changes to Ordering Guide ... 18

1/2011—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—2.5 V OPERATION

V_{SY} = 2.5 V, V_{CM} = V_{SY}/2, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 0 V to 2.5 V		0.3	2.5	µV
		−40°C ≤ T_A ≤ +125°C, MSOP package			4	µV
		−40°C ≤ T_A ≤ +125°C, LFCSP package			4.3	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C, MSOP package		0.002	0.015	µV/°C
		−40°C ≤ T_A ≤ +125°C, LFCSP package			0.018	µV/°C
Input Bias Current	I_B			220	400	pA
		−40°C ≤ T_A ≤ +125°C			600	pA
Input Offset Current	I_{OS}			440	800	pA
		−40°C ≤ T_A ≤ +125°C			1	nA
Input Voltage Range			0		2.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.5 V	135	158		dB
		−40°C ≤ T_A ≤ +125°C	116			dB
Open-Loop Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.1 V to 2.4 V	130	140		dB
		−40°C ≤ T_A ≤ +125°C	126			dB
ADA4528-1		R_L = 2 kΩ, V_O = 0.1 V to 2.4 V	125	132		dB
		−40°C ≤ T_A ≤ +125°C	121			dB
ADA4528-2		R_L = 2 kΩ, V_O = 0.1 V to 2.4 V	122	132		dB
		−40°C ≤ T_A ≤ +125°C	119			dB
Input Resistance						
Differential Mode	R_{INDM}			225		kΩ
Common Mode	R_{INCM}			1		GΩ
Input Capacitance						
Differential Mode	C_{INDM}			15		pF
Common Mode	C_{INCM}			30		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	2.49	2.495		V
		−40°C ≤ T_A ≤ +125°C	2.485			V
		R_L = 2 kΩ to V_{CM}	2.46	2.48		V
		−40°C ≤ T_A ≤ +125°C	2.44			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		5	10	mV
		−40°C ≤ T_A ≤ +125°C			15	mV
		R_L = 2 kΩ to V_{CM}		20	40	mV
		−40°C ≤ T_A ≤ +125°C			60	mV
Short-Circuit Current	I_{SC}			±30		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +10		0.1		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.2 V to 5.5 V	130	150		dB
		−40°C ≤ T_A ≤ +125°C	127			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		1.4	1.7	mA
		−40°C ≤ T_A ≤ +125°C			2.1	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 100 pF, A_V = +1		0.45		V/µs
Settling Time to 0.1%	t_S	V_{IN} = 1.5 V step, R_L = 10 kΩ, C_L = 100 pF, A_V = −1		7		µs
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +1		4		MHz
Phase Margin	Φ_M	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +1		57		Degrees
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +100		3		MHz

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
−3 dB Closed-Loop Bandwidth	f_{-3dB}	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +1		6.2		MHz
Overload Recovery Time		R_L = 10 kΩ, C_L = 100 pF, A_V = −10		50		μs
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz, A_V = +100		97		nV p-p
Voltage Noise Density	e_n	f = 1 kHz, A_V = +100		5.6		nV/√Hz
		f = 1 kHz, A_V = +100, V_{CM} = 2.0 V		5.5		nV/√Hz
Current Noise	i_n p-p	f = 0.1 Hz to 10 Hz, A_V = +100		10		pA p-p
Current Noise Density	i_n	f = 1 kHz, A_V = +100		0.7		pA/√Hz

ELECTRICAL CHARACTERISTICS—5 V OPERATION

V_{SY} = 5 V, V_{CM} = $V_{SY}/2$, T_A = 25°C, unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 0 V to 5 V		0.3	2.5	μV
		−40°C ≤ T_A ≤ +125°C			4	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.002	0.015	μV/°C
Input Bias Current	I_B					
ADA4528-1				90	200	pA
		−40°C ≤ T_A ≤ +125°C			300	pA
ADA4528-2				125	250	pA
		−40°C ≤ T_A ≤ +125°C			350	pA
Input Offset Current	I_{OS}					
ADA4528-1				180	400	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
ADA4528-2				250	500	pA
		−40°C ≤ T_A ≤ +125°C			600	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	137	160		dB
		−40°C ≤ T_A ≤ +125°C	122			dB
Open-Loop Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.1 V to 4.9 V	127	139		dB
		−40°C ≤ T_A ≤ +125°C	125			dB
		R_L = 2 kΩ, V_O = 0.1 V to 4.9 V	121	131		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Input Resistance						
Differential Mode	R_{INDM}			190		kΩ
Common Mode	R_{INCM}			1		GΩ
Input Capacitance						
Differential Mode	C_{INDM}			16.5		pF
Common Mode	C_{INCM}			33		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	4.99	4.995		V
		−40°C ≤ T_A ≤ +125°C	4.98			V
		R_L = 2 kΩ to V_{CM}	4.96	4.98		V
		−40°C ≤ T_A ≤ +125°C	4.94			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		5	10	mV
		−40°C ≤ T_A ≤ +125°C			20	mV
		R_L = 2 kΩ to V_{CM}		20	40	mV
		−40°C ≤ T_A ≤ +125°C			60	mV
Short-Circuit Current	I_{SC}			±40		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +10		0.1		Ω

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.2 V to 5.5 V	130	150		dB
		−40°C ≤ T_A ≤ +125°C	127			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		1.5	1.8	mA
		−40°C ≤ T_A ≤ +125°C			2.2	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 100 pF, A_V = +1		0.5		V/μs
Settling Time to 0.1%	t_S	V_{IN} = 4 V step, R_L = 10 kΩ, C_L = 100 pF, A_V = −1		10		μs
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +1		4		MHz
Phase Margin	$Φ_M$	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +1		57		Degrees
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +100		3.4		MHz
−3 dB Closed-Loop Bandwidth	f_{-3dB}	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 100 pF, A_V = +1		6.5		MHz
Overload Recovery Time		R_L = 10 kΩ, C_L = 100 pF, A_V = −10		50		μs
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz, A_V = +100		99		nV p-p
Voltage Noise Density	e_n	f = 1 kHz, A_V = +100		5.9		nV/√Hz
		f = 1 kHz, A_V = +100, V_{CM} = 4.5 V		5.3		nV/√Hz
Current Noise	i_n p-p	f = 0.1 Hz to 10 Hz, A_V = +100		10		pA p-p
Current Noise Density	i_n	f = 1 kHz, A_V = +100		0.5		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	$\pm V_{SY} \pm 0.3$ V
Input Current[1]	±10 mA
Differential Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] The input pins have clamp diodes to the power supply pins. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages using a 4-layer JEDEC board. The exposed pad of the LFCSP package is soldered to the board.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP (RM-8)	142	45	°C/W
8-Lead LFCSP (CP-8-11)	83.5	48.5[1]	°C/W

[1] θ_{JC} is measured on the top surface of the package.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

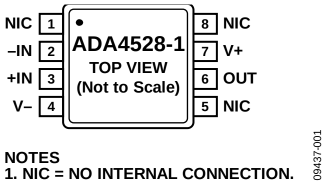

Figure 4. ADA4528-1 Pin Configuration, 8-Lead MSOP

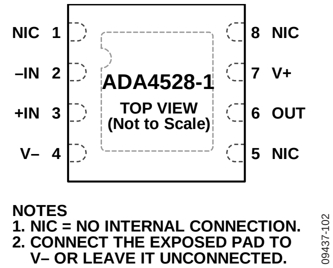

Figure 5. ADA4528-1 Pin Configuration, 8-Lead LFCSP

Table 6. ADA4528-1 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5, 8	NIC	No Internal Connection.
2	−IN	Inverting Input.
3	+IN	Noninverting Input.
4	V−	Negative Supply Voltage.
6	OUT	Output.
7	V+	Positive Supply Voltage.
	EPAD	Exposed Pad (LFCSP Only). Connect the exposed pad to V− or leave it unconnected.

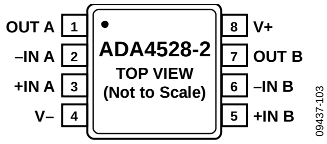

Figure 6. ADA4528-2 Pin Configuration, 8-Lead MSOP

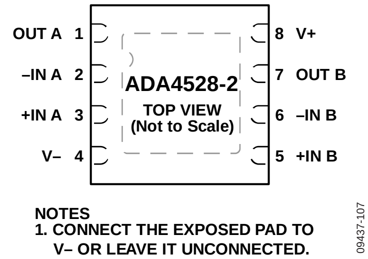

Figure 7. ADA4528-2 Pin Configuration, 8-Lead LFCSP

Table 7. ADA4528-2 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A.
2	−IN A	Inverting Input, Channel A.
3	+IN A	Noninverting Input, Channel A.
4	V−	Negative Supply Voltage.
5	+IN B	Noninverting Input, Channel B.
6	−IN B	Inverting Input, Channel B.
7	OUT B	Output, Channel B.
8	V+	Positive Supply Voltage.
	EPAD	Connect the exposed pad to V- or leave it unconnected.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

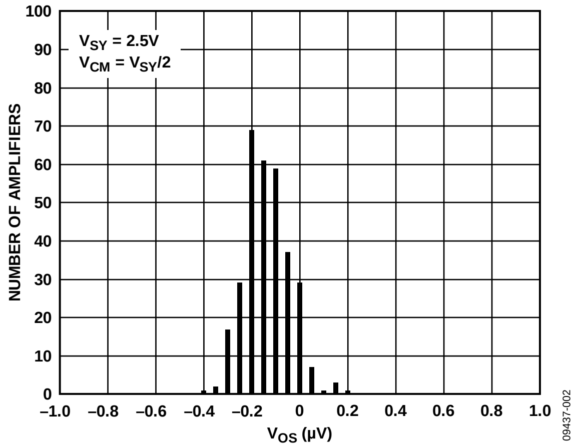

Figure 8. Input Offset Voltage Distribution

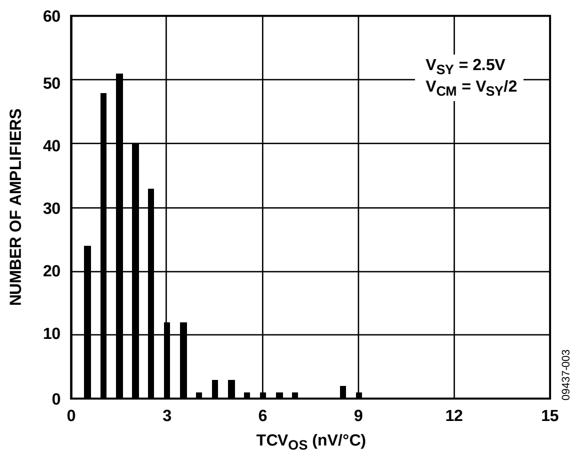

Figure 9. Input Offset Voltage Drift Distribution

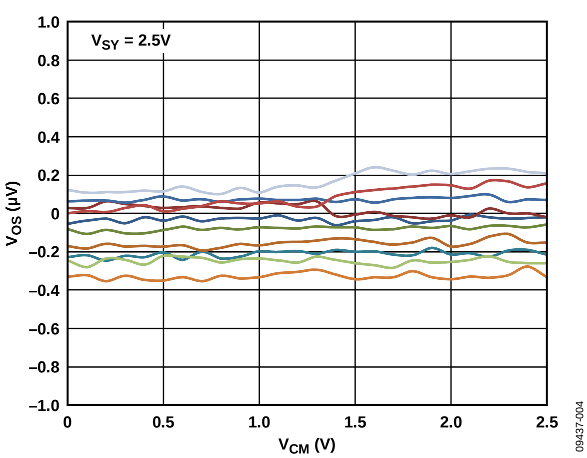

Figure 10. Input Offset Voltage vs. Common-Mode Voltage

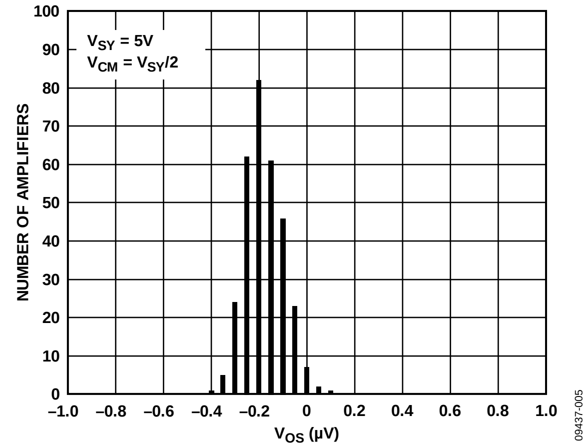

Figure 11. Input Offset Voltage Distribution

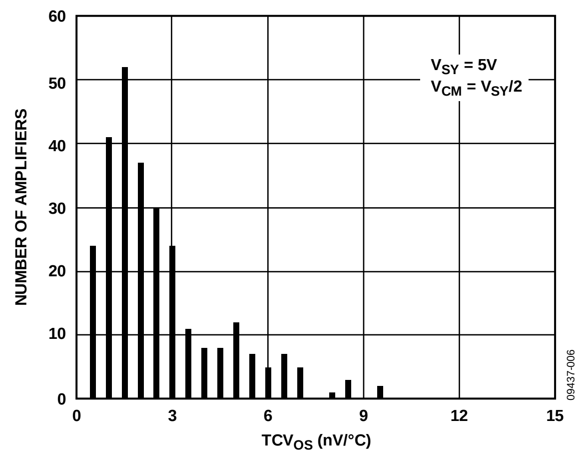

Figure 12. Input Offset Voltage Drift Distribution

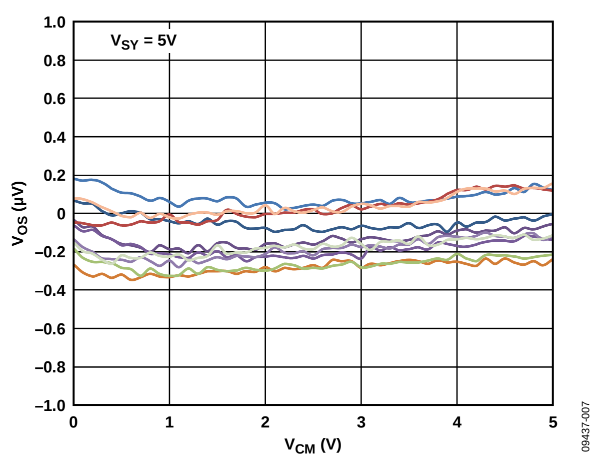

Figure 13. Input Offset Voltage vs. Common-Mode Voltage

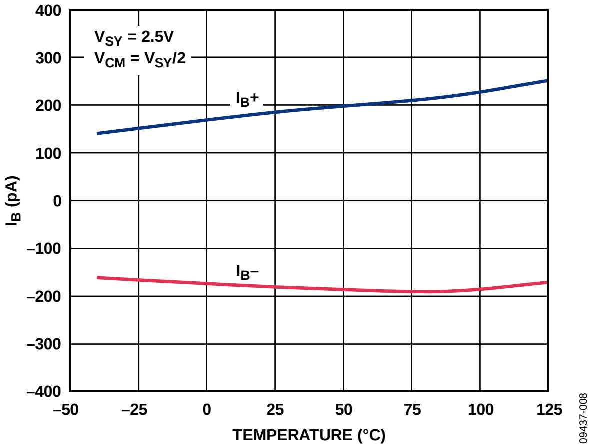

Figure 14. Input Bias Current vs. Temperature

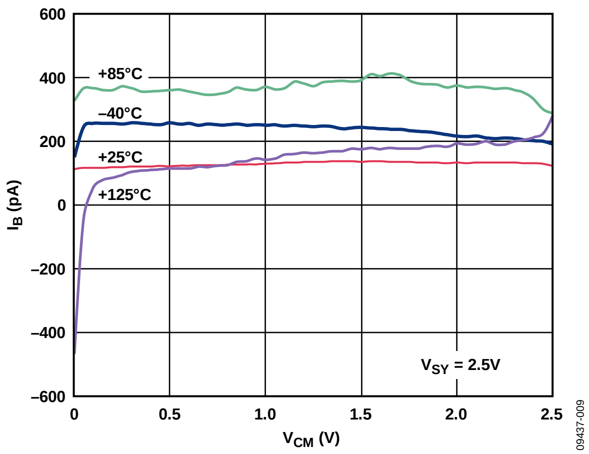

Figure 15. Input Bias Current vs. Common-Mode Voltage

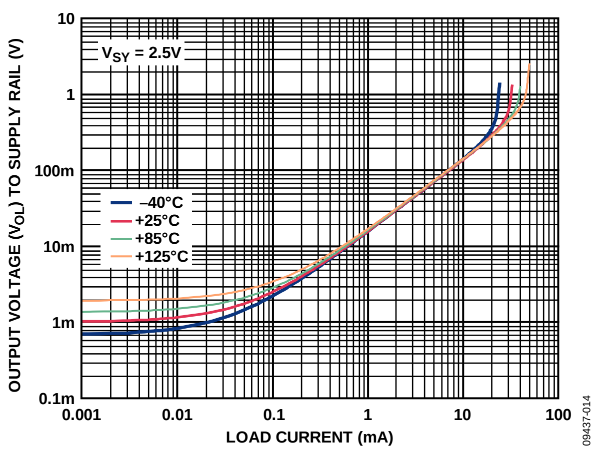

Figure 16. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

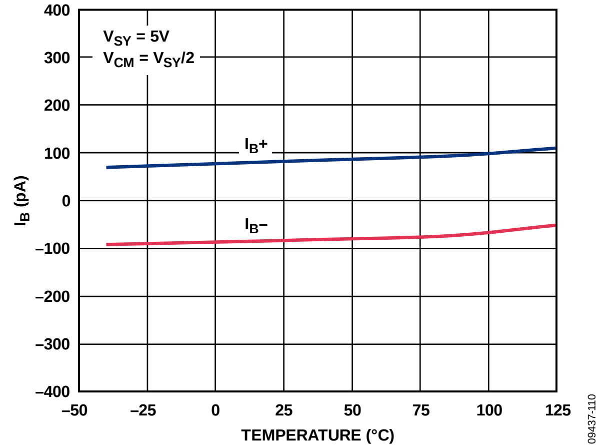

Figure 17. Input Bias Current vs. Temperature

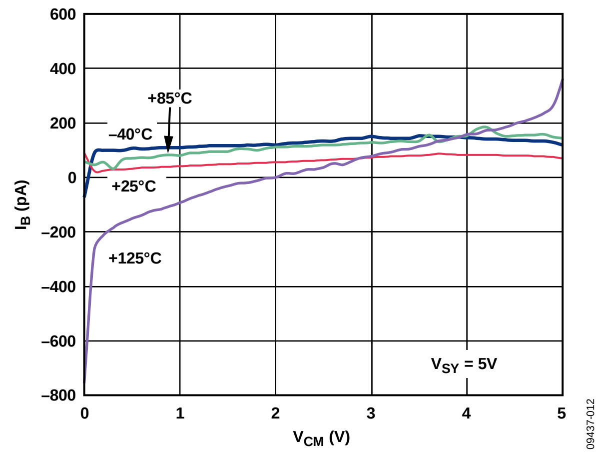

Figure 18. Input Bias Current vs. Common-Mode Voltage

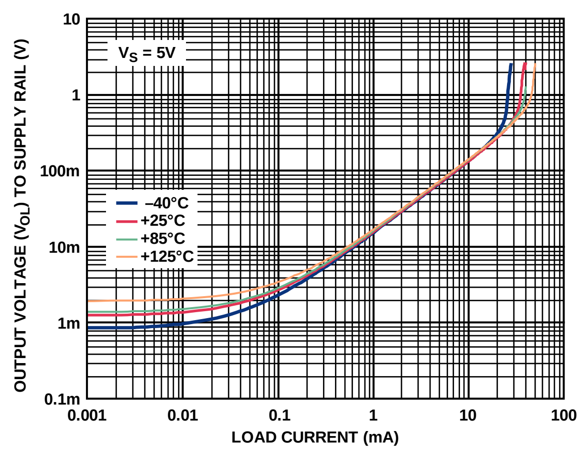

Figure 19. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

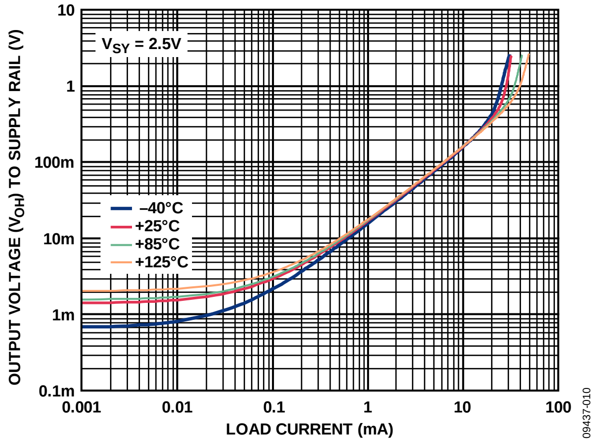

Figure 20. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

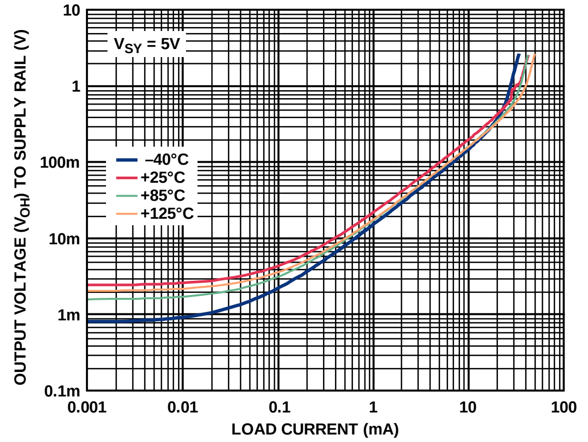

Figure 23. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

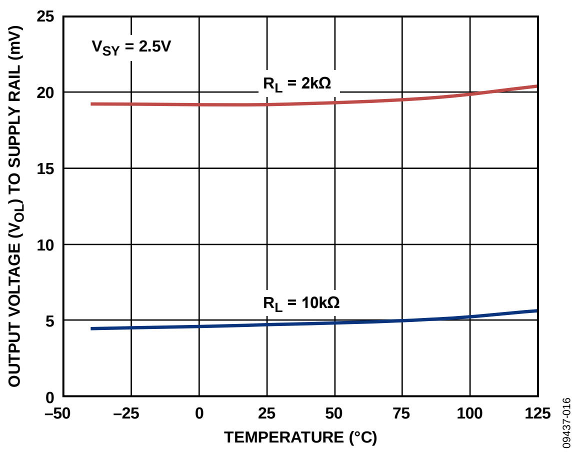

Figure 21. Output Voltage (V_{OL}) to Supply Rail vs. Temperature

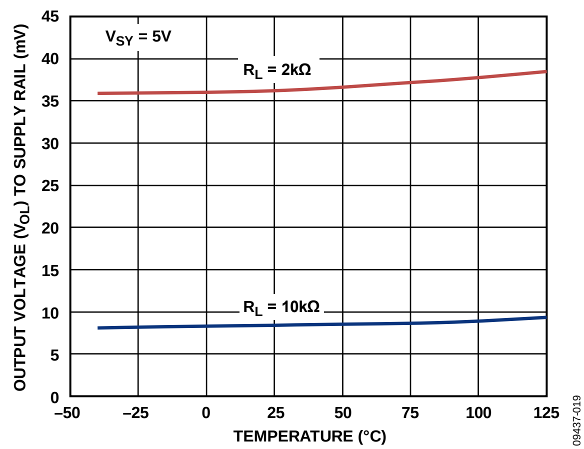

Figure 24. Output Voltage (V_{OL}) to Supply Rail vs. Temperature

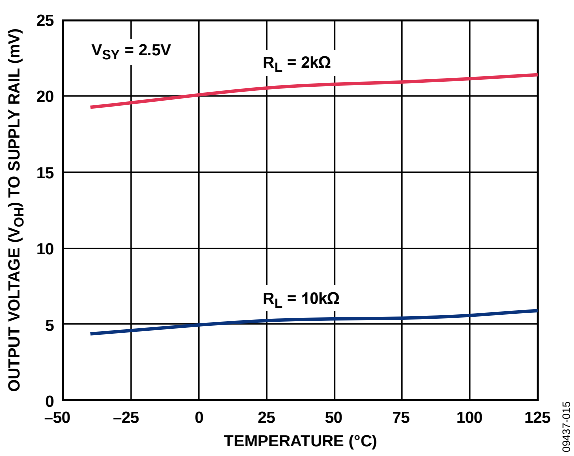

Figure 22. Output Voltage (V_{OH}) to Supply Rail vs. Temperature

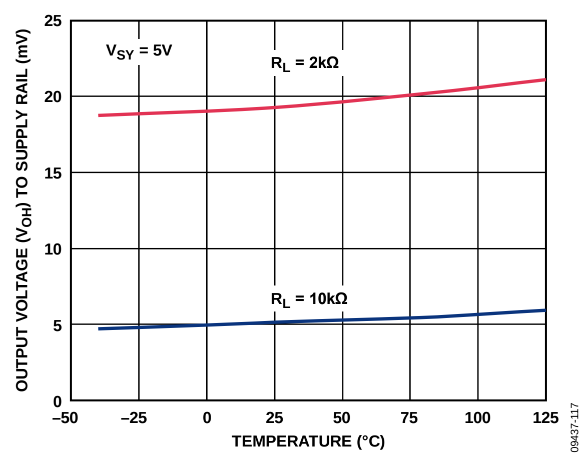

Figure 25. Output Voltage (V_{OH}) to Supply Rail vs. Temperature

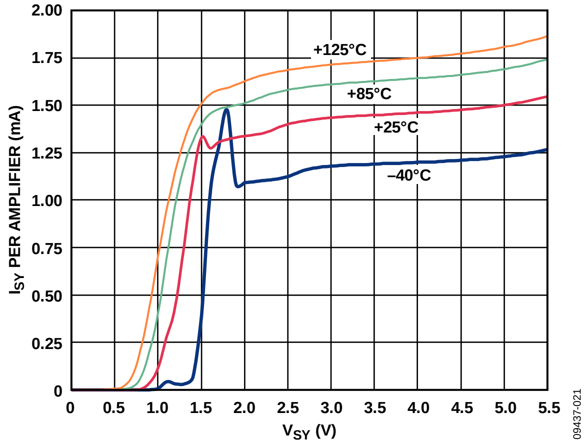

Figure 26. Supply Current vs. Supply Voltage

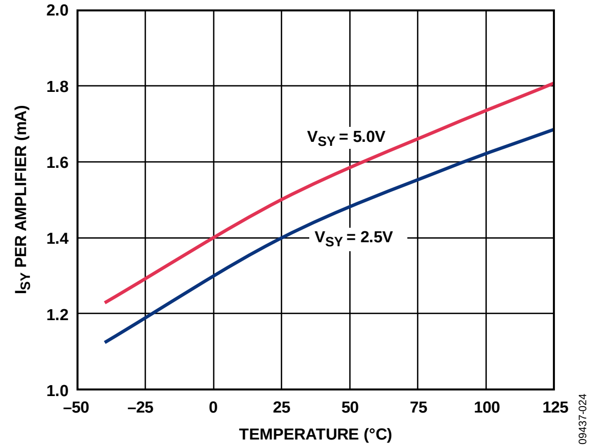

Figure 29. Supply Current vs. Temperature

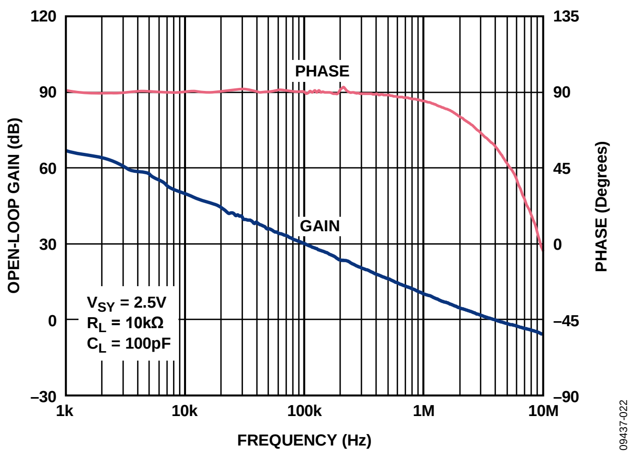

Figure 27. Open-Loop Gain and Phase vs. Frequency

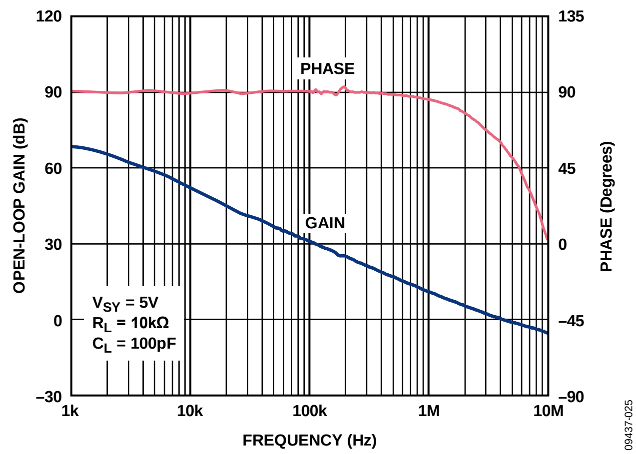

Figure 30. Open-Loop Gain and Phase vs. Frequency

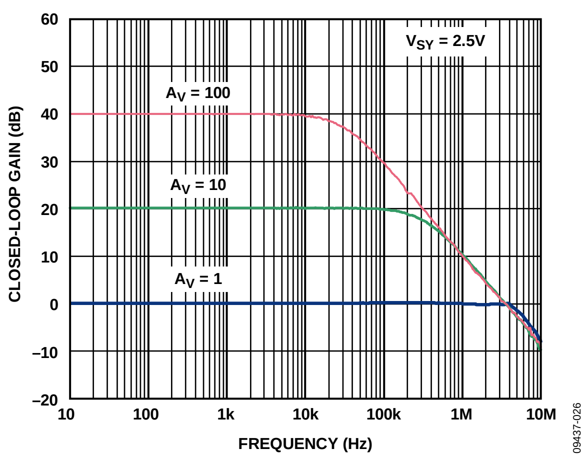

Figure 28. Closed-Loop Gain vs. Frequency

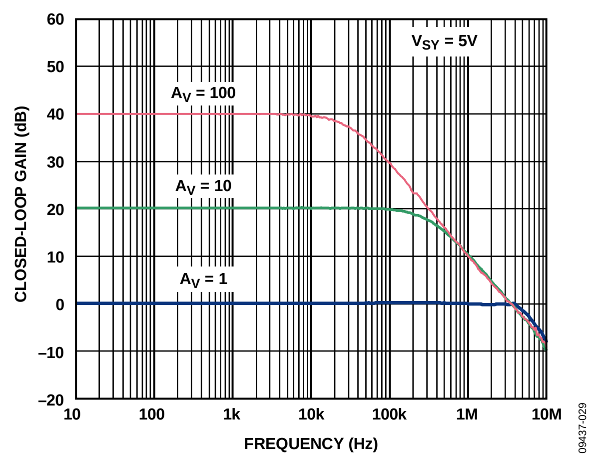

Figure 31. Closed-Loop Gain vs. Frequency

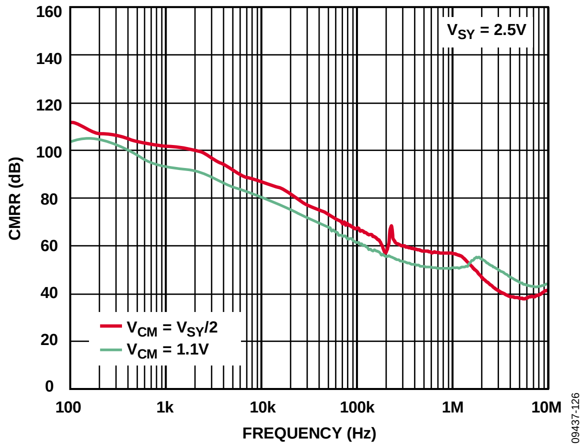

Figure 32. CMRR vs. Frequency

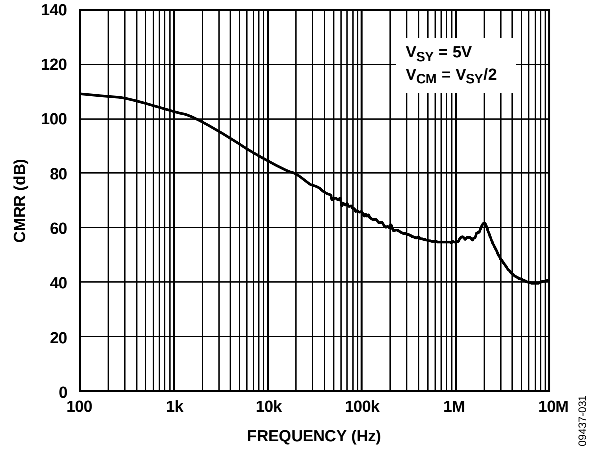

Figure 35. CMRR vs. Frequency

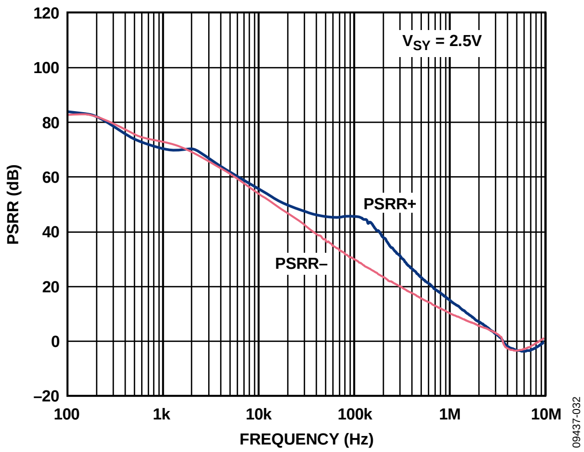

Figure 33. PSRR vs. Frequency

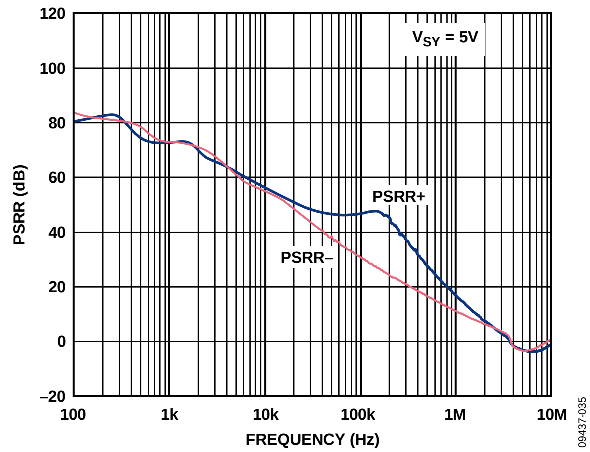

Figure 36. PSRR vs. Frequency

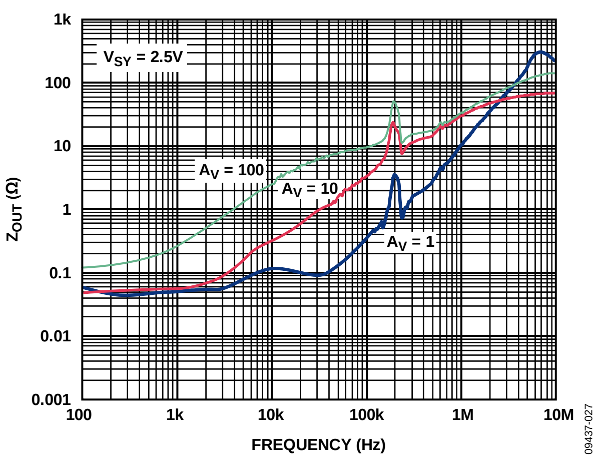

Figure 34. Closed-Loop Output Impedance vs. Frequency

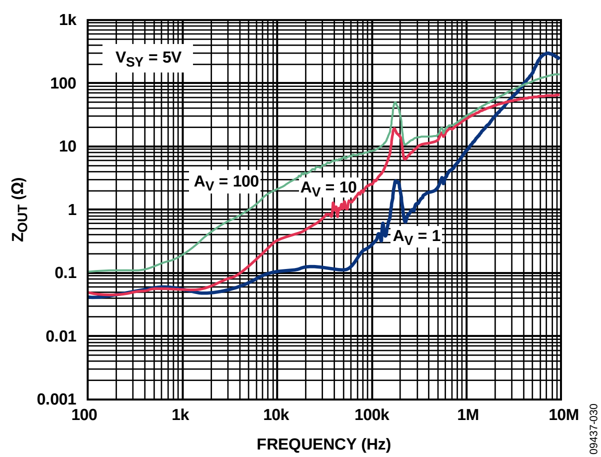

Figure 37. Closed-Loop Output Impedance vs. Frequency

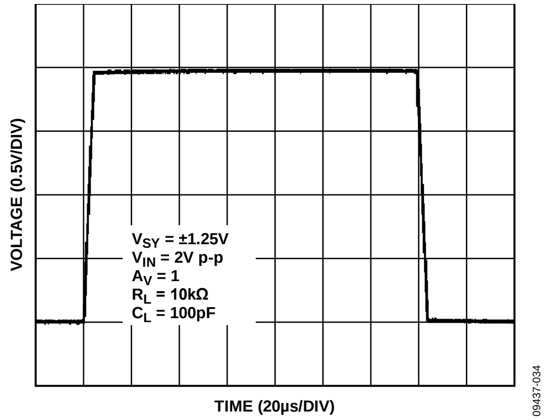

Figure 38. Large Signal Transient Response

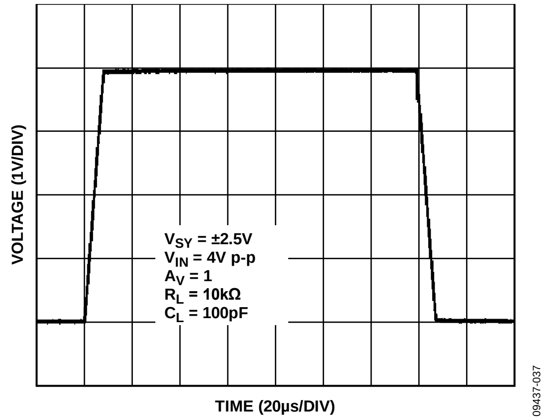

Figure 41. Large Signal Transient Response

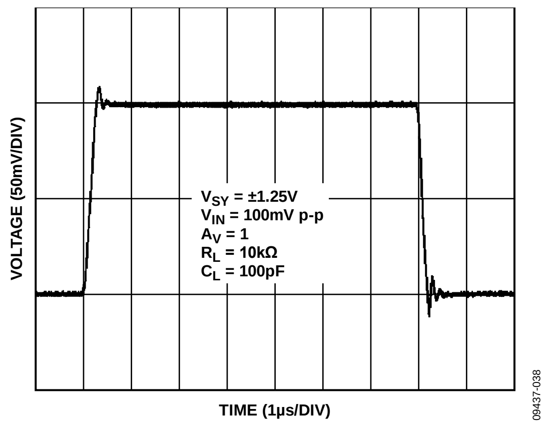

Figure 39. Small Signal Transient Response

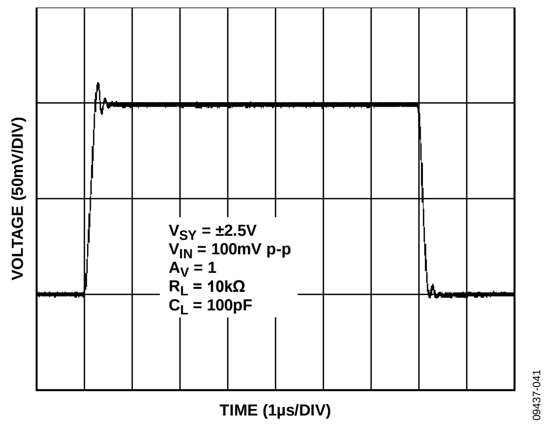

Figure 42. Small Signal Transient Response

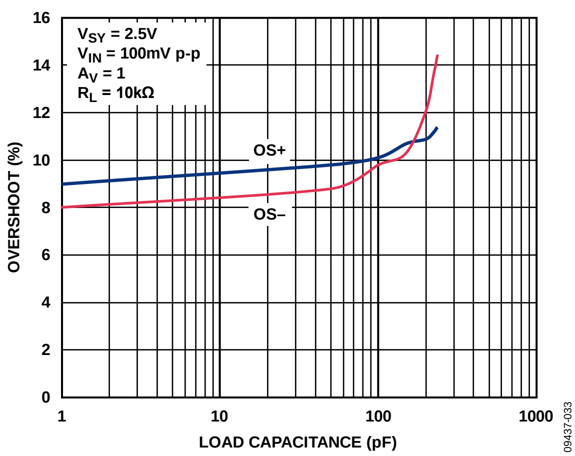

Figure 40. Small Signal Overshoot vs. Load Capacitance

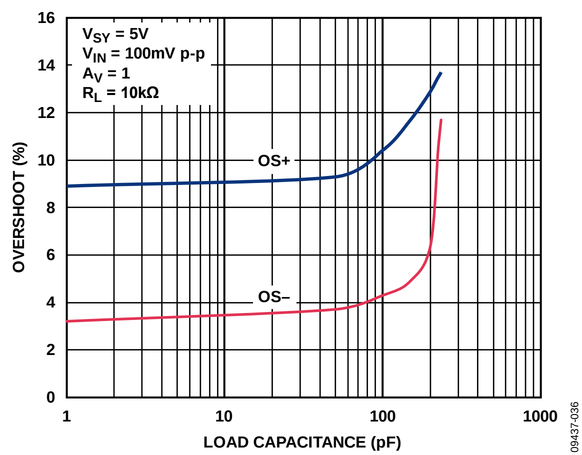

Figure 43. Small Signal Overshoot vs. Load Capacitance

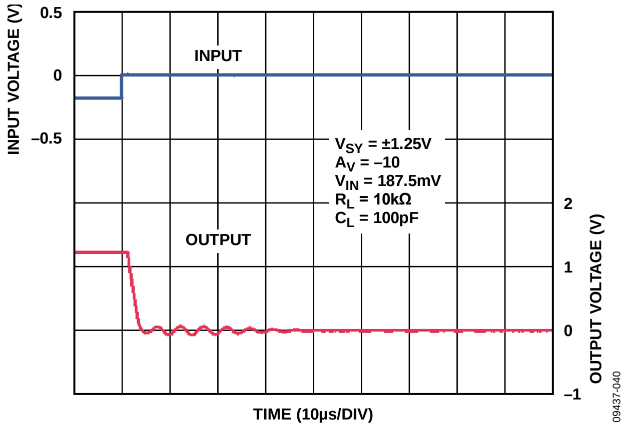

Figure 44. Positive Overload Recovery

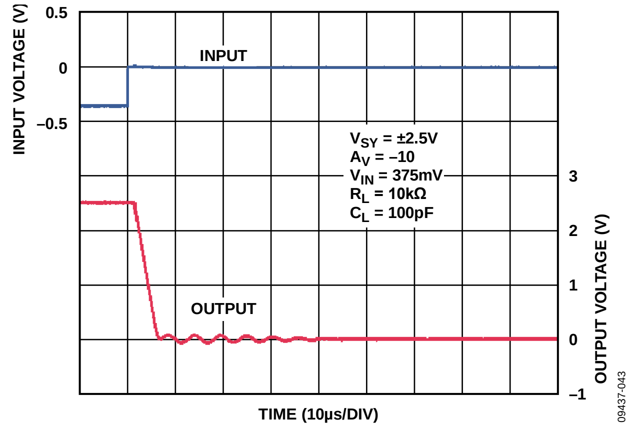

Figure 47. Positive Overload Recovery

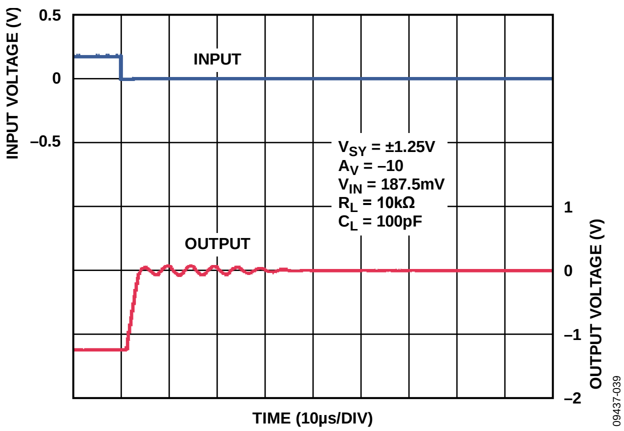

Figure 45. Negative Overload Recovery

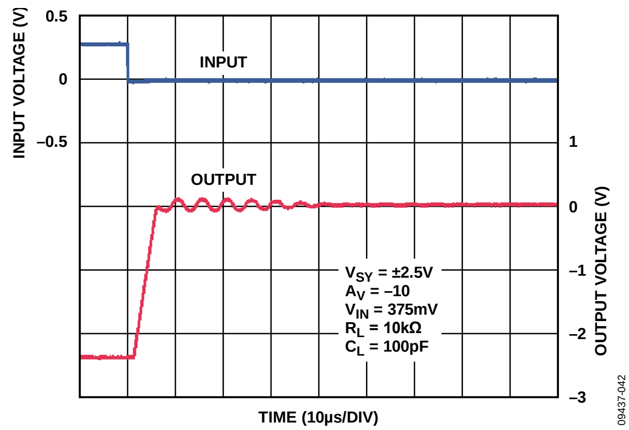

Figure 48. Negative Overload Recovery

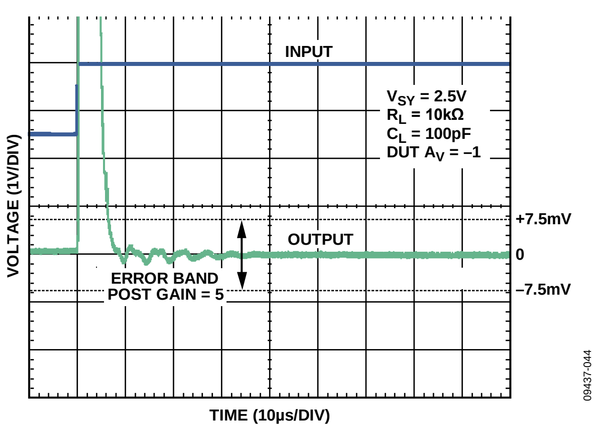

Figure 46. Positive Settling Time to 0.1%

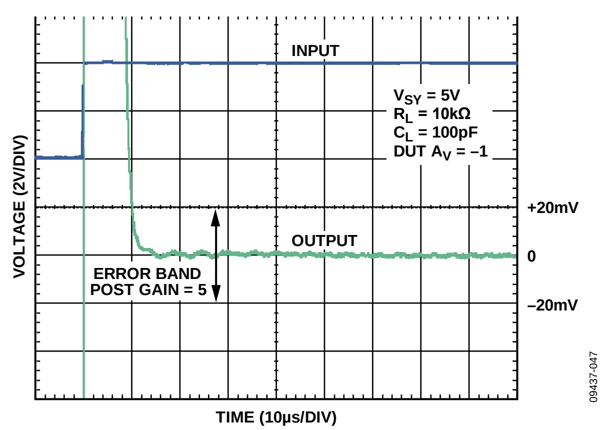

Figure 49. Positive Settling Time to 0.1%

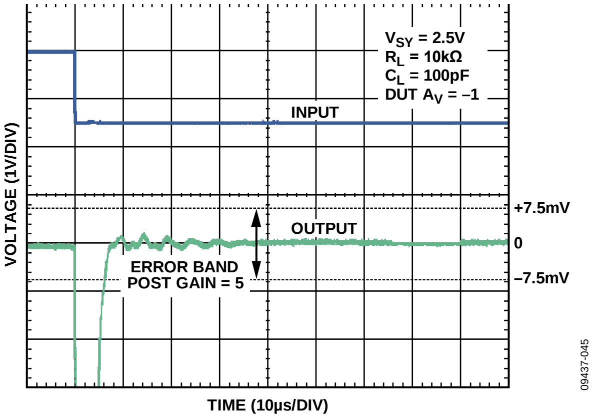

Figure 50. Negative Settling Time to 0.1%

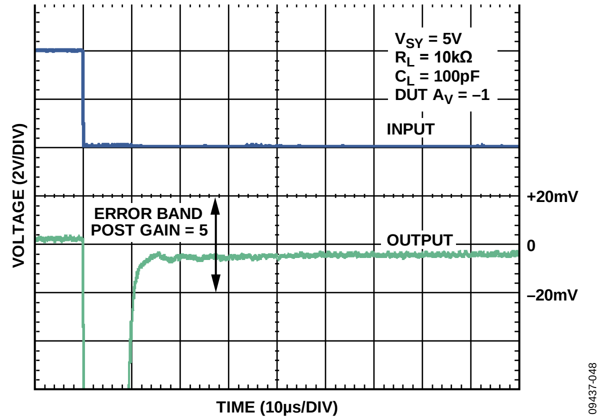

Figure 53. Negative Settling Time to 0.1%

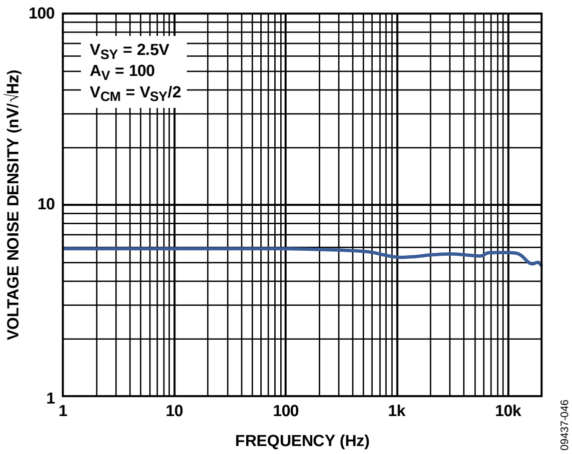

Figure 51. Voltage Noise Density vs. Frequency

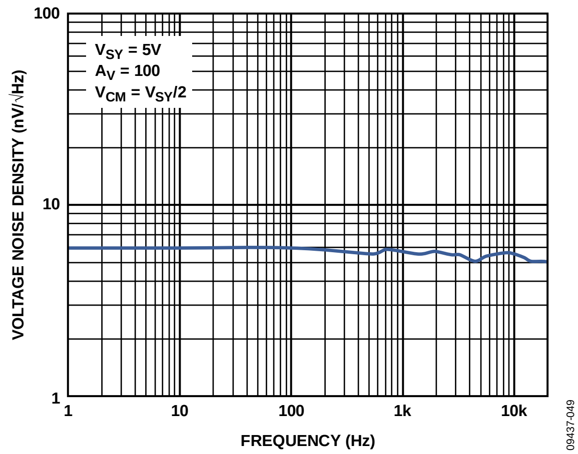

Figure 54. Voltage Noise Density vs. Frequency

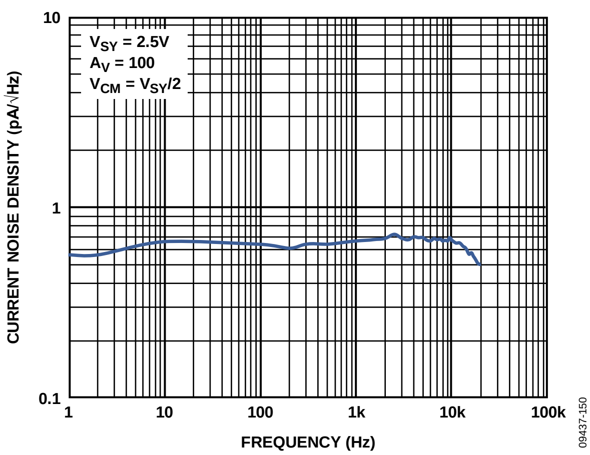

Figure 52. Current Noise Density vs. Frequency

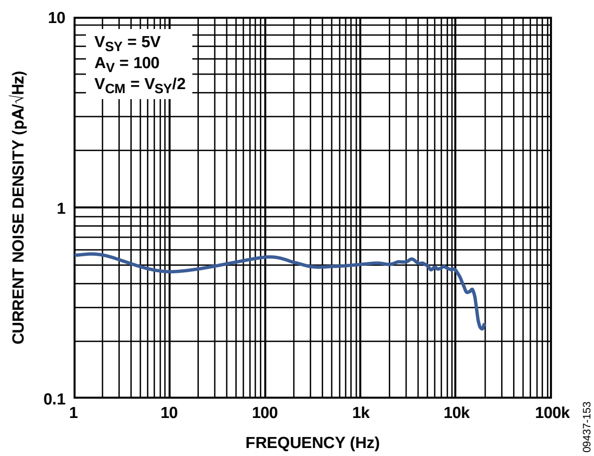

Figure 55. Current Noise Density vs. Frequency

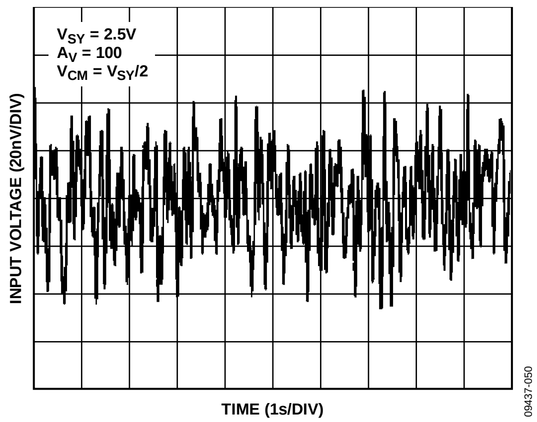

Figure 56. 0.1 Hz to 10 Hz Noise

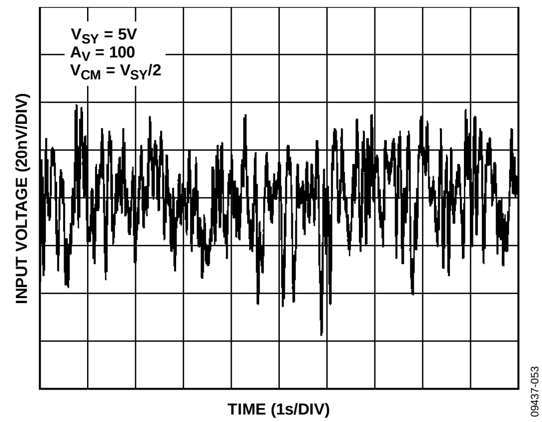

Figure 59. 0.1 Hz to 10 Hz Noise

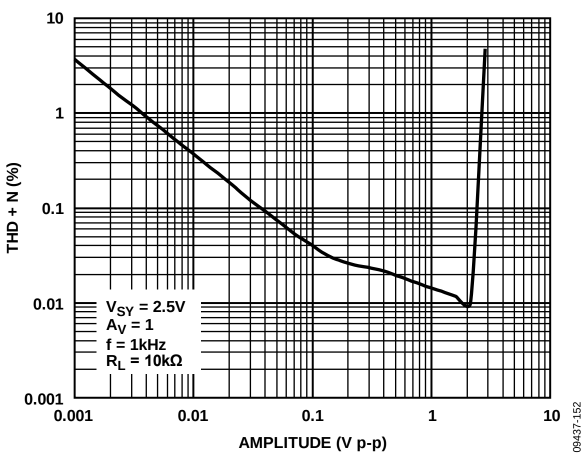

Figure 57. THD + N vs. Amplitude

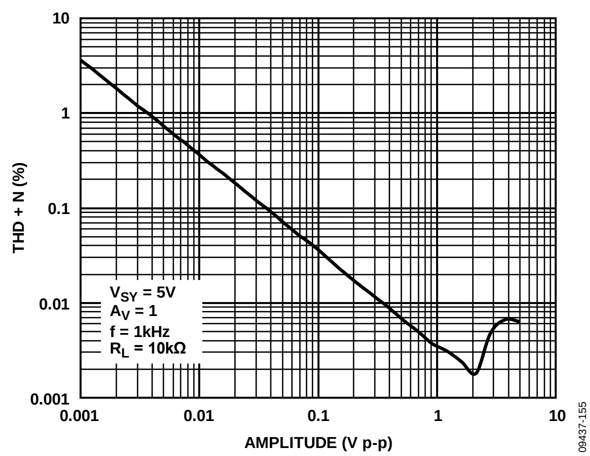

Figure 60. THD + N vs. Amplitude

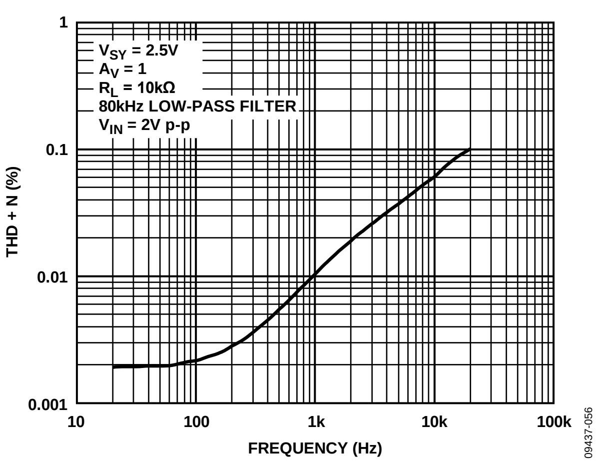

Figure 58. THD + N vs. Frequency

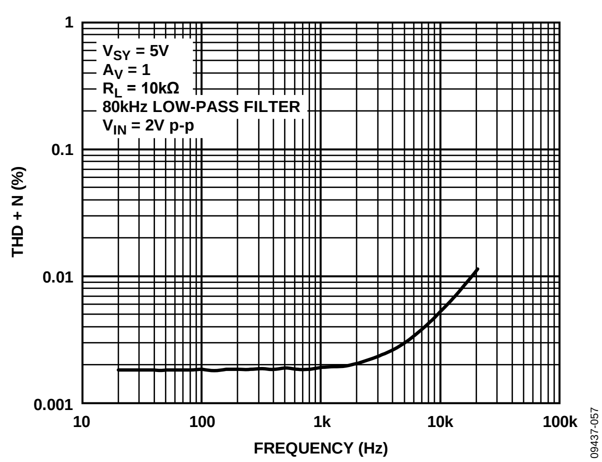

Figure 61. THD + N vs. Frequency

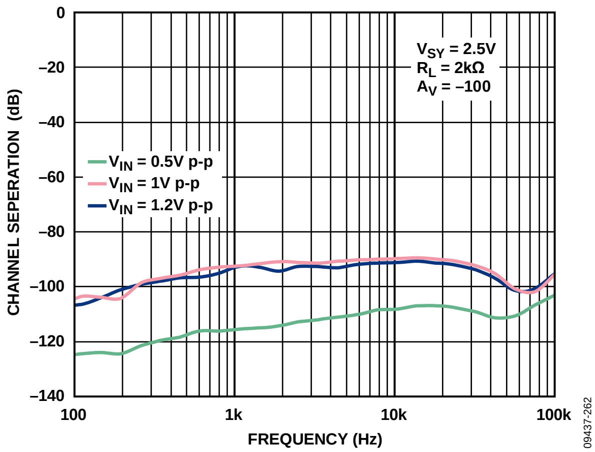

Figure 62. Channel Separation vs. Frequency

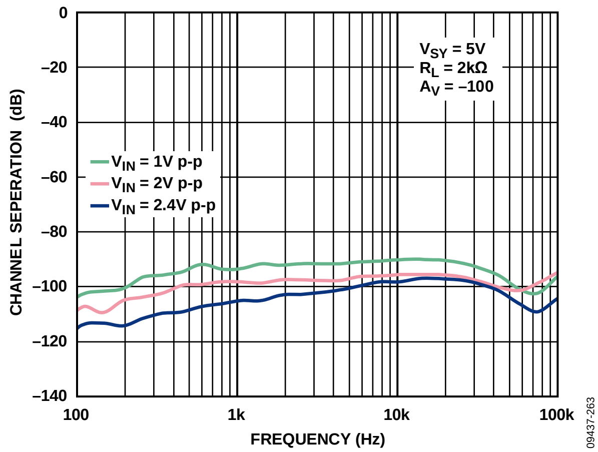

Figure 63.Channel Separation vs. Frequency

APPLICATIONS INFORMATION

The ADA4528-1/ADA4528-2 are precision, ultralow noise, zero-drift operational amplifiers that feature a patented chopping technique. This chopping technique offers ultralow input offset voltage of 0.3 µV typical and input offset voltage drift of 0.002 µV/°C typical.

Offset voltage errors due to common-mode voltage swings and power supply variations are also corrected by the chopping technique, resulting in a typical CMRR figure of 158 dB and a PSRR figure of 150 dB at 2.5 V supply voltage. The ADA4528-1/ADA4528-2 have low broadband noise of 5.6 nV/√Hz (at f = 1 kHz, A_V = +100, and V_{SY} = 2.5 V) with no 1/f noise component. These features are ideal for amplification of low level signals in dc or subhertz high precision applications.

For more information about the chopper architecture of the ADA4528-1/ADA4528-2, see the AN-1114 Application Note, *Lowest Noise Zero-Drift Amplifier Has 5.6 nV/√Hz Voltage Noise Density*.

INPUT PROTECTION

The ADA4528-1/ADA4528-2 have internal ESD protection diodes that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 300 mV beyond the rails to be applied at the input of either terminal without causing permanent damage (see Table 4 in the Absolute Maximum Ratings section).

When either input exceeds one of the supply rails by more than 300 mV, the ESD diodes become forward biased and large amounts of current begin to flow through them. Without current limiting, this excessive fault current causes permanent damage to the device.

If the inputs are subjected to overvoltage conditions, insert a resistor in series with each input to limit the input current to 10 mA maximum. However, consider the resistor thermal noise effect on the entire circuit.

For example, at a 5 V supply voltage, the broadband voltage noise of the ADA4528-1/ADA4528-2 is approximately 6 nV/√Hz (at unity gain). A 1 kΩ resistor has thermal noise of 4 nV/√Hz. Adding a 1 kΩ resistor at the noninverting input pin increases the total noise by 30% root sum square (rss).

RAIL-TO-RAIL INPUT AND OUTPUT

The ADA4528-1/ADA4528-2 feature rail-to-rail input and output with a supply voltage from 2.2 V to 5.5 V. Figure 64 shows the input and output waveforms of the ADA4528-1/ADA4528-2 configured as a unity-gain buffer with a supply voltage of ±2.5 V and a resistive load of 10 kΩ. With an input voltage of ±2.5 V, the ADA4528-1/ADA4528-2 allow the output to swing very close to both rails. Additionally, the devices do not exhibit phase reversal.

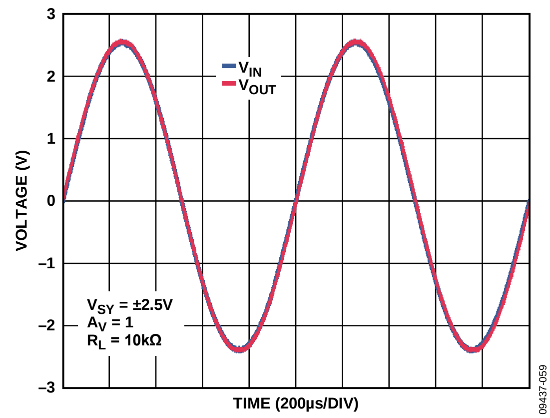

Figure 64. Rail-to-Rail Input and Output

NOISE CONSIDERATIONS

For more information about the noise characteristics of the ADA4528-1/ADA4528-2, see the AN-1114 Application Note, *Lowest Noise Zero-Drift Amplifier Has 5.6 nV/√Hz Voltage Noise Density*.

1/f Noise

1/f noise, also known as pink noise or flicker noise, is inherent in semiconductor devices and increases as frequency decreases. At low frequency, 1/f noise is a major noise contributor and causes a significant output voltage offset when amplified by the noise gain of the circuit. However, the ADA4528-1/ADA4528-2 eliminate the 1/f noise internally, thus making these devices an excellent choice for dc or subhertz high precision applications. The 0.1 Hz to 10 Hz amplifier voltage noise is only 97 nV p-p (A_V = +100) at a supply voltage of 2.5 V.

The low frequency 1/f noise, which appears as a slow varying offset to the ADA4528-1/ADA4528-2, is greatly reduced by the chopping technique. This reduction in 1/f noise allows the ADA4528-1/ADA4528-2 to have much lower noise at dc and low frequency compared to standard low noise amplifiers that are susceptible to 1/f noise. Figure 51 and Figure 54 show the voltage noise density of the amplifier with no 1/f noise.

Source Resistance

With 5.6 nV/√Hz of broadband noise at 1 kHz (V_{SY} = 2.5 V and A_V = +100), the ADA4528-1/ADA4528-2 are among the lowest noise zero-drift amplifiers currently available in the industry. Therefore, it is important to carefully select the input source resistance to maintain a total low noise.

The total input referred broadband noise (e_n total) from any amplifier is primarily a function of three types of noise: input voltage noise, input current noise, and thermal (Johnson) noise from the external resistors.

These uncorrelated noise sources can be summed up in a root sum squared (rss) manner using the following equation:

$$e_n\ total = [e_n^2 + 4\ kTR_S + (i_n \times R_S)^2]^{1/2}$$

where:
e_n is the input voltage noise of the amplifier (V/√Hz).
k is the Boltzmann's constant (1.38 × 10^{-23} J/K).
T is the temperature in Kelvin (K).
R_S is the total input source resistance (Ω).
i_n is the input current noise of the amplifier (A/√Hz).

The total equivalent rms noise over a specific bandwidth is expressed as

$$e_{n,rms} = e_n\ total \times \sqrt{BW}$$

where *BW* is the bandwidth in hertz.

This analysis is valid for broadband noise calculation. If the bandwidth of concern includes the chopping frequency, more complicated calculations must be made to include the effect of the noise energy spectrum at the chopping frequency (see the Residual Voltage Ripple section).

With a low source resistance of R_S < 1 kΩ, the voltage noise of the amplifier dominates. As source resistance increases, the thermal noise of R_S dominates. As the source resistance increases further, where R_S > 100 kΩ, the current noise becomes the main contributor to the total input noise. A good selection table for low noise op amps can be found in the AN-940 Application Note, *Low Noise Amplifier Selection Guide for Optimal Noise Performance*.

Voltage Noise Density with Different Gain Configurations

Figure 65 shows the voltage noise density vs. closed-loop gain of a zero-drift amplifier from a leading competitor. The voltage noise density of the amplifier increases from 11 nV/√Hz to 21 nV/√Hz as the closed-loop gain decreases from 1000 to 1.

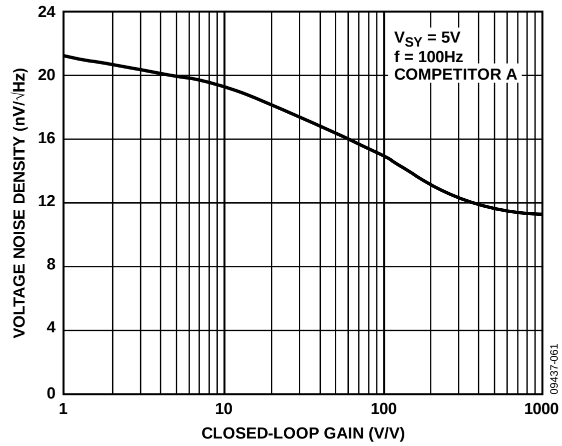

Figure 65. Competitor A: Voltage Noise Density vs. Closed-Loop Gain

Figure 66 shows the voltage noise density vs. frequency of the ADA4528-1/ADA4528-2 for three different gain configurations. The ADA4528-1/ADA4528-2 offer a constant input voltage noise density of 6 nV/√Hz to 7 nV/√Hz, regardless of the gain configuration.

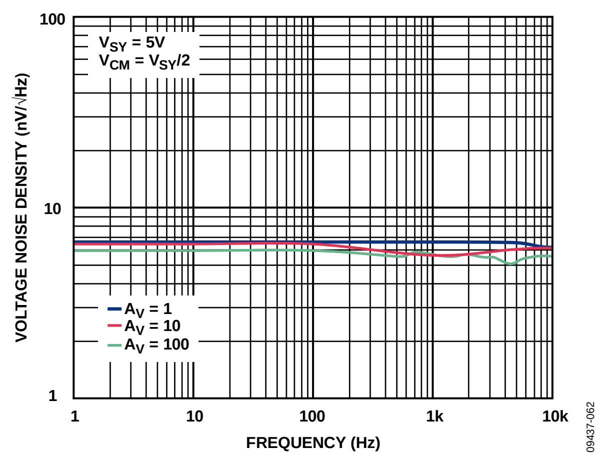

Figure 66. Voltage Noise Density vs. Frequency with Different Gain Configurations

Residual Voltage Ripple

Although autocorrection feedback (ACFB) suppresses the chopping related voltage ripple, higher noise spectrum exists at the chopping frequency and its harmonics due to the remaining ripple. Figure 67 shows the voltage noise density of the ADA4528-1/ADA4528-2 configured in unity gain. A noise energy spectrum of 50 nV/√Hz can be seen at the chopping frequency of 200 kHz. This noise energy spectrum is significant when the op amp has a closed-loop frequency that is higher than the chopping frequency.

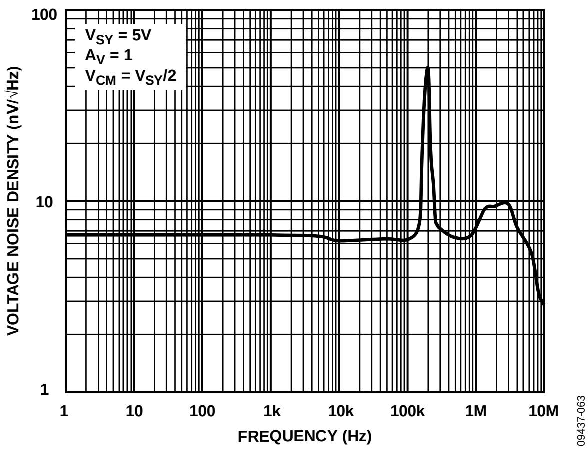

Figure 67. Voltage Noise Density vs. Frequency

To further suppress the noise at the chopping frequency, it is recommended that a post filter be placed at the output of the amplifier. For more information about residual voltage ripple, see the AN-1114 Application Note, *Lowest Noise Zero-Drift Amplifier Has 5.6 nV/√Hz Voltage Noise Density*.

COMPARATOR OPERATION

Figure 68 shows the ADA4528-2 configured as a voltage follower with an input voltage that is always kept at midpoint of the power supplies. The same configuration is applied to the unused channel. A1 and A2 indicate the placement of ammeters to measure supply current. As shown in Figure 69, as expected, in normal operating condition, $I_{SY}+ = I_{SY}- = 3$ mA for the dual ADA4528-2 at 5 V of supplies.

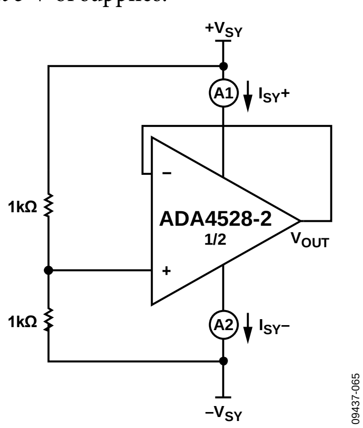

Figure 68. Voltage Follower

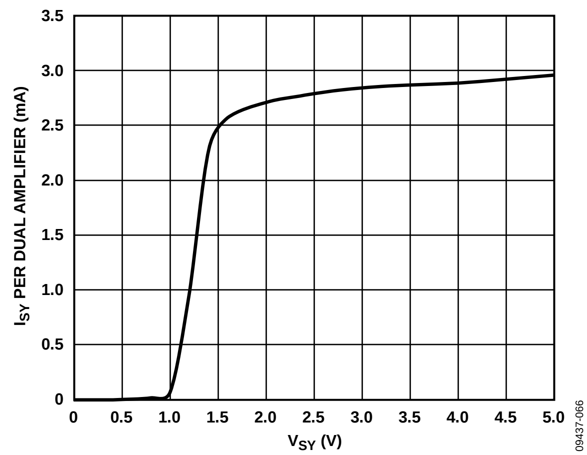

Figure 69. Supply Current vs. Supply Voltage (Voltage Follower)

Figure 70 and Figure 71 show the ADA4528-2 configured as comparators, with 1kΩ resistors in series with the input pins. Figure 72 shows the supply currents for both configurations. Supply currents increase slightly to 3.2 mA per dual amplifier at 5 V of supplies.

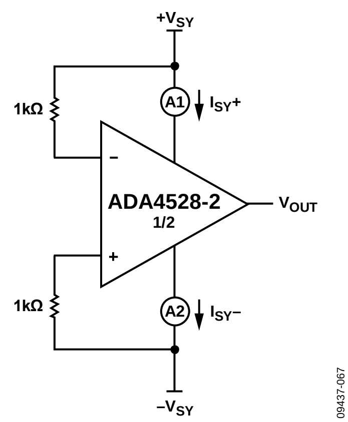

Figure 70. Comparator A

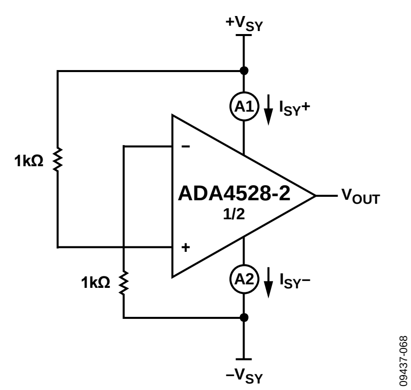

Figure 71. Comparator B

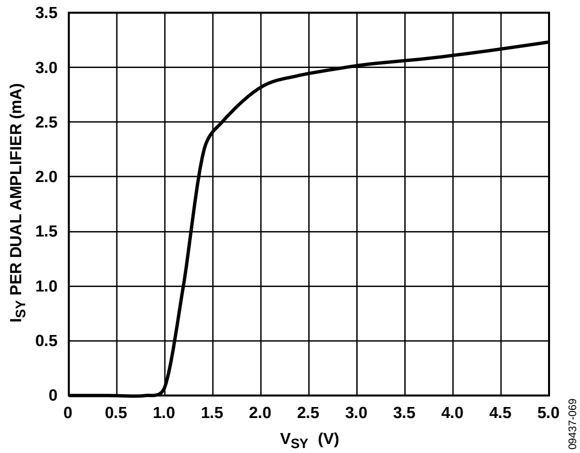

Figure 72. Supply Current vs. Supply Voltage (Comparator A and Comparator B)

For more details on op amps as comparators, refer to the AN-849 Application Note, *Using Op Amps as Comparators*.

PRINTED CIRCUIT BOARD LAYOUT

The ADA4528-1/ADA4528-2 are high precision devices with ultralow offset voltage and noise. Therefore, care must be taken in the design of the printed circuit board (PCB) layout to achieve the optimum performance of the ADA4528-1/ADA4528-2 at board level.

To avoid leakage currents, keep the surface of the board clean and free of moisture. Coating the board surface creates a barrier to moisture accumulation and reduces parasitic resistance on the board.

To minimize power supply disturbances caused by output current variation, properly bypass the power supplies and keep the supply traces short. Connect bypass capacitors as close as possible to the device supply pins.

Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at a distance of at least 5 mm from supply lines to minimize coupling.

A potential source of offset error is the Seebeck voltage on the circuit board. The Seebeck voltage occurs at the junction of two dissimilar metals and is a function of the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead.

Figure 73 shows a cross section of a surface-mount component soldered to a PCB. A variation in temperature across the board (where $T_{A1} \neq T_{A2}$) causes a mismatch in the Seebeck voltages at the solder joints, thereby resulting in thermal voltage errors that degrade the ultralow offset voltage performance of the ADA4528-1/ADA4528-2.

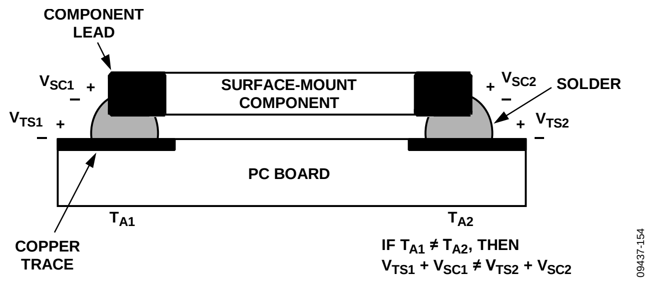

Figure 73. Mismatch in Seebeck Voltages Causes Seebeck Voltage Error

To minimize these thermocouple effects, orient resistors so that heat sources warm both ends equally. Where possible, the input signal paths must contain matching numbers and types of components to match the number and type of thermocouple junctions. For example, dummy components, such as zero value resistors, can be used to match the thermoelectric error source (real resistors in the opposite input path). Place matching components in close proximity and orient them in the same manner to ensure equal Seebeck voltages, thus canceling thermal errors. Additionally, use leads of equal length to keep thermal conduction in equilibrium. Keep heat sources on the PCB as far away from the amplifier input circuitry as practical.

It is highly recommended that a ground plane be used. A ground plane helps to distribute heat throughout the board, maintains a constant temperature across the board, and reduces EMI noise pickup.

OUTLINE DIMENSIONS

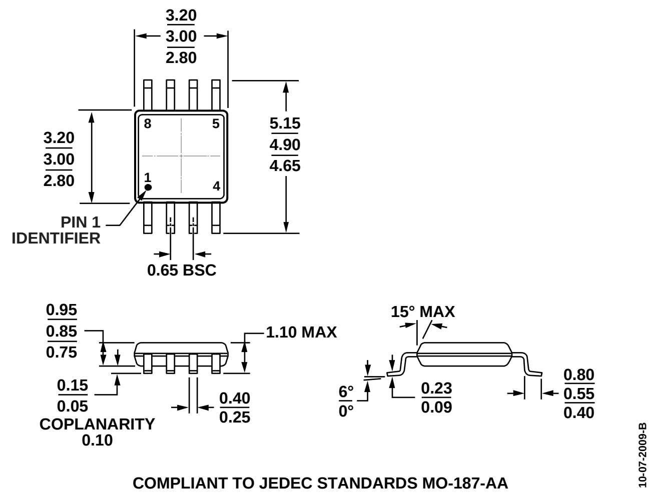

Figure 74. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

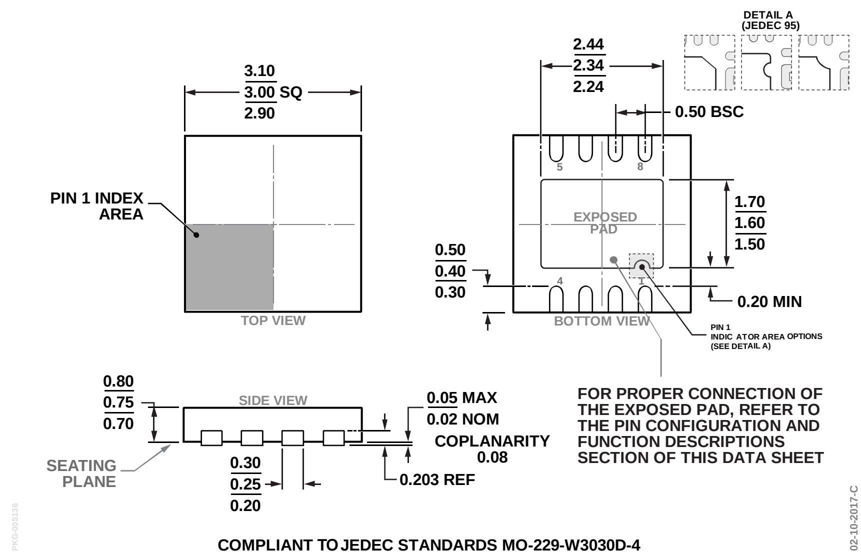

Figure 75. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-11)
Dimensions shown in millimeters

ORDERING GUIDE

Model [1]	Temperature Range	Package Description	Package Option	Branding
ADA4528-1ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2R
ADA4528-1ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2R
ADA4528-1ARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2R
ADA4528-1ACPZ-R2	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-11	A2R
ADA4528-1ACPZ-R7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-11	A2R
ADA4528-1ACPZ-RL	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-11	A2R
ADA4528-2ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A32
ADA4528-2ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A32
ADA4528-2ARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A32
ADA4528-2ACPZ-R7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-11	A32
ADA4528-2ACPZ-RL	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-11	A32

[1] Z = RoHS Compliant Part.

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