Bridge Sensor Signal Conditioner IC with LIN Interface, Nonlinearity Correction, Temperature Compensation

Data Sheet

ADA4558

FEATURES

LIN 2.1 compliant interface (bridge sensor signal, temperature)
Digitally programmable gain and offset voltage adjustment
Gain range from 2.94 V/V to 971.10 V/V
Sensor temperature compensation (first- or second-order)
Sensor nonlinearity correction (first- or second-order)
Internal or external temperature sensor compensation
EEPROM nonvolatile memory for calibration data
High system accuracy: 0.1% FSR over temperature
EMC and EMI protection
Fault protection for open circuits and short circuits
4 mm × 4 mm, 20-lead LFCSP
6 V to 18 V supply operation
−40°C to +150°C operating temperature range
AEC-Q100 qualified for automotive applications

APPLICATIONS

Strain gage
Pressure signal conditioner for automotive vehicles

GENERAL DESCRIPTION

The ADA4558 is a fully integrated, sensor signal conditioner IC for bridge sensors. The device provides digital nonlinearity correction and temperature compensation via internal or external sensed temperatures using on-chip correction and calibration hardware that can be optimized for a specific bridge sensor.

The ADA4558 utilizes a fourth-order digital correction algorithm and delivers a system accuracy of 0.1% full scale range (FSR) for bridge sensors with second-order nonlinearity sensitivity. The ADA4558 includes a local interconnect network (LIN) physical interface for single-wire, high voltage communications in automotive environments. LIN 2.1 and earlier versions are supported. The LIN interface allows access to measurements, end of line (EOL) calibration, and a wide range of diagnostic functions.

The analog subsystem consists of an analog-to-digital converter (ADC) and a programmable gain amplifier (PGA) with a wide gain range from 2.94 V/V to 971.10 V/V. To minimize power supply noise, the bridge sensor is biased with an internal 4 V voltage regulator. The ADA4558 is fully specified from −40°C to +150°C. The device operates from battery supply voltages of 6 V to 18 V. The ADA4558 is available in a 4 mm × 4 mm, 20-lead lead frame chip scale package (LFCSP).

FUNCTIONAL BLOCK DIAGRAM

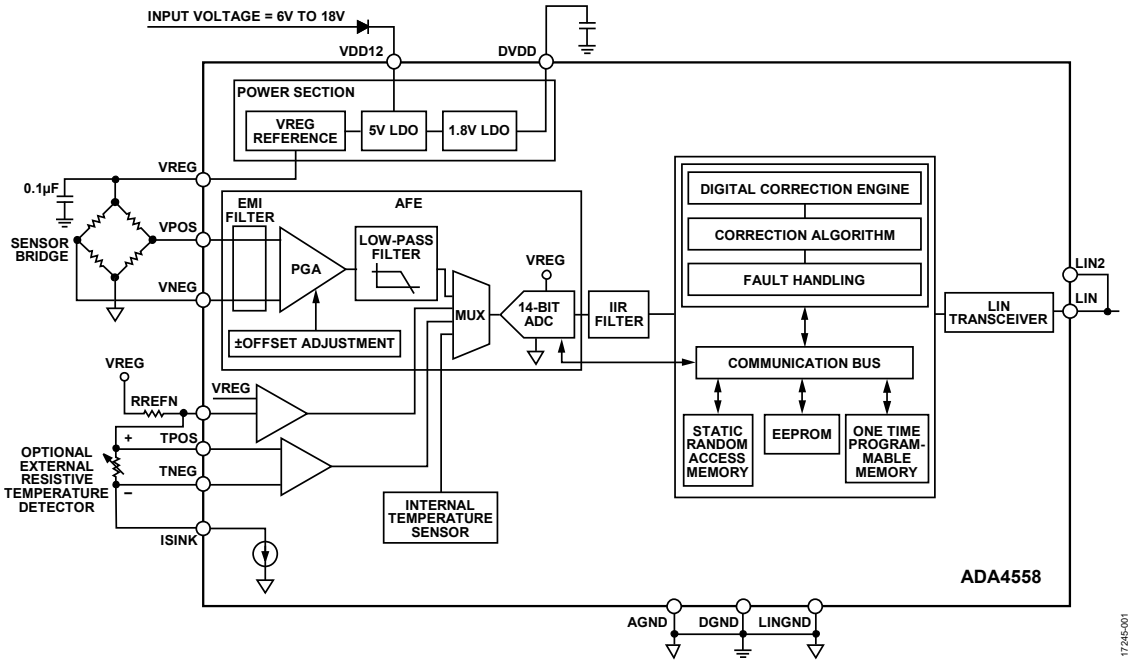

Figure 1.

Rev. 0 **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

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REVISION HISTORY

6/2019—Revision 0: Initial Version

SPECIFICATIONS

Supply voltage (VDD12) = 12 V, common-mode voltage (V_{CM}) = 2 V, and T_A = 25°C, unless otherwise specified. Minimum and maximum values are specified over the full supply voltage and a temperature range of −40°C to +150°C.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY (SYSTEM)						
Supply Voltage	VDD12		6	12	18	V
Operating Range[1]	$VDD12_{LOAD\ DUMP}$	Load dump for 0.3 sec	27			V
	$VDD12_{JUMP\ START}$	Jump start for 60 sec	26			V
Undervoltage Lockout (UVLO)	V_{UVLO}					
Rising				5.1		V
Hysteresis				0.2		V
Supply Current	I_{SY}	Normal operation, VREG current (I_{VREG}), LIN current (I_{LIN}) = 0 mA, T_A = −40°C to +85°C		5.0	7	mA
		Normal operation, I_{VREG}, I_{LIN} = 0 mA, T_A = −40°C to +150°C			8.2	mA
Sleep Mode Current		Enabled with inactivity on the LIN bus		150		µA
VREG Output	V_{REG}		3.8	4.0	4.2	V
VREG Temperature Coefficient[2]				95		ppm/°C
DVDD Regulated Voltage	DV_{DD}		1.6	1.8	2.0	V
SYSTEM SPECIFICATIONS						
Full-Scale Accuracy with Calibration		Sensor characteristic dependent				
		PGA gain = 2.94 V/V to 162.52 V/V		0.1		% FSR
		PGA gain = 224.72 V/V to 971.10 V/V		0.25		% FSR
INPUT STAGE						
PGA Gain Setting			2.94		971.10	V/V
Common-Mode Input Voltage Range			34		65	% V_{REG}
Bridge Resistance	R_{BR}		2		20	kΩ
Input Electromagnetic Interference (EMI) Filter[3]						
Cutoff Frequency ($f_{-3\ dB}$) Differential				0.55		MHz
$f_{-3\ dB}$ Common Mode				0.58		MHz
Input Offset						
Voltage[4]	V_{OS}			5	20	µV
Voltage Drift	T_CV_{OS}			10		nV/°C
Maximum Input Capacitance		VPOS/VNEG nodes			15	nF
COARSE OFFSET[5]						
Bridge Offset Cancellation Range		At PGA input		±60		mV/V
Offset Trim						
Resolution		PGA gain = 2.94		6		Bits
		PGA gain = 971.10		14		Bits
Step Size		At PGA output		31		mV
COARSE GAIN						
Gain Setting Accuracy		Gain = 2.94 to 162.52	−1.2	±0.2	+1.2	%
		Gain = 224.72 to 971.10	−2.75	±1	+2.75	%
Gain Error Temperature Coefficient		Gain ≤ 573.0			50	ppm/°C
		Gain = 722.3			64	ppm/°C
		Gain = 971.10			121	ppm/°C
ADC PERFORMANCE						
Main ADC Resolution				14		Bits
ADC Integral Nonlinearity (INL)			−4		+4	LSB_{14}
ADC Differential Nonlinearity (DNL)			−1		+1	LSB_{14}

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
EXTERNAL TEMPERATURE SENSOR						
Valid Temperature Range			−50		+165	°C
External Temperature Sensor Accuracy		Two calibration points using a PT1000 sensor	−0.5		+0.5	°C
		One calibration point using a PT1000 sensor	−2		+2	°C
Gain Setting Accuracy			−2	±0.2	+2	%
LIN INPUT AND OUTPUT STAGE		Compliant with LIN Specification 2.1				
Voltage		Voltage range over which LIN is functional	6		18	V
Baud Rate			1		20	kbps
Current Limit for Driver (LIN Bus Dominant State)	ILIN_DOM_MAX	Pulled to maximum VDD12	40		200	mA
Driver Off	ILIN_PASS_REC	8 V < VDD12 < 18 V, V_{LIN} ≥ VDD12			20	µA
Input Leakage	ILIN_PAS_DOM	V_{LIN} = 0 V	−1			mA
LIN Pin Current						
While Ground Disconnected	ILIN_NO_GND	VDD12 = 12 V, control unit disconnected from ground	−1		+1	mA
While Battery Disconnected	ILIN_NO_BAT	VDD12 disconnected, 0 V < V_{LIN} < 18 V			30	µA
LIN Receiver						
Dominant State	VLIN_DOM				40	%VDD12
Recessive State	VLIN_REC		60			%VDD12
Center Voltage	VLIN_CNT		47.5	50	52.5	%VDD12
Hysteresis Voltage	VHYS				17.5	%VDD12
Slave Termination Resistance	RSLAVE		21	25	34	kΩ
LIN RECEIVER TIMING PARAMETERS						
Propagation Delay of Receiver	t_{RX_PD}				6	µs
Symmetry of Receiver Propagation Delay	t_{RX_SYM}	Rising edge with the respect to falling edge	−2		+2	µs
LIN DRIVER TIMING PARAMETERS		Bus load conditions (C_{BUS}, R_{BUS}): 1 nF and 1 kΩ; 6.8 nF and 660 Ω; 10 nF and 500 Ω				
Duty Cycle 1	D1	For proper operation at 20 kbps	0.396			
Duty Cycle 2	D2	For proper operation at 20 kbps			0.581	
Duty Cycle 3	D3	For proper operation at 10.4 kbps	0.417			
Duty Cycle 4	D4	For proper operation at 10.4 kbps			0.590	
ADC Measurement Time		To valid reading			120	µs
LIN SLEEP/WAKE-UP		Force sleep mode by sending a diagnostic master request frame (frame identifier = 0x3C, with the first data byte equal to 0x00); sleep mode is also entered if there is no activity on the LIN bus for a certain time				
Auto Sleep Enable Time		Wake-up occurs if a recessive to dominant transition on the LIN bus is followed by a dominant level on the LIN bus maintained for a certain time (minimum dominant time), followed by a dominant to recessive transition; the dominant to recessive transition wakes up the device		4		sec
Minimum Dominant Time				150		µs

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Start-Up Time (System)		First readback of valid data, filter setting = 500 Hz, all faults enabled or disabled			100	ms
Main Oscillator Frequency		All internal timers are related to oscillator	9.5	10	10.5	MHz
Oscillator Frequency (Sleep Mode)				300		kHz
ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)						
Programming						
Number of Cycles			1000			Cycles
Time		Per 32-bit written word		20	40	ms
Temperature			−40		+150	°C
Data Retention		1000 write cycles, operation at 150°C	10			Years
		1000 write cycles, 40,000 hour operation (10,000 hours at 55°C + 27,000 hours at 125°C + 3000 hours at 150°C)	15			Years
FAULTS						
Bridge Sensor Input Bias Current	I_B	Detects input open circuit (startup)		5		µA
		Detects input open circuit, normal/running mode operation (EEPROM register PGA_ADD_PULUP_150 = 0), default		300		nA
		Detects input open circuit, normal/running mode operation (EEPROM register PGA_ADD_PULUP_150 = 1)		450		nA
Input Open Detection Resistance		Startup		320		kΩ
		Normal running mode operation		32		MΩ
Open Detection Threshold						
Low				18.75		% V_{REG}
High				81.25		% V_{REG}
Input Short Detection Resistance				0.5		kΩ
Oscillator Crosscheck Limit				14		%
External Temperature Sensor Bias Current		Detects external temperature open circuit		28		nA
Thermal Shutdown	T_{SD}			170		°C
Hysteresis	T_{SD_HY}			7		°C

[1] Guaranteed by absolute maximum ratings (see the Absolute Maximum Ratings section).
[2] The VREG voltage is also the reference to the ADC. Therefore, reference temperature drift does not affect system error. This specification can be useful in gain and offset selection at EOL calibration.
[3] Guaranteed by design.
[4] Errors in PGA, temperature sensor gain, offset, and temperature drift are eliminated based on the EOL calibration routine.
[5] The input offset trim range is −60 mV/V to +60 mV/V. The ADC reference is 4 V. The resulting input offset trim range is 0.48 V. The output preferred offset trim resolution is 31 mV. For a gain of 2.9, the input referred offset trim resolution is 10.6 mV. Dividing range by resolution gives approximately 50 steps, which is close to a 6-bit resolution. For a gain of 971, the input referred offset trim resolution is 32 µV. Dividing range by resolution equals 16,287 LSBs, which is close to 14-bit resolution. In all cases, this only provides the coarse offset calibration required to get the PGA output into the valid ADC range of operation. The digital linearization engine provides fine offset calibration to meet the system accuracy targets.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VDD12	40 V
LIN	40 V
Reverse Protection	
VDD12	AGND to −0.3 V
LIN	−40 V
VREG, VPOS, VNEG, TPOS, TNEG, ISINK, RREFN	−0.3 V to +6 V
LIN Short-Circuit Duration to LINGND or VDD12	Indefinite
ESD	
Human Body Model (All Pins)	4000 V
LIN and LIN2 Pins	6000 V
Charged Device Model	1000 V
Machine Model	200 V
LIN, LIN2 ESD (IEC 61000-4-2)	>8 kV contact
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +150°C
Junction Temperature Range	−40°C to +165°C
Soldering Profile	IPC/JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

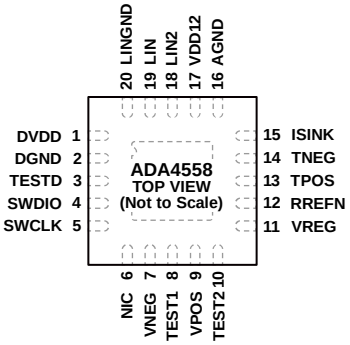
Package Type	θ_{JA}	θ_{JC}	Unit
CP-20-8[1]	49	1.42	°C/W

[1] Test Condition 1: Thermal impedance simulated values are based on JEDEC 4-layer test board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED. THIS PIN IS NOT INTERNALLY CONNECTED. CONNECT NIC TO THE GROUND PLANE.
2. CONNECT THE EXPOSED PAD OF THE LFCSP PACKAGE TO THE ANALOG GROUND PLANE. ENSURE THAT AGND IS CONNECTED TO DGND AND LINGND AT A SINGLE POINT ON THE PCB.

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DVDD	1.8 V Low Dropout (LDO) Digital Supply. Add a 0.1 µF capacitor placed as close to Pin 1 as possible between DVDD and the DGND plane.
2	DGND	Digital Ground.
3	TESTD	Test Pin. Analog Devices, Inc., uses this pin at the production test. Connect TESTD to the DGND plane in the application.
4	SWDIO	Test Pin. Analog Devices uses this pin at the production test. Connect SWDIO to the DGND plane in the application.
5	SWCLK	Test Pin. Analog Devices uses this pin at the production test. Connect SWCLK to the DGND plane in the application.
6	NIC	Not Internally Connected. This pin is not internally connected. Connect NIC to the ground plane.
7	VNEG	Negative Input. Pin 7 is the negative input to the PGA from the external resistive bridge.
8	TEST1	Test Pin. Analog Devices uses this pin at the production test. Connect TEST1 to the AGND plane in the application.
9	VPOS	Positive Input. Pin 9 is the positive input to the PGA from an external resistive bridge.
10	TEST2	Test Pin. Analog Devices uses this pin at the production test. Connect TEST2 to the AGND plane in the application.
11	VREG	Regulated 4.0 V Output. Pin 11 drives the top of the external bridge. Add a 0.1 µF capacitor between VREG and the AGND plane, placed as close to the VREG pin as possible.
12	RREFN	Reference Resistor. Pin 12 is the reference resistor for the external temperature sensor sense connection. Connect Pin 12 to ground when there is no external temperature sensor.
13	TPOS	External Temperature Positive Input. Connect Pin 13 to ground when there is no external temperature sensor.
14	TNEG	External Temperature Sensor Negative Input. Connect Pin 14 to ground when there is no external temperature sensor.
15	ISINK	Current Sink. Pin 15 drives the external temperature sensor. Connect Pin 15 to ground when there is no external temperature sensor.
16	AGND	Analog Ground.
17	VDD12	Supply. Connect the 12 V battery supply to this pin. Decouple VDD12 with a 1 µF capacitor. A 100 nF capacitor can be used only when a 1 µF capacitor to ground is placed on the anode of the diode on the module battery supply.
18	LIN2	Not in Use. The LIN2 function is not in use. Connect LIN2 to the LIN pin.
19	LIN	LIN Compliant Interface. All communication to and from the IC is via the LIN pin. Connect a LIN capacitor to ground on this pin, per the LIN specification.
20	LINGND	Local LIN Ground.
	EPAD	Exposed Pad. Connect the exposed pad of the LFCSP to the analog ground plane. Ensure that AGND is connected to DGND and LINGND at a single point on the PCB.

TYPICAL PERFORMANCE CHARACTERISTICS

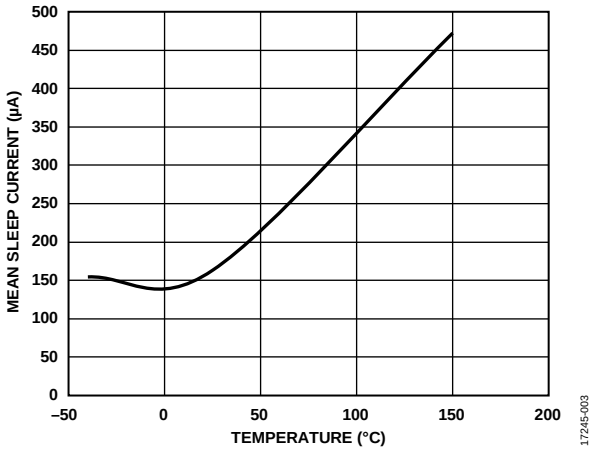


Figure 3. Mean Sleep Current vs. Temperature, VDD12 = 12 V

THEORY OF OPERATION

The ADA4558 interfaces to a range of Wheatstone resistive bridge sensors. Figure 1 shows the block diagram of the ADA4558. The differential signal from the bridge output is applied to the analog front end (AFE) and then to the infinite impulse response (IIR) filter. A correction algorithm is applied in the processor to compensate for sensor nonlinearity and temperature dependency.

The ADA4558 power section includes the 4 V regulator output at the VREG pin, which drives the bridge and the external temperature sensor. The VREG pin also supplies the reference to the ADC to create a fully ratiometric measurement system.

The AFE consists of an input EMI filter, inverting input switch, PGA, low-pass filter, mux switch, and 14-bit successive approximation register (SAR) ADC.

The differential signal from the bridge sensor is applied to the PGA, which amplifies the input differential signal and applies sensor offset voltage adjustment.

The internal mux selects the signal from the PGA, internal temperature sensor, external local temperature (optional), and other miscellaneous signals, and applies them to the 14-bit on-chip SAR ADC, which in turn converts the analog inputs into the digital domain for further processing.

Next, the digital signal is applied to the IIR filter to filter out any unwanted noise signals, after which time the filtered signal is applied to the processor.

The ADA4558 and bridge sensor are calibrated over its signal and temperature range by the customer via the ADA4558 LIN interface. Correction coefficients are calculated and stored in EEPROM. During normal operation, these correction coefficients are applied to the correction algorithm.

The ADA4558 uses a LIN interface to provide linearized bridge sensor data in customizable frame formats. The ADA4558 also provides temperature and extensive diagnostics and status information. LIN 2.1, LIN 2.0, and LIN 1.3 modes are supported.

For more information and register details for the ADA4558, see the ADA4558 Hardware Reference Manual.

APPLICATIONS INFORMATION

TYPICAL CONNECTION DIAGRAM

Figure 4 shows the typical connection diagram for the ADA4558, and Table 5 provides the component list.

EMC PERFORMANCE

The ADA4558 meets the electromagnetic compatibility (EMC) requirements specified in OEM Hardware Requirements for LIN, CAN, and FlexRay interfaces in Automotive Applications Revision 1.3, May 2012 using the applications reference circuit and corresponding bill of materials.

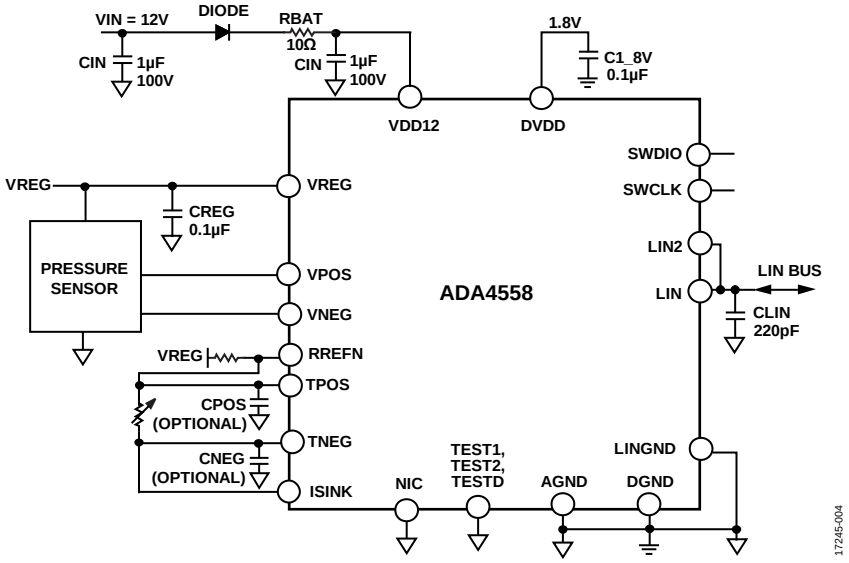


Figure 4. Typical Connection Diagram

Table 5. Component List

Product Reference	Temperature Range	Package Description	Package	Product No.
ADA4558	−40°C to +150°C	20-lead LFCSP	CP-20-8	ADA4558
RBAT	−40°C to +150°C	10 Ω, 250 mW resistor to meet ISO transients	0603	CRCW060310R0JNEAHP
CREG, C1_8V	−55°C to +125°C	Murata, X7R, 16 V, 0.1 µF	0402	GCG155R71C104KA15D
CIN	−55°C to +125°C	TDK, X7S, 100 V, 1 µF	0805	CGA4J3X7S2A105K
Diode	−55°C to +125°C	150 V, reverse protection diode	SOD323	BAS21-03WE6327
CLIN	−55°C to +125°C	220 pf, LIN capacitor	0402	GCM155R72A221KA37

PCB LAYOUT GUIDELINES

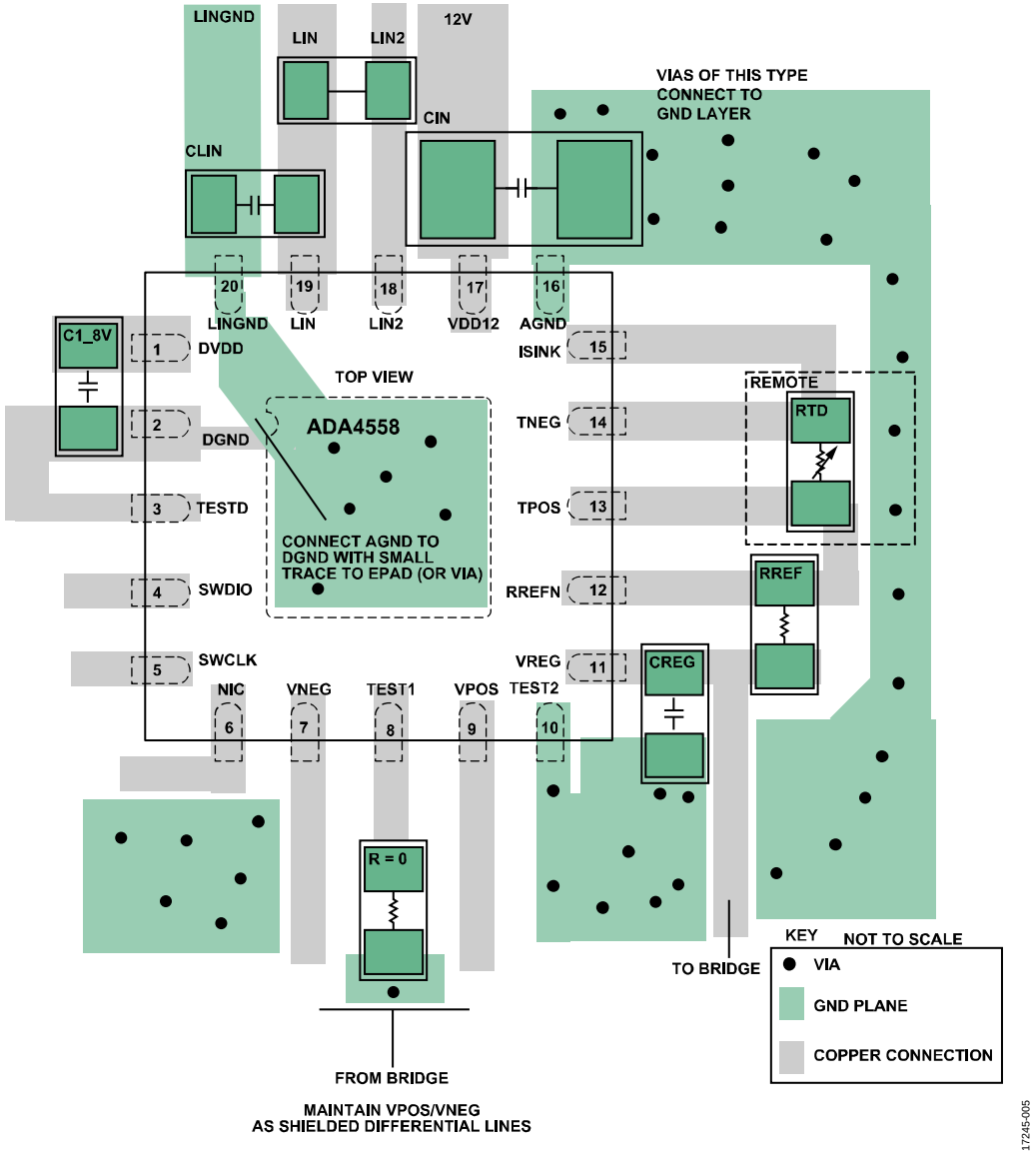


Figure 5. Example PCB Layout

The following items outline best practice for PCB layout.

- Place the 220 pF CLIN capacitor close to the IC between the LIN and LINGND traces.
- Place the CREG, CIN, and C1_8V capacitors close to the IC using short, thick tracks. These components decouple the supplies and reduce high frequency noise on these nodes.
- The length of the C1_8V traces is critical. Keep the traces as short as possible.
- Shield the noisy DVDD regulator pin from the sensitive analog circuitry at VPOS, VNEG, and VREG.
- Maintain shielded matched differential lines for VNEG and VPOS to ensure that noise pickup is both minimal and common mode. The PGA can potentially obtain significant noise at this point.
- Shield the VPOS trace from the VREG trace because VREG can have noise pickup during EMC testing.
- Shield the VDD12 line from VPOS, VNEG, and VREG using a ground plane.
- Connect DGND and LINGND to AGND at a single point. Use a short narrow trace for DGND and a wide trace for LINGND.
- TESTD is connected internally to DGND. Connect Pin 3 to a small DGND plane to avoid multiple connections between AGND and DGND.
- To minimize total ground plane impedance, use a separate ground layer, if available, with many via connections to the top layer ground plane.
- When a second routing layer is available, the LINGND trace can be connected to the AGND plane with a large via close to CDVDD. Connect DGND to AGND at this point with a narrow trace.

OUTLINE DIMENSIONS

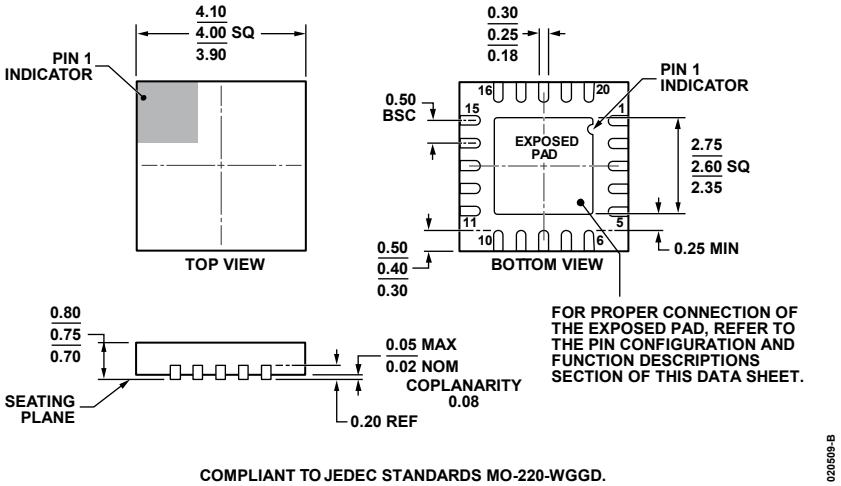


Figure 6. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-20-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADA4558WHCPZ-RL	–40°C to +150°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-8
ADA4558WHCPZ-R7	–40°C to +150°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-8
EVAL-ADA4558EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for automotive applications.

AUTOMOTIVE PRODUCTS

The ADA4558W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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