ANALOG DEVICES

# 30 V, High Speed, Low Noise, Low Bias Current, JFET Operational Amplifier

Data Sheet

# ADA4627-1/ADA4637-1

## FEATURES

**Low offset voltage: 200 µV maximum**
**Offset drift: 1 µV/°C typical**
**Very low input bias current: 5 pA maximum**
**Extended temperature range: −40°C to +125°C**
**±5 V to ±15 V dual supply**
**ADA4627-1 GBW: 19 MHz**
**ADA4637-1 GBW: 79 MHz**
**Voltage noise: 6.1 nV/√Hz at 1 kHz**
**ADA4627-1 slew rate: 82 V/µs**
**ADA4637-1 slew rate: 170 V/µs**
**High gain: 120 dB typical**
**High CMRR: 116 dB typical**
**High PSRR: 112 dB typical**

## APPLICATIONS

**High impedance sensors**
**Photodiode amplifier**
**Precision instrumentation**
**Phase-locked loop filters**
**High end, professional audio**
**DAC output amplifier**
**ATE**
**Medical**

## PIN CONFIGURATIONS

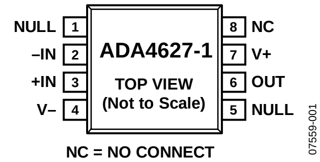


*Figure 1. 8-Lead SOIC_N (R-8)*

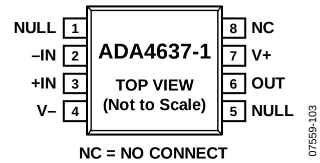


*Figure 2. 8-Lead SOIC_N (R-8)*

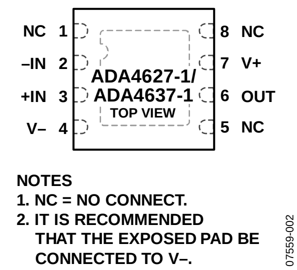


*Figure 3. 8-Lead LFCSP_VD (CP-8-13)*

## GENERAL DESCRIPTION

The ADA4627-1/ADA4637-1 are wide bandwidth precision amplifiers featuring low noise, very low offset, drift, and bias current. The devices operate from ±5 V to ±15 V dual supply.

The ADA4627-1/ADA4637-1 provide benefits previously found in few amplifiers. These amplifiers combine the best specifications of precision dc and high speed ac op amps. The ADA4637-1 is a decompensated version of the ADA4627-1 and is stable at a noise gain of 5 or greater.

With a typical offset voltage of only 70 µV, drift of less than 1 µV/°C, and noise of only 0.86 µV p-p (0.1 Hz to 10 Hz), the ADA4627-1/ADA4637-1 are suited for applications where error sources cannot be tolerated.

The ADA4627-1/ADA4637-1 are specified for both the industrial temperature range of −25°C to +85°C and the extended industrial temperature range of −40°C to +125°C. The ADA4627-1/ADA4637-1 are available in tiny 8-lead LFCSP and 8-lead SOIC packages.

The ADA4627-1/ADA4637-1 are members of a growing series of high speed, precision op amps offered by Analog Devices, Inc. (see Table 1).

**Table 1. High Speed Precision Op Amps**

| Supply | 5 V Low Cost | 5 V | 26 V Low Power | 30 V Low Cost | 30 V |
|---|---|---|---|---|---|
| Single | AD8615 | AD8651 | AD8610 | AD8510 | ADA4627-1/ADA4637-1 |
| Dual | AD8616 | AD8652 | AD8620 | AD8512 | |
| Quad | AD8618 | | | AD8513 | |


**Rev. F** **Document Feedback**




**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781.329.4700**



**Technical Support** **www.analog.com**

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**6/15—Rev. E to Rev. F**

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Changes to Ordering Guide ... 18

**1/14—Rev. D to Rev. E**

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**10/10—Rev. C to Rev. D**

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**7/10—Rev. B to Rev. C**

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Added Figure 2; Renumbered Sequentially ... 1
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**10/09—Rev. A to Rev. B**

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**9/09—Rev. 0 to Rev. A**

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**7/09—Revision 0: Initial Version**

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—30 V OPERATION

$V_{SY}$ = ±15 V, $V_{CM}$ = 0 V, $T_A$ = 25°C, unless otherwise noted.

**Table 2.**

| Parameter | Symbol | Test Conditions/Comments | B Grade Min | B Grade Typ | B Grade Max | A Grade Min | A Grade Typ | A Grade Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | | | | | |
| Offset Voltage[1] | $V_{OS}$ | | | 70 | 200 | | 120 | 300 | µV |
| | | −40°C ≤ $T_A$ ≤ +85°C | | | 350 | | | 410 | µV |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 400 | | | 660 | µV |
| Offset Voltage Drift, Average | $\Delta V_{OS}/\Delta T$ | −40°C ≤ $T_A$ ≤ +125°C | | 1 | 2 | | 1 | 3 | µV/°C |
| Power Supply Rejection Ratio | PSRR | $V_{SY}$ = ±4.5 V to ±18 V | 106 | 112 | | 103 | 108 | | dB |
| | | −40°C ≤ $T_A$ ≤ +125°C | 101 | | | 99 | | | dB |
| Input Bias Current[2] | $I_B$ | | | 1 | 5 | | 1 | 5 | pA |
| | | −40°C ≤ $T_A$ ≤ +85°C | | | 0.5 | | | 0.5 | nA |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 2 | | | 2 | nA |
| Input Offset Current | $I_{OS}$ | | | 0.5 | 5 | | 0.5 | 5 | pA |
| | | −40°C ≤ $T_A$ ≤ +85°C | | | 0.5 | | | 0.5 | nA |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | 2 | | | 2 | nA |
| NOISE PERFORMANCE | | | | | | | | | |
| Voltage Noise Density | $e_n$ | f = 10 Hz | | 16.5 | 40 | | 16.5 | 40 | nV/√Hz |
| | | f = 100 Hz | | 7.9 | 20 | | 7.9 | 20 | nV/√Hz |
| | | f = 1 kHz | | 6.1 | 8 | | 6.1 | 8 | nV/√Hz |
| | | f = 10 kHz | | 4.8 | 6 | | 4.8 | 6 | nV/√Hz |
| Voltage Noise | $e_n$ p-p | 0.1 Hz to 10 Hz | | 0.7 | 1.6 | | 0.7 | 1.6 | µV p-p |
| Current Noise Density | $i_n$ | f = 100 Hz | | 1.6 | | | 2.5 | | fA/√Hz |
| Current Noise | $i_n$ p-p | 0.1 Hz to 10 Hz | | 30 | | | 48 | | fA p-p |
| Input Resistance | $R_{IN}$ | | | 10 | | | 10 | | TΩ |
| Input Capacitance, Differential Mode | $C_{INDM}$ | | | 8 | | | 8 | | pF |
| Input Capacitance, Common Mode | $C_{INCM}$ | | | 7 | | | 7 | | pF |
| Input Voltage Range | IVR | | −11 | | +11 | −11 | | +11 | V |
| | | −40°C ≤ $T_A$ ≤ +125°C | −10.5 | | +10.5 | −10.5 | | +10.5 | V |
| Common-Mode Rejection Ratio | CMRR | $T_A$ = 25°C, $V_{CM}$ = −11 V to +11 V | 106 | 116 | | 100 | 110 | | dB |
| | | −40°C ≤ $T_A$ ≤ +125°C, $V_{CM}$ = −10.5 V to +10.5 V | 98 | | | 97 | | | dB |
| Large Signal Voltage Gain | $A_{VO}$ | $R_L$ = 1 kΩ, $V_O$ = −10 V to +10 V | 112 | 120 | | 106 | 120 | | dB |
| | | −40 ≤ $T_A$ ≤ +85°C | 110 | | | 104 | | | dB |
| | | −40 ≤ $T_A$ ≤ +125°C | 102 | | | 100 | | | dB |
| DYNAMIC PERFORMANCE | | | | | | | | | |
| Slew Rate ADA4627-1 | SR | ±10 V step, $R_L$ = 1 kΩ, $C_L$ = 100 pF, $A_V$ = +1 | 40 | 56/78[3] | | 40 | 56/78[3] | | V/µs |
| | SR | ±10 V step, $R_L$ = 1 kΩ, $C_L$ = 100 pF, $R_s$ = $R_f$ = 1 kΩ, $A_V$ = −1 | 40 | 82/84[3] | | 40 | 82/84[3] | | V/µs |
| Slew Rate ADA4637-1 | SR | ±10 V out, $C_f$ = 4.8 pF, $A_V$ = −4 | | 170 | | | 170 | | V/µs |
| | SR | ±10 V out, $C_f$ = 4.8 pF, $A_V$ = +5 | | 170 | | | 170 | | V/µs |

| Parameter | Symbol | Test Conditions/Comments | B Grade Min | B Grade Typ | B Grade Max | A Grade Min | A Grade Typ | A Grade Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Settling Time to 0.01% | $t_S$ | | | | | | | | |
| ADA4627-1 | | $V_{IN}$ = 10 V step, $C_L$ = 35 pF, $R_L$ = +1 kΩ, $A_V$ = −1 | | 550 | | | 550 | | ns |
| ADA4637-1 | | $V_{IN}$ = 10 V step, $C_L$ = 35 pF, $R_L$ = +1 kΩ, $A_V$ = −4 | | 300 | | | 300 | | ns |
| Settling Time to 0.1% | $t_S$ | | | | | | | | |
| ADA4627-1 | | $V_{IN}$ = 10 V step, $C_L$ = 35 pF, $R_L$ = +1 kΩ, $A_V$ = −1 | | 450 | | | 450 | | ns |
| ADA4637-1 | | $V_{OUT}$ = 10 V step, $C_L$ = 35 pF, $R_L$ = +1 kΩ, $A_V$ = −4 | | 200 | | | 200 | | ns |
| Gain Bandwidth Product | GBP | | | | | | | | |
| ADA4627-1 | | $R_L$ = 1 kΩ, $C_L$ = 20 pF, $A_V$ = 1 | 16[4] | 19 | | 16[4] | 19 | | MHz |
| ADA4637-1 | | $A_V$ = 10 | | 79.9 | | | 79.9 | | |
| Phase Margin | $Φ_M$ | | | | | | | | |
| ADA4627-1 | | $R_L$ = 1 kΩ, $C_L$ = 20 pF, $A_V$ = 1 | | 72 | | | 72 | | Degrees |
| ADA4637-1 | | $A_V$ = 10 | | 85 | | | 85 | | |
| Total Harmonic Distortion + Noise | THD + N | $V_{IN}$ = 6 V rms, f = 1 kHz, $A_V$ = 1, ADA4627-1 | | 0.000045 | | | 0.000045 | | % |
| POWER SUPPLY | | | | | | | | | |
| Supply Current per Amplifier | $I_{SY}$ | $I_O$ = 0 mA | | ±7.0 | ±7.5 | | ±7.0 | ±7.5 | mA |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | ±7.8 | | | ±7.8 | mA |
| OUTPUT CHARACTERISTICS | | | | | | | | | |
| Output Voltage High | $V_{OH}$ | $R_L$ = 1 kΩ to $V_{CM}$ | 12.0 | 12.3 | | 12.0 | 12.3 | | V |
| | | −40°C ≤ $T_A$ ≤ +85°C | 11.8 | | | 11.8 | | | V |
| | | −40°C ≤ $T_A$ ≤ +125°C | 11.7 | | | 11.7 | | | V |
| Output Voltage Low | $V_{OL}$ | $R_L$ = 1 kΩ to $V_{CM}$ | | −12.7 | −12.3 | | −12.7 | −12.3 | V |
| | | −40°C ≤ $T_A$ ≤ +85°C | | | −12.1 | | | −12.1 | V |
| | | −40°C ≤ $T_A$ ≤ +125°C | | | −12.0 | | | −12.0 | V |
| Output Current | $I_{OUT}$ | $V_O$ = ±10 V | | ±45 | | | ±45 | | mA |
| Short-Circuit Current | $I_{SC}$ | $T_A$ = 25°C | | +70/−55 | | | +70/−55 | | mA |
| Closed-Loop Output Impedance | $Z_{OUT}$ | f = 1 MHz, $A_V$ = −100 | | 41 | | | 41 | | Ω |

[1] $V_{OS}$ is measured fully warmed up.
[2] Tested/extrapolated from 125°C.
[3] Rising/falling.
[4] Not tested. Guaranteed by simulation and characterization.

# ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter | Rating |
|---|---|
| Supply Voltage | 36 V |
| Input Voltage Range[1] | (V−) − 0.3 V to (V+) + 0.3 V |
| Input Current[1] | ±10 mA |
| Differential Input Voltage[2] | $\pm V_{SY}$ |
| Output Short-Circuit Duration to GND | Indefinite |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range | −40°C to +125°C |
| Junction Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 60 sec) | 300°C |
| ESD Human Body Model | 4 kV |

[1] Input pin has clamp diodes to the power supply pins. Input current should be limited to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.
[2] Differential input voltage is limited to ±30 V or the supply voltage, whichever is less.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

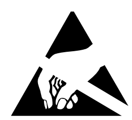
## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. This was measured using a standard 2-layer board. For the LFCSP package, the exposed pad should be soldered to a copper plane.

Table 4. Thermal Resistance

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 8-Lead SOIC_N (R-8) | 155 | 45 | °C/W |
| 8-Lead LFCSP (CP-8-2) | 77 | 14 | °C/W |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, unless otherwise noted.

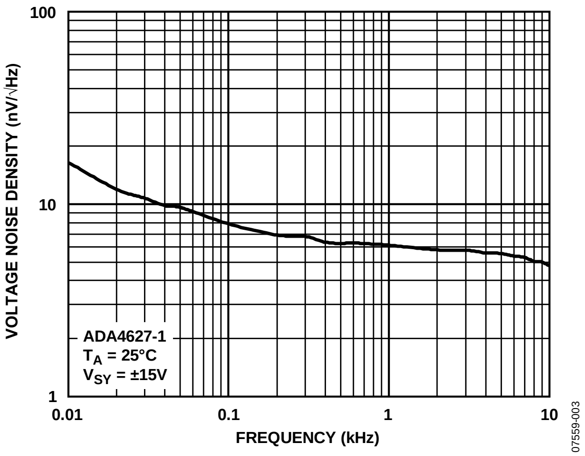



Figure 4. Voltage Noise Density vs. Frequency

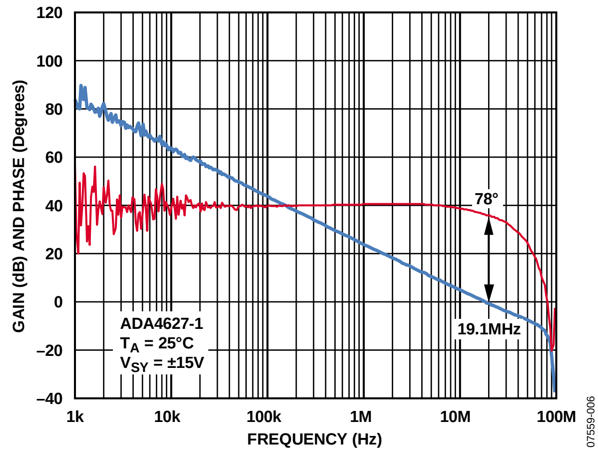



Figure 7. Open-Loop Gain and Phase vs. Frequency

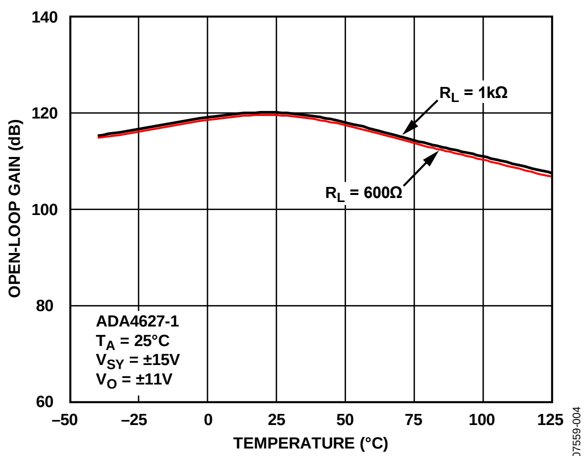



Figure 5. Open-Loop Gain vs. Temperature

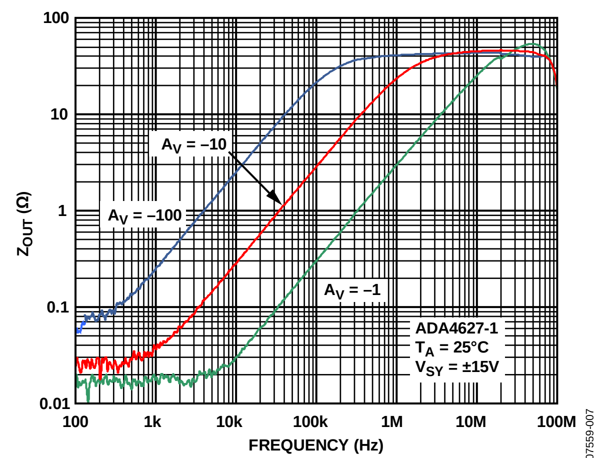



Figure 8. Closed-Loop $Z_{OUT}$ vs. Frequency

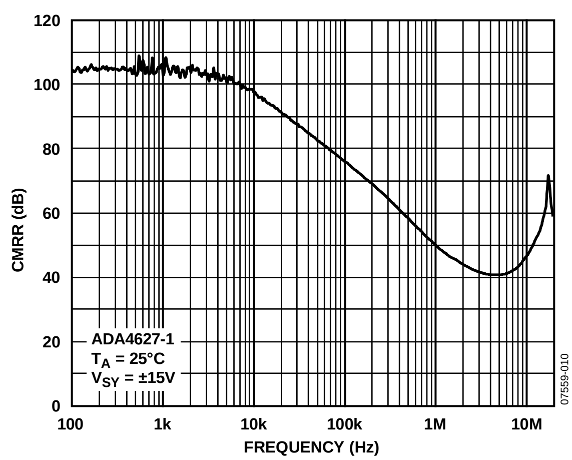



Figure 6. CMRR vs. Frequency

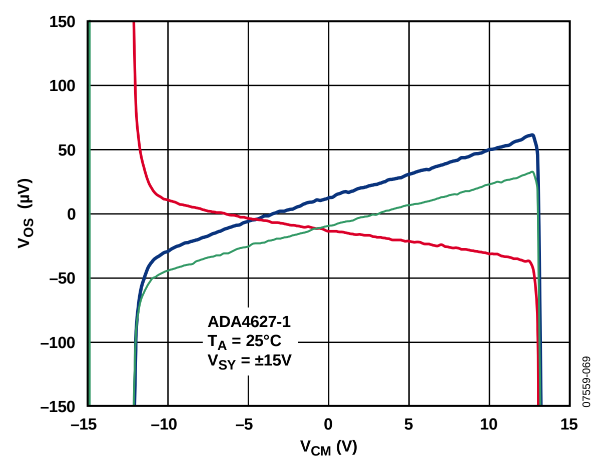



Figure 9. $V_{OS}$ vs. Common-Mode Voltage

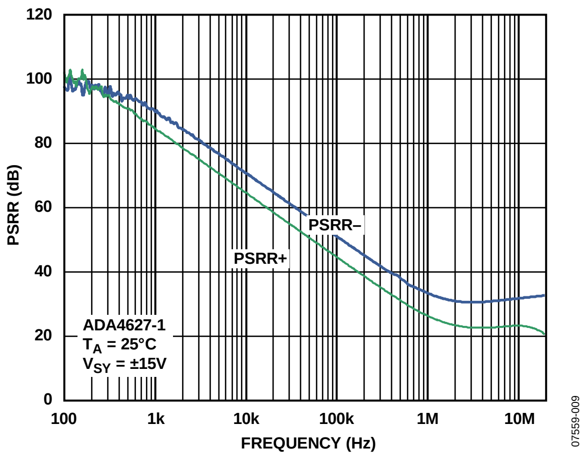


Figure 10. PSRR vs. Frequency

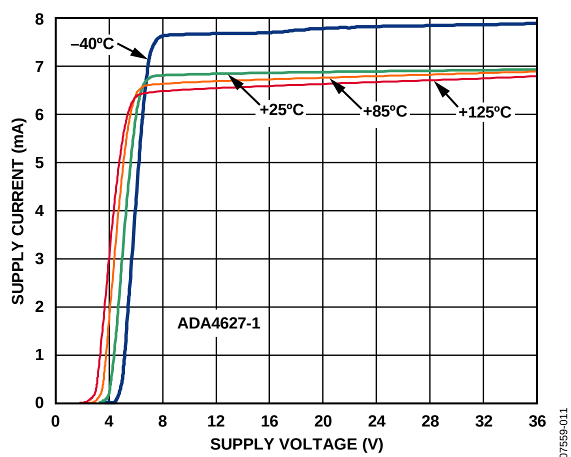


Figure 11. Supply Current vs. Supply Voltage and Temperature

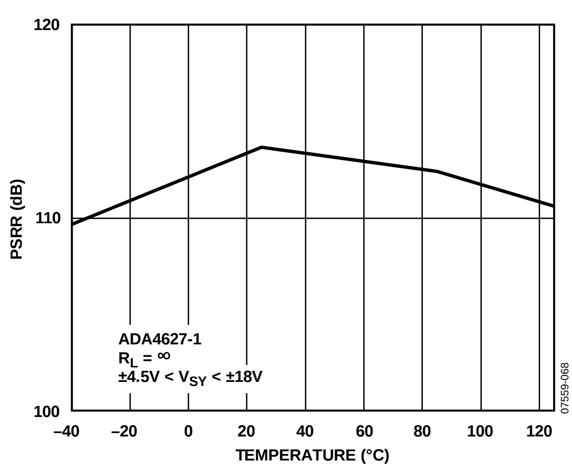


Figure 12. PSRR vs. Temperature

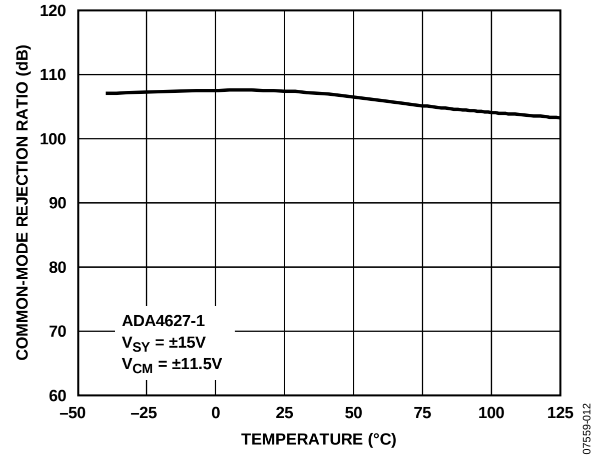


Figure 13. CMRR vs. Temperature

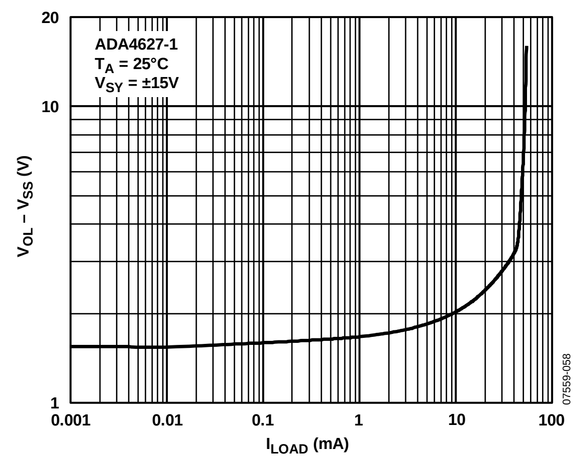


Figure 14. $V_{OUT}$ Sinking vs. $I_{LOAD}$ Current

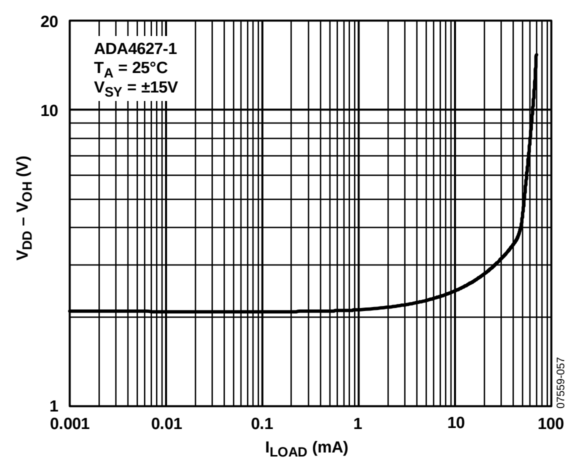


Figure 15. $V_{OUT}$ Sourcing vs. $I_{LOAD}$ Current

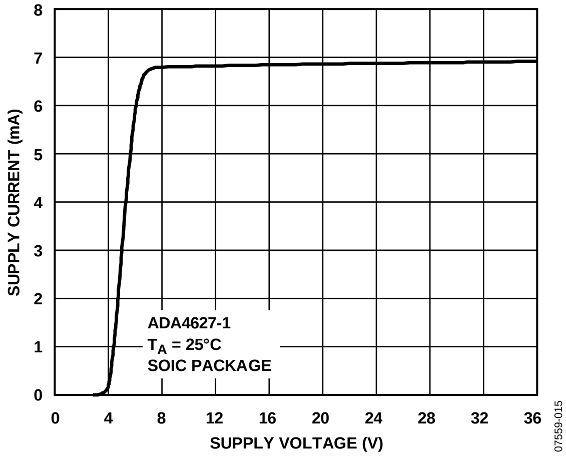



*Figure 16. Supply Current vs. Supply Voltage*

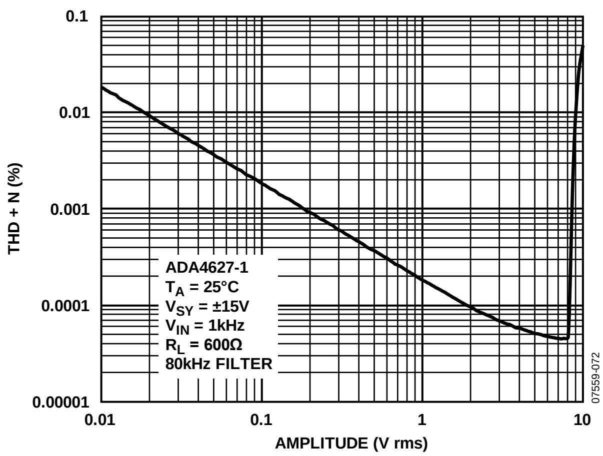



*Figure 17. THD + N vs. $V_{IN}$*

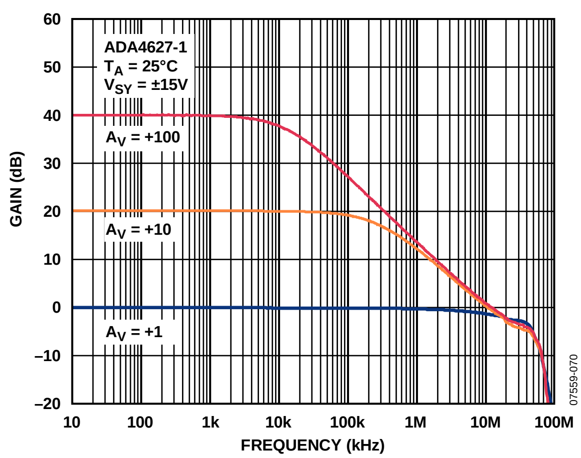



*Figure 18. Closed-Loop Gain vs. Frequency*

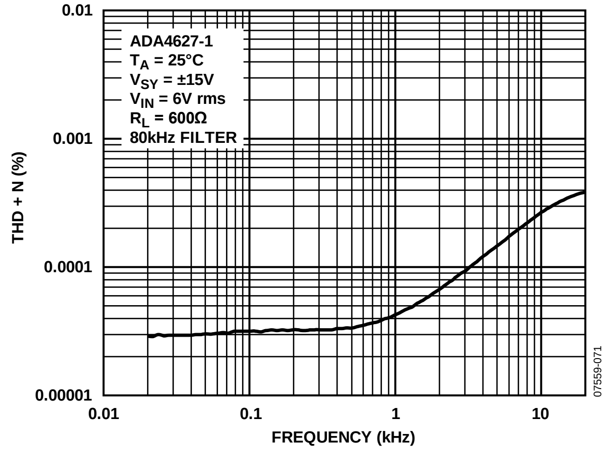



*Figure 19. THD + N vs. Frequency*

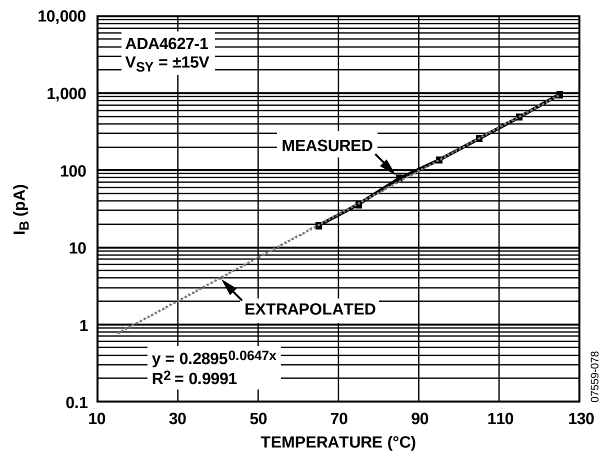



*Figure 20. Input Bias Current vs. Temperature*

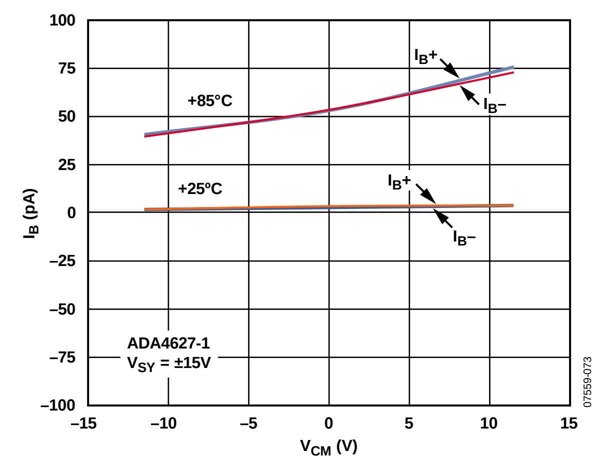



*Figure 21. Input Bias Current vs. $V_{CM}$ and Temperature*

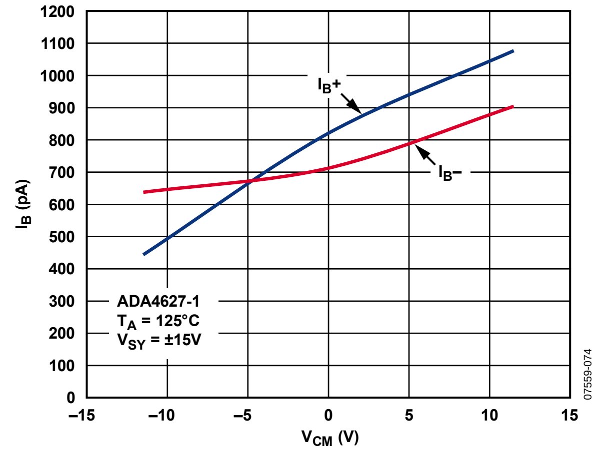



Figure 22. Input Bias Current vs. $V_{CM}$ at 125°C

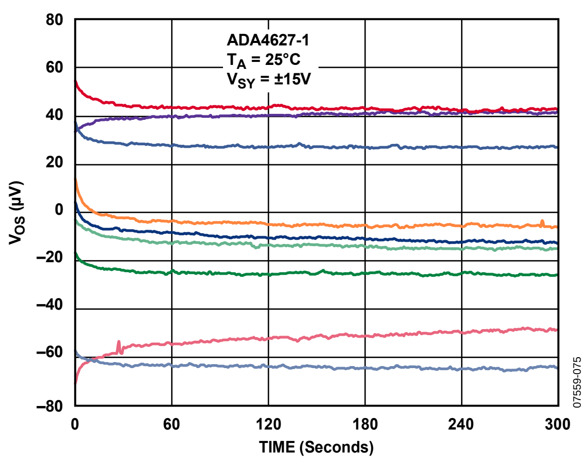



Figure 23. Input Offset Voltage vs. Time

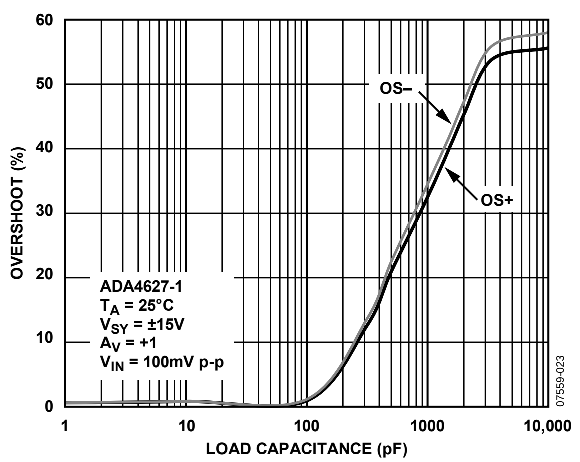



Figure 24. Small Signal Overshoot vs. Load Capacitance

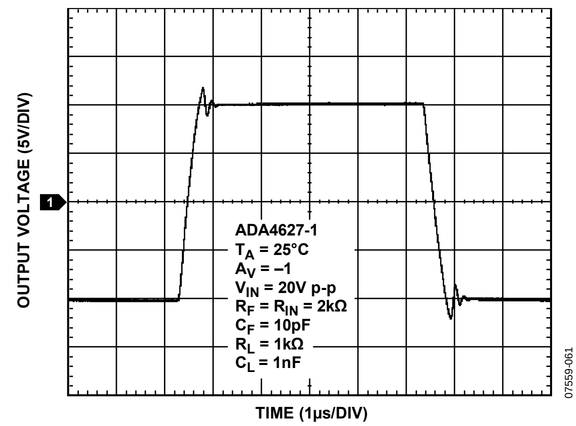



Figure 25. Large Signal Transient Response

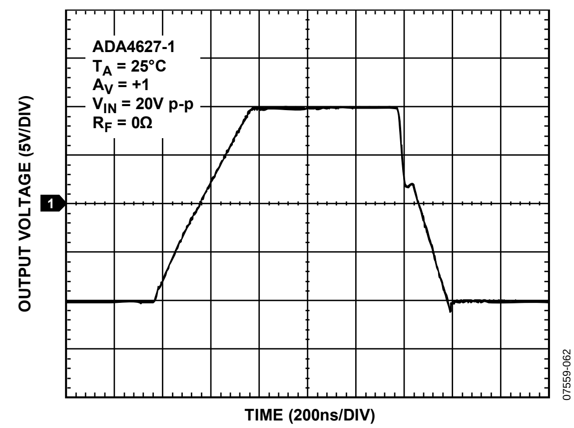



Figure 26. Large Signal Transient Response

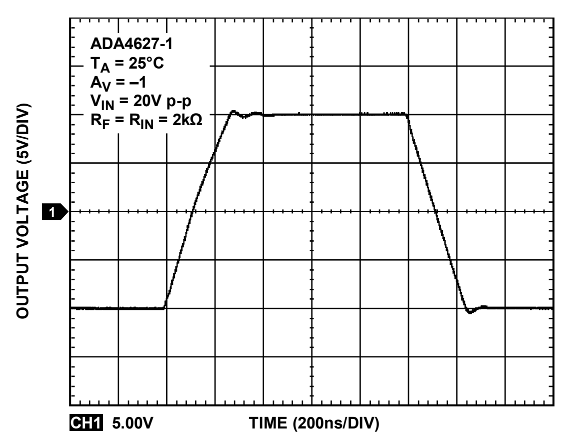



Figure 27. Large Signal Transient Response

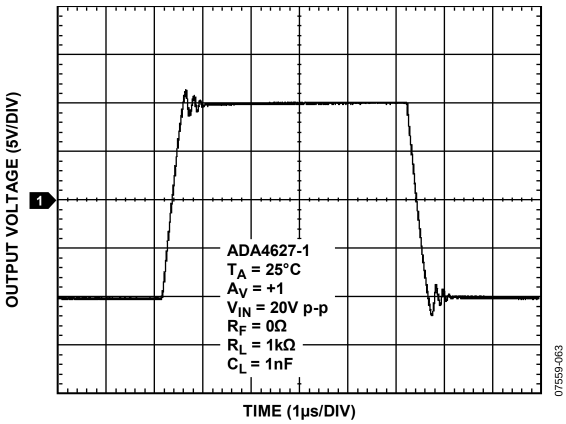



*Figure 28. Large Signal Transient Response*

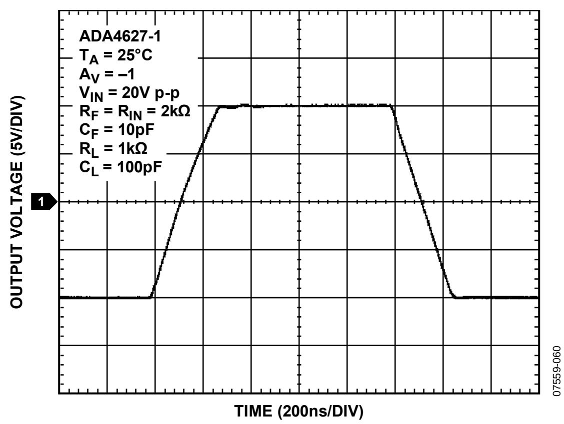



*Figure 29. Large Signal Transient Response*

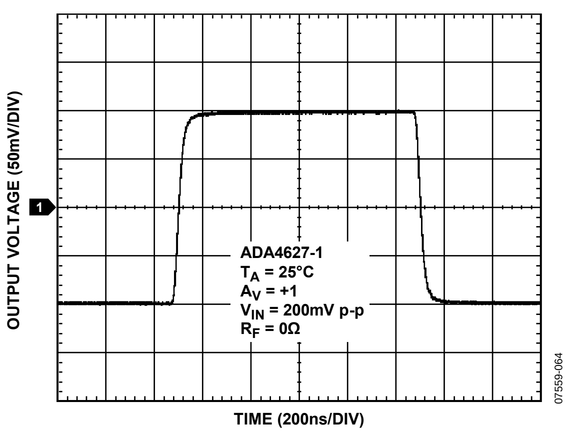



*Figure 30. Small Signal Transient Response*

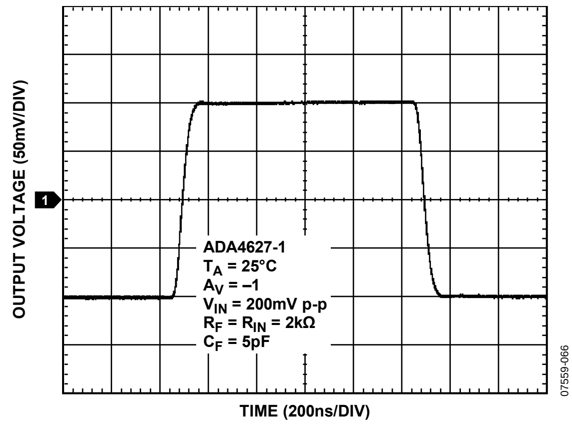



*Figure 31. Small Signal Transient Response*

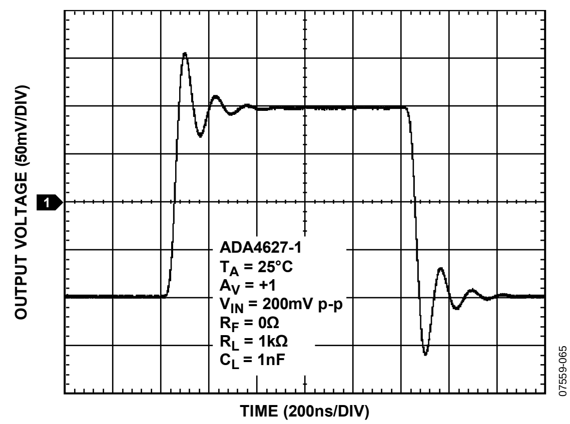



*Figure 32. Small Signal Transient Response*

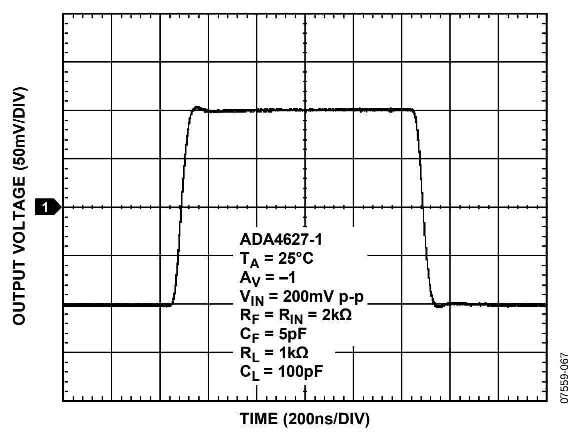



*Figure 33. Small Signal Transient Response*

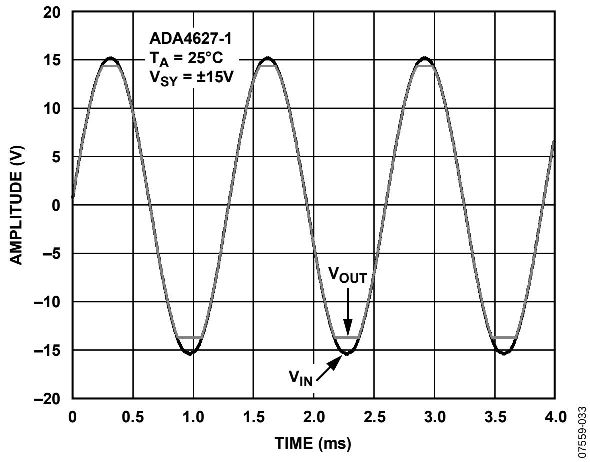



Figure 34. No Phase Reversal

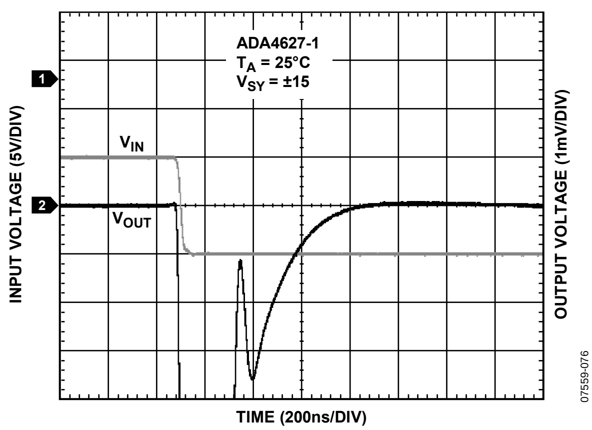



Figure 35. Negative Settling Time to 0.01%

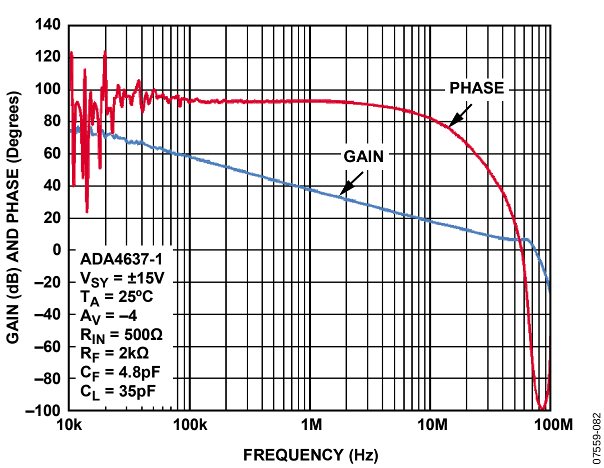



Figure 36. Open-Loop Gain and Phase vs. Frequency

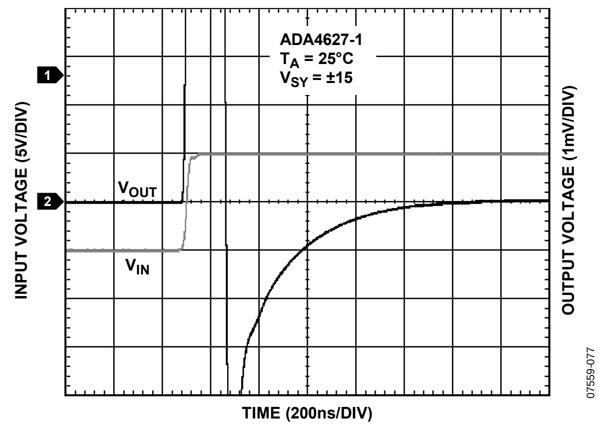



Figure 37. Positive Settling Time to 0.01%

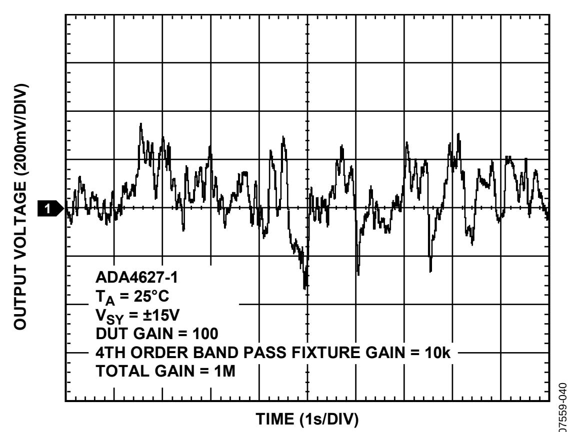



Figure 38. 0.1 Hz to 10 Hz Noise

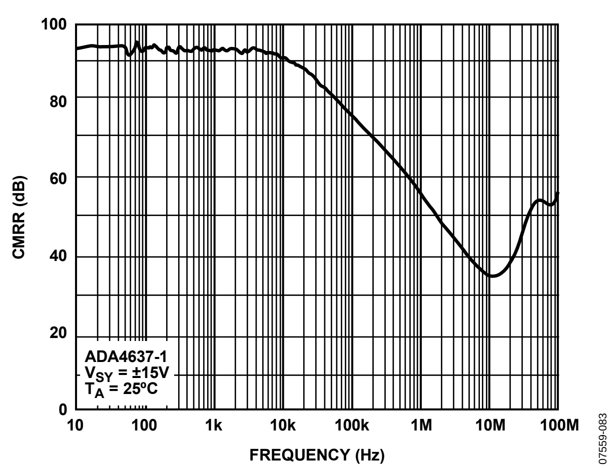



Figure 39. CMRR vs. Frequency

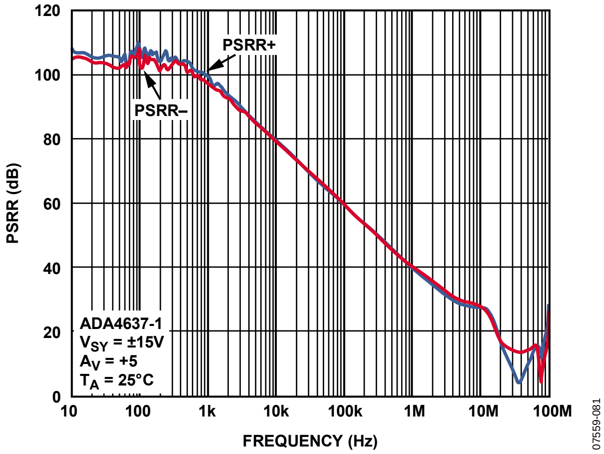



Figure 40. PSRR vs. Frequency

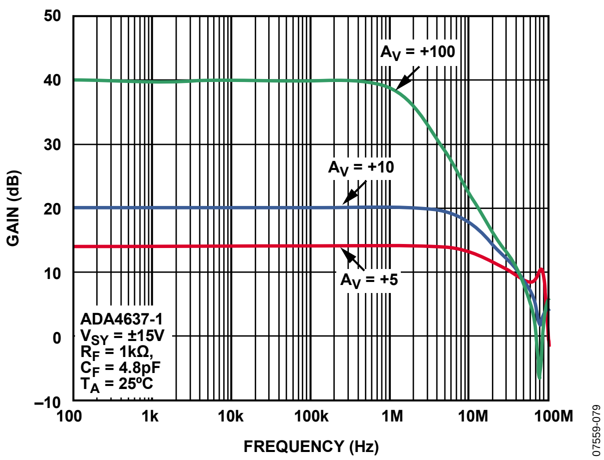



Figure 41. Closed-Loop Gain vs. Frequency

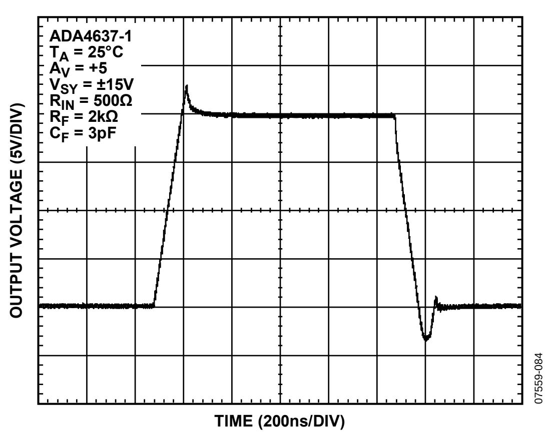



Figure 42. Large Signal Transient Response

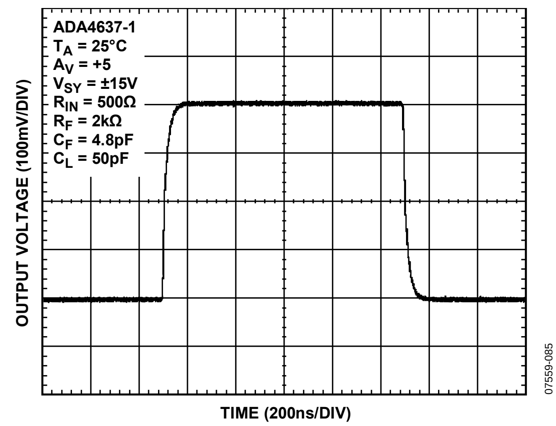



Figure 43. Small Signal Transient Response

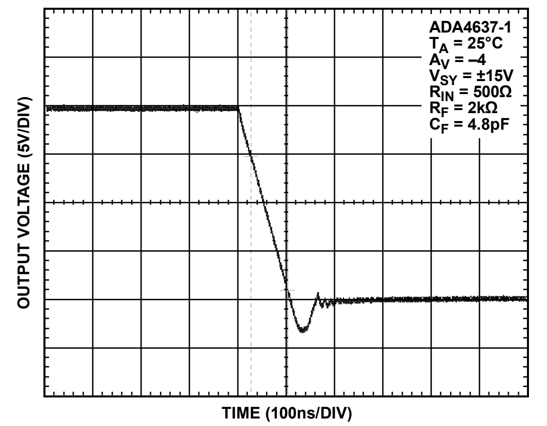



Figure 44. Slew Rate Falling

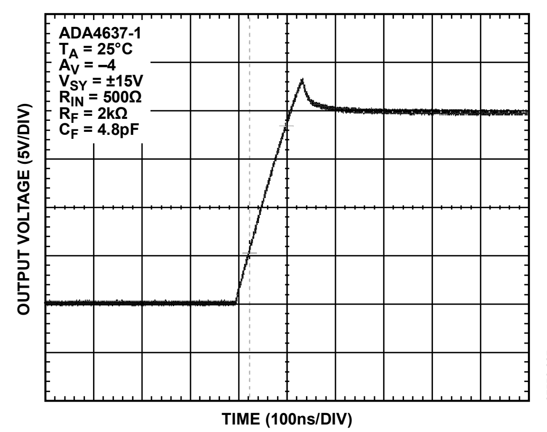



Figure 45. Slew Rate Rising

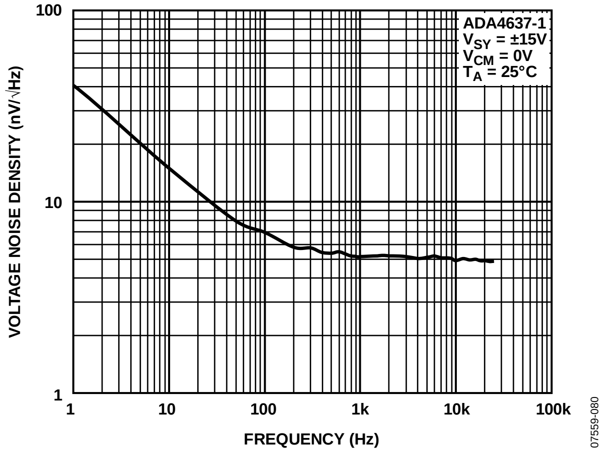


Figure 46. Voltage Noise Density vs. Frequency

# THEORY OF OPERATION

The ADA4627-1 is a high speed, unity gain stable amplifier with excellent dc characteristics. The ADA4637-1 is a decompensated version that is stable at a gain of 5 or greater. The typical offset voltage of 70 µV allows the amplifiers to be easily configured for high gains without the risk of excessive output voltage errors. The small temperature drift of 2 µV/°C ensures a minimum offset voltage error over the entire temperature range of −40°C to +125°C, making the amplifiers ideal for a variety of sensitive measurement applications in harsh operating environments.

## INPUT VOLTAGE RANGE

The ADA4627-1/ADA4637-1 are not rail-to-rail input amplifiers; therefore, care is required to ensure that both inputs do not exceed the input voltage range. Under normal negative feedback operating conditions, the amplifier corrects its output to ensure that the two inputs are at the same voltage. However, if either input exceeds the input voltage range, the loop opens, and large currents begin to flow through the ESD protection diodes in the amplifier.

These diodes are connected between the inputs and each supply rail to protect the input transistors against an electrostatic discharge event, and they are normally reverse-biased. However, if the input voltage exceeds the supply voltage, these ESD diodes can become forward-biased. Without current limiting, excessive amounts of current can flow through these diodes, causing permanent damage to the device. If inputs are subject to overvoltage, insert appropriate series resistors to limit the diode current to less than 5 mA.

## INPUT OFFSET VOLTAGE ADJUST RANGE

The ADA4627-1/ADA4637-1 SOIC packages have offset adjust pins for compatibility with some existing designs. The recommended offset nulling circuit is shown in Figure 47.

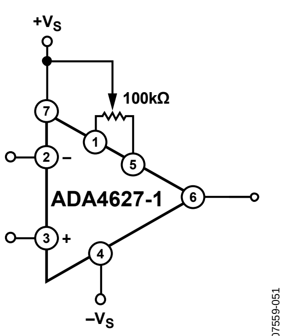



*Figure 47. Standard Offset Null Circuit*

With a 100 kΩ potentiometer, the adjustment range is more than ±11 mV. However, the $V_{OS}$ temperature drift increases by several µV/°C for every millivolt of offset adjust. The ADA4627-1/ADA4637-1 have matching thin film resistors that are laser trimmed at two temperatures to minimize both offset voltage and offset voltage drift. The offset voltage at room temperature is less than 0.5 mV, and the offset voltage drift is only a few µV/°C or less; therefore, it is not recommended to use the offset adjust pins, especially for offset adjust of a complete signal chain. Signal chain offset can be addressed with an auto-zero amplifier used to form a composite amplifier; or, if the ADA4627-1 or the ADA4637-1 is in an inverting amplifier stage, it can be modified easily to add a potentiometer (see Figure 48). The LFCSP package does not have offset adjust pins.

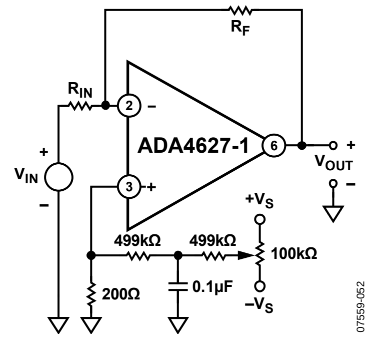



*Figure 48. Alternate Offset Null Circuit for Inverting Stage*

## INPUT BIAS CURRENT

Because the ADA4627-1/ADA4637-1 have a JFET input stage, the input bias current, due to the reverse-biased junction, has a leakage current that approximately doubles every 10°C. The power dissipation of the device, combined with the thermal resistance of the package, results in the junction temperature increasing 20°C to 30°C above ambient. This parameter is tested with high speed ATE equipment, which does not result in the die temperature reaching equilibrium. This is correlated with bench measurements to match the guaranteed maximum at room temperature shown in Table 2.

The input current can be reduced by keeping the temperature as low as possible and using a light load on the output.

## NOISE CONSIDERATIONS

The JFET input stage offers very low input voltage noise and input current noise. The thermal noise of a 1 kΩ resistor at room temperature is 4 nV/√Hz; therefore, low values of resistance should be used for dc-coupled inverting and noninverting amplifier configurations. In the case of transimpedance amplifiers (TIAs), current noise is more important.

The ADA4627-1/ADA4637-1 are an excellent choice for both of these applications. Analog Devices offers a wide variety of low voltage noise and low current noise op amps in a variety of processes that are optimized for different supply voltage ranges. Refer to Application Note AN-940 for a discussion of noise, calculations, and selection tables for more than three dozen low noise, op amp families.

### THD + N MEASUREMENTS

Total harmonic distortion plus noise (THD + N) is usually measured with an audio analyzer, such as those from Audio Precision, Inc™. The analyzer consists of a low distortion oscillator that is swept from the starting frequency to the ending frequency. The oscillator is connected to the circuit under test, and the output of the circuit goes back to the analyzer.

The analyzer has a tunable notch filter in lock step with the swept oscillator. This removes the fundamental frequency but allows all of the harmonics and wideband noise to be measured with an integrating voltmeter. However, there is a switchable low-pass filter in series with the notch filter. If the sine wave is at 100 Hz, then the tenth harmonic is still at 1 kHz; therefore, having a low pass at 80 kHz is not a problem. When the oscillator reaches 20 kHz, the fourth harmonic (80 kHz) is partially attenuated, resulting in a lower reading from the voltmeter. When evaluating THD + N curves from any manufacturer, careful attention should be paid to the test conditions. The difference between an 80 kHz low-pass filter and a 500 kHz filter is shown in Figure 49.

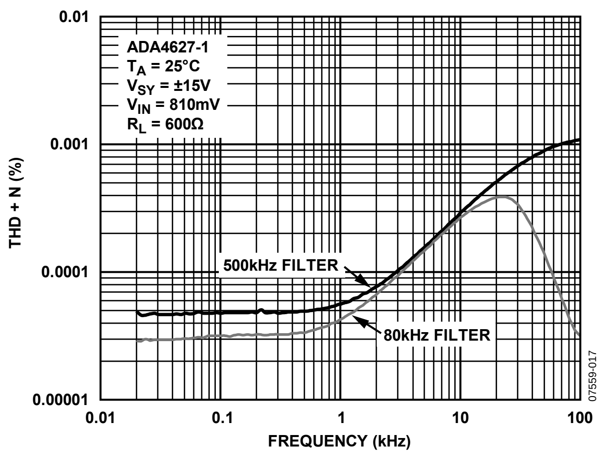



*Figure 49. THD + N vs. Frequency*

### PRINTED CIRCUIT BOARD LAYOUT, BIAS CURRENT, AND BYPASSING

To take advantage of the very low input bias current of the ADA4627-1/ADA4637-1 at room temperature, leakage paths must be considered. A printed circuit board (PCB), with dust and humidity, can have 100 MΩ of resistance over a few tenths of an inch. A 1 mV differential between the two points results in 10 pA of leakage current, more than the guaranteed maximum.

The op amp inputs should be guarded by surrounding the nets with a metal trace maintained at the predicted voltage. In the case of an inverting configuration or transimpedance amplifier, (see Figure 50), the inverting and noninverting nodes can be surrounded by traces held at a quiet analog ground.

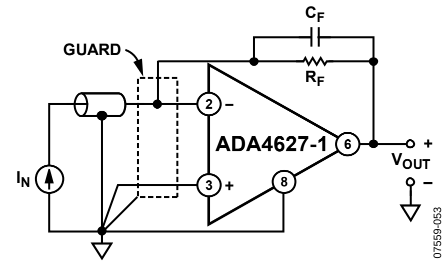



*Figure 50. Inverting Amplifier with Guard*

For a noninverting configuration, the trace can be driven from the feedback divider, but the resistors should be chosen to offer a low impedance drive to the trace (see Figure 51).

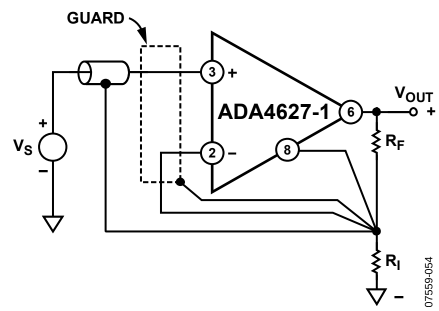



*Figure 51. Noninverting Amplifier with Guard*

The board layout should be compact with traces as short as possible. For second-order board considerations, such as triboelectric effects and piezoelectric effects, as well as a table of insulating material properties, see the AD549 data sheet.

In some cases, shielding from air currents may be helpful. A general rule of thumb, for op amps with gain bandwidth products higher than 1 MHz, bypass capacitors should be very close to the device, within 3 mm. Each supply should be bypassed with a 0.01 µF ceramic capacitor in parallel with a 1 µF bulk decoupling capacitor. The ceramic capacitors should be closer to the op amp. Sockets, which add inductance and capacitance, should not be used.

### OUTPUT PHASE REVERSAL

Output phase reversal occurs in some amplifiers when the input common-mode voltage range is exceeded. As common-mode voltage is moved outside the common-mode range, the outputs of these amplifiers can suddenly jump in the opposite direction to the supply rail. This is the result of the differential input pair shutting down, causing a radical shifting of internal voltages that results in the erratic output behavior.

The ADA4627-1/ADA4637-1 amplifiers are carefully designed to prevent any output phase reversal if both inputs are maintained within or slightly above the power supply rails. The ADA4627-1/ADA4637-1 do not phase reverse, as shown in Figure 34.

## DECOMPENSATED OP AMPS

The ADA4637-1 is a decompensated op amp, and, as such, must always be operated at a noise gain of 5 or greater. See tutorial MT-033, *Voltage Feedback Op Amp Gain and Bandwidth*, at www.analog.com for more information.

## DRIVING CAPACITIVE LOADS

Adding capacitance to the output of any op amp results in additional phase shift, which reduces stability and leads to overshoot or oscillation.

The ADA4627-1/ADA4637-1 have a high phase margin and low output impedance, so they can drive reasonable values of capacitance. This is a common situation when an amplifier is used to drive the input of switched capacitor ADCs. For other considerations and various circuit solutions, see the Analog Dialogue article titled *Ask the Applications Engineer-25, Op Amps Driving Capacitive Loads*.

## OUTLINE DIMENSIONS

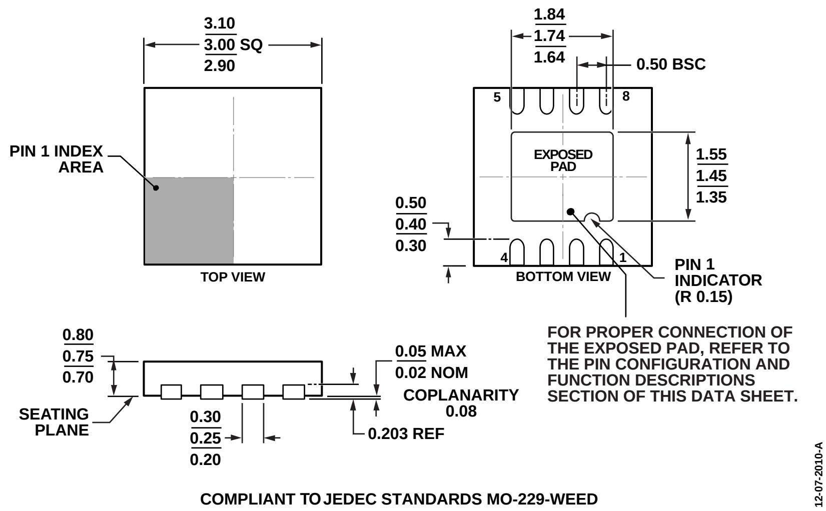



*Figure 52. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]*
*3 mm × 3 mm Body, Very Very Thin, Dual Lead*
*(CP-8-13)*
*Dimensions shown in millimeters*

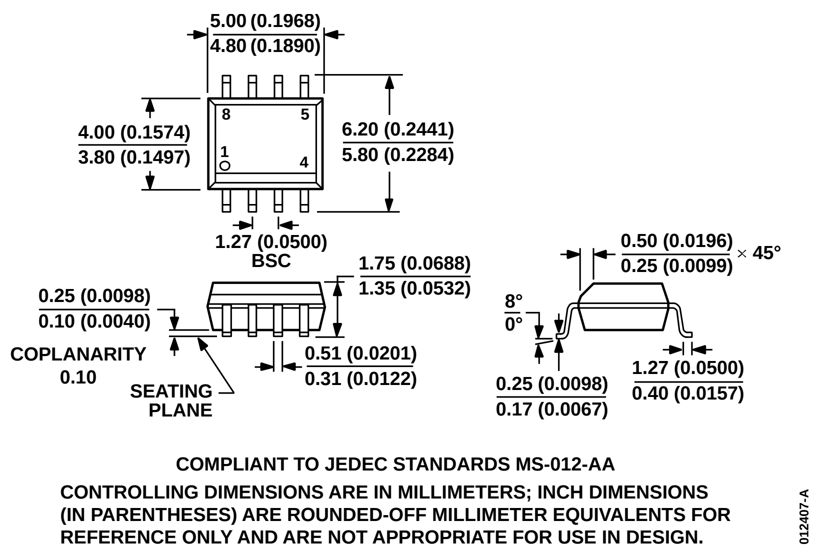



*Figure 53. 8-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body*
*(R-8)*
*Dimensions shown in millimeters and (inches)*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|
| ADA4627-1ACPZ-R2 | −40°C to +125°C | 8-Lead LFCSP_WD | CP-8-13 | A29 |
| ADA4627-1ACPZ-RL | −40°C to +125°C | 8-Lead LFCSP_WD | CP-8-13 | A29 |
| ADA4627-1ACPZ-R7 | −40°C to +125°C | 8-Lead LFCSP_WD | CP-8-13 | A29 |
| ADA4627-1ARZ | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADA4627-1ARZ-RL | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADA4627-1ARZ-R7 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADA4627-1BRZ | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADA4627-1BRZ-R7 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADA4627-1BRZ-RL | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADA4637-1ACPZ-R2 | −40°C to +125°C | 8-Lead LFCSP_WD | CP-8-13 | A2S |
| ADA4637-1ACPZ-RL | −40°C to +125°C | 8-Lead LFCSP_WD | CP-8-13 | A2S |
| ADA4637-1ACPZ-R7 | −40°C to +125°C | 8-Lead LFCSP_WD | CP-8-13 | A2S |
| ADA4637-1ARZ | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADA4637-1ARZ-RL | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADA4637-1ARZ-R7 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADA4637-1BRZ | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADA4637-1BRZ-R7 | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |
| ADA4637-1BRZ-RL | −40°C to +125°C | 8-Lead SOIC_N | R-8 | |

[1] Z = RoHS Compliant Part.

## NOTES

## NOTES