Low Power, Selectable Gain Differential ADC Driver, G = 1, 2, 3

Data Sheet

ADA4950-1/ADA4950-2

FEATURES

- High performance at low power
- High speed
  - −3 dB bandwidth of 750 MHz, G = 1
  - 0.1 dB flatness to 210 MHz, $V_{OUT, dm}$ = 2 V p-p, $R_{L, dm}$ = 200 Ω
  - Slew rate: 2900 V/µs, 25% to 75%
  - Fast 0.1% settling time of 9 ns
- Low power: 9.5 mA per amplifier
- Low harmonic distortion
  - 108 dB SFDR @ 10 MHz
  - 98 dB SFDR @ 20 MHz
- Low output voltage noise: 9.2 nV/√Hz, G = 1, RTO
- ±0.2 mV typical input offset voltage
- Selectable differential gains of 1, 2, and 3
- Differential-to-differential or single-ended-to-differential operation
- Adjustable output common-mode voltage
- Input common-mode range shifted down by 1 V_{BE}
- Wide supply range: +3 V to ±5 V
- Available in 16-lead and 24-lead LFCSP packages

APPLICATIONS

- ADC drivers
- Single-ended-to-differential converters
- IF and baseband gain blocks
- Differential buffers
- Line drivers

GENERAL DESCRIPTION

The ADA4950-1/ADA4950-2 are gain-selectable versions of the ADA4932-1/ADA4932-2 with on-chip feedback and gain resistors. They are ideal choices for driving high performance ADCs as single-ended-to-differential or differential-to-differential amplifiers. The output common-mode voltage is user adjustable by means of an internal common-mode feedback loop, allowing the ADA4950-1/ADA4950-2 output to match the input of the ADC. The internal feedback loop also provides exceptional output balance as well as suppression of even-order harmonic distortion products.

Differential gain configurations of 1, 2, and 3 are easily realized with internal feedback networks that are connected externally to set the closed-loop gain of the amplifier.

The ADA4950-1/ADA4950-2 are fabricated using the Analog Devices, Inc., proprietary silicon-germanium (SiGe) complementary bipolar process, enabling them to achieve low levels of distortion and noise at low power consumption. The low offset and excellent dynamic performance of the ADA4950-x make it well suited for a wide variety of data acquisition and signal processing applications.

FUNCTIONAL BLOCK DIAGRAMS

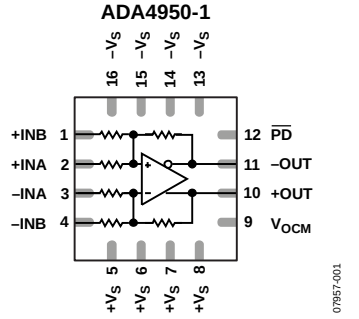

Figure 1. ADA4950-1

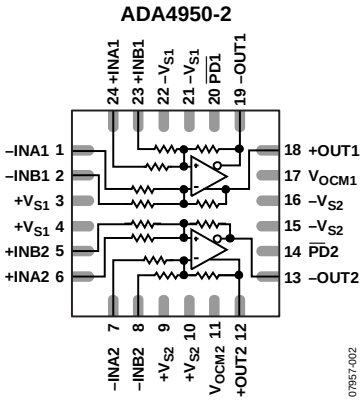

Figure 2. ADA4950-2

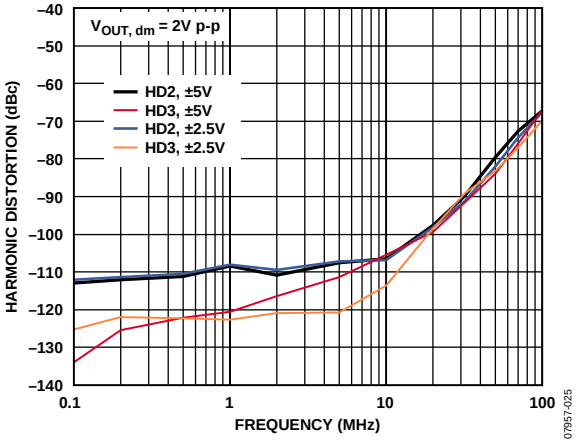

Figure 3. Harmonic Distortion vs. Frequency at Various Supplies

The devices are available in a Pb-free, 3 mm × 3 mm, 16-lead LFCSP (ADA4950-1, single) or a Pb-free, 4 mm × 4 mm, 24-lead LFCSP (ADA4950-2, dual). The pinout has been optimized to facilitate PCB layout and minimize distortion. The ADA4950-1/ADA4950-2 are specified to operate over the −40°C to +105°C temperature range; both operate on supplies from +3 V to ±5 V.

Rev. B Document Feedback

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REVISION HISTORY

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Changed CP-16-2 to CP-16-21 ... Universal
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Updated Outline Dimensions ... 25
Changes to Ordering Guide ... 25

3/13—Rev. 0 to Rev. A

Updated Outline Dimensions ... 25
Changes to Ordering Guide ... 25

5/09—Revision 0: Initial Version

SPECIFICATIONS

±5 V OPERATION

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = −5 V, V_{OCM} = 0 V, G = 1, R_T = 53.6 Ω (when used), $R_{L, dm}$ = 1 kΩ, unless otherwise noted. All specifications refer to single-ended input and differential outputs, unless otherwise noted. Refer to Figure 52 for signal definitions.

Differential Inputs to $V_{OUT, dm}$ Performance

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small-Signal Bandwidth	$V_{OUT, dm}$ = 0.1 V p-p		750		MHz
−3 dB Large-Signal Bandwidth	$V_{OUT, dm}$ = 2.0 V p-p		350		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT, dm}$ = 2.0 V p-p, R_L = 200 Ω				
ADA4950-1			210		MHz
ADA4950-2			230		MHz
Slew Rate	$V_{OUT, dm}$ = 2 V p-p, 25% to 75%		2900		V/µs
Settling Time to 0.1%	$V_{OUT, dm}$ = 2 V step		9		ns
Overdrive Recovery Time	V_{IN} = 0 V to 5 V ramp, G = 2		20		ns
NOISE/HARMONIC PERFORMANCE	See Figure 51 for distortion test circuit				
Second Harmonic	$V_{OUT, dm}$ = 2 V p-p				
	1 MHz		−108		dBc
	10 MHz		−107		dBc
	20 MHz		−98		dBc
	50 MHz		−80		dBc
Third Harmonic	$V_{OUT, dm}$ = 2 V p-p				
	1 MHz		−126		dBc
	10 MHz		−105		dBc
	20 MHz		−99		dBc
	50 MHz		−84		dBc
IMD3	f_1 = 30 MHz, f_2 = 30.1 MHz, $V_{OUT, dm}$ = 2 V p-p		−94		dBc
Voltage Noise (Referred to Output)	f = 1 MHz				
	Gain = 1		9.2		nV/√Hz
	Gain = 2		12.5		nV/√Hz
	Gain = 3		16.6		nV/√Hz
Crosstalk (ADA4950-2)	f = 10 MHz; Channel 2 active, Channel 1 output		−87		dB
INPUT CHARACTERISTICS					
Offset Voltage (Referred to Input)	$V_{+DIN} = V_{-DIN} = V_{OCM}$ = 0 V	−2.5	±0.2	+2.5	mV
	T_{MIN} to T_{MAX} variation		−3.7		µV/°C
Input Capacitance	Single-ended at package pin		0.5		pF
Input Common-Mode Voltage Range	Directly at internal amplifier inputs, not external input terminals		$-V_S$ + 0.2 to $+V_S$ − 1.8		V
CMRR	DC, $\Delta V_{OUT, dm}/\Delta V_{IN, cm}$, $\Delta V_{IN, cm}$ = ±1 V		−64	−49	dB
Open-Loop Gain		64	66		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}, single-ended output, R_L = 1 kΩ	$-V_S$ + 1.4 to $+V_S$ − 1.4	$-V_S$ + 1.2 to $+V_S$ − 1.2		V
Linear Output Current	200 kHz, $R_{L, dm}$ = 10 Ω, SFDR = 69 dB		114		mA peak
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$, $\Delta V_{OUT, dm}$ = 2 V p-p, 1 MHz; see Figure 50 for output balance test circuit		−62		dB
Gain Error	Gain = 1		0.5	1.2	%
	Gain = 2		1.0	1.9	%
	Gain = 3		0.8	1.7	%

V_{OCM} to $V_{OUT, cm}$ Performance

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Small-Signal Bandwidth	$V_{OUT, cm}$ = 100 mV p-p		250		MHz
−3 dB Large-Signal Bandwidth	$V_{OUT, cm}$ = 2 V p-p		105		MHz
Slew Rate	V_{IN} = 1.5 V to 3.5 V, 25% to 75%		430		V/µs
Input Voltage Noise (Referred to Input)	f = 1 MHz		9.8		nV/√Hz
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range			$-V_S$ + 1.2 to $+V_S$ − 1.2		V
Input Resistance		22	26	32	kΩ
Input Offset Voltage	$V_{+DIN} = V_{-DIN}$ = 0 V	−6	+0.8	+6	mV
V_{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V		−60	−49	dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V	0.98	1.0	1.01	V/V

General Performance

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		3.0		11	V
Quiescent Current per Amplifier		8.8	9.5	10.1	mA
	T_{MIN} to T_{MAX} variation		31		µA/°C
	Powered down		0.7	1.0	mA
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$, ΔV_S = 1 V p-p		−96	−84	dB
POWER-DOWN ($\overline{PD}$)					
$\overline{PD}$ Input Voltage	Powered down		≤($+V_S$ − 2.5)		V
	Enabled		≥($+V_S$ − 1.8)		V
Turn-Off Time			600		ns
Turn-On Time			28		ns
$\overline{PD}$ Pin Bias Current per Amplifier					
Enabled	$\overline{PD}$ = 5 V	−1.0	+0.2	+1.0	µA
Disabled	$\overline{PD}$ = 0 V	−250	−180	−140	µA
OPERATING TEMPERATURE RANGE		−40		+105	°C

5 V OPERATION

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = 0 V, V_{OCM} = 2.5 V, G = 1, R_T = 53.6 Ω (when used), $R_{L, dm}$ = 1 kΩ, unless otherwise noted. All specifications refer to single-ended input and differential outputs, unless otherwise noted. Refer to Figure 52 for signal definitions.

Differential Inputs to $V_{OUT, dm}$ Performance

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small-Signal Bandwidth	$V_{OUT, dm}$ = 0.1 V p-p		770		MHz
−3 dB Large-Signal Bandwidth	$V_{OUT, dm}$ = 2.0 V p-p		320		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT, dm}$ = 2.0 V p-p, R_L = 200 Ω				
ADA4950-1			220		MHz
ADA4950-2			160		MHz
Slew Rate	$V_{OUT, dm}$ = 2 V p-p, 25% to 75%		2200		V/µs
Settling Time to 0.1%	$V_{OUT, dm}$ = 2 V step		10		ns
Overdrive Recovery Time	V_{IN} = 0 V to 2.5 V ramp, G = 2		19		ns
NOISE/HARMONIC PERFORMANCE	See Figure 51 for distortion test circuit				
Second Harmonic	$V_{OUT, dm}$ = 2 V p-p				
	1 MHz		−108		dBc
	10 MHz		−107		dBc
	20 MHz		−98		dBc
	50 MHz		−82		dBc
Third Harmonic	$V_{OUT, dm}$ = 2 V p-p				
	1 MHz		−124		dBc
	10 MHz		−114		dBc
	20 MHz		−99		dBc
	50 MHz		−83		dBc
IMD3	f_1 = 30 MHz, f_2 = 30.1 MHz, $V_{OUT, dm}$ = 2 V p-p		−94		dBc
Voltage Noise (Referred to Input)	f = 1 MHz				
	Gain = 1		9.2		nV/√Hz
	Gain = 2		12.5		nV/√Hz
	Gain = 3		16.6		nV/√Hz
Crosstalk (ADA4950-2)	f = 10 MHz; Channel 2 active, Channel 1 output		−87		dB
INPUT CHARACTERISTICS					
Offset Voltage (Referred to Input)	$V_{+DIN} = V_{-DIN} = V_{OCM}$ = 2.5 V	−4	±0.4	+4	mV
	T_{MIN} to T_{MAX} variation		−3.7		µV/°C
Input Capacitance	Single-ended at package pin		0.5		pF
Input Common-Mode Voltage Range	Directly at internal amplifier inputs, not external input terminals		$-V_S$ + 0.2 to $+V_S$ − 1.8		V
CMRR	DC, $\Delta V_{OUT, dm}/\Delta V_{IN, cm}$, $\Delta V_{IN, cm}$ = ±1 V		−64	−49	dB
Open-Loop Gain		64	66		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}, single-ended output, R_L = 1 kΩ	$-V_S$ + 1.2 to $+V_S$ − 1.2	$-V_S$ + 1.1 to $+V_S$ − 1.1		V
Linear Output Current	200 kHz, $R_{L, dm}$ = 10 Ω, SFDR = 67 dB		70		mA peak
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$, $\Delta V_{OUT, dm}$ = 1 V p-p, 1 MHz; see Figure 50 for output balance test circuit		−62		dB
Gain Error	Gain = 1		0.5	1.2	%
	Gain = 2		1.0	1.9	%
	Gain = 3		0.8	1.7	%

V_{OCM} to $V_{OUT, cm}$ Performance

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Small-Signal Bandwidth	$V_{OUT, cm}$ = 100 mV p-p		240		MHz
−3 dB Large-Signal Bandwidth	$V_{OUT, cm}$ = 2 V p-p		90		MHz
Slew Rate	V_{IN} = 1.5 V to 3.5 V, 25% to 75%		380		V/µs
Input Voltage Noise (Referred to Input)	f = 1 MHz		9.8		nV/√Hz
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range			$-V_S$ + 1.2 to $+V_S$ − 1.2		V
Input Resistance		22	26	32	kΩ
Input Offset Voltage	$V_{+DIN} = V_{-DIN}$ = 2.5 V	−6.5	+1.0	+6.5	mV
V_{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V		−60	−49	dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$, ΔV_{OCM} = ±1 V	0.98	1.0	1.01	V/V

General Performance

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		3.0		11	V
Quiescent Current per Amplifier		8.4	8.9	9.6	mA
	T_{MIN} to T_{MAX} variation		31		µA/°C
	Powered down		0.6	0.9	mA
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$, ΔV_S = 1 V p-p		−96	−84	dB
POWER-DOWN ($\overline{PD}$)					
$\overline{PD}$ Input Voltage	Powered down		≤($+V_S$ − 2.5)		V
	Enabled		≥($+V_S$ − 1.8)		V
Turn-Off Time			600		ns
Turn-On Time			29		ns
$\overline{PD}$ Pin Bias Current per Amplifier					
Enabled	$\overline{PD}$ = 5 V	−1.0	+0.2	+1.0	µA
Disabled	$\overline{PD}$ = 0 V	−100	−65	−40	µA
OPERATING TEMPERATURE RANGE		−40		+105	°C

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Supply Voltage	11 V
Power Dissipation	See Figure 4
Input Current, +INx, −INx, $\overline{PD}$	±5 mA
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	
ADA4950-1	−40°C to +105°C
ADA4950-2	−40°C to +105°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device (including exposed pad) soldered to a high thermal conductivity 2s2p printed circuit board, as described in EIA/JESD51-7.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
ADA4950-1, 16-Lead LFCSP (Exposed Pad)	91	28	°C/W
ADA4950-2, 24-Lead LFCSP (Exposed Pad)	65	16	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADA4950-x package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4950-x. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. The power dissipated due to the load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads/exposed pad from metal traces, through holes, ground, and power planes reduces θ_{JA}.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the single 16-lead LFCSP (91°C/W) and the dual 24-lead LFCSP (65°C/W) on a JEDEC standard 4-layer board with the exposed pad soldered to a PCB pad that is connected to a solid plane.

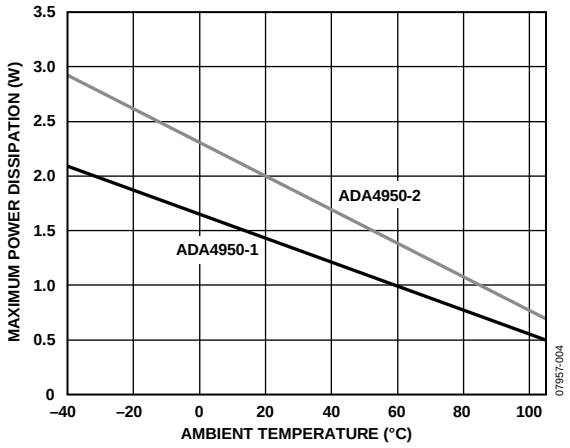

Figure 4. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

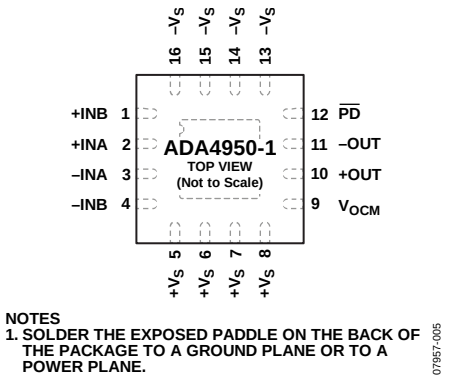

Figure 5. ADA4950-1 Pin Configuration

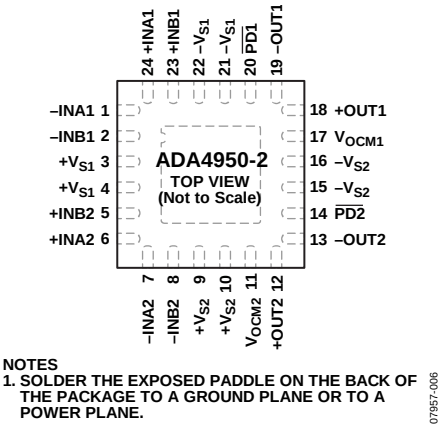

Figure 6. ADA4950-2 Pin Configuration

Table 9. ADA4950-1 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	+INB	Positive Input B, 250 Ω Input. Use alone for G = 2 or tie to +INA for G = 3.
2	+INA	Positive Input A, 500 Ω Input. Use alone for G = 1 or tie to +INB for G = 3.
3	−INA	Negative Input A, 500 Ω Input. Use alone for G = 1 or tie to −INB for G = 3.
4	−INB	Negative Input B, 250 Ω Input. Use alone for G = 2 or tie to −INA for G = 3.
5 to 8	$+V_S$	Positive Supply Voltage.
9	V_{OCM}	Output Common-Mode Voltage.
10	+OUT	Positive Output.
11	−OUT	Negative Output.
12	$\overline{PD}$	Power-Down Pin.
13 to 16	$-V_S$	Negative Supply Voltage.
17 (EPAD)	Exposed Paddle (EPAD)	Solder the exposed paddle on the back of the package to a ground plane or to a power plane.

Table 10. ADA4950-2 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−INA1	Negative Input A, Amplifier 1, 500 Ω Input. Use alone for G = 1 or tie to −INB1 for G = 3.
2	−INB1	Negative Input B, Amplifier 1, 250 Ω Input. Use alone for G = 2 or tie to −INA1 for G = 3.
3, 4	$+V_{S1}$	Positive Supply Voltage, Amplifier 1.
5	+INB2	Positive Input B, Amplifier 2, 250 Ω Input. Use alone for G = 2 or tie to +INA2 for G = 3.
6	+INA2	Positive Input A, Amplifier 2, 500 Ω Input. Use alone for G = 1 or tie to +INB2 for G = 3.
7	−INA2	Negative Input A, Amplifier 2, 500 Ω Input. Use alone for G = 1 or tie to −INB2 for G = 3.
8	−INB2	Negative Input B, Amplifier 2, 250 Ω Input. Use alone for G = 2 or tie to −INA2 for G = 3.
9, 10	$+V_{S2}$	Positive Supply Voltage, Amplifier 2.
11	V_{OCM2}	Output Common-Mode Voltage, Amplifier 2.
12	+OUT2	Positive Output, Amplifier 2.
13	−OUT2	Negative Output, Amplifier 2.
14	$\overline{PD2}$	Power-Down Pin, Amplifier 2.
15, 16	$-V_{S2}$	Negative Supply Voltage, Amplifier 2.
17	V_{OCM1}	Output Common-Mode Voltage, Amplifier 1.
18	+OUT1	Positive Output, Amplifier 1.
19	−OUT1	Negative Output, Amplifier 1.
20	$\overline{PD1}$	Power-Down Pin, Amplifier 1.
21, 22	$-V_{S1}$	Negative Supply Voltage, Amplifier 1.
23	+INB1	Positive Input B, Amplifier 1, 250 Ω Input. Use alone for G = 2 or tie to +INA1 for G = 3.
24	+INA1	Positive Input A, Amplifier 1, 500 Ω Input. Use alone for G = 1 or tie to +INB1 for G = 3.
25 (EPAD)	Exposed Paddle (EPAD)	Solder the exposed paddle on the back of the package to a ground plane or to a power plane.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = −5 V, V_{OCM} = 0 V, G = 1, R_T = 53.6 Ω (when used), $R_{L, dm}$ = 1 kΩ, unless otherwise noted. Refer to Figure 49 for test setup. Refer to Figure 52 for signal definitions.

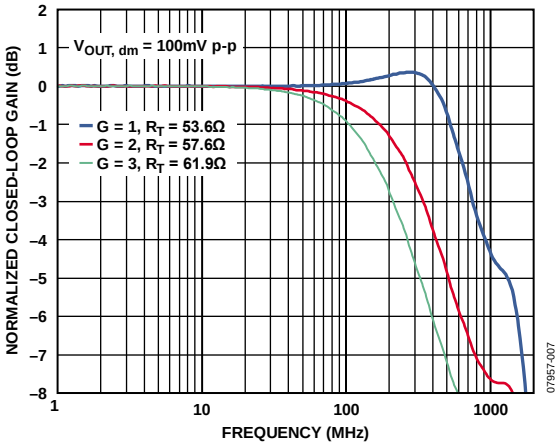

Figure 7. Small-Signal Frequency Response for Various Gains

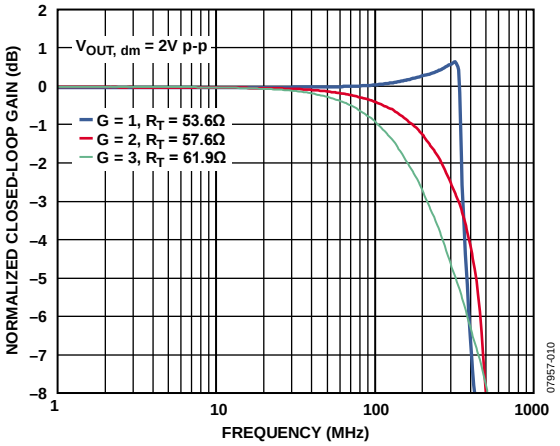

Figure 10. Large-Signal Frequency Response for Various Gains

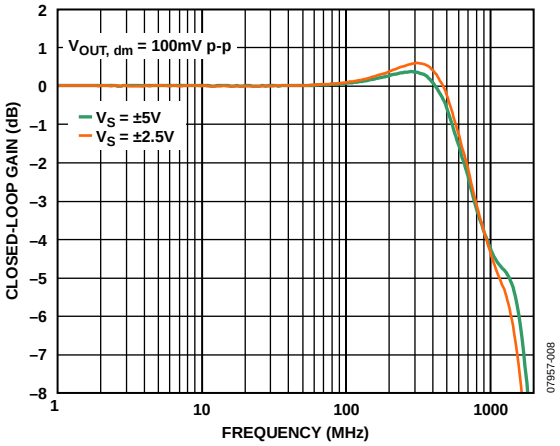

Figure 8. Small-Signal Frequency Response for Various Supplies

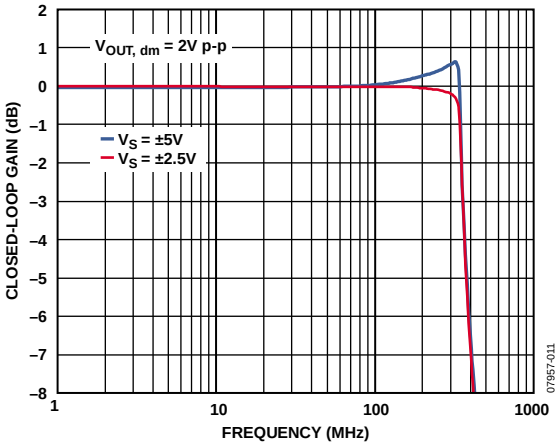

Figure 11. Large-Signal Frequency Response for Various Supplies

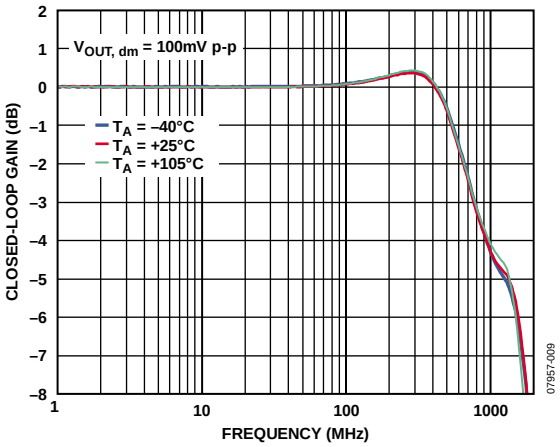

Figure 9. Small-Signal Frequency Response for Various Temperatures

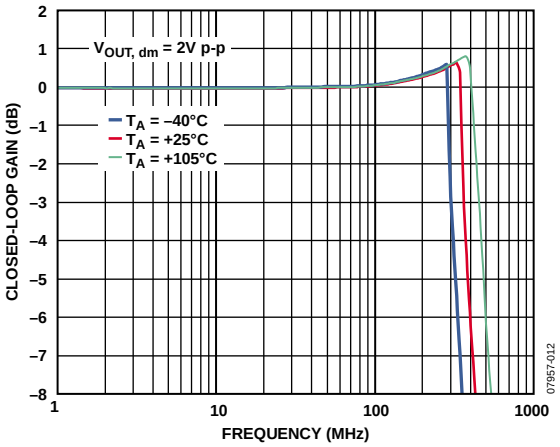

Figure 12. Large-Signal Frequency Response for Various Temperatures

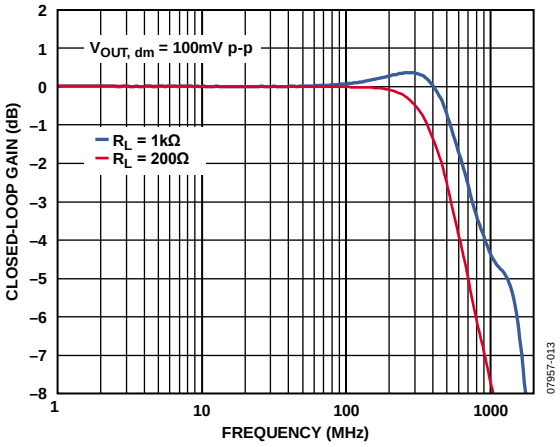

Figure 13. Small-Signal Frequency Response at Various Loads

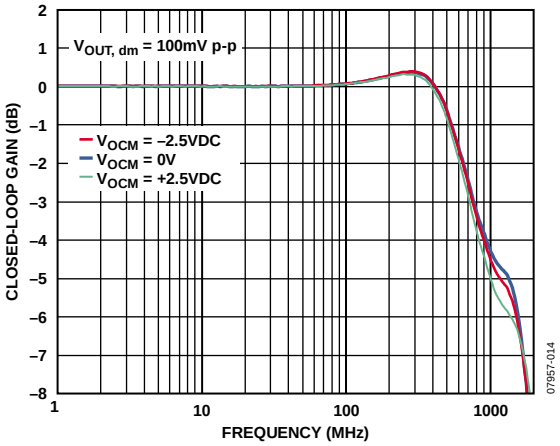

Figure 14. Small-Signal Frequency Response for Various V_{OCM} Levels

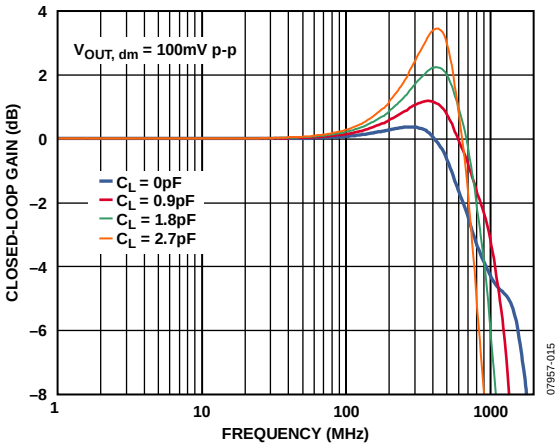

Figure 15. Small-Signal Frequency Response at Various Capacitive Loads

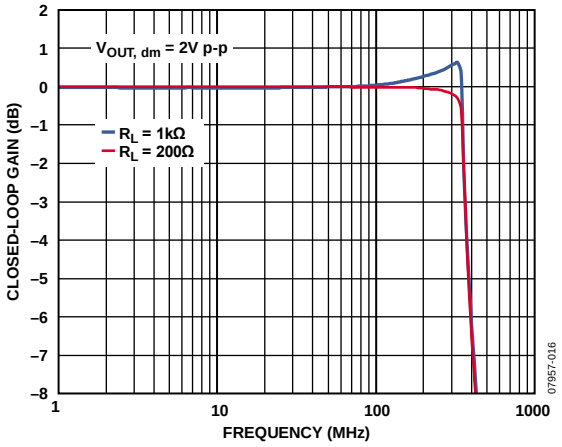

Figure 16. Large-Signal Frequency Response at Various Loads

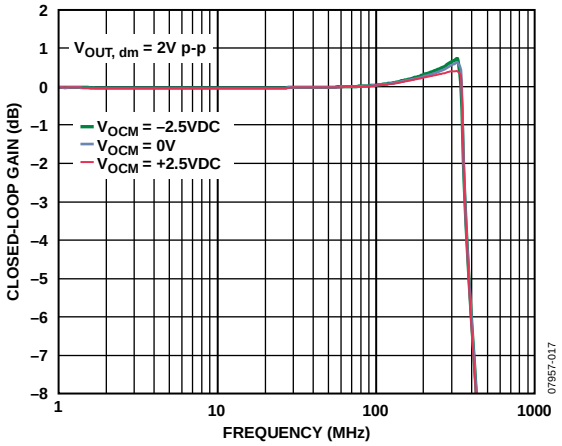

Figure 17. Large-Signal Frequency Response for Various V_{OCM} Levels

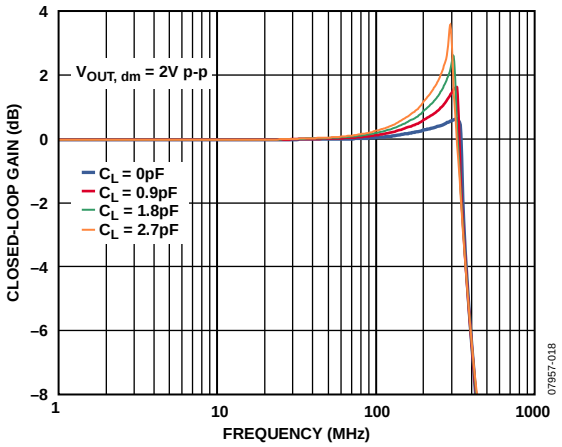

Figure 18. Large-Signal Frequency Response at Various Capacitive Loads

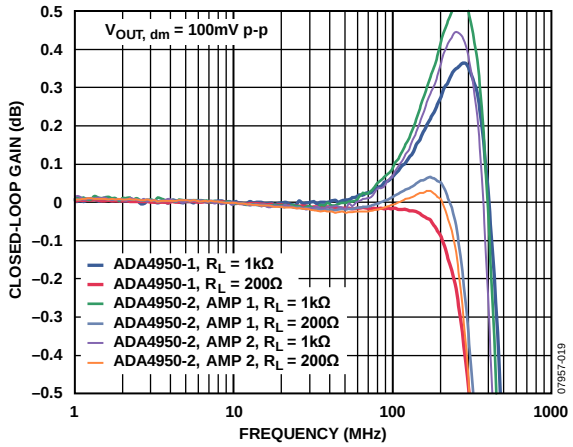

Figure 19. 0.1 dB Flatness, Small-Signal Frequency Response for Various Loads

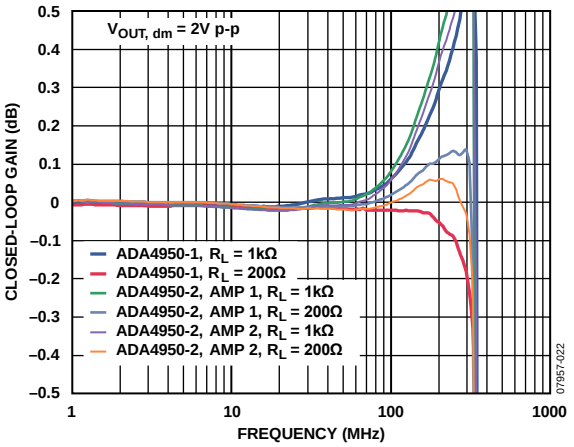

Figure 22. 0.1 dB Flatness, Large-Signal Frequency Response for Various Loads

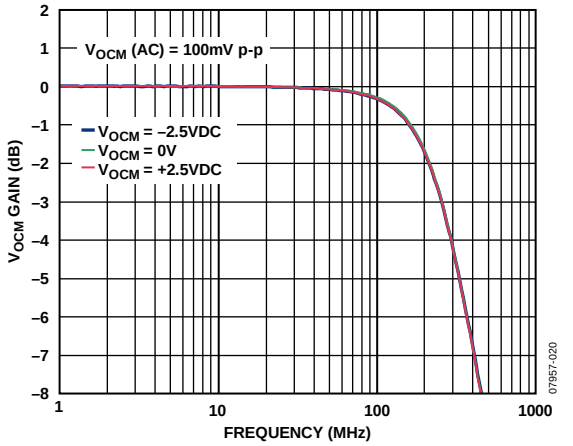

Figure 20. V_{OCM} Small-Signal Frequency Response at Various DC Levels

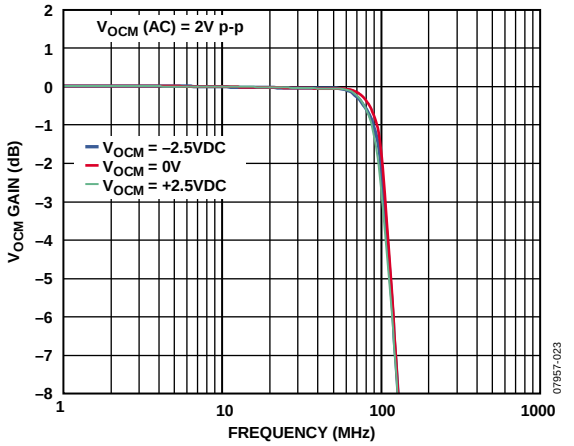

Figure 23. V_{OCM} Large-Signal Frequency Response at Various DC Levels

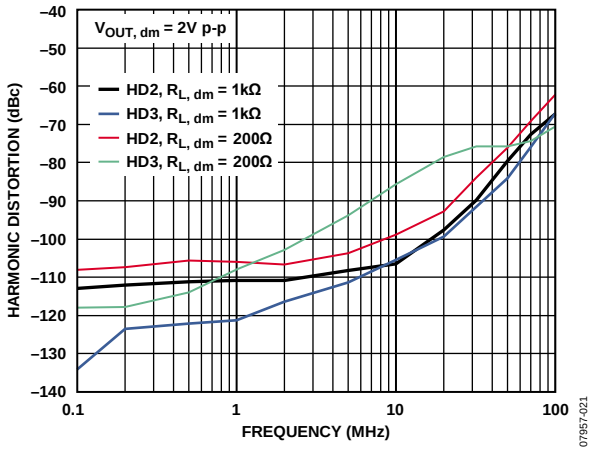

Figure 21. Harmonic Distortion vs. Frequency at Various Loads

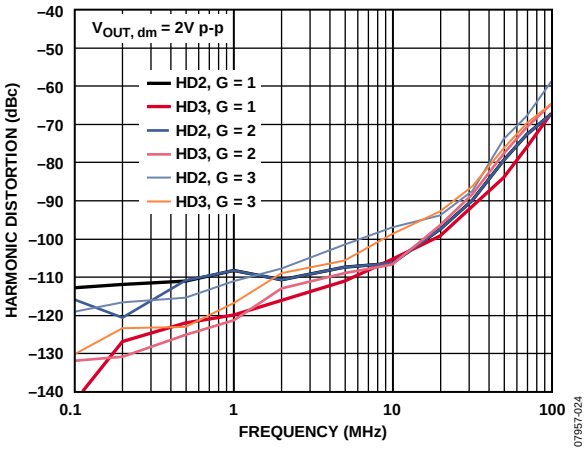

Figure 24. Harmonic Distortion vs. Frequency at Various Gains

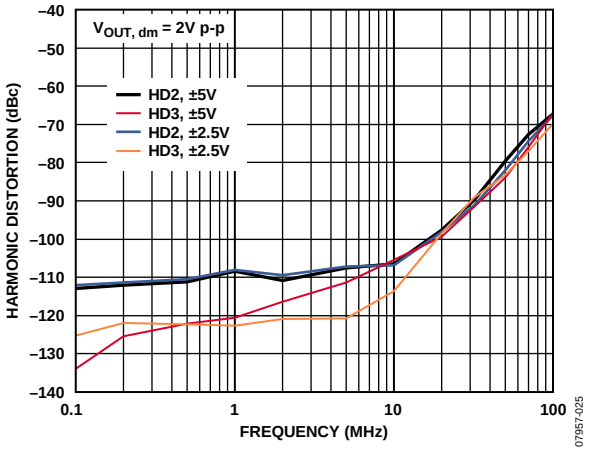

Figure 25. Harmonic Distortion vs. Frequency at Various Supplies

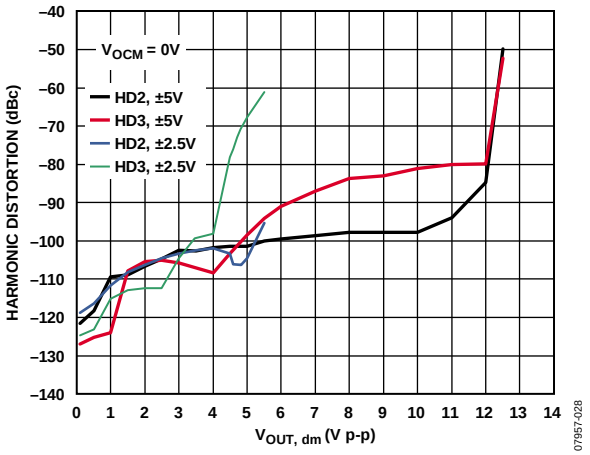

Figure 28. Harmonic Distortion vs. $V_{OUT, dm}$, f = 10 MHz

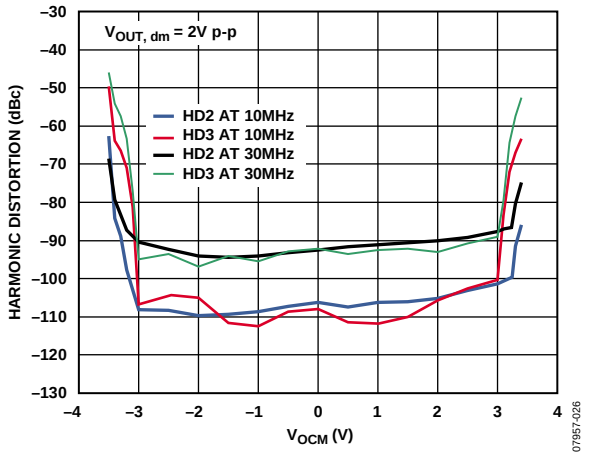

Figure 26. Harmonic Distortion vs. V_{OCM} at Various Frequencies, ±5 V Supplies

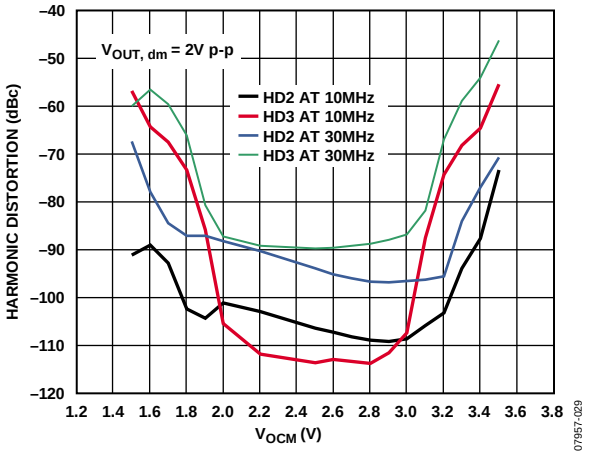

Figure 29. Harmonic Distortion vs. V_{OCM} at Various Frequencies, 5 V Supply

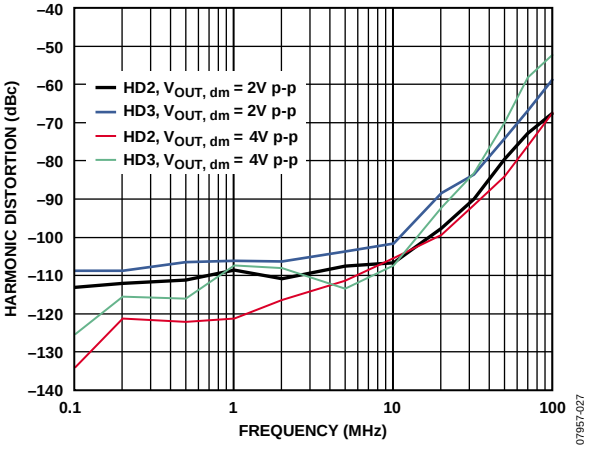

Figure 27. Harmonic Distortion vs. Frequency at Various $V_{OUT, dm}$

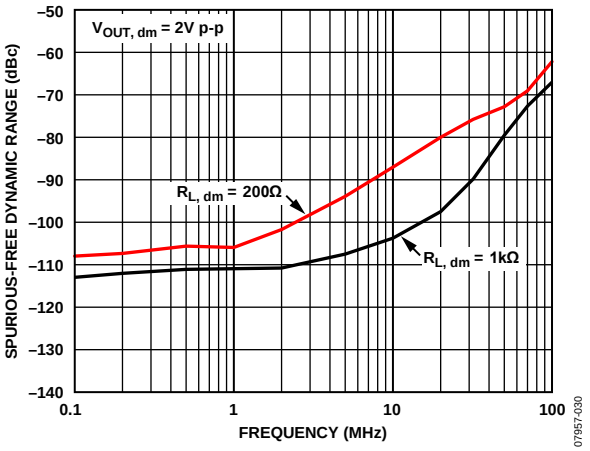

Figure 30. Spurious-Free Dynamic Range vs. Frequency at Various Loads

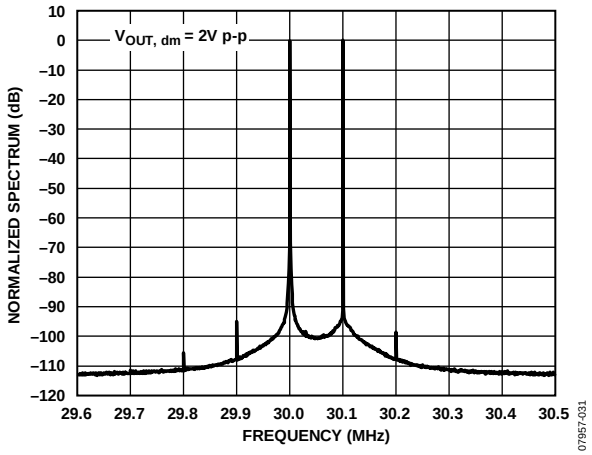

Figure 31. 30 MHz Intermodulation Distortion

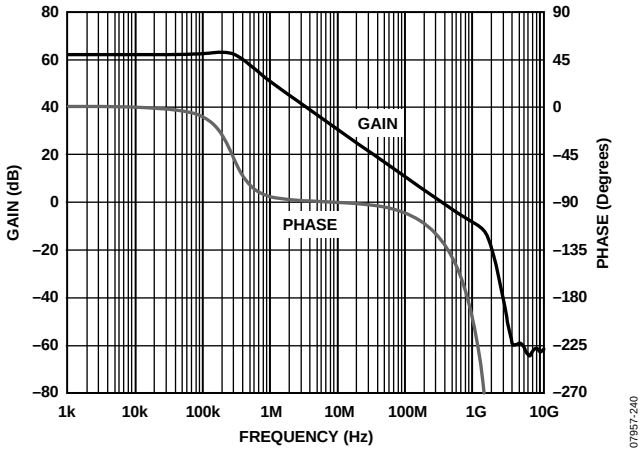

Figure 34. Open-Loop Gain and Phase vs. Frequency

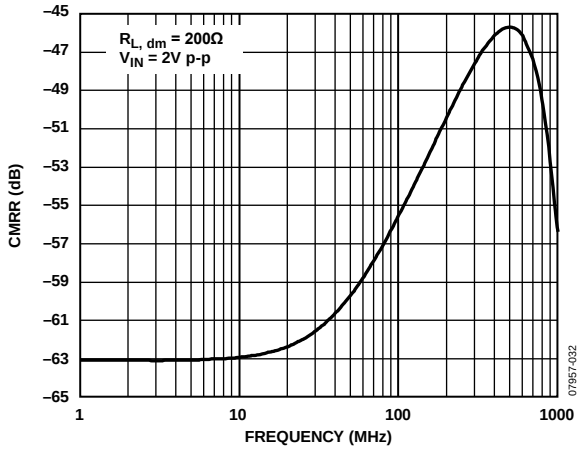

Figure 32. CMRR vs. Frequency

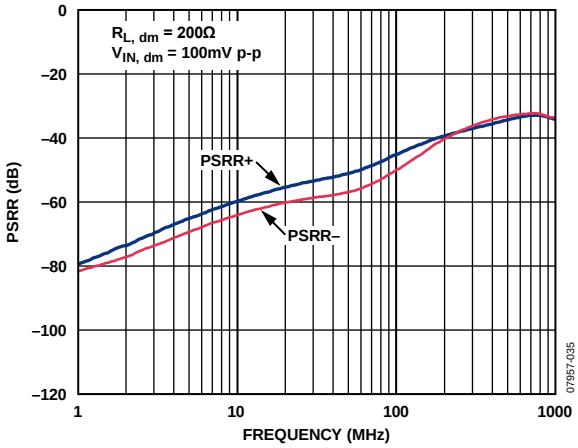

Figure 35. PSRR vs. Frequency

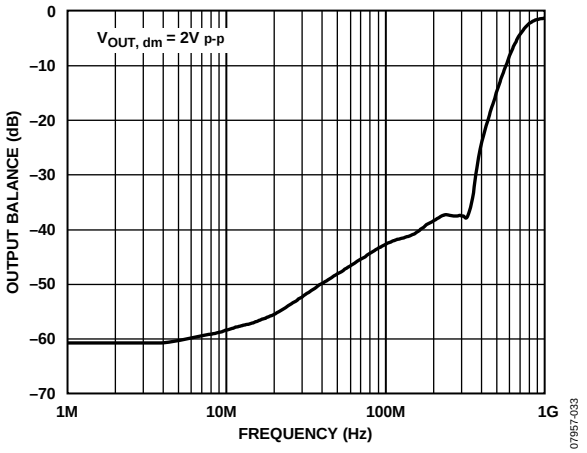

Figure 33. Output Balance vs. Frequency

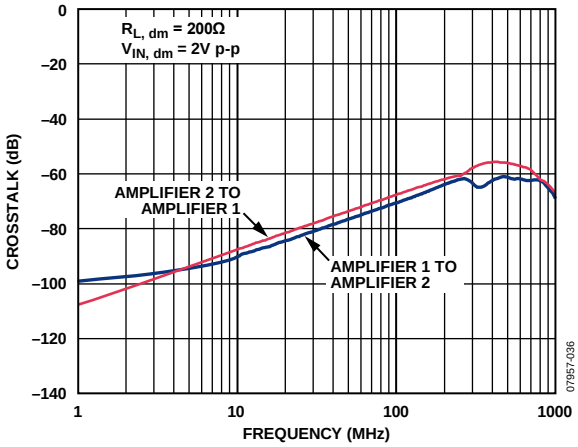

Figure 36. Crosstalk vs. Frequency, ADA4950-2

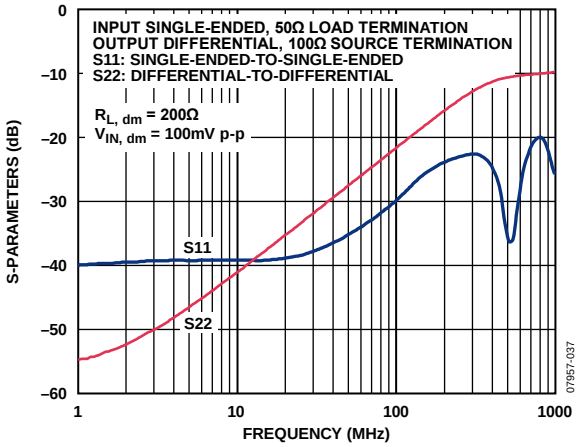

Figure 37. Return Loss (S_{11}, S_{22}) vs. Frequency

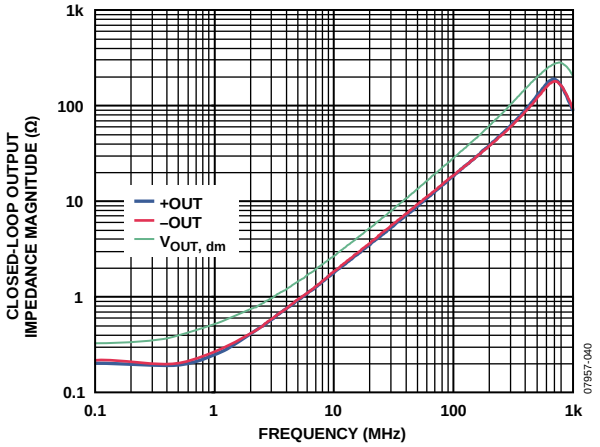

Figure 40. Closed-Loop Output Impedance Magnitude vs. Frequency, G = 1

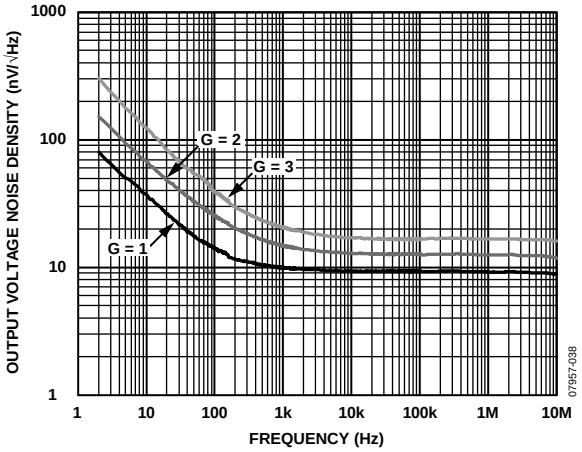

Figure 38. Voltage Noise Spectral Density for Various Gains, Referred to Output

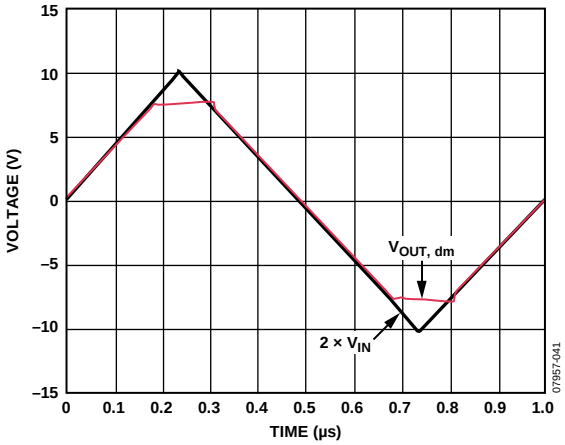

Figure 41. Overdrive Recovery, G = 2

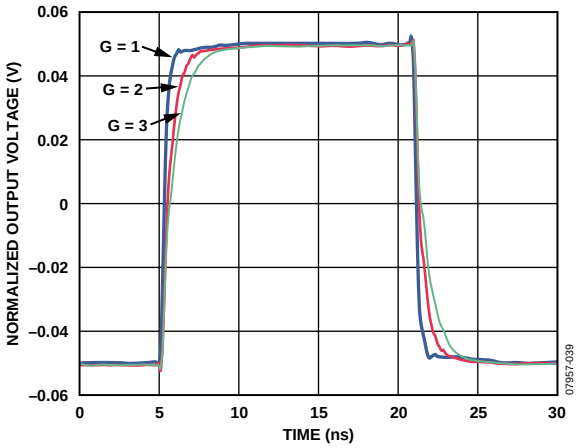

Figure 39. Small-Signal Pulse Response for Various Gains

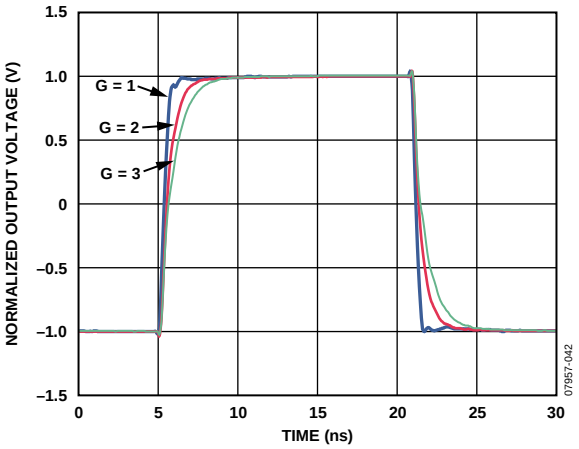

Figure 42. Large-Signal Pulse Response for Various Gains

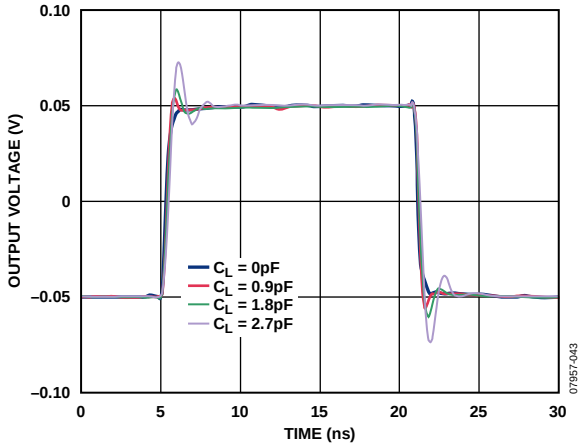

Figure 43. Small-Signal Pulse Response for Various Capacitive Loads

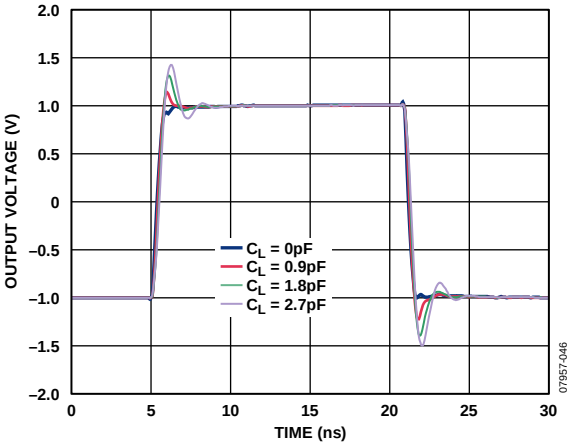

Figure 46. Large-Signal Pulse Response for Various Capacitive Loads

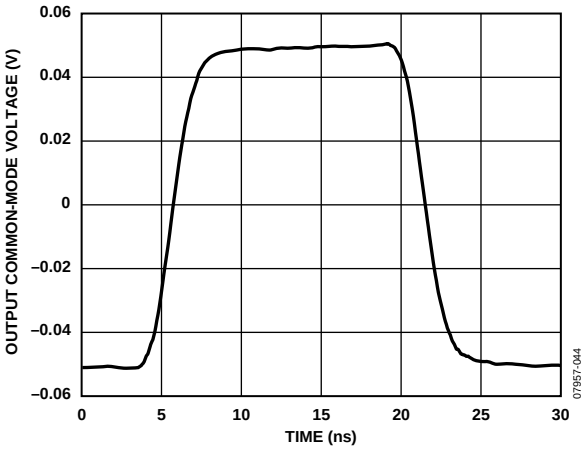

Figure 44. V_{OCM} Small-Signal Pulse Response

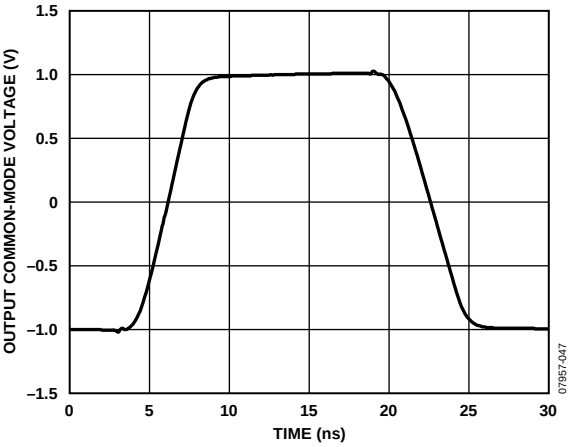

Figure 47. V_{OCM} Large-Signal Pulse Response

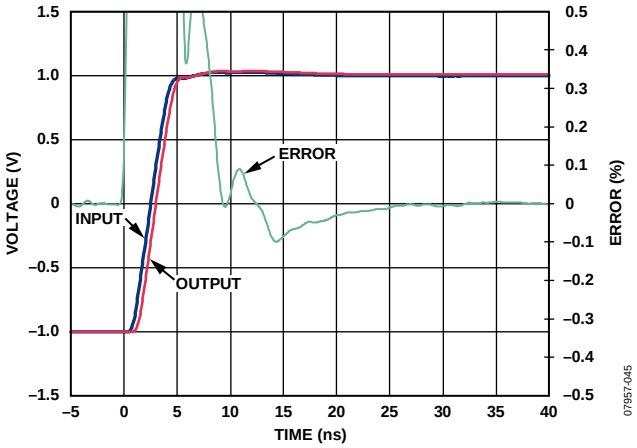

Figure 45. Settling Time

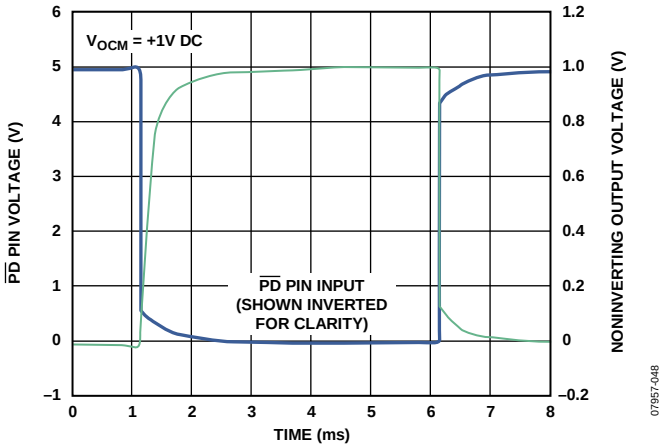

Figure 48. $\overline{PD}$ Response Time

TEST CIRCUITS

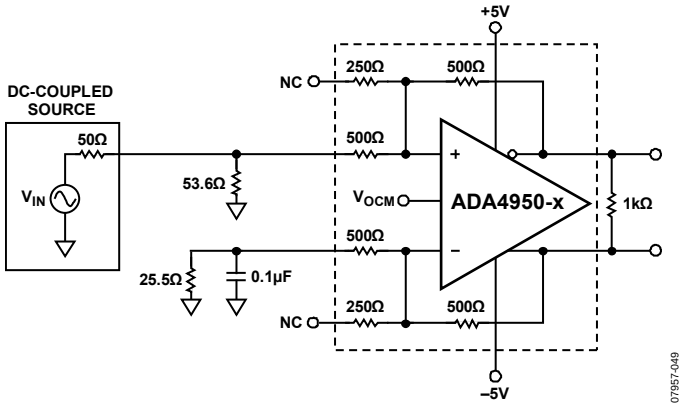

Figure 49. Equivalent Basic Test Circuit, G = 1

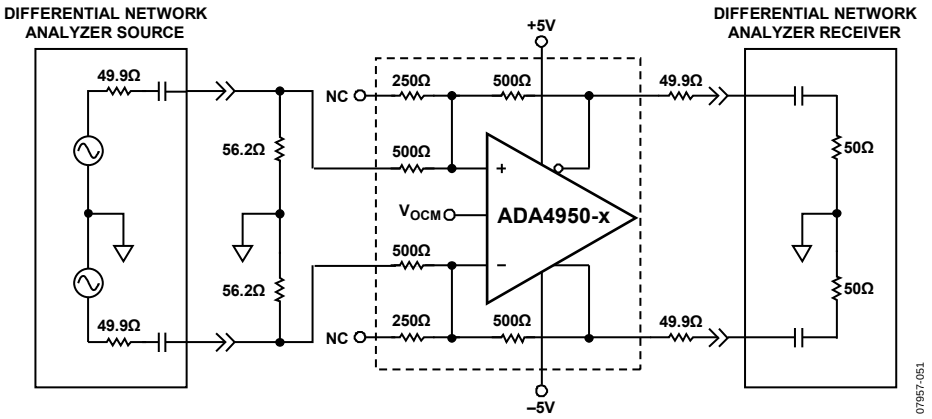

Figure 50. Test Circuit for Output Balance, CMRR

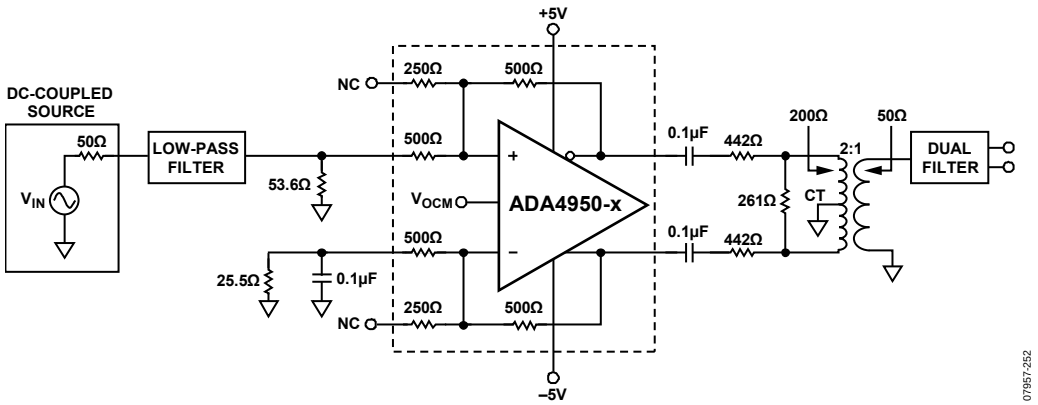

Figure 51. Test Circuit for Distortion Measurements

TERMINOLOGY

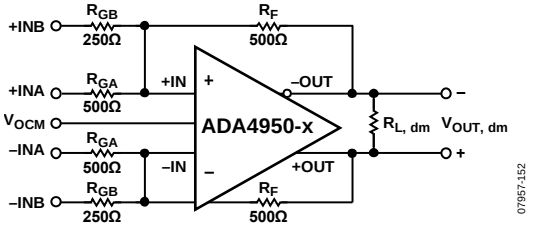

Figure 52. Signal and Circuit Definitions

Differential Voltage

Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or equivalently, output differential node voltage) is defined as

$$V_{OUT,\,dm} = (V_{+OUT} - V_{-OUT})$$

where V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and −OUT output terminals with respect to a common ground reference.

The input differential voltage is defined in different ways, depending upon the selected gain.

For G = 1

$$V_{IN,\,dm} = (+INA - (-INA))$$

where *+INA* and *−INA* refer to the voltages at the +INA and −INA input terminals with respect to a common ground reference (input terminals +INB and −INB are floating).

For G = 2

$$V_{IN,\,dm} = (+INB - (-INB))$$

where *+INB* and *−INB* refer to the voltages at the +INB and −INB input terminals with respect to a common ground reference (input terminals +INA and −INA are floating).

For G = 3, input terminals +INA and +INB are connected together, and input terminals −INA and −INB are connected together.

$$V_{IN,\,dm} = (+INAB - (-INAB))$$

where *+INAB* and *−INAB* refer to the voltages at the connection of input terminals +INA and +INB and at the connection of input terminals −INA and −INB with respect to a common ground reference.

Common-Mode Voltage

Common-mode voltage refers to the average of two node voltages with respect to the local ground reference. The output common-mode voltage is defined as

$$V_{OUT,\,cm} = (V_{+OUT} + V_{-OUT})/2$$

Output Balance

Output balance is a measure of how close the output differential signals are to being equal in amplitude and opposite in phase. Any imbalances in amplitude or phase produce an undesired common-mode signal at the amplifier output. Output balance error is defined as the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage.

$$Output\ Balance\ Error = \left| \frac{\Delta V_{OUT,\,cm}}{\Delta V_{OUT,\,dm}} \right|$$

THEORY OF OPERATION

The ADA4950-x differs from conventional op amps in that it has two outputs whose voltages move in opposite directions and an additional input, V_{OCM}. Like an op amp, it relies on high open-loop gain and negative feedback to force these outputs to the desired voltages. The ADA4950-x behaves much like a standard voltage feedback op amp and facilitates single-ended-to-differential conversions, common-mode level shifting, and amplifications of differential signals. Like an op amp, the ADA4950-x has high input impedance at its internal input terminals (to the right of the internal gain resistors) and low output impedance. Because it uses voltage feedback, the ADA4950-x manifests a nominally constant gain bandwidth product.

Two feedback loops are used to control the differential and common-mode output voltages. The differential feedback loop, set with on-chip feedback and gain resistors, controls only the differential output voltage. The common-mode feedback loop is internal to the actual amplifier and controls only the common-mode output voltage. This architecture makes it easy to set the output common-mode level to any arbitrary value within the specified limits. The output common-mode voltage is forced, by the internal common-mode feedback loop, to be equal to the voltage applied to the V_{OCM} input.

The internal common-mode feedback loop produces outputs that are highly balanced over a wide frequency range without requiring tightly matched external components. This results in differential outputs that are very close to the ideal of being identical in amplitude and that are exactly 180° apart in phase.

APPLICATIONS INFORMATION

ANALYZING AN APPLICATION CIRCUIT

The ADA4950-x uses high open-loop gain and negative feedback to force its differential and common-mode output voltages in such a way as to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs labeled +INx and −INx (see Figure 52). For most purposes, this voltage can be assumed to be 0. Similarly, the difference between the actual output common-mode voltage and the voltage applied to V_{OCM} can also be assumed to be 0. Starting from these principles, any application circuit can be analyzed.

SELECTING THE CLOSED-LOOP GAIN

Using the approach described in the Analyzing an Application Circuit section, the differential gain of the circuit in Figure 52 can be determined by

$$\left|\frac{V_{OUT,\,dm}}{V_{IN,\,dm}}\right| = \frac{R_F}{R_G}$$

where the input resistors (R_G) and the feedback resistors (R_F) on each side are equal.

For G = 1, the +INA and −INA inputs are used, and the +INB and −INB inputs are left floating. The differential gain in this case is calculated as follows:

$$G = \frac{R_F}{R_G} = \frac{500\,\Omega}{500\,\Omega} = 1$$

For G = 2, the +INB and −INB inputs are used, and the +INA and −INA inputs are left floating. The differential gain in this case is calculated as follows:

$$G = \frac{R_F}{R_G} = \frac{500\,\Omega}{250\,\Omega} = 2$$

For G = 3, the +INA and +INB inputs are connected together, and the −INA and −INB inputs are connected together. The differential gain in this case is calculated as follows:

$$G = \frac{R_F}{R_G} = \frac{500\,\Omega}{500\,\Omega||250\,\Omega} = 3$$

ESTIMATING THE OUTPUT NOISE VOLTAGE

The differential output noise of the ADA4950-x can be estimated using the noise model in Figure 53. The values of R_G depend on the selected gain. The input-referred noise voltage density, v_{nIN}, is modeled as a differential input, and the noise currents, i_{nIN-} and i_{nIN+}, appear between each input and ground. The output voltage due to v_{nIN} is obtained by multiplying v_{nIN} by the noise gain, G_N (defined in the G_N equation that follows Table 13). The noise currents are uncorrelated with the same mean-square value, and each produces an output voltage that is equal to the noise current multiplied by the associated feedback resistance. The noise voltage density at the V_{OCM} pin is v_{nCM}. When the feedback networks have the same feedback factor, as is true in most cases, the output noise due to v_{nCM} is common mode. Each of the four resistors contributes $(4kTR_{xx})^{1/2}$. The noise from the feedback resistors appears directly at the output, and the noise from the gain resistors appears at the output multiplied by R_F/R_G. Table 11 summarizes the input noise sources, the multiplication factors, and the output-referred noise density terms.

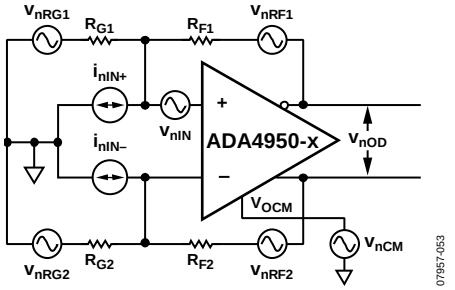

Figure 53. Noise Model

Table 11. Output Noise Voltage Density Calculations for Matched Feedback Networks

Input Noise Contribution	Input Noise Term	Input Noise Voltage Density	Output Multiplication Factor	Differential Output Noise Voltage Density Term
Differential Input	v_{nIN}	v_{nIN}	G_N	$v_{nO1} = G_N(v_{nIN})$
Inverting Input	i_{nIN-}	$i_{nIN-} \times (R_{F2})$	1	$v_{nO2} = (i_{nIN-})(R_{F2})$
Noninverting Input	i_{nIN+}	$i_{nIN+} \times (R_{F1})$	1	$v_{nO3} = (i_{nIN+})(R_{F1})$
V_{OCM} Input	v_{nCM}	v_{nCM}	0	v_{nO4} = 0 V
Gain Resistor, R_{G1}	v_{nRG1}	$(4kTR_{G1})^{1/2}$	R_{F1}/R_{G1}	$v_{nO5} = (R_{F1}/R_{G1})(4kTR_{G1})^{1/2}$
Gain Resistor, R_{G2}	v_{nRG2}	$(4kTR_{G2})^{1/2}$	R_{F2}/R_{G2}	$v_{nO6} = (R_{F2}/R_{G2})(4kTR_{G2})^{1/2}$
Feedback Resistor, R_{F1}	v_{nRF1}	$(4kTR_{F1})^{1/2}$	1	$v_{nO7} = (4kTR_{F1})^{1/2}$
Feedback Resistor, R_{F2}	v_{nRF2}	$(4kTR_{F2})^{1/2}$	1	$v_{nO8} = (4kTR_{F2})^{1/2}$

Table 12. Differential Input, DC-Coupled

Nominal Linear Gain	R_F (Ω)	R_G (Ω)	$R_{IN, dm}$ (Ω)	Differential Output Noise Density (nV/√Hz)
1	500	500	1000	9.25
2	500	250	500	12.9
3	500	250||500	333	16.6

Table 13. Single-Ended, Ground-Referenced Input, DC-Coupled, R_S = 50 Ω

Nominal Linear Gain	R_F (Ω)	R_{G1} (Ω)	R_T (Ω) (Std 1%)	$R_{IN, se}$ (Ω)	R_{G2} (Ω)[1]	Differential Output Noise Density (nV/√Hz)
1	500	500	53.6	667	526	9.07
2	500	250	57.6	375	277	12.2
3	500	250||500	61.9	267	194	15.0

[1] $R_{G2} = R_{G1} + (R_S||R_T)$.

Similar to the case of a conventional op amp, the output noise voltage densities can be estimated by multiplying the input-referred terms at +INx and −INx by the appropriate output factor, where:

$G_N = \frac{2}{(\beta_1 + \beta_2)}$ is the circuit noise gain.

$\beta_1 = \frac{R_{G1}}{R_{F1} + R_{G1}}$ and $\beta_2 = \frac{R_{G2}}{R_{F2} + R_{G2}}$ are the feedback factors.

When the feedback factors are matched, $R_{F1}/R_{G1} = R_{F2}/R_{G2}$, $\beta 1 = \beta 2 = \beta$, and the noise gain becomes

$$G_N = \frac{1}{\beta} = 1 + \frac{R_F}{R_G}$$

Note that the output noise from V_{OCM} goes to 0 in this case. The total differential output noise density, v_{nOD}, is the root-sum-square of the individual output noise terms.

$$v_{nOD} = \sqrt{\sum_{i=1}^{8} v_{nOi}^2}$$

Table 12 and Table 13 list the three available gain settings, associated resistor values, input impedance, and output noise density for both balanced and unbalanced input configurations.

CALCULATING THE INPUT IMPEDANCE FOR AN APPLICATION CIRCUIT

The effective input impedance of a circuit depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, as shown in Figure 54, the input impedance ($R_{IN, dm}$) is

$$R_{IN, dm} = (R_G + R_G) = 2 \times R_G$$

The value of R_G depends on the selected gain.

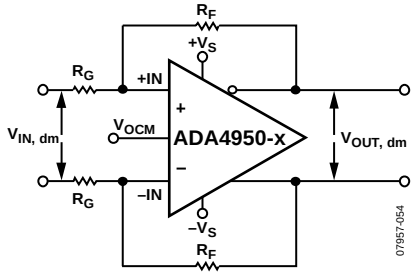

Figure 54. ADA4950-x Configured for Balanced (Differential) Inputs

For an unbalanced, single-ended input signal (see Figure 55), the input impedance is

$$R_{IN, se} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right)$$

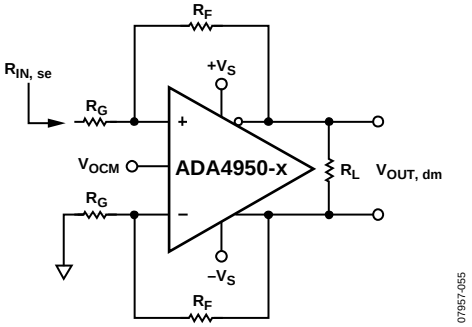

Figure 55. ADA4950-x with Unbalanced (Single-Ended) Input

The input impedance of the circuit is effectively higher than it is for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor, R_G. The common-mode voltage at the amplifier input terminals can be easily determined by noting that the voltage at the inverting input is equal to the noninverting output voltage divided down by the voltage divider that is formed by R_F and R_G in the lower loop. This voltage is present at both input terminals due to negative voltage feedback and is in phase with the input signal, thus reducing the effective voltage across R_G in the upper loop and partially bootstrapping R_G.

Terminating a Single-Ended Input

This section describes how to properly terminate a single-ended input to the ADA4950-x with a gain of 1, R_F = 500 Ω, and R_G = 500 Ω. An example using an input source with a terminated output voltage of 1 V p-p and source resistance of 50 Ω illustrates the steps that must be followed. Note that because the terminated output voltage of the source is 1 V p-p, the open-circuit output voltage of the source is 2 V p-p. The source shown in Figure 56 indicates this open-circuit voltage.

1. The input impedance is calculated using the following formula:

$$R_{IN,se} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right) = \left(\frac{500}{1 - \frac{500}{2 \times (500 + 500)}} \right) = 667\ \Omega$$

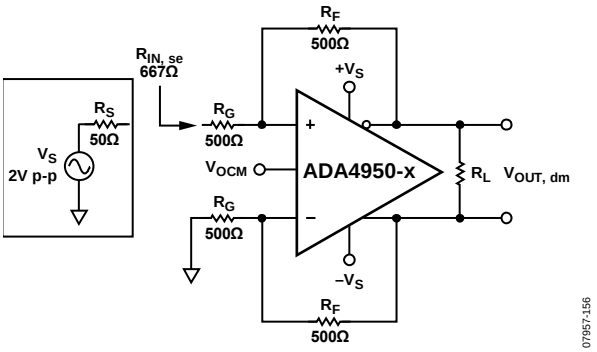

Figure 56. Calculating Single-Ended Input Impedance, R_{IN}

2. To match the 50 Ω source resistance, calculate the termination resistor, R_T, using $R_T||667\ \Omega = 50\ \Omega$. The closest standard 1% value for R_T is 53.6 Ω.

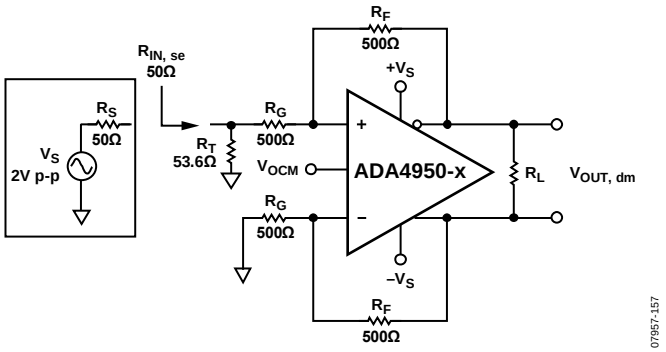

Figure 57. Adding Termination Resistor, R_T

3. Figure 57 shows that the effective R_G in the upper feedback loop is now greater than the R_G in the lower loop due to the addition of the termination resistors. To compensate for the imbalance of the gain resistors, add a correction resistor (R_{TS}) in series with R_G in the lower loop. R_{TS} is the Thevenin equivalent of the source resistance, R_S, and the termination resistance, R_T, and is equal to $R_S||R_T$.

$R_{TS} = R_{TH} = R_S||R_T = 25.9\ \Omega$

Figure 58. Calculating the Thevenin Equivalent

Note that V_{TH} is greater than 1 V p-p, which was obtained with R_T = 50 Ω. The modified circuit with the Thevenin equivalent (closest 1% value used for R_{TH}) of the terminated source and R_{TS} in the lower feedback loop is shown in Figure 59.

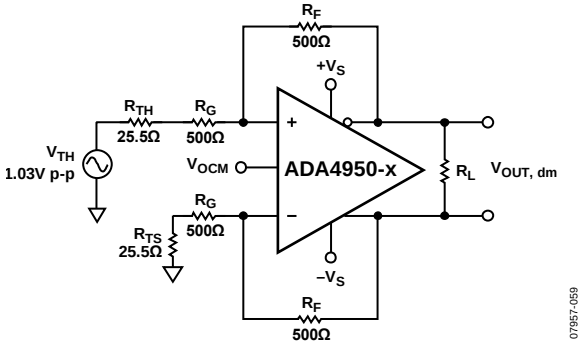

Figure 59. Thevenin Equivalent and Matched Gain Resistors

Figure 59 presents a tractable circuit with matched feedback loops that can be easily evaluated.

It is useful to point out two effects that occur with a terminated input. The first is that the value of R_G is increased in both loops, lowering the overall closed-loop gain. The second is that V_{TH} is a little larger than 1 V p-p, as it would be if R_T = 50 Ω. These two effects have opposite impacts on the output voltage, and for large resistor values in the feedback loops (~1 kΩ), the effects essentially cancel each other out. For small R_F and R_G, or high gains, however, the diminished closed-loop gain is not canceled completely by the increased V_{TH}. This can be seen by evaluating Figure 59.

The desired differential output in this example is 1 V p-p because the terminated input signal is 1 V p-p and the closed-loop gain = 1. The actual differential output voltage, however, is equal to (1.03 V p-p)(500/525.5) = 0.98 V p-p.

INPUT COMMON-MODE VOLTAGE RANGE

The ADA4950-x input common-mode voltage range is shifted down by approximately one V_{BE}, in contrast to other ADC drivers with centered input ranges such as the ADA4939-x. The downward-shifted input common-mode range is especially suited to dc-coupled, single-ended-to-differential, and single-supply applications.

For ±5 V operation, the input common-mode voltage range at the summing nodes of the amplifier is specified as −4.8 V to +3.2 V. With a 5 V supply, the input common-mode voltage range at the summing nodes of the amplifier is specified as +0.2 V to +3.2 V. To avoid nonlinearities, the voltage swing at the +INx and −INx terminals must be confined to these ranges.

INPUT AND OUTPUT CAPACITIVE AC COUPLING

Although the ADA4950-x is well suited to dc-coupled applications, it is nonetheless possible to use it in ac-coupled circuits. Input ac coupling capacitors can be inserted between the source and R_G. This ac coupling blocks the flow of the dc common-mode feedback current and causes the ADA4950-x dc input common-mode voltage to equal the dc output common-mode voltage. The ac coupling capacitors must be placed in both loops to keep the feedback factors matched. Output ac coupling capacitors can be placed in series between each output and its respective load.

INPUT SIGNAL SWING CONSIDERATIONS

The input terminals of fully differential amplifiers with external gain and feedback resistors connect directly to the amplifier summing nodes; the common-mode voltage swing at these terminals is generally smaller than the input and output swings. In most linear applications, the summing node voltages do not approach levels that result in the forward-biasing of the internal ESD protection diodes on the amplifier inputs.

Signals at the inputs of the ADA4950-x are applied to the input side of the gain resistors, and, if caution is not exercised, these signals can be large enough to forward-bias the ESD protection diodes. The four inputs that make up the differential signal paths each have four ESD diodes in series to the negative supply and one diode to the positive supply; the V_{OCM} input has one ESD diode to each supply. Figure 60 illustrates the ESD protection circuitry.

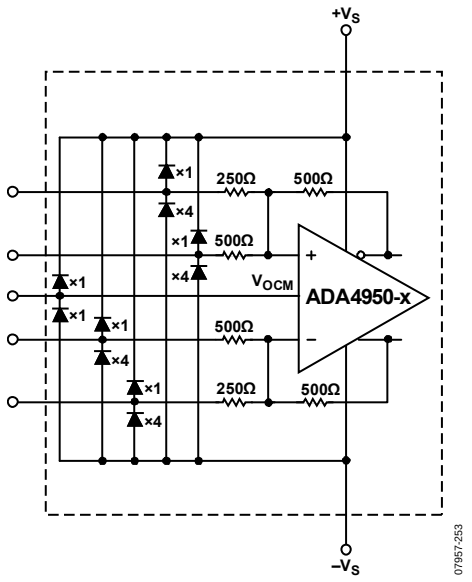

Figure 60. Input ESD Protection Circuitry

SETTING THE OUTPUT COMMON-MODE VOLTAGE

The V_{OCM} pin of the ADA4950-x is internally biased with a voltage divider comprising two 50 kΩ resistors across the supplies, with a tap at a voltage approximately equal to the midsupply point, $[(+V_S) + (-V_S)]/2$. Because of this internal divider, the V_{OCM} pin sources and sinks current, depending on the externally applied voltage and its associated source resistance. Relying on the internal bias results in an output common-mode voltage that is within approximately 100 mV of the expected value.

In cases where more accurate control of the output common-mode level is required, it is recommended that an external source or resistor divider be used with source resistance less than 100 Ω. If an external voltage divider consisting of equal resistor values is used to set V_{OCM} to midsupply with greater accuracy than produced internally, higher values can be used because the external resistors are placed in parallel with the internal resistors. The input V_{OCM} offset listed in the Specifications section assumes that the V_{OCM} input is driven by a low impedance voltage source.

It is also possible to connect the V_{OCM} input to a common-mode level (CML) output of an ADC; however, care must be taken to ensure that the output has sufficient drive capability. The input impedance of the V_{OCM} pin is approximately 10 kΩ to a voltage of nominally midsupply. If multiple ADA4950-x devices share one ADC reference output, a buffer may be necessary to drive the parallel inputs.

LAYOUT, GROUNDING, AND BYPASSING

As a high speed device, the ADA4950-x is sensitive to the PCB environment in which it operates. Realizing its superior performance requires attention to the details of high speed PCB design.

The first requirement is a solid ground plane that covers as much of the board area around the ADA4950-x as possible. The thermal resistance, θ_{JA}, is specified for the device, including the exposed pad, soldered to a high thermal conductivity 4-layer circuit board, as described in EIA/JESD51-7.

Bypass the power supply pins as close to the device as possible and directly to a nearby ground plane. Use high frequency ceramic chip capacitors. It is recommended that two parallel bypass capacitors (1000 pF and 0.1 µF) be used for each supply. Place the 1000 pF capacitor closer to the device. Farther away, provide low frequency bulk bypassing using 10 µF tantalum capacitors from each supply to ground.

Signal routing should be short and direct to avoid parasitic effects. Wherever complementary signals exist, provide a symmetrical layout to maximize balanced performance. When routing differential signals over a long distance, keep PCB traces close together, and twist any differential wiring to minimize loop area. Doing this reduces radiated energy and makes the circuit less susceptible to interference.

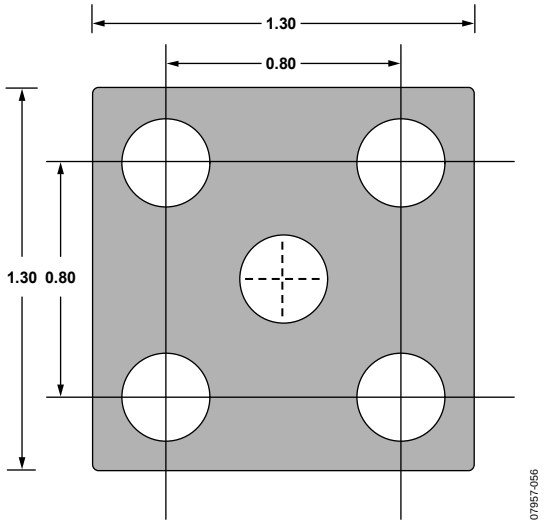

Figure 61. Recommended PCB Thermal Attach Pad (Dimensions in Millimeters)

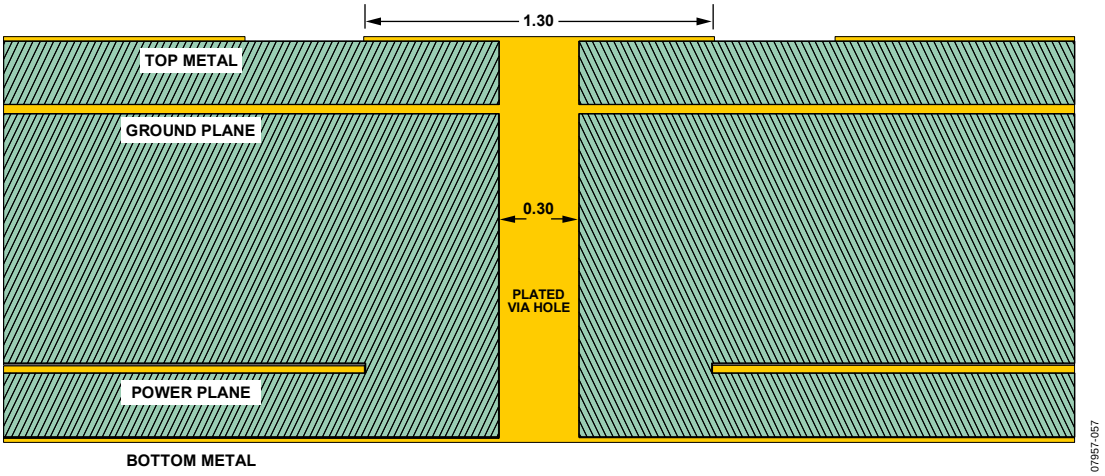

Figure 62. Cross-Section of 4-Layer PCB Showing Thermal Via Connection to Buried Ground Plane (Dimensions in Millimeters)

HIGH PERFORMANCE ADC DRIVING

The ADA4950-x is ideally suited for broadband dc-coupled applications. The circuit in Figure 63 shows a front-end connection for an ADA4950-1 driving an AD9245 ADC, with dc coupling on the ADA4950-1 input and output. (The AD9245 achieves its optimum performance when driven differentially.) The ADA4950-1 eliminates the need for a transformer to drive the ADC and performs a single-ended-to-differential conversion and buffering of the driving signal.

The ADA4950-1 is configured with a single 3.3 V supply and a gain of 2 for a single-ended input to differential output. The 57.6 Ω termination resistor, in parallel with the single-ended input impedance of 375 Ω, provides a 50 Ω termination for the source. The additional 26.7 Ω Thevenin resistance added to the inverting input balances the parallel impedance of the 50 Ω source and the termination resistor driving the noninverting input. The required Thevenin bias voltage of 0.27 VDC applied to the lower loop is obtained by scaling the VREF output of the AD9245 and buffering it with the AD8031.

In this example, the 50 Ω signal generator has a 1 V p-p unipolar open-circuit output voltage, and 0.5 V p-p output voltage when terminated in 50 Ω. The V_{OCM} input is bypassed for noise reduction and set externally with 1% resistors to maximize output dynamic range on the tight 3.3 V supply.

Because the inputs are dc-coupled, dc common-mode current flows in the feedback loops, and a nominal dc level of 0.76 V is present at the amplifier input terminals. A fraction of the output signal is also present at the input terminals as a common-mode signal; its level is equal to the ac output swing at the noninverting output, divided down by the feedback factor of the lower loop. In this example, this ripple is 0.5 V p-p × [276.7/(276.7 + 500)] = 0.18 V p-p. This ac signal is riding on the 0.76 V dc level, producing a voltage swing between 0.67 V and 0.85 V at the input terminals. This is well within the specified limits of 0.2 V to 1.5 V.

With an output common-mode voltage of 1.65 V, each ADA4950-1 output swings between 1.4 V and 1.9 V, opposite in phase, providing a gain of 2 and a 1 V p-p differential signal to the ADC input. The differential RC section between the ADA4950-1 output and the ADC provides single-pole low-pass filtering and extra buffering for the current spikes that are output from the ADC input when its SHA capacitors are discharged.

The AD9245 is configured for a 1 V p-p full-scale input by connecting its SENSE pin to VREF, as shown in Figure 63.

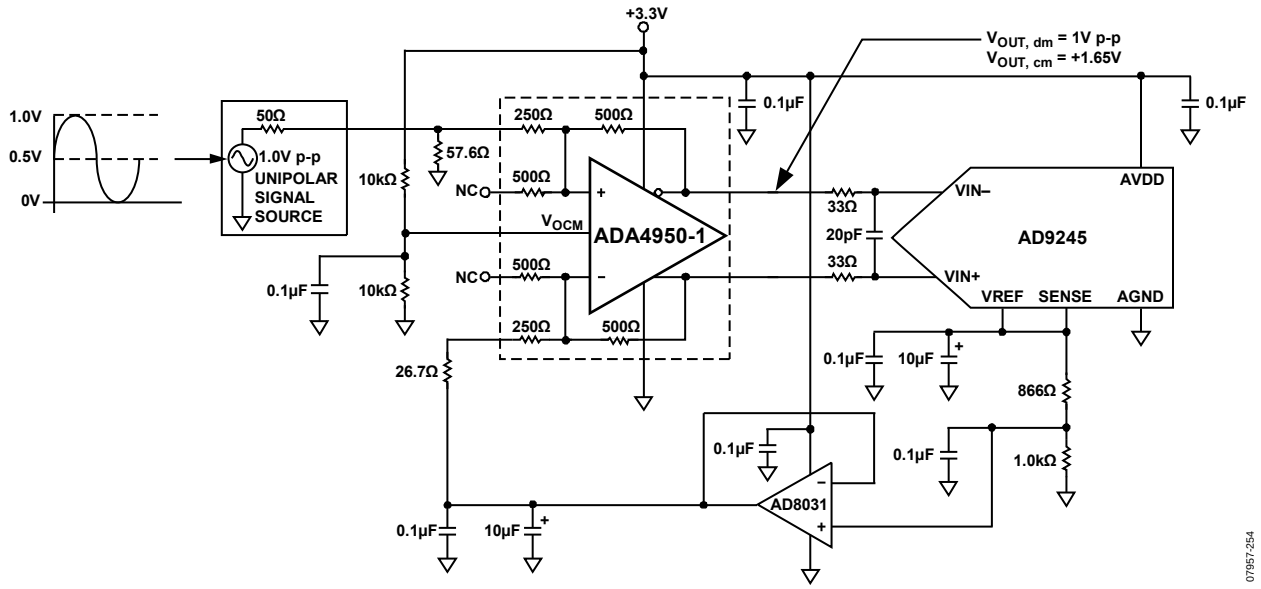

Figure 63. ADA4950-1 Driving an AD9245 ADC with Unipolar DC-Coupled Input and Output, Gain = 2

OUTLINE DIMENSIONS

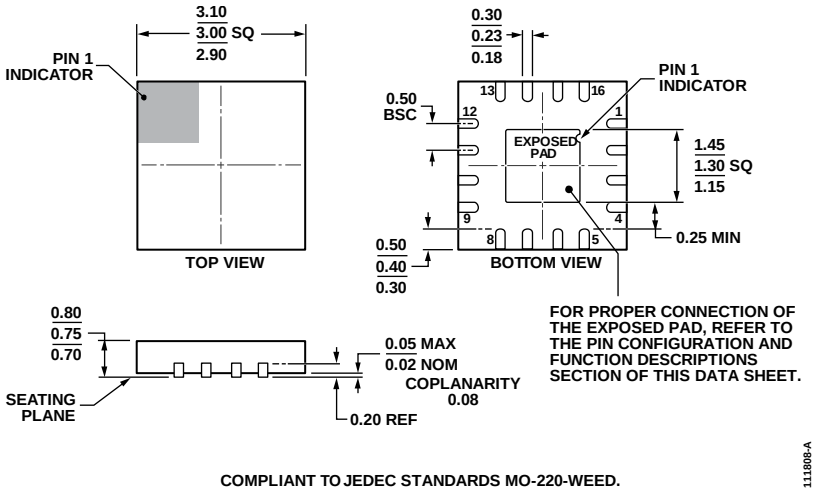

Figure 64. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad (CP-16-21)
Dimensions shown in millimeters

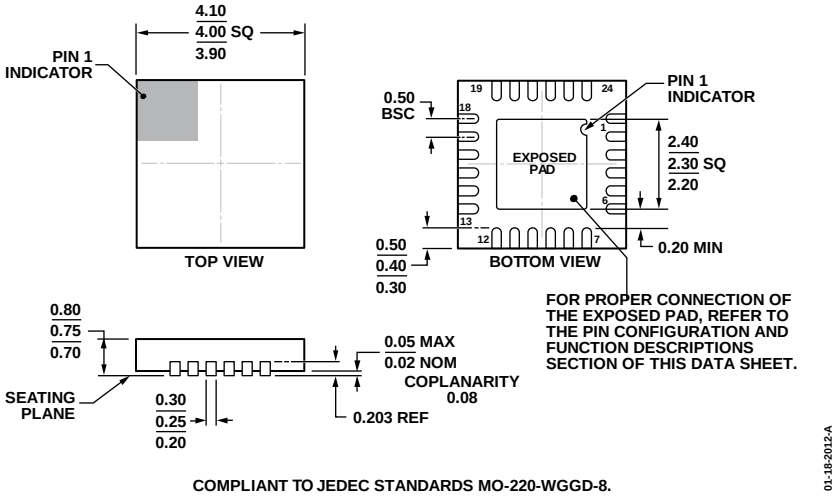

Figure 65. 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad (CP-24-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADA4950-1YCPZ-R2	−40°C to +105°C	16-Lead LFCSP_WQ	CP-16-21	250	H1L
ADA4950-1YCPZ-RL	−40°C to +105°C	16-Lead LFCSP_WQ	CP-16-21	5,000	H1L
ADA4950-1YCPZ-R7	−40°C to +105°C	16-Lead LFCSP_WQ	CP-16-21	1,500	H1L
ADA4950-1YCP-EBZ		Evaluation Board			
ADA4950-2YCPZ-R2	−40°C to +105°C	24-Lead LFCSP_WQ	CP-24-14	250	
ADA4950-2YCPZ-RL	−40°C to +105°C	24-Lead LFCSP_WQ	CP-24-14	5,000	
ADA4950-2YCPZ-R7	−40°C to +105°C	24-Lead LFCSP_WQ	CP-24-14	1,500	
ADA4950-2YCP-EBZ		Evaluation Board			

[1] Z = RoHS Compliant Part.

NOTES

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