Data Sheet

ADAQ7768-1

24-Bit Single-Channel Precision µModule Data Acquisition System

FEATURES

- Highly-integrated data acquisition solution
- Seven programmable-gain options
  - G = 0.325, 0.65, 1.3, 2.6, 5.2, 10.4, 20.8 V/V
- Maximum input range of ±12.6 V differential
- Maximum input common-mode range of -12 V to +12 V
- Fourth-order AAF with maximum flatness and linear phase
- Full aliasing protection with 100 dB typical rejection
- Excellent device-to-device phase matching and drift
- Combined precision AC and DC performance:
  - Total system dynamic range up to 130 dB
  - −120 dB typical THD at 0.325 V/V gain
  - 100 dB minimum DC CMRR at 20.8 V/V gain
  - 25 pA maximum input bias current at 25°C
  - ±6 ppm typical INL
  - 5.5 ppm/°C maximum gain error drift
  - ±0.13° maximum device-to-device phase mismatch at 20 kHz
- Programmable output data rate, filter type, and latency
- Linear phase digital filter options:
  - Wideband low-ripple FIR filter (110 kHz maximum input bandwidth)
  - Sinc5 filter (1.024 MSPS, 198.4 kHz maximum input bandwidth, 4 µs maximum group delay)
  - Sinc3 filter (50 Hz/60 Hz rejection)
- Integrated LDO
- Built-in supply decoupling capacitors
- Configuration through pin strapping or SPI
- Digital interface optimized for isolated applications
- Suite of diagnostic check mechanisms
- Operating temperature range: −40°C to +85°C
- Packaging:12.00 mm × 6.00 mm 84-ball CSP_BGA with an 0.80 mm ball pitch
  - 10× footprint reduction vs. discrete solution

APPLICATIONS

- Universal input measurement platform
- Electrical test and measurement
- Sound and vibration, acoustic and material science research and development
- Control and hardware in loop verification
- Condition monitoring for predictive maintenance
- Audio test

FUNCTIONAL BLOCK DIAGRAM

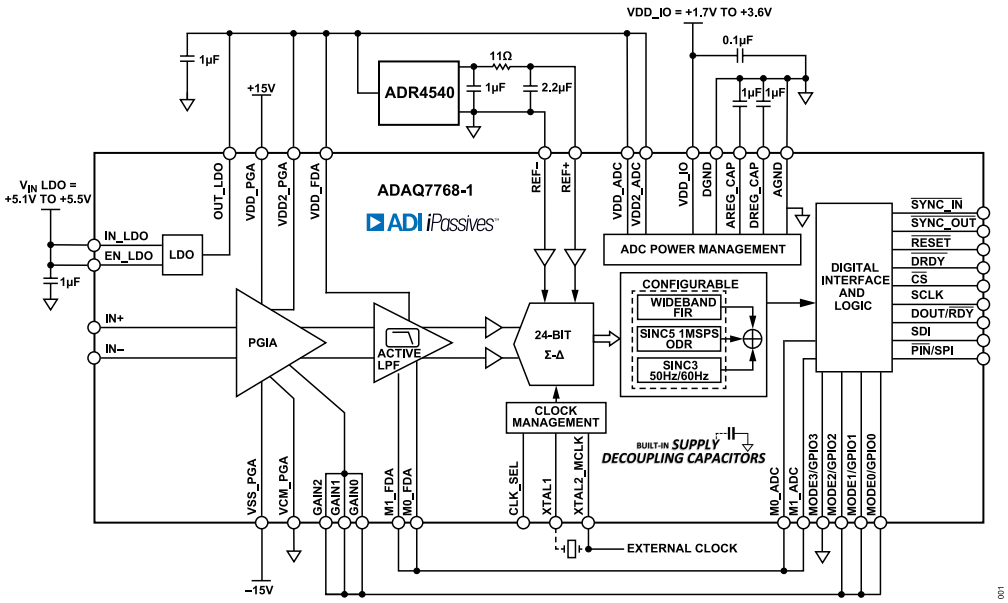

Figure 1. Functional Block Diagram

Protected by U.S. patents 10,680,633 B1 and 10,979,062 B2.

Rev. 0

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

3/2023—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADAQ7768-1 is a 24-bit precision data acquisition (DAQ) µModule® system that encapsulates signal conditioning, conversion, and processing blocks into one system-in-package (SiP) design for the rapid development of highly compact, high-performance precision DAQ systems.

The ADAQ7768-1 consists of:

- A low-noise, low-bias current, high-bandwidth programmable-gain instrumentation amplifier (PGIA) also capable of signal amplification and signal attenuation while maintaining high input impedance.
- A fourth-order, low-noise, linear phase anti-aliasing filter.
- A low-noise, low-distortion, high-bandwidth ADC driver plus an optional linearity boost buffer.
- A high-performance medium bandwidth 24-bit Σ-Δ ADC with programmable digital filter.
- A low-noise, low-dropout linear regulator.
- Reference buffers.
- Critical passive components required for the signal chain.

The ADAQ7768-1 supports fully differential input signal with a maximum range of ±12.6 V. It has an input common-mode voltage range of ±12 V with excellent common-mode rejection ratio (CMRR).

The input signal is fully buffered with very low input bias current of 2 pA typical. This allows easy input impedance matching and enables the ADAQ7768-1 to directly interface to sensors with high output impedance.

The seven pin-configurable gain settings offer additional system dynamic range and improved signal chain noise performance with input signals of lower amplitude.

A fourth-order low-pass analog filter combined with the user-programmable digital filter ensures the signal chain is fully protected against the high frequency noise and out-of-band tones presented at the input node from aliasing back into the band of interest. The analog low-pass filter is carefully designed to achieve high phase linearity and maximum in-band magnitude response flatness. Constructed with Analog Devices's iPASSIVES™ technology, the resistor network used within the analog low-pass filter possesses superior resistance matching in both absolute values and overtemperature. As a result, the signal chain performance is maintained with minimum drift overtemperature and the ADAQ7768-1 has a tight phase mismatch across devices.

A high-performance ADC driver amplifier ensures the full settling of the ADC input at the maximum sampling rate. The driver circuit is designed for minimum additive noise, error, and distortion while maintaining stability. The fully differential architecture helps to maximize the signal chain dynamic range.

The analog-to-digital converter (ADC) inside the ADAQ7768-1 is a high-performance, 24-bit precision, single-channel sigma-delta converter with excellent AC performance and DC precision, and the throughput rate of 256 kSPS from a 16.384 MHz MCLK.

An optional linearity boost buffer further improves the signal chain linearity.

The ADAQ7768-1 is specified with the input reference voltage of 4.096 V, but the device can support reference voltages ranging from VDD_ADC down to 1 V.

The ADAQ7768-1 has two types of reference buffers: a precharge reference buffer to ease the reference input driving requirement or a full reference buffer to provide high impedance reference input. Both buffers are optional and can be turned off through register configuration.

ADAQ7768-1 supports three clock input types: crystal, complementary-metal-oxide-semiconductor (CMOS), or low-voltage differential signaling (LVDS).

Three types of digital low pass filters are available on the ADAQ7768-1. The wideband filter offers a filter profile similar to an ideal brick wall filter, making it ideal for frequency analysis. The sinc5 filter offers a low latency path with a smooth step response while maintaining a good level of aliasing rejection. It also supports an output data rate up to 1.024 MSPS from a 16.384 MHz MCLK, making the sinc5 filter ideal for low latency data capturing and time domain analysis. The sinc3 filter supports a wide decimation ratio and can produce output data rate down to 50 SPS from a 16.384 MHz MCLK. This, combined with the simultaneous 50Hz/60Hz rejection post filter, makes the sinc3 filter especially useful for precision DC measurement. All the three digital filters on the ADAQ7768-1 are FIR filters with linear phase response. The bandwidths of the filters, which directly correspond to the bandwidth of the DAQ signal chain, are fully programmable through register configuration.

The ADAQ7768-1 also supports two device configuration methods. The user has the option to choose to configure the device through register write through its SPI, or through a simple hardware pin strapping method to configure the device to operate under a number of predefined modes.

A single SPI supports both the register access and sample data readback functions. The ADAQ7768-1 always acts as a SPI target. Multiple interface modes are supported with a minimum of three IO channels required to communicate with the device.

The ADAQ7768-1 also features a suite of internal diagnostic functions to detect a broad range of errors during operation to improve the system reliability.

The ADAQ7768-1 device has an operating temperature range of −40°C to +85°C and is available in a 12.00 mm × 6.00 mm 84-ball CSP_BGA package with an 0.80 mm ball pitch, which makes it ideal for multiple channel applications. The ADAQ7768-1 uses only 75 mm^2 of board space, 10 times less than the discrete solution that uses 750 mm^2.

SPECIFICATIONS

VDD_PGA = 15 V, VSS_PGA = -15 V, AGND = DGND = 0 V, input common-mode voltage = 0 V, IN_LDO = 5.1 V to 5.5 V, OUT_LDO = VDD2_PGA = VDD_FDA = VDD_ADC, VDD2_ADC = 2 V to 5.5 V, VDD_IO = 1.7 V to 3.6 V, REF+ = 4.096 V, REF− = 0 V, MCLK = SCLK = 16.384 MHz 50:50 duty cycle, f_{MOD} = MCLK/2, filter = wideband low ripple, decimation = 32, ODR = 256 kSPS, linearity boost buffer on, reference precharge buffers on, FDA = full power mode, T_A = - 40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG INPUT CHARACTERISTICS					
Input Bias Current	T_A = 25°C		2	25	pA
	−40°C < T_A < +85°C			100	pA
Input Offset Current	T_A = 25°C		2	25	pA
	−40°C < T_A < +85°C			60	pA
Input Voltage Range	Individual pin, IN+ and IN−	VSS_PGA + 3.25		VDD_PGA − 3	V
Input Common Mode Range[1]		−12		12	V
Analog Front-End Gain (AFE_GAIN)	Gain 0 mode		0.325		V/V
	Gain 1 mode		0.65		V/V
	Gain 2 mode		1.3		V/V
	Gain 3 mode		2.6		V/V
	Gain 4 mode		5.2		V/V
	Gain 5 mode		10.4		V/V
	Gain 6 mode		20.8		V/V
Full-Scale Input Range (FSR)	Differential IN+ to IN−				
	FSR = ±V_{REF}/AFE_GAIN				
	Gain 0 mode		±12.603		V
	Gain 1 mode		±6.302		V
	Gain 2 mode		±3.151		V
	Gain 3 mode		±1.575		V
	Gain 4 mode		±0.788		V
	Gain 5 mode		±0.394		V
	Gain 6 mode		±0.197		V
Common-Mode Rejection DC	DC to 60 Hz, RTI, V_{ICM} = ± 10 V				
Gain 0 Mode	T_A = 25°C		92		dB
	−40°C < T_A < +85°C	71			
Gain 1 Mode	T_A = 25°C		95		dB
	−40°C < T_A < +85°C	75			
Gain2 Mode	T_A = 25°C		97		dB
	−40°C < T_A < +85°C	78			
Gain 3 Mode	T_A = 25°C		102		dB
	−40°C < T_A < +85°C	84			
Gain 4 Mode	T_A = 25°C		108		dB
	−40°C < T_A < +85°C	90			
Gain 5 Mode	T_A = 25°C		114		dB
	−40°C < T_A < +85°C	95			
Gain 6 Mode	T_A = 25°C		120		dB
	−40°C < T_A < +85°C	100			
Common-Mode Rejection AC	AC CMRR (f = 1 kHz), RTI				
	Gain 0 mode		63		dB
	Gain 1 mode		65		dB
	Gain 2 mode		78		dB
	Gain 3 mode		78		dB

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	Gain 4 mode		90		dB
	Gain 5 mode		90		dB
	Gain 6 mode		113		dB
Input Current Noise					
Spectral Density	f = 10 kHz		1		fA/√Hz
Peak-to-Peak	f = 0.1 Hz to 10 Hz		100		fA p-p
Input Resistance	Common mode and differential		5×10^{12}		Ω
Input Capacitance			15		pF
OVERALL SYSTEM DC ACCURACY					
Gain Error	All gain modes, RTI, T_A = 25°C	−0.05	±0.005	+0.05	%
		−500	±50	+500	ppm
Gain Error Drift	All gain modes, RTI, endpoint method	−5.5	−1.6	+2.5	ppm/°C
Offset Error	RTI, T_A = 25°C				
	Gain 0 mode		±0.60	±5.8	mV
	Gain 1 mode		±0.30	±2.9	mV
	Gain 2 mode		±0.14	±2.1	mV
	Gain 3 mode		±0.06	±1.4	mV
	Gain 4 mode		±0.02	±1.0	mV
	Gain 5 mode		±0.01	±0.8	mV
	Gain 6 mode		±0.01	±0.7	mV
Offset Error Drift	RTI, endpoint method				
	Gain 0 mode	−61.0	−16.0	+29.0	µV/°C
	Gain 1 mode	−31.0	−8.0	+15.0	µV/°C
	Gain 2 mode	−16.0	−4.0	+8.0	µV/°C
	Gain 3 mode	−8.5	−2.2	+4.0	µV/°C
	Gain 4 mode	−5.0	−1.2	+2.5	µV/°C
	Gain 5 mode	−3.0	−0.7	+1.7	µV/°C
	Gain 6 mode	−2.2	−0.5	+1.3	µV/°C
Integral Nonlinearity (INL)	Endpoint method				
Gain 0 Mode	T_A = 25°C		±6		ppm of FSR
	−40°C < T < +85°C			±18	ppm of FSR
Gain 1 Mode	T_A = 25°C		±6		ppm of FSR
	−40°C < T_A < +85°C			±17	ppm of FSR
Gain 2 Mode	T_A = 25°C		±6		ppm of FSR
	−40°C < T_A < +85°C			±17	ppm of FSR
Gain 3 Mode	T_A = 25°C		±6		ppm of FSR
	−40°C < T_A < +85°C			±18	ppm of FSR
Gain 4 Mode	T_A = 25°C		±6		ppm of FSR
	−40°C < T_A < +85°C			±19	ppm of FSR
Gain 5 Mode	T_A = 25°C		±6		ppm of FSR
	−40°C < T_A < +85°C			±22	ppm of FSR
Gain 6 Mode	T_A = 25°C		±6.5		ppm of FSR
	−40°C < T_A < +85°C			±30	ppm of FSR
Low Frequency Noise	Sinc3 filter, ODR = 50 SPS, bandwidth = 15 Hz, shorted input, RTI, FDA = low power mode				
	Gain 0 mode		1.55		µV RMS
	Gain 1 mode		0.89		µV RMS
	Gain 2 mode		0.51		µV RMS

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	Gain 3 mode		0.33		µV RMS
	Gain4 mode		0.25		µV RMS
	Gain 5 mode		0.22		µV RMS
	Gain 6 mode		0.21		µV RMS
	Sinc3 filter, ODR = 50 SPS, bandwidth = 15 Hz, shorted input, RTI, FDA = full power mode				
	Gain 0 mode		3.02		µV RMS
	Gain 1 mode		1.55		µV RMS
	Gain 2 mode		0.89		µV RMS
	Gain 3 mode		0.48		µV RMS
	Gain 4 mode		0.30		µV RMS
	Gain 5 mode		0.25		µV RMS
	Gain 6 mode		0.22		µV RMS
Peak-to-Peak Resolution[2]	Sinc3 filter, ODR = 50 SPS, bandwidth = 15 Hz, shorted input, RTI, FDA = low power mode				
	Gain 0 mode		21.2		Bits
	Gain 1 mode		21.0		Bits
	Gain 2 mode		20.8		Bits
	Gain 3 mode		20.5		Bits
	Gain 4 mode		19.9		Bits
	Gain 5 mode		19.0		Bits
	Gain 6 mode		18.1		Bits
	Sinc3 filter, ODR = 50 SPS, bandwidth = 15 Hz, shorted input, RTI, FDA = full power mode				
	Gain 0 mode		20.3		Bits
	Gain 1 mode		20.2		Bits
	Gain 2 mode		20.0		Bits
	Gain 3 mode		19.9		Bits
	Gain 4 mode		19.6		Bits
	Gain 5 mode		18.9		Bits
	Gain 6 mode		18.0		Bits
OVERALL SYSTEM AC PERFORMANCE	Wideband low ripple FIR filter, ODR = 256 kSPS, bandwidth = 110.8 kHz, decimation by 32				
Dynamic Range[3]	Shorted input				
Gain0 Mode		105.8	106.7		dB
	Bandwidth = 1 Hz		157.2		dB
Gain 1 Mode		105.5	106.4		dB
	Bandwidth = 1 Hz		156.9		dB
Gain 2 Mode		104.7	105.7		dB
	Bandwidth = 1 Hz		156.1		dB
Gain 3 Mode		103.7	104.8		dB
	Bandwidth = 1 Hz		155.3		dB
Gain 4 Mode		101.5	102.7		dB
	Bandwidth = 1 Hz		153.1		dB
Gain 5 Mode		97.3	98.9		dB
	Bandwidth = 1 Hz		149.3		dB

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Gain6 Mode		92.1	93.8		dB
	Bandwidth = 1 Hz		144.1		dB
	total system		130		dB
Noise Spectral Density	RTI, shorted input, at 1 kHz				
	Gain 0 mode		122		nV/√Hz
	Gain 1 mode		63.8		nV/√Hz
	Gain 2 mode		35		nV/√Hz
	Gain 3 mode		19		nV/√Hz
	Gain 4 mode		12.3		nV/√Hz
	Gain 5 mode		9.5		nV/√Hz
	Gain 6 mode		8.6		nV/√Hz
Integrated Voltage Noise	RTI, shorted input				
	Gain 0 mode		41.2		µV RMS
	Gain 1 mode		21.4		µV RMS
	Gain 2 mode		11.6		µV RMS
	Gain 3 mode		6.4		µV RMS
	Gain 4 mode		4.1		µV RMS
	Gain 5 mode		3.1		µV RMS
	Gain 6 mode		2.8		µV RMS
Signal-to-Noise Ratio (SNR)	−0.5 dBFS, sine input, 1 kHz input tone				
	Gain 0 mode	103.9	105.9		dB
	Gain 1 mode	102.2	104.9		dB
	Gain 2 mode	101.8	104.4		dB
	Gain 3 mode	100.5	103.4		dB
	Gain 4 mode	98.5	100.8		dB
	Gain 5 mode	96.1	98.0		dB
	Gain 6 mode	91.2	93.1		dB
Total Harmonic Distortion (THD)	−0.5 dBFS, sine input, 1 kHz input tone				
	Gain 0 mode		−120		dB
	Gain 1 mode		−120		dB
	Gain 2 mode		−120		dB
	Gain 3 mode		−120		dB
	Gain 4 mode		−120		dB
	Gain 5 mode		−120		dB
	Gain 6 mode		−115		dB
Signal-to-Noise and Distortion Ratio (SINAD)	−0.5 dBFS, sine input, 1 kHz input tone				
	Gain 0 mode	103.8			dB
	Gain 1 mode	102.1			dB
	Gain 2 mode	101.7			dB
	Gain 3 mode	100.4			dB
	Gain 4 mode	98.4			dB
	Gain 5 mode	96.0			dB
	Gain 6 mode	91.1			dB
Spurious-Free Dynamic Range (SFDR)	−0.5 dBFS, sine input, 1 kHz input tone				
	Gain 0 mode		121		dBc
	Gain 1 mode		121		dBc
	Gain 2 mode		121		dBc
	Gain 3 mode		121		dBc
	Gain 4 mode		121		dBc

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	Gain 5 mode		121		dBc
	Gain 6 mode		116		dBc
Intermodulation Distortion (IMD)	f_{IN_A} = 19.5 kHz, f_{IN_B} = 20.5 kHz				
	Gain 0 mode second order		−115		dB
	Gain 0 mode third order		−105		dB
	Gain 2 mode second order		−115		dB
	Gain 2 mode third order		−115		dB
	Gain 6 mode second order		−111		dB
	Gain 6 mode third order		−95		dB
ANALOG FRONT-END MAGNITUDE AND PHASE PERFORMANCE[4]					
Analog Group Delay	f_{IN} = 20 kHz, Gain0 mode		1.011		µs
	f_{IN} = 20 kHz, Gain6 mode		1.070		µs
Phase Angle Mismatch Over Gain	Sine wave, f_{IN} = 20 kHz, single device, normalized to Gain 0, T_A = 25°C				
	Gain 1 mode	−0.030	−0.019	−0.008	Degrees
	Gain 2 mode	−0.038	−0.007	0.024	Degrees
	Gain 3 mode	−0.055	−0.023	0.008	Degrees
	Gain 4 mode	0.000	0.031	0.062	Degrees
	Gain 5 mode	0.084	0.115	0.146	Degrees
	Gain 6 mode	0.363	0.427	0.491	Degrees
Phase Angle Drift	f_{IN} = 20 kHz				
	Gain 0 mode	0.10	0.73	1.37	m°/°C
	Gain 1 mode	0.16	0.77	1.39	m°/°C
	Gain 2 mode	0.20	0.83	1.46	m°/°C
	Gain 3 mode	0.25	0.88	1.51	m°/°C
	Gain 4 mode	0.34	1.00	1.65	m°/°C
	Gain 5 mode	0.55	1.24	1.94	m°/°C
	Gain 6 mode	0.80	1.68	2.56	m°/°C
Device-to-Device Phase Angle Mismatch	f_{IN} = 20 kHz, typical = ±1 σ, T_A = 25°C				
	Gain 0 mode	−0.11	±0.018	+0.11	Degrees
	Gain 1 mode	−0.11	±0.017	+0.11	Degrees
	Gain 2 mode	−0.11	±0.017	+0.11	Degrees
	Gain 3 mode	−0.11	±0.017	+0.11	Degrees
	Gain 4 mode	−0.11	±0.017	+0.11	Degrees
	Gain 5 mode	−0.11	±0.017	+0.11	Degrees
	Gain 6 mode	−0.13	±0.021	+0.13	Degrees
Device-to-Device Phase Angle Mismatch Drift	f_{IN} = 20 kHz, typical = change in |1σ| per °C				
	Gain 0 mode		−21	−126	µ°/°C
	Gain 1 mode		−19	−112	µ°/°C
	Gain 2 mode		−16	−97	µ°/°C
	Gain 3 mode		−16	−98	µ°/°C
	Gain 4 mode		−19	−114	µ°/°C
	Gain 5 mode		−25	−149	µ°/°C
	Gain 6 mode		−30	−179	µ°/°C
Magnitude Flatness	f_{IN} = 20 kHz		−2.3		mdB
	f_{IN} = 100 kHz		−20		mdB
Alias Rejection	All gain modes, −20 dBFS input signal				
	at 16.384 MHz		100		dB

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	at 13.107 MHz		100		dB
ADC SPEED AND PERFORMANCE					
Output Data Rate (ODR)[5]					
	Wideband low ripple FIR	1		256	kSPS
	Sinc5	1		1024	kSPS
	Sinc3	0.0125		256	kSPS
No Missing Codes	Wideband low ripple FIR filter, decimation ratio ≥ 32	24			Bits
	Sinc5 filter, decimation ratio ≥ 32	24			Bits
	Sinc3 filter, decimation ratio ≥ 64	24			Bits
Data Output Coding		Twos complement, MSB first			
REFERENCE INPUT CHARACTERISTICS					
REFIN Voltage	REFIN = (REF+) − (REF−)	1		VDD_ADC − AGND	V
Absolute REFIN Voltage Limit	Reference unbuffered	AGND − 0.05		VDD_ADC + 0.05	V
	Reference buffer on	AGND		VDD_ADC	V
	Reference precharge buffer on	AGND		VDD_ADC	V
Average REFIN Current	Reference unbuffered		±80		uA/V
	Reference buffer on		±300		nA
	Reference precharge buffer on		±20		uA
Average REFIN Current Drift	Reference unbuffered		±1.7		nA/V/C
	Reference buffer on		125		nA/C
	Reference precharge buffer on		4		nA/C
Common Mode Rejection	Up to 10 MHz		100		dB
DIGITAL FILTER RESPONSE					
Wideband Low Ripple FIR Filter					
Decimation Rate	6 selectable decimation rates	32		1024	
Output Data Rate				256	kSPS
Group Delay	Latency		34/ODR		Sec
Settling Time	Complete settling		68/ODR		Sec
Pass-Band Ripple				±0.005	dB
Pass-Band	−0.005 dB		0.4 × ODR		Hz
	−0.1 dB pass-band		0.409 × ODR		
	−3 dB bandwidth		0.433 × ODR		Hz
Stop-Band Frequency	Attenuation > 105 dB		0.499 × ODR		Hz
Stop-Band Attenuation		105			dB
Sinc5 Filter					
Decimation Rate	8 selectable decimation rates	8		1024	
Output Data Rate				1.024	MSPS
Group Delay	Latency		< 3/ODR		Sec
Settling Time	Complete settling		< 6/ODR		Sec
Pass Band	−0.1dB bandwidth		0.0376 × ODR		Hz
	−3dB bandwidth		0.204 × ODR		Hz
Sinc3 Filter					
Decimation Rate	1024 decimation rates	32		185,280	
Output Data Rate				256	kSPS
Group Delay	Latency		2/ODR		Sec

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Settling Time	Complete settling to reject 50 Hz		60		ms
Pass-Band	−0.1dB bandwidth		0.0483 × ODR		Hz
	−3dB bandwidth		0.2617 × ODR		Hz
CLOCK					
External Clock MCLK		0.6	16.384	17	MHz
Internal Clock MCLK			16.384		MHz
Input High Voltage	See logic input parameter.				
Duty Cycle	16.384 MHz MCLK	25:75	50:50	25:75	%
MCLK Logic Low Pulse Width		16			ns
MCLK Logic High Pulse Width		16			ns
Crystal Frequency		8	16	17	MHz
Crystal Start-Up Time	Clock output valid		2		ms
ADC RESET					
ADC Start-Up Time after Reset	Reset rising edge to first DRDY, PIN mode, decimate by 8		100		µs
Minimum RESET Low Pulse Width		0.0001		100	ms
LOGIC INPUTS	Applies to all logic inputs, unless specified otherwise, voltage referenced to AGND.				
Input High Voltage, V_{INH}	1.7 V ≤ VDD_IO ≤ 1.9 V	0.65 × VDD_IO			V
	2.22 V ≤ VDD_IO ≤ 3.6 V	0.65 × VDD_IO			V
Input Low Voltage, V_{INL}	1.7 V ≤ VDD_IO ≤ 1.9 V			0.35 × VDD_IO	V
	2.22 V ≤ VDD_IO ≤ 3.6 V			0.7	V
Hysteresis	2.22 V ≤ VDD_IO ≤ 3.6 V	0.08		0.25	V
	1.7 V ≤ VDD_IO < 1.9 V	0.04		0.2	V
Leakage Current	Excluding $\overline{\text{RESET}}$ pin	−10	+0.05	+10	µA
	$\overline{\text{RESET}}$ pin pullup resistor		1		kΩ
GAIN0, GAIN1, GAIN2	Voltage referenced to AGND				
Input High Voltage		1.5			V
Input Low Voltage				0.6	V
Input Current	GAIN 0, GAIN 1, GAIN 2 = 5 V		8	12	µA
EN_LDO	Voltage referenced to AGND				
Input High Voltage	5.1 V ≤ IN_LDO ≤ 5.5 V	1.2			V
Input Low Voltage	5.1 V ≤ IN_LDO ≤ 5.5 V			0.4	V
Input Current	EN_LDO = IN_LDO or GND		0.1		µA
LOGIC OUTPUTS					
Output High Voltage	2.2 V ≤ VDD_IO < 3.6 V, I_{SOURCE} = 500 µA, LV_BOOST_off	0.8 × VDD_IO			V
	1.7 V ≤ VDD_IO < 1.9 V, I_{SOURCE} = 200 µA, LV_BOOST_on	0.8 × VDD_IO			V
Output Low Voltage	2.2 V ≤ VDD_IO < 3.6 V, I_{SINK} = 1 mA, LV_BOOST_off			0.4	V
	1.7 V ≤ VDD_IO < 1.9 V, I_{SINK} = 400 µA, LV_BOOST_on			0.4	V
Leakage Current	Floating state	−10		+10	µA
Output Capacitance	Floating state		10		pF
LDO CHARACTERISTIC					
Input Voltage Range		5.1		5.5	V
IN_LDO Supply Current	OUT_LDO load current = 20 mA		80		µA

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OUT_LDO Voltage		4.80	4.90	5.03	V
Load Regulation	I_{OUT} = 1 mA to 20 mA		0.0005		%/mA
Dropout Voltage[6]	I_{OUT} = 20 mA		3		mV
Start-Up Time[7]			350		µs
Current Limit Threshold			500		mA
Thermal Shutdown Threshold			150		°C
Thermal Shutdown Hysteresis			15		°C
POWER REQUIREMENTS					
VDD_PGA	Referenced to AGND	4.5		16	V
VSS_PGA	Referenced to AGND	−16		−4.5	V
VDD2_PGA	Referenced to AGND	4.75		5.5	V
VDD_FDA	Referenced to AGND	4.75	5	5.5	V
VDD_ADC	Referenced to AGND	4.75	5	5.5	V
VDD2_ADC	Referenced to AGND	2	2.5	5.5	V
VDD_IO	Referenced to AGND	1.7	1.8	3.6	V
POWER SUPPLY REJECTION	Referred to output (RTO), DC to 100 Hz, V_{STEP} = 0.4 V p-p				
VDD_PGA and VSS_PGA	Gain 0 mode		112		dB
	Gain 6 mode		130		dB
VDD2_PGA			124		dB
VDD_FDA			116		dB
VDD_ADC			105		dB
VDD2_ADC			124		dB
VDD_IO			104		dB
LDO			124		dB
POWER SUPPLY CURRENT					
VDD_PGA	IN+ = IN− = AGND		3.1		mA
	Full-scale 1 kHz sine input with common mode = AGND, Gain 0 mode		6.5		mA
	Full-scale 1 kHz sine input with common mode = AGND, Gain 6 mode		3.4		mA
	Full-scale DC input with common mode = AGND, Gain 0 mode		7.6		mA
	Full-scale DC input with common mode = AGND, Gain 6 mode		4.1		mA
	Standby		230		µA
VDD2_PGA	IN+ = IN− = AGND		0.75		mA
	Full-scale 1 kHz sine input with common mode = AGND, Gain 0 mode		2.4		mA
	Full-scale 1 kHz sine input with common mode = AGND, Gain 6 mode		1.1		mA
	Full-scale DC input with common mode = AGND, Gain 0 mode		3.3		mA
	Full-scale DC input with common mode = AGND, Gain 6 mode		2		mA
	Standby		1		µA
VSS_PGA	IN+ = IN− = AGND		−5.9		mA
	Full-scale 1 kHz sine input with common mode = AGND, Gain 0 mode		−10.3		mA

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	Full-scale 1 kHz sine input with common mode = AGND, Gain 6 mode		−6.4		mA
	Full-scale DC input with common mode = AGND, Gain 0 mode		−13		mA
	Full-scale DC input with common mode = AGND, Gain 6 mode		−8		mA
	Standby		−210		µA
VDD_FDA	IN+ = IN- = AGND, low power		3.4		mA
	IN+ = IN- = AGND, full power		5.6		mA
	Full scale 1 kHz sine input with common mode = AGND, low power		3.7		mA
	Full scale 1 kHz sine input with common mode = AGND, full power		5.8		mA
	Full scale DC input with common mode = AGND, low power		4.2		mA
	Full-scale DC input with common mode = AGND, full power		6.3		mA
	Standby		90		µA
VDD_ADC	Linearity boost buffer on, reference precharge buffer on		6.3		mA
	Linearity boost buffer off, reference precharge buffers off		2.4		mA
	Standby		205		µA
VDD2_ADC			4.7		mA
	Standby		30		µA
VDD_IO					
Sinc3 Filter			3.7		mA
Sinc5 Filter			3.7		mA
Wideband Low Ripple FIR Filter			9.5		mA
Standby			380		µA
POWER DISSIPATION	External CMOS MCLK, VDD2_ADC = VDD_IO = 3.3 V				
Full Operating Mode					
Sinc3 Filter	IN+ = IN− = AGND		223		mW
Sinc5 Filter	IN+ = IN− = AGND		224		mW
Wideband Low Ripple FIR Filter	IN+ = IN− = AGND		243		mW
	Full-scale 1 kHz sine input with common mode = AGND, Gain 0 mode		359		mW
	Full-scale 1 kHz sine input with common mode = AGND, Gain 6 mode		277		mW
	Full-scale DC input with common mode = AGND, Gain 0 mode		455		mW
	Full-scale DC input with common mode = AGND, Gain 6 mode		312		mW
Standby Mode			0.96		mW

[1] See the Common-Mode Input Range section for more details.

[2] See Terminology for Peak-to-Peak Resolution. Noise used in calculation is listed under the "Low Frequency Noise" specification.

[3] See the Noise Performance and Resolution section for dynamic range performance across decimation factor and throughput.

[4] See the Calculations on AFE Phase Performance section for AFE performance, terminology, and calculation.

SPECIFICATIONS

[5] Output data rate (ODR) ranges refer to the programmable decimation rates available on the ADAQ7768-1 for a fixed MCLK of 16.384 MHz. Varying MCLK allows a wider variation of ODR. See the ADC Speed and Performance section for suggestion on the ODR speed to achieve optimum performance.

[6] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages greater than 2.3 V.

[7] Start-up time is defined as the time between the rising edge of EN to V_{OUT} being at 90% of its nominal value.

TIMING SPECIFICATIONS

VDD_ADC = 4.5 V to 5.5 V, VDD2_ADC = 2.0 V to 5.5 V, VDD_IO = 2.2 V to 3.6 V, AGND = DGND = 0 V, input logic 0 = 0 V, input logic 1 = VDD_IO, and load capacitance (C_{LOAD}) = 20 pF, LV_BOOST bit (Bit 7, INTERFACE_FORMAT register (Register 0x14) disabled, unless otherwise noted.

These specifications were sample tested during the initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of VDD_IO and timed from a voltage level of VDD_IO/2). See Figure 2 to Figure 8 for the timing diagrams.

These specifications are not production tested, but are supported by characterization data at initial product release.

Table 2.

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
MCLK	Frequency			16.384	17	MHz
t_{MCLK_HIGH}	MCLK high time		16			ns
t_{MCLK_LOW}	MCLK low time		16			ns
f_{MOD}	Modulator frequency	MCLK_DIV[1:0] = 11		MCLK/2		Hz
		MCLK_DIV[1:0] = 10		MCLK/4		Hz
		MCLK_DIV[1:0] = 01		MCLK/8		Hz
		MCLK_DIV[1:0] = 00		MCLK/16		Hz
$t_{\overline{DRDY}}$	Conversion period	Rising $\overline{DRDY}$ edge to next rising $\overline{DRDY}$ edge, continuous conversion mode		f_{MOD}/DEC_RATE		Hz
$t_{\overline{DRDY}\_HIGH}$	$\overline{DRDY}$ high time	t_{MCLK} = 1/MCLK	t_{MCLK} − 5	1 × t_{MCLK}		ns
$t_{MCLK\_\overline{DRDY}}$	MCLK to $\overline{DRDY}$	Rising MCLK edge to $\overline{DRDY}$ rising edge	10	13	18	ns
$t_{MCLK\_\overline{RDY}}$	MCLK to $\overline{RDY}$ indicator on the DOUT/$\overline{RDY}$ pin	Rising MCLK edge to $\overline{RDY}$ falling edge	10	13	18	ns
t_{UPDATE}	ADC data update	Time before $\overline{DRDY}$ rising edge where the ADC conversion register updates, single conversion read		1 × t_{MCLK}		ns
$t_{\overline{START}}$	$\overline{START}$ pulse width		1.5 × t_{MCLK}			ns
$t_{MCLK\_\overline{SYNC\_OUT}}$	MCLK to $\overline{SYNC\_OUT}$	Falling MCLK to falling $\overline{SYNC\_OUT}$			t_{MCLK} + 16	ns
t_{SCLK}	SCLK period		50			ns
t_1	$\overline{CS}$ falling to SCLK falling		0			ns
t_2	$\overline{CS}$ falling to data output enable				6	ns
t_3	SCLK falling edge to data output valid			10	15	ns
t_4	Data output hold time after SCLK falling edge		4			ns
t_5	SDI setup time before SCLK rising edge		3			ns
t_6	SDI hold time after SCLK rising edge		8			ns
t_7	$\overline{CS}$ high time	4-wire interface	10			ns
t_8	SCLK high time		20			ns
t_9	SCLK low time		20			ns
t_{10}	SCLK rising edge to $\overline{DRDY}$ high	Single conversion read only; time from last SCLK rising edge to $\overline{DRDY}$ high	1 × t_{MCLK}			ns
t_{11}	SCLK rising edge to $\overline{CS}$ rising edge		6			ns
t_{12}	$\overline{CS}$ rising edge to DOUT/$\overline{RDY}$ output disable		4		7	ns

SPECIFICATIONS

Table 2. (Continued)

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_{13}	DOUT/$\overline{RDY}$ indicator pulse width	In continuous read mode with $\overline{RDY}$ on, DOUT enabled, with SCLK idling high		1 × t_{MCLK}		ns
t_{14}	$\overline{CS}$ falling edge to SCLK rising edge		2			ns
t_{15}	$\overline{SYNC\_IN}$ setup time before MCLK rising edge		2			ns
t_{16}	$\overline{SYNC\_IN}$ pulse width		1.5 × t_{MCLK}			ns
t_{17}	SCLK rising edge to $\overline{RDY}$ indicator rising edge	In continuous read mode with $\overline{RDY}$ enabled on DOUT	1			ns
t_{18}	$\overline{DRDY}$ rising edge to SCLK falling edge	In continuous read mode with $\overline{RDY}$ enabled on DOUT	8			ns

1.8 V TIMING SPECIFICATIONS

VDD_ADC = 4.5 V to 5.5 V, VDD2_ADC = 2 V to 5.5 V, VDD_IO = 1.7 V to 1.9 V, AGND = DGND = 0 V, input logic 0 = 0 V, input logic 1 = VDD_IO, and C_{LOAD} = 20 pF, LV_BOOST bit (Bit 7, INTERFACE_FORMAT register (Register 0x14) enabled, unless otherwise noted.

These specifications were sample tested during the initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of VDD_IO and timed from a voltage level of VDD_IO/2). See Figure 2 to Figure 8 for the timing diagrams.

These specifications are not production tested but are supported by characterization data at initial product release.

Table 3.

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
MCLK	Frequency			16.384	17	MHz
t_{MCLK_HIGH}	MCLK high time		16			ns
t_{MCLK_LOW}	MCLK low time		16			ns
f_{MOD}	Modulator frequency	MCLK_DIV[1:0] = 11		MCLK/2		Hz
		MCLK_DIV[1:0] = 10		MCLK/4		Hz
		MCLK_DIV[1:0] = 01		MCLK/8		Hz
		MCLK_DIV[1:0] = 00		MCLK/16		Hz
$t_{\overline{DRDY}}$	Conversion period	Rising $\overline{DRDY}$ edge to next rising $\overline{DRDY}$ edge, continuous conversion mode		f_{MOD}/DEC_RATE		Hz
$t_{\overline{DRDY}\_HIGH}$	$\overline{DRDY}$ high time	t_{MCLK} = 1/MCLK	t_{MCLK} − 5	1 × t_{MCLK}		ns
$t_{MCLK\_\overline{DRDY}}$	MCLK to $\overline{DRDY}$	Rising MCLK edge to $\overline{DRDY}$ rising edge	13	19	25	ns
$t_{MCLK\_\overline{RDY}}$	MCLK to $\overline{RDY}$ indicator on the DOUT/$\overline{RDY}$ pin	Rising MCLK edge to $\overline{RDY}$ falling edge	13	19	25	ns
t_{UPDATE}	ADC data update	Time before $\overline{DRDY}$ rising edge where the ADC conversion register updates.		1 × t_{MCLK}		ns
$t_{\overline{START}}$	$\overline{START}$ pulse width		1.5 × t_{MCLK}			ns
$t_{MCLK\_\overline{SYNC\_OUT}}$	MCLK to $\overline{SYNC\_OUT}$	Falling MCLK to falling $\overline{SYNC\_OUT}$, see the Synchronization of Multiple ADAQ7768-1 Devices section.			t_{MCLK} + 31	ns
t_{SCLK}	SCLK period		50			ns
t_1	$\overline{CS}$ falling to SCLK falling		0			ns
t_2	$\overline{CS}$ falling to data output enable				11	ns
t_3	SCLK falling edge to data output valid			14	19	ns
t_4	Data output hold time after SCLK falling edge		7			ns
t_5	SDI setup time before SCLK rising edge		3			ns
t_6	SDI hold time after SCLK rising edge		8			ns
t_7	$\overline{CS}$ high time	4-wire interface	10			ns
t_8	SCLK high time		23			ns

SPECIFICATIONS

Table 3. (Continued)

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_9	SCLK low time		23			ns
t_{10}	SCLK rising edge to $\overline{DRDY}$ high	Time from last SCLK rising edge to DRDY high; if this is exceeded, conversion N + 1 is missed; single conversion read.	1 × t_{MCLK}			ns
t_{11}	SCLK rising edge to $\overline{CS}$ rising edge		6			ns
t_{12}	$\overline{CS}$ rising edge to DOUT/$\overline{RDY}$ output disable		7.5		13	ns
t_{13}	DOUT/$\overline{RDY}$ indicator pulse width	In the continuous read mode with $\overline{RDY}$ on, DOUT enabled, with SCLK idling high.		1 × t_{MCLK}		ns
t_{14}	$\overline{CS}$ falling edge to SCLK rising edge		2.5			ns
t_{15}	$\overline{SYNC\_IN}$ setup time before MCLK rising edge		2			ns
t_{16}	$\overline{SYNC\_IN}$ pulse width		1.5 × t_{MCLK}			ns
t_{17}	SCLK rising edge to $\overline{RDY}$ indicator rising edge	In the continuous read mode with $\overline{RDY}$ on, DOUT enabled.	5.5			ns
t_{18}	$\overline{DRDY}$ rising edge to SCLK falling edge	In the continuous read mode with $\overline{RDY}$ on, DOUT enabled.	15			ns

Timing Diagrams

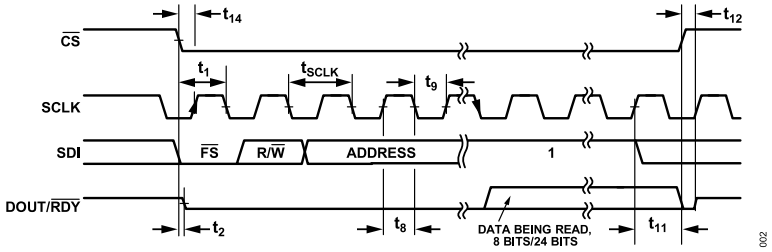

Figure 2. SPI Read Timing Diagram

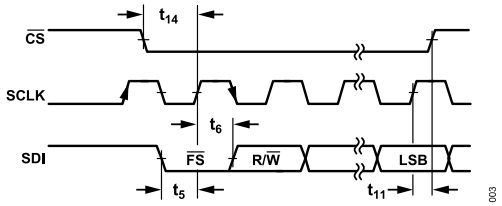

Figure 3. SPI Write Timing Diagram

SPECIFICATIONS

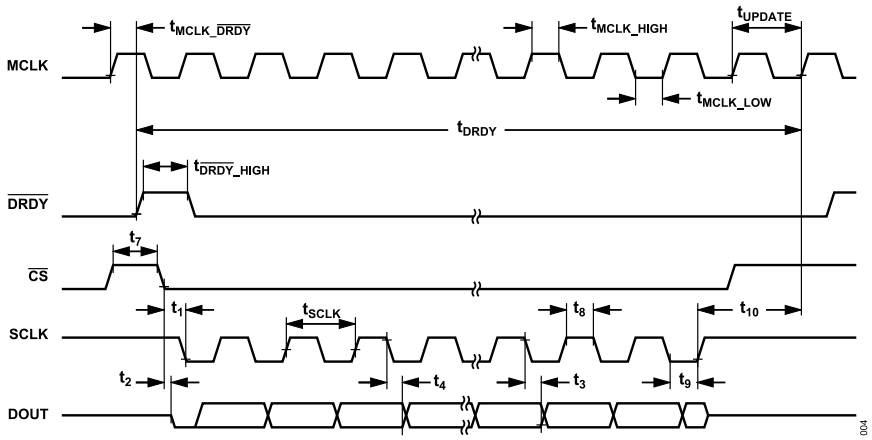

Figure 4. Reading Conversion Result in Continuous Conversion Mode (CS Toggling)

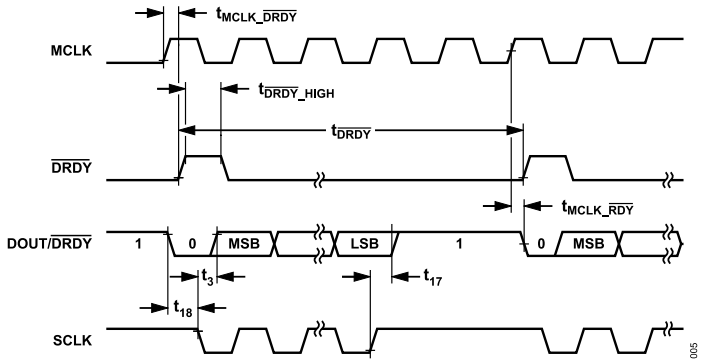

Figure 5. Reading Conversion Result in Continuous Conversion Mode, Continuous Read Mode with RDY Enabled (CS Held Low)

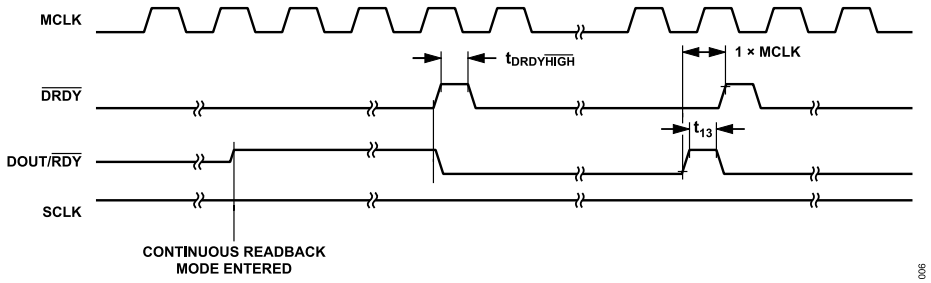

Figure 6. DOUT/RDY Behavior Without SCLK Applied

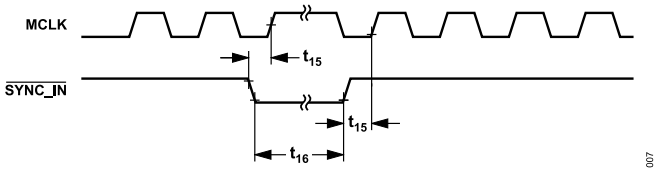

Figure 7. Synchronous SYNC_IN Pulse

SPECIFICATIONS

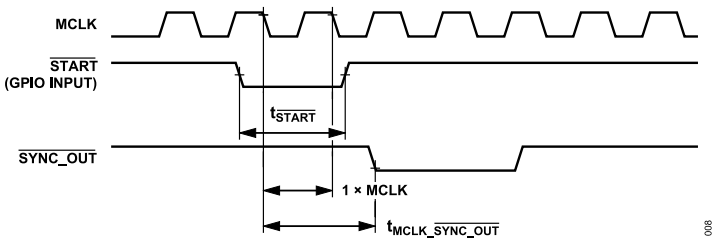

Figure 8. Asynchronous START and SYNC_OUT

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
VDD_PGA to AGND	+20 V
VSS_PGA to AGND	−20 V
VDD2_PGA to AGND	−0.3 V to +6.5 V
IN+, IN−	VSS_PGA to VDD_PGA
GAIN 0, GAIN 1, GAIN 2	VSS_PGA to VDD_PGA
VCM_PGA	VSS_PGA to VDD2_PGA
VDD_FDA to VDD_ADC	−0.3 V to +0.3 V
VDD_FDA to AGND	−0.3 V to +6.5 V
IN_LDO to AGND	−0.3 V to +6.5 V
EN_LDO to AGND	−0.3 V to +6.5 V
OUT_LDO to AGND	−0.3 V to IN_LDO
VDD_ADC to AGND	−0.3 V to +6.5 V
VDD2_ADC to AGND	−0.3 V to +6.5 V
VDD_IO to DGND	−0.3 V to +6.5 V
DGND to AGND	−0.3 V to +0.3V
VDD_IO, DREG_CAP to DGND (VDD_IO tied to DREG_CAP for 1.8 V operation)	−0.3 V to +2.25 V
REF+, REF− to AGND	−0.3 V to VDD_ADC + 0.3 V
Digital Input Voltage to DGND	−0.3 V to VDD_IO + 0.3 V
Digital Output Voltage to DGND	−0.3 V to VDD_IO + 0.3 V
XTAL1 to DGND	−0.3 V to +2.1 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Pb-Free Temperature, Soldering Reflow (10 sec to 30 sec)	260°C
Maximum Package Classification Temperature	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 5. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC_TOP}	θ_{JC_BOTTOM}	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
BC-84-4	45.2	38.7	26.1	33.9	20.9	31.2	°C/W

[1] Test Condition 1: Thermal impedance simulated values are based on the use of a 2S2P with vias JEDEC PCB excluding the θ_{JC_TOP}, which uses 1S0P JEDEC PCB.

θ_{JA} is the natural convection, junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC_TOP} is the top junction to case thermal resistance.

θ_{JC_BOTTOM} is the bottom junction to case thermal resistance.

θ_{JB} is the junction-to-board thermal resistance.

Ψ_{JT} is the junction-to-top thermal characterization.

Ψ_{JB} is the junction-to-board thermal characterization.

Thermal resistance values specified in Table 5 are simulated based on JEDEC specifications (unless specified otherwise) and must be used in compliance with JESD51-12.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADAQ7768-1

Table 6. ADAQ7768-1, 84-Ball CSP_BGA

ESD Model	Withstand Voltage (V)	Class
HBM	±4000	3A
FICDM	±500	C2A

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

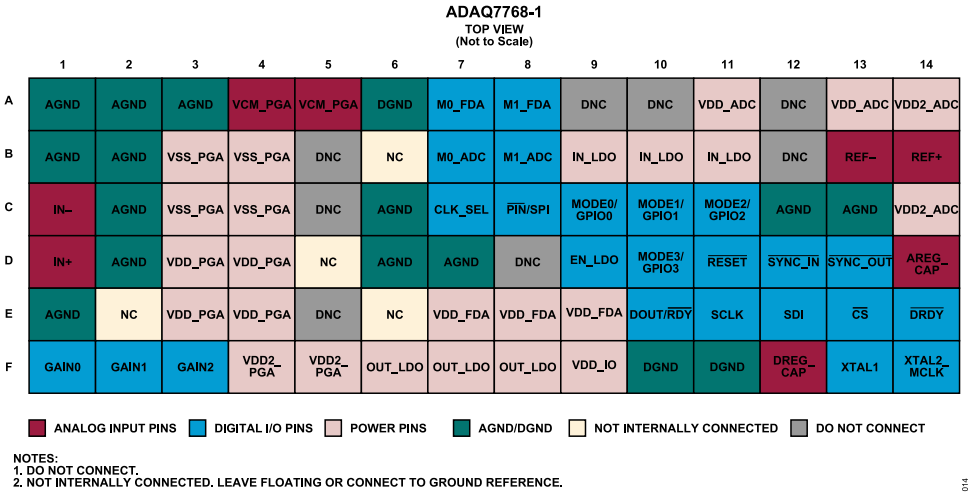

Figure 9. Pin Configuration

Table 7. ADAQ7768-1 Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1, A2, A3	AGND	P	Ground Reference for VDD_FDA, IN_LDO, VDD_ADC, and VDD2_ADC Supplies. Connect to system ground for normal operation.
A4, A5	VCM_PGA	AI	Output Common-Mode Voltage Control Input of the PGIA. Connect to AGND for normal operation.
A6	DGND	P	Ground Reference for VDD_IO Supplies. Connect to system ground for normal operation.
A7	M0_FDA	DI	FDA Mode Control Input 0. Connect to M0_ADC for normal operation.
A8	M1_FDA	DI	FDA Mode Control Input 1. Connect to M1_ADC for normal operation.
A9, A10	DNC		Do Not Connect.
A11, A13	VDD_ADC	P	ADC Analog Supply Voltage. Referenced to AGND. Connect to OUT_LDO if using on-device LDO, else connect it to a single power source that also supplies the VDD2_PGA and VDD_FDA pins.
A12	DNC		Do Not Connect.
A14	VDD2_ADC	P	ADC Secondary Analog Supply Voltage. Referenced to AGND.
B1, B2	AGND	P	Ground Reference for VDD_FDA, IN_LDO, VDD_ADC, and VDD2_ADC Supplies. Connect to system ground for normal operation.
B3, B4	VSS_PGA	P	PGIA Input and Output Stage Negative Supply. Referenced to AGND.
B5	DNC		Do Not Connect.
B6	NC		Not Internally Connected. Leave floating or connect to ground reference.
B7	M0_ADC	DO	FDA Mode Control Output 0. Connect to M0_FDA for FDA full power mode.
B8	M1_ADC	DO	FDA Mode Control Output 1. Connect to M1_FDA for normal operation.
B9, B10, B11	IN_LDO	P	On-Device LDO Supply Input. Bypass IN_LDO to AGND with a capacitor of at least 1 µF.
B12	DNC		Do Not Connect.
B13	REF−	AI	ADC Reference Input Negative Node. Connect to AGND for normal operation.
B14	REF+	AI	ADC Reference Input Positive Node.
C1	IN-	AI	Signal Input, Inverting.
C2	AGND	P	Ground Reference for VDD_FDA, IN_LDO, VDD_ADC, and VDD2_ADC Supplies. Connect to system ground for normal operation.
C3, C4	VSS_PGA	P	PGIA Input and Output Stage Negative Supply. Referenced to AGND.
C5	DNC		Do Not Connect.
C6	AGND		Connect to System Ground for Normal Operation.
C7	CLK_SEL	DI	ADC Clock Source Selection Input.
			In pin control mode, 0 = CMOS clock option. Apply external CMOS clock signal to XTAL2_MCLK pin, tie XTAL1 pin to DGND, and 1 = crystal option. Connect external crystal across the XTAL1 and XTAL2_MCLK pins.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 7. ADAQ7768-1 Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
			In SPI control mode, tie CLK_SEL pin to DGND. Select the clock source through register access. The LVDS clock option is available only in SPI control mode.
C8	$\overline{\text{PIN}}$/SPI	DI	Device Mode Selection Input. 0: pin mode operation. Control and configure device operation through configuration pin logic. 1: control and configuration through register over SPI.
C9	MODE0/GPIO0	DI/O	Multifunction Pin. In pin control mode, MODE0 is the Pin Control Operating Profile Selection Input 0. In SPI control mode, GPIO0 has its logic level referenced to the VDD_IO and DGND pins.
C10	MODE1/GPIO1	DI/O	Multifunction Pin. In pin control mode, MODE1 is the Pin Control Operating Profile Selection Input 1. In SPI control mode, GPIO1 has its logic level referenced to the VDD_IO and DGND pins.
C11	MODE2/GPIO2	DI/O	Multifunction Pin. In pin control mode, MODE2 is the Pin Control Operating Profile Selection Input 2. In SPI control mode, GPIO2 has its logic level referenced to the VDD_IO and DGND pins.
C12, C13	AGND	P	Ground Reference for VDD_FDA, IN_LDO, VDD_ADC, and VDD2_ADC Supplies. Connect to system ground for normal operation.
C14	VDD2_ADC	P	ADC Secondary Analog Supply Voltage. Referenced to AGND.
D1	IN+	AI	Signal Input, Noninverting.
D2	AGND	P	Ground Reference for VDD_FDA, IN_LDO, VDD_ADC, and VDD2_ADC Supplies. Connect to system ground for normal operation.
D3, D4	VDD_PGA	P	PGIA Positive Supply Input. Referenced to AGND.
D5	NC		Not Internally Connected. Leave floating or connect to ground reference.
D6	AGND	P	Connect to System Ground for Normal Operation.
D7	AGND	P	Ground Reference for VDD_FDA, IN_LDO, VDD_ADC, and VDD2_ADC Supplies. Connect to system ground for normal operation.
D8	DNC		Do Not Connect.
D9	EN_LDO	DI	On-Device LDO Enable Input. Active high.
D10	MODE3/GPIO3	DI/O	Multifunction Pin. In pin control mode, MODE3 is the Pin Control Operating Profile Selection Input 3. In SPI control mode, GPIO3 has its logic level referenced to the VDD_IO and DGND pins.
D11	$\overline{\text{RESET}}$	DI	ADC Hardware Asynchronous Reset Input. After the device is fully powered up, it is recommended to do a hardware or software reset.
D12	$\overline{\text{SYNC\_IN}}$	DI	$\overline{\text{SYNC\_IN}}$ receives the synchronization signal from $\overline{\text{SYNC\_OUT}}$ or from the main controller. The synchronization signal must be synchronous to MCLK.$\overline{\text{SYNC\_IN}}$ enables synchronization and simultaneous sampling of multiple ADAQ7768-1 devices.
D13	$\overline{\text{SYNC\_OUT}}$	DO	Synchronization Pulse Output Synchronous to MCLK. This pin allows one or multiple ADAQ7768-1 devices to be synchronized through SPI. Send a synchronization command over the SPI to initiate a $\overline{\text{SYNC\_OUT}}$. If used, route the $\overline{\text{SYNC\_OUT}}$ signal back to the $\overline{\text{SYNC\_IN}}$ pin of the same device and the $\overline{\text{SYNC\_IN}}$ pins of the other ADAQ7768-1 devices for simultaneous sampling.
D14	AREG_CAP	AO	Internal Analog LDO Regulator Output of the ADC. Decouple this pin to AGND with a 1µF capacitor. Do not use the voltage output from AREG_CAP in circuits external to the ADAQ7768-1.
E1	AGND	P	Ground Reference for VDD_FDA, IN_LDO, VDD_ADC, and VDD2_ADC Supplies. Connect to system ground for normal operation.
E2	NC		Not Internally Connected. Leave floating or connect to ground reference.
E3, E4	VDD_PGA	P	PGIA Positive Supply Input. Referenced to AGND.
E5	DNC		Do Not Connect.
E6	NC		Not Internally Connected. Leave floating or connect to ground reference.
E7, E8, E9	VDD_FDA	P	ADC Driver Amplifier Positive Supply. Referenced to AGND. Connect to OUT_LDO if using on-device LDO, or connect it to a single power source that also supplies the VDD2_PGA and VDD_ADC pins.
E10	DOUT/$\overline{\text{RDY}}$	DO	Serial Interface Data Output and Data Ready Signal Combined. This output data pin can be configured as either a DOUT pin only or through the SPI control mode, and include the ready signal ($\overline{\text{RDY}}$). The ability to program the

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 7. ADAQ7768-1 Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
			device to provide a combined DOUT and $\overline{RDY}$ signal can reduce the number of required interface input and output lines.
E11	SCLK	DI	Serial Interface Clock.
E12	SDI	DI	Serial Interface Data Input.
E13	$\overline{CS}$	DI	Serial Interface Chip-Select Input. Active low.
E14	$\overline{DRDY}$	DO	ADC Conversion Data Ready Output. Periodic signal output to signify conversion results are available.
F1	GAIN0	DI	PGIA Gain Control Logic Input 0.
F2	GAIN1	DI	PGIA Gain Control Logic Input 1.
F3	GAIN2	DI	PGIA Gain Control Logic Input 2.
F4, F5	VDD2_PGA	P	PGIA Output Stage Positive Power Supply. Referenced to AGND. Connect to OUT_LDO if using on-device LDO, else connect it to a single power source that also supplies the VDD_FDA and VDD_ADC pins. Bypass VDD2_PGA to AGND with a decoupling capacitor of 1 µF.
F6, F7, F8	OUT_LDO	P	On-Device LDO Output. Bypass OUT_LDO to AGND with a capacitor of at least 1 µF.
F9	VDD_IO	P	Digital Supply. The VDD_IO pin sets the logic levels for all interface pins. This pin powers the digital processing through the internal digital LDO. Referenced to DGND. Bypass VDD_IO to DGND with a capacitor of at least 1 µF.
F10, F11	DGND	P	Ground reference for VDD_IO supplies. Connect to system ground for normal operation.
F12	DREG_CAP	AO	Internal Digital LDO Regulator Output for the ADC. Decouple this pin to DGND with a 1 µF capacitor. For VDD_IO ≤ 1.8 V, use a 10 µF capacitor. Do not use the voltage output from AREG_CAP in circuits external to the ADAQ7768-1.
F13	XTAL1	DI	ADC Clock Input 1. External crystal: connect to one node of the external crystal. LVDS: connect to one node of the LVDS clock source. CMOS clock: connect to DGND.
F14	XTAL2_MCLK	DI	ADC Clock Input 2. External Crystal: Connect to the second node of the external crystal. LVDS: Connect to the second node of the LVDS clock source. CMOS clock: Connect to the CMOS clock source. Logic level referenced to VDD_IO and DGND.

[1] AI is analog input; AO is analog output; DI is digital input; DO is digital output; DI/O is bidirectional digital; P is power or ground.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD_PGA = 15 V, VSS_PGA = -15 V, AGND = DGND = 0 V, input common-mode voltage = 0 V, IN_LDO = 5.1 V to 5.5 V, OUT_LDO = VDD2_PGA = VDD_FDA = VDD_ADC, VDD2_ADC = 2 V to 5.5 V, VDD_IO = 1.7 V to 3.6 V, REF+ = 4.096 V, REF− = 0 V, MCLK = SCLK = 16.384 MHz 50:50 duty cycle, f_{MOD} = MCLK/2, filter = wideband low ripple, decimation = 32, ODR = 256 kSPS, linearity boost buffer on, reference precharge buffers on, FDA = full power mode, T_A = - 40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C.

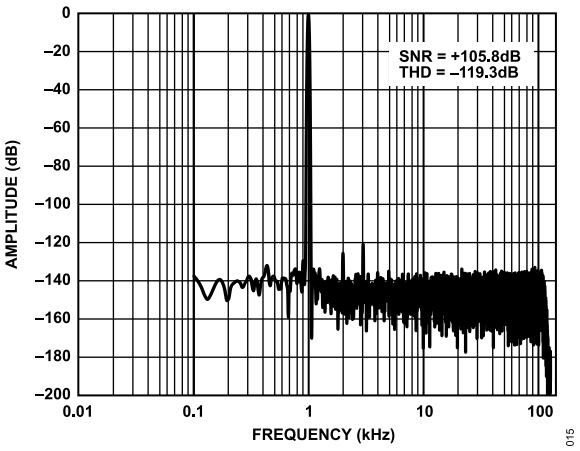

Figure 10. Fully Differential Input, −0.5 dBFS 1 kHz Sine, ODR = 256 kSPS, AFE_GAIN = 0.325 V/V (Gain 0 Mode)

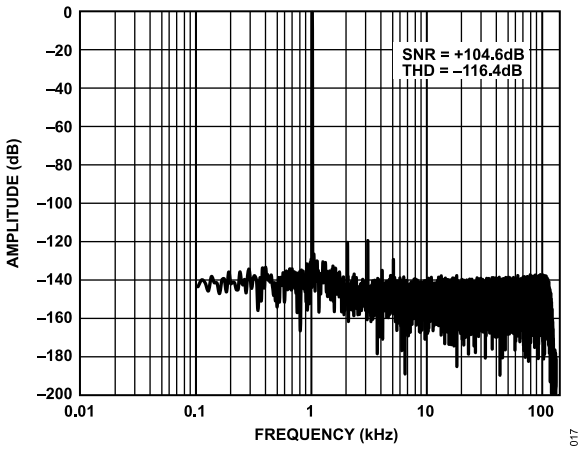

Figure 12. Fully Differential Input, −0.5 dBFS 1 kHz Sine, ODR = 256 kSPS, AFE_GAIN = 1.3 V/V (Gain 2 Mode)

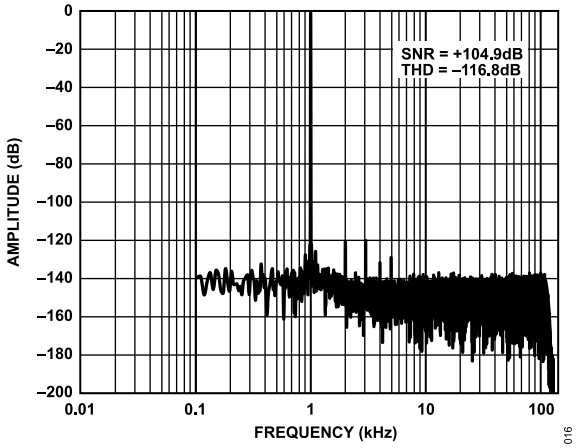

Figure 11. Fully Differential Input, −0.5 dBFS 1 kHz Sine, ODR = 256 kSPS, AFE_GAIN = 0.65 V/V (Gain 1 Mode)

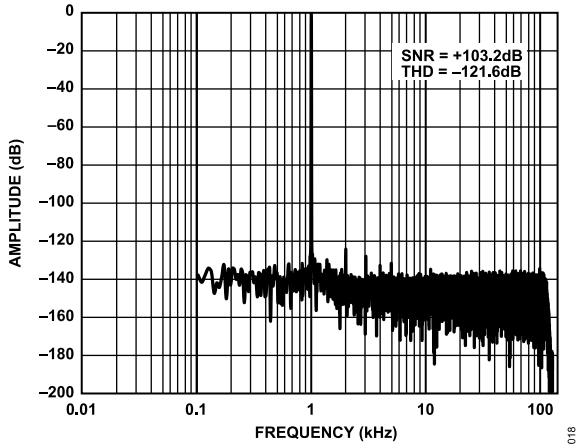

Figure 13. Fully Differential Input, −0.5 dBFS 1 kHz Sine, ODR = 256 kSPS, AFE_GAIN = 2.6 V/V (Gain 3 Mode)

TYPICAL PERFORMANCE CHARACTERISTICS

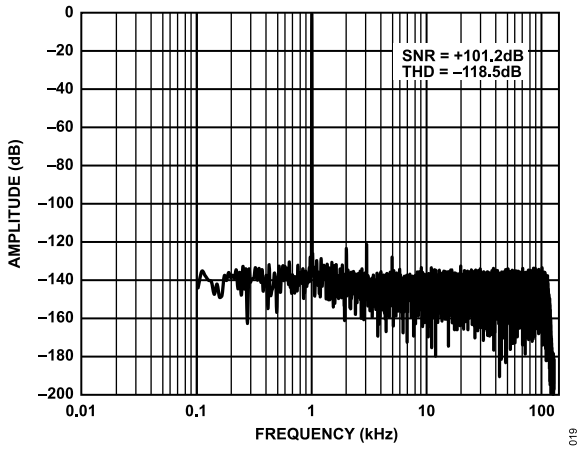

Figure 14. Fully Differential Input, −0.5 dBFS 1 kHz Sine, ODR = 256 kSPS, AFE_GAIN = 5.2 V/V (Gain 4 Mode)

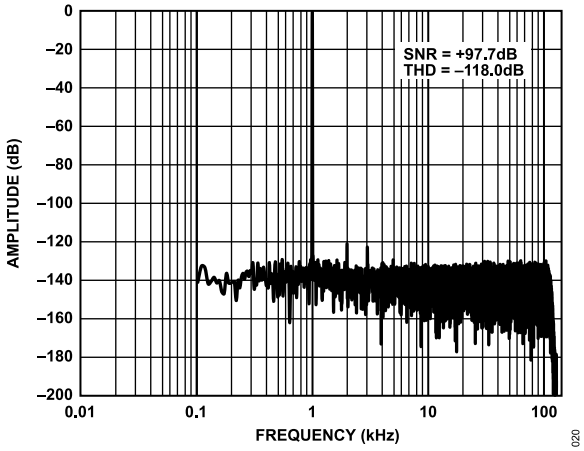

Figure 15. Fully Differential Input, −0.5 dBFS 1 kHz Sine, ODR = 256 kSPS, AFE_GAIN = 10.4 V/V (Gain 5 Mode)

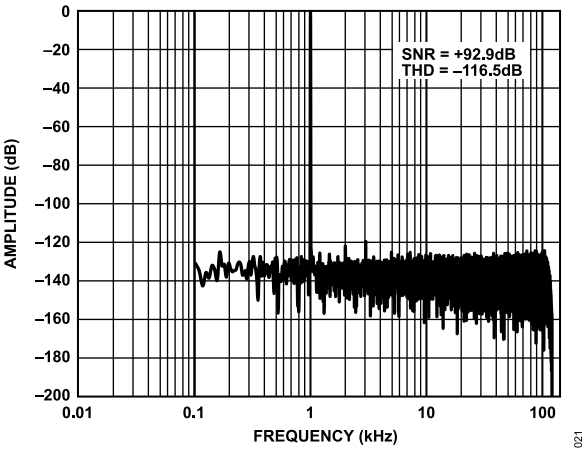

Figure 16. Fully Differential Input, −0.5 dBFS 1 kHz Sine, ODR = 256 kSPS, AFE_GAIN = 20.8 V/V (Gain 6 Mode)

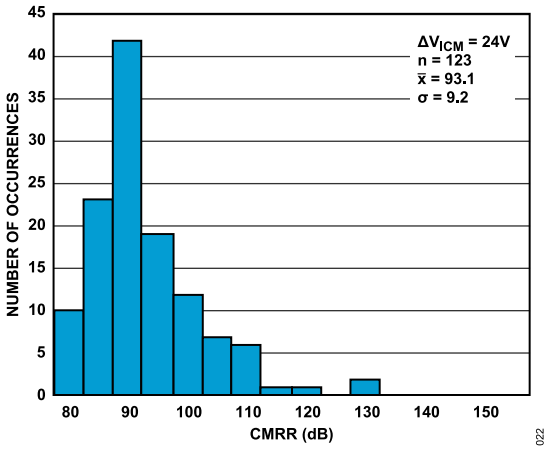

Figure 17. DC CMRR Distribution, V_{ICM} Full Range of ± 12 V = Δ V_{ICM} of 24 V, AFE_GAIN = 0.325 V/V (Gain 0 Mode)

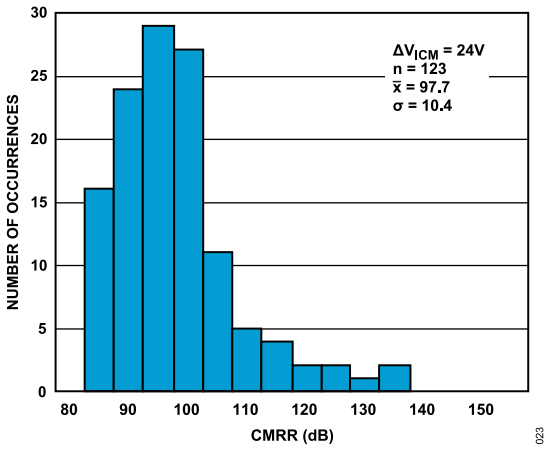

Figure 18. DC CMRR Distribution, V_{ICM} Full Range of ± 12 V = ΔV_{ICM} of 24 V, AFE_GAIN = 0.65 V/V (Gain 1 Mode)

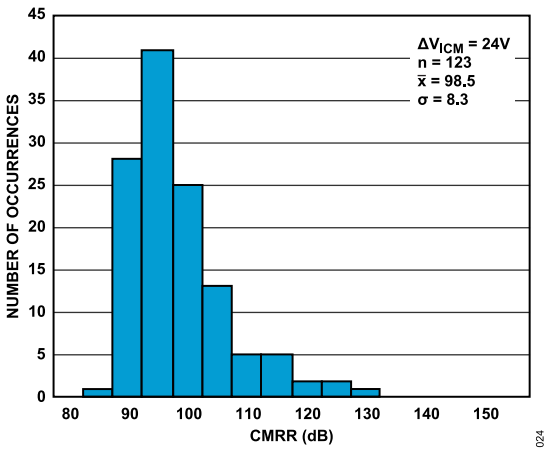

Figure 19. DC CMRR Distribution, V_{ICM} Full Range of ± 12 V = ΔV_{ICM} of 24 V, AFE_GAIN = 1.3 V/V (Gain 2 Mode)

TYPICAL PERFORMANCE CHARACTERISTICS

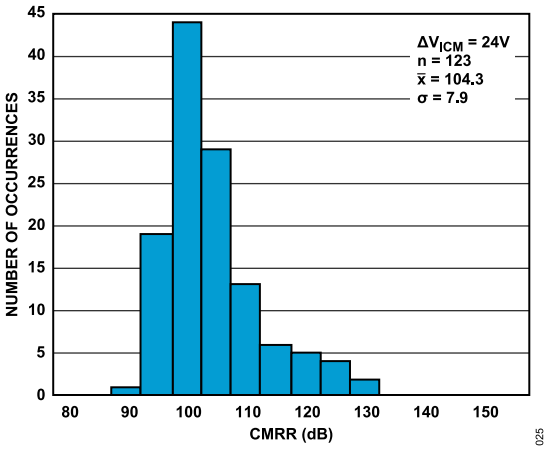

Figure 20. DC CMRR Distribution, V_{ICM} Full Range of ± 12 V = ΔV_{ICM} of 24 V, AFE_GAIN = 2.6 V/V (Gain 3 Mode)

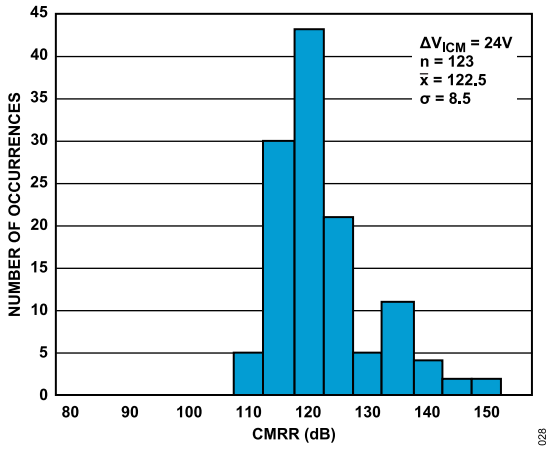

Figure 23. DC CMRR Distribution, V_{ICM} Full Range of ± 12 V = ΔV_{ICM} of 24 V, AFE_GAIN = 20.8 V/V (Gain 6 Mode)

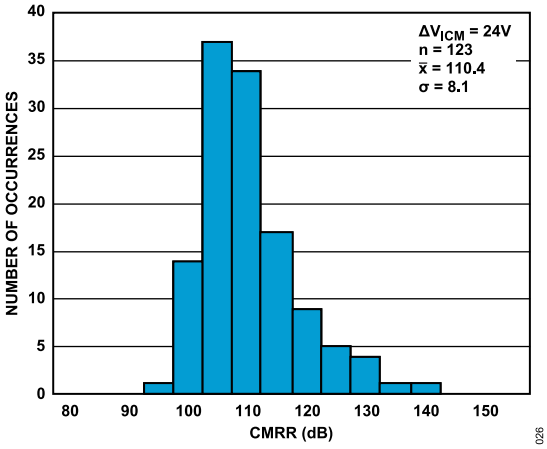

Figure 21. DC CMRR Distribution, V_{ICM} Full Range of ± 12 V = ΔV_{ICM} of 24 V, AFE_GAIN = 5.2 V/V (Gain 4 Mode)

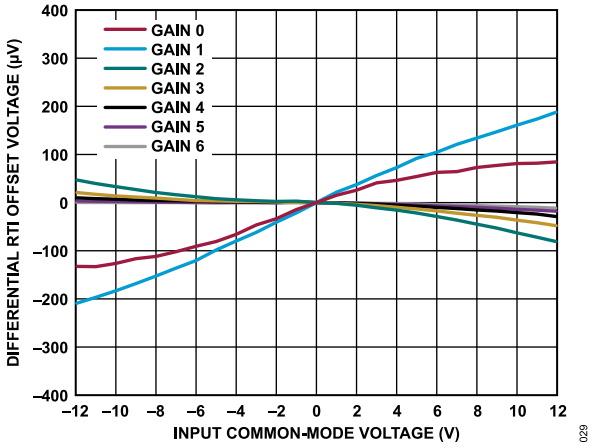

Figure 24. Differential RTI Offset Voltage vs. Input Common-Mode Voltage Across All Gain Modes

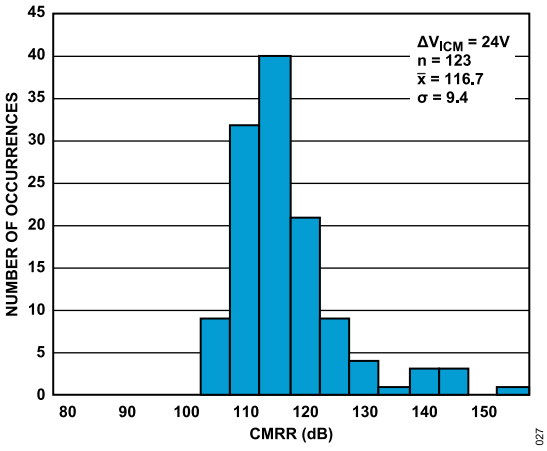

Figure 22. DC CMRR Distribution, V_{ICM} Full Range of ± 12 V = ΔV_{ICM} of 24 V, AFE_GAIN = 10.4 V/V (Gain 5 Mode)

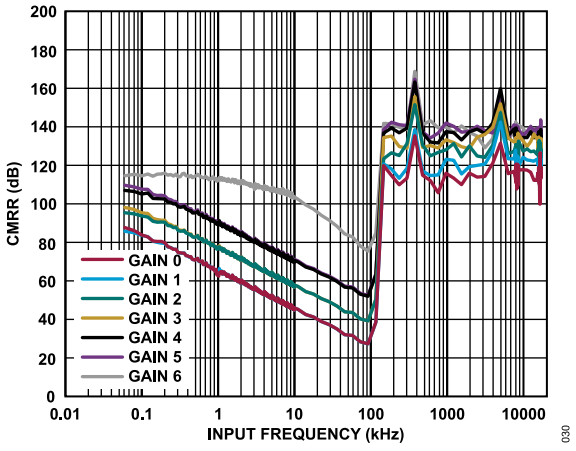

Figure 25. AC CMRR vs. Input Frequency Across All Gain Modes

TYPICAL PERFORMANCE CHARACTERISTICS

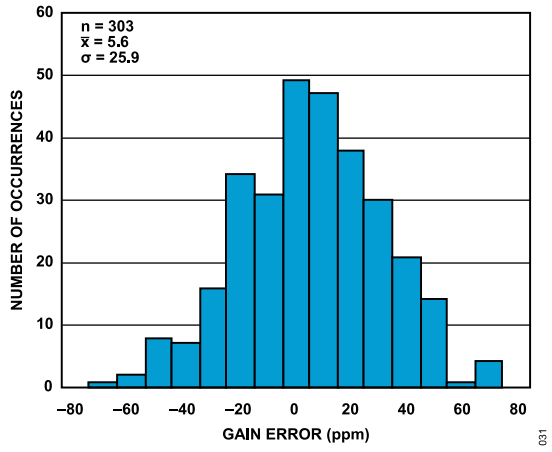

Figure 26. Gain Error Distribution, AFE_GAIN = 0.325 V/V (Gain 0 Mode)

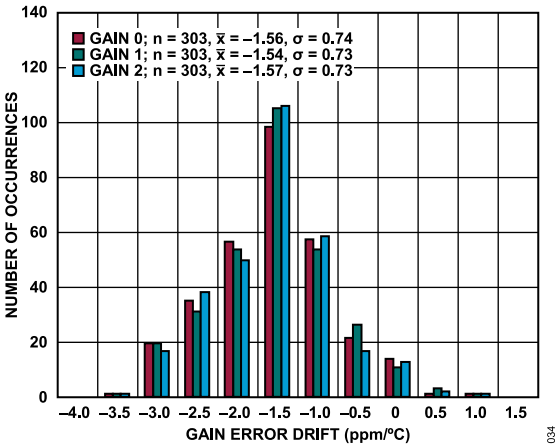

Figure 29. Gain Error Drift Distributions at Various Gain Modes

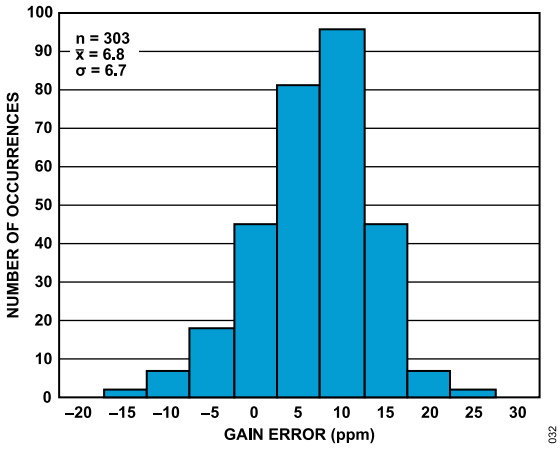

Figure 27. Gain Error Distribution, AFE_GAIN = 1.3 V/V (Gain 2 Mode)

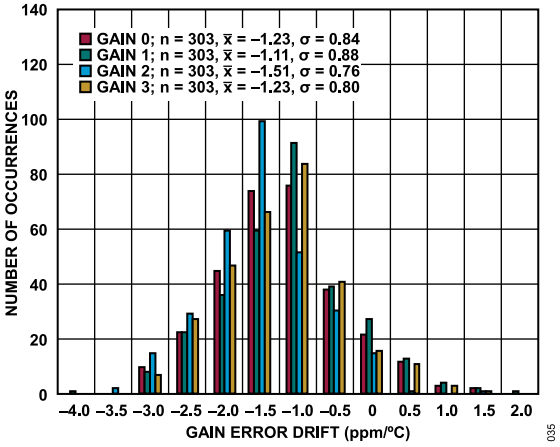

Figure 30. Gain Error Drift Distributions at Various Gain Modes

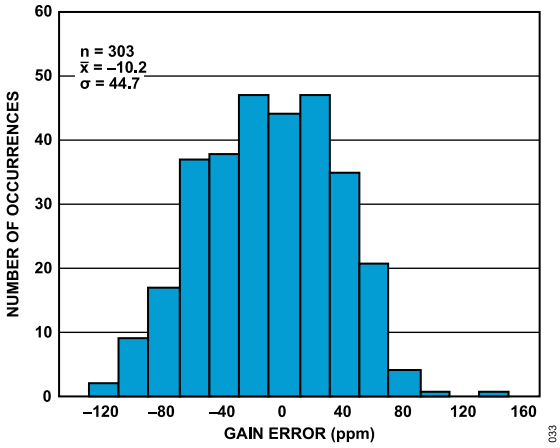

Figure 28. Gain Error Distribution, AFE_GAIN = 20.8 V/V (Gain 6 Mode)

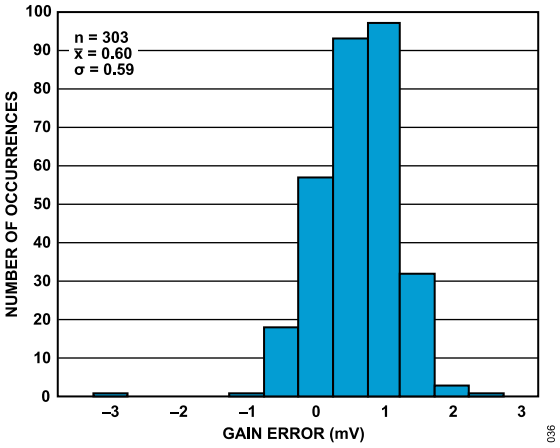

Figure 31. Offset Error Distribution, AFE_GAIN = 0.325 V/V (Gain 0 Mode)

TYPICAL PERFORMANCE CHARACTERISTICS

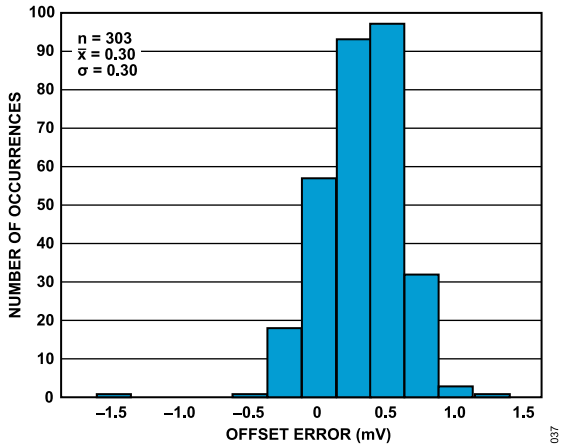

Figure 32. Offset Error Distribution, AFE_GAIN = 0.65 V/V (Gain 1 Mode)

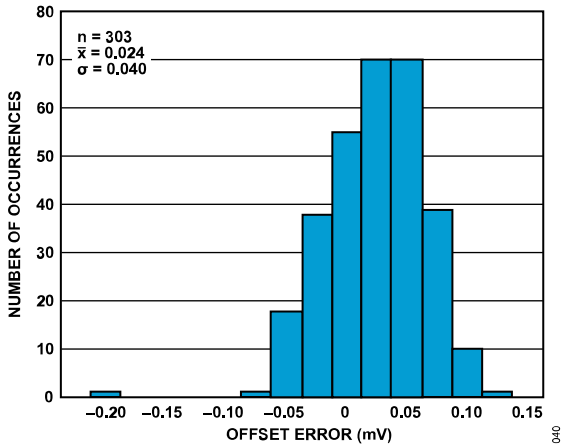

Figure 35. Offset Error Distribution, AFE_GAIN = 5.2 V/V (Gain 4 Mode)

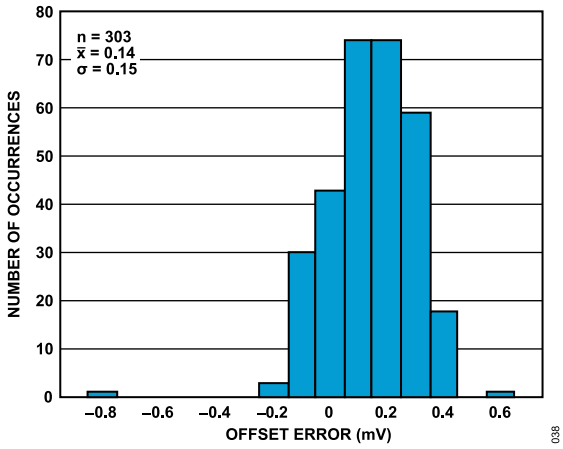

Figure 33. Offset Error Distribution, AFE_GAIN = 1.3 V/V (Gain 2 Mode)

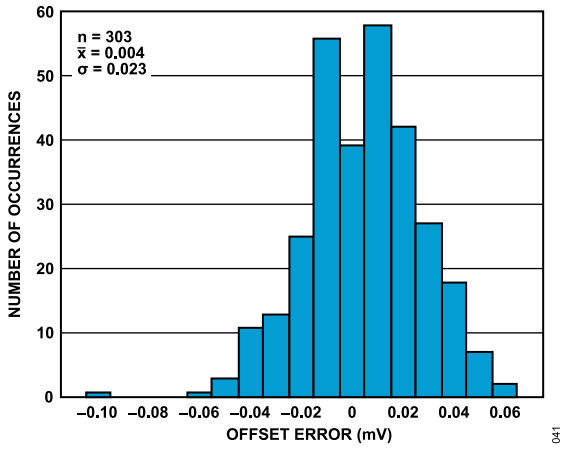

Figure 36. Offset Error Distribution, AFE_GAIN = 10.4 V/V (Gain 5 Mode)

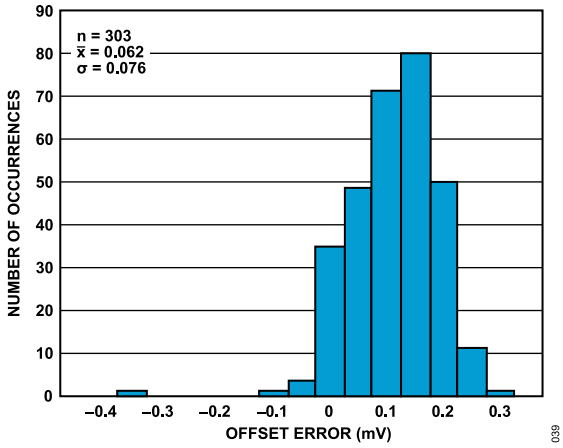

Figure 34. Offset Error Distribution, AFE_GAIN = 2.6 V/V (Gain 3 Mode)

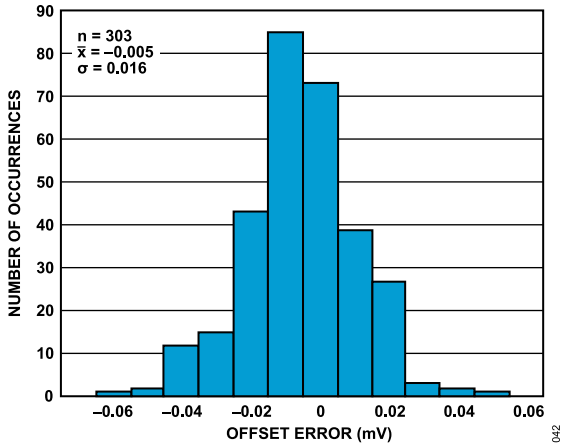

Figure 37. Offset Error Distribution, AFE_GAIN = 20.8 V/V (Gain 6 Mode)

TYPICAL PERFORMANCE CHARACTERISTICS

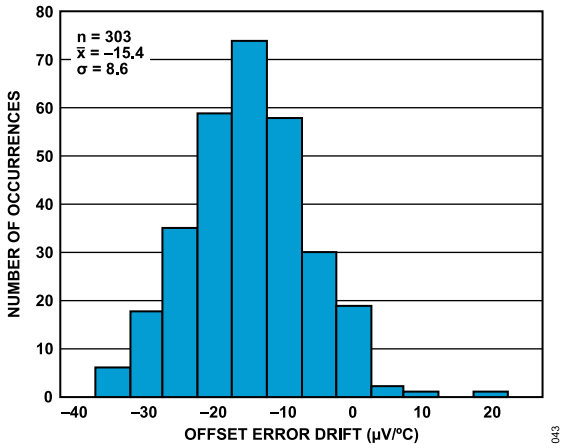

Figure 38. Offset Error Drift Distribution, AFE_GAIN = 0.325 V/V (Gain 0 Mode)

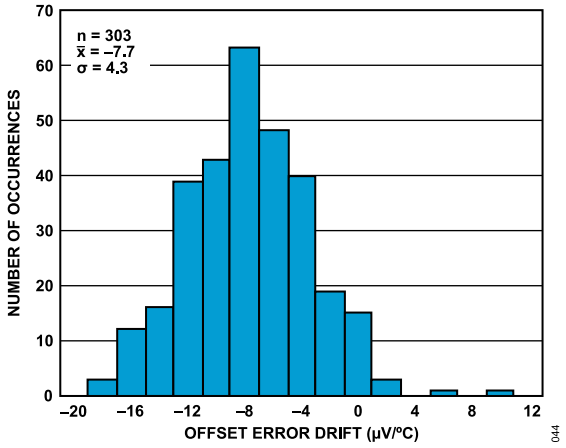

Figure 39. Offset Error Drift Distribution, AFE_GAIN = 0.65 V/V (Gain 1 Mode)

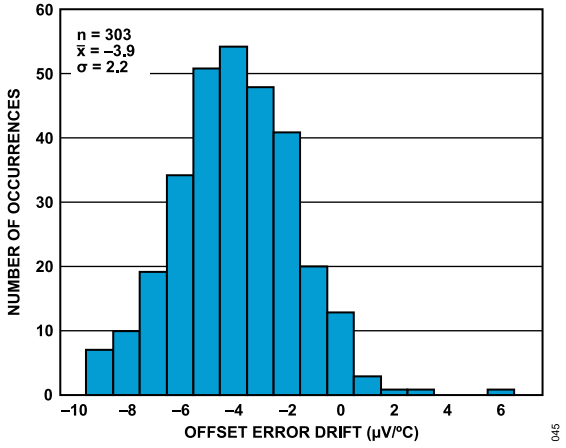

Figure 40. Offset Error Drift Distribution, AFE_GAIN = 1.3 V/V (Gain 2 Mode)

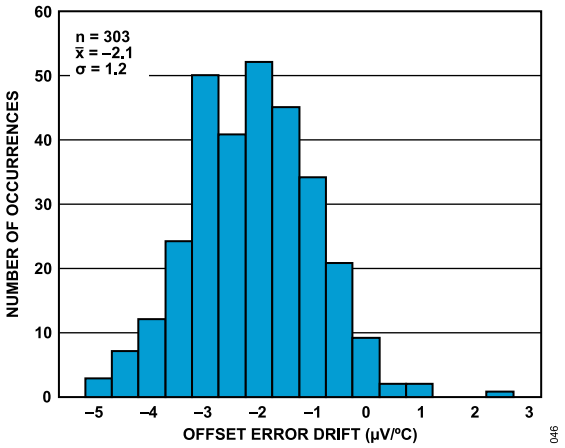

Figure 41. Offset Error Drift Distribution, AFE_GAIN = 2.6 V/V (Gain 3 Mode)

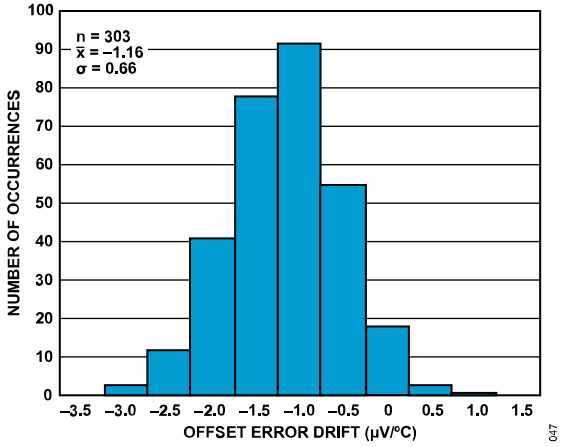

Figure 42. Offset Error Drift Distribution, AFE_GAIN = 5.2 V/V (Gain 4 Mode)

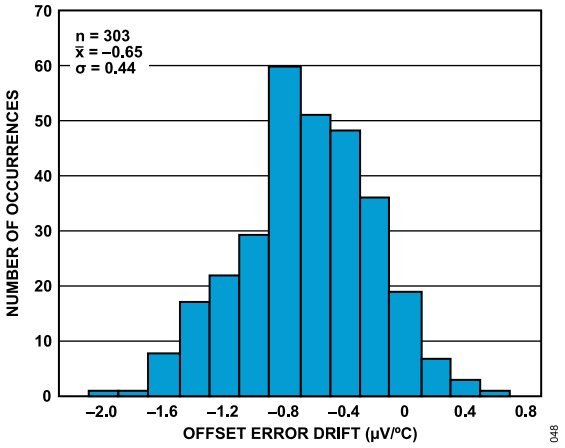

Figure 43. Offset Error Drift Distribution, AFE_GAIN = 10.4 V/V (Gain 5 Mode)

TYPICAL PERFORMANCE CHARACTERISTICS

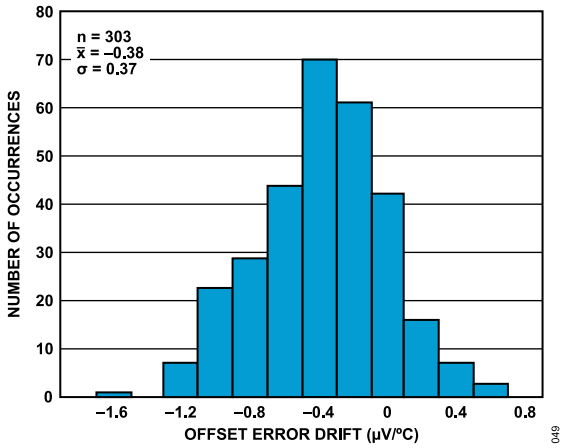

Figure 44. Offset Error Drift Distribution, AFE_GAIN = 20.8 V/V (Gain 6 Mode)

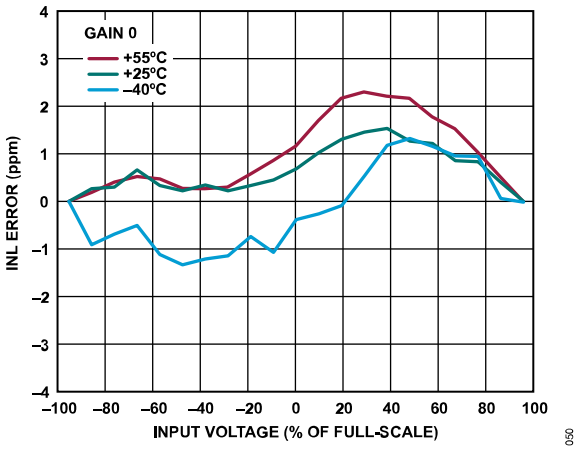

Figure 45. INL Error vs. Input Voltage over Temperature, Differential Input, AFE_GAIN = 0.325 V/V (Gain 0 Mode)

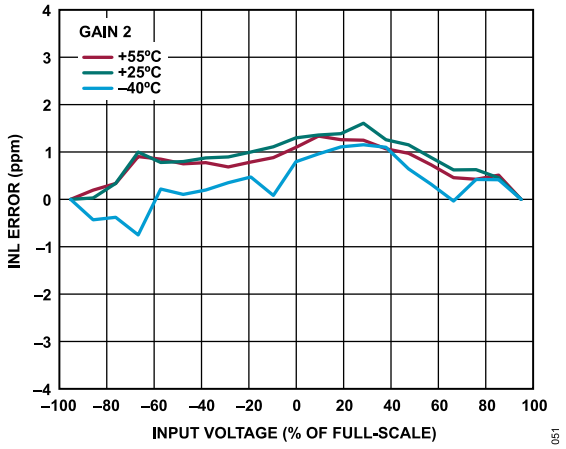

Figure 46. INL Error vs. Input Voltage over Temperature, Differential Input, AFE_GAIN = 1.3 V/V (Gain 2 Mode)

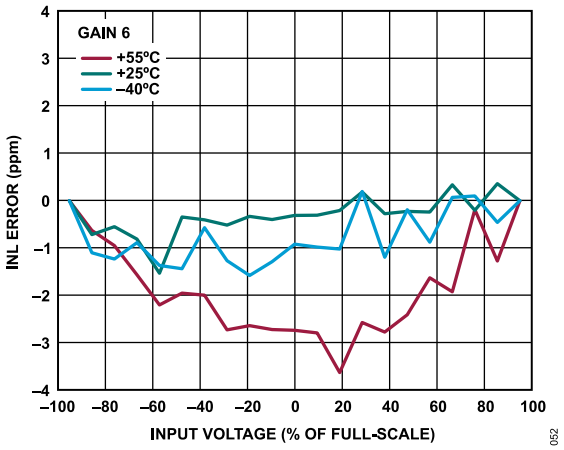

Figure 47. INL Error vs. Input Voltage over Temperature, Differential Input, AFE_GAIN = 20.8 V/V (Gain 6 Mode)

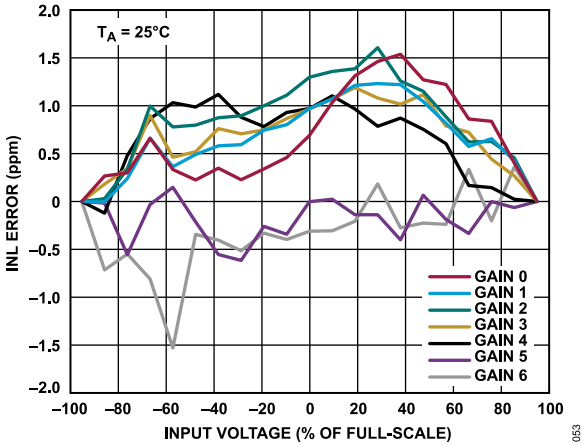

Figure 48. INL Error vs. Input Voltage Across All Gain Modes, Differential Input, Temp = +25°C

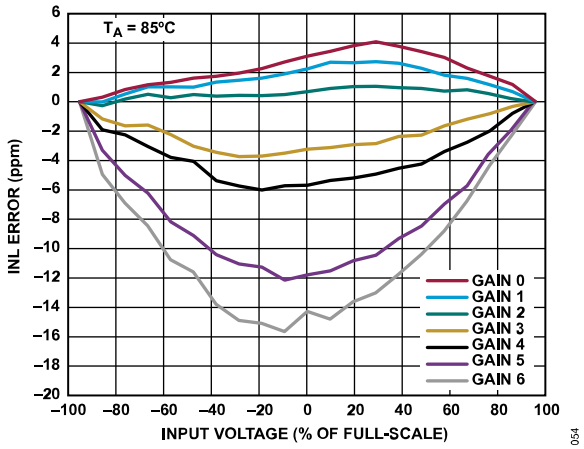

Figure 49. INL Error vs. Input Voltage Across All Gain Modes, Differential Input, Temp = +85°C

TYPICAL PERFORMANCE CHARACTERISTICS

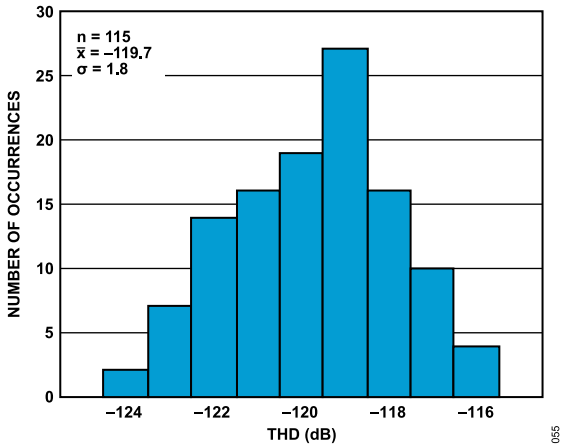

Figure 50. THD Distribution, AFE_GAIN = 0.325 V/V (Gain 0 Mode)

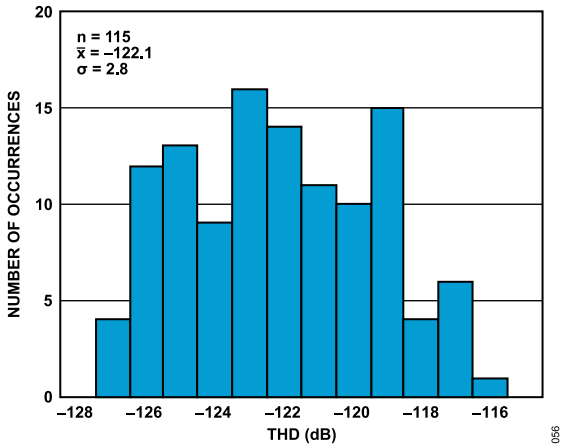

Figure 51. THD Distribution, AFE_GAIN = 1.3 V/V (Gain 2 Mode)

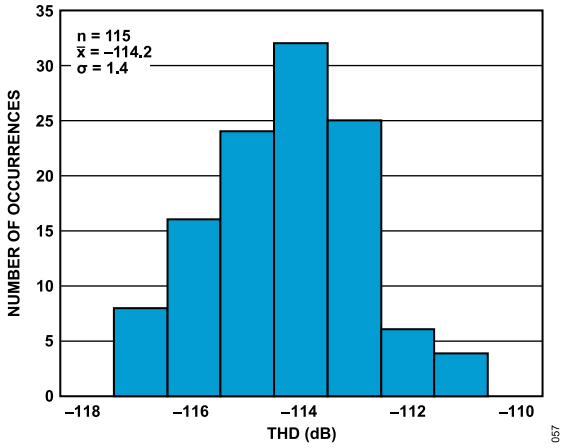

Figure 52. THD Distribution, AFE_GAIN = 20.8 V/V (Gain 6 Mode)

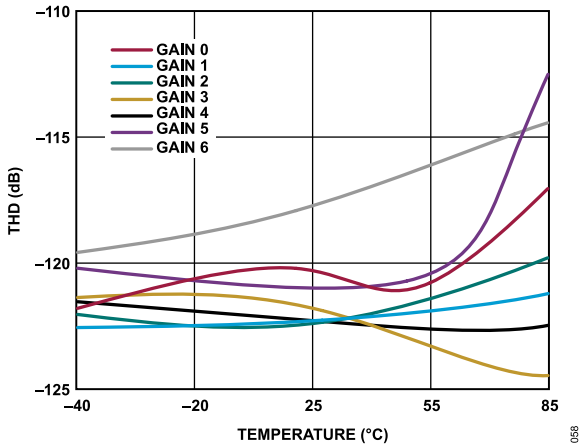

Figure 53. THD vs. Temperature Across All Gain Modes, −0.5 dBFS, 1 kHz

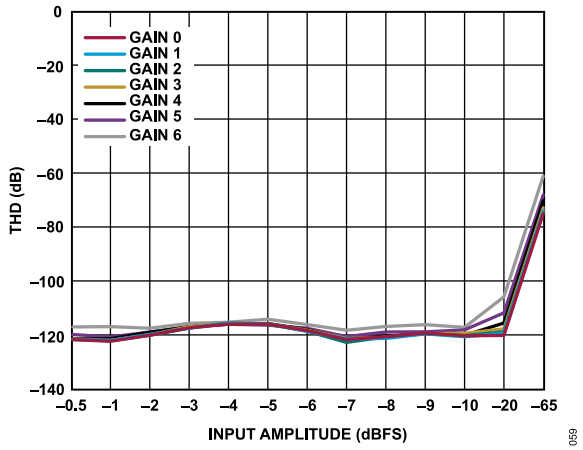

Figure 54. THD vs. Input Amplitude Across All Gain Modes, 1 kHz

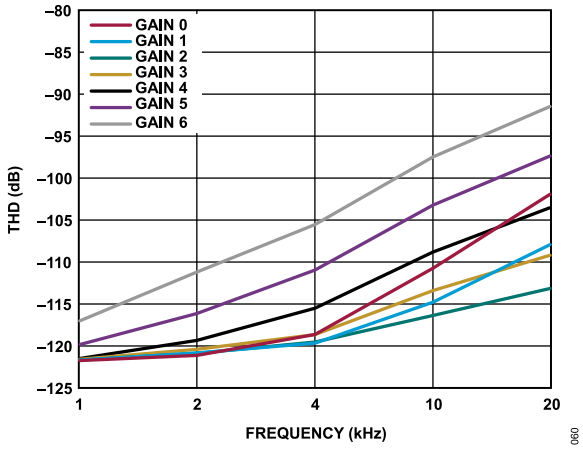

Figure 55. THD vs. Input Frequency Across All Gain Modes, −0.5 dBFS

TYPICAL PERFORMANCE CHARACTERISTICS

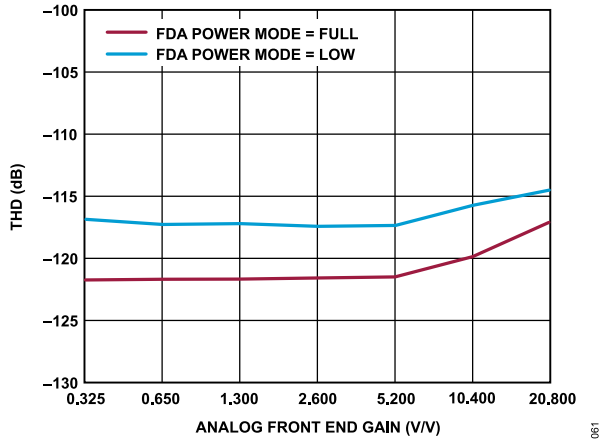

Figure 56. THD vs. Analog Front-End (AFE) Gain over FDA Power Mode, −0.5 dBFS, 1 kHz

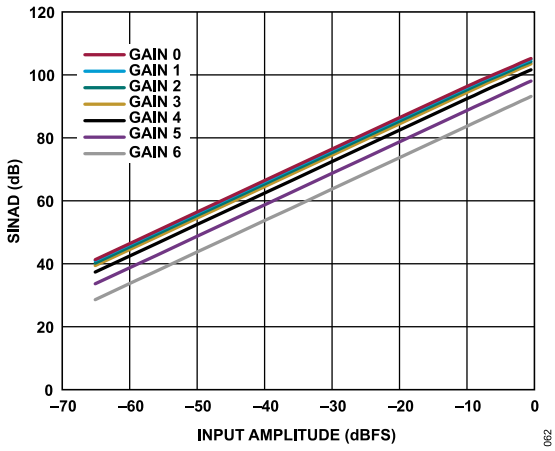

Figure 57. SINAD vs. Input Amplitude Across All Gain Modes, 1 kHz

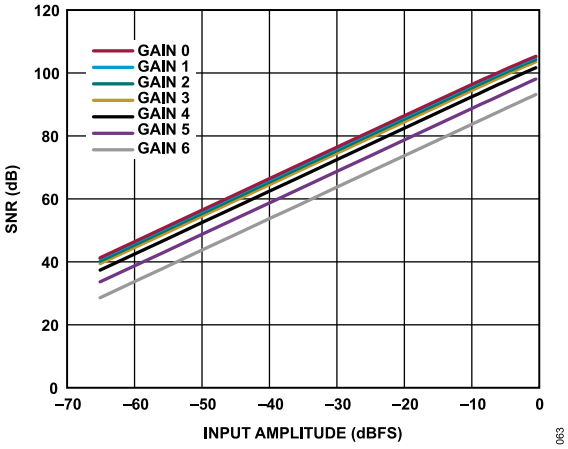

Figure 58. SNR vs. Input Amplitude Across All Gain Modes, 1 kHz

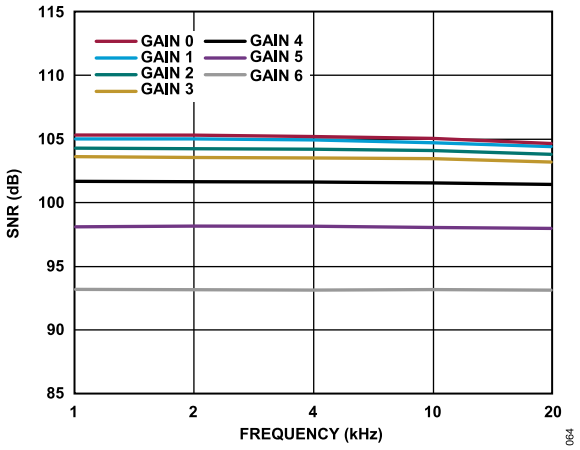

Figure 59. SNR vs. Input Frequency Across All Gain Modes, 1 kHz

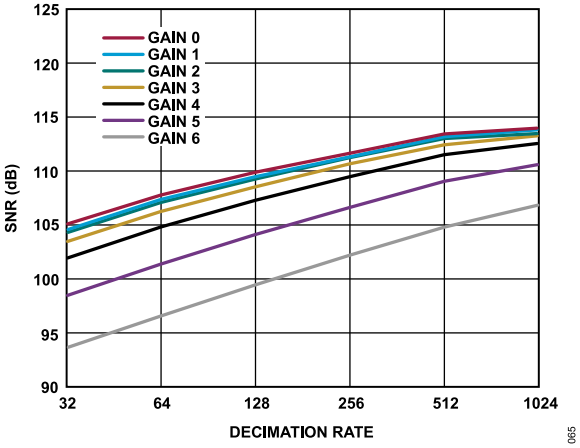

Figure 60. SNR vs. Decimation Rate Across All Gain Modes, Wideband Low Ripple Filter, −0.5 dBFS, 1 kHz

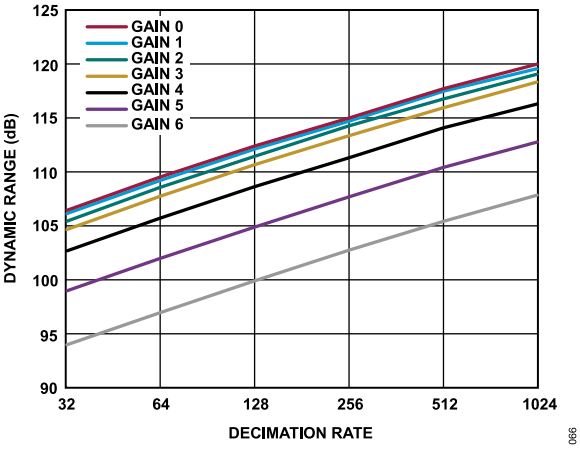

Figure 61. Dynamic Range vs. Decimation Rate Across All Gain Modes, Wideband Low Ripple Filter, Shorted Inputs

TYPICAL PERFORMANCE CHARACTERISTICS

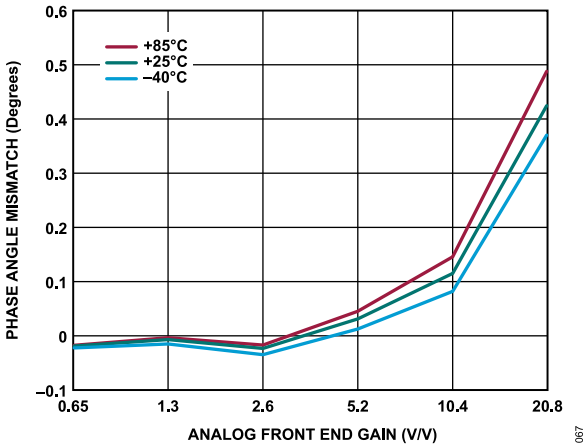

Figure 62. Phase Angle Mismatch vs. Analog Front-End (AFE) Gain over Temperature, Normalized to AFE_GAIN = 0.325 V/V (Gain 0 Mode)

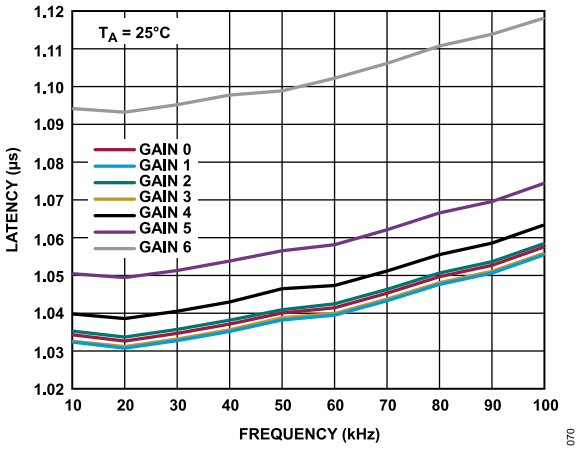

Figure 65. Analog Front-End (AFE) Latency vs. Passband Frequency Across All Gain Modes at 25°C

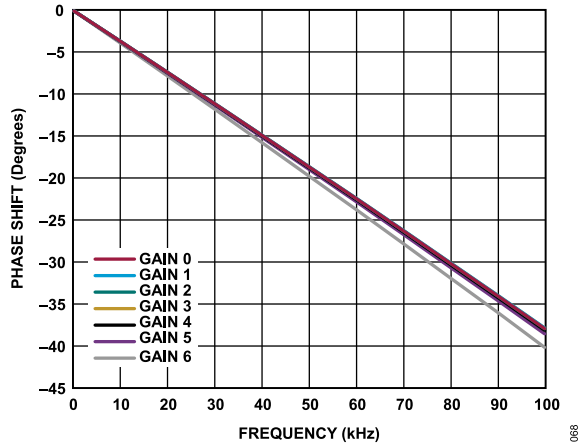

Figure 63. Analog Front-End (AFE) Phase Response Across All Gain Modes at 25°C

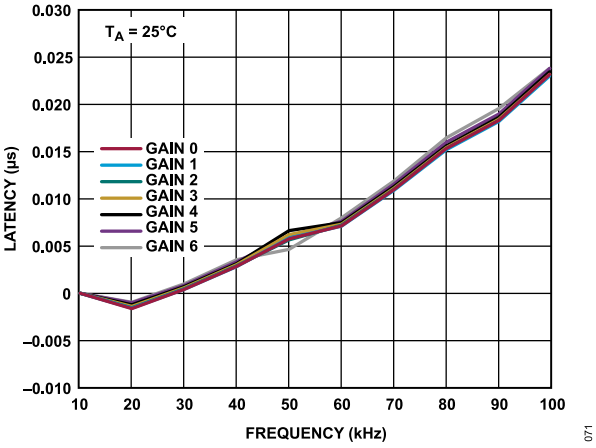

Figure 66. Analog Front-End (AFE) Latency vs. Passband Frequency Across All Gain Modes, at 25°C, Normalized to Latency at 10 kHz

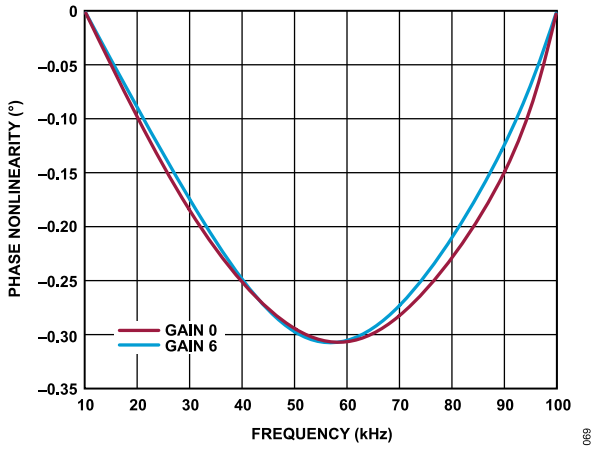

Figure 64. Analog Front-End (AFE) Phase Nonlinearity vs. Passband Frequency at Gain 0 and Gain 6, Endpoint Method (10 kHz to 100 kHz)

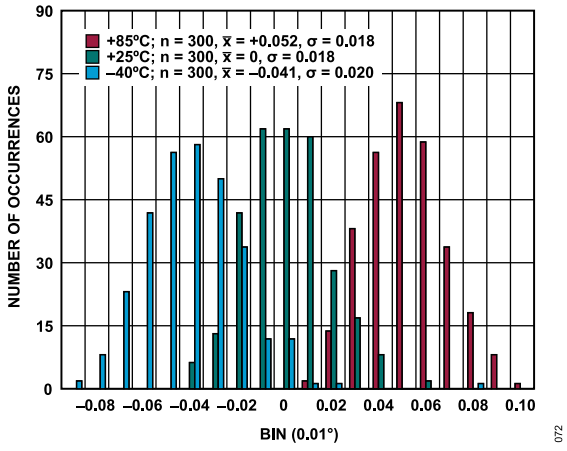

Figure 67. Device-to-Device Phase Angle Mismatch, 20 kHz, AFE_GAIN = 0.325 V/V (Gain 0 Mode), Normalized to the Mean Value at 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

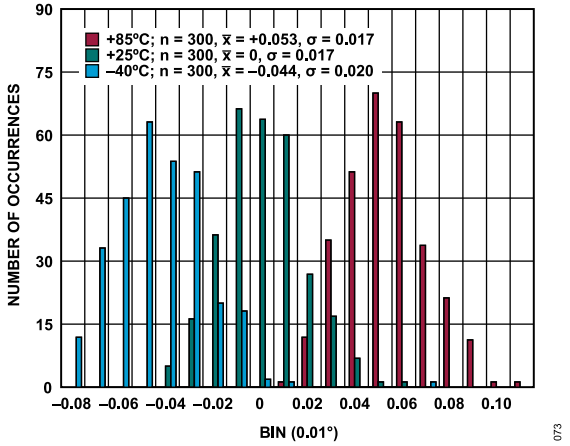

Figure 68. Device-to-Device Phase Angle Mismatch, 20 kHz, AFE_GAIN = 0.65 V/V (Gain 1 Mode), Normalized to the Mean Value at 25°C

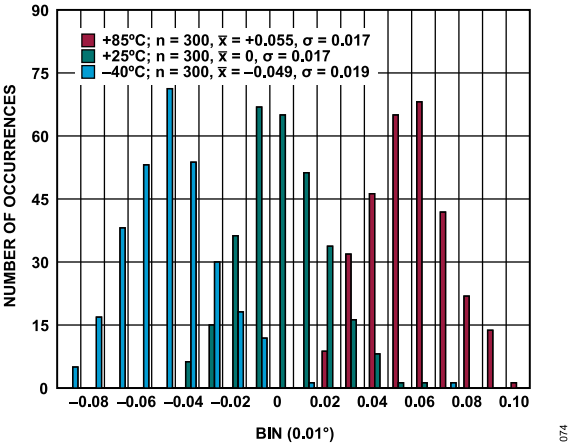

Figure 69. Device-to-Device Phase Angle Mismatch, 20 kHz, AFE_GAIN = 1.3 V/V (Gain 2 Mode), Normalized to the Mean Value at 25°C

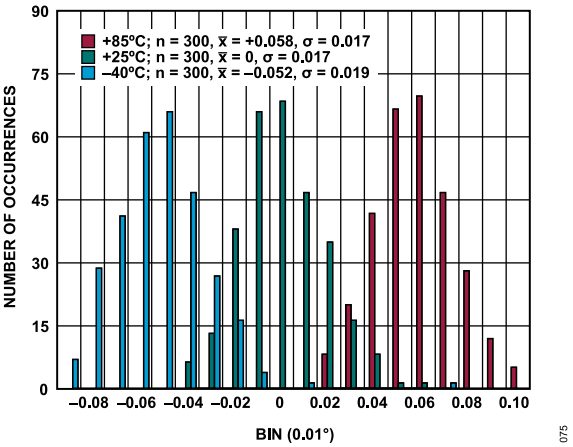

Figure 70. Device-to-Device Phase Angle Mismatch, 20 kHz, AFE_GAIN = 2.6 V/V (Gain 3 Mode), Normalized to the Mean Value at 25°C

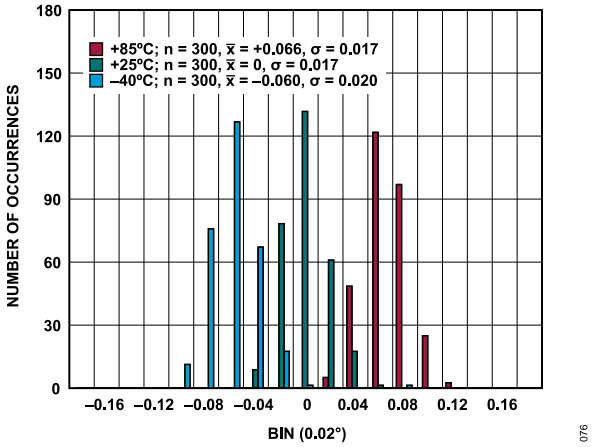

Figure 71. Device-to-Device Phase Angle Mismatch, 20 kHz, AFE_GAIN = 5.2 V/V (Gain 4 Mode), Normalized to the Mean Value at 25°C

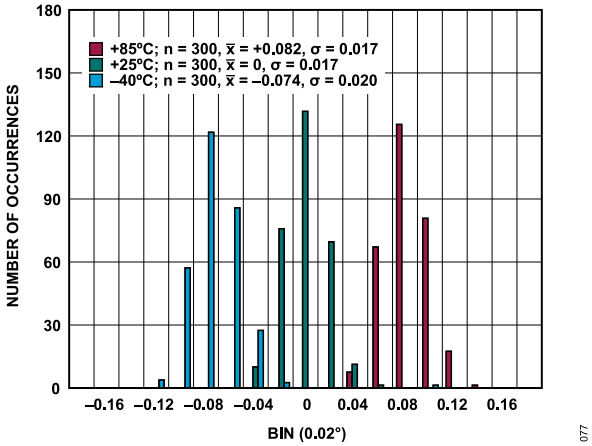

Figure 72. Device-to-Device Phase Angle Mismatch, 20 kHz, AFE_GAIN = 10.4 V/V (Gain 5 Mode), Normalized to the Mean Value at 25°C

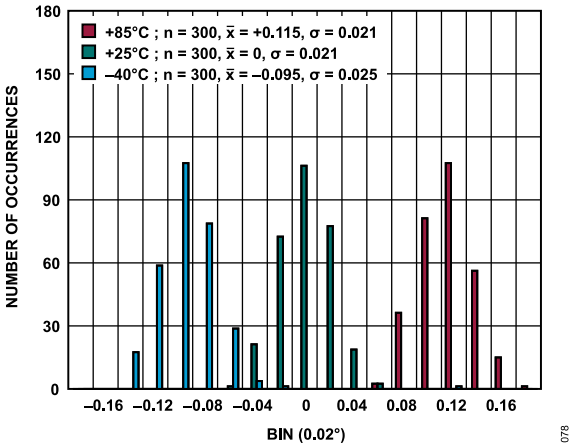

Figure 73. Device-to-Device Phase Angle Mismatch, 20 kHz, AFE_GAIN = 20.8 V/V (Gain 6 Mode), Normalized to the Mean Value at 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

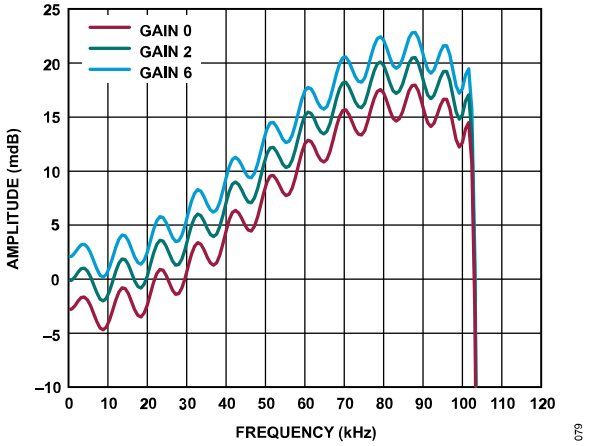

Figure 74. Wideband Low Ripple FIR Filter Pass-Band Ripple, ODR = 256 kSPS, Normalized to AFE_GAIN = 1.3 V/V (Gain 2 Mode)

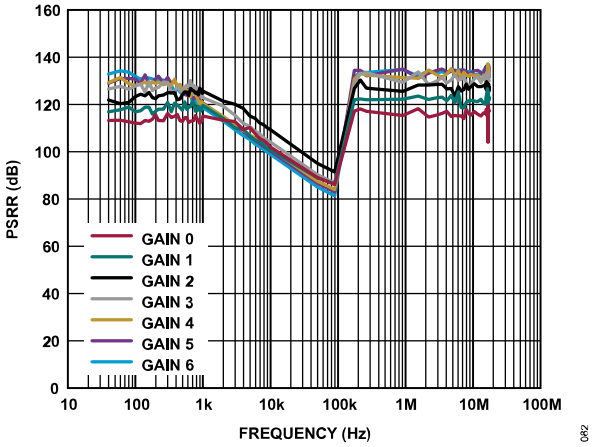

Figure 77. VDD_PGA AC PSSR Across All Gain Modes, Using the Internal Supply Decoupling Capacitor Only

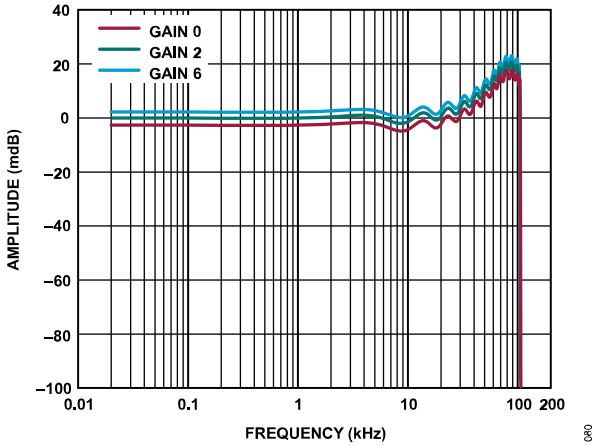

Figure 75. Magnitude Flatness Response, Wideband Low Ripple FIR Filter, ODR = 256 kSPS, Normalized to AFE_GAIN = 1.3 V/V (Gain 2 Mode)

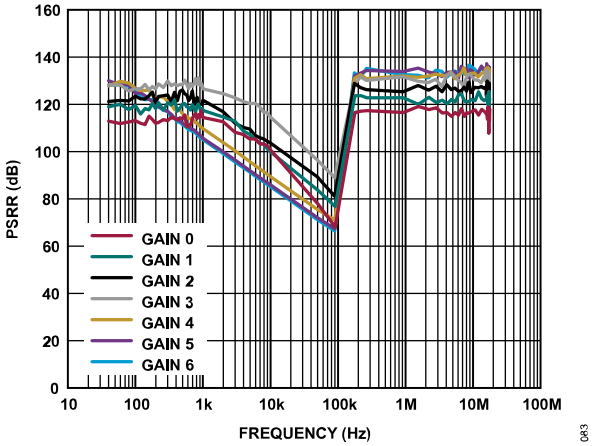

Figure 78. VSS_PGA AC PSSR Across All Gain Modes, Using the Internal Supply Decoupling Capacitor Only

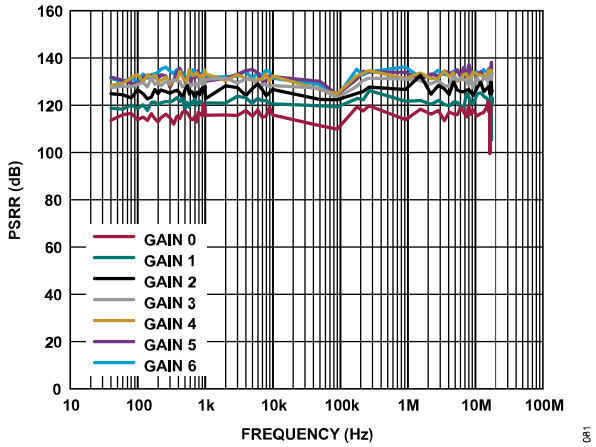

Figure 76. LDO AC PSRR Across All Gain Modes, Connected to VDD2_PGA, VDD_FDA, VDD_ADC, VDD2_ADC with 1 µF External Supply Decoupling Capacitor at OUT_LDO

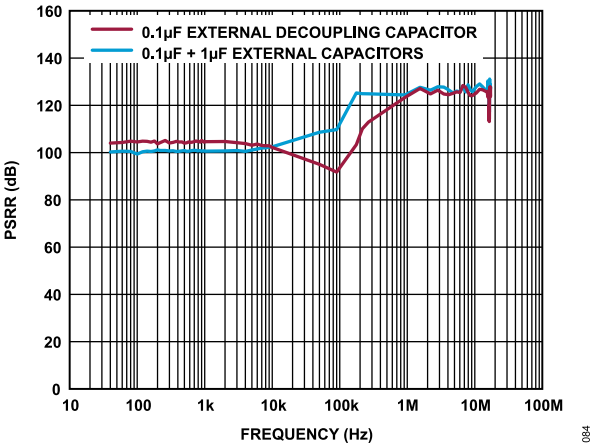

Figure 79. VDD_IO AC PSRR Using External Supply Decoupling Capacitor

TYPICAL PERFORMANCE CHARACTERISTICS

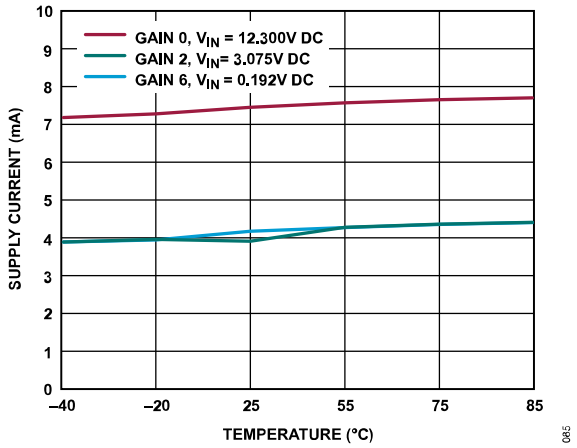

Figure 80. VDD_PGA Supply Current vs. Temperature at Various Gain Modes, DC Input

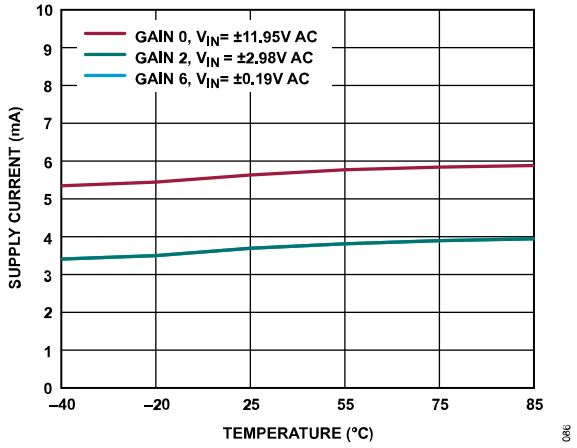

Figure 81. VDD_PGA Supply Current vs. Temperature at Various Gain Modes, AC Input

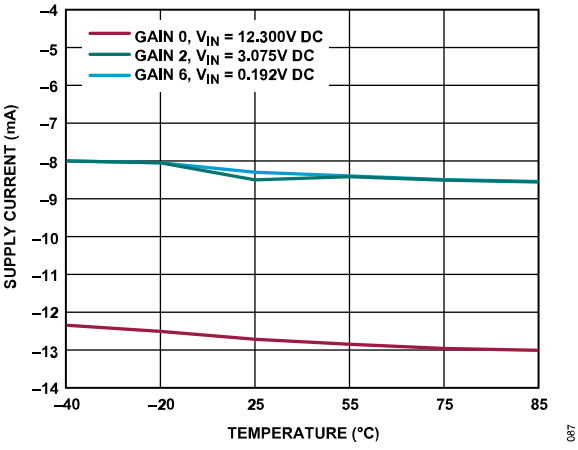

Figure 82. VSS_PGA Supply Current vs. Temperature at Various Gain Modes, DC Input

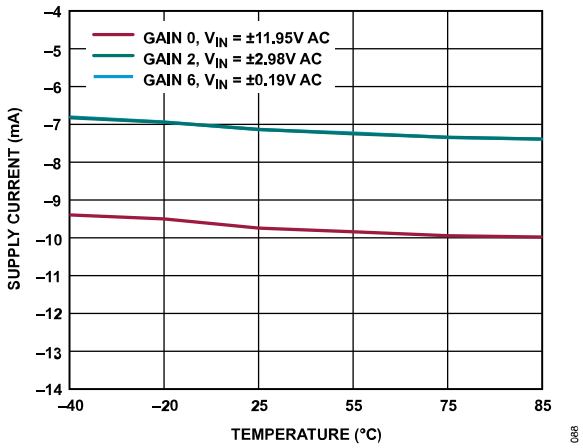

Figure 83. VSS_PGA Supply Current vs. Temperature at Various Gain Modes, AC Input

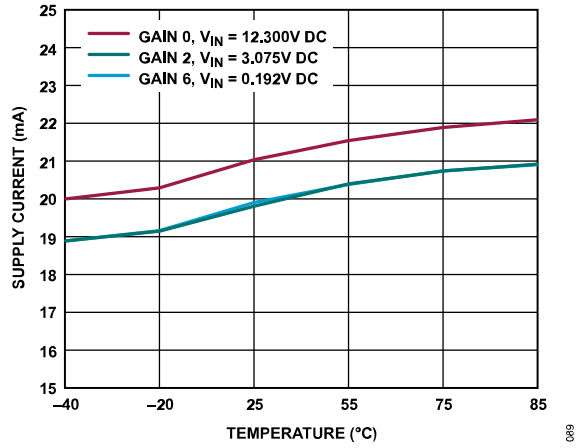

Figure 84. LDO Supply Current vs. Temperature at Various Gain Modes, DC Input, FDA = Full Power, OUT_LDO Connected to VDD2_PGA, VDD_FDA, VDD_ADC, VDD2_ADC

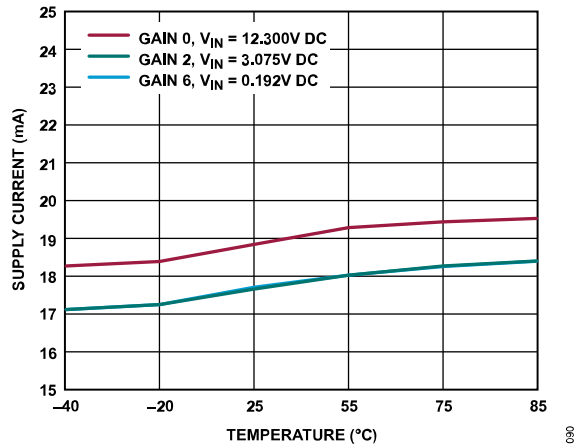

Figure 85. LDO Supply Current vs. Temperature at Various Gain Modes, DC Input, FDA = Low Power, OUT_LDO Connected to VDD2_PGA, VDD_FDA, VDD_ADC, VDD2_ADC

TYPICAL PERFORMANCE CHARACTERISTICS

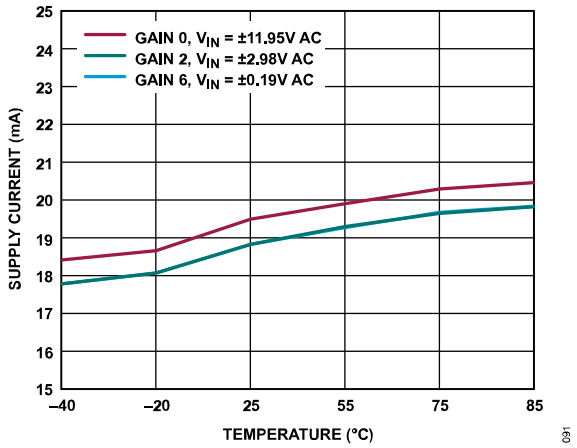

Figure 86. LDO Supply Current vs. Temperature at Various Gain Modes, AC Input, FDA = Full Power, OUT_LDO Connected to VDD2_PGA, VDD_FDA, VDD_ADC, VDD2_ADC

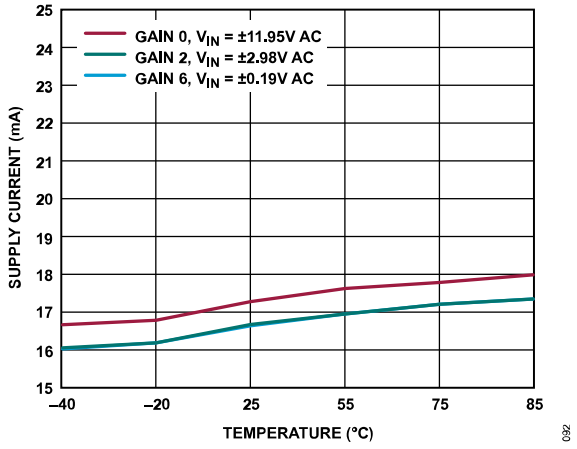

Figure 87. LDO Supply Current vs. Temperature at Various Gain Modes, AC Input, FDA = Low Power, OUT_LDO Connected to VDD2_PGA, VDD_FDA, VDD_ADC, VDD2_ADC

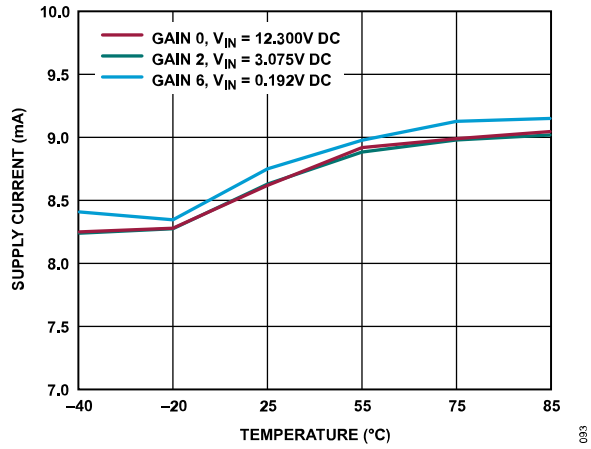

Figure 88. VDD_IO Supply Current vs. Temperature at Various Gain Modes, DC Input

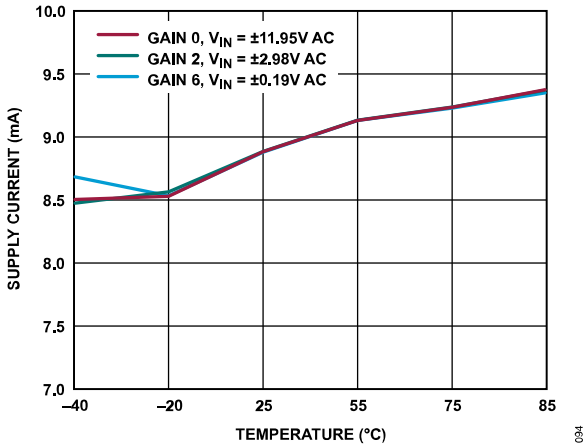

Figure 89. VDD_IO Supply Current vs. Temperature at Various Gain Modes, AC Input

TERMINOLOGY

AC Common-Mode Rejection Ratio (CMRR)

The ratio of the power in the ADC output at frequency, f, to the power of a 600 mV p-p sine-wave applied to the common-mode voltage of IN+ and IN− at frequency, f_S.

$$CMRR\ (dB) = 10\ \log\left(\frac{Pf}{Pf_S}\right) \quad (1)$$

where:

Pf is the power at frequency, f, in the ADC output.

Pf_S is the power at frequency, f_S, in the ADC output.

Least Significant Bit (LSB)

The smallest increment that can be represented by a converter. For a fully differential input ADC with N bits of resolution, the LSB expressed in volts is:

$$LSB\ (V) = \frac{V_{REF} \times 2}{2^N \times AFE\_GAIN} \quad (2)$$

Gain Error

The first transition (from 100 … 000 to 100 …001) occurs at a level ½ LSB above nominal negative full scale. The last transition (from 011 … 110 to 011 … 111) occurs for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and actual level of the first transition from the difference between the ideal levels.

Gain Error Drift

The ratio of the gain error change due to a temperature change of 1°C and the full-scale range (2^N). It is expressed in parts per million.

Offset Error

The difference between the ideal midscale input voltage (0 V) and actual voltage producing the midscale output code.

Offset Error Drift

The ratio of the offset error change due to a temperature change of 1°C and the full scale code range (2^N). It is expressed in parts per million.

Differential Nonlinearity (DNL) Error

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value, often specified in terms of resolution for which no missing codes are guaranteed.

Integral Nonlinearity (INL) Error

The deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Dynamic Range

The ratio of the root mean-square (RMS) value of the full scale to the RMS noise measured when input pins are shorted together. The value is expressed in decibels.

Total System Dynamic Range

The ratio of the RMS value of the full scale at Gain0 mode to the input referred RMS noise measured when input pins are shorted together in the Gain6 mode. The value is expressed in decibels.

Peak-to-Peak Resolution

The number of bits unaffected by peak-to-peak noise or flicker. It is also sometimes called 'flicker-free resolution' or 'noise-free code resolution'. It follows this formula:

$$\log_2\left(\frac{Full\ \ Scale\ \ Range}{6.6 \times RMS\ Noise}\right) \quad (3)$$

Signal-to-Noise Ratio (SNR)

The ratio of the RMS value of the actual input signal to the RMS sum of all other spectral components below the Nyquist frequency, excluding harmonics and DC. The value is expressed in decibels.

Total Harmonic Distortion (THD)

The ratio of the RMS sum of the harmonics to the fundamental. It is expressed in decibels. For the ADAQ7768-1, THD is defined as:

$$THD\ (dB) = 20\ \log\left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}\right) \quad (4)$$

where:

V_2, V_3, V_4, V_5, V_6 are the RMS amplitudes of the second to sixth harmonics.

V_1 is the RMS amplitude of the fundamental.

Signal-to-Noise and Distortion (SINAD) Ratio

The ratio of the RMS value of the actual input signal to the RMS sum of all other spectral components below the Nyquist frequency, including harmonics but excluding DC. The value is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

The difference, in decibels, between the RMS amplitude of the input signal and peak spurious signal (including harmonics).

TERMINOLOGY

Intermodulation Distortion

With inputs consisting of sine-waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa and nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the RMS sum of the individual distortion products to the RMS amplitude of the sum of the fundamentals expressed in decibels.

Device-to-Device Phase Mismatch

It measures the deviation of the phase delay of a single ADAQ7768-1 device relative to the average phase delay of a group of ADAQ7768-1 devices at a given input signal frequency. It shows how well the phase response of the data acquisition signal chain matches among channels. The typical specification is equal to ±1σ (standard deviation) of the distribution.

Device-to-Device Phase Mismatch Drift

It quantifies how much the device-to-device phase mismatch distribution widens/tightens across temperature. A positive sign indicates a wider phase mismatch distribution as temperature increases, while a negative sign indicates a tighter phase mismatch distribution as temperature increases. The typical specification is computed as shown in Figure 90, while the maximum is six times this value.

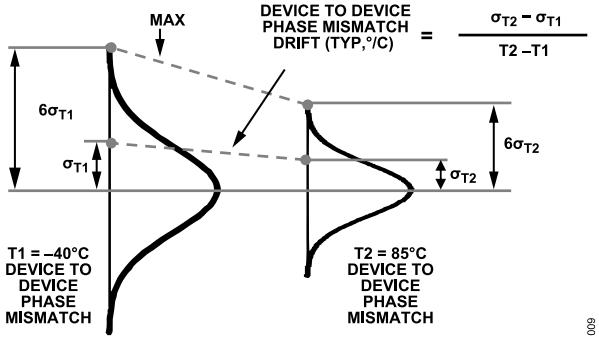

Figure 90. Device-to-Device Phase Mismatch Drift Calculation

Power Supply Rejection Ratio (PSRR)

Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

THEORY OF OPERATION

ANALOG INPUT

The wide common-mode input range and high CMRR of the ADAQ7768-1 allow its IN+ and IN– pins to swing with an arbitrary relationship to each other, allowing the device to accept a wide variety of signal swings, including unipolar and bipolar single-ended, pseudodifferential and fully-differential signals, as shown in Figure 91.

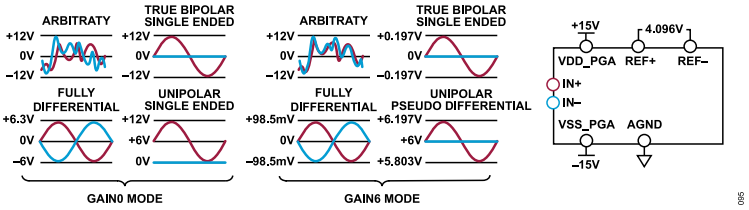

Figure 91. Input Signal Example

THEORY OF OPERATION

Arbitrary Input

The two-tone test shown in Figure 92 demonstrates the arbitrary input drive capability of the ADAQ7768-1. This test simultaneously drives IN+ with a −6.5 dBFS, 19.5 kHz single-ended sine-wave, and IN− with a −6.5 dBFS, 20.5 kHz single-ended sine-wave. Together, these signals sweep the analog inputs across a wide range of common-mode and differential-mode voltage combinations, similar to the more general arbitrary input signal case. They also have a simple spectral representation. An ideal differential converter with no common-mode sensitivity digitizes this signal as two −6.5 dBFS spectral tones, one at each sine-wave frequency. The FFT plot in Figure 92 demonstrates the ADAQ7768-1 response and how it approaches this in the ideal manner.

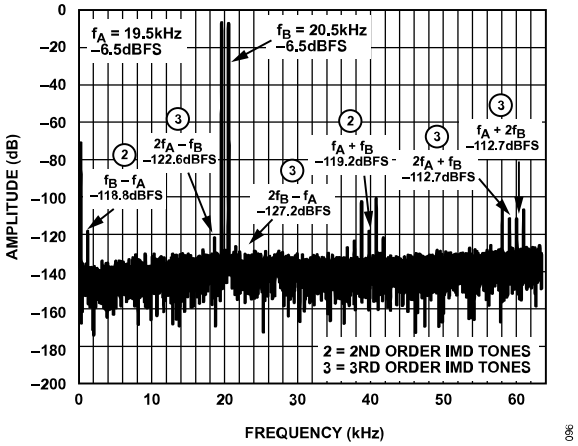

Figure 92. Two-Tone Input, IN+ = −6.5 dBFS, 19.5 kHz Sine, IN− = −6.5 dBFS, 20.5 kHz Sine, ODR = 256 kSPS, V_{REF} = 4.096 V, AFE_GAIN = 0.325 V/V (Gain 0 Mode)

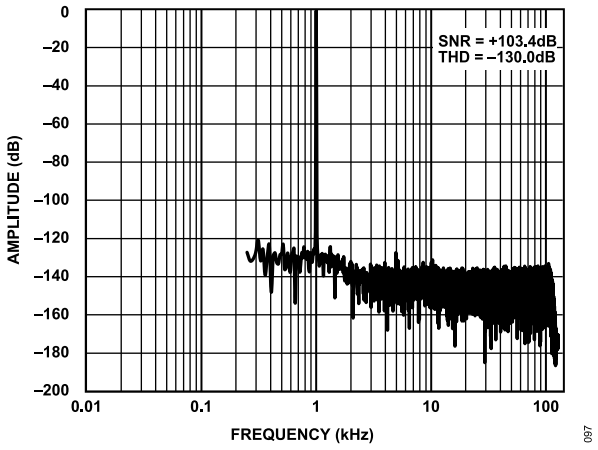

Figure 93. Bipolar Single-Ended Input, IN+ = −0.5 dBFS, 1 kHz Sine, IN− = 0V, ODR = 256 kSPS, V_{REF} = 4.096V, AFE_GAIN = 1.3 V/V (Gain 2 Mode)

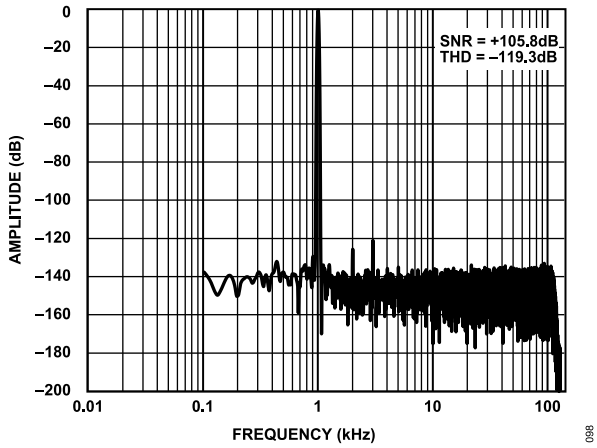

Figure 94. Fully Differential Input, −0.5 dBFS, 1 kHz Sine, V_{CM} = 0 V, ODR = 256 kSPS, V_{REF} = 4.096 V, AFE_GAIN = 0.325 V/V (Gain 0 Mode)

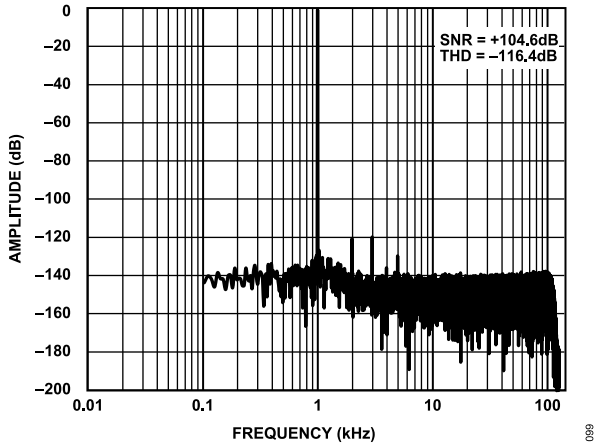

Figure 95. Fully Differential Input, −0.5 dBFS, 1 kHz Sine, V_{CM} = 0 V, ODR = 256 kSPS, V_{REF} = 4.096 V, AFE_GAIN = 1.3 V/V (Gain 2 Mode)

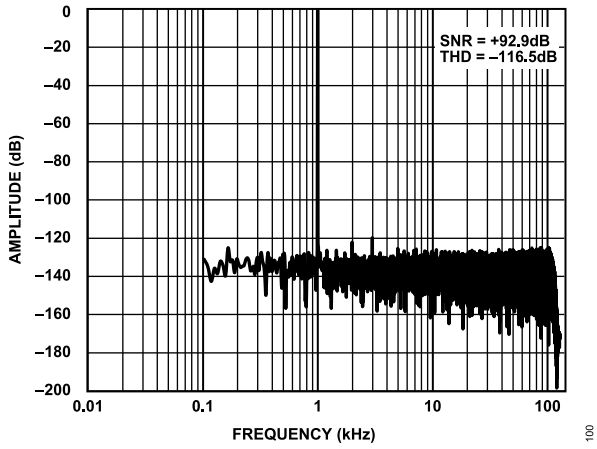

Figure 96. Fully Differential Input, −0.5 dBFS, 1 kHz Sine, V_{CM} = 0 V, ODR = 256 kSPS, V_{REF} = 4.096 V, AFE_GAIN = 20.8 V/V (Gain 6 Mode)

THEORY OF OPERATION

ANALOG INPUT RANGE

Input Voltage Range

The absolute voltage on the IN+ and IN− pins are limited to VDD_PGA −3 V and VSS_PGA + 3.25 V in all gain modes.

Differential Input Range

The differential signal amplitude depends on the front-end signal gain and reference voltage level. The maximum differential input voltage can be calculated by:

$$V_{IN+} - V_{IN-} = \frac{\pm V_{REF}}{AFE\_GAIN} \quad (5)$$

$$AFE\_GAIN = PGIA\_GAIN \times FDA\_GAIN \quad (6)$$

where, FDA_GAIN = 1.3 V/V

Common-Mode Input Range

The input signal common-mode range depends on the PGIA supply voltage and gain mode. Instrumentation amplifiers traditionally specify a valid input common-mode range and an output swing range. This however, often fails to identify swing limitations associated with internal nodes, as they experience a combination of gained differential signal and common-mode signal. Figure 97 and Figure 98 show the operating region where a valid output is produced for the various gain modes of the ADAQ7768-1.

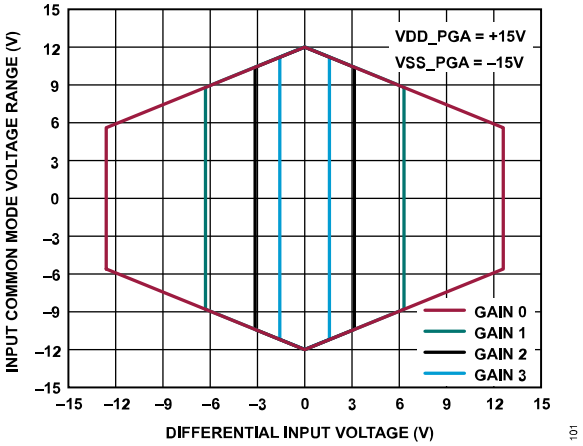

Figure 97. Input Range Diamond Plot for Various Gains

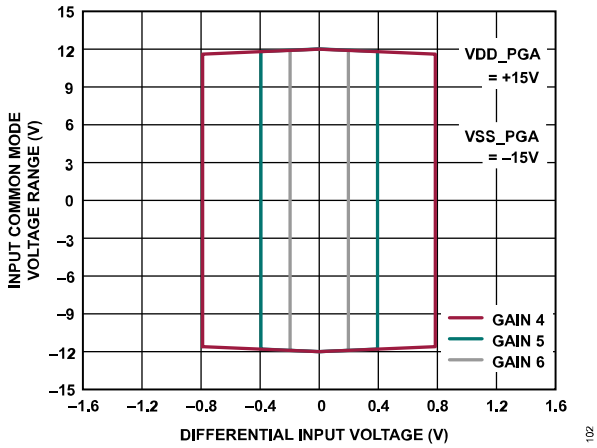

Figure 98. Input Range Diamond Plot for Various Gains

SELECTING THE INPUT RANGE

The input range of the ADAQ7768-1 is controlled by its front-end PGIA gain and can be programmed to its desired setting using a digital interface with three parallel gain control pins: GAIN0, GAIN1, and GAIN2. The logic threshold for the gain control pins is specified with respect to the AGND pins. Any voltage between AGND and AGND + 0.6 V on the gain control pins generates a logic-low (L) state for that pin; any voltage between AGND + 1.5 V and VDD_PGA on the gain control pins generates a logic-high (H) state for that pin. The gain of the PGIA and ADAQ7768-1 input range are programmed according to Table 8.

THEORY OF OPERATION

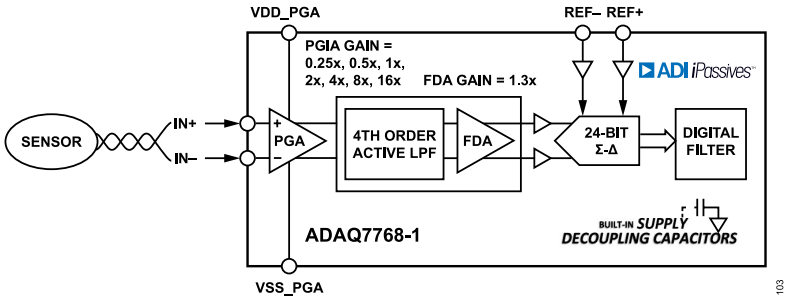

Figure 99. ADAQ7768-1 Top Level Core Signal Chain

Table 8. Input Range Selection Truth Table

Gain Mode	GAIN 2 Pin Logic	GAIN 1 Pin Logic	GAIN 0 Pin Logic	PGIA Gain (V/V)	FDA Gain (V/V)	Total Signal Chain Gain (V/V)	Differential Input Range with V_{REF} = 4.096 V (V)	Common-Mode Input Range with Full Scale Input Signal V_{REF} = 4.096 V (V)
Gain 0	High	High	Low	0.25	1.3	0.325	±12.603	±5.6
Gain 1	High	Low	High	0.5	1.3	0.65	±6.302	±8.8
Gain 2	High	Low	Low	1	1.3	1.3	±3.151	±10.4
Gain 3	Low	High	High	2	1.3	2.6	±1.575	±11.2
Gain 4	Low	High	Low	4	1.3	5.2	±0.788	±11.6
Gain 5	Low	Low	High	8	1.3	10.4	±0.394	±11.8
Gain 6	Low	Low	Low	16	1.3	20.8	±0.197	±11.9

THEORY OF OPERATION

ANTI-ALIASING FILTER

The input-signal bandwidth of the ADAQ7768-1 is dominated by its digital filter. The user can program the decimation ratio to adjust the digital filter bandwidth. The filter bandwidth can also be fine-tuned through the change of MCLK frequency. For example, with the wideband low ripple FIR filter option and an ODR = 256 kSPS, the −3 dB bandwidth of the overall signal chain is equal to the digital filter bandwidth of 0.433 × ODR = 110.85 KHz. The same filter has a stop band of 0.499 × ODR and a stop-band attenuation of -100 dB. As with any sampled system, the ADAQ7768-1's digital filter does not reject signals around the signal sampling frequency, f_S. Figure 100 shows that an additional analog anti-aliasing filter is required to reject signals around f_S to prevent out-of-band signals from folding back to the band of interest.

The digital filter does not reject signals within the frequency range of $f_S \pm f_{3dB}$. The ADAQ7768-1's core ADC samples at a frequency of 2 x f_{MOD}. In the normal operating mode with f_{MOD} = MCLK/2, the ADC's sampling frequency f_S is equal to MCLK.

The ADAQ7768-1 features a fourth-order analog anti-aliasing filter designed to achieve 100 dB of rejection at 16.384 MHz. Combining its analog anti-aliasing filter with its wideband low ripple filter, the ADAQ7768-1 can reject all of the out-of-band signals by a minimum of 105 dB.

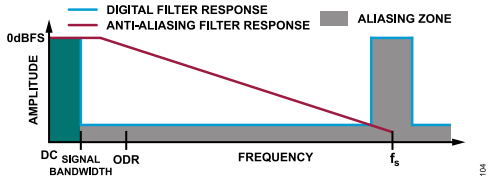

Figure 100. Simplified Illustration of the Overall Frequency Response

THEORY OF OPERATION

Magnitude and Phase Response

The anti-aliasing filter is designed to achieve optimal aliasing rejection level with minimum magnitude and phase distortion to the in-band signal. Its typical magnitude droop is 2.3 mdB at 20 kHz and 20 mdB at 100 kHz. The filter's passband phase response in the passband is also highly linear. With the help of ADI's iPASSIVES™ technology, the filter has a tightly controlled −3 dB corner at 330 kHz, allowing for a minimal device-to-device phase mismatch, as shown in Figure 105. This performance is highly desirable in simultaneously sampling applications, such as using three accelerometers for the X, Y, and Z axes to locate faults in machine health monitoring applications. This can be challenging and expensive to achieve in signal chains using discrete resistors and capacitors, which vary with respect to their tolerance and temperature drift behavior, making this performance a key advantage of signal chain µModules.

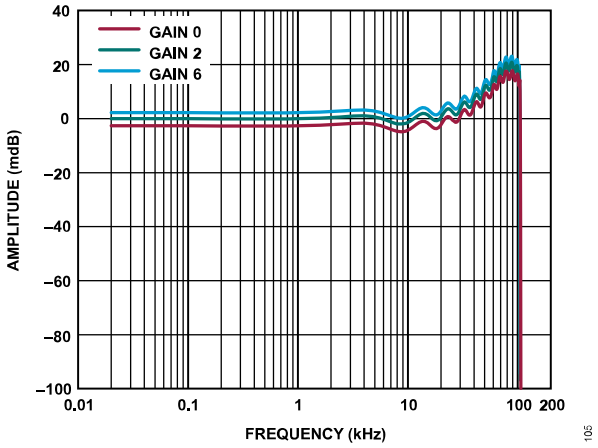

Figure 101. AAF Frequency Response at Various Gain Modes

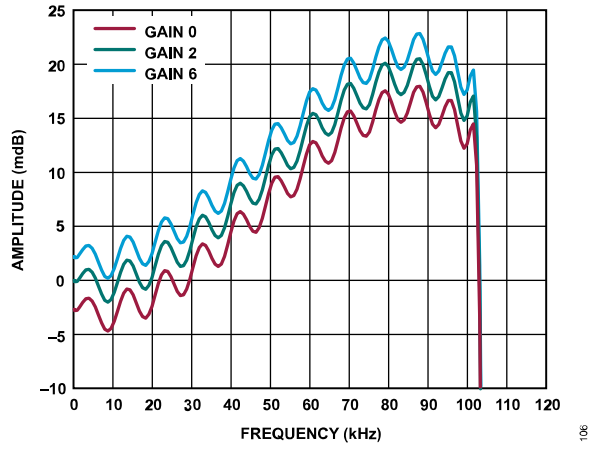

Figure 102. AAF Passband Droop at Various Gain Modes

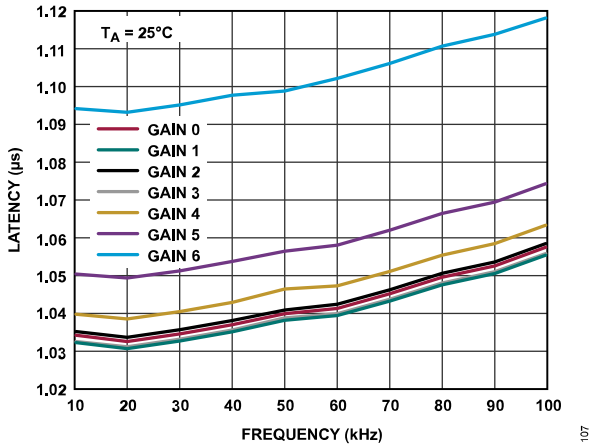

Figure 103. Group Delay vs. Frequency Across All Gain Modes at 25°C

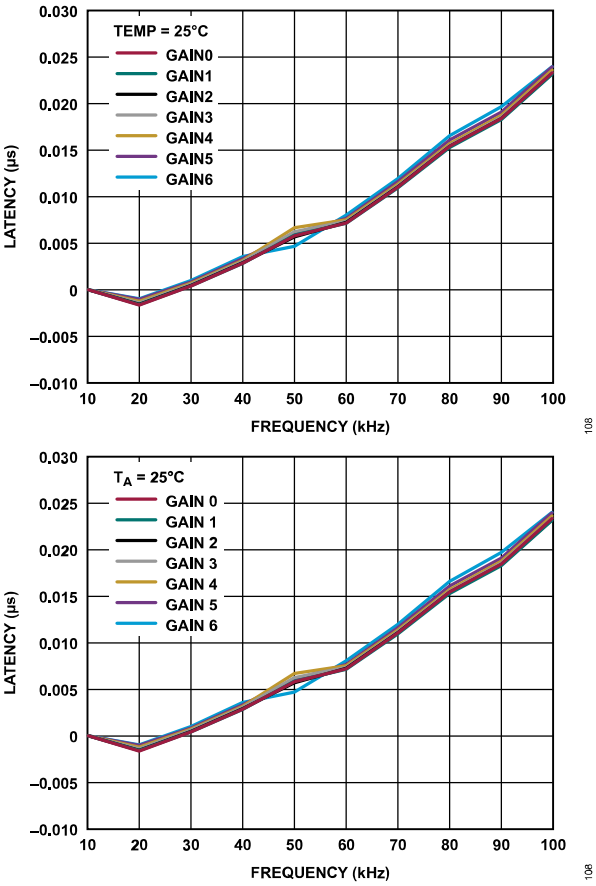

Figure 104. Group Delay vs. Frequency Across All Gain Modes at 25°C, Normalized to Delay at 10 kHz

THEORY OF OPERATION

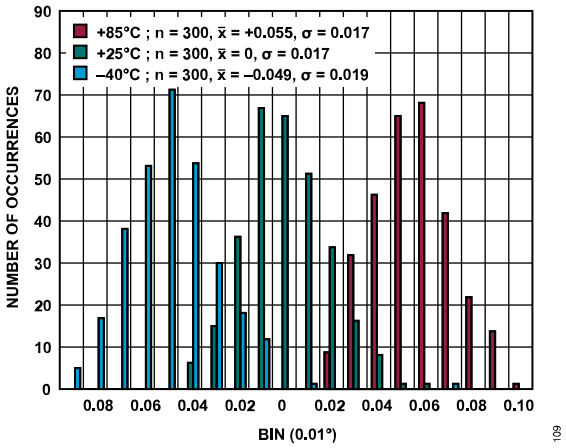

Figure 105. Device-to-Device Phase Mismatch Histogram, 20 kHz, AFE_GAIN = 1.3 V/V (Gain 2 Mode), Normalized to the Mean Value at 25°C

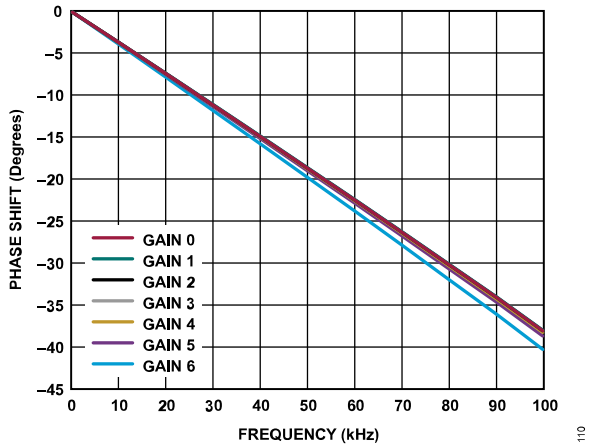

Figure 106. Analog Front-End (AFE) Phase Response Across All Gain Modes

Calculations on AFE Phase Performance

All mismatches on the phase angle across gain or temperature, or from device-to-device are due to the analog front-end and its filters, as the group delay of the digital filter is constant.

Phase Angle Over Frequency

The ADAQ7768-1 has a linear phase response. To interpolate the phase delay from one frequency to another, the ideal formula is:

$$\frac{\theta_1}{f_{IN\_1}} = \frac{\theta_2}{f_{IN\_2}} \quad (7)$$

where, θ_x is the phase delay of the AFE using an input frequency of f_{IN_x}.

However, due to small nonlinearities, calibrate the formula in terms of its slope and intercept.

$$\theta = m \times f_{IN} + b + nonlinearity \quad (8)$$

where:

m is the slope.

b is the y-intercept of the linear equation of the phase delay with respect to the input frequency over the span of the passband frequency using endpoint method, as shown in Figure 106.

Using the phase delay at 10 kHz to 100 kHz as endpoints, a typical device has a worst nonlinearity of approximately −0.3°, as shown in Figure 107.

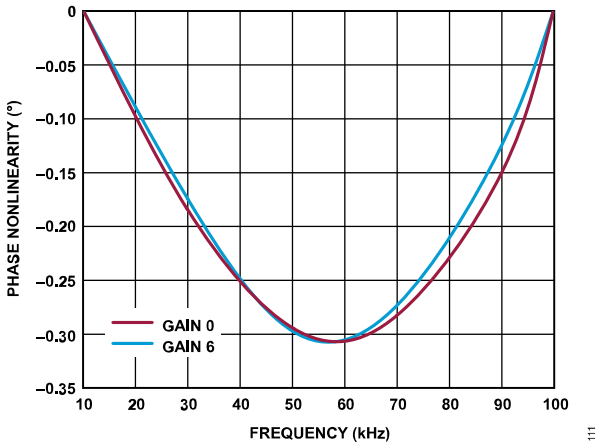

Figure 107. Analog Front-End (AFE) Phase Nonlinearity vs. Passband Frequency, Endpoint Method (10 kHz to 100 kHz)

Phase Angle Mismatch Over Gain

The phase angle mismatch over gain is the phase delay of Gain modes 1 to 6 relative to its phase delay at Gain 0 mode of the same device. The typical specification is the average phase angle mismatch over gain across a large number of devices, while the maximum (or minimum) specification is six standard deviations (σ) away from the typical value.

For example, Typical Device A has 7.4° phase delay from input to output at 20 kHz on Gain 0 mode. On Gain 6 mode, the same Device A typically has:

7.4° + 0.427° (typical specification) = 7.827° phase delay.

If a Device B is operating on the maximum phase angle mismatch over gain specifications, then, on Gain 6 mode, the same Device B has:

7.4° + 0.491° (maximum specification) = 7.891° phase delay.

THEORY OF OPERATION

Phase Angle Drift

The phase angle drift defines the rate of change of the phase delay over temperature of a single device at a given input signal frequency. The drift in degrees/°C is calculated using the endpoint method over the full operating temperature range of -40°C and 85°C. The typical specification is the average phase angle drift across a large number of devices, while the maximum (or minimum) specification is six standard deviations (σ) away from the typical value.

For example, Typical Device A has a 7.4° phase delay from input to output at 20 kHz at T_A = 25°C on Gain 0 mode. At T_A = 85°C, the same Device A typically has:

7.4° + 0.00073°/°C (typical specification) × (85°C − 25°C) = 7.4438° phase delay.

If a Device B is operating on the maximum phase angle drift specifications, then the same Device B typically has:

7.4° + 0.00137°/°C (maximum specification) × (85°C − 25°C) = 7.4822° phase delay.

Device-to-Device Phase Angle Mismatch

The device-to-device phase angle mismatch measures the deviation of the phase delay of a single ADAQ7768-1 device relative to the average phase delay of a group of ADAQ7768-1 devices at a given input signal frequency. It shows how well the phase response of the data acquisition signal chain matches between channels. The typical specification is equal to ±1σ (standard deviation) of the distribution, while the maximum (or minimum) is six times this value.

For example, measuring the phase delay of a large number of devices with 20 kHz input at Gain 0 mode, Device C has a phase delay on the minimum side of the distribution, which is (−) 0.11° earlier than the average. Again, Device D has a phase delay on the maximum side of the distribution, which is (+) 0.11° later than the average. The phase angle mismatch between Device C and Device D is:

+0.11° (max) – (−) 0.11° (minimum) = 0.22°

This is the worst-case phase angle mismatch between any two ADAQ7768-1 devices (at Gain 0 mode, T_A = 25°C, 20 kHz input).

Device-to-Device Phase Angle Mismatch Drift

The device-to-device phase angle mismatch drift quantifies how much the device-to-device phase angle mismatch standard deviation (σ) widens/tightens across temperature at a given input signal frequency. A positive sign indicates a wider phase mismatch distribution as temperature increases, while a negative sign indicates a tighter phase mismatch distribution as temperature increases. This specification is calculated using the endpoint method over the full operating temperature range of -40°C and 85°C. The typical specification is the change in 1σ per °C, while the maximum is six times this value, as shown in Figure 108.

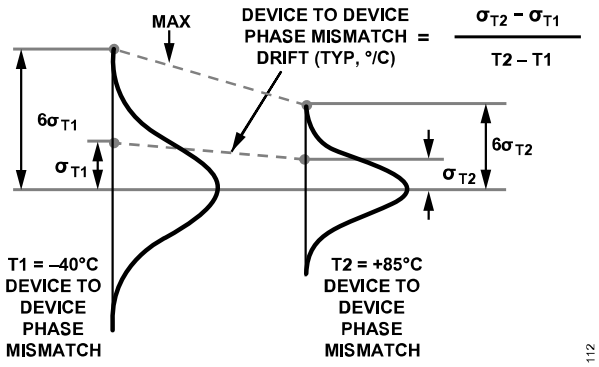

Figure 108. Device-to-Device Phase Mismatch Drift Calculation

Measuring the device-to-device phase angle mismatch standard deviation (σ) of a large number of devices at 25°C with 20 kHz input at Gain 0 mode, it is observed that the σ of the distribution is 0.018°. To interpolate the standard deviation at another temperature:

$\sigma_{T2} = \sigma_{T1}$ + Device-to-Device Phase Angle Mismatch Drift × ($T_2 - T_1$)

Example: $\sigma_{-40°C}$ = 0.018° + (−21 µ°/°C) × (−40°C − 25°C) = 0.019365°

FDA POWER MODES

The ADAQ7768-1 fully differential amplifier (FDA) is a low-noise, low-distortion amplifier that can drive high resolution and high performance Σ-Δ analog-to-digital converters (ADC).

The FDA's two selectable power modes are the low-power and full-power modes. The FDA low- power mode is ideal for DC input applications due to its low 1/f noise at low gain settings, 0.325 V/V and 0.65 V/V system gains. The full-power mode offers better linearity performance at a higher current consumption.

Figure 109 shows the connection between M0_FDA, M1_FDA, and M0_ADC, M1_ADC. The connection sets the FDA to full-power mode. To set the FDA to low-power mode, the M0_FDA needs to be pulled to ground, while keeping the M1_FDA and M1_ADC connected, as shown in Figure 110.

THEORY OF OPERATION

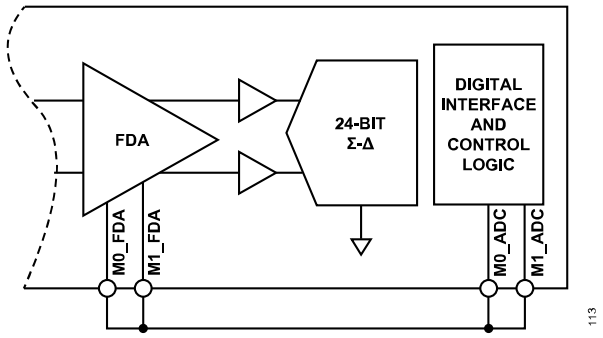

Figure 109. FDA Full-Power Mode Connection

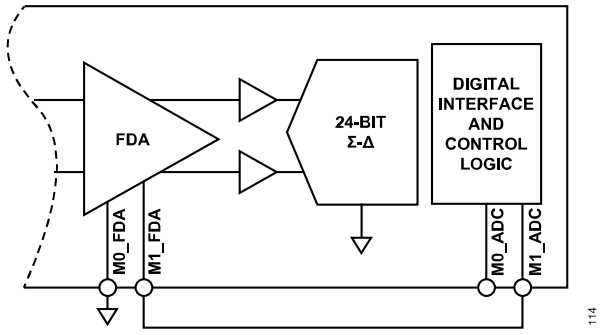

Figure 110. FDA Low-Power Mode Connection

LINEARITY BOOST BUFFERS

The ADAQ7768-1 has a pair of linearity boost buffers placed between the driver amplifier and core ADC. The user has the option to turn them on to boost the linearity performance of the device. The linearity boost buffers add no noise to the signal chain performance and consume additional 2 mA typical current (as a pair) on the VDD_ADC supply.

The linearity boost buffers are enabled by default. The user can turn them off in the SPI control mode by setting the LINEARITY_BOOST_A_OFF and LINEARITY_BOOST_B_OFF (Bits[1:0] in Register 0x16) to zero. The linearity boost buffers are always enabled in the $\overline{\text{PIN}}$ control mode.

REFERENCE INPUT AND BUFFERING

The ADAQ7768-1 has differential reference inputs, REF+ and REF−. The absolute input reference voltage range is from 1 V to VDD_ADC − AGND.

The reference inputs can be configured for a fully buffered input on each of the REF+ and REF− pins, a precharge buffered input, or to bypass both buffers.

Use of either the full buffers or precharge buffers reduces the burden on the external reference when driving large loads or multiple devices. The fully buffered input to the reference pins provides a high-impedance input node and enables the use of the ADAQ7768-1 in ratiometric applications, where the ultra-low source impedance of a traditional external reference is not available.

In the $\overline{\text{PIN}}$ control mode, the reference precharge buffers are on by default. In the SPI mode, the user can choose full or precharge buffers.

The reference input current scales linearly with the modulator clock rate.

For MCLK = 16.384 MHz in the fast mode, the reference input current is ~80 µA/V unbuffered and ~20 µA with the precharge buffers enabled.

With the precharge buffers off, REF+ = 5 V and REF− = 0 V.

REF± = 5 V × 80 µA/V = + 400 µA

With the precharge buffers on, REF+ = 5 V, and REF− = 0 V.

REF± = approximately 20 µA

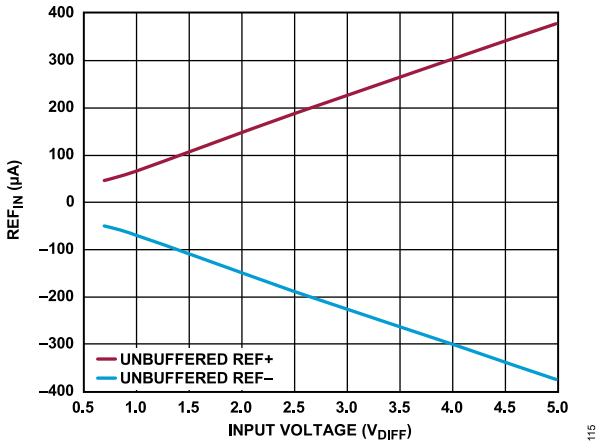

Figure 111. Reference Input Current (REF_{IN}) vs. Input Voltage, Unbuffered REF+ and REF−

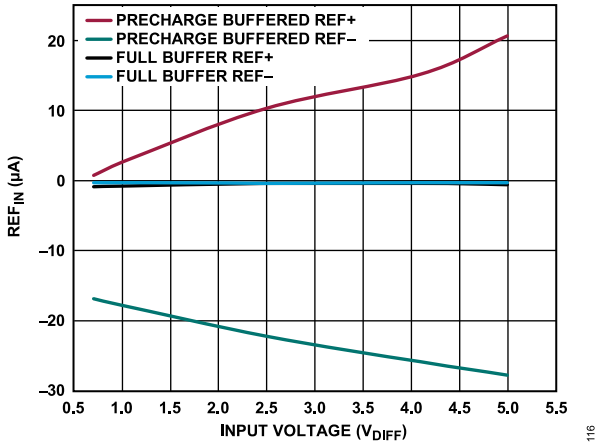

Figure 112. Reference Input Current (REF_{IN}) vs. Input Voltage, Precharge Buffered REF+ and REF−, and Full Buffer REF+ and REF−

For the best performance and headroom, use a 4.096 V reference, such as the ADR444 or ADR4540, that can both be supplied by a 5 V rail and shared to the VDD_ADC supply.

THEORY OF OPERATION

A reference detect function is available in the SPI control mode. See the Reference Detection section for details.

CORE CONVERTER

The ADAQ7768-1 can use up to a 5 V reference and convert the differential voltage between the analog inputs with the differential input range of ±V_{REF}/−AFE_GAIN to a digital output. The 24-bit conversion result is in MSB first, twos complement format. Figure 113 shows the ideal transfer functions for the ADAQ7768-1.

Use the following equation to convert from codes to volts, assuming the codes are first converted from twos complement to straight binary:

$$Voltage = \frac{(Code - MidscaleCode) \times 2 \times V_{REF}}{2^{24} \times AFE\_GAIN}$$

where, the Midscale Code is 0x800000 in straight binary.

0x7FFFFF in Table 9 is converted to 0xFFFFFF in straight binary.

Use the previous equation to calculate a voltage in the V_{REF}+ to V_{REF}− range.

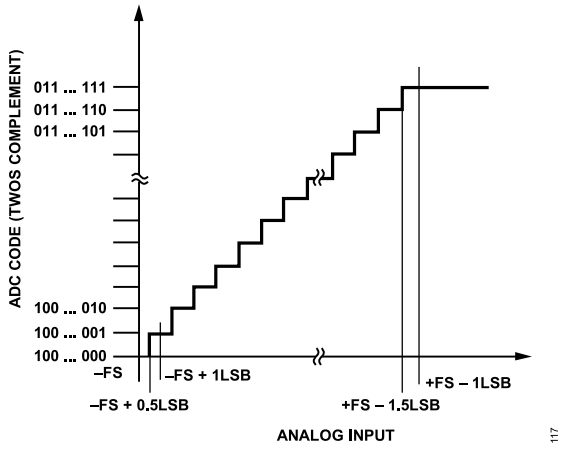

Figure 113. ADC Ideal Transfer Functions (FS is Full-Scale)

Table 9. Output Codes and Ideal Input Voltages

Description	Analog Input (IN+ − IN−) (V)	Digital Output Code, Twos Complement (Hex)
FS − 1 LSB	+V_{REF}/AFE_GAIN × (1−1/2^{23})	0x7FFFFF
Midscale + 1 LSB	+V_{REF}/AFE_GAIN/2^{23}	0x000001
Midscale	0	0x000000
Midscale − 1 LSB	−V_{REF}/AFE_GAIN /2^{23}	0xFFFFFF
−FS + 1 LSB	−V_{REF}/AFE_GAIN *(1−1/2^{23})	0x800001
−FS	−V_{REF}/AFE_GAIN	0x800000

POWER SUPPLIES

The ADAQ7768-1 has several power supplies to power the analog front-end and ADC. To simplify the connection, the ADAQ7768-1 has an internal LDO that can be used to supply the voltage of the VDD_ADC, VDD2_ADC, VDD2_PGA, and VDD_FDA (as shown in Figure 114). The LDO can also power the ADR4540 reference for the REF+ and REF- pins. The LDO input can handle inputs ranges from 5.1 V to 5.5 V. For proper operation, it is recommended to use 1µF capacitor at the input and output of the LDO.

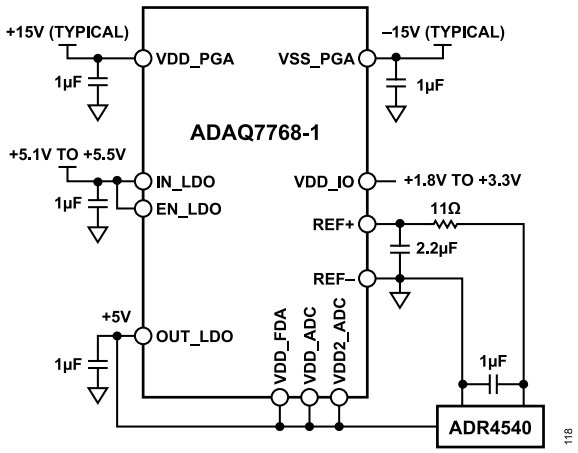

Figure 114. ADAQ7768-1 Power Supply Connection Using Internal LDO

If the LDO is not used during normal operation, it is recommended to keep all the LDO pins floating. Figure 115 illustrates the use of an external power supply for VDD_ADC, VDD2_ADC, VDD2_PGA, VDD_FDA, and the reference if the internal LDO is not preferred.

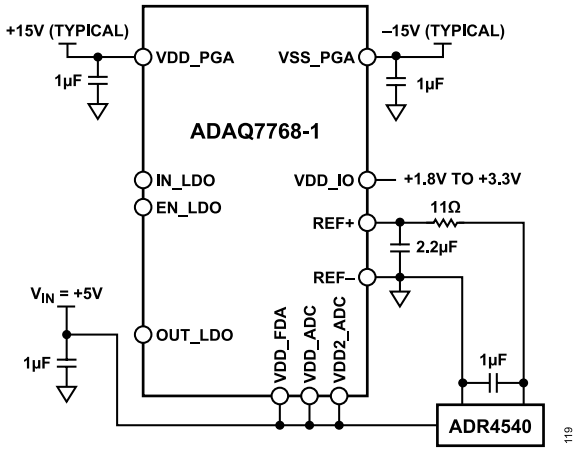

Figure 115. ADAQ7768-1 Power Supply Connection Using External 5 V Supply

The VDD_PGA and VSS_PGA supply power to the front-end amplifiers of the PGIA.

The VDD2_PGA supplies the PGIA output driver with the positive supply. The return current of the output driver flows back through the VSS_PGA.

The VDD_FDA supplies power to the ADC driver.

The VDD_ADC supply powers the linearity boost buffer, core ADC front-end, and reference input.

THEORY OF OPERATION

The VDD2_ADC supply connects to an internal 1.8 V analog LDO regulator. This regulator powers the ADC core. VDD2_ADC − AGND can range from 5.5 V (maximum) to 2.0 V (minimum).

VDD_IO powers the internal 1.8 V digital LDO regulator. This regulator powers the digital logic of the ADC. VDD_IO sets the voltage levels for the SPI of the ADC. VDD_IO is referenced to DGND, and VDD_IO − DGND can vary from 3.6 V (maximum) to 1.7 V (minimum).

POWER SUPPLY DECOUPLING

The ADAQ7768-1 has built-in 0.1 µF supply decoupling capacitors on VDD_PGA, VSS_PGA, VDD2_PGA, VDD_FDA, VDD_ADC, and VDD2_ADC supply pins. Together with the internal LDO, these features minimize the needed components to operate the ADAQ7768-1.

Figure 116 shows the AC PSRR of the internal LDO while it is connected to VDD2_PGA, VDD_FDA, and VDD_ADC with the internal supply decoupling capacitor, and the recommended 1 µF decoupling capacitor at the OUT_LDO pin, as shown in Figure 114.

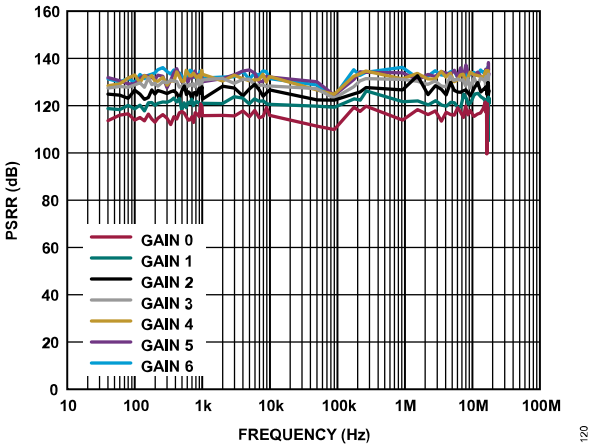

Figure 116. LDO AC PSRR, Using the 0.1 µF Internal Decoupling Capacitors of VDD2_PGA, VDD_FDA, VDD_ADC, VDD2_ADC, and Recommended 1 µF External Decoupling Capacitor at OUT_LDO

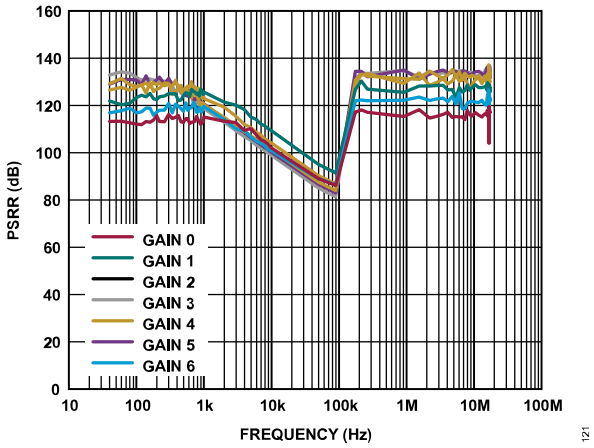

Figure 117. VDD_PGA AC PSSR vs. All Gains, Using the Internal 0.1 µF Supply Decoupling Capacitor Only

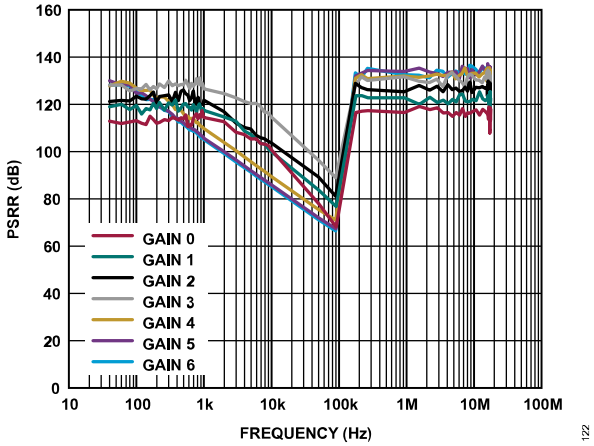

Figure 118. VSS_PGA AC PSSR vs. All Gains, Using the Internal 0.1 µF Supply Decoupling Capacitor Only

Only the VDD_IO requires an external decoupling capacitor. Figure 119 shows the AC power supply rejection ratio (PSRR) of the VDD_IO supply pin using a 0.1 µF external supply decoupling capacitor and the AC PSRR with an additional 1µF supply decoupling capacitor.

THEORY OF OPERATION

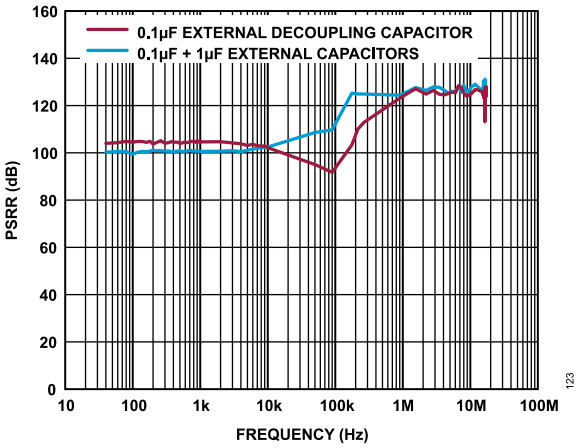

Figure 119. VDD_IO AC PSRR Using External 0.1 µF and Additional 1 µF Supply Decoupling Capacitor

POWER STANDBY

Each functional block of the ADAQ7768-1 can be put into the standby mode. The device can achieve 0.96 mW of total power consumption while all functional blocks are put into the standby mode.

CLOCKING AND SAMPLING TREE

The ADAQ7768-1 core ADC receives a controller clock (MCLK) signal. The MCLK signal can be sourced from one of four options: a CMOS clock, a crystal connected between the XTAL1 and XTAL2 pins, an LVDS signal, or the internal clock. The MCLK signal received by the ADAQ7768-1 defines the core ADC's sigma-delta modulator clock rate (f_{MOD}) and, in turn, the sampling frequency of the modulator of 2 × f_{MOD}.

$$f_{MOD} = \frac{MCLK}{MCLK\_DIV}$$

To determine f_{MOD}, select one of the four clock divider settings: MCLK/2, MCLK/4, MCLK/8, or MCLK/16. For example, to maximize the ODR or input bandwidth, an MCLK rate of 16.384 MHz is required. Select an MCLK divider (MCLK_DIV) equal to 2 for a modulator frequency of 8.192 MHz.

Control of the settings for the modulator frequency differs in the $\overline{\text{PIN}}$ control mode vs. SPI control mode.

In the $\overline{\text{PIN}}$ control mode, the MODEx pins determine the modulator frequency. The MODEx pins are also used to select the filter type and decimation rate. See Table 17 for the $\overline{\text{PIN}}$ control mode setting for MODEx pins.

It is recommended to keep the f_{MOD} frequency high to maximize the out-of-band tone rejection from the front-end anti-aliasing filter. Increase the decimation ratio if low input bandwidth is required.

CLOCKING AND CLOCK SELECTION

The ADAQ7768-1 has an internal oscillator for initial power-up of the device. After the ADAQ7768-1 completes the start-up routine, a clock handover occurs to the external MCLK. The ADAQ7768-1 counts the falling edges of the external MCLK over a given number of internal clock cycles to determine if the clock is valid and of a frequency of at least 600 kHz. If there is a fault with the external MCLK, the handover does not occur, the ADAQ7768-1 clock error bit is set, and the ADAQ7768-1 continues to operate from the internal clock.

In the SPI control mode, use the clock source bits in the POWER_CLOCK register (Register 0x15) to set the external MCLK source. Four clock options are available: internal oscillator, external CMOS, crystal oscillator, or LVDS. If selecting the LVDS clock option, the clock source must be selected using the CLOCK_SEL bits (Bits[7:6] in Register 0x15).

In the $\overline{\text{PIN}}$ control mode, the CLK_SEL pin sets the external MCLK source. Three clock options are available in the $\overline{\text{PIN}}$ control mode: an internal oscillator, an external CMOS, or a crystal oscillator. The CLK_SEL pin is sampled on power-up.

Set the EN_ERR_EXT_CLK_QUAL bit (Bit 0 in Register 0x29) to turn off the clock qualification. Turning off the clock qualification allows the use of slower external MCLK rates outside the recommended MCLK frequency.

CLK_SEL Pin

If CLK_SEL = 0 in the $\overline{\text{PIN}}$ control mode, the CMOS clock option is selected and must be applied to the MCLK pin. In this case, tie the XTAL1 pin to DGND.

If CLK_SEL = 1 in the $\overline{\text{PIN}}$ control mode, the crystal option is selected and must be connected between the XTAL1 and XTAL2 pins.

In the SPI control mode, the CLK_SEL pin does not determine the MCLK source used and CLK_SEL must be tied to DGND.

Using the Internal Oscillator

In some cases, conversion using an internal clock oscillator may be preferred, such as in isolated applications, where DC input voltages must be measured. Converting AC signals with the internal clock is not recommended because using the internal clock can result in degradation of the signal-to-noise ratio (SNR) due to jitter.

DIGITAL FILTERING

The ADAQ7768-1 has three types of digital filters:

- Wideband low ripple FIR filter, −3 dB at 0.433 × ODR (6 rates)
- Sinc5 low latency filter, −3 dB at 0.204 × ODR (8 rates)
- Sinc3 low latency filter, −3 dB at 0.2617 × ODR, widely programmable data rate

THEORY OF OPERATION

Decimation Rate Control

The ADAQ7768-1 has programmable decimation rates for the sinc3, sinc5, and wideband low ripple FIR digital filters. The decimation rates allow to band limit the measurement, which reduces the speed and input bandwidth, but increases the resolution because there is further averaging in the digital filter. Control of the decimation rate on the ADAQ7768-1 when using the SPI control is set in the DIGITAL_FILTER register (Register 0x19) for the sinc5 and wideband low ripple FIR filters.

The decimation rate of the sinc3 filter is controlled using the SINC3_DEC_RATE_LSB (Register 0x1A) and SINC3_DEC_RATE_MSB registers (Register 0x1B). These registers combine to provide 13 bits of programmability. Set the decimation rate by incrementing the value in these registers by one and multiplying the value by 32. For example, setting a value of 0x5 in the SINC3_DEC_RATE_LSB register results in a decimation rate of 192 for the sinc3 filter.

In the $\overline{\text{PIN}}$ control mode, the MODE0 pin controls the decimation ratio. Only decimation rates of ×32 and ×64 are available for use with the sinc5 and wideband filter options. See Table 17 for the full list of options available in the $\overline{\text{PIN}}$ control mode.

Table 10. Decimation Rate Options

	Available Decimation Rates	
Filter Option	**SPI Control Mode**	**Pin Control Mode**
Wideband Low Ripple FIR	×32, ×64, ×128, ×256, ×512, ×1024	×32, ×64
Sinc5	×8, ×16, ×32, ×64, ×128, ×256, ×512, ×1024	×8, ×32, ×64
Sinc3	Programmable decimation rate	50 Hz and 60 Hz output only, based on a 16.384 MHz MCLK.

Wideband Low Ripple FIR Filter

The FIR filter is a wideband low ripple, input pass-band up to 0.433 × ODR. The wideband low ripple FIR filter has almost full attenuation at 0.5 × ODR (Nyquist), maximizing anti-alias protection. Figure 121 shows the ADAQ7768-1 wideband low ripple FIR filter pass-band ripple of 2.3 mdB up to 20 kHz and 20 mdB up to 100 kHz. The wideband low ripple FIR filter is a 64-order digital filter. The group delay of the filter is 34/ODR. After a sync pulse, there is an additional delay from the $\overline{\text{SYNC\_IN}}$ rising edge to fully settled data. Table 11 shows the time from a $\overline{\text{SYNC\_IN}}$ pulse to both the first $\overline{\text{DRDY}}$ and to fully-settled data for various ODR values.

The wideband low ripple FIR filter can be selected in one of six different decimation rates to choose the optimal input bandwidth and speed of the conversion vs. the desired resolution.

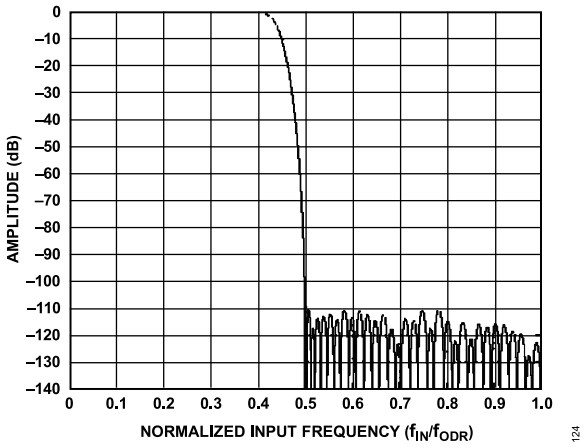

Figure 120. Low Ripple FIR Filter Frequency Response

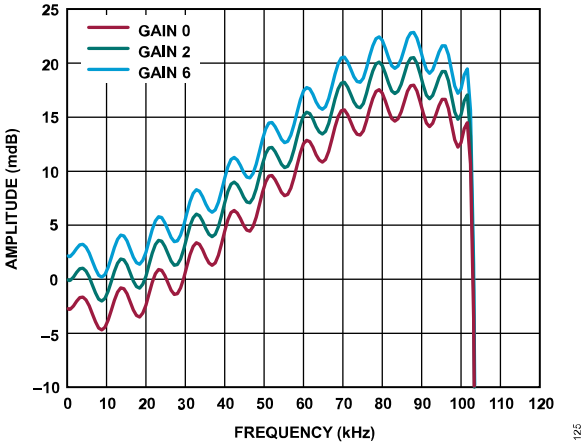

Figure 121. Wideband Low Ripple FIR Filter Passband Ripple, Normalized to Gain 2 Mode

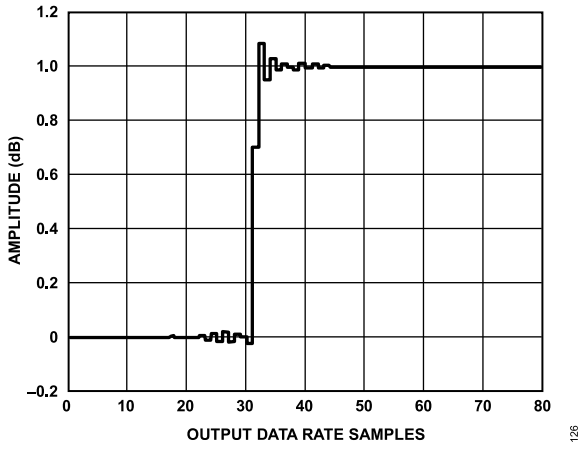

Figure 122. Wideband Low Ripple FIR Filter Step Response

THEORY OF OPERATION

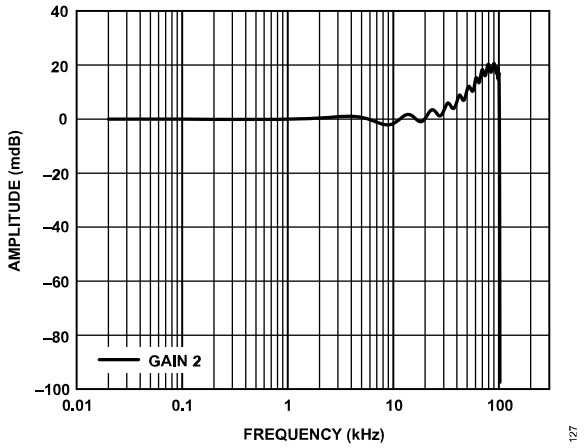

Figure 123. Wideband Low Ripple FIR Filter Magnitude Flatness Response, ODR = 256 kSPS, Gain 2 Mode Normalized

Figure 121 shows the ADAQ7768-1 magnitude flatness using the wideband low ripple FIR filter at 256 kSPS ODR. Using the following calculation, the wideband low ripple FIR filter offers −0.1 dB attenuation up to 104.7 kHz, as seen in Figure 124.

$$-0.1 \text{ dB Passband} = 0.406 \times \text{ODR} = 104.7 \text{ kHz}$$

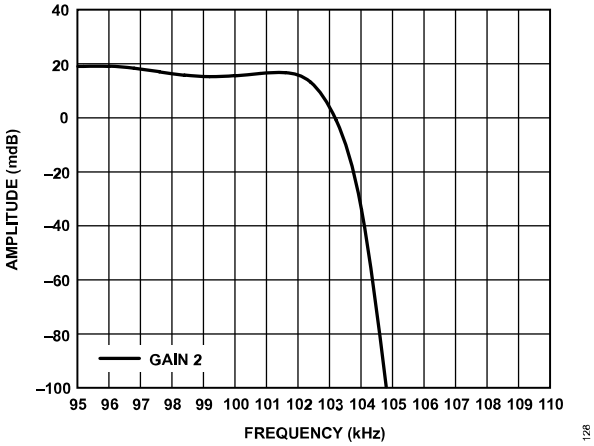

Figure 124. Wideband Low Ripple FIR Filter, −0.1dB Passband

Table 11. Low Ripple FIR Filter to Settled Data

		ODR (kSPS)		MCLK Periods	
MCLK Divide Setting	Decimation Ratio	MCLK = 16.384 MHz	MCLK = 13.107 MHz	Delay from First MCLK Rise After $\overline{\text{SYNC\_IN}}$ Rise to First $\overline{\text{DRDY}}$ Rise	Delay from First MCLK Rise After $\overline{\text{SYNC\_IN}}$ Rise to Earliest Settled $\overline{\text{DRDY}}$ Rise
MCLK/2	32	256	204.8	284	4,252
	64	128	102.4	413	8,349
	128	64	51.2	797	16,669
	256	32	25.6	1,565	33,309
	512	16	12.8	3,101	66,589
	1024	8	6.4	6,157	133,133
MCLK/4	32	128	102.4	428	8,364
	64	64	51.2	812	16,684
	128	32	25.6	1,580	33,324
	256	16	12.8	3,116	66,604
	512	8	6.4	6,188	133,164
	1024	4	3.2	12,300	266,252
MCLK/16	32	32	25.6	1,674	33,418
	64	16	12.8	3,202	66,690
	128	8	6.4	6,274	133,250
	256	4	3.2	12,418	266,370
	512	2	1.6	24,706	532,610
	1024	1	0.8	49,154	1,064,962

THEORY OF OPERATION

Sinc5 Filter

The sinc5 filter in the ADAQ7768-1 enables a low latency signal path useful for DC inputs on control loops, or for where user-specific postprocessing is required. For output data rate of 512 kSPS and lower, the sinc5 filter has a −3 dB bandwidth of 0.204 × ODR. Setting the output data rate of sinc5 filter to 1.024 MSPS makes its −3dB bandwidth close to the analog anti-alias filter cutoff. Due to the influence of the anti-alias filter, the sinc5 filter −3 dB bandwidth slightly decreases to 198.4 kHz. Table 21 shows the noise performance for the sinc5 filter across power modes and decimation ratios.

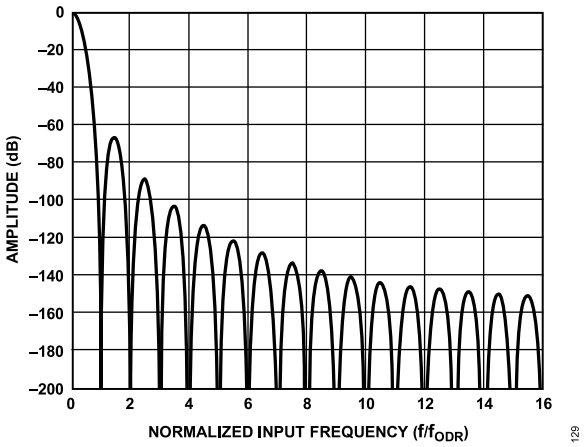

Figure 125. Sinc5 Filter Frequency Response

The impulse response of the filter is five times the ODR. For 250 kSPS ODR, the time to settle the data fully is 20 µs. For the 1 MSPS ODR, the time to settle the data fully is 5 µs.

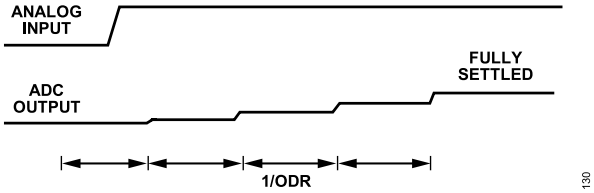

Figure 126. Sinc5 Filter Step Response

Table 12 shows the time from a $\overline{\text{SYNC\_IN}}$ pulse to both the first $\overline{\text{DRDY}}$ and to fully-settled data for various ODR values for the sinc5 filter.

Table 12. Sinc5 Filter to Settled Data

		ODR (kSPS)		MCLK Periods	
MCLK Divide Setting	Decimation Ratio	MCLK = 16.384 MHz	MCLK = 13.107 MHz	Delay from First MCLK Rise After $\overline{\text{SYNC\_IN}}$ Rise to First $\overline{\text{DRDY}}$ Rise	Delay from First MCLK Rise After $\overline{\text{SYNC\_IN}}$ Rise to Earliest Settled $\overline{\text{DRDY}}$ Rise
MCLK/2	8	1024	819.2	46	110
	16	512	409.6	62	190
	32	256	204.8	94	350
	64	128	102.4	162	674
	128	64	51.2	295	1,319
	256	32	25.6	561	2,609
	512	16	12.8	1,093	5,189
	1024	8	6.4	2,173	10,365
MCLK/4	8	512	409.6	79	207
	16	256	204.8	111	367
	32	128	102.4	175	687
	64	64	51.2	310	1,334
	128	32	25.6	576	2,624
	256	16	12.8	1,108	5,204
	512	8	6.4	2,172	10,364
	1024	4	3.2	4,332	20,716
MCLK/16	8	128	102.4	278	790
	16	64	51.2	406	1,430
	32	32	25.6	662	2,710

THEORY OF OPERATION

Table 12. Sinc5 Filter to Settled Data (Continued)

		ODR (kSPS)		MCLK Periods	
MCLK Divide Setting	Decimation Ratio	MCLK = 16.384 MHz	MCLK = 13.107 MHz	Delay from First MCLK Rise After $\overline{SYNC\_IN}$ Rise to First $\overline{DRDY}$ Rise	Delay from First MCLK Rise After $\overline{SYNC\_IN}$ Rise to Earliest Settled $\overline{DRDY}$ Rise
	64	16	12.8	1,194	5,290
	128	8	6.4	2,258	10,450
	256	4	3.2	4,386	20,770
	512	2	1.6	8,642	41,410
	1024	1	0.8	17,282	82,818

Programming for 1.024 MSPS Output Data Rate

A 1.024 MSPS sinc5 filter path exists for users seeking an even higher ODR than is achievable using the wideband low ripple FIR filter. This path is quantization noise limited. Therefore, it is best suited for users requiring minimum latency for control loops or implementing custom digital filtering on an external field-programmable gate array (FPGA) or digital signal processor (DSP).

To configure the sinc5 filter for 1.024 MSPS output data rate, write 001 to the FILTER bits [6:4] of the DIGITAL_FILTER register (Register 0x19). The ADAQ7768-1 automatically changes the decimation rate to 8 and output data length is reduced to 16 bits from 24 bits due to the maximum speed limitation of the digital serial interface.

For example, to program the ADAQ7768-1 to 1.024 MSPS output data rate from power up using 16.384 MHz MCLK, while using the CMOS_MCLK as the clock source, the subsequent SPI writes can be used.

- Data 0x33 to Register 0x15
- Data 0x10 to Register 0x19

Sinc3 Filter

The sinc3 filter in the ADAQ7768-1 enables a low latency signal path useful for DC inputs on control loops, or eliminates unwanted known interferers at specific frequencies. The sinc3 filter path incorporates a programmable decimation rate to reject known interferers. Decimation rates from 32 to 185,280 are achievable using the sinc3 filter. The sinc3 filter has a −3 dB bandwidth of 0.2617 × ODR. Table 13 and Table 14 show the minimum rejection measured at the frequencies of interest with a 50 Hz ODR.

For example, to calculate the DEC_RATE of the sinc3 filter with a 16.384 MHz MCLK and ODR of 50 Hz with MCLK_DIV = 2, use this formula:

$$DEC\_RATE = \frac{MCLK}{MCLK\_DIV \times ODR}$$

$$DEC\_RATE = \frac{16.384MHz}{2 \times 50} = 163,840$$

To program the sinc3 decimation ratio, the user must first calculate the equivalent sinc3 decimation ratio to be written on the SINC3_DECIMATION_RATE registers (Registers 0x1A and 0x1B) using the following equation:

$$Value = \frac{DEC\_RATE}{32} - 1 = 5119$$

To set the decimation ratio to 163,840, write the equivalent binary value of 5119 to the SINC3_DECIMATION_RATE registers (Registers 0x1A and 0x1B) because the value in the register is incremented by 1 and then multiplied by 32 to give the actual decimation rate.

Table 13. Sinc3 Filter 50 Hz Rejection, 50 Hz ODR and Decimate by 163,840

Frequency Band (Hz)	Minimum Measured Rejection (dB)
50 ± 1	101
100 ± 2	102
150 ± 3	102
200 ± 4	102

THEORY OF OPERATION

Table 14. Sinc3 Filter 50 Hz and 60 Hz Rejection, 50 Hz ODR and Decimate by 163,840

Frequency Band (Hz)	Minimum Measured Rejection (dB)
50 ± 1	81
60 ± 1	67
100 ± 2	83
120 ± 2	72
150 ± 3	86
180 ± 3	78
200 ± 4	90
240 ± 4	87

The impulse response of the filter is three times the ODR. For 250 kSPS ODR, the time to settle the data fully is 12 µs.

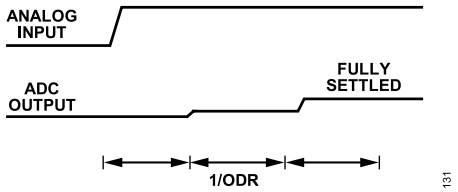

Figure 127. Sinc3 Filter Step Response

To reject 50 Hz tones, program the ODR of the sinc3 filter to 50 Hz (see Figure 128). It is also possible to simultaneously reject both 50 Hz and 60 Hz by setting Bit 7 in the DIGITAL_FILTER register (Register 0x19). Both 50 Hz and 60 Hz line frequencies can be rejected in this configuration (see Figure 128).

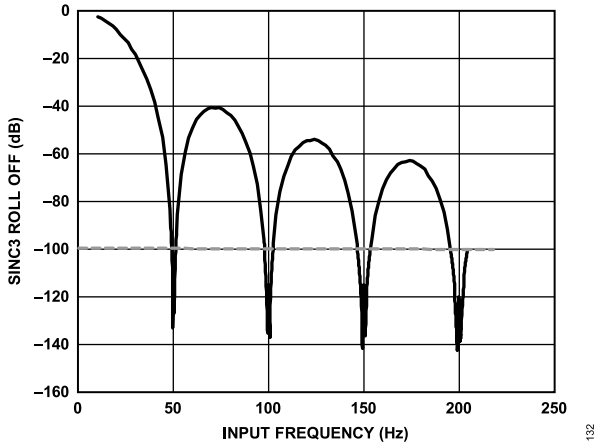

Figure 128. Sinc3 Filter Frequency Response Showing 50 Hz Rejection, 50 Hz ODR, ×163,840 Decimation

Programming for 50 Hz, 60 Hz, and 50 Hz and 60 Hz Rejection

Table 15. Sinc3 Filter to Settled Data

			ODR (kSPS)		MCLK Periods	
MCLK Divide Setting	Decimation Ratio	Equivalent Sinc3 Decimation Ratio	MCLK = 16.384 MHz	MCLK = 13.107 MHz	Delay from First MCLK Rise After $\overline{SYNC\_IN}$ Rise to First $\overline{DRDY}$ Rise	Delay from First MCLK Rise After $\overline{SYNC\_IN}$ Rise to Earliest Settled $\overline{DRDY}$ Rise
MCLK/2	32	0	256	204.8	127	255
	64	1	128	102.4	191	447
	128	3	64	51.2	319	831
	256	7	32	25.6	575	1,599
	512	15	16	12.8	1,087	3,135
	1024	31	8	6.4	2,111	6,207
	163,840	5119	0.05	0.04	327,743	983,103
MCLK/4	32	0	128	102.4	241	497
	64	1	64	51.2	369	881
	128	3	32	25.6	625	1,649
	256	7	16	12.8	1,137	3,185
	512	15	8	6.4	2,161	6,257
	1024	31	4	3.2	4,209	12,401
	81,920	2559	0.05	0.04	327,793	983,153
MCLK/16	32	0	32	25.6	926	1,950
	64	1	16	12.8	1,438	3,486
	128	3	8	6.4	2,462	6,558
	256	7	4	3.2	4,510	12,702
	512	15	2	1.6	8,606	24,990
	1024	31	1	0.8	16,798	49,566
	20,480	639	0.05	0.04	328,094	983,454

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ADC SPEED AND PERFORMANCE

The ADAQ7768-1 offers a wide selection of ODR depending on the digital filter used. The ADAQ7768-1 can have an ODR as low as 1 kSPS using the wideband low ripple FIR filter and sinc5 filter, and 0.0125 kSPS using the sinc3 filter. This can be achieved using a high decimation ratio and operating the modulator at the lowest possible sampling rate. For example, with the wideband low ripple FIR filter option, 1 kSPS ODR can be achieved using MCLK = 16.384 MHz, decimation rate = 1024, and f_{MOD} = MCLK / 16.

The user must take note that the ADAQ7768-1 modulator samples on the rising and falling edge of the f_{MOD} and outputs data to the digital filter at a rate of f_{MOD}. There is a zero in the frequency response profile of the modulator centered at the odd multiples of f_{MOD}, which means there is no foldback from frequencies at the f_{MOD} rate and at odd multiple rates. However, the modulator is open to noise for even multiples of f_{MOD}. There is no attenuation at these zones.

For optimum performance, it is recommended to use MCLK = 16.384 MHz and MCLK_DIV = 2. This sets the f_{MOD} = 8.192 MHz, and by keeping the f_{MOD} frequency high, it maximizes the out-of-band tone rejection from the front-end anti-aliasing filter.

The default controller clock divider setting for the ADAQ7768-1 is MCLK_DIV = 16. To configure the MCLK divider to MCLK = 2, write 11 to MCLK_DIV bits [5:4] of the POWER_CLOCK register (Register 0x15) after power-up.

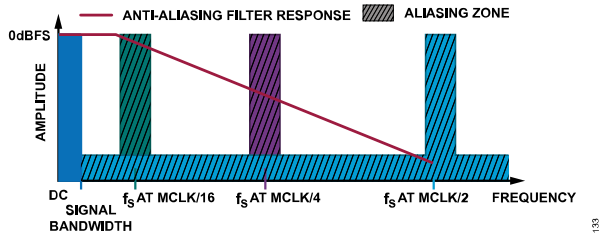

Figure 129. Anti-Alias Filter Response vs. MCLK Divider

Figure 129 shows the AAF rejection relative to the sampling frequency. Using higher MCLK divider results in lower sampling frequency with reduced rejection from the anti-alias filter.

DEVICE CONFIGURATION METHOD

The ADAQ7768-1 has two options f to control the device functionality. On power-up, the mode is determined by the state of the $\overline{PIN}$/SPI pin. The two modes of configuration are:

- SPI: Over a 3-wire or 4-wire SPI (complete configurability).
- $\overline{PIN}$: Pin-strapped digital logic inputs (a subset of complete configurability).

On power-up, the user must apply a soft or hard reset to the device when using either control mode. A $\overline{SYNC\_IN}$ pulse is also recommended after the reset or after any change to the device configuration. Choose between controlling and configuring over the SPI or through pin connections only.

The first design decision is setting the ADAQ7768-1 in either the SPI or $\overline{PIN}$ mode of configuration. In either mode, the digital host reads the ADC data over the SPI port lines.

$\overline{PIN}$ Configuration

An overview of the $\overline{PIN}$ control mode features is as follows:

- No SPI write access to the device.
- Pins control all functions.
- ADC results read back over the SPI pins.
- ADC result includes an 8-bit status header output after each conversion result.
- SDI pin can be used to create a daisy-chain of multiple devices operating in the $\overline{PIN}$ mode.

SPI Control

An overview of the SPI control mode features is as follows:

- Standard SPI Mode 3 interface for register access, where the ADC always behaves as an SPI target.
- Indication of a new conversion through the $\overline{DRDY}$ pin output.
  - A second method allows the user to merge the ready signal within the DOUT output stream, which allows a reduction in the number of lines across an isolation barrier.
- Read back conversions by writing 8 bits to address the ADC register and reading back the result from the register.
- Continuous readback mode, which is enabled through an SPI write. There is no need to supply the 8 bits to address the ADC_DATA register (Register 0x2C). Data readback occurs on the application of SCLK. The $\overline{DRDY}$ pin indicates that a conversion result is complete and can be used to trigger a readback of the conversion result.
- In the continuous read back mode, there is the option to append either the 8-bit status header or an 8-bit CRC check, or both.

PIN CONTROL MODE OVERVIEW

The $\overline{PIN}$ control mode eliminates the need for SPI communication to set the required mode of operation. For situations where the user requires a single, known configuration, reduce routing signals to the digital host. The $\overline{PIN}$ control mode is useful in digitally-isolated applications, where minimal configuration is needed. The $\overline{PIN}$ control mode offers a subset of the core functionality and ensures a known state of operation after power-up, reset, or a fault condition on the power supply. In the $\overline{PIN}$ control mode, the linearity boost buffers and the reference input precharge buffers are enabled by default for best performance.

An automatic sync pulse drives out on the $\overline{SYNC\_OUT}$ pin in the $\overline{PIN}$ control mode when the device is either initially powered up or after a reset. A $\overline{SYNC\_OUT}$ pulse also occurs when a GPIOx

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pin toggles, meaning after a change to the $\overline{\text{PIN}}$ control mode settings of the device, the synchronization is automatically performed. For this synchronization to work, tie $\overline{\text{SYNC\_OUT}}$ to $\overline{\text{SYNC\_IN}}$, eliminating the need to provide a synchronous $\overline{\text{SYNC\_IN}}$ pulse. The $\overline{\text{SYNC\_OUT}}$ of one device can also be tied to the $\overline{\text{SYNC\_IN}}$ of many devices when the synchronization of multiple devices is required. If synchronization of multiple devices is required, all devices must share a common MCLK.

Data Output Format

The $\overline{\text{PIN}}$ control mode has a set output format for conversion data. The rising $\overline{\text{DRDY}}$ edge indicates that a new conversion is ready. The next 24 serial clock falling edges clock out the 24-bit ADC result. The following eight serial clocks output the status bits of the ADAQ7768-1. The ADC data is output MSB first in the twos complement format. If further SCLK falling edges are applied to the ADC after clocking out the status bits, the logic level applied to SDI is clocked out, similar to a daisy-chain scenario. Figure 130 shows an extra serial clock edge (33rd falling edge). If an extra serial clock edge occurs, the logic level of the SDI pin clocks out.

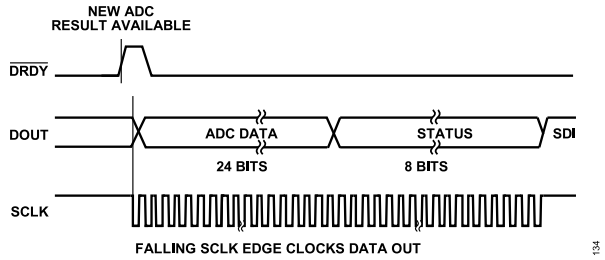

Figure 130. $\overline{\text{PIN}}$ Mode Data Output Format (Without the $\overline{\text{CS}}$ Signal)

Table 16. Differences in the Control and Interface Pin Functions in the $\overline{\text{PIN}}$ and SPI Control Modes

	Pin Function	
Name	**$\overline{\text{PIN}}$ Control Mode**	**SPI Control Mode**
MODE0/GPIO0	MODE0 configuration pin	GPIO0 pin
MODE1/GPIO1	MODE1 configuration pin	GPIO1 pin
MODE2/GPIO2	MODE2 configuration pin	GPIO2 pin
MODE3/GPIO3	MODE3 configuration pin	GPIO3 pin
$\overline{\text{CS}}$	SPI pin for readback of ADC conversion results.	SPI for full configuration of the ADAQ7768-1 through a register read/write and readback of the ADC conversion results.
SCLK	SPI pin for readback of ADC conversion results.	SPI for full configuration of the ADAQ7768-1 through a register read/write and readback of the ADC conversion results.
SDI	SPI pin for readback of ADC conversion results.	SPI for full configuration of the ADAQ7768-1 through a register read/write and readback of the ADC conversion results.
DOUT/$\overline{\text{RDY}}$	SPI pin for readback of ADC conversion results.	SPI for full configuration of the ADAQ7768-1 through a register read/write and readback of the ADC conversion results.

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Diagnostics and Status Bits

The $\overline{\text{PIN}}$ control mode offers a subset of diagnostics features. Internal errors are reported in the status header output with the data conversion results for each channel.

The status header reports the internal CRC errors, memory map flipped bits, and the undetected external clock, indicating a reset is required. The status header also reports filter settled and filter saturated signals. Users can determine when to ignore data by monitoring these error flags.

If a significant error shows in the status bits, a reset of the ADC using the $\overline{\text{RESET}}$ pin is recommended because, like in the $\overline{\text{PIN}}$ mode, there is no way to interrogate further for specific errors.

Daisy-Chaining ($\overline{\text{PIN}}$ Control Mode Only)

Daisy-chaining devices allow multiple devices to use the same data interface lines by cascading the outputs of multiple ADCs from separate ADAQ7768-1 devices. Daisy-chaining devices is only possible in the $\overline{\text{PIN}}$ control mode.

When configured for daisy-chaining, only one ADAQ7768-1 device has its data interface in direct connection with the digital host.

For the ADAQ7768-1, cascading the DOUT/$\overline{\text{RDY}}$ pin of the upstream ADAQ7768-1 device to the SDI pin of the next downstream ADAQ7768-1 device in the chain implements this daisy-chaining. The ability to daisy-chain devices and the limit on the number of devices that can be handled by the chain is dependent on the serial clock frequency used and the time available to clock through multiple 32-bit conversion outputs (24-bit conversion + 8-bit status) before the next conversion is complete.

The daisy-chaining feature is useful to reduce component count and to wire connections to the controller.

Figure 131 shows an example of daisy-chaining multiple ADAQ7768-1 devices.

The daisy-chain scheme depends on all devices receiving the same MCLK and SCLK, being synchronized, and being configured with the same decimation rate. The chip select signal ($\overline{\text{CS}}$) gates each conversion chain of data, its rising edge resetting the SPI to a known state after each conversion ripples through. The ADAQ7768-1 device furthest from the controller must have its SDI pin tied to VDD_IO, logic high.

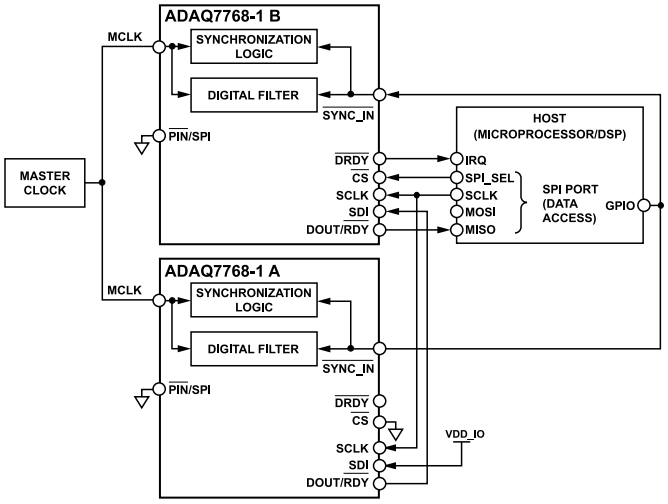

Figure 131. Daisy-Chaining Multiple ADAQ7768-1 Devices

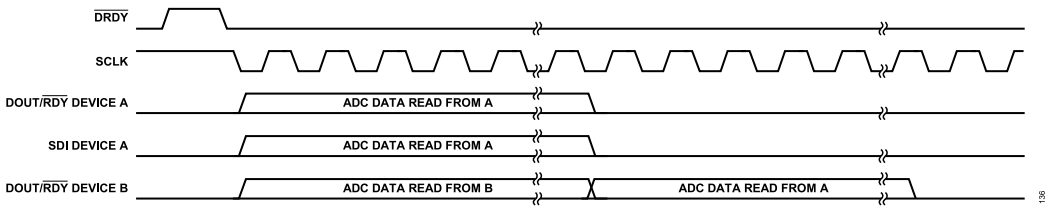

Figure 132. Data Output Format When Devices are Daisy-Chained ($\overline{\text{PIN}}$ Control Mode Only)

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Table 17. $\overline{PIN}$ Control Settings for MODEx Pins

MODEx Pin Settings					ADC Configuration			MCLK = 16.384 MHz
MODEx (Hex)	MODE3/ GPIO3	MODE2/ GPIO2	MODE1/ GPIO1	MODE0/ GPIO0	f_{MOD} Frequency	Filter	Decimation	ODR
0	0	0	0	0	MCLK/2	Low ripple FIR	×32	256 kHz
1	0	0	0	1	MCLK/2	Low ripple FIR	×64	128 kHz
2	0	0	1	0	MCLK/2	Sinc5	×32	256 kHz
3	0	0	1	1	MCLK/2	Sinc5	×64	128 kHz
4	0	1	0	0	MCLK/4	Low ripple FIR	×32	128 kHz
5	0	1	0	1	MCLK/4	Low ripple FIR	×64	64 kHz
6	0	1	1	0	MCLK/4	Sinc5	×32	128 kHz
7	0	1	1	1	MCLK/4	Sinc5	×64	64 kHz
8	1	0	0	0	MCLK/16	Low ripple FIR	×32	32 kHz
9	1	0	0	1	MCLK/16	Low ripple FIR	×64	16 kHz
A	1	0	1	0	MCLK/16	Sinc5	×32	32 kHz
B	1	0	1	1	MCLK/16	Sinc5	×64	16 kHz
C	1	1	0	0	MCLK/2	Sinc5	×8	1 MHz
D	1	1	0	1	MCLK/2	Sinc3 50 Hz and 60 Hz rejection[1]	×163,840	50 Hz
E	1	1	1	0	MCLK/16	Sinc3 50 Hz and 60 Hz rejection.[1]	×20,480	50 Hz
F	1	1	1	1	ADC Standby			

[1] Sinc3 filter, rejection of 50 Hz and 60 Hz. Rejection of 50 Hz and 60 Hz is possible only if the MCLK applied in the PIN control mode is equal to 16.384 MHz. The decimation rate is tuned internally for these pin mode settings so that the sinc filter notches fall at 50 Hz and 60 Hz.

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SPI CONTROL OVERVIEW

SPI control offers a superset of flexibility and diagnostics to the user. The categories described in Table 18 define the major controls, conversion modes, and diagnostic monitoring abilities enabled in the SPI control mode.

Table 18. SPI Control Capabilities

SPI Control	Capabilities	Meaning for the User
MCLK Division	MCLK/2 to MCLK/16	Customize clock frequency relating to the bandwidth of interest.
MCLK Source	CMOS, crystal, LVDS, and internal clock	Allows a distributed or local clock capability.
Digital Filter Style	Wideband low ripple FIR, Sinc5, Sinc3 (programmable)	Customize the latency and frequency response to the measurement target of the user and its bandwidth.
Interface Format	Bit length	Change between a 24-bit and a 16-bit conversion length in the continuous read mode.
	Status bits	View output device status bits with the ADC conversion results.
	CRC	Implement error checking when transmitting data.
	Data streaming	Stream conversion of data, eliminating interface write overhead.
Analog Buffers	Linearity boost buffer	Boost the linearity performance.
	Reference input precharge	Reduces reference input current, making it easier to filter the reference.
	Reference input full buffer	This full high-impedance buffer enables filtering of reference source and enables high-impedance sources, that is, reference resistors.
Conversion Modes	Single conversion	Return to standby after one conversion.
	One shot	Perform a conversion similar to a timed successive approximation register (SAR) conversion, in which the ADAQ7768-1 converts on a timed pulse.
	Continuous conversion	Normal operation keeps the modulator continually converting, offering the fastest response to a change on the input.
	Duty-cycled conversion	Save more power for point conversions. Times the rate of conversion and sets the time for the ADC to remain in standby after the conversion completes.
	Calibration	Run a calibration of the system and save gain calibration or offset calibration results to the system settings of the user by reading back from the gain/offset registers.
Conversion Targets	ADC inputs	Measure the input signal applied at the ADC input.
	Temperature sensor	Measure local temperatures with an on-chip temperature sensor. Used for relative temperature measurement.
	Diagnostic sources	Measure reference inputs and internal voltages for periodic functional safety checking.
GPIO Control	Up to four GPIOx pins	Control other local hardware (such as gain stages),to power down other blocks in the signal chain, or read local status signals over the SPI of the ADAQ7768-1.
System Offset and Gain Correction	System calibration routines	Correct offset and/or gain by writing to registers when the environment changes (that is, the temperature increases). Requires characterization of system errors to feed these registers.
Diagnostics	Internal checks and flags	Users can have the highest confidence in the conversion results.

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SPI CONTROL MODE

MCLK Source and Division

The (Register 0x15) MCLK division (MCLK_DIV) Bits[5:4] control the divided ratio between the MCLK applied at the input to the ADAQ7768-1 and the clock used by the ADC modulator (see the Power and Clock Control Register section). Select the division ratio best for configuration of the clocks.

In the SPI control mode, the following options for the MCLK input source are available, and these can be set from the (Register 0x15) CLOCK_SEL Bits[7:6] (see the Power and Clock Control Register section):

- CLOCK_SEL bits = 00 → CMOS input MCLK
- CLOCK_SEL bits = 01 → External crystal
- CLOCK_SEL bits = 10 → LVDS (exclusive to SPI control mode)
- CLOCK_SEL bits = 11 → Internal clock

When switching from one clock source to another, the user must apply soft reset to the device.

ADC Power-Down Mode

All blocks on the core ADC are turned off. A specific code is required to wake the ADC. All register contents are lost when entering the power-down mode. Ensure the FDA is powered down before entering the ADC into the power-down mode.

Standby Mode

The core ADC's analog clocking and power functions are powered down. The digital LDO and register settings are retained when in the standby mode. This mode is best used in scenarios where the ADC is not in use, briefly, and the user wants to save power.

SPI Synchronization

The ADAQ7768-1 can be synchronized over the SPI. The final SCLK rising edge of the command is the instance of synchronization. This command initiates the $\overline{\text{SYNC\_OUT}}$ pin to pulse active low and then back active high again. $\overline{\text{SYNC\_OUT}}$ is a signal synchronized internally to the MCLK of the ADC. By connecting the output of $\overline{\text{SYNC\_OUT}}$ to the $\overline{\text{SYNC\_IN}}$ input, the user can synchronize that individual ADC. Routing $\overline{\text{SYNC\_OUT}}$ to other ADAQ7768-1 devices also ensures the devices are synchronized, as long as the devices share a common MCLK source (see Figure 133).

It is recommended to perform synchronization functions directly after the $\overline{\text{DRDY}}$ pulse. If the ADAQ7768-1 $\overline{\text{SYNC\_IN}}$ pulse occurs too close to the upcoming $\overline{\text{DRDY}}$ pulse edge, the upcoming $\overline{\text{DRDY}}$ pulse may still be output because the $\overline{\text{SYNC\_IN}}$ pulse has not yet propagated through the device.

When using the $\overline{\text{SYNC\_OUT}}$ function with an VDD_IO voltage of 1.8 V, it is recommended to set the SYNC_OUT_POS_EDGE bit to a one (Register 0x1D, Bit 6).

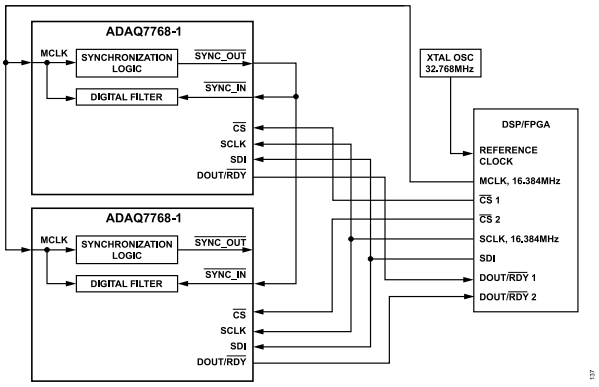

Figure 133. Basic SPI Synchronization Diagram

Offset Calibration

In the SPI control mode, the ADAQ7768-1 can calibrate the offset and gain. The user can alter the gain and offset of the ADAQ7768-1 and its subsystem. These options are available in the SPI control mode only.

The offset correction registers provide 24-bit, signed, twos complement registers for channel offset adjustment. If the channel gain setting is at the ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. As offset calibration occurs before gain calibration, the LSB ratio of −4/3 changes linearly with gain adjustment through the gain correction registers.

The Offset Calibration Registers section provides further register information and calibration instructions.

Gain Calibration

In the SPI control mode, the user can alter the gain and offset of the ADAQ7768-1 and its subsystem. These options are available in the SPI control mode only.

The ADC has an associated gain coefficient stored for each ADC after factory programming. Nominally, this gain is approximately the 0x555555 value (for an ADC channel). The user can overwrite the gain register setting. However, after a reset or power cycle, the gain register values revert to the hard-coded, programmed factory setting.

$$ADC\_DATA = \left[\frac{3 \times V_{IN} \times AFE\_GAIN}{V_{REF}} \times 2^{21} - \left(OffsetCal\right)\right] \times \frac{GainCal}{4} \times \frac{4,194,300}{2^{42}} \quad (9)$$

where:

ADC_DATA is in the twos complement format.

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OffsetCal is the decimal value from the Offset Calibration Registers.

GainCal is the decimal value from the Gain Calibration Registers.

The Gain Calibration Registers section provides further register information and calibration instructions.

Reset over SPI Control

The user can issue a reset command to the ADAQ7768-1 by writing to the SPI_RESET bits [1:0] in the Synchronization Modes and Reset Triggering Register (Register 0x1D). Two successive writes to these bits are required to initiate the device reset.

Resume from Shutdown

The shutdown mode features the lowest possible current consumption with all blocks on the device turned off, including the standard SPI. Therefore, to wake the ADC up from this mode, either a hardware reset on the $\overline{\text{RESET}}$ pin, or a specific code on the SPI SDI input, is required. The specific sequence required on the SDI consists of a 1 followed by 63 zeros, clocked in by SCLK while $\overline{\text{CS}}$ is low, which allows the system to wake up the ADAQ7768-1 from shutdown without using the $\overline{\text{RESET}}$ pin. This reset function is useful in isolated applications, where the number of pins brought across the isolation barrier must be minimized.

GPIO and $\overline{\text{START}}$ Functions

When operating in the SPI mode, the ADAQ7768-1 has additional GPIO functionality. This fully-configurable mode allows the device to operate four GPIOs. These pins can be configured as read or write in any order.

GPIO read is a useful feature because it allows a peripheral device to send information to the input GPIO. Then, this information can be read from the SPI of the ADAQ7768-1.

The GPIOx pins can be set as inputs or outputs on a per pin basis, and there is an option to configure the outputs as open-drain.

In the SPI control mode, one of the GPIOx pins can be assigned the function of the $\overline{\text{START}}$ input. The $\overline{\text{START}}$ function allows a signal asynchronous to MCLK to be used to generate the $\overline{\text{SYNC\_OUT}}$ signal to reset the digital filter path of the ADAQ7768-1. The $\overline{\text{START}}$ pin function can be enabled on GPIO3 through the EN_GPIO_START bit [3] of the Synchronization Modes and Reset Triggering Register (Register 0x1D).

SPI Mode Diagnostic Features

The ADAQ7768-1 includes diagnostic coverage across the internal blocks within the core ADC. The diagnostics in the following list allow the user to monitor the ADC and increase confidence in the fidelity of the data acquired:

- Reference detection
- Clock qualification
- CRC on SPI transaction
- Flags to detect an illegal register write
- CRC checks
- POR monitor
- MCLK counter

In addition, these diagnostics are useful in situations where instruments require remote checking of power supplies and references during initialization stages.

The diagnostics are selectable through enable registers. The flags for power-on reset (POR) and clock qualification are on by default. The flags are readable through registers, but also ripple through to the top level status bits that can be output with each ADC conversion, if desired.

Reference Detection

Write 1 to Bit 3 of the ADC_DIAG_ENABLE register (Register 0x29) to enable the reference detection block in the SPI control mode. When enabled, the error flags in the ADC_DIAG_ STATUS register (Register 0x2F). Any error flags then propagate through to the MASTER_STATUS register (Register 0x2D). The reference error flags when the reference applied on the REF+ pin is below 1/3 of (VDD_ADC − AGND).

Clock Qualification

The clock qualification check attempts to detect when a valid MCLK is detected. When the MCLK applied is greater than 600 kHz, the clock qualification passes. The error flags in both the ADC_DIAG_STATUS (Register 0x2F) and MASTER_STATUS (Register 0x2D) registers. If the clock detected is below the 600 kHz frequency threshold, or if an external MCLK is not detected, the clock qualification error bit is set to 1. To disable the clock qualification check, write 0 to Bit 0 of the ADC_DIAG_ENABLE register (Register 0x29).

CRC on SPI Transaction

See the Cyclic Redundancy Check (CRC) on Serial Interface section for more details.

Flags to Detect Illegal Register Write

See the SPI Control Error Handling section for more details.

CRC Checks

Enable CRC checks in the DIG_DIAG_ENABLE register (Register 0x2A) to check the state of the memory map of the ADAQ7768-1, and the internal random access memory (RAM) and fuse settings. If any of these errors flag on the device, perform a reset to return the device to a valid state.

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POR Monitor

The POR monitor flag appears in both the MASTER_STATUS register and status bits when output. The POR flag indicates that a reset or a temporary supply brown out occurred.

MCLK Counter

The MCLK_COUNTER register (Register 0x31) updates every 64 MCLKs. The MCLK counter register verifies that the ADAQ7768-1 is still receiving a valid MCLK. Read the MCLK counter register according to the specific MCLK to SCLK ratio to ensure that a valid read occurs. The SCLK applied to read the MCLK_COUNTER register must not be less than 2.1 × MCLK or greater than 4.6 × MCLK. For example, if MCLK = 2 MHz, the SCLK applied cannot be in the 4.2 MHz to 9.2 MHz range. If the MCLK to SCLK ratio is not adhered to, the read may corrupt because the MCLK may update during the read of the register, causing an error.

Product Identification (ID) Number

The ADAQ7768-1 contains ID registers that allow software interrogation of the silicon. The class of the product (precision ADC), product ID, device revision, and grade of device can all be read from the registry over the SPI. The vendor ID for Analog Devices, Inc., is also included in the registry for readback. These registers, in addition to a scratch pad that allows free reads from and writes to a specific register address, are methods to verify the correct operation of the serial control interface.

Table 19. Product Identification Registers

Register Address (Hex)	Name	Bit Fields	
0x03	Chip type	Reserved	Class
0x04	Product ID [7:0]	PRODUCT_ID[7:0]	
0x05	Product ID [15:8]	PRODUCT_ID[15:8]	
0x06	Grade and revision	Grade	DEVICE_REVISION
0x0A	Scratch pad	Value	
0x0C	Vendor ID	VID[7:0]	
0x0D		VID[15:8]	

QUICK START-UP GUIDE

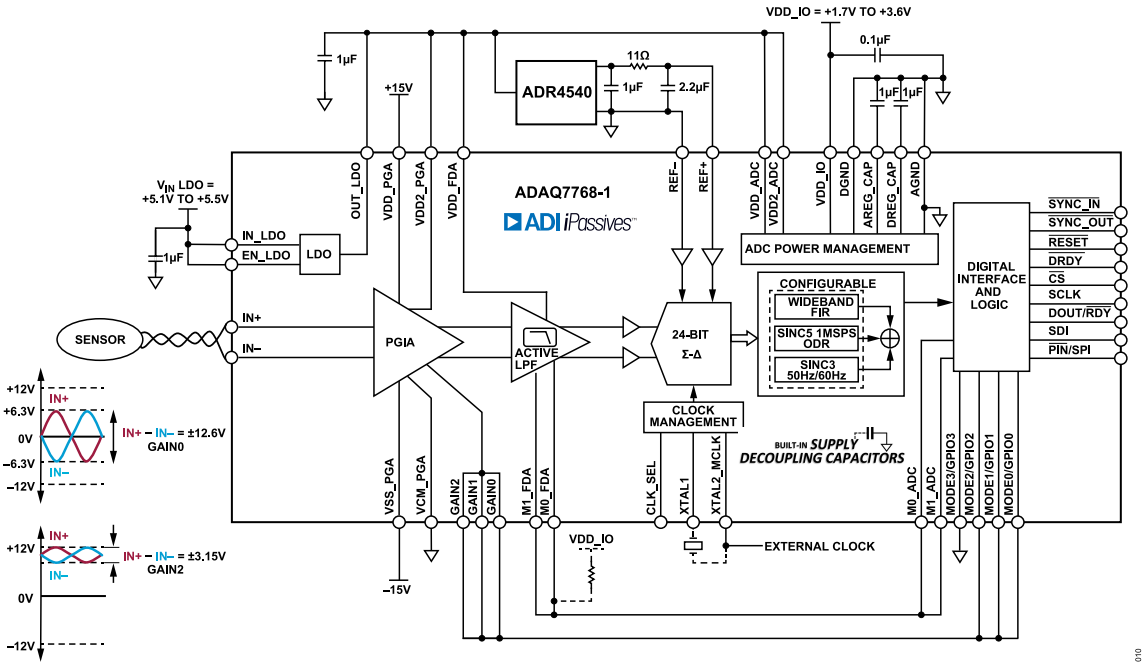

Figure 134. Typical Connection Diagram

POWER SUPPLY CONNECTION

The ADAQ7768-1 has several power supplies to power the analog front-end and ADC. To simplify the connection, the ADAQ7768-1 has an internal LDO that can be used to supply the voltage of the VDD_ADC, VDD2_PGA, and VDD_FDA. The LDO can also power the ADR4540 reference for the REF+ and REF- pins. The LDO input can handle inputs ranges of 5.1 V to 5.5 V. For proper operation, it is recommended to use a 1µF capacitor at the input and output of the LDO. If the LDO is not used during normal operation, it is recommended to keep all the LDO pins floating.

Depending on the input signal rail, the VDD_PGA can be set from 4.5 V to 18 V, while the VSS_PGA can be set from -4.5 V to -18 V. The VDD_IO powers the internal regulator needed by the digital logic of the ADC. The VDD_IO is referenced to DGND and can vary from 1.7 V to 3.6 V.

The ADAQ7768-1 has a built-in 0.1µF internal decoupling capacitor on each power supply, except for the VDD_IO. For detailed information regarding power supply connection and power supply decoupling, see the Power Supplies and Power Supply Decoupling sections.

DEVICE CONTROL MODE

The ADAQ7768-1 has two options to control device functionality. On power-up, the mode is determined by the state of the $\overline{\text{PIN}}$/ SPI pin. The two modes of configuration are:

- $\overline{\text{PIN}}$/SPI = VDD_IO = SPI control mode: over a 3- or 4-wire SPI interface (complete configurability), suggested control mode.
- $\overline{\text{PIN}}$/SPI = DGND = Pin control mode: pin-strapped digital logic inputs (a subset of complete configurability, daisy-chain is available only at this mode).

The first design decision is setting the ADAQ7768-1 in either the SPI or $\overline{\text{PIN}}$ mode of configuration.

On power-up, apply a soft or hard reset to the device when using either control mode. A $\overline{\text{SYNC\_IN}}$ pulse is also recommended after the reset or after any change to the device configuration. Choose between controlling and configuring over the SPI or through pin connections only.

The Device Configuration Method section provides a detailed discussion on the capability and limitations of the two control mode options.

SELECTING THE INPUT RANGE

The ADAQ7768-1 input is a low-noise, low-bias current, high-bandwidth programmable-gain instrumentation amplifier (PGIA) capable of signal attenuation and signal amplification. The PGIA has seven gain settings capable of varying the input range from ±0.197 V to ±12.603 V fully differential input signal.

The PGIA gain can be controlled with the GAIN 0, GAIN 1, and GAIN 2 pins. The gain pin can be set using an external pull-up or pull-down resistor connected between AGND and VDD_IO, as shown in Figure 135.

QUICK START-UP GUIDE

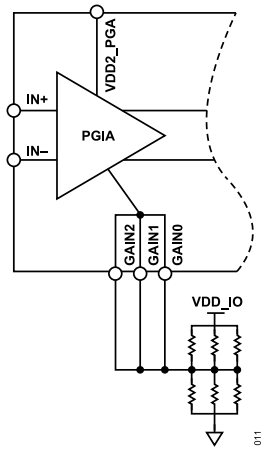

Figure 135. PGIA Gain Control Using External Resistors

Selecting the Input Range shows the truth table of the gain pin combinations and the resulting PGIA gain setting.

The PGIA gain pin can also be connected to the GPIO pins of the ADAQ7768-1, as shown in Figure 134, for the user to control the PGIA gain over the SPI. When the GPIO pins are used to control the PGIA gain, the user must set the GPIO ports as output, on GPIO Port Control Register (Register 0x1E). The GPIO Output Control Register (Register 0x1F) sets the desire output logic for GPIO pins.

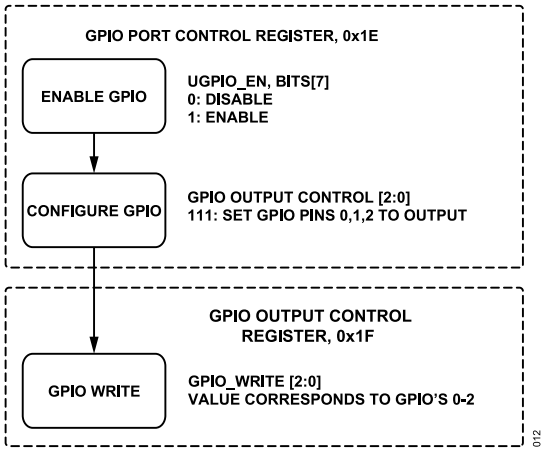

Figure 136. GPIO Gain Control Flowchart

Writing 111 to the GPIOx_OP_EN bits [2:0] of the GPIO Port Control Register (Register 0x1E) enables GPIO0, GPIO1, and GPIO2. Using the default output logic of the GPIO Output Control Register (Register 0x1F), which is 000, sets the ADAQ7768-1 to a system gain of 20.8 V/V capable of input voltage of ± 0.197 V.

SELECTING THE MCLK DIVIDER AND SOURCE

Selecting the MCLK Source

The ADAQ7768-1 has an internal oscillator used for initial power-up of the device. After the ADAQ7768-1 completes the start-up routine, a clock handover occurs to the external MCLK. The MCLK source can be programmed using the two control mode options, pin and SPI control modes.

In the $\overline{\text{PIN}}$ control mode, the CLK_SEL pin sets the external MCLK source. Three clock options are available in the $\overline{\text{PIN}}$ control mode: an internal oscillator, an external CMOS, or a crystal oscillator.

- CLK_SEL = 0 in the $\overline{\text{PIN}}$ control mode, the CMOS clock option is selected and must be applied to the MCLK pin. In this case, tie the XTAL1 pin to DGND.
- CLK_SEL = 1 in the $\overline{\text{PIN}}$ control mode, select the crystal option is selected and must be connected between the XTAL1 and XTAL2 pins.
- On the condition that no external clock is detected, the ADAQ7768-1 uses its internal clock as a default clock source.

In the SPI control mode, the following options are available for the MCLK input source, and can be set from the Power and Clock Control Register (Register 0x15) CLOCK_SEL bits [7:6]:

- CLOCK_SEL bits = 00 → CMOS input MCLK
- CLOCK_SEL bits = 01 → External crystal
- CLOCK_SEL bits = 10 → LVDS (exclusive to the SPI control mode)
- CLOCK_SEL bits = 11 → Internal clock

When switching from one clock source to another, apply soft reset to the device.

For optimum AC performance, it is not recommended to use in the internal clock as MCLK source.

MCLK Divider

The MCLK signal received by the ADAQ7768-1 defines the core ADC's sigma-delta modulator clock rate (f_{MOD}) and, in turn, the sampling frequency of the modulator of 2 × f_{MOD}. For optimum performance, it is recommended to use MCLK = 16.384 MHz and MCLK_DIV = 2. This sets the f_{MOD} = 8.192 MHz. Keeping the f_{MOD} frequency high maximizes the out-of-band tone rejection from the front-end anti-aliasing filter.

$$f_{MOD}(Hz) = \frac{MCLK}{MCLK\_DIV} \quad (10)$$

The default controller clock divider setting for ADAQ7768-1 is MCLK_DIV = 16. To configure the MCLK divider to MCLK = 2, write 11 to MCLK_DIV bits [5:4] of the Power and Clock Control Register (Register 0x15) after power up.

Table 17 shows how to configure MCLK when operating under the $\overline{\text{PIN}}$ control mode.

MCLK and SCLK Alignment

The ADAQ7768-1 interface is flexible to allow the multiple modes of operation and various data output formats to work across different digital signal processors (DSPs) and microcontroller units (MCUs).

QUICK START-UP GUIDE

To achieve maximum performance, it is recommended to have a synchronous SCLK and MCLK from the same clock source. It is also possible to set SCLK to be a divided down version of MCLK. The Recommended Interface section provides a detailed discussion about digital interface.

DIGITAL FILTER SETTING

The ADAQ7768-1 has three types of digital filters.

- Wideband Low Ripple FIR filter, −3 dB at 0.433 × ODR (6 rates)
- Sinc5 low latency filter, −3 dB at 0.204 × ODR (8 rates)
- Sinc3 low latency filter, –3 dB at 0.2617 × ODR, widely programmable data rate

The digital filter section provides details on the digital filter setting.

Decimation Rate and Output Data Rate

The ADAQ7768-1 has programmable decimation rates for the Sinc5, Sinc3, and Wideband Low Ripple FIR digital filters. The decimation rates allow to band limit the measurement, which reduces the speed and input bandwidth, but increases the resolution because there is further averaging in the digital filter. Filter selection and decimation rate setting when using the $\overline{PIN}$ control mode are listed in Table 17, while the SPI control mode requires a register write to the Digital Filter and Decimation Control Register (Register 0x19). Another register (SINC3 Decimation Rate (LSB) Register) is needed when setting the decimation rate for Sinc3 using SPI.

The ODR of the ADAQ7768-1 can be calculated using the formula:

$$ODR = \frac{f_{MOD}}{DEC\_RATE} \quad (11)$$

ADC POWER MODE

The ADC core power mode must match the MCLK_DIV setting, and for optimum performance it is recommended to use MCLK_DIV = 2. This sets the ADAQ7768-1 in the high-performance mode (fast mode). Be aware that the ADAQ7768-1 ADC power mode defaults to the eco power mode upon power up. To change the ADC power mode to high performance, write 11 to the ADC_MODE bits [1:0] of Power and Clock Control Register (Register 0x15).

BASIC REGISTER SETUP

Figure 137 shows the basic flow of register writes for ADAQ7768-1 upon power up.

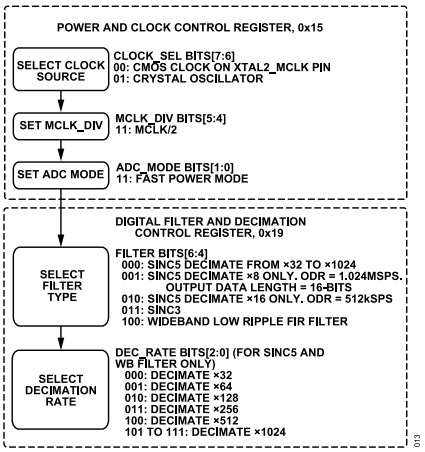

Figure 137. Basic Register Setup for ADAQ7768-1

The subsequent SPI writes needed upon power up to set the ADAQ7768-1 to the following conditions are:

- MCLK sourced from CMOS clock.
- The MCLK divider should be set to 2 (recommended).
- ADC power mode should be set to the high-performance mode, or fast mode (recommended).
- Wideband low ripple filter
- Decimation rate to 32

The equivalent SPI writes are:

- Data 0x33 to Power and Clock Control Register (Register 0x15)
- Data 0x40 to Digital Filter and Decimation Control Register (Register 0x19)

NOISE PERFORMANCE AND RESOLUTION

The noise performance of the signal chain is highly dependent on the application's input range and desired output data rate (ODR) of the ADAQ7768-1.

The ODR of the device is dependent on the MCLK and configured decimation rate. The ODR, for any digital filter, can be calculated by:

$$f_{MOD} = \frac{MCLK}{MCLK\_DIV} \quad (12)$$

$$ODR = \frac{f_{MOD}}{DEC\_RATE} \quad (13)$$

where:

f_{MOD} is the ADC modulator frequency.

DEC_RATE is the decimation rate.

MCLK is the controller clock frequency.

MCLK_DIV is the ratio between the MCLK applied at the input to the ADAQ7768-1 and the clock used by the ADC modulator.

Noise performance also depends on the type of digital filter used, each having different −3 dB bandwidths. The digital filters available on the ADAQ7768-1 are:

- Wideband low ripple FIR filter, −3 dB at 0.433 × ODR
- Sinc5 low latency filter, −3 dB at 0.204 × ODR
- Sinc3 low latency filter, –3 dB at 0.2617 × ODR

The DEC_RATE, MCLK, MCLK_DIV, and type of digital filter can be varied by the user, and the manner of configuration varies between the $\overline{PIN}$ and SPI modes (see Device Configuration Method).

Table 20, Table 21, and Table 22 show the noise performance for the wideband low ripple, sinc5, and sinc3 digital filters of the ADAQ7768-1 for various ODR values. The specified noise values and dynamic ranges are typical for the bipolar input range with an external 4.096 V reference (V_{REF}). The RMS noise is measured with shorted analog inputs to ground reference. The dynamic range (DR) is the ratio of the RMS value of the full-scale range (FSR) to the RMS noise measured when input pins are shorted together. The FSR is dependent on the active gain mode. In decibels, the DR is given by:

$$\text{Dynamic Range} = 20 \log\left(\frac{\text{FSR (in V p-p)}}{2\sqrt{2} \times \text{RMS Noise}}\right) \quad (14)$$

Table 20. Wideband Low Ripple FIR Filter Noise for Performance vs. ODR (V_{REF} = 4.096 V, f_{MOD} = MCLK/2)

MCLK (MHz)	Decimation Rate	ODR (kSPS)	−3 dB Bandwidth (kHz)	Gain Mode	Full-Scale Input Range (V)	Shorted Input Dynamic Range (dB)	Input Referred RMS Noise (µV)
16.384	32	256	110.8	GAIN 0	±12.603	106.7	41.2
16.384	32	256	110.8	GAIN 1	±6.302	106.4	21.4
16.384	32	256	110.8	GAIN 2	±3.151	105.7	11.6
16.384	32	256	110.8	GAIN 3	±1.575	104.8	6.4
16.384	32	256	110.8	GAIN 4	±0.788	102.7	4.1
16.384	32	256	110.8	GAIN 5	±0.394	98.9	3.1
16.384	32	256	110.8	GAIN 6	±0.197	93.8	2.8
16.384	64	128	55.4	GAIN 0	±12.603	109.5	29.8
16.384	64	128	55.4	GAIN 1	±6.302	109.2	15.4
16.384	64	128	55.4	GAIN 2	±3.151	108.6	8.31
16.384	64	128	55.4	GAIN 3	±1.575	107.7	4.57
16.384	64	128	55.4	GAIN 4	±0.788	105.7	2.88
16.384	64	128	55.4	GAIN 5	±0.394	102.0	2.22
16.384	64	128	55.4	GAIN 6	±0.197	97.0	1.98
16.384	128	64	27.7	GAIN 0	±12.603	112.4	21.4
16.384	128	64	27.7	GAIN 1	±6.302	112.1	11.0
16.384	128	64	27.7	GAIN 2	±3.151	111.4	5.97
16.384	128	64	27.7	GAIN 3	±1.575	110.7	3.26
16.384	128	64	27.7	GAIN 4	±0.788	108.6	2.06
16.384	128	64	27.7	GAIN 5	±0.394	104.9	1.59
16.384	128	64	27.7	GAIN 6	±0.197	99.9	1.41
16.384	256	32	13.9	GAIN 0	±12.603	115.0	15.9
16.384	256	32	13.9	GAIN 1	±6.302	114.7	8.20
16.384	256	32	13.9	GAIN 2	±3.151	114.3	4.31
16.384	256	32	13.9	GAIN 3	±1.575	113.4	2.39

NOISE PERFORMANCE AND RESOLUTION

Table 20. Wideband Low Ripple FIR Filter Noise for Performance vs. ODR (V_{REF} = 4.096 V, f_{MOD} = MCLK/2) (Continued)

MCLK (MHz)	Decimation Rate	ODR (kSPS)	−3 dB Bandwidth (kHz)	Gain Mode	Full-Scale Input Range (V)	Shorted Input Dynamic Range (dB)	Input Referred RMS Noise (µV)
16.384	256	32	13.9	GAIN 4	±0.788	111.3	1.51
16.384	256	32	13.9	GAIN 5	±0.394	107.7	1.15
16.384	256	32	13.9	GAIN 6	±0.197	102.7	1.01
16.384	512	16	6.9	GAIN 0	±12.603	117.7	11.6
16.384	512	16	6.9	GAIN 1	±6.302	117.5	5.96
16.384	512	16	6.9	GAIN 2	±3.151	116.8	3.24
16.384	512	16	6.9	GAIN 3	±1.575	115.9	1.78
16.384	512	16	6.9	GAIN 4	±0.788	114.1	1.10
16.384	512	16	6.9	GAIN 5	±0.394	110.4	0.84
16.384	512	16	6.9	GAIN 6	±0.197	105.4	0.75
16.384	1024	8	3.5	GAIN 0	±12.603	120.0	8.94
16.384	1024	8	3.5	GAIN 1	±6.302	119.6	4.69
16.384	1024	8	3.5	GAIN 2	±3.151	119.0	2.49
16.384	1024	8	3.5	GAIN 3	±1.575	118.3	1.35
16.384	1024	8	3.5	GAIN 4	±0.788	116.3	0.85
16.384	1024	8	3.5	GAIN 5	±0.394	112.8	0.64
16.384	1024	8	3.5	GAIN 6	±0.197	107.9	0.56
13.107	32	204.8	88.7	GAIN 0	±12.603	106.8	40.8
13.107	32	204.8	88.7	GAIN 1	±6.302	106.5	21.1
13.107	32	204.8	88.7	GAIN 2	±3.151	105.8	11.4
13.107	32	204.8	88.7	GAIN 3	±1.575	105.1	6.22
13.107	32	204.8	88.7	GAIN 4	±0.788	103.2	3.84
13.107	32	204.8	88.7	GAIN 5	±0.394	99.7	2.88
13.107	32	204.8	88.7	GAIN 6	±0.197	94.7	2.55
13.107	64	102.4	44.3	GAIN 0	±12.603	110.1	28.0
13.107	64	102.4	44.3	GAIN 1	±6.302	109.8	14.3
13.107	64	102.4	44.3	GAIN 2	±3.151	109.0	7.88
13.107	64	102.4	44.3	GAIN 3	±1.575	108.3	4.29
13.107	64	102.4	44.3	GAIN 4	±0.788	106.4	2.68
13.107	64	102.4	44.3	GAIN 5	±0.394	102.8	2.02
13.107	64	102.4	44.3	GAIN 6	±0.197	97.8	1.79
13.107	128	51.2	22.2	GAIN 0	±12.603	113.2	19.5
13.107	128	51.2	22.2	GAIN 1	±6.302	112.9	10.1
13.107	128	51.2	22.2	GAIN 2	±3.151	112.1	5.51
13.107	128	51.2	22.2	GAIN 3	±1.575	111.3	3.03
13.107	128	51.2	22.2	GAIN 4	±0.788	109.4	1.89
13.107	128	51.2	22.2	GAIN 5	±0.394	105.8	1.44
13.107	128	51.2	22.2	GAIN 6	±0.197	100.7	1.28
13.107	256	25.6	11.1	GAIN 0	±12.603	116.2	13.9
13.107	256	25.6	11.1	GAIN 1	±6.302	115.7	7.35
13.107	256	25.6	11.1	GAIN 2	±3.151	114.8	4.04
13.107	256	25.6	11.1	GAIN 3	±1.575	114.1	2.20
13.107	256	25.6	11.1	GAIN 4	±0.788	112.2	1.37
13.107	256	25.6	11.1	GAIN 5	±0.394	108.6	1.04
13.107	256	25.6	11.1	GAIN 6	±0.197	103.5	0.93

NOISE PERFORMANCE AND RESOLUTION

Table 21. Sinc5 Filter Noise for Performance vs. ODR (V_{REF} = 4.096 V, f_{MOD} = MCLK/2)

MCLK (MHz)	Decimation Rate	ODR (kSPS)	−3 dB Bandwidth (kHz)	Gain Mode	Input Range (V)	Shorted Input Dynamic Range (dB)	Input Referred RMS Noise (µV)
16.384	8	1024 (16-bit)	198.4	GAIN 0	±12.603	93.3	192.0
16.384	8	1024 (16-bit)	198.4	GAIN 1	±6.302	93.3	96.7
16.384	8	1024 (16-bit)	198.4	GAIN 2	±3.151	93.2	48.5
16.384	8	1024 (16-bit)	198.4	GAIN 3	±1.575	93.1	24.7
16.384	8	1024 (16-bit)	198.4	GAIN 4	±0.788	92.8	12.8
16.384	8	1024 (16-bit)	198.4	GAIN 5	±0.394	91.6	7.29
16.384	8	1024 (16-bit)	198.4	GAIN 6	±0.197	89.1	4.89
16.384	16	512	104.4	GAIN 0	±12.603	105.8	45.9
16.384	16	512	104.4	GAIN 1	±6.302	105.5	23.8
16.384	16	512	104.4	GAIN 2	±3.151	104.8	12.8
16.384	16	512	104.4	GAIN 3	±1.575	104.0	7.01
16.384	16	512	104.4	GAIN 4	±0.788	102.1	4.35
16.384	16	512	104.4	GAIN 5	±0.394	98.6	3.27
16.384	16	512	104.4	GAIN 6	±0.197	93.7	2.87
16.384	32	256	52.2	GAIN 0	±12.603	109.8	28.7
16.384	32	256	52.2	GAIN 1	±6.302	109.5	14.9
16.384	32	256	52.2	GAIN 2	±3.151	108.7	8.17
16.384	32	256	52.2	GAIN 3	±1.575	107.9	4.50
16.384	32	256	52.2	GAIN 4	±0.788	105.8	2.86
16.384	32	256	52.2	GAIN 5	±0.394	102.1	2.19
16.384	32	256	52.2	GAIN 6	±0.197	97.0	1.96
16.384	64	128	26.1	GAIN 0	±12.603	113.0	20.0
16.384	64	128	26.1	GAIN 1	±6.302	112.7	10.4
16.384	64	128	26.1	GAIN 2	±3.151	111.8	5.70
16.384	64	128	26.1	GAIN 3	±1.575	111.0	3.14
16.384	64	128	26.1	GAIN 4	±0.788	108.9	2.00
16.384	64	128	26.1	GAIN 5	±0.394	105.1	1.55
16.384	64	128	26.1	GAIN 6	±0.197	100.0	1.39
16.384	128	64	13.1	GAIN 0	±12.603	115.9	14.3
16.384	128	64	13.1	GAIN 1	±6.302	115.6	7.41
16.384	128	64	13.1	GAIN 2	±3.151	114.9	4.01
16.384	128	64	13.1	GAIN 3	±1.575	113.9	2.24
16.384	128	64	13.1	GAIN 4	±0.788	111.8	1.43
16.384	128	64	13.1	GAIN 5	±0.394	108.0	1.10
16.384	128	64	13.1	GAIN 6	±0.197	102.9	1.00
16.384	256	32	6.5	GAIN 0	±12.603	118.8	10.2
16.384	256	32	6.5	GAIN 1	±6.302	118.6	5.26
16.384	256	32	6.5	GAIN 2	±3.151	117.7	2.89
16.384	256	32	6.5	GAIN 3	±1.575	116.8	1.61
16.384	256	32	6.5	GAIN 4	±0.788	114.6	1.04
16.384	256	32	6.5	GAIN 5	±0.394	110.8	0.80
16.384	256	32	6.5	GAIN 6	±0.197	105.6	0.73
13.107	32	204.8	41.8	GAIN 0	±12.603	110.1	27.8
13.107	32	204.8	41.8	GAIN 1	±6.302	109.8	14.4
13.107	32	204.8	41.8	GAIN 2	±3.151	109.1	7.80
13.107	32	204.8	41.8	GAIN 3	±1.575	108.4	4.23

NOISE PERFORMANCE AND RESOLUTION

Table 21. Sinc5 Filter Noise for Performance vs. ODR (V_{REF} = 4.096 V, f_{MOD} = MCLK/2) (Continued)

MCLK (MHz)	Decimation Rate	ODR (kSPS)	−3 dB Bandwidth (kHz)	Gain Mode	Input Range (V)	Shorted Input Dynamic Range (dB)	Input Referred RMS Noise (µV)
13.107	32	204.8	41.8	GAIN 4	±0.788	106.5	2.63
13.107	32	204.8	41.8	GAIN 5	±0.394	102.9	1.99
13.107	32	204.8	41.8	GAIN 6	±0.197	97.9	1.77
13.107	64	102.4	20.9	GAIN 0	±12.603	113.0	19.9
13.107	64	102.4	20.9	GAIN 1	±6.302	112.9	10.1
13.107	64	102.4	20.9	GAIN 2	±3.151	112.1	5.53
13.107	64	102.4	20.9	GAIN 3	±1.575	111.4	2.99
13.107	64	102.4	20.9	GAIN 4	±0.788	109.5	1.87
13.107	64	102.4	20.9	GAIN 5	±0.394	105.9	1.42
13.107	64	102.4	20.9	GAIN 6	±0.197	100.9	1.26
13.107	128	51.2	10.4	GAIN 0	±12.603	116.0	14.2
13.107	128	51.2	10.4	GAIN 1	±6.302	115.7	7.30
13.107	128	51.2	10.4	GAIN 2	±3.151	115.1	3.94
13.107	128	51.2	10.4	GAIN 3	±1.575	114.2	2.17
13.107	128	51.2	10.4	GAIN 4	±0.788	112.3	1.34
13.107	128	51.2	10.4	GAIN 5	±0.394	108.7	1.02
13.107	128	51.2	10.4	GAIN 6	±0.197	103.8	0.90
13.107	256	25.6	5.2	GAIN 0	±12.603	118.7	10.3
13.107	256	25.6	5.2	GAIN 1	±6.302	118.5	5.33
13.107	256	25.6	5.2	GAIN 2	±3.151	117.7	2.89
13.107	256	25.6	5.2	GAIN 3	±1.575	117.0	1.57
13.107	256	25.6	5.2	GAIN 4	±0.788	115.0	0.99
13.107	256	25.6	5.2	GAIN 5	±0.394	111.4	0.75
13.107	256	25.6	5.2	GAIN 6	±0.197	106.4	0.67

Table 22. Sinc3 Filter Noise for Performance vs. ODR (V_{REF} = 4.096 V, f_{MOD} = MCLK/2)

MCLK (MHz)	Decimation Rate	ODR (kSPS)	−3 dB Bandwidth (kHz)	Gain Mode	Input Range (V)	Shorted Input Dynamic Range (dB)	Input Referred RMS Noise (µV)
16.384	32	256	67	GAIN 0	±12.603	102.9	63.7
16.384	32	256	67	GAIN 1	±6.302	102.8	32.3
16.384	32	256	67	GAIN 2	±3.151	102.6	16.6
16.384	32	256	67	GAIN 3	±1.575	102.3	8.51
16.384	32	256	67	GAIN 4	±0.788	101.4	4.73
16.384	32	256	67	GAIN 5	±0.394	99.3	3.02
16.384	32	256	67	GAIN 6	±0.197	95.2	2.43
16.384	128	64	16.7	GAIN 0	±12.603	116.5	13.4
16.384	128	64	16.7	GAIN 1	±6.302	116.3	6.86
16.384	128	64	16.7	GAIN 2	±3.151	115.6	3.69
16.384	128	64	16.7	GAIN 3	±1.575	114.8	2.04
16.384	128	64	16.7	GAIN 4	±0.788	112.1	1.38
16.384	128	64	16.7	GAIN 5	±0.394	107.9	1.12
16.384	128	64	16.7	GAIN 6	±0.197	102.6	1.03
16.384	512	16	4.2	GAIN 0	±12.603	120.5	8.38
16.384	512	16	4.2	GAIN 1	±6.302	120.2	4.36
16.384	512	16	4.2	GAIN 2	±3.151	119.5	2.35
16.384	512	16	4.2	GAIN 3	±1.575	118.5	1.32

NOISE PERFORMANCE AND RESOLUTION

Table 22. Sinc3 Filter Noise for Performance vs. ODR (V_{REF} = 4.096 V, f_{MOD} = MCLK/2) (Continued)

MCLK (MHz)	Decimation Rate	ODR (kSPS)	−3 dB Bandwidth (kHz)	Gain Mode	Input Range (V)	Shorted Input Dynamic Range (dB)	Input Referred RMS Noise (µV)
16.384	512	16	4.2	GAIN 4	±0.788	116.3	0.85
16.384	512	16	4.2	GAIN 5	±0.394	112.1	0.69
16.384	512	16	4.2	GAIN 6	±0.197	107.0	0.62
16.384	2048	4	1.05	GAIN 0	±12.603	126.1	4.42
16.384	2048	4	1.05	GAIN 1	±6.302	125.4	2.38
16.384	2048	4	1.05	GAIN 2	±3.151	123.8	1.43
16.384	2048	4	1.05	GAIN 3	±1.575	121.3	0.96
16.384	2048	4	1.05	GAIN 4	±0.788	117.3	0.76
16.384	2048	4	1.05	GAIN 5	±0.394	111.6	0.74
16.384	2048	4	1.05	GAIN 6	±0.197	105.8	0.71
16.384	8192	1	0.26	GAIN 0	±12.603	128.4	3.40
16.384	8192	1	0.26	GAIN 1	±6.302	128.0	1.78
16.384	8192	1	0.26	GAIN 2	±3.151	127.6	0.93
16.384	8192	1	0.26	GAIN 3	±1.575	126.4	0.53
16.384	8192	1	0.26	GAIN 4	±0.788	124.0	0.35
16.384	8192	1	0.26	GAIN 5	±0.394	119.4	0.30
16.384	8192	1	0.26	GAIN 6	±0.197	114.3	0.27
16.384	163840	0.05	0.013	GAIN 0	±12.603	135.5	1.50
16.384	163840	0.05	0.013	GAIN 1	±6.302	134.0	0.89
16.384	163840	0.05	0.013	GAIN 2	±3.151	132.3	0.54
16.384	163840	0.05	0.013	GAIN 3	±1.575	130.6	0.33
16.384	163840	0.05	0.013	GAIN 4	±0.788	127.0	0.25
16.384	163840	0.05	0.013	GAIN 5	±0.394	122.0	0.22
16.384	163840	0.05	0.013	GAIN 6	±0.197	116.4	0.21

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The ADAQ7768-1 has a 4-wire SPI. The interface operates in SPI Mode 3. In SPI Mode 3, SCLK idles high, the first data is clocked out on the first falling or drive edge of SCLK, and data is clocked in on the rising or sample edge. Figure 139 shows the SPI Mode 3 operation, where the falling edge of SCLK drives out the data and the rising edge of SCLK is the instance when the data is sampled.

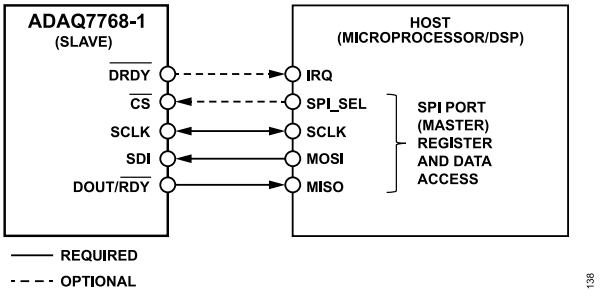

Figure 138. Basic Serial Port Connection Diagram

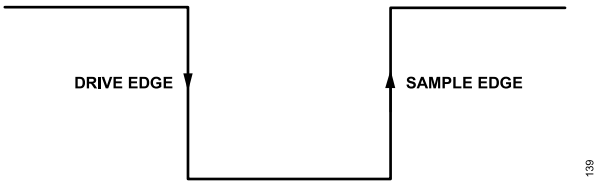

Figure 139. SPI Mode 3

SPI READING AND WRITING

To use the SPI control mode, set the PIN/SPI pin high. The SPI control operates as a 4-wire interface allowing read and write access. In systems where CS can be tied low, such as those requiring isolation, the ADAQ7768-1 can operate in a 3-wire configuration. Figure 138 shows a typical connection between the ADAQ7768-1 and digital host. The corresponding 3-wire interface involves tying the CS pin low and using SCLK, SDI, and DOUT/RDY.

Figure 140 shows the format of the SPI read or write. The MSB is the first bit in both the read and write operations. An active low-frame start signal (FS) begins the transaction, followed by the R/W bit that determines if the transaction being carried out is to a read (1) or a write (0). The next six bits are used for the address, and the eight bits of data to be written follow. All registers in the ADAQ7768-1 are 8 bits in width, except for the ADC_DATA register (Register 0x2C), which is 24 bits in width. In the case where CS is tied low, the last SCLK rising edge completes the SPI transaction and resets the interface. When reading back data with CS held low, it is recommended that SDI is idle high to prevent an accidental reset of the device where SCLK is free running (see the Reset section).

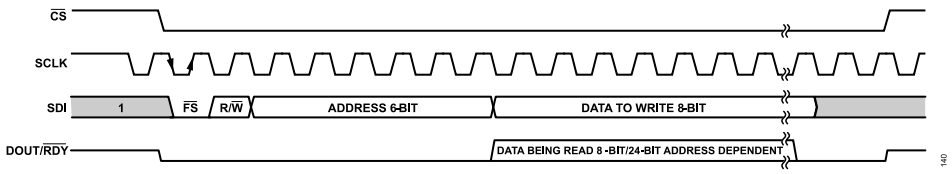

Figure 140. SPI Basic Read/Write Frame

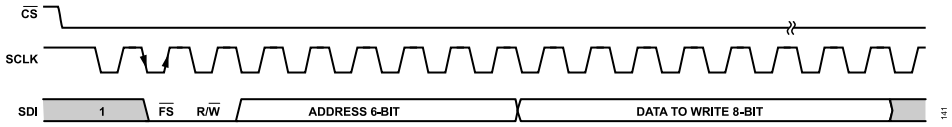

Figure 141. 3-Wire SPI Write Frame (CS = 0)

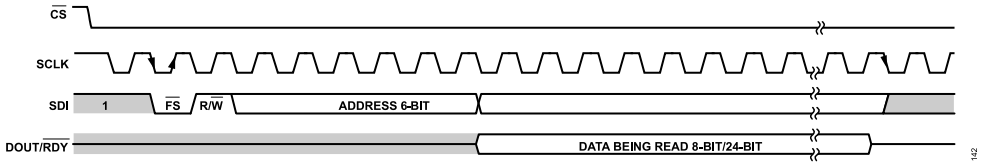

Figure 142. 3-Wire SPI Read Frame (CS = 0)

DIGITAL INTERFACE

SPI CONTROL ERROR HANDLING

The ADAQ7768-1 SPI control detects if an illegal command is received. An illegal command is a write to a read-only register, a write to a register address that does not exist, or a read from a register address that does not exist. If any of these illegal commands are received by the ADAQ7768-1,, error bits are set in the SPI_DIAG_STATUS register (Register 0x2E).

Five sources of SPI error can be detected. Tthese detectable error sources must be enabled in the SPI_DIAG_ENABLE register (Register 0x28). Only the EN_ERR_SPI_IGNORE (Bit 4) error is enabled on start-up.

The five detectable sources of SPI error are as follows:

- SPI CRC error. When the received CRC/XOR does not match the calculated CRC/XOR.
- SPI read error. When an incorrect read address is detected (for example, during attempts to access a register that does not exist).
- SPI write error. When a write to an incorrect address is detected (for example, during attempts to write to a register that does not exist).
- SPI clock count error. When the SPI transaction is controlled by $\overline{CS}$, this error flags when the SPI clock count during the frame is not equal to 8, 16, 24, 32, or 40. This error can be detected in both the continuous read mode and normal SPI mode.
- SPI ignore error. This error flags when an SPI transaction is attempted before initial power-up completes.

All SPI errors are sticky, meaning they can only be cleared if the user writes a 1 to the corresponding error location.

CYCLIC REDUNDANCY CHECK (CRC) ON SERIAL INTERFACE

The ADAQ7768-1 can deliver up to 40 bits with each conversion result, consisting of 24 bits of data and eight status bits, with the option to add eight further CRC/XOR check bits in the SPI mode only.

The status bits default per the description in the Status Header section. The CRC functionality is available only when operating in the SPI control mode. When the CRC functionality is in use, the CRC message is calculated internally by the ADAQ7768-1.. The CRC is then appended to the conversion data and optional status bits.

The ADAQ7768-1 uses a CRC polynomial to calculate the CRC message. The 8-bit CRC polynomial used is $x^8 + x^2 + x + 1$.

To generate the checksum, shift the data by eight bits to create a number ending in eight Logic 0s.

The polynomial is aligned such that the MSB is adjacent to the leftmost Logic 1 of the "command bits and register data". For example, when reading the ADC_DATA register containing 0xABCDEF:

Initial Value = Frame Start bit + R/W bit + ADDR[5:0] + ADC_DATA[23:0]

Initial Value = 0x6CABCDEF

Apply an exclusive OR (XOR) function to the data to produce a new, shorter number. The polynomial is again aligned such that the MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process repeats until the original data is reduced to a value less than the polynomial, which is the 8-bit checksum. In the example above, the CRC checksum = 0x9E.

If enabled, the SPI writes always use CRC, regardless of whether the XOR option is selected in the INTERFACE_FORMAT register (Register 0x14). The initial CRC checksum for SPI transactions is 0x00, unless reading back data in the continuous read mode, in which case the initial CRC is 0x03.

If using the XOR option in the continuous read mode, the initial value is set to 0x6C. The XOR option is only available for SPI reads.

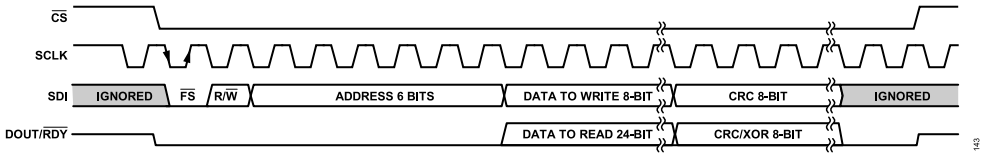

Figure 143. Data Output Format When Using CRC

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Example of a Polynomial CRC Calculation (24-Bit Word: 0x654321 (Eight Command Bits and 16-Bit Data))

An example to generate the 8-bit checksum using the polynomial-based checksum is as follows:

```
011001010100001100100001          = Initial Value
01100101010000110010000100000000  left shifted eight bits
 100000111                        = x^8 + x^2 + x + 1 polynomial value
  10010010000011001000010000000   XOR result
  100000111                       polynomial value
     10001100011001000010000000   XOR result
     100000111                    polynomial value
         11111110010000100000000  XOR result
         100000111                polynomial value
          11111011100001000000000 XOR result
          100000111               polynomial value
           11110000000100000000   XOR result
           100000111              polynomial value
            11100111000100000000  XOR result
            100000111             polynomial value
             11001001001000000000 XOR result
             100000111            polynomial value
              10010101010000000   XOR result
              100000111           polynomial value
                 101101100000000  XOR result
                 100000111        polynomial value
                   1101011000000  XOR result
                   100000111      polynomial value
                    101010110000  XOR result
                    100000111     polynomial value
                      1010001000  XOR result
                      100000111   polynomial value
                        10000110  XOR result; checksum = 0x86
```

Example of an XOR Calculation (24-Bit Word: 0x654321 (Eight Command Bits and 16-Bit Data))

Using the previous example, divide into three bytes (0x65, 0x43, and 0x21) as follows:

```
01100101 0x65
01000011 0x43
00100110 XOR result
00100001 0x21
00000111 XOR result; checksum = 0x07
```

CONVERSION READ MODES

The digital interface of the ADAQ7768-1 is a 4-wire SPI implementation operating in SPI Mode 3. An 8-bit write instruction is needed to access the memory map address space. All registers are eight bits wide, except the ADC data register. The ADAQ7768-1 operates in a continuously converting mode by default. The user must decide whether to read the data. Two read modes are available to access the ADC conversion results: single-conversion read mode and continuous read mode.

The single-read mode is a basic SPI read cycle where the user must write an 8-bit instruction to read the ADC data register. The status register must be read separately, if needed.

Write a 1 to the LSB of the INTERFACE_FORMAT register to enter the continuous read mode. Subsequent data reads do not require an initial 8-bit write to query the ADC_DATA register. Simply provide the required number of SCLKs for continuous readback of the data. Figure 144 shows an SPI read in the continuous read mode.

The key considerations for users on the interface are as follows:

DIGITAL INTERFACE

- Conversion data is available for readback after the rising edge of $\overline{DRDY}$. In the continuous read mode, the $\overline{RDY}$ function can be enabled, and the $\overline{DRDY}$ function can be ignored. Data is available for readback on the falling edge of $\overline{RDY}$.
- The ADC conversion data register is updated internally 1 MCLK period before the rising $\overline{DRDY}$ edge.
- MCLK has a maximum frequency of 16.384 MHz.
- SCLK has a maximum frequency of 20 MHz.
- The $\overline{DRDY}$ high time is 1 × t_{MCLK}.
- In the fast-power mode, decimate by 32. The $\overline{DRDY}$ period is ~4 µs, and the fastest conversion can have a $\overline{DRDY}$ period of 1 µs.
- The $\overline{CS}$ rising edge resets the serial data interface. If $\overline{CS}$ is tied low, the final rising SCLK edge of the SPI transaction resets the serial interface. The point at which the interface is reset corresponds to 16 × SCLKs for a normal read operation and up to 40 SCLKs when reading back ADC conversion data, plus the status and CRC headers.

Single-Conversion Read Mode

When using the single-conversion read mode, the ADC_DATA register can be accessed in the same way as a normal SPI read transaction. The ADC_DATA register (Register 0x2C) is 24 bits wide. Therefore, 32 SCLKs are required to read a conversion result.

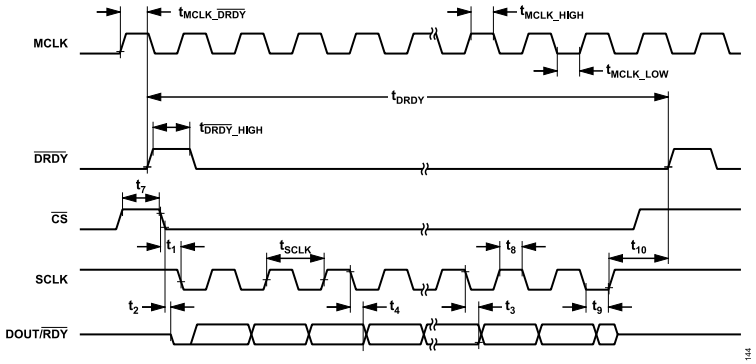

Figure 144. Serial Interface Timing Diagram, Example Reflects Reading an ADC Conversion in the Continuous Read Mode

Continuous Read Mode

To eliminate the overhead of needing to write a command to read the ADC data register each time, place the ADC in the continuous read mode so that the ADC register can be read directly after the data ready signal is pulsed. In the continuous read mode, data is output on the falling edge of the first SCLK received. Therefore, only 24 SCLKs are required to read a conversion. In this continuous read mode, it is also possible to append one or both of the status or CRC headers (eight bits each) to the conversion result. If both the status and CRC headers are enabled, the data format is ADC data + status bits + CRC.

When the $\overline{RDY}$ function is not used, the ADC conversion result can be read multiple times in the $\overline{DRDY}$ period, as shown in Figure 145. When the $\overline{RDY}$ function is enabled, the DOUT/$\overline{RDY}$ pin goes high after reading the ADAQ7768-1 conversion result and, therefore, the data cannot be read more than once (see Figure 146).

Continuous readback is the readback mode used in the $\overline{PIN}$ control mode. However, in this mode, the data output format is fixed. There is no option for $\overline{RDY}$ on the DOUT pin. See the Pin Control Mode Overview section for more details.

When using the continuous read mode with the LV_BOOST bit enabled (Bit 7 in the INTERFACE_FORMAT register, Address 0x14), it is necessary to re-enable LV_BOOST each time the continuous read mode is exited.

Exiting the Continuous Read Mode

To exit the continuous read mode, write a key of 0x6C on the SDI, which allows access to the register map one more time and allows further configuration of the device. To comply with a normal SPI write, use the $\overline{CS}$ signal to reset the SPI after this key is entered (see Figure 147). If $\overline{CS}$ cannot be controlled and is permanently held low, 16 SCLKs are needed to complete the transaction so that the SPI remains synchronized. For example, when $\overline{CS}$ is permanently tied low, write 0x006C to exit the continuous read mode when using the 3-wire version of the interface (see Figure 148). The exit command must be written between $\overline{DRDY}$ pulses to ensure that the device exits correctly.

A software reset can also be written in this mode like the exit command, but by writing 0xAD instead of 0x6C.

DIGITAL INTERFACE

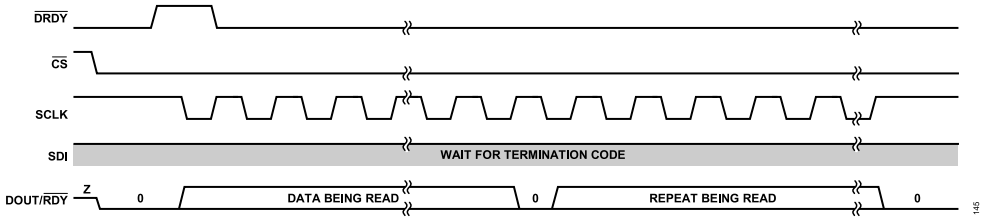

Figure 145. Continuous ADC Read Data Format with $\overline{RDY}$ Function Disabled

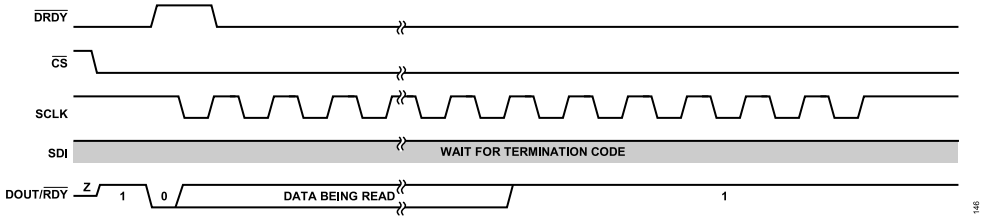

Figure 146. Continuous ADC Read Data Format with $\overline{RDY}$ Function Enabled on the DOUT/$\overline{RDY}$ Pin

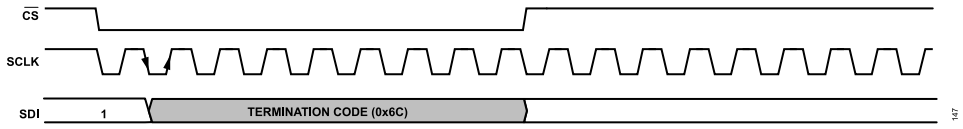

Figure 147. Exiting the Continuous Read Mode

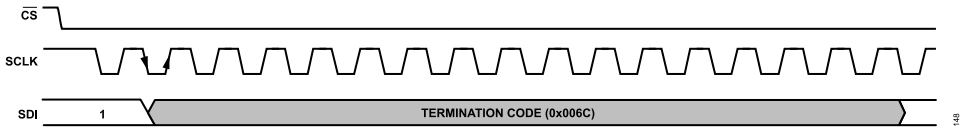

Figure 148. Exiting the Continuous Read Mode (CS = 0)

DATA CONVERSION MODES

The two data conversion modes available in the SPI control mode are:

- Continuous conversion
- One-shot conversion

The default conversion mode is continuous conversion. A $\overline{\text{SYNC\_IN}}$ pulse must be provided to the ADAQ7768-1 after any change to the configuration of the device, including changing filter settings and data conversion modes.

CONTINUOUS CONVERSION MODE

In the continuous conversion mode, the ADC continuously converts and a new ADC result is ready at an interval determined by the ODR, which is the default conversion operation in the SPI control mode. This is the only data conversion mode in which the wideband low ripple FIR filter is available. Two methods of data readback are available in the SPI control mode and are described in the Conversion Read Modes section.

ONE-SHOT CONVERSION MODE

Figure 149 shows the device operating in the one-shot conversion mode. In this mode, conversions occur on request by the controller device, for example, the digital signal processing (DSP) or field-programmable gate array (FPGA). The $\overline{\text{SYNC\_IN}}$ pin receives the command initiating the data output.

In the one-shot conversion mode, the ADC runs continuously. However, the $\overline{\text{SYNC\_IN}}$ pin rising controls the point in time from which data is output.

To receive data, the controller device must pulse the $\overline{\text{SYNC\_IN}}$ pin, which resets the filter and forces $\overline{\text{DRDY}}$ low. $\overline{\text{DRDY}}$ subsequently goes high to indicate to the controller device that the device has valid settled data available.

When the controller asserts $\overline{\text{SYNC\_IN}}$ and the ADAQ7768-1 receives the rising edge of this signal, the digital filter is reset, the full settling time of the filter elapses before the data is settled, and the output is available. The duration of the settling time depends on the filter path and decimation rate. The one-shot conversion mode is only available for use with the sinc5 or sinc3 filters because these filters feature a minimal settling time. The one-shot conversion mode is not available as an option with the wideband low ripple FIR filter .

When settled data is available, the $\overline{\text{DRDY}}$ signal pulses. Figure 149 shows the time from the $\overline{\text{SYNC\_IN}}$ signal until the ADC path settles data (t_{SETTLE}). After the settled data is available, $\overline{\text{DRDY}}$ is asserted high, and the user can read the conversion result. The device then waits for another $\overline{\text{SYNC\_IN}}$ signal before outputting more data.

The settling time is calculated relative to the settling time of the filter used, with some added latency for starting the one-shot conversion. This settling time limits the overall throughput achievable in the one-shot conversion mode.

Because the ADC is sampling continuously, the one-shot conversion mode affects the sampling theory of the ADAQ7768-1. Periodically sending a $\overline{\text{SYNC\_IN}}$ pulse to the device is a form of subsampling of the ADC output. The bandwidth around this subsampling rate can now alias down to the baseband. Consider keeping the $\overline{\text{SYNC\_IN}}$ pulse synchronous with the controller clock (MCLK) to ensure coherent sampling and to reduce the effects of jitter on the frequency response, which otherwise heavily distort the output.

Perform any SPI configuration of the ADAQ7768-1 required in the continuous conversion mode before switching back to the one-shot conversion mode.

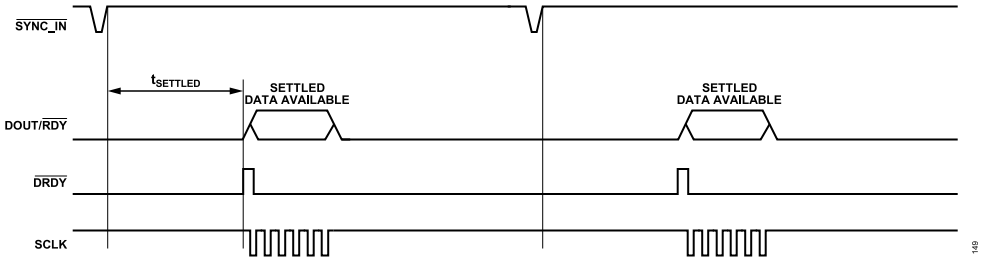

Figure 149. One-Shot Conversion Mode, $\overline{\text{SYNC\_IN}}$ Pin Driven with an External Source

DATA CONVERSION MODES

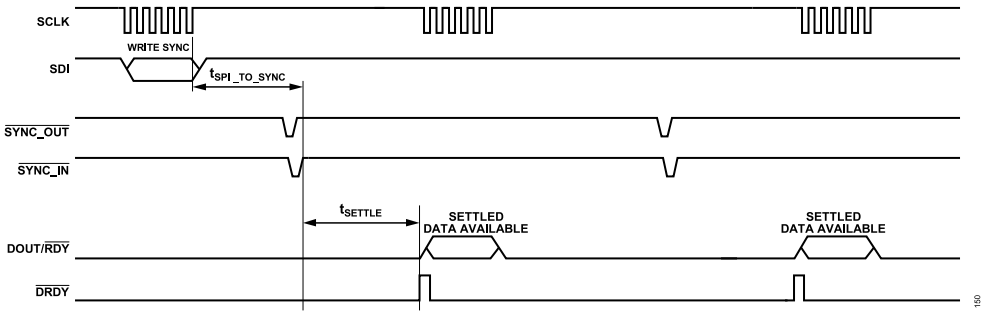

Figure 150. One-Shot Conversion Mode, SYNC_IN Pulse Initiated by a Register Write

SYNCHRONIZATION OF MULTIPLE ADAQ7768-1 DEVICES

Synchronization is important when using multiple ADAQ7768-1 devices in a system. The basic provision to synchronize multiple devices is that each device is clocked with the same base MCLK signal. A $\overline{\text{SYNC\_IN}}$ pulse must be provided to the ADAQ7768-1 both after power-up and after any change to the configuration of the device. This pulse flushes out the digital filters and ensures that the device is in a known configuration, as well as synchronizing multiple devices in a system.

The ADAQ7768-1 has three options to ease system synchronization. Choosing among the options depends on the system. However, the most basic consideration is whether the user can supply a synchronization pulse truly synchronous with the base MCLK signal.

If a signal synchronous to the base MCLK signal cannot be provided, use one of the following methods:

- Configure the GPIOx pin of one of the ADAQ7768-1 devices in the system as a $\overline{\text{START}}$ input. Apply a $\overline{\text{START}}$ pulse to the configured GPIOx pin. Route the $\overline{\text{SYNC\_OUT}}$ pin output to the $\overline{\text{SYNC\_IN}}$ input of that same device and all other devices to synchronize.
- The ADAQ7768-1 samples the asynchronous $\overline{\text{START}}$ pulse and generates a $\overline{\text{SYNC\_OUT}}$ pulse related to the base MCLK signal for local distribution.
- Use synchronization over SPI (only available in the SPI control mode). Write a synchronization command to one predetermined ADC device. Connect the $\overline{\text{SYNC\_OUT}}$ pin of this device to its own $\overline{\text{SYNC\_IN}}$ pin and to the $\overline{\text{SYNC\_IN}}$ pin of any other device locally. Similar to the $\overline{\text{START}}$ pin method, the SPI synchronization is received by one device and, subsequently, the $\overline{\text{SYNC\_OUT}}$ signal is routed to local devices to allow synchronization.

If a $\overline{\text{SYNC\_IN}}$ signal synchronous to the base MCLK can be provided, apply the $\overline{\text{SYNC\_IN}}$ synchronous signal to the $\overline{\text{SYNC\_IN}}$ pin from a star point and connect directly to the pin of each ADAQ7768-1 device. The $\overline{\text{SYNC\_IN}}$ signal is sampled on the rising MCLK edge and, therefore, setup and hold times are associated with the $\overline{\text{SYNC\_IN}}$ input relative to the ADAQ7768-1 MCLK rising edge (see Figure 7).

In this case, $\overline{\text{SYNC\_OUT}}$ is redundant and can remain open-circuit or tied to VDD_IO. Use GPIOx for a different purpose because it is not required for the $\overline{\text{START}}$ function. Figure 151 shows synchronization in channel-to-channel isolated systems.

Perform synchronization functions directly after the $\overline{\text{DRDY}}$ pulse. If the ADAQ7768-1 $\overline{\text{SYNC\_IN}}$ pulse occurs too close to the upcoming $\overline{\text{DRDY}}$ pulse edge, the upcoming $\overline{\text{DRDY}}$ pulse may still be output because the $\overline{\text{SYNC\_IN}}$ pulse has not yet propagated through the device.

When using the $\overline{\text{SYNC\_OUT}}$ function with a VDD_IO voltage of 1.8 V, it is recommended to set the SYNC_OUT_POS_EDGE bit (Register 0x1D, Bit 6) to 1.

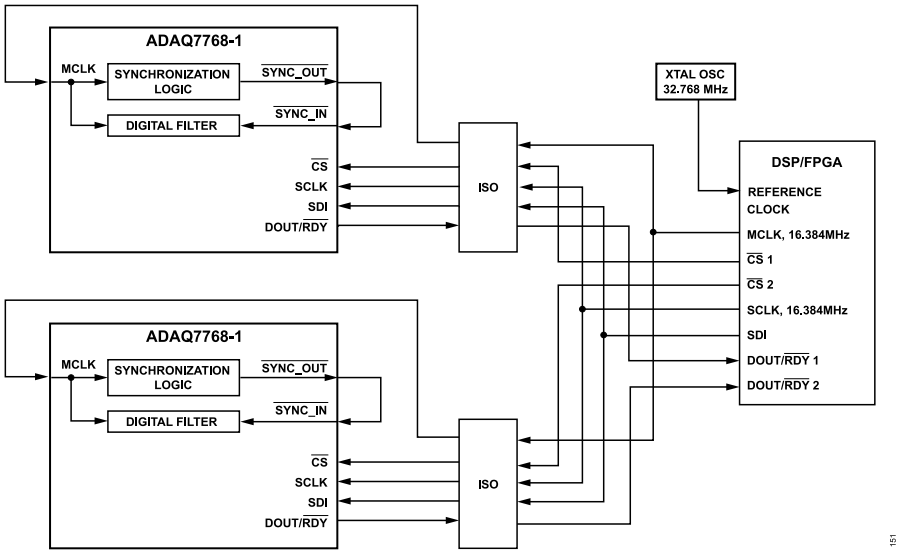

Figure 151. Synchronization in Channel-to-Channel Isolated Systems

ADDITIONAL FUNCTIONALITY OF THE ADAQ7768-1

RESET

After powering up the device, it is recommended to perform a full reset. There are multiple options available on the ADAQ7768-1 to perform a reset, including:

- Using the dedicated $\overline{\text{RESET}}$ pin. See the Pin Configuration and Function Descriptions section.
- When in the continuous read mode, the ADAQ7768-1 monitors for the exit command or a reset command of 0xAD. See the Exiting Continuous Read Mode section for more details.
- A software reset can be performed by two consecutive writes to the SYNC_RESET register (Register 0x1D).
- When $\overline{\text{CS}}$ is held low, it is possible to provide a reset by clocking in a 1 followed by 63 zeros on SDI, which is the SPI resume command reset function used to exit the power-down mode.

The time taken from $\overline{\text{RESET}}$ to an SPI write must be at least 200 µs.

STATUS HEADER

In the SPI control mode, the status header can be output after the conversion result when operating the ADAQ7768-1 in the continuous read back mode. The status header mirrors the MASTER_STATUS register (Register 0x2D).

In the $\overline{\text{PIN}}$ control mode, the status header is output by default after the conversion result. The status header contains the following bits and functions:

- The MASTER_ERROR bit is an OR of all other errors present and can be monitored to provide a quick indication of a problem having occurred.
- The ADC_ERROR bit sets to 1 if any error is present in the ADC_DIAG_STATUS register (Register 0x2F). It is an OR of the error bits in the ADC_DIAG_STATUS register.
- The DIG_ERROR bit sets to 1 if any error is present in the DIG_DIAG_STATUS register (Register 0x30). It is an OR of the error bits in the DIG_DIAG_STATUS register.
- The ADC_ERR_EXT_CLK_QUAL bit sets if a valid clock is not detected (see the Clock Qualification section).
- The ADC_FILT_SATURATED bit sets to 1 if the digital filter is clipped on either positive or negative full-scale. The clipping can be caused by the analog input exceeding the analog input range, or by a large step input to the device that causes a large overshoot in the digital filter. In addition, the filter may saturate if the ADC gain registers are incorrectly set. The combination of a full-scale signal and a large gain saturates the digital filter.
- The ADC_FILT_NOT_SETTLED bit is set to 1 if the output of the digital filter is not settled. The digital filters are cleared following a $\overline{\text{RESET}}$ pulse, or after a $\overline{\text{SYNC\_IN}}$ command is received.
- Table 11, Table 12, and Table 15 list the time for $\overline{\text{SYNC\_IN}}$ to settled data for each filter type. When using the wideband low ripple FIR filter, the filter not settled bit takes longer to update and propagate through the device than to read the status header. The filter not settled bit appears set when in fact the data output is settled. The worst-case update delay is 128 MCLK cycles for the wideband low ripple, wideband filter, decimate by 1024 setting. In this case, if the readback is delayed by 128 MCLK cycles, the filter not settled bit has time to update, and the time to settled data is equal to the data shown in Table 11, Table 12, and Table 15.
- The SPI_ERROR bit sets to 1 if any error is present in the SPI_DIAG_STATUS register (Register 0x2E). The bit is an OR of the error bits in the SPI_DIAG_STATUS register.
- The POR_FLAG bit detects if a reset or a temporary supply brown out occurred. In the $\overline{\text{PIN}}$ control mode, instead of being the POR flag, this bit is always set to 1 and then detects if the interface is operating correctly.

DIAGNOSTICS

The ADAQ7768-1 has internal diagnostics to check both the functionality of the ADC and the environment in which the ADC is operating. The internal diagnostics are enabled in the conversion register (Register 0x18). To use the diagnostics, the device must be configured to the eco mode, MCLK_DIV = MCLK/16, and the linearity boost buffers must be enabled. The diagnostics available are as follows:

- The temperature sensor is an on-chip temperature sensor that determines the approximate temperature. Temperature changes measured give approximately a 0.6 mV/°C change in the DC-converted voltage. For example, at ambient temperature, the conversion result is approximately 180 mV. A 50°C increase in temperature reads back as approximately 210 mV, signaling, for example, a potential fault or the need to calibrate the system.
- The analog input short disconnects the core ADC's input pins from the external input and creates an internal short across the analog input pins that can detect a fault.
- The voltage converted is V_{REF+} for positive full scale, if selected.
- The voltage converted is V_{REF-} for negative full scale, if selected.

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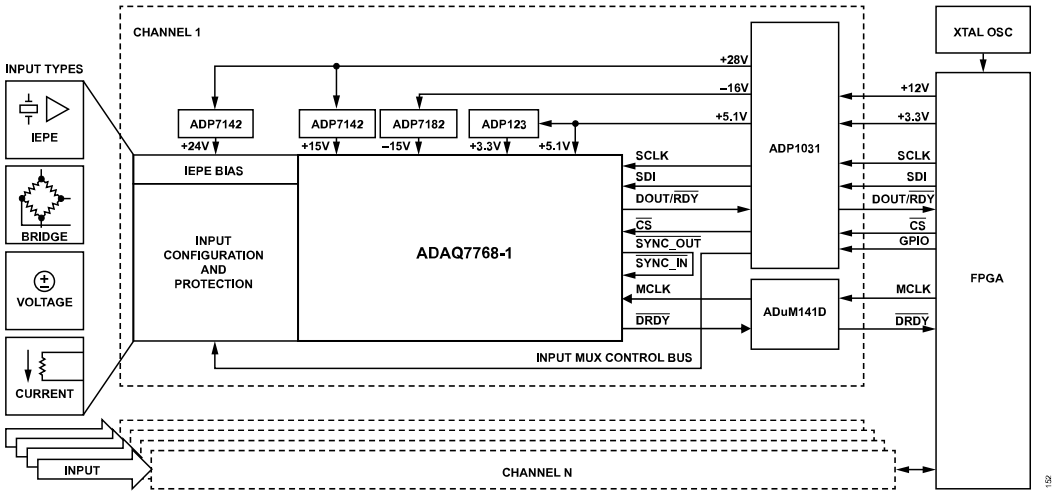

Figure 152. Typical Applications Diagram of a Per Channel Isolated DAQ System

QUICK START-UP

A Quick Start-Up Guide earlier in the document discusses the bare minimum requirements to power up and capture data from the device. This includes discussions on the power supply connection, clocking, and basic register writes. See the quick start-up guide first before reading the following sections, which discuss system-level applications and further performance optimization.

SENSOR INTERFACING AND GAIN CONTROL

The ADAQ7768-1 supports a wide variety of input types, including IEPE sensors, resistive bridges, voltage and current inputs, as illustrated in Figure 152. For integrated electronics piezo-electric (IEPE) sensors, it is necessary to provide the proper biasing for functional operation.

It is recommended to connect the inputs first to a switch or multiplexer with fault protection before going into the ADAQ7768-1. Fault flag pins can be used with an LED or through a digital line to the FPGA to signal input faults.

Switched or multiplexed inputs may require a separate MUX control bus to select the input, which entails additional digitally-isolated lines in an isolated system.

The AFE_GAIN can be easily set through an SPI write to GPIO Port Control Register and GPIO Output Control Register when the ADAQ7768-1 GPIOs are connected to its GAIN pins, decreasing the number of digital lines to the FPGA, which is especially beneficial in an isolated system.

ISOLATION AND POWER SOLUTION

Figure 152 shows a channel-to-channel isolated solution, using ADP1031 and ADUM142 to provide power and digital isolation.

The ADP1031 contains a flyback, a buck, and an inverting switching converter to provide the power rails required. These can be further regulated by LDOs (ADP7142, ADP7182, ADP123, and ADAQ7768-1's internal 5V LDO) to decrease the power supply noise. 0.1µF decoupling capacitors are also built-in on all supply pins except VDD_IO to decrease PCB footprint.

The ADuM142D is used to provide additional digitally-isolated lines to supplement to ADP1031.

POWER SUPPLY SEQUENCING

When powering up the device, no particular power supply sequencing is required, given that all AGND pins of the ADAQ7768-1 are connected to a single ground plane.

REFERENCE, REFERENCE BUFFER, AND LINEARITY BOOST BUFFER

While the ADC reference may range from VDD_ADC down to 1 V, the typical application and specification of the ADAQ7768-1 is set with an input reference at 4.096 V. This can be implemented by connecting the output of the integrated 5V LDO to an ADR4540 to output a voltage reference of 4.096 V.

It is recommended to use the ADC's integrated reference precharge buffers to lessen the burden on the external reference, as discussed in Reference Input and Buffering.

It is also recommended to enable the Linearity Boost Buffers, which ease the driving between the differential amplifier and core ADC input.

In the $\overline{\text{PIN}}$ mode, the reference precharge buffers and linearity boost buffers are enabled by default for enhanced performance, while the SPI mode requires a register write to the Analog Buffer Control Register to enable them.

RECOMMENDED INTERFACE

The ADAQ7768-1 interface is flexible to allow the many modes of operation and for data output formats to work across different DSPs and microcontroller units (MCUs). To achieve maximum performance, Figure 153 show the recommended interface configuration

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for reading conversion results. This recommended implementation uses a synchronous SCLK to MCLK relationship.

Configure the interface as follows to achieve the recommended operation:

1. Tie the $\overline{CS}$ signal low during the conversion readback.
2. Enter the continuous readback mode to avoid the need to provide the address bits for the ADC_DATA register. The continuous readback mode is the default readback mode in the $\overline{PIN}$ mode.
3. 32 bits of data are clocked out, consisting of the 24-bit conversion result plus eight bits that can be selected as either the status or CRC bits. In the $\overline{PIN}$ mode, this is always the conversion result plus the eight status bits.
4. Provide an SCLK that is phase-coherent to MCLK. SCLK can be identical to MCLK (SCLK = MCLK), or a divided down version of MCLK (SCLK = MCLK/N). For example, SCLK = MCLK/2 in a case where decimate by 32 is selected.
5. Clocking 32 bits ensures that the data readback operation fills the entire $\overline{DRDY}$ period when SCLK = MCLK/2. SCLK runs continuously. The readback spans the full $\overline{DRDY}$ period, thus spreading the noise coupling due to the current on VDD_IO across the full ODR period.
6. The $\overline{DRDY}$ signal can synchronize the data being read into the host controller.

Figure 153 shows how the recommended interface operates. The data read back spans the entire length of the $\overline{DRDY}$ period and the LSB remains until $\overline{DRDY}$ goes high for the next conversion.

Initializing the Recommended Interface

Follow these steps to configure the recommended interface:

1. Configure the device settings, such as the power mode, decimation ratio, filter type, and so on.
2. Enter the continuous readback mode.
3. Issue a synchronization pulse to apply the changes to the digital domain and reset the digital filter. Issue the pulse immediately after $\overline{DRDY}$ goes high.

Recommended Interface for Reading Data

The recommended interface for reading data is as follows:

1. Synchronize the host controller with the $\overline{DRDY}$ or $\overline{RDY}$ pulse. See Figure 6 for details on the $\overline{RDY}$ behavior before data is clocked out.
2. Generate SCLK based on the $\overline{DRDY}$ or $\overline{RDY}$ timing. SCLK is high when the $\overline{DRDY}$ signal goes high and transitions on the MCLK falling edges (see Figure 153) to ensure that the LSB can be read correctly as the DOUT/$\overline{RDY}$ output is reset on the $\overline{DRDY}$ rising edge. However, SCLK rising occurs before this transition.
3. The MSB is clocked out on the next falling edge of SCLK.
4. In the $\overline{PIN}$ control mode, the LSB of the conversion output is the last bit of the status output. In the $\overline{PIN}$ control mode, this bit is always 1 and, therefore, does not need to be read.

Resynchronization of the Recommended Interface

Because the full ODR period is for clocking data, the $\overline{RDY}$ signal no longer flags after each LSB outputs. This signal only flags if the ADAQ7768-1 is in the continuous readback mode, or if the ADAQ7768-1 does not count 32 SCLKs within 1 × t_{MCLK} before $\overline{DRDY}$, as shown in Figure 153.

The $\overline{RDY}$ function is only available in the continuous readback mode. In normal readback, where the ADC_DATA register must be addressed each time, the DOUT line is reset 1 × t_{MCLK} before $\overline{DRDY}$, per t_{10} in the Timing Specifications section. If $\overline{DRDY}$ is used, the device operates as normal, and conversion readback is timed from the $\overline{DRDY}$ pulse. In the case wheref $\overline{RDY}$ detects the beginning of each sample, and where the data readback loses synchronization, the SCLK timing can be recovered by one of the following two methods:

- Using $\overline{CS}$ to reset the interface and to observe the $\overline{RDY}$ transition.
- Stopping SCLK toggling until the $\overline{RDY}$ transition is detected one more time.

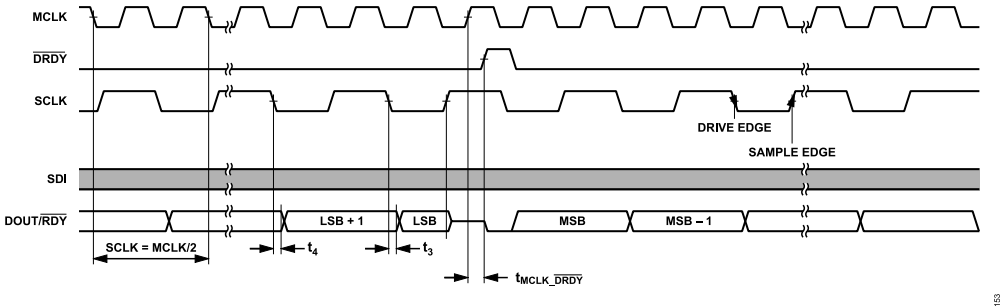

Figure 153. Recommended Interface for Reading Conversions, SPI Control, Continuous Readback Mode

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PROGRAMMABLE DIGITAL FILTER

If there are additional filter requirements outside of the digital filters offered by default on the ADAQ7768-1, there is the added option to design and upload a custom digital filter to memory. This upload overwrites the default wideband low ripple FIR filter coefficients to be replaced by a set of user-defined coefficients.

The ADAQ7768-1 filter path has three separate stages:

- Initial sinc filter
- Sinc compensation filter
- Wideband low ripple FIR filter

The user cannot change the first two stages. The only programmable stage is the third stage, where the default wideband low ripple FIR filter coefficients can be replaced by a set of user-defined coefficients.

The data rate into the third stage is double the final ODR due to a fixed decimation by two that occurs after the final stage of filtering. Therefore, the programmable FIR stage receives data at a rate decimated from f_{MOD} by rates of 16, 32, 64, 128, 256, and 512.

After the final decimation by 2, the overall decimation values are given and are in the range of decimate by 32 to decimate by 1024. Table 23 lists the data rates into the final FIR stage. Table 23 describes the data rate into the final filter stage for each power mode, assuming the correct MCLK_DIV setting is selected for the corresponding power mode.

Filter Coefficients

The ADAQ7768-1 wideband low ripple FIR filter uses a set of 112 coefficients. By writing the appropriate key to the ADAQ7768-1, these coefficients can be overwritten. Then, the customized filter coefficients can upload and lock into memory. If the ADAQ7768-1 is reset, these coefficients must be rewritten.

The coefficients uploaded are subject to the following required conditions:

- The number of coefficients in a full set is 112, made up of 56 coefficients mirrored to make the total coefficients sum of 112. Therefore, only 56 coefficients are written to during any one filter upload.
- Coefficients written must be in the integer form. The format used is twos complement.
- The coefficient data register to be written is 24 bits wide, which is the only 24-bit register write used on the ADAQ7768-1. Only 23 bits are used for the coefficients. The remaining MSB is a control bit, detailed in the Register 0x33.
- Filter coefficients are scaled such that the 56 coefficients must sum to 2^{22}. The total (112) coefficients, therefore, sum to 2^{23}.

For example, if the filter coefficient to be written to is −0.0123, this value is scaled to $-0.0123 \times 2^{22} = -51{,}590$. In the twos complement format, this value is represented by 0x7F367A.

Each filter coefficient is written by first selecting the coefficient address. Then, a separate write of the data occurs, which is repeated for all 56 coefficients from Address 0 to Address 55.

Because the FIR size cannot be changed, the filter group delay remains fixed at 34/ODR when using the programmable filter option. If a shorter number of coefficients are required, padding the end coefficients with zeros can achieve this requirement. The group delay of the uploaded filter must always be equal to the group delay of the default ADAQ7768-1 FIR filter that equals approximately 34/ODR.

Each time either the coefficient address register or the coefficient data register (COEFF_CONTROL or COEFF_DATA) is accessed, the user must wait before performing another read or write. The following equation determines the wait time:

$$t_{WAIT} = 512/MCLK$$

This wait time allows time for the register contents to update. Then, the coefficients are written to memory.

Table 23. Data Rates into the Final FIR Input Stage

	Input to Third Stage, Programmable FIR (MCLK = 16.384 MHz)								
Power Mode	**512 kHz**	**256 kHz**	**128 kHz**	**64 kHz**	**32 kHz**	**16 kHz**	**8 kHz**	**4 kHz**	**2 kHz**
High Performance (Fast)	Yes	Yes	Yes	Yes	Yes	Yes		Not applicable	Not applicable
Eco Mode	Not applicable	Not applicable	Not applicable	Yes	Yes	Yes	Yes	Yes	Yes

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Upload Sequence

To program a user-defined set of filter coefficients, perform the following sequence of steps:

1. Write 0x4 to the filter bits in the DIGITAL_FILTER register (Register 0x19, Bits[6:4]).
2. The following key must be written to access the filter upload. First, write 0xAC to the ACCESS_KEY register (Register 0x34). Second, write 0x45 to the ACCESS_KEY register. Bit 0 (the key bit) of the ACCESS_KEY register can be read back to check if the key is entered correctly.
3. Write 0xC0 to the COEFF_CONTROL register (Register 0x32). Wait for t_{WAIT} seconds to perform the following actions:
   a. Set the coefficient address to Address 0.
   b. Enable the access to memory (COEFFACCESSEN = 1).
   c. Allow a write to the coefficient memory (COEFFWRITEEN = 1).
4. The address of the first coefficient is selected. Write the required coefficient to the COEFF_DATA register (Register 0x33), and then wait for t_{WAIT} seconds. Always wait t_{WAIT} seconds between writes to Register 0x32 and Register 0x33.
5. Repeat steps 4 and 5 for each of the 56 coefficients. For example, write 0xC1 to COEFF_CONTROL to select coefficient Address 1. After waiting t_{WAIT} seconds, enter the coefficient data. Increment the data until Coefficient 55 is reached (Coefficient 55 is a write of 0xF7 to COEFF_ CONTROL).
6. Disable writing to the coefficients by first writing 0x80 to COEFF_CONTROL. Then, wait t_{WAIT} seconds. Then, write 0x00 to COEFF_CONTROL to disable coefficient access.
7. Set USERCOEFFEN = 1 by writing 0x800 to COEFF_DATA to allow the user to toggle the synchronization pulse and begin reading data.
8. Exit the filter upload by writing 0x55 to the ACCESS_KEY register (Register 0x34).
9. Send a synchronization pulse to the ADAQ7768-1. One way of sending this pulse is by writing to the SYNC_RESET register (Register 0x1D). The filter upload is now complete.

The RAM CRC error check fails when the digital filter uploads. To disable this check, use the DIG_DIAG_ENABLE register (Register 0x2A).

See the Register Details section for further details on the register bits.

Example of Filter Upload

The following sequence programs a Sinc1 filter. The coefficients in Address 0 to Address 23 = 0. The coefficients from Address 24 to Address 55 = 131,072 ($2^{22}/32$). When MCLK = 16.384 MHz and ODR = 256 kHz, the filter notch appears at 8 kHz and multiples of 8 kHz. This filter provides low noise and is recognizable by the distinctive filter profile shown in Figure 154.

Follow these steps to program the filter:

1. Write 0x4 to the filter bits in the DIGITAL_FILTER register (Register 0x19, Bits[6:4]).
2. Enter the key by writing to the ACCESS_KEY register (Register 0x34).
3. Write 0xC0 to the COEFF_CONTROL register, Register 0x32, (COEFFADDR = 0, COEFFACCESSEN = 1, and COEFFWRITEEN = 1). Wait t_{WAIT} seconds.
4. Write 0x000000 to COEFF_DATA (Register 0x33). Wait t_{WAIT} seconds.
5. Write 0xC1 to the COEFF_CONTROL register (COEFFADDR = 1). Wait t_{WAIT} seconds. In this case, the coefficient in Address 0 is equal to Address 1 and, therefore, the value in COEFF_DATA does not change.
6. Write 0xC2 to the COEFF_CONTROL register (COEFFADDR = 2). Wait t_{WAIT} seconds.
7. Increment the address of the COEFF_CONTROL register (COEFFADDR = 23) until the write of 0xD7. Continue to wait t_{WAIT} seconds.
8. Write 0xD8 to COEFF_CONTROL (COEFFADDR = 24).
9. Write 0x010000 to COEFF_DATA. Wait t_{WAIT} seconds.
10. Write 0xD9 to COEFF_CONTROL (COEFFADDR = 25). Wait t_{WAIT} seconds.
11. Write 0xDA to COEFF_CONTROL (COEFFADDR = 26) Wait t_{WAIT} seconds.
12. Increment the address of the COEFF_CONTROL register (COEFFADDR = 55) until the write 0xF7. Wait t_{WAIT} seconds.
13. Disable write and access by first writing 0x80 to the COEFF_CONTROL register. Wait t_{WAIT} seconds. Then, write 0x00 to the COEFF_CONTROL register.
14. Set USERCOEFFEN = 1 to toggle the synchronization without reloading the default coefficients (write 0x800000 to COEFF_DATA).
15. Exit the write by writing 0x55 to the ACCESS_KEY register.
16. Toggle the synchronization.
17. Gather data. Figure 154 shows the resulting filter profile.

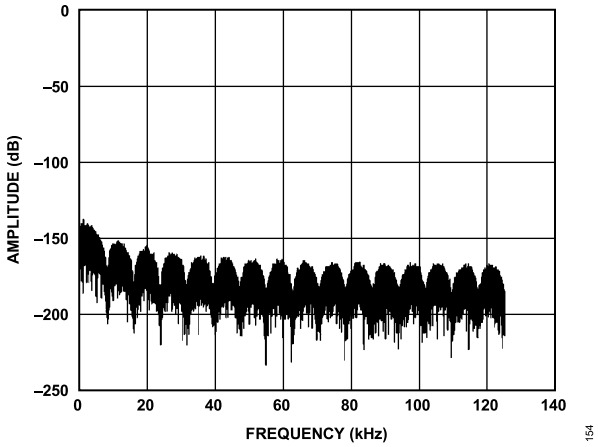

Figure 154. Example of Filter Profile Upload

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Verifying the Filter Upload

To check that the filter coefficients are uploaded correctly, it is possible to read back the values written to the COEFF_DATA register. This read can be performed after an upload with the following steps:

1. Enter the key by writing to the ACCESS_KEY register (Register 0x34). First, write 0xAC to the ACCESS_KEY register, and then write 0x45 to the ACCESS_KEY register.
2. Write 0x80 to the COEFF_CONTROL register, Register 0x32, (COEFFADDR = 0, COEFFACCESSEN = 1, COEFFWRITEEN = 0). Wait t_{WAIT} seconds.
3. Read back the contents of the 24-bit COEFF_DATA register (Register 0x33). Check that the coefficient matches the uploaded value.
4. Write 0x81 to the COEFF_CONTROL register (COEFFADDR = 1). Wait t_{WAIT} seconds.
5. Read the 24-bit COEFF_DATA register for Address 1. Increment and continue to read back the data. Continue to wait t_{WAIT} seconds between updates to the COEFF_CONTROL register.
6. Disable the coefficient access by writing 0x00 to the COEFF_CONTROL register.
7. Exit the readback process by writing 0x55 to the ACCESS_KEY register.

LAYOUT GUIDELINES

To achieve a reliable and optimal performance of the ADAQ7768-1, there are some guidelinesfor the printed circuit board (PCB).

It is recommended to have non-solder mask-defined (NSMD) pads on the PCB. This provides a larger metal area for the solder to bind to, improving solder joint reliability.

The PCB that houses the ADAQ7768-1 should be designed so that the analog and digital sections are separated and confined to different areas of the board. The ADAQ7768-1 pins are laid out with analog and digital pin partitioning. For ease of routing, the analog input pins (IN- and IN+) are located on C1 and D1.

At least one ground plane should be used. It can be common or split between the digital and analog sections. For the split plane, the digital and analog ground planes should be joined in only one place, preferably as close as possible to the ADAQ7768-1.

If the ADAQ7768-1 is in a system where multiple devices require analog-to-digital ground connections, the connection should still be made at only one point: a star ground point that should be established as close as possible to the ADAQ7768-1. Good connections should be made to the ground plane. Avoid sharing one connection for multiple ground pins. Use individual vias or multiple vias to the ground plane for each ground pin.

Avoid running digital lines under the devices because doing so couples noise onto the die. The analog ground plane should be allowed to run under the ADAQ7768-1 to avoid noise coupling. Fast switching signals like MCLK should be shielded with digital ground to avoid radiating noise to other sections of the board, and they should never run near analog signal paths. Avoid the crossover of digital and analog signals. Traces on layers close on the board should run at right angles to each other to reduce the effect of feedthrough through the board.

The power supply lines to the VDD_PGA, VSS_PGA, IN_LDO, and VDD_IO pins on the ADAQ7768-1 should use as large trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. When possible, use supply planes to make good connections between the ADAQ7768-1 supply pins and power supplies on the board. Use a single via or multiple vias for each supply pin.

Decouple the REF, AREG_CAP, and DREG_CAP pins with minimal parasitic inductances by placing the reference decoupling ceramic capacitor close to (ideally right up against) the REF and GND pins, and connect them with wide, low-impedance traces.

Figure 155 shows an example of the ADAQ7768-1 layout.

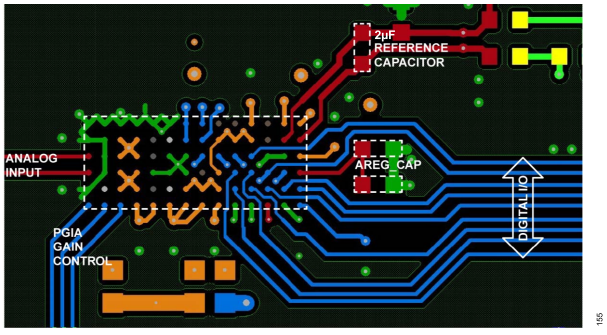

Figure 155. Example Layout of ADAQ7768-1 (Top Layer)

REGISTER SUMMARY

Table 24. ADAQ7768-1 Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x03	CHIP_TYPE	[7:0]	RESERVED				CLASS				0x07	R
0x04	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]								0x01	R
0x05	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]								0x00	R
0x06	CHIP_GRADE	[7:0]	GRADE				DEVICE_REVISION				0x00	R
0x0A	SCRATCH_PAD	[7:0]	VALUE								0x00	R/W
0x0C	VENDOR_L	[7:0]	VID[7:0]								0x56	R
0x0D	VENDOR_H	[7:0]	VID[15:8]								0x04	R
0x14	INTERFACE_FORMAT	[7:0]	LV_BOOST	EN_SPI_CRC	CRC_TYPE	STATUS_EN	CONVLEN	EN_RDY_DOUT	RESERVED	EN_CONT_READ	0x00	R/W
0x15	POWER_CLOCK	[7:0]	CLOCK_SEL		MCLK_DIV		ADC_POWER_DOWN	RESERVED	ADC_MODE		0x00	R/W
0x16	ANALOG	[7:0]	REF_BUF_POS		REF_BUF_NEG		RESERVED		LINEARITY_BOOST_A_OFF	LINEARITY_BOOST_B_OFF	0x00	R/W
0x18	CONVERSION	[7:0]	DIAG_MUX_SELECT				CONV_DIAG_SELECT	CONV_MODE			0x00	R/W
0x19	DIGITAL_FILTER	[7:0]	EN_60HZ_REJ	FILTER			RESERVED	DEC_RATE			0x00	R/W
0x1A	SINC3_DEC_RATE_MSB	[7:0]	RESERVED			SINC3_DEC[12:8]					0x00	R/W
0x1B	SINC3_DEC_RATE_LSB	[7:0]	SINC3_DEC[7:0]								0x00	R/W
0x1C	DUTY_CYCLE_RATIO	[7:0]	IDLE_TIME								0x00	R/W
0x1D	SYNC_RESET	[7:0]	SPI_START	SYNC_OUT_POS_EDGE	RESERVED		EN_GPIO_START	RESERVED	SPI_RESET		0x80	R/W
0x1E	GPIO_CONTROL	[7:0]	UGPIO_EN	GPIO2_OPEN_DRAIN_EN	GPIO1_OPEN_DRAIN_EN	GPIO0_OPEN_DRAIN_EN	GPIO3_OP_EN	GPIO2_OP_EN	GPIO1_OP_EN	GPIO0_OP_EN	0x00	R/W
0x1F	GPIO_WRITE	[7:0]	RESERVED				GPIO_WRITE_3	GPIO_WRITE_2	GPIO_WRITE_1	GPIO_WRITE_0	0x00	R/W
0x20	GPIO_READ	[7:0]	RESERVED				GPIO_READ_3	GPIO_READ_2	GPIO_READ_1	GPIO_READ_0	0x00	R
0x21	OFFSET_HI	[7:0]	OFFSET[23:16]								0x00	R/W
0x22	OFFSET_MID	[7:0]	OFFSET[15:8]								0x00	R/W
0x23	OFFSET_LO	[7:0]	OFFSET[7:0]								0x00	R/W
0x24	GAIN_HI	[7:0]	GAIN[23:16]								0x00	R/W
0x25	GAIN_MID	[7:0]	GAIN[15:8]								0x00	R/W
0x26	GAIN_LO	[7:0]	GAIN[7:0]								0x00	R/W
0x28	SPI_DIAG_ENABLE	[7:0]	RESERVED			EN_ERR_SPI_IGNORE	EN_ERR_SPI_CLK_CNT	EN_ERR_SPI_RD	EN_ERR_SPI_WR	RESERVED	0x10	R/W
0x29	ADC_DIAG_ENABLE	[7:0]	RESERVED		EN_ERR_DLDO_PSM	EN_ERR_ALDO_PSM	EN_ERR_REF_DET	EN_ERR_FILTER_SATURATED	EN_ERR_FILTER_NOT_SETTLED	EN_ERR_EXT_CLK_QUAL	0x07	R/W
0x2A	DIG_DIAG_ENABLE	[7:0]	RESERVED			EN_ERR_MEMMAP_CRC	EN_ERR_RAM_CRC	EN_ERR_FUSE_CRC	RESERVED	EN_FREQ_COUNT	0x0D	R/W
0x2C	ADC_DATA	[23:16]	ADC_READ_DATA[23:16]								0x000000	R

REGISTER SUMMARY

Table 24. ADAQ7768-1 Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
		[15:8]	ADC_READ_DATA[15:8]									
		[7:0]	ADC_READ_DATA[7:0]									
0x2D	MASTER_STATUS	[7:0]	MASTER_ERROR	ADC_ERROR	DIG_ERROR	ERR_EXT_CLK_QUAL	FILT_SATURATED	FILT_NOT_SETTLED	SPI_ERROR	POR_FLAG	0x00	R
0x2E	SPI_DIAG_STATUS	[7:0]	RESERVED			ERR_SPI_IGNORE	ERR_SPI_CLK_CNT	ERR_SPI_RD	ERR_SPI_WR	ERR_SPI_CRC	0x00	R/W
0x2F	ADC_DIAG_STATUS	[7:0]	RESERVED		ERR_DLDO_PSM	ERR_ALDO_PSM	ERR_REF_DET	FILT_SATURATED	FILT_NOT_SETTLED	ERR_EXT_CLK_QUAL	0x00	R
0x30	DIG_DIAG_STATUS	[7:0]	RESERVED			ERR_MEMMAP_CRC	ERR_RAM_CRC	ERR_FUSE_CRC	RESERVED		0x00	R
0x31	MCLK_COUNTER	[7:0]	MCLK_COUNTER								0x00	R
0x32	COEFF_CONTROL	[7:0]	COEFF_ACCESS_EN	COEFF_WRITE_EN	COEFF_ADDR						0x00	R/W
0x33	COEFF_DATA	[23:16]	USER_COEFF_EN	COEFF_DATA[22:16]							0x000000	R/W
		[15:8]	COEFF_DATA[15:8]									
		[7:0]	COEFF_DATA[7:0]									
0x34	ACCESS_KEY	[7:0]	RESERVED							KEY	0x00	R/W

REGISTER DETAILS

COMPONENT TYPE REGISTER

Register: 0x03, Reset: 0x07, Name: CHIP_TYPE

Table 25. Bit Descriptions for CHIP_TYPE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CLASS	Chip Type 111: Analog to digital converter.	0x7	R

UNIQUE PRODUCT ID REGISTER

Register: 0x04, Reset: 0x01, Name: PRODUCT_ID_L

Table 26. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product ID	0x1	R

Register: 0x05, Reset: 0x00, Name: PRODUCT_ID_H

Table 27. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product ID	0x0	R

DEVICE GRADE AND REVISION REGISTER

Register: 0x06, Reset: 0x00, Name: CHIP_GRADE

Table 28. Bit Descriptions for CHIP_GRADE

Bits	Bit Name	Description	Reset	Access
[7:4]	GRADE	Device Grade	0x0	R
[3:0]	DEVICE_REVISION	Device Revision ID	0x0	R

USER SCRATCHPAD REGISTER

Register: 0x0A, Reset: 0x00, Name: SCRATCH_PAD

Table 29. Bit Descriptions for SCRATCH_PAD

Bits	Bit Name	Description	Reset	Access
[7:0]	VALUE	Scratch PAD - Read/Write area communication/POR check	0x0	R/W

DEVICE VENDOR ID REGISTER

Register: 0x0C, Reset: 0x56, Name: VENDOR_L

Table 30. Bit Descriptions for VENDOR_L

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[7:0]	Vendor ID	0x56	R

Register: 0x0D, Reset: 0x04, Name: VENDOR_H

Table 31. Bit Descriptions for VENDOR_H

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[15:8]	Vendor ID	0x4	R

INTERFACE FORMAT CONTROL REGISTER

Register: 0x14, Reset: 0x00, Name: INTERFACE_FORMAT

REGISTER DETAILS

Table 32. Bit Descriptions for INTERFACE_FORMAT

Bits	Bit Name	Description	Reset	Access
7	LV_BOOST	Boosts drive strength of SPI output for use with IOVDD levels of 1.8 V, or when a high capacitive-load is present on the DOUT/$\overline{RDY}$ pin. The default state is LV_BOOST enabled when in the $\overline{PIN}$ control mode. 0: Disables LV_BOOST. 1: Enables LV_BOOST. Re-enable this bit following an exit from the continuous read mode, if applicable.	0x0	R/W
6	EN_SPI_CRC	Activates CRC on all SPI transactions 0: Disable CRC function on all SPI transfers. 1: Enable CRC function on all SPI transfers.	0x0	R/W
5	CRC_TYPE	Selects CRC method as XOR or 8-bit polynomial 1: XOR instead of CRC (applied to read transactions only). 0: CRC bits are based on CRC-8 Polynomial.	0x0	R/W
4	STATUS_EN	Enables Status bits output. In the SPI control mode, the status bits can be output after the ADC conversion result by setting the bits in this bit field. In the $\overline{PIN}$ control mode, the status bits are output after the ADC conversion result. 0: Disable outputting STATUS bits after ADC result in the continuous read mode. 1: Output STATUS bits after ADC result in the continuous read mode.	0x0	R/W
3	CONVLEN	Conversion Result Output Length 0: Full 24 BIT. 1: Output only 16 MSB of the ADC result.	0x0	R/W
2	EN_RDY_DOUT	Enables $\overline{RDY}$ signal on DOUT/$\overline{RDY}$ pin. Enables $\overline{RDY}$ indicator on DOUT/$\overline{RDY}$ pin in the continuous read mode. By default, the DOUT/$\overline{RDY}$ pin does not signal when new ADC conversion data is ready. Setting this bit causes DOUT/RDY to signal the availability of ADC conversion data. 0: Disables $\overline{RDY}$ function on DOUT/$\overline{RDY}$ in the continuous read mode after the result is clocked out. 1: Enables $\overline{RDY}$ function on DOUT/$\overline{RDY}$ in the continuous read mode after the result is clocked out.	0x0	R/W
1	RESERVED	Reserved.	0x0	R
0	EN_CONT_READ	Continuous read enable bit 0: Disable Continuous Read Mode. 1: Enable Continuous Read Mode.	0x0	R/W

POWER AND CLOCK CONTROL REGISTER

Register: 0x15, Reset: 0x00, Name: POWER_CLOCK

Table 33. Bit Descriptions for POWER_CLOCK

Bits	Bit Name	Description	Reset	Access
[7:6]	CLOCK_SEL	Options for setting the clock used by the device. 00: CMOS clock on XTAL2_MCLK. 01: Crystal oscillator. 10: LVDS input enable. 11: Internal coarse RC clock (diagnostics).	0x0	R/W
[5:4]	MCLK_DIV	Sets the division of the MCLK to create the ADC modulator frequency f_{MOD}. 00: Modulator CLK is equal to controller clock divided by 16. 01: Modulator CLK is equal to controller clock divided by 8. 10: Modulator CLK is equal to controller clock divided by 4. 11: Modulator CLK is equal to controller clock divided by 2.	0x0	R/W
3	ADC_POWER_DOWN	Places ADC into a power-down state. All blocks including the SPI are powered down. The standard SPI is not active in this state. Power-down is the lowest power consumption mode. To enter the power-down mode, write 0x08 to this register. For attempts to set Bit 3 while also setting other bits in this register, the SPI write command is ignored, the device does not enter power-down, and the other bits are not set. Exit the power-down mode in three ways: by a reset using the $\overline{RESET}$ pin, by issuing the SPI resume command over SDI and SCLK, or by using the power cycle of the device.	0x0	R/W
2	RESERVED	Reserved.	0x0	R/W

REGISTER DETAILS

Table 33. Bit Descriptions for POWER_CLOCK (Continued)

Bits	Bit Name	Description	Reset	Access
[1:0]	ADC_MODE	Sets the operation mode of the ADC core. This setting with MCLK_DIV create the conditions for the power scaling the ADC vs. input bandwidth/throughput. 00: Eco Mode. 11: High Performance Mode.	0x0	R/W

ANALOG BUFFER CONTROL REGISTER

Register: 0x16, Reset: 0x00, Name: ANALOG

Table 34. Bit Descriptions for ANALOG

Bits	Bit Name	Description	Reset	Access
[7:6]	REF_BUF_POS	Buffering options for the reference positive input. 00: Precharge reference buffer on. 01: Unbuffered reference input. 10: Full reference buffer on.	0x0	R/W
[5:4]	REF_BUF_NEG	Buffering options for the reference negative input. 00: Precharge reference buffer on. 01: Unbuffered input. 10: Full reference buffer on.	0x0	R/W
[3:2]	RESERVED	Reserved.	0x0	R
1	LINEARITY_BOOST_A_OFF	Linearity boost buffer A disable control. Setting this bit disables the linearity boost buffer A. Use with LINEARITY_BOOST_B_OFF. 0: Linearity boost buffer A enable. 1: Linearity boost buffer A disable.	0x0	R/W
0	LINEARITY_BOOST_B_OFF	Linearity boost buffer B disable control. Setting this bit disables the linearity boost buffer B. Use with LINEARITY_BOOST_A_OFF. 0: Linearity boost buffer B enable. 1: Linearity boost buffer B disable.	0x0	R/W

CONVERSION SOURCE SELECT AND MODE CONTROL REGISTER

Register: 0x18, Reset: 0x00, Name: CONVERSION

Table 35. Bit Descriptions for CONVERSION

Bits	Bit Name	Description	Reset	Access
[7:4]	DIAG_MUX_SELECT	Selects which signal to route through diagnostic mux. Perform diagnostic checks in low-power mode only. 0000: Temperature sensor. 1000: ADC input short (zero check). 1001: Positive full scale. 1010: Negative full scale.	0x0	R/W
3	CONV_DIAG_SELECT	Selects the ADC's input for conversion as normal or diagnostic mux. 0: Converting signal through the normal signal chain. 1: ADC converting (and turning on) diagnostic sub-blocks.	0x0	R/W
[2:0]	CONV_MODE	Sets the conversion mode of the ADC. 000: Continuous Conversion Mode. The modulator is converting continuously. Continuous $\overline{\text{DRDY}}$ pulse for every filter conversion. 001: Continuous One-Shot Mode. One shot is the method of using the $\overline{\text{SYNC\_IN}}$ time to start a conversion. It is similar to a conversion start signal when using the one-shot mode. The ADC modulator is continuously running while waiting on a $\overline{\text{SYNC\_IN}}$ rising edge. On release of a pulse (low to high transition) to the $\overline{\text{SYNC\_IN}}$ pin, a new conversion begins, converting and integrating over the settling time of the filter selected. $\overline{\text{DRDY}}$ toggles when the conversion completes, indicating it is available for readback over the SPI.	0x0	R/W

REGISTER DETAILS

Table 35. Bit Descriptions for CONVERSION (Continued)

Bits	Bit Name	Description	Reset	Access
		010: Single-Conversion Standby Mode. In single-conversion standby mode, the ADC runs one conversion with the selected filter, sampling and integrating over the full settling time of the filter before providing a single conversion result. After the conversion is complete, the ADC goes into standby. Initiating another single conversion from standby means that there is a start-up time to come out of standby before the ADC begins converting to produce the single conversion. This mode is recommended for use in the low-power mode. 011: Duty Cycled Conversion Standby Mode. Low-power periodic conversion is a method of setting the single conversion to run in a timed loop. A separate register sets the ratio for the time spent in standby vs. converting. The ADC automatically comes out of standby periodically, performs a single conversion, and then returns to standby without the need to initiate the single conversion over the SPI. 100: Standby.		

DIGITAL FILTER AND DECIMATION CONTROL REGISTER

Register: 0x19, Reset: 0x00, Name: DIGITAL_FILTER

Table 36. Bit Descriptions for DIGITAL_FILTER

Bits	Bit Name	Description	Reset	Access
7	EN_60HZ_REJ	For use with Sinc3 filter only. First, program the Sinc3 filter to output at 50 Hz. Subsequently selecting EN_60HZ_REJ bit allows one zero of the Sinc3 filter to fall at 60 Hz. This bit only enables rejection of both 50 Hz and 60 Hz if it is set in combination with programming the Sinc3 filter for 50 Hz ODR. 0: Sinc3 Filter optimized for single frequency rejection — 50 Hz or 60 Hz. 1: Filter operation is modified to allow both 50 Hz and 60 Hz Rejection.	0x0	R/W
[6:4]	FILTER	Selects the style of filter for use 000: Sinc5 filter. Decimate x32 to x1024. Use DEC_RATE bits to select one of six available decimation rates from x32 to x1024. 001: Sinc5 filter. Decimate x8 only. Enables a maximum data rate of 1 MHz. This path allows viewing of wider bandwidth. However, it is quantization noise limited so output data is reduced to 16-bits. 010: Sinc5 filter. Decimate x16 only. Enables a maximum data rate of 512 kHz. This path allows viewing of wider bandwidth. 011: Sinc3 filter. Programmable decimation rate. Decimation rate is selected through SINC3_DEC bits in Sinc3 decimation rate MSB and LSB registers. The Sinc3 filter can be tuned to reject 50 Hz or 60 Hz. With EN_60HZ_REJ bit set, it can allow rejection of both 50 Hz and 60 Hz when used with a 16.384 MHz MCLK. 100: Wideband Low Ripple FIR filter. FIR filter with wideband low ripple passband and sharp transition band. Use DEC_RATE bits to select one of six available decimation rates from x32 to x1024.	0x0	R/W
3	RESERVED	Reserved.	0x0	R
[2:0]	DEC_RATE	Selects the decimation rate for the Sinc5 filter and wideband low ripple FIR filter. 000: Decimate x32. 001: Decimate x64. 010: Decimate x128. 011: Decimate x256. 100: Decimate x512. 101: Decimate x1024. 110: Decimate x1024. 111: Decimate x1024.	0x0	R/W

SINC3 DECIMATION RATE (MSB) REGISTER

Register: 0x1A, Reset: 0x00, Name: SINC3_DEC_RATE_MSB

Table 37. Bit Descriptions for SINC3_DEC_RATE_MSB

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS

Table 37. Bit Descriptions for SINC3_DEC_RATE_MSB (Continued)

Bits	Bit Name	Description	Reset	Access
[4:0]	SINC3_DEC[12:8]	Determines the decimation rate used with the Sinc3 filter. Value entered is incremented by 1 and multiplied by 32 to give actual decimation rate.	0x0	R/W

SINC3 DECIMATION RATE (LSB) REGISTER

Register: 0x1B, Reset: 0x00, Name: SINC3_DEC_RATE_LSB

Table 38. Bit Descriptions for SINC3_DEC_RATE_LSB

Bits	Bit Name	Description	Reset	Access
[7:0]	SINC3_DEC[7:0]	Determines the decimation rate used with the Sinc3 filter. Value entered is incremented by 1 and multiplied by 32 to give actual decimation rate.	0x0	R/W

PERIODIC CONVERSION RATE CONTROL REGISTER

Register: 0x1C, Reset: 0x00, Name: DUTY_CYCLE_RATIO

Table 39. Bit Descriptions for DUTY_CYCLE_RATIO

Bits	Bit Name	Description	Reset	Access
[7:0]	IDLE_TIME	Sets idle time for periodic conversion when in standby. 1 in this register corresponds to time for one output from filter selected. The value in this register is incremented by one and doubled.	0x0	R/W

SYNCHRONIZATION MODES AND RESET TRIGGERING REGISTER

Register: 0x1D, Reset: 0x80, Name: SYNC_$\overline{\text{RESET}}$

Table 40. Bit Descriptions for SYNC_$\overline{\text{RESET}}$

Bits	Bit Name	Description	Reset	Access
7	SPI_$\overline{\text{START}}$	Trigger $\overline{\text{START}}$ signal. Initiates a $\overline{\text{SYNC\_OUT}}$ pulse over SPI. Setting this bit low drives a low pulse through $\overline{\text{SYNC\_OUT}}$, which can be used as a $\overline{\text{SYNC\_IN}}$ signal to the same device and other ADAQ7768-1 devices where synchronized sampling is required. This bit clears itself after use.	0x1	R
6	$\overline{\text{SYNC_OUT}}$_POS_EDGE	$\overline{\text{SYNC\_OUT}}$ drive edge select. Setting this bit causes $\overline{\text{SYNC\_OUT}}$ to be driven low by the positive edge of MCLK. Device default is that $\overline{\text{SYNC\_OUT}}$ is driven low on the negative edge of MCLK.	0x0	R/W
[5:4]	RESERVED	Reserved.	0x0	R
3	EN_GPIO_$\overline{\text{START}}$	Enable $\overline{\text{START}}$ function on the GPIO input. Allows to use one of the GPIO pins as a $\overline{\text{START}}$ input pin. When enabled, a low pulse on the $\overline{\text{START}}$ input generates a low pulse through $\overline{\text{SYNC\_OUT}}$ that can be used as a $\overline{\text{SYNC\_IN}}$ signal to the same device and other ADAQ7768-1 devices where synchronized sampling is required. When enabled, GPIO3 becomes the $\overline{\text{START}}$ input. While the $\overline{\text{START}}$ function is enabled, the GPIOx pins cannot be used for general-purpose input/output reading and writing. The remaining GPIOs are set to outputs. 0: Disable 1: Enable	0x0	R/W
2	RESERVED	Reserved.	0x0	R
[1:0]	SPI_$\overline{\text{RESET}}$	Enables device reset over SPI. Two writes to these bits are required to initiate the reset. First set the bits to 11, then set the bits to 10. Once this sequence is detected on these two bits, the reset occurs. It is not dependent on other bits in this register being set or cleared.	0x0	R/W

GPIO PORT CONTROL REGISTER

Register: 0x1E, Reset: 0x00, Name: GPIO_CONTROL

Table 41. Bit Descriptions for GPIO_CONTROL

Bits	Bit Name	Description	Reset	Access
7	UGPIO_EN	Universal enabling of GPIO pins. Set this bit high to change the GPIO settings.	0x0	R/W
6	GPIO2_OPEN_DRAIN_EN	Change GPIO2 output from strong driver to open-drain.	0x0	R/W
5	GPIO1_OPEN_DRAIN_EN	Change GPIO1 output from strong driver to open-drain.	0x0	R/W

REGISTER DETAILS

Table 41. Bit Descriptions for GPIO_CONTROL (Continued)

Bits	Bit Name	Description	Reset	Access
4	GPIO0_OPEN_DRAIN_EN	Change GPIO0 output from strong driver to open-drain.	0x0	R/W
3	GPIO3_OP_EN	Output Enable for GPIO pin. 0 -> input, 1-> output	0x0	R/W
2	GPIO2_OP_EN	Output Enable for GPIO pin. 0 -> input, 1-> output	0x0	R/W
1	GPIO1_OP_EN	Output Enable for GPIO pin. 0 -> input, 1-> output	0x0	R/W
0	GPIO0_OP_EN	Output Enable for GPIO pin. 0 -> input, 1-> output	0x0	R/W

GPIO OUTPUT CONTROL REGISTER

Register: 0x1F, Reset: 0x00, Name: GPIO_WRITE

Table 42. Bit Descriptions for GPIO_WRITE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	GPIO_WRITE_3	Write to this bit to set GPIO[3] HI	0x0	R/W
2	GPIO_WRITE_2	Write to this bit to set GPIO[2] HI	0x0	R/W
1	GPIO_WRITE_1	Write to this bit to set GPIO[1] HI	0x0	R/W
0	GPIO_WRITE_0	Write to this bit to set GPIO[0] HI	0x0	R/W

GPIO INPUT READ REGISTER

Register: 0x20, Reset: 0x00, Name: GPIO_READ

Table 43. Bit Descriptions for GPIO_READ

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	GPIO_READ_3	Read the value from GPIO[3]	0x0	R
2	GPIO_READ_2	Read the value from GPIO[2]	0x0	R
1	GPIO_READ_1	Read the value from GPIO[1]	0x0	R
0	GPIO_READ_0	Read the value from GPIO[0]	0x0	R

OFFSET CALIBRATION MSB REGISTER

Register: 0x21, Reset: 0x00, Name: OFFSET_HI

Table 44. Bit Descriptions for OFFSET_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	OFFSET[23:16]	User offset calibration coefficient. The offset correction registers provide 24-bit, signed, 2s-complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction. So, the ratio above changes linearly with any gain adjustment applied through the gain calibration registers.	0x0	R/W

OFFSET CALIBRATION MID REGISTER

Register: 0x22, Reset: 0x00, Name: OFFSET_MID

Table 45. Bit Descriptions for OFFSET_MID

Bits	Bit Name	Description	Reset	Access
[7:0]	OFFSET[15:8]	User offset calibration coefficient. The offset correction registers provide 24-bit, signed, 2s-complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction. So, the ratio above changes linearly with any gain adjustment applied through the gain calibration registers.	0x0	R/W

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OFFSET CALIBRATION LSB REGISTER

Register: 0x23, Reset: 0x00, Name: OFFSET_LO

Table 46. Bit Descriptions for OFFSET_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	OFFSET[7:0]	User offset calibration coefficient. The offset correction registers provide 24-bit, signed, 2s-complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction. So, the ratio above changes linearly with any gain adjustment applied through the gain calibration registers.	0x0	R/W

GAIN CALIBRATION MSB REGISTER

Register: 0x24, Reset: 0x00, Name: GAIN_HI

Table 47. Bit Descriptions for GAIN_HI

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN[23:16]	User gain calibration coefficient. The ADC has an associated factory programmed gain calibration coefficient. The coefficient is stored in the ADC during factory programming and the nominal value is around 0x555555. The user can read back the factory programmed value, and may overwrite the gain register setting to apply their own calibration coefficient. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction.	0x0	R/W

GAIN CALIBRATION MID REGISTER

Register: 0x25, Reset: 0x00, Name: GAIN_MID

Table 48. Bit Descriptions for GAIN_MID

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN[15:8]	User gain calibration coefficient. The ADC has an associated factory programmed gain calibration coefficient. The coefficient is stored in the ADC during factory programming and the nominal value is around 0x555555. The user can read back the factory programmed value, and may overwrite the gain register setting to apply their own calibration coefficient. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction.	0x0	R/W

GAIN CALIBRATION LSB REGISTER

Register: 0x26, Reset: 0x00, Name: GAIN_LO

Table 49. Bit Descriptions for GAIN_LO

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN[7:0]	User gain calibration coefficient. The ADC has an associated factory programmed gain calibration coefficient. The coefficient is stored in the ADC during factory programming and the nominal value is around 0x555555. The user can read back the factory programmed value, and may overwrite the gain register setting to apply their own calibration coefficient. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction.	0x0	R/W

SPI DIAGNOSTIC CONTROL REGISTER

Register: 0x28, Reset: 0x10, Name: SPI_DIAG_ENABLE

Table 50. Bit Descriptions for SPI_DIAG_ENABLE

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	EN_ERR_SPI_IGNORE	SPI Ignore Error Enable	0x1	R/W
3	EN_ERR_SPI_CLK_CNT	SPI Clock Count Error Enable. The SPI clock count error is only valid for SPI transactions that use $\overline{CS}$.	0x0	R/W
2	EN_ERR_SPI_RD	SPI Read Error Enable	0x0	R/W
1	EN_ERR_SPI_WR	SPI Write Error Enable	0x0	R/W

REGISTER DETAILS

Table 50. Bit Descriptions for SPI_DIAG_ENABLE (Continued)

Bits	Bit Name	Description	Reset	Access
0	RESERVED	Reserved.	0x0	R

ADC DIAGNOSTIC FEATURE CONTROL REGISTER

Register: 0x29, Reset: 0x07, Name: ADC_DIAG_ENABLE

Table 51. Bit Descriptions for ADC_DIAG_ENABLE

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	EN_ERR_DLDO_PSM	DLDO PSM Error Enable	0x0	R/W
4	EN_ERR_ALDO_PSM	ALDO PSM Error Enable	0x0	R/W
3	EN_ERR_REF_DET	REF DET Error Enable	0x0	R/W
2	EN_ERR_FILTER_SATURATED	Filter Saturated Error Enable	0x1	R/W
1	EN_ERR_FILTER_NOT_SETTLED	Filter Not Settled Error Enable	0x1	R/W
0	EN_ERR_EXT_CLK_QUAL	Enable qualification check on external clock.	0x1	R/W

DIGITAL DIAGNOSTIC FEATURE CONTROL REGISTER

Register: 0x2A, Reset: 0x0D, Name: DIG_DIAG_ENABLE

Table 52. Bit Descriptions for DIG_DIAG_ENABLE

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	EN_ERR_MEMMAP_CRC	Memmap CRC Error Enable	0x0	R/W
3	EN_ERR_RAM_CRC	RAM CRC Error Enable	0x1	R/W
2	EN_ERR_FUSE_CRC	Fuse CRC Error Enable	0x1	R/W
1	RESERVED	Reserved.	0x0	R/W
0	EN_FREQ_COUNT	Enable MCLK counter.	0x1	R/W

CONVERSION RESULT REGISTER

Register: 0x2C, Reset: 0x000000, Name: ADC_DATA

Table 53. Bit Descriptions for ADC_DATA

Bits	Bit Name	Description	Reset	Access
[23:16]	ADC_READ_DATA[23:16]	ADC Read Data	0x0	R
[15:8]	ADC_READ_DATA[15:8]	ADC Read Data	0x0	R
[7:0]	ADC_READ_DATA[7:0]	ADC Read Data	0x0	R

DEVICE ERROR FLAGS MASTER REGISTER

Register: 0x2D, Reset: 0x00, Name: MASTER_STATUS

Table 54. Bit Descriptions for MASTER_STATUS

Bits	Bit Name	Description	Reset	Access
7	MASTER_ERROR	Master Error	0x0	R
6	ADC_ERROR	Any ADC Error (OR)	0x0	R
5	DIG_ERROR	Any Digital Error (OR)	0x0	R
4	ERR_EXT_CLK_QUAL	No Clock Error - Applied to Master Status Register Only	0x0	R
3	FILT_SATURATED	Filter Saturated	0x0	R
2	FILT_NOT_SETTLED	Filter Not Settled	0x0	R
1	SPI_ERROR	Any SPI Error (OR)	0x0	R
0	POR_FLAG	POR Flag	0x0	R

REGISTER DETAILS

SPI ERROR REGISTER

Register: 0x2E, Reset: 0x00, Name: SPI_DIAG_STATUS

Table 55. Bit Descriptions for SPI_DIAG_STATUS

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	ERR_SPI_IGNORE	SPI Ignore Error	0x0	R/W1C
3	ERR_SPI_CLK_CNT	SPI Clock Count Error	0x0	R
2	ERR_SPI_RD	SPI Read Error	0x0	R/W1C
1	ERR_SPI_WR	SPI Write Error	0x0	R/W1C
0	ERR_SPI_CRC	SPI CRC Error	0x0	R/W1C

ADC DIAGNOSTICS OUTPUT REGISTER

Register: 0x2F, Reset: 0x00, Name: ADC_DIAG_STATUS

Table 56. Bit Descriptions for ADC_DIAG_STATUS

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	ERR_DLDO_PSM	DLDO PSM Error	0x0	R
4	ERR_ALDO_PSM	ALDO PSM Error	0x0	R
3	ERR_REF_DET	REF DET Error	0x0	R
2	FILT_SATURATED	Filter Saturated	0x0	R
1	FILT_NOT_SETTLED	Filter Not Settled	0x0	R
0	ERR_EXT_CLK_QUAL	No Clock Error - Applied to Master Status Register Only	0x0	R

DIGITAL DIAGNOSTICS OUTPUT REGISTER

Register: 0x30, Reset: 0x00, Name: DIG_DIAG_STATUS

Table 57. Bit Descriptions for DIG_DIAG_STATUS

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	ERR_MEMMAP_CRC	Memmap CRC Error	0x0	R
3	ERR_RAM_CRC	RAM CRC Error	0x0	R
2	ERR_FUSE_CRC	Fuse CRC Error	0x0	R
[1:0]	RESERVED	Reserved.	0x0	R

MCLK DIAGNOSTIC OUTPUT REGISTER

Register: 0x31, Reset: 0x00, Name: MCLK_COUNTER

Table 58. Bit Descriptions for MCLK_COUNTER

Bits	Bit Name	Description	Reset	Access
[7:0]	MCLK_COUNTER	MCLK Counter. This register increments after every 64 MCLKs.	0x0	R

COEFFICIENT CONTROL REGISTER

Register: 0x32, Reset: 0x00, Name: COEFF_CONTROL

Table 59. Bit Descriptions for COEFF_CONTROL

Bits	Bit Name	Description	Reset	Access
7	COEFF_ACCESS_EN	Setting this bit to a 1 allows access to the coefficient memory.	0x0	R/W
6	COEFF_WRITE_EN	Enables write to the coefficient memory. Write a 1 to enable.	0x0	R/W
[5:0]	COEFF_ADDR	Address to be accessed for the coefficient memory. The address ranges from 0 to 55 for 56 coefficients that form one symmetrical half of the 112 coefficients.	0x00	R/W

REGISTER DETAILS

COEFFICIENT DATA REGISTER

Register: 0x33, Reset: 0x00, Name: COEFF_DATA

Table 60. Bit Descriptions for COEFF_DATA

Bits	Bit Name	Description	Reset	Access
23	USER_COEFF_EN	Setting this bit to a 1 prevents the coefficients from ROM over writing the user-defined coefficients after a sync toggle. A sync pulse is required after every change to the ADAQ7768-1 digital filter configuration, including a customized filter upload.	0x0	R/W
[22:0]	COEFF_DATA	Data read from or to be written to coefficient memory. These bits are 23 bits wide.	0x000000	R/W

ACCESS KEY REGISTER

Register: 0x34, Reset: 0x00, Name: ACCESS_KEY

Table 61. Bit Descriptions for ACCESS_KEY

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	KEY	Write a specific key to the ACCESS_KEY register before any filter upload. If written correctly, the key bit reads back as 1.	0x0	R/W

OUTLINE DIMENSIONS

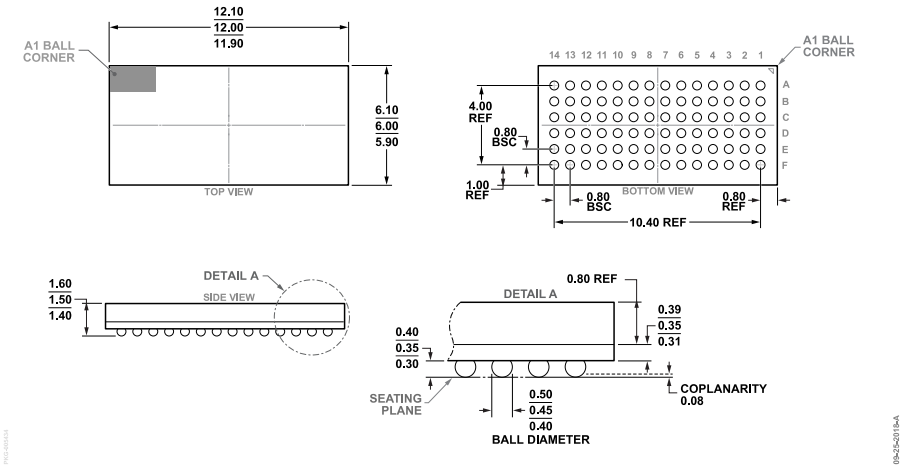

Figure 156. 84-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-84-4)
Dimensions in millimeters

Updated: March 31, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADAQ7768-1BBCZ	-40°C to +85°C	84-Ball CSP-BGA (12.00 mm x 6.00 mm x 1.50 mm)	Tray, 280	BC-84-4

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Package Description
EV-ADAQ7768-1FMC1Z	Evaluation Board

[1] Z = RoHS Compliant Part.

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