

### FEATURES

- 118 dB DAC dynamic range and SNR
- 98 dB THD + N
- Differential voltage DAC output
- 2.5 V digital, 5 V analog and 3.3 V or 5 V I/O supplies
- 521 mW total (32.6 mW/channel) quiescent power
- PLL generated or direct MCLK master clock
- Low EMI design
- Linear regulator driver to generate digital supply
- Supports 24-bit and 32 kHz to 192 kHz sample rates
- Low propagation 192 kHz sample rate mode
- Log volume control with autoramp function
- Temperature sensor with digital readout  $\pm 3^{\circ}\text{C}$  accuracy
- SPI and I<sup>2</sup>C controllable for flexibility
- Software-controllable clickless mute
- Software power-down
- Right-justified, left-justified, I<sup>2</sup>S, and TDM modes
- Master and slave modes with up to 16-channel input/output
- 80-lead LQFP package
- Qualified for automotive applications

### APPLICATIONS

- Automotive audio systems
- Home theater systems
- Digital audio effects processors

### GENERAL DESCRIPTION

The ADAU1966 is a high performance, single-chip DAC that provides 16 digital-to-analog converters (DACs) with differential output using the Analog Devices, Inc., patented multibit sigma-delta ( $\Sigma$ - $\Delta$ ) architecture. An SPI/I<sup>2</sup>C port is included, allowing a microcontroller to adjust volume and many other parameters. The ADAU1966 operates from 2.5 V digital, 5 V analog and 3.3 V or 5 V input/output supplies. A linear regulator is included to generate the digital supply voltage from the analog supply voltage. The ADAU1966 is available in an 80-lead LQFP package.

The ADAU1966 is designed for low EMI. This consideration is apparent in both the system and circuit design architectures. By using the on-board PLL to derive the internal master clock from an external LRCLK, the ADAU1966 can eliminate the need for a separate high frequency master clock and can be used with or without a bit clock. The DACs are designed using the latest Analog Devices continuous time architectures to further minimize EMI. By using 2.5 V digital supplies, power consumption is minimized, and the digital waveforms are a smaller amplitude, further reducing emissions.

### FUNCTIONAL BLOCK DIAGRAM

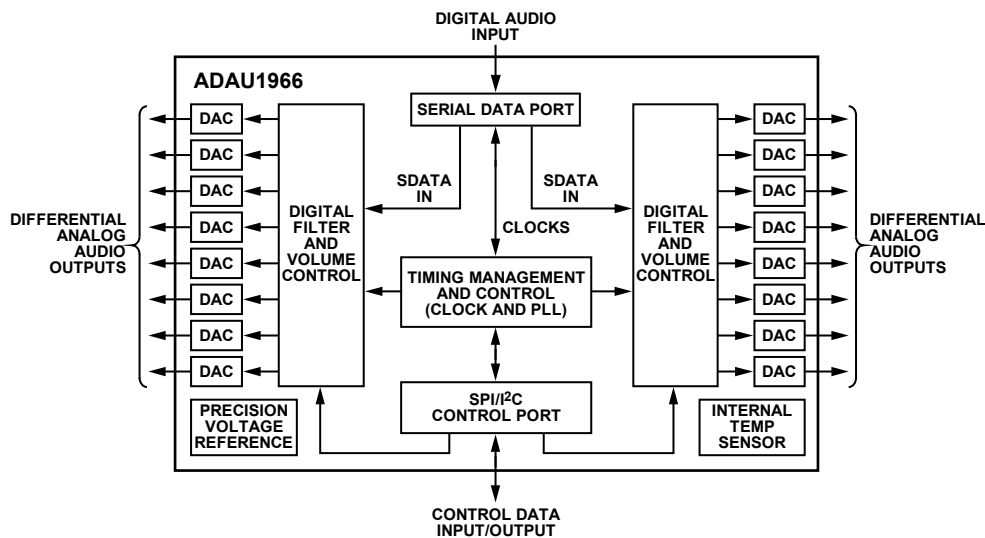


Figure 1.

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**REVISION HISTORY****3/16—Rev. D to Rev. E**

Changes to Table 4 .....5

**12/13—Rev. C to Rev. D**

Changes to Features Section ..... 1

Changes to General Description ..... 1

Changes to Specifications Section.....4

Deleted Table 3 and Table 4; Renumbered Sequentially .....5

Changes to Table 5 .....6

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Changes to Serial Control Port: SPI Control Mode Section.....19

Added Figure 14, Figure 15, and Figure 16; Renumbered  
Sequentially .....19

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Changes to Table 52, Common Mode and Pad Strength  
Register .....44**3/13—Rev. B to Rev. C**

Changes to Table 2 and Table 3 ..... 5

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Changes to I<sup>2</sup>C Control Port Section..... 18Changes to Figure 13, Table 19, Table 20, Table 21, and  
Table 22..... 19

Changes to Serial Control Port: SPI Control Mode Section .....20

**8/12—Rev. A to Rev. B**

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**7/12—Rev. 0 to Rev. A**Changed Output Resistance at Each Pin Parameter from 100  $\Omega$   
to 33  $\Omega$  ..... 4

Changes to Figure 13 ..... 19

Added Figure 14 .....20

Updated Outline Dimensions.....52

**9/11—Revision 0: Initial Version**

## SPECIFICATIONS

Performance of all channels is identical, exclusive of the interchannel gain mismatch and interchannel phase deviation specifications. Master clock = 12.288 MHz (48 kHz  $f_s$ ,  $256 \times f_s$  mode), input sample rate = 48 kHz, measurement bandwidth = 20 Hz to 20 kHz, word width = 24 bits, load capacitance (digital output) = 20 pF, load current (digital output) =  $\pm 1$  mA or  $1.5 \text{ k}\Omega$  to  $\frac{1}{2}$  DVDD supply, input voltage high = 2.0 V, input voltage low = 0.8 V, analog audio output resistive load =  $3100 \Omega$  per pin, unless otherwise noted.

### ANALOG PERFORMANCE SPECIFICATIONS

Specifications guaranteed at AVDDx = 5 V and an ambient temperature of 25°C. Supply voltages = AVDDx = 5 V, DVDD = 2.5 V, ambient temperature<sup>1</sup> ( $T_A$ ) = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
<b>DIGITAL-TO-ANALOG CONVERTERS</b>					
Dynamic Range	20 Hz to 20 kHz, -60 dB input	105	115.5		dB
No Filter (RMS)					
With A-Weighted Filter (RMS)		108	118		dB
Total Harmonic Distortion + Noise	0 dBFS		-90		dB
	Two channels running, -1 dBFS		-98		dB
	16 channels running, -1 dBFS		-98	-85	dB
Full-Scale Differential Output Voltage			3.00 ( $\pm 8.49$ )		V rms (V p-p)
Gain Error		-10		+10	%
Offset Error		-25	-6	+25	mV
Gain Drift		-30		+30	ppm/°C
Interchannel Isolation			100		dB
Interchannel Phase Deviation			0		Degrees
Volume Control Step			0.375		dB
Volume Control Range			95.25		dB
De-emphasis Gain Error				$\pm 0.6$	dB
Output Resistance at Each Pin			33		$\Omega$
<b>REFERENCE VOLTAGES</b>					
Temperature Sensor Reference Voltage	TS_REF pin		1.50		V
Common-Mode Reference Output	CM pin	2.14	2.25	2.29	V
External Reference Voltage Source	CM pin		2.25		V
<b>TEMPERATURE SENSOR</b>					
Temperature Accuracy		-3		+3	°C
Temperature Readout Range		-60		+140	°C
Temperature Readout Step Size			1		°C
Temperature Sample Rate		0.25		6	Hz
<b>REGULATOR</b>					
Input Supply Voltage	VSUPPLY pin	3.0	5	5.5	V
Regulated Output Voltage	VSENSE pin	2.26	2.50	2.59	V

<sup>1</sup> Functionally guaranteed at -40°C to +125°C case temperature.

Specifications guaranteed at AVDDx = 5 V and an ambient temperature of 105°C. Supply voltages = AVDDx = 5 V, DVDD = 2.5 V, ambient temperature<sup>1</sup> (T<sub>A</sub>) = 105°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
<b>DIGITAL-TO-ANALOG CONVERTERS</b>					
Dynamic Range	20 Hz to 20 kHz, –60 dB input	109	113.5		dB
No Filter (RMS)					
With A-Weighted Filter (RMS)		110.5	116		dB
Total Harmonic Distortion + Noise	0 dBFS		–85		dB
	Two channels running –1 dBFS		–92.5		dB
	Eight channels running –1 dBFS		–92.5	–85	dB
Full-Scale Differential Output Voltage			3.00 (±8.49)		V rms (V p-p)
Gain Error		–10		+10	%
Offset Error		–25	–6	+25	mV
Gain Drift		–30		+30	ppm/°C
Interchannel Isolation			100		dB
Interchannel Phase Deviation			0		Degrees
Volume Control Step			0.375		dB
Volume Control Range			95.25		dB
De-emphasis Gain Error				±0.6	dB
Output Resistance at Each Pin			33		Ω
<b>REFERENCE</b>					
Temperature Sensor Reference Voltage	TS_REF pin		1.50		V
Common-Mode Reference Output	CM pin	2.14	2.25	2.29	V
External Reference Voltage Source	CM pin		2.25		V
<b>REGULATOR</b>					
Input Supply Voltage	VSUPPLY pin	3.0	5	5.5	V
Regulated Output Voltage	VSENSE pin	2.25	2.50	2.55	V

<sup>1</sup> Functionally guaranteed at –40°C to +125°C case temperature.

## CRYSTAL OSCILLATOR SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit
Transconductance, T <sub>A</sub> = 25°C	6.4	7 to 10	14	mmhos
Transconductance, T <sub>A</sub> = 105°C	5.2	7.5 to 8.5	12	mmhos

## DIGITAL INPUT/OUTPUT SPECIFICATIONS

–40°C < T<sub>A</sub> < +105°C, IOVDD = 5.0 V and 3.3 V ± 10%.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
High Level Input Voltage (V <sub>IH</sub> )		0.7 × IOVDD			V
Low Level Input Voltage (V <sub>IL</sub> )	IOVDD = 5.0 V			0.3 × IOVDD	V
Input Leakage	I <sub>IH</sub> at V <sub>IH</sub> = 3.3 V			10	μA
	I <sub>IL</sub> at V <sub>IL</sub> = 0 V			10	μA
High Level Output Voltage (V <sub>OH</sub> )	I <sub>OH</sub> = 1 mA	0.8 × IOVDD			V
Low Level Output Voltage (V <sub>OL</sub> )	I <sub>OL</sub> = 1 mA			0.1 × IOVDD	V
Input Capacitance				5	pF

**POWER SUPPLY SPECIFICATIONS**

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
<b>SUPPLIES</b>					
Voltage	AVDD	4.5	5.0	5.5	V
	DVDD	2.25	2.5	3.6	V
	PLLVDD	2.25	2.5	3.6	V
	IOVDD	3.0	5.0	5.5	V
	VSUPPLY	3.0	5.0	5.5	V
Analog Current—AVDD = 5.0 V			84		mA
			1		μA
Digital Current—DVDD = 2.5 V			30		mA
			4		μA
PLL Current—PLLVDD = 2.5 V			5		mA
			1		μA
IO Current—IOVDD = 3.3 V			4		mA
			1		μA
<b>QUIESCENT DISSIPATION—DITHER INPUT</b>					
Operation	MCLK = 256 × f <sub>s</sub> , 48 kHz AVDDx = 5.0 V, DVDD/PLLVDD = 2.5 V, IOVDD = 3.3 V				521
					420
					75
					13
					13
					0
<b>POWER SUPPLY REJECTION RATIO</b>					
Signal at Analog Supply Pins	1 kHz, 200 mV p-p 20 kHz, 200 mV p-p				85
					85

**DIGITAL FILTERS**

Table 6.

Parameter	Mode	Factor	Min	Typ	Max	Unit
<b>DAC INTERPOLATION FILTER</b>						
Pass Band	48 kHz mode, typical at 48 kHz	0.4535 × f <sub>s</sub>		22		kHz
	96 kHz mode, typical at 96 kHz	0.3646 × f <sub>s</sub>	35			kHz
	192 kHz mode, typical at 192 kHz	0.3646 × f <sub>s</sub>		70		kHz
Pass-Band Ripple	48 kHz mode, typical at 48 kHz				±0.01	dB
	96 kHz mode, typical at 96 kHz				±0.05	dB
	192 kHz mode, typical at 192 kHz				±0.1	dB
Transition Band	48 kHz mode, typical at 48 kHz	0.5 × f <sub>s</sub>		24		kHz
	96 kHz mode, typical at 96 kHz	0.5 × f <sub>s</sub>		48		kHz
	192 kHz mode, typical at 192 kHz	0.5 × f <sub>s</sub>		96		kHz
Stop Band	48 kHz mode, typical at 48 kHz	0.5465 × f <sub>s</sub>		26		kHz
	96 kHz mode, typical at 96 kHz	0.6354 × f <sub>s</sub>		61		kHz
	192 kHz mode, typical at 192 kHz	0.6354 × f <sub>s</sub>		122		kHz
Stop-Band Attenuation	48 kHz mode, typical at 48 kHz		68			dB
	96 kHz mode, typical at 96 kHz		68			dB
	192 kHz mode, typical at 192 kHz		68			dB

Parameter	Mode	Factor	Min	Typ	Max	Unit
Propagation Delay	48 kHz mode, typical at 48 kHz	25/f <sub>s</sub>		521		μs
	96 kHz mode, typical at 96 kHz	11/f <sub>s</sub>		115		μs
	192 kHz mode, typical at 192 kHz	8/f <sub>s</sub>		42		μs
	192 kHz low delay mode, typical at 192 kHz	2/f <sub>s</sub>		10		μs

## TIMING SPECIFICATIONS

−40°C < T<sub>A</sub> < +105°C, DVDD = 2.5 V ± 10%.

Table 7.

Parameter	Description	Min	Typ	Max	Unit
<b>INPUT MASTER CLOCK (MCLK) AND RESET</b>					
t <sub>MH</sub>	MCLK duty cycle, DAC clock source = PLL clock at 256 × f <sub>s</sub> , 384 × f <sub>s</sub> , 512 × f <sub>s</sub> , and 768 × f <sub>s</sub>	40		60	%
t <sub>MH</sub>	DAC clock source = direct MCLK at 512 × f <sub>s</sub> (bypass on-chip PLL)	40		60	%
f <sub>MCLK</sub>	MCLKI frequency, PLL mode	6.9		40.5	MHz
f <sub>MCLK</sub>	Direct MCLK 512 × f <sub>s</sub> mode			27.1	MHz
f <sub>BCLK</sub>	DBCLK frequency, PLL mode			27.0	MHz
t <sub>PDR</sub>	Low	15			ns
t <sub>PDRR</sub>	Recovery, reset to active output	300			ms
<b>PLL</b>					
Lock Time	MCLK input			10	ms
Lock Time	DLRCLK input			50	ms
	256 × f <sub>s</sub> VCO Clock, Output Duty Cycle, MCLKO Pin	40		60	%
<b>SPI PORT</b>					
t <sub>CCH</sub>	CCLK high	35			ns
t <sub>CCL</sub>	CCLK low	35			ns
f <sub>CCLK</sub>	CCLK frequency, f <sub>CCLK</sub> = 1/t <sub>CCP</sub> ; only t <sub>CCP</sub> shown in Figure 17			10	MHz
t <sub>CDS</sub>	CDATA setup, time to CCLK rising	10			ns
t <sub>CDH</sub>	CDATA hold, time from CCLK rising	10			ns
t <sub>CLS</sub>	CLATCH setup, time to CCLK rising	10			ns
t <sub>CLH</sub>	CLATCH hold, time from CCLK falling	10			ns
t <sub>CLHIGH</sub>	CLATCH high, not shown in Figure 17	10			ns
t <sub>COE</sub>	COUT enable from CCLK falling			30	ns
t <sub>COD</sub>	COUT delay from CCLK falling			30	ns
t <sub>COH</sub>	COUT hold from CCLK falling, not shown in Figure 17	30			ns
t <sub>COTS</sub>	COUT tristate from CCLK falling			30	ns
<b>I<sup>2</sup>C</b>					
f <sub>SCL</sub>	SCL clock frequency			400	kHz
t <sub>SCLL</sub>	SCL low	1.3			μs
t <sub>SCLH</sub>	SCL high	0.6			μs
t <sub>SCS</sub>	Setup time (start condition), relevant for repeated start condition	0.6			μs
t <sub>SCH</sub>	Hold time (start condition), first clock generated after this period	0.6			μs
t <sub>SSH</sub>	Setup time (stop condition)	0.6			μs
t <sub>DS</sub>	Data setup time	100			ns
t <sub>SR</sub>	SDA and SCL rise time			300	ns
t <sub>SF</sub>	SDA and SCL fall time			300	ns
t <sub>BFT</sub>	Bus-free time between stop and start	1.3			μs

Parameter	Description	Min	Typ	Max	Unit
DAC SERIAL PORT					
$t_{DBH}$	DBCLK high, slave mode	10			ns
$t_{DBL}$	DBCLK low, slave mode	10			ns
$t_{DLS}$	DLRCLK setup, time to DBCLK rising, slave mode	10			ns
$t_{DLH}$	DLRCLK hold from DBCLK rising, slave mode	5			ns
$t_{DLS}$	DLRCLK skew from DBCLK falling, master mode	-8		+8	ns
$t_{DDS}$	DSDATAx setup to DBCLK rising	10			ns
$t_{DDH}$	DSDATAx hold from DBCLK rising	5			ns

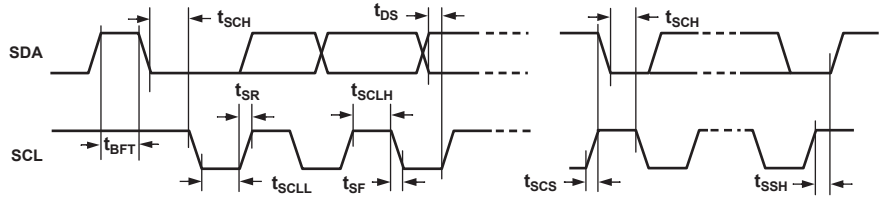


Figure 2. I2C Timing Diagram

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## ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
Analog (AVDD)	−0.3 V to +5.5 V
Input/Output (IOVDD)	−0.3 V to +5.5 V
Digital (DVDD)	−0.3 V to +3.6 V
PLL (PLLVD)	−0.3 V to +3.6 V
VSUPPLY	−0.3 V to +6.0 V
Input Current (Except Supply Pins)	±20 mA
Analog Input Voltage (Signal Pins)	−0.3 V to AVDD + 0.3 V
Digital Input Voltage (Signal Pins)	−0.3 V to IOVDD + 0.3 V
Operating Temperature Range (Case)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  represents junction-to-ambient thermal resistance;  $\theta_{JC}$  represents the junction-to-case thermal resistance. All characteristics are for a 4-layer board with a solid ground plane.

Table 9. Thermal Resistance

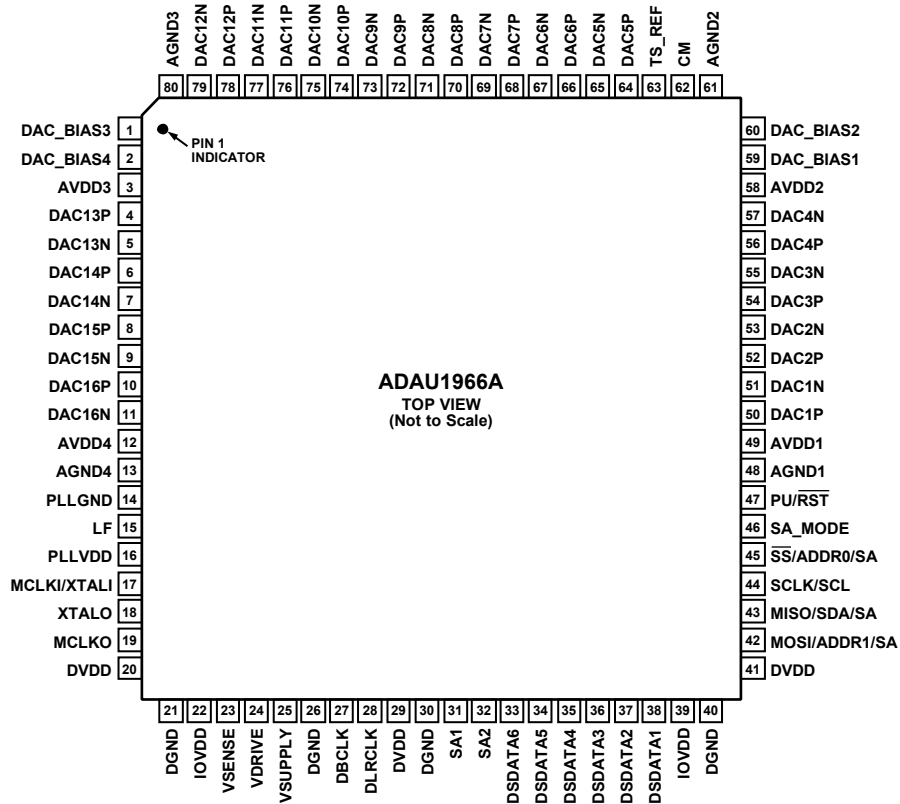
Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
80-Lead LQFP	42.3	10.0	°C/W

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

### PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES  
 1. SEE THE STANDALONE MODE SECTION (TABLE 13 AND TABLE 14) FOR THE SA\_MODE SETTINGS FOR PIN 31, PIN 32, PIN 42, PIN 43, AND PIN 45.

Figure 3. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Type <sup>1</sup>	Mnemonic	Description
1	I	DAC_BIAS3	DAC Bias 3. AC couple with 470 nF to AGND3.
2	I	DAC_BIAS4	DAC Bias 4. AC couple with 470 nF to AVDD3.
3	PWR	AVDD3	Analog Power.
4	O	DAC13P	DAC13 Positive Output.
5	O	DAC13N	DAC13 Negative Output.
6	O	DAC14P	DAC14 Positive Output.
7	O	DAC14N	DAC14 Negative Output.
8	O	DAC15P	DAC15 Positive Output.
9	O	DAC15N	DAC15 Negative Output.
10	O	DAC16P	DAC16 Positive Output.
11	O	DAC16N	DAC16 Negative Output.
12	PWR	AVDD4	Analog Power.
13	GND	AGND4	Analog Ground.
14	GND	PLLGND	PLL Ground.
15	O	LF	PLL Loop Filter, Reference to PLLVDD.
16	PWR	PLLVDD	Apply 2.5 V to Power PLL.
17	I	MCLKI/XTALI	Master Clock Input, Input to Crystal Inverter.
18	O	XTALO	Output from Crystal Inverter.
19	O	MCLKO	Master Clock Output.

Pin No.	Type <sup>1</sup>	Mnemonic	Description
20, 29, 41	PWR	DVDD	Digital Power, 2.5 V.
21, 26, 30, 40	GND	DGND	Digital Ground.
22, 39	PWR	IOVDD	Power for Digital Input and Output Pins, 3.3 V to 5 V.
23	I	VSENSE	2.5 V Output of Regulator, Collector of Pass Transistor. Bypass with 10 $\mu$ F in parallel with 100 nF.
24	O	VDRIVE	Drive for Base of Pass Transistor.
25	I	VSUPPLY	5 V Input to Voltage Regulator, Emitter of Pass Transistor. Bypass with 10 $\mu$ F in parallel with 100 nF.
27	I/O	DBCLK	Bit Clock for DACs.
28	I/O	DLRCLK	Frame Clock for DACs.
31	I	DSDATA8/SA	DAC15 and DAC 16 Serial Data Input/SA_MODE TDM State (see the Standalone Mode section, Table 13, and Table 14).
32	I	DSDATA7/SA	DAC13 and DAC 14 Serial Data Input/SA_MODE TDM State (see the Standalone Mode section, Table 13, and Table 14).
33	I	DSDATA6	DAC11 and DAC 12 Serial Data Input.
34	I	DSDATA5	DAC9 and DAC 10 Serial Data Input.
35	I	DSDATA4	DAC7 and DAC 8 Serial Data Input.
36	I	DSDATA3	DAC5 and DAC 6 Serial Data Input.
37	I	DSDATA2	DAC3 and DAC 4 Serial Data Input.
38	I	DSDATA1	DAC1 and DAC 2 Serial Data Input.
42	I	CDATA/ADDR1/SA	Control Data Input (SPI)/Address 1 (I <sup>2</sup> C)/SA_MODE State (see the Standalone Mode section and Table 13).
43	I/O	COUT/SDA/SA	Control Data Output (SPI)/Control Data Input (I <sup>2</sup> C)/SA_MODE State (see the Standalone Mode section and Table 13).
44	I	CCLK/SCL/SA	Control Clock Input (SPI)/Control Clock Input (I <sup>2</sup> C)/SA_MODE State (see the Standalone Mode section and Table 13).
45	I	CLATCH/ADDR0/SA	Control Chip Select (SPI) (Low Active)/Address 0 (I <sup>2</sup> C)/SA_MODE State (see the Standalone Mode section and Table 13).
46	I	SA_MODE	Standalone Mode. This pin allows mode control of <a href="#">ADAU1966</a> using Pin 42 to Pin 45, Pin 31, and Pin 32 (high active, see Table 13 and Table 14).
47	I	PU/ $\overline{\text{RST}}$	Power-Up/Reset (Low Active).
48	GND	AGND1	Analog Ground.
49	PWR	AVDD1	Analog Power.
50	O	DAC1P	DAC1 Positive Output.
51	O	DAC1N	DAC1 Negative Output.
52	O	DAC2P	DAC2 Positive Output.
53	O	DAC2N	DAC2 Negative Output.
54	O	DAC3P	DAC3 Positive Output.
55	O	DAC3N	DAC3 Negative Output.
56	O	DAC4P	DAC4 Positive Output.
57	O	DAC4N	DAC4 Negative Output.
58	PWR	AVDD2	Analog Power.
59	I	DAC_BIAS1	DAC Bias 1. AC couple with 470 nF to AVDD2.
60	I	DAC_BIAS2	DAC Bias 2. AC couple with 470 nF to AGND2.
61	GND	AGND2	Analog Ground.
62	O	CM	Common-Mode Reference Filter Capacitor Connection. Bypass with 10 $\mu$ F in parallel with 100 nF to AGND2. This reference can be shut off in the PLL_CLK_CTRL1 register and the pin can be driven with an outside voltage source.
63	O	TS_REF	Voltage Reference Filter Capacitor Connection. Bypass with 10 $\mu$ F in parallel with 100 nF to AGND2.
64	O	DAC5P	DAC5 Positive Output.
65	O	DAC5N	DAC5 Negative Output.
66	O	DAC6P	DAC6 Positive Output.
67	O	DAC6N	DAC6 Negative Output.

<b>Pin No.</b>	<b>Type<sup>1</sup></b>	<b>Mnemonic</b>	<b>Description</b>
68	O	DAC7P	DAC7 Positive Output.
69	O	DAC7N	DAC7 Negative Output.
70	O	DAC8P	DAC8 Positive Output.
71	O	DAC8N	DAC8 Negative Output.
72	O	DAC9P	DAC9 Positive Output.
73	O	DAC9N	DAC9 Negative Output.
74	O	DAC10P	DAC10 Positive Output.
75	O	DAC10N	DAC10 Negative Output.
76	O	DAC11P	DAC11 Positive Output.
77	O	DAC11N	DAC11 Negative Output.
78	O	DAC12P	DAC12 Positive Output.
79	O	DAC12N	DAC12 Negative Output.
80	GND	AGND3	Analog Ground.

<sup>1</sup> I = input, O = output, I/O = input/output, PWR = power, GND = ground.

### TYPICAL PERFORMANCE CHARACTERISTICS

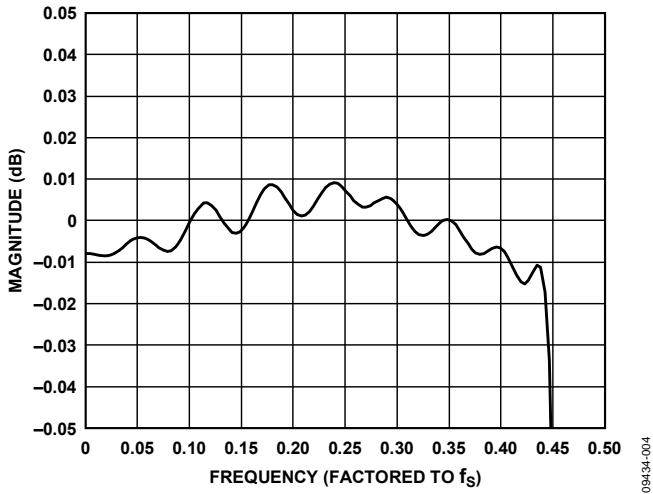


Figure 4. DAC Pass-Band Filter Response, 48 kHz

09434-004

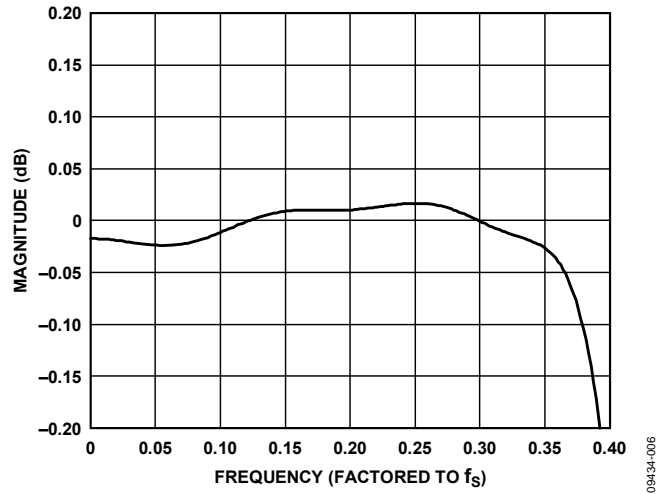


Figure 6. DAC Pass-Band Filter Response, 96 kHz

09434-006

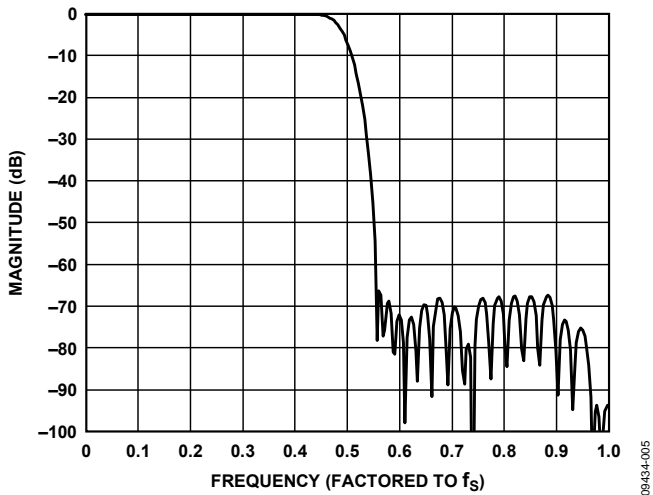


Figure 5. DAC Stop-Band Filter Response, 48 kHz

09434-005

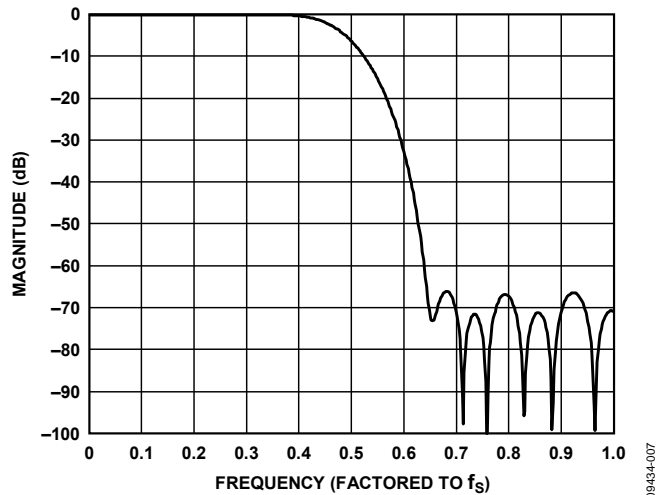


Figure 7. DAC Stop-Band Filter Response, 96 kHz

09434-007

# APPLICATION CIRCUITS

Typical application circuits are shown in Figure 8 to Figure 11. Recommended loop filters for DLRCLK and MCLKI/XTALI modes of the PLL reference are shown in Figure 8. Output filters for the DAC outputs are shown in Figure 9 and Figure 10, and an external regulator circuit is shown in Figure 11.

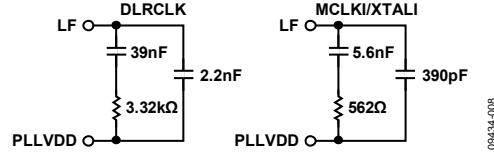


Figure 8. Recommended Loop Filters for DLRCLK or MCLKI/XTALI PLL Reference Modes

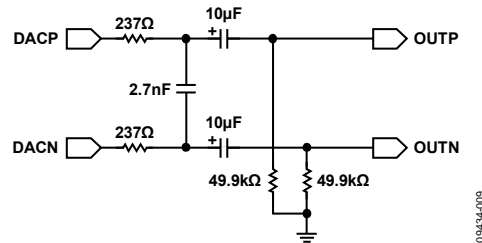


Figure 9. Typical DAC Output Passive Filter Circuit (Differential)

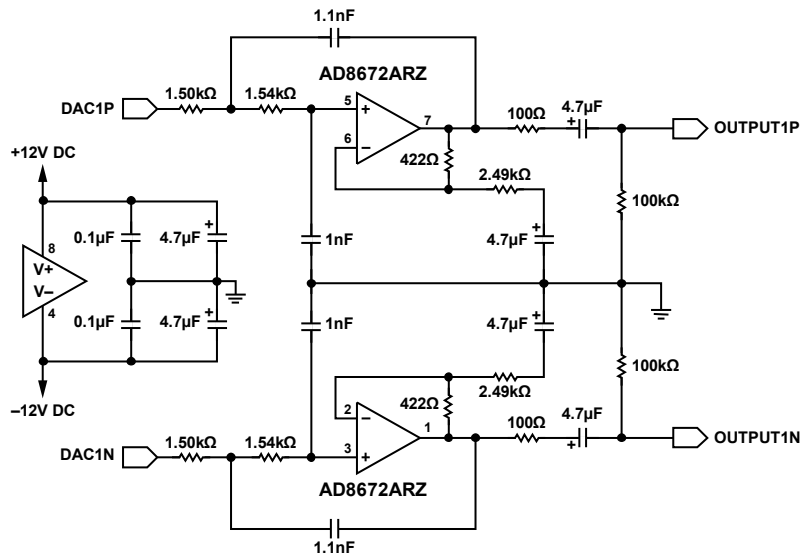


Figure 10. Typical DAC Output Active Filter Circuit (Differential)

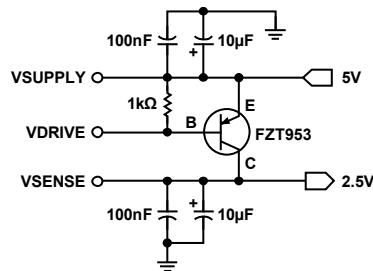


Figure 11. Recommended 2.5 V Regulator Circuit

## THEORY OF OPERATION

### DIGITAL-TO-ANALOG CONVERTERS (DACs)

The 16 ADAU1966 digital-to-analog converter (DAC) channels are differential for improved noise and distortion performance and are voltage output for simplified connection. The DACs include on-chip digital interpolation filters with 68 dB stop-band attenuation and linear phase response, operating at an over-sampling ratio of 256× (48 kHz range), 128× (96 kHz range), or 64× (192 kHz range). Each channel has its own independently programmable attenuator, adjustable in 255 steps in increments of 0.375 dB. Digital inputs are supplied through eight serial data input pins (two channels on each pin), a common frame clock (DLRCLK), and a bit clock (DBCLK). Alternatively, any one of the TDM modes can be used to access up to 16 channels on a single TDM data line.

The ADAU1966 has a low propagation delay mode; this mode is an option for an fS of 192 kHz and is enabled in Register DAC\_CTRL0[2:1]. By setting these bits to b11, the propagation delay is reduced by the amount shown in Table 6. The shorter delay is achieved by reducing the amount of digital filtering; the negative impact of selecting this mode is reduced audio frequency response and increased out-of-band energy.

When AVDD is supplied with 5 V, each analog output pin has a nominal common-mode (CM) dc level of 2.25 V and swings ±2.12 V above and below the 2.25 V for a 1.5 V rms signal on each pin. Differentially, the signal is 3 V rms, 8.48 V p-p, from a 0 dBFS digital input signal.

The differential analog outputs require only a single-order passive differential RC filter to provide the specified DNR performance; see Figure 9 for an example filter. The outputs can easily drive differential inputs on a separate PCB through cabling as well as differential inputs on the same PCB.

If more signal level is required or if a more robust filter is needed, a single op amp gain stage designed as a second-order, low-pass Bessel filter can be used to remove the high frequency out-of-band noise present on each pin of the differential outputs. The choice of components and design of this circuit is critical to yield the full DNR of the DACs (see the recommended passive and active circuits in Figure 9 and Figure 10). This filter can be built into an active difference amplifier to provide a single-ended output with gain, if necessary. Note that the use of op amps with low slew rate or low bandwidth can cause high frequency noise and tones to fold down into the audio band; exercise care when selecting these components.

The ADAU1966 offers control over the analog performance of the DACs; it is possible to program the registers to reduce the power consumption with the trade-off of lower SNR and THD + N. The reduced power consumption is the result of changing the internal bias current to the analog output amplifiers.

Register DAC\_POWER1 to Register DAC\_POWER4 present four basic settings for the DAC power vs. performance in each of the 16 channels: best performance, good performance, low power, and lowest power. Alternatively, in Register PLL\_CLK\_CTRL1[7:6], the LOPWR\_MODE bits offer global control over the power and performance for all 16 channels. The default setting is b00. This setting allows the channels to be controlled individually using the DAC\_POWERx registers. Setting b10 and Setting b11 select the low power and lowest power settings. The data presented in Table 11 shows the result of setting all 16 channels to each of the four settings. The SNR and THD + N specifications are shown in relation to the measured performance of a device at the best performance setting.

The voltage at CM, the common-mode reference pin, can be used to bias the external op amps that buffer the output signals (see the Power Supply and Voltage Reference section).

### CLOCK SIGNALS

Upon powering the ADAU1966 and asserting the PU/RST pin high, the device starts in either standalone mode (SA\_MODE) or program mode, depending on the state of SA\_MODE (Pin 46). The clock functionality of SA\_MODE is described in the Standalone Mode section. In program mode, the default for the ADAU1966 is for the MCLKO pin to feed a buffered output of the MCLKI signal. The default for the DLRCLK and DBCLK ports is slave mode; the DAC must be driven with a coherent set of MCLK, LRCLK, and BCLK signals to function.

The MCLKO pin can be programmed to provide different clock signals using Register Bits PLL\_CLK\_CTRL1[5:4]. The default, b10, provides a buffered copy of the clock signal that is driving the MCLKI pin. Two modes, b00 and b01, provide low jitter clock signals. The b00 setting yields a clock rate between 4 MHz and 6 MHz, and b01 yields a clock rate between 8 MHz and 12 MHz. Both of these clock frequencies are scaled as ratios of MCLK automatically inside the ADAU1966. As an example, an MCLK of 8.192 MHz and a setting of b00 yield an MCLKO of  $(8.192/2) = 4.096$  MHz. Alternatively, an MCLK of 36.864 MHz and a setting of b01 yield an MCLKO frequency of  $(36.864/3) = 12.288$  MHz. The setting b11 shuts off the MCLKO pin.

Table 11. DAC Power vs. Performance

Register Setting	Best Performance	Good Performance	Low Power	Lowest Power
Total AVDD Current	84 mA	75 mA	66 mA	56 mA
SNR	Reference	-0.2 dB	-1.5 dB	-14.2 dB
THD + N (-1 dBFS signal)	Reference	-1.8 dB	-3.0 dB	-5.8 dB

After the  $\overline{\text{PU/RST}}$  pin has been asserted high, the PLL\_CLK\_CTRLx registers (Register 0x00 and Register 0x01) can be programmed. The on-chip phase-locked loop (PLL) can be selected to use the clock appearing at the MCLKI/XTALI pin at a frequency of 256, 384, 512, or 768 times the sample rate ( $f_s$ ), referenced to the 48 kHz mode from the master clock select (MCS) setting, as described in Table 12. In 96 kHz mode, the master clock frequency stays at the same absolute frequency; therefore, the actual multiplication rate is divided by 2. In 192 kHz mode, the actual multiplication rate is divided by 4. For example, if the ADAU1966 is programmed in  $256 \times f_s$  mode, the frequency of the master clock input is  $256 \times 48 \text{ kHz} = 12.288 \text{ MHz}$ . If the ADAU1966 is then switched to 96 kHz operation (by writing to DAC\_CTRL0 [2:1]), the frequency of the master clock remains at 12.288 MHz, which is  $128 \times f_s$  in this example. In 192 kHz mode, MCS becomes  $64 \times f_s$ .

The internal clock for the digital core varies by mode:  $512 \times f_s$  (48 kHz mode),  $256 \times f_s$  (96 kHz mode), or  $128 \times f_s$  (192 kHz mode). By default, the on-board PLL generates this internal master clock from an external clock.

The PLL must be powered and stable before the ADAU1966 is used as a source for quality audio. The PLL is enabled by reset and does not require writing to the I<sup>2</sup>C or SPI port for normal operation.

With the PLL enabled, the performance of the ADAU1966 is not affected by jitter as high as a 300 ps rms time interval error (TIE). If the internal PLL is not used, it is best to use an independent crystal oscillator to generate the master clock.

If the ADAU1966 is to be used in direct MCLK mode, the PLL can be powered down in the PDN\_THRMSSENS\_CTRL\_1 register. For direct MCLK mode, a  $512 \times f_s$  (referenced to 48 kHz mode) master clock must be used as MCLK, and the CLK\_SEL bit in the PLL\_CLK\_CTRL1 register must be set to b1.

The ADAU1966 PLL can also be programmed to run from an external LRCLK. When the PLLIN bits in the PLL\_CLK\_CTRL0 register are set to 01 and the appropriate loop filter is connected to the LF pin (see Figure 8), the ADAU1966 PLL generates all of the necessary internal clocks for operation with no external MCLK. This mode reduces the number of high frequency signals in the design, reducing EMI emissions.

It is possible to further reduce EMI emissions of the circuit by using the internal DBCLK generation setting of the BCLK\_GEN

bit in the DAC\_CTRL1 register. With the BCLK\_GEN bit set to b1 (internal) and the SAI\_MS bit set to b0 (slave), the ADAU1966 generate its own DBCLK; this works with the PLL input set to either MCLKI/XTALI or DLRCLK. DLRCLK is the only required clock in DLRCLK PLL mode.

## POWER-UP AND RST

Power sequencing for the ADAU1966 starts with AVDD and IOVDD, followed by DVDD. It is very important that AVDD be settled at a regulated voltage and that IOVDD be within 10% of regulated voltage before applying DVDD. When using the ADAU1966 internal regulator, this timing occurs by default.

To guarantee proper startup, the  $\overline{\text{PU/RST}}$  pin must be pulled low by an external resistor and then driven high after the power supplies stabilize. The  $\overline{\text{PU/RST}}$  can also be pulled high using a simple RC network.

Driving the  $\overline{\text{PU/RST}}$  pin low puts the device into a very low power state ( $<3 \mu\text{A}$ ). All functionality of the ADAU1966 is disabled until the  $\overline{\text{PU/RST}}$  pin is asserted high. Once this pin is asserted high, the ADAU1966 requires 300 ms to stabilize. The MMUTE bit in the DAC\_CTRL0 register must be toggled for operation.

The PUP bit in the PLL\_CLK\_CTRL0 register can be used to power down the ADAU1966. Engaging the master power-down puts the ADAU1966 in an idle state while maintaining the settings of all registers. Additionally, the power-down bits in the PDN\_THRMSSENS\_CTRL1 register (TS\_PDN, PLL\_PDN, and VREG\_PDN) can be used to power down individual sections of the ADAU1966.

The SOFT\_RST bit in the PLL\_CLK\_CTRL0 register sets all of the control registers to their default settings while maintaining the internal clocks in default mode. The SOFT\_RST bit does not power down the analog outputs; toggling this bit does not cause audible popping sounds at the differential analog outputs.

Proper startup of the ADAU1966 proceeds as follows:

1. Apply power to the ADAU1966 as described previously.
2. Assert the  $\overline{\text{PU/RST}}$  pin high after power supplies have stabilized.
3. Set the PUP bit to b1.
4. Program all necessary registers for the desired settings.
5. Set the MMUTE bit to b0 to unmute all channels.



Table 12. MCS and  $f_s$  Modes

Sample Rate Select (FS) DAC_CTRL0[2:1]	Master Clock Select (MCS), PLL_CLK_CTRL0[2:1]							
	Setting 0, b00		Setting 1, b01		Setting 2, b10		Setting 3, b11	
	Ratio	MCLK (MHz)	Ratio	MCLK	Ratio	MCLK	Ratio	MCLK
32 kHz, b00	$256 \times f_s$	8.192	$384 \times f_s$	12.288	$512 \times f_s$	16.384	$768 \times f_s$	24.576
44.1 kHz, b00	$256 \times f_s$	11.2896	$384 \times f_s$	16.9344	$512 \times f_s$	22.5792	$768 \times f_s$	33.8688
48 kHz, b00	$256 \times f_s$	12.288	$384 \times f_s$	18.432	$512 \times f_s$	24.576	$768 \times f_s$	36.864
64 kHz, b01	$128 \times f_s$	8.192	$192 \times f_s$	12.288	$256 \times f_s$	16.384	$384 \times f_s$	24.576
88.2 kHz, b01	$128 \times f_s$	11.2896	$192 \times f_s$	16.9344	$256 \times f_s$	22.5792	$384 \times f_s$	33.8688
96 kHz, b01	$128 \times f_s$	12.288	$192 \times f_s$	18.432	$256 \times f_s$	24.576	$384 \times f_s$	36.864
128 kHz, b10 or b11	$64 \times f_s$	8.192	$96 \times f_s$	12.288	$128 \times f_s$	16.384	$192 \times f_s$	24.576
176.4 kHz, b10 or b11	$64 \times f_s$	11.2896	$96 \times f_s$	16.9344	$128 \times f_s$	22.5792	$192 \times f_s$	33.8688
192 kHz, b10 or b11	$64 \times f_s$	12.288	$96 \times f_s$	18.432	$128 \times f_s$	24.576	$192 \times f_s$	36.864

## STANDALONE MODE

The ADAU1966 can operate without a typical I<sup>2</sup>C or SPI connection to a microcontroller. This standalone mode is made available by setting the SA\_MODE (Pin 46) to high (IOVDD). All registers are set to default except the options shown in Table 13.

Table 13. SA\_MODE Settings

Pin No.	Setting	Function
42	0	Master mode serial audio interface (SAI)
	1	Slave mode SAI
43	0	MCLK = $256 \times f_s$ , PLL on
	1	MCLK = $384 \times f_s$ , PLL on
44	0	Must be set to 0
45	0	I <sup>2</sup> S SAI format
	1	TDM modes, determined by Pin 31 and Pin 32

When both SA\_MODE and Pin 45 are set high, TDM mode is selected. Table 14 shows the available TDM modes; these modes are set by connecting Pin 31 (DSDATA8) and Pin 32 (DSDATA7) to GND or IOVDD.

Table 14. TDM Modes

Pin No.	Setting	Function
32:31	00	TDM4—DLRCLK pulse
	01	TDM8—DLRCLK pulse
	10	TDM16—DLRCLK pulse
	11	TDM8—DLRCLK 50% duty cycle

When the ADAU1966 is powered up in SA\_MODE and the PU/RST pin is asserted high, the MCLKO pin provides a buffered version of the MCLKI pin, whether the source is a crystal or an active oscillator.

## I<sup>2</sup>C CONTROL PORT

The ADAU1966 has an I<sup>2</sup>C-compatible control port that permits programming and reading back of the internal control registers for the DACs and clock system. The I<sup>2</sup>C interface of the ADAU1966 is a 2-wire interface consisting of a clock line, SCL, and a data line, SDA. SDA is bidirectional, and the ADAU1966 drives SDA

either to acknowledge the master (ACK) or to send data during a read operation. The SDA pin for the I<sup>2</sup>C port is an open-drain collector and requires a 2 k $\Omega$  pull-up resistor. A write or read access occurs when the SDA line is pulled low while the SCL line is high, indicated by a start in Figure 12 and Figure 13. SDA is only allowed to change when SCL is low except when a start or stop condition occurs, as shown in Figure 12 and Figure 13. The first eight bits of the data-word consist of the device address and the R/W bit. The device address consists of an internal built-in address (0x04) and two address pins, ADDR1 and ADDR0. The two address bits allow four ADAU1966 devices to be used in a system. Initiating a write operation to the ADAU1966 involves sending a start condition and then sending the device address with the R/W bit set low. The ADAU1966 responds by issuing an acknowledge to indicate that it has been addressed. The user then sends a second frame telling the ADAU1966 which register is required to be written. Another acknowledge is issued by the ADAU1966. Finally, the user can send another frame with the eight data bits required to be written to the register. A third acknowledge is issued by the ADAU1966 after which the user can send a stop condition to complete the data transfer.

A read operation requires that the user first write to the ADAU1966 to point to the correct register and then read the data. This is achieved by sending a start condition followed by the device address frame, with the R/W bit low, and then the register address frame. Following the acknowledge from the ADAU1966, the user must issue a repeated start condition. The next frame is the device address with the R/W bit set high. On the next frame, the ADAU1966 outputs the register data on the SDA line. A stop condition completes the read operation.

Table 15. I<sup>2</sup>C Addresses

ADDR1	ADDR0	Slave Address
0	0	0x04
0	1	0x24
1	0	0x44
1	1	0x64

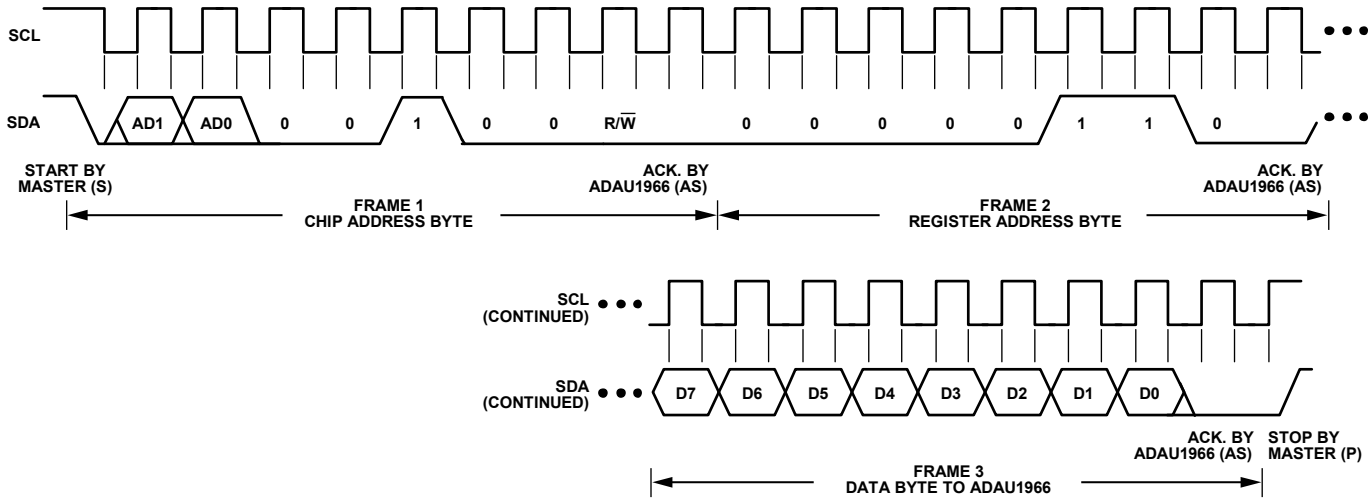


Figure 12. I<sup>2</sup>C Write Format

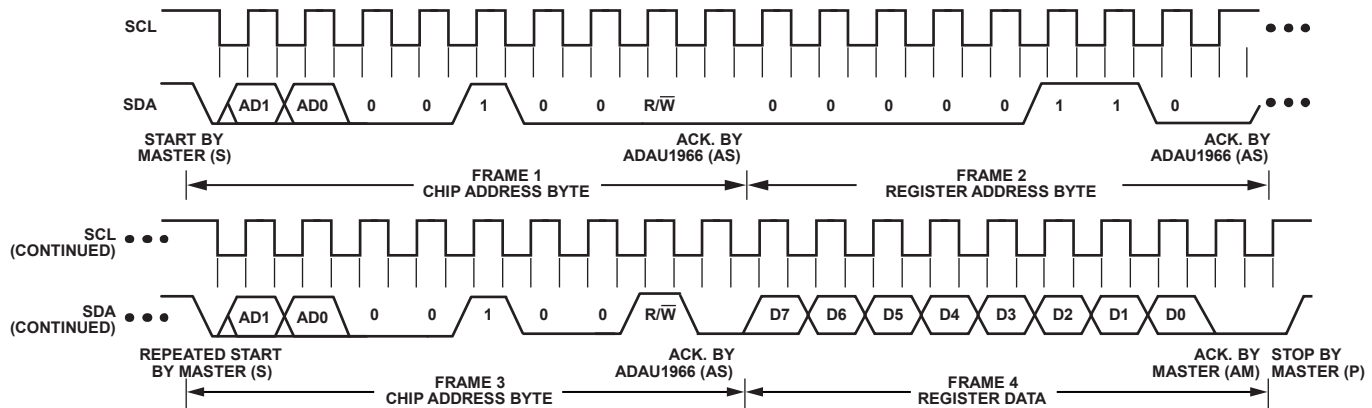


Figure 13. I<sup>2</sup>C Read Format

Table 16. I<sup>2</sup>C Abbreviations

Abbreviation	Condition
S	Start bit
P	Stop bit
AM	Acknowledge by master
AS	Acknowledge by slave

Table 17. Single Word I<sup>2</sup>C Write

S	Chip Address, R/W = 0	AS	Register Address	AS	Data-Word	AS	P
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Table 18. Burst Mode I<sup>2</sup>C Write

S	Chip Address, R/W = 0	AS	Register Address	AS	Data-Word 1	AS	Data-Word 2	AS	Data-Word N	AS	P
---	-----------------------	----	------------------	----	-------------	----	-------------	----	-------------	----	---

Table 19. Single Word I<sup>2</sup>C Read

S	Chip Address, R/W = 0	AS	Register Address	AS	S	Chip Address, R/W = 1	AS	Data-Word	AM	P
---	-----------------------	----	------------------	----	---	-----------------------	----	-----------	----	---

Table 20. Burst Mode I<sup>2</sup>C Read

S	Chip Address, R/W = 0	AS	Register Address	AS	S	Chip Address, R/W = 1	AS	Data-Word 1	AM	Data-Word 2	AM	Data-Word N	AM	P
---	-----------------------	----	------------------	----	---	-----------------------	----	-------------	----	-------------	----	-------------	----	---

**SERIAL CONTROL PORT: SPI CONTROL MODE**

The ADAU1966 has an SPI control port that permits programming and readback of the internal control registers for the DACs and clock system. A standalone mode is also available for operation without serial control; it is configured at reset using the SA\_MODE pin. See the Standalone Mode section for details about SA\_MODE.

By default, the ADAU1966 is in I<sup>2</sup>C mode; however, SPI control mode can be entered by pulling CLATCH low three times. To enter SPI control mode, perform three dummy writes to the SPI port (the ADAU1966 does not acknowledge these three writes). Beginning with the fourth SPI write, data can be written to or read from the IC. The ADAU1966 can exit SPI control mode only by a full reset initiated by power cycling the device.

The SPI control port of the ADAU1966 is a 4-wire serial control port. The format is a 24-bit wide data-word. The serial bit clock and latch can be completely asynchronous to the sample rate of the DACs. Table 21 shows the format of the SPI address byte. The first byte is the global address with a read/write bit. For the ADAU1966, the address is Address 0x06, shifted left one bit due to the R/W bit. The second byte is the ADAU1966 register address, and the third byte is the data, as shown in Figure 15 and Figure 16.

**Table 21. SPI Address and R/W Byte Format**

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	0	0	0	1	1	0	R/W

When reading data from the ADAU1966, the COUT pin is tristated until the third byte, at which point it drives the data out (see Figure 16). The COUT pin is tristated at all other times, allowing the pin to be bussed with other devices, see Figure 17 for the timing requirements.

**Chip Address R/W**

The LSB of the first byte of a SPI transaction is an R/W bit. This bit determines whether the communication is a read (Logic Level 1) or a write (Logic Level 0); see Table 21 for this format.

**SPI Burst Read/Write**

The SPI port is capable of performing burst reads or writes. This is accomplished by sending the chip address byte with the R/W bit, followed by the first register address that needs to be read or written to. Then, as long as the CLATCH pin is held low, registers can be sequentially read or written by continuing to send out clock pulses into the CCLK pin. A very efficient procedure to initialize the ADAU1966 is accomplished by

1. Sending out the address byte with the R/W bit low (write).
2. Sending out the address of the first register.
3. Sending out all the register byte values.
4. Toggling the CLATCH pin.
5. Performing a burst read to verify the register writes.

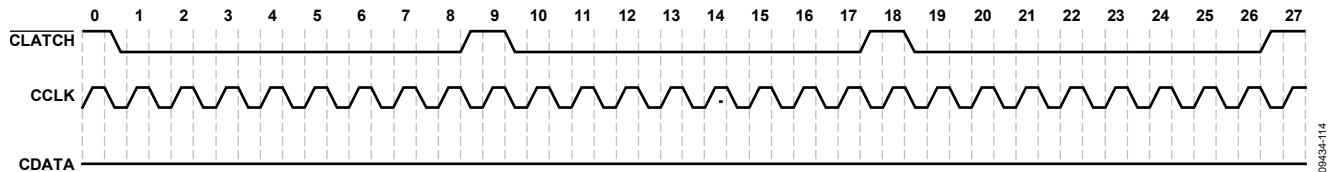


Figure 14. SPI Mode Initial Sequence

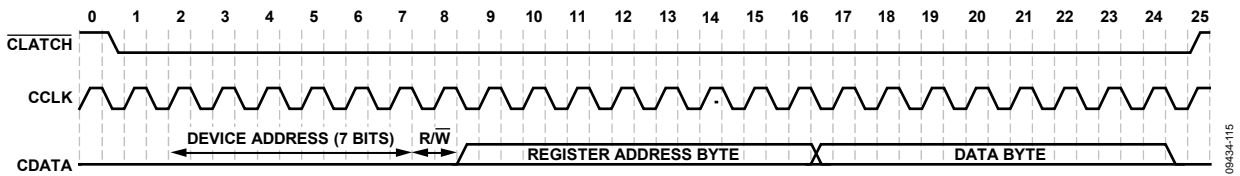


Figure 15. SPI Write to ADAU1966 Clcking

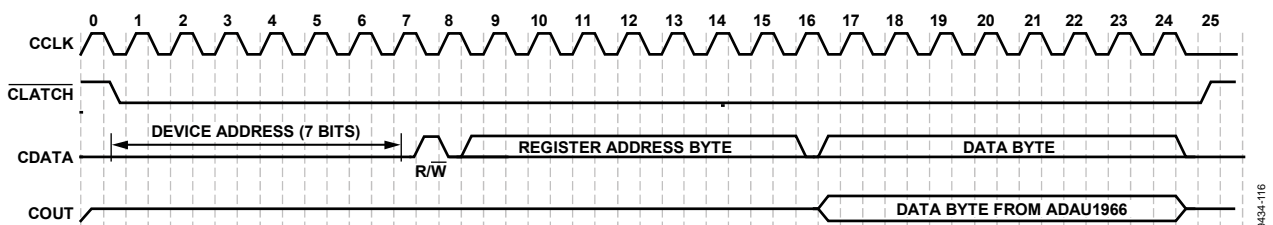


Figure 16. SPI Read from the ADAU1966 Clcking

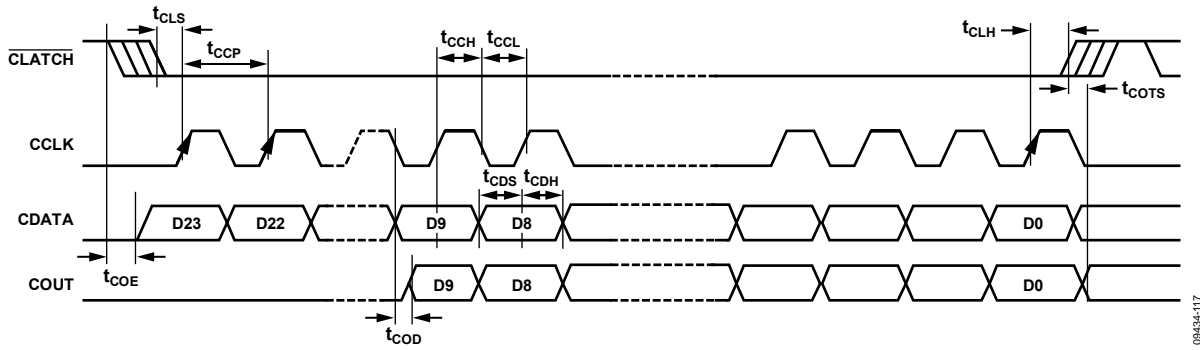


Figure 17. Format of the SPI Signal

**POWER SUPPLY AND VOLTAGE REFERENCE**

The ADAU1966 is designed for 5 V analog and 2.5 V digital supplies. To minimize noise pickup, bypass the power supply pins with 100 nF ceramic chip capacitors placed as close to the pins as possible. Also, provide a bulk aluminum electrolytic capacitor of at least 22 μF for each rail on the same PC board as the codec. It is important that the analog supply be as clean as possible.

The ADAU1966 includes a 2.5 V regulator driver that requires only an external pass transistor and bypass capacitors to make a 2.5 V regulator from a 5 V supply. The VSUPPLY and VSENSE pins must be decoupled with no more than 10 μF, in parallel with 100 nF high frequency bypassing. If the regulator driver is not used, connect VSUPPLY and VDRIVE to GND and leave VSENSE unconnected.

All digital inputs are compatible with TTL and CMOS levels. All outputs are driven from the 3.3 V or 5 V IOVDD supply and are compatible with TTL and 3.3 V CMOS levels.

The temperature sensor internal voltage reference ( $V_{TS\_REF}$ ) is brought out on the TS\_REF pin and must be bypassed as close as possible to the chip with a parallel combination of 10 μF and 100 nF.

The internal band gap reference can be disabled in the PLL\_CLK\_CTRL1 register by setting VREF\_EN to 0; the CM pin can be then be driven from an external source. This can be used to scale the DAC output to the clipping level of a power amplifier based on its power supply voltage.

The CM pin is the internal common-mode reference. It must be bypassed as close as possible to the chip, with a parallel combination of 10 μF and 100 nF. This voltage can be used to bias external op amps to the common-mode voltage of the analog input and output signal pins. It is recommended that the CM pin be isolated from the external circuitry by using a high quality buffer to provide a quiet, low impedance source for the external circuitry. Use of a quiet op amp is critical, because any noise added to the reference voltage is injected into the signal path.

**SERIAL DATA PORTS—DATA FORMAT**

The 16 DAC channels use a common serial bit clock (DBCLK) and a common left-right framing clock (DLRCLK) in the serial data port. The clock signals are all synchronous with the sample rate. The normal stereo serial modes are shown in Figure 18.

The DAC serial data mode defaults to I<sup>2</sup>S (1 BCLK delay) upon power-up and reset. The ports can also be programmed for left-justified and right-justified (24-bit and 16-bit) operation using DAC\_CTRL0[7:6]. Stereo and TDM modes can be selected using DAC\_CTRL0[5:3]. The polarity of the DLRCLK pin is programmable according to the DAC\_CTRL1[5] bit, allowing for easy channel swapping.

The DBCLK pin can latch on the rising or falling edge of the clock signal. DAC\_CTRL1[1] selects the active edge.

The serial ports are programmable as the clock masters according to the DAC\_CTRL1[0] bit. By default, the serial port is in slave mode.

**TIME-DIVISION MULTIPLEXED (TDM) MODES**

The ADAU1966 serial ports also have several different TDM serial data modes. The ADAU1966 can support a single data line TDM16, a dual data line (TDM8), a quad data line (TDM4), or eight data lines (TDM2). The DLRCLK can be operated in both single-cycle pulse mode and a 50% duty cycle mode. Both 16 DBCLKs or 32 DBCLKs per channel are selectable for each mode.

The I/O pins of the serial ports are defined according to the serial mode that is selected. For a detailed description of the function of each pin in TDM and stereo modes, see Table 22.

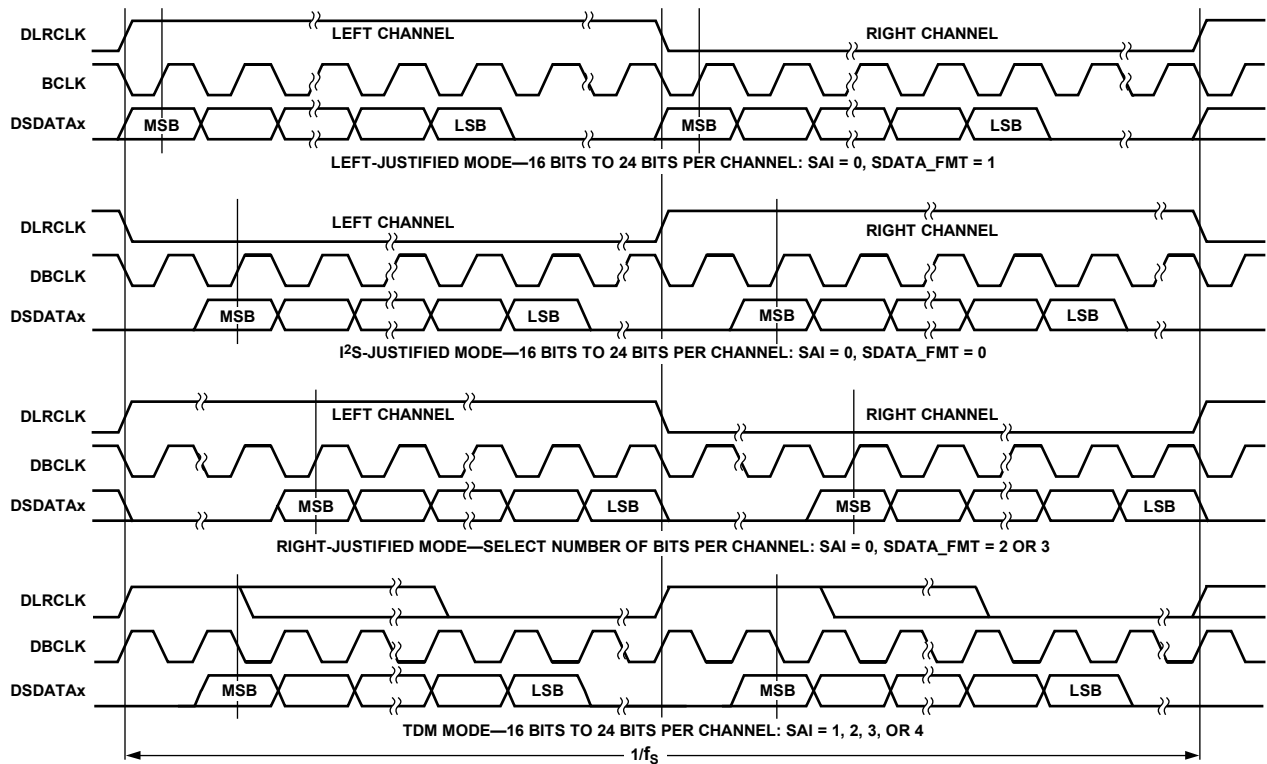
**TEMPERATURE SENSOR**

The ADAU1966 has an on-board temperature sensor that allows the user to read the temperature of the silicon inside the device. The temperature sensor readout has a range of -60°C to +140°C in 1°C steps. The PDN\_THRMSSENS\_CTRL\_1 register controls the settings of the sensor. The temperature sensor is powered on by default and can be shut off by setting the TS\_PDN[2] bit to b1 in PDN\_THRMSSENS\_CTRL\_1. The temperature sensor can be run in either continuous operation or one-shot mode. The temperature sensor conversion mode is modified using Bit 5, THRM\_MODE; the default is THRM\_MODE = 1, one-shot

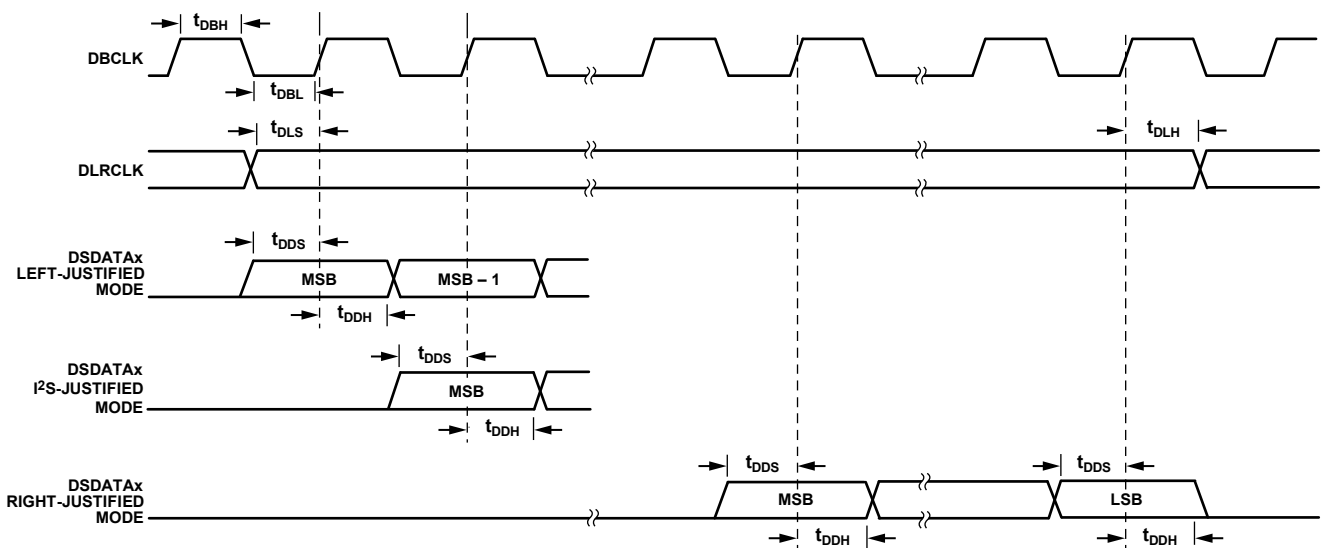
mode. In one-shot mode, writing a 0 followed by writing a 1 to Bit 4, THRM\_GO, results in a single reset and temperature conversion, placing the resulting temperature data in the THRM\_TEMP\_STAT register. In continuous operation mode, the data conversion takes place at a rate set by Bits[7:6], THRM\_RATE, with a range of 0.5 sec to 4 sec between samples. Faster rates are possible using the one-shot mode.

Once a temperature conversion is placed in the THRM\_TEMP\_STAT register, the data can be translated into degrees Celsius (°C) using the following steps:

1. Convert the binary or hexadecimal data read from THRM\_TEMP\_STAT into decimal form.
2. Subtract 60 from the converted THRM\_TEMP\_STAT data; this is the temperature of the silicon in °C.



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Table 22. Pin Function Changes in Different Serial Audio Interface Modes

Signal	Stereo Modes (SAI = 0 or 1)	TDM4 Mode (SAI = 2)	TDM8 Mode (SAI = 3)	TDM16 Mode (SAI = 4)
DSDATA1	Channel 1/Channel 2 data in	Channel 1 to Channel 4 data in	Channel 1 to Channel 8 data in	Channel 1 to Channel 16 data in
DSDATA2	Channel 3/Channel 4 data in	Channel 5 to Channel 8 data in	Channel 9 to Channel 16 data in	Not used
DSDATA3	Channel 5/Channel 6 data in	Channel 9 to Channel 12 data in	Not used	Not used
DSDATA4	Channel 7/Channel 8 data in	Channel 13 to Channel 16 data in	Not used	Not used
DSDATA5	Channel 9/Channel 10 data in	Not used	Not used	Not used
DSDATA6	Channel 11/Channel 12 data in	Not used	Not Used	Not used
DSDATA7	Channel 13/Channel 14 data in	Not used	Not used	Not used
DSDATA8	Channel 15/Channel 16 data in	Not used	Not used	Not used
DLRCLK	DLRCLK in/DLRCLK out	TDM frame sync in/ TDM frame sync out	TDM frame sync in/ TDM frame sync out	TDM frame sync in/ TDM frame sync out
DBCLK	DBCLK in/DBCLK out	TDM DBCLK in/TDM DBCLK out	TDM DBCLK in/TDM DBCLK out	TDM DBCLK in/ TDM DBCLK out
Maximum Sample Rate	192 kHz	192 kHz	96 kHz	48 kHz

**ADDITIONAL MODES**

The ADAU1966 offers several additional modes for board level design enhancements. To reduce the EMI in board level design, serial data can be transmitted without an explicit DBCLK. See Figure 20 for an example of a DAC TDM data transmission mode that does not require a high speed DBCLK or an external MCLK. This configuration is applicable when the ADAU1966 master clock is generated by the PLL with the DLRCLK as the PLL reference frequency.

To relax the requirement for the setup time of the ADAU1966 in cases of high speed TDM data transmission, the ADAU1966 can latch in the data using the falling edge of DBCLK; see the BCLK\_EDGE bit in the DAC\_CTRL1 register. This effectively dedicates the entire BCLK period to the setup time. This mode is useful in cases where the source has a large delay time in the serial data driver. Figure 21 shows this inverted DBCLK mode of data transmission.

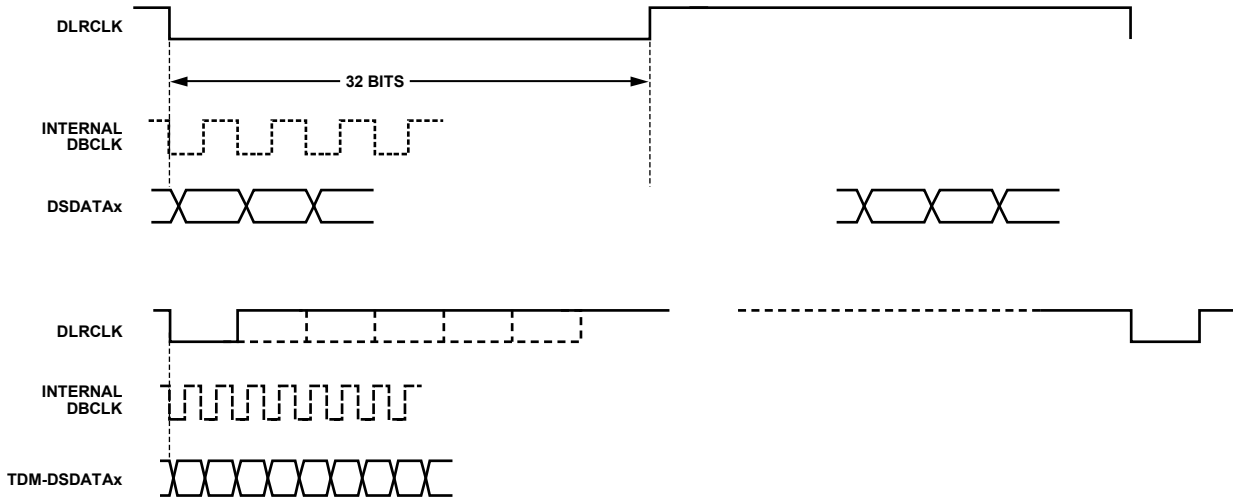


Figure 20. Serial DAC Data Transmission in TDM Format Without DBCLK  
(Applicable Only If PLL Locks to DLCLK)

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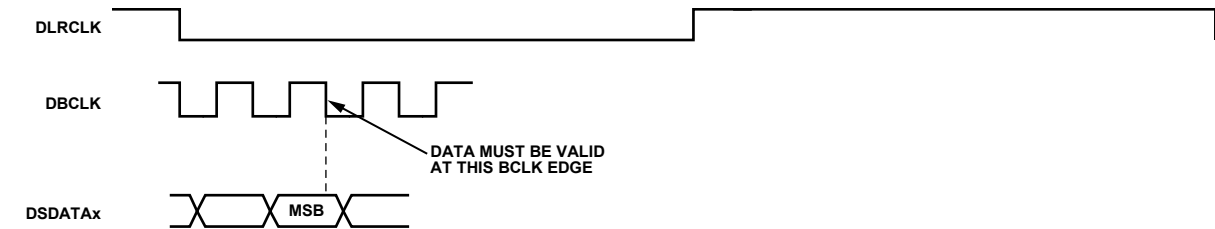


Figure 21. Inverted DBCLK Mode in DAC Serial Data Transmission  
(Applicable in Stereo and TDM, Useful for High Frequency TDM Transmission)

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## REGISTER SUMMARY

Table 23. ADAU1966 Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW	
0x00	PLL_CLK_CTRL0	[7:0]	PLLIN		XTAL_SET		SOFT_RST	MCS		PUP	0x00	RW	
0x01	PLL_CLK_CTRL1	[7:0]	LOPWR_MODE		MCLKO_SEL		PLL_MUTE	PLL_LOCK	VREF_EN	CLK_SEL	0x2A	RW	
0x02	PDN_THRMSSENS_CTRL_1	[7:0]	THRM_RATE		THRM_MODE	THRM_GO	RESERVED	TS_PDN	PLL_PDN	VREG_PDN	0xA0	RW	
0x03	PDN_CTRL2	[7:0]	DAC08_PDN	DAC07_PDN	DAC06_PDN	DAC05_PDN	DAC04_PDN	DAC03_PDN	DAC02_PDN	DAC01_PDN	0x00	RW	
0x04	PDN_CTRL3	[7:0]	DAC16_PDN	DAC15_PDN	DAC14_PDN	DAC13_PDN	DAC12_PDN	DAC11_PDN	DAC10_PDN	DAC09_PDN	0x00	RW	
0x05	THRM_TEMP_STAT	[7:0]	TEMP									0x00	R
0x06	DAC_CTRL0	[7:0]	SDATA_FMT		SAI			FS		MMUTE	0x01	RW	
0x07	DAC_CTRL1	[7:0]	BCLK_GEN	LRCLK_MODE	LRCLK_POL	SAI_MSB	RESERVED	BCLK_RATE	BCLK_EDGE	SAI_MS	0x00	RW	
0x08	DAC_CTRL2	[7:0]	RESERVED	VREG_CTRL		BCLK_TDMC	DAC_POL	AUTO_MUTE_EN	DAC_OSR	DE_EMP_EN	0x06	RW	
0x09	DAC_MUTE1	[7:0]	DAC08_MUTE	DAC07_MUTE	DAC06_MUTE	DAC05_MUTE	DAC04_MUTE	DAC03_MUTE	DAC02_MUTE	DAC01_MUTE	0x00	RW	
0x0A	DAC_MUTE2	[7:0]	DAC16_MUTE	DAC15_MUTE	DAC14_MUTE	DAC13_MUTE	DAC12_MUTE	DAC11_MUTE	DAC10_MUTE	DAC09_MUTE	0x00	RW	
0x0B	DACMSTR_VOL	[7:0]	DACMSTR_VOL									0x00	RW
0x0C	DAC01_VOL	[7:0]	DAC01_VOL									0x00	RW
0x0D	DAC02_VOL	[7:0]	DAC02_VOL									0x00	RW
0x0E	DAC03_VOL	[7:0]	DAC03_VOL									0x00	RW
0x0F	DAC04_VOL	[7:0]	DAC04_VOL									0x00	RW
0x10	DAC05_VOL	[7:0]	DAC05_VOL									0x00	RW
0x11	DAC06_VOL	[7:0]	DAC06_VOL									0x00	RW
0x12	DAC07_VOL	[7:0]	DAC07_VOL									0x00	RW
0x13	DAC08_VOL	[7:0]	DAC08_VOL									0x00	RW
0x14	DAC09_VOL	[7:0]	DAC09_VOL									0x00	RW
0x15	DAC10_VOL	[7:0]	DAC10_VOL									0x00	RW
0x16	DAC11_VOL	[7:0]	DAC11_VOL									0x00	RW
0x17	DAC12_VOL	[7:0]	DAC12_VOL									0x00	RW
0x18	DAC13_VOL	[7:0]	DAC13_VOL									0x00	RW
0x19	DAC14_VOL	[7:0]	DAC14_VOL									0x00	RW
0x1A	DAC15_VOL	[7:0]	DAC15_VOL									0x00	RW
0x1B	DAC16_VOL	[7:0]	DAC16_VOL									0x00	RW
0x1C	CM_SEL_PAD_STRGTH	[7:0]	RESERVED	RESERVED	PAD_DRV	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	0x02	RW	
0x1D	DAC_POWER1	[7:0]	DAC04_POWER		DAC03_POWER		DAC02_POWER		DAC01_POWER			0xAA	RW
0x1E	DAC_POWER2	[7:0]	DAC08_POWER		DAC07_POWER		DAC06_POWER		DAC05_POWER			0xAA	RW
0x1F	DAC_POWER3	[7:0]	DAC12_POWER		DAC11_POWER		DAC10_POWER		DAC09_POWER			0xAA	RW
0x20	DAC_POWER4	[7:0]	DAC16_POWER		DAC15_POWER		DAC14_POWER		DAC13_POWER			0xAA	RW



## REGISTER DETAILS

## PLL AND CLOCK CONTROL 0 REGISTER

Address: 0x00, Reset: 0x00, Name: PLL\_CLK\_CTRL0

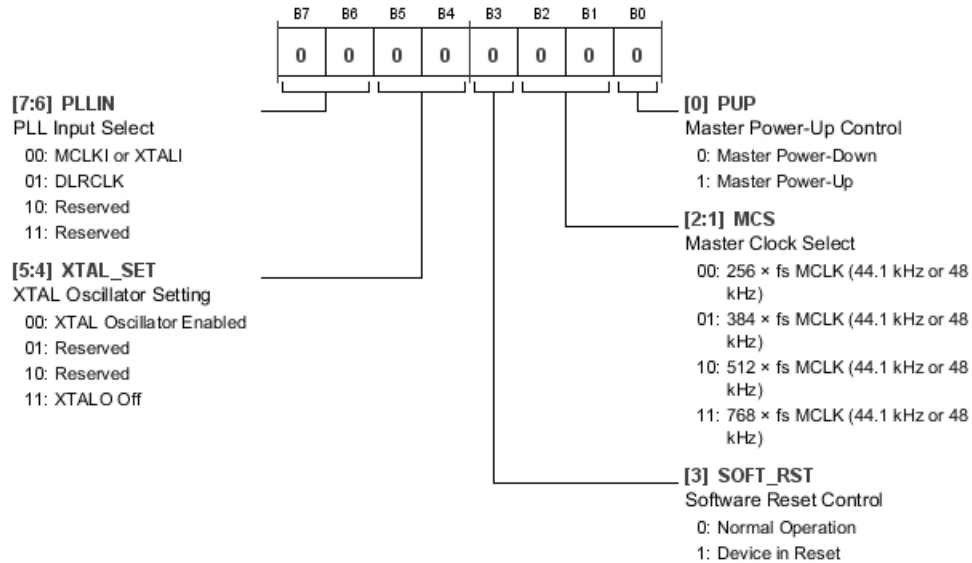


Table 24. Bit Descriptions for PLL\_CLK\_CTRL0

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	PLLIN	00 01 10 11	PLL Input Select. Selects between MCLKI/XTALI or DLRCLK as the input to the PLL. MCLKI or XTALI DLRCLK Reserved Reserved	0x0	RW
[5:4]	XTAL_SET	00 01 10 11	XTAL Oscillator Setting. XTALO pin status. XTAL Oscillator Enabled Reserved Reserved XTALO Off	0x0	RW
3	SOFT_RST	0 1	Software Reset Control. This bit resets all circuitry inside the IC, except I <sup>2</sup> C/SPI communications. All control registers are reset to default values, except Register 0x00 and Register 0x01. The PLL_CLK_CTRLx registers do not change state. Normal Operation Device in Reset	0x0	RW
[2:1]	MCS	00 01 10 11	Master Clock Select. MCLKI/XTALI pin functionality (PLL active), master clock rate setting. The following values are for the $f_s$ rate window from 32 kHz to 48 kHz. See Table 12 for details when using other $f_s$ selections. $256 \times f_s$ MCLK (44.1 kHz or 48 kHz) $384 \times f_s$ MCLK (44.1 kHz or 48 kHz) $512 \times f_s$ MCLK (44.1 kHz or 48 kHz) $768 \times f_s$ MCLK (44.1 kHz or 48 kHz)	0x0	RW
0	PUP	0 1	Master Power-Up Control. This bit must be set to 1 as the first register write to power up the IC. Master Power-Down Master Power-Up	0x0	RW

**PLL AND CLOCK CONTROL 1 REGISTER**

Address: 0x01, Reset: 0x2A, Name: PLL\_CLK\_CTRL1

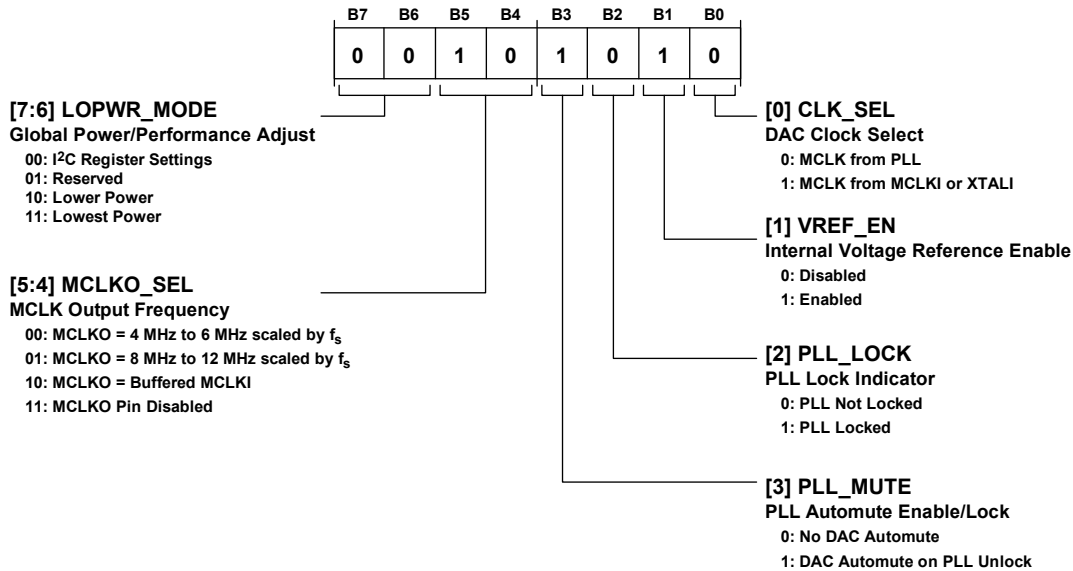


Table 25. Bit Descriptions for PLL\_CLK\_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	LOPWR_MODE	00 01 10 11	Global Power/Performance Adjust. These bits adjust the power consumption and performance level for all 16 DAC channels at once. See the Digital-to-Analog Converters (DACs) section for more details. I <sup>2</sup> C Register Settings Reserved Low Power Lowest Power	0x0	RW
[5:4]	MCLKO_SEL	00 01 10 11	MCLK Output Frequency. Frequency selection for MCLKO pin. See the Clock Signals section for more details. MCLKO = 4 MHz to 6 MHz scaled by $f_s$ MCLKO = 8 MHz to 12 MHz scaled by $f_s$ MCLKO = Buffered MCLKI MCLKO Pin Disabled	0x2	RW
3	PLL_MUTE	0 1	PLL Automute Enable/Lock. This bit enables the PLL lock automute function. No DAC Automute DAC Automute on PLL Unlock	0x1	RW
2	PLL_LOCK	0 1	PLL Lock Indicator. PLL Not Locked PLL Locked	0x0	R
1	VREF_EN	0 1	Internal Voltage Reference Enable. The internal voltage reference powers the common mode for the ADAU1966. Disabling this bit allows the user to drive the CM pin with an outside voltage source. Disabled Enabled	0x1	RW
0	CLK_SEL	0 1	DAC Clock Select. Selects between PLL or Direct MCLK mode. MCLK from PLL MCLK from MCLKI or XTALI	0x0	RW

**BLOCK POWER-DOWN AND THERMAL SENSOR CONTROL 1 REGISTER**

Address: 0x02, Reset: 0xA0, Name: PDN\_THRMSSENS\_CTRL\_1

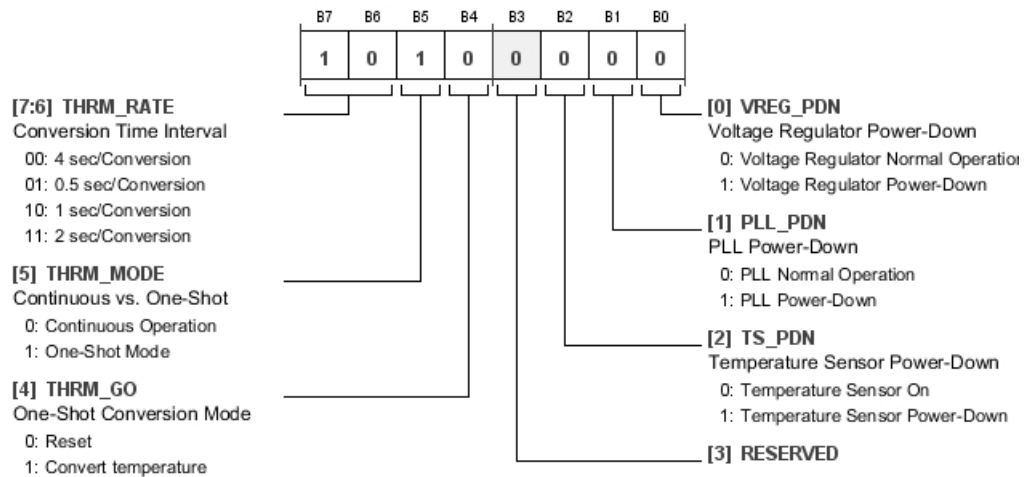


Table 26. Bit Descriptions for PDN\_THRMSSENS\_CTRL\_1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	THRM_RATE	00 01 10 11	Conversion Time Interval. When THERM_MODE = 0, the THERM_RATE bits control the time interval between temperature conversions. 4 sec/Conversion 0.5 sec/Conversion 1 sec/Conversion 2 sec/Conversion	0x2	RW
5	THRM_MODE	0 1	Continuous vs. One-Shot. Determines whether the temperature conversions occur continuously or only when commanded. To perform one-shot temperature conversions, set this bit to 1. Continuous Operation One-Shot Mode	0x1	RW
4	THRM_GO	0 1	One-Shot Conversion Mode. When in one-shot conversion mode, THERM_MODE = 1, the THERM_GO bit must be set to 0 followed by a write of 1. This sequence results in a single temperature conversion. The temperature data is available 120 ms after writing a 1 to this bit. Reset Convert temperature	0x0	RW
2	TS_PDN	0 1	Temperature Sensor Power-Down. Temperature Sensor On Temperature Sensor Power-Down	0x0	RW
1	PLL_PDN	0 1	PLL Power-Down. PLL Normal Operation PLL Power-Down	0x0	RW
0	VREG_PDN	0 1	Voltage Regulator Power-Down. Voltage Regulator Normal Operation Voltage Regulator Power-Down	0x0	RW

**POWER-DOWN CONTROL 2 REGISTER**

Address: 0x03, Reset: 0x00, Name: PDN\_CTRL2

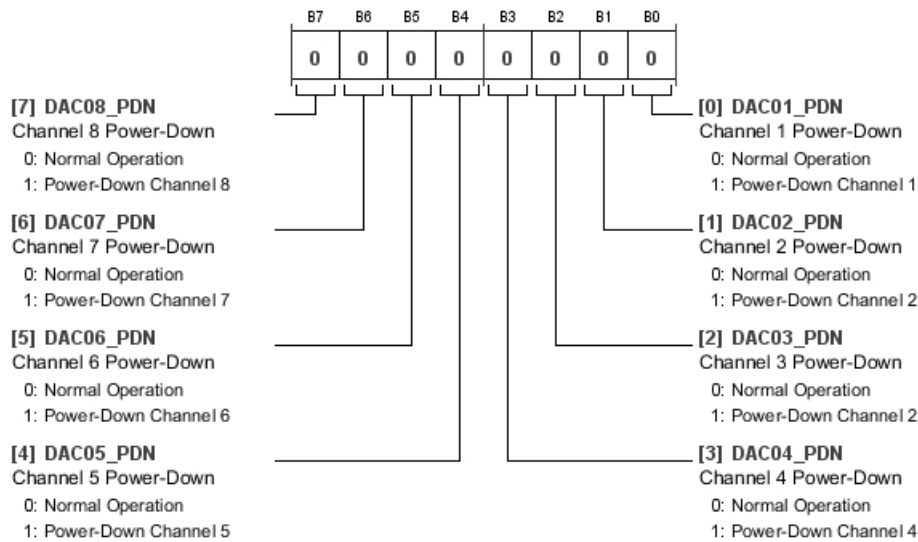


Table 27. Bit Descriptions for PDN\_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
7	DAC08_PDN	0 1	Channel 8 Power-Down. Normal Operation Power-Down Channel 8	0x0	RW
6	DAC07_PDN	0 1	Channel 7 Power-Down. Normal Operation Power-Down Channel 7	0x0	RW
5	DAC06_PDN	0 1	Channel 6 Power-Down. Normal Operation Power-Down Channel 6	0x0	RW
4	DAC05_PDN	0 1	Channel 5 Power-Down. Normal Operation Power-Down Channel 5	0x0	RW
3	DAC04_PDN	0 1	Channel 4 Power-Down. Normal Operation Power-Down Channel 4	0x0	RW
2	DAC03_PDN	0 1	Channel 3 Power-Down. Normal Operation Power-Down Channel 2	0x0	RW
1	DAC02_PDN	0 1	Channel 2 Power-Down. Normal Operation Power-Down Channel 2	0x0	RW
0	DAC01_PDN	0 1	Channel 1 Power-Down. Normal Operation Power-Down Channel 1	0x0	RW

**POWER-DOWN CONTROL 3 REGISTER**

Address: 0x04, Reset: 0x00, Name: PDN\_CTRL3

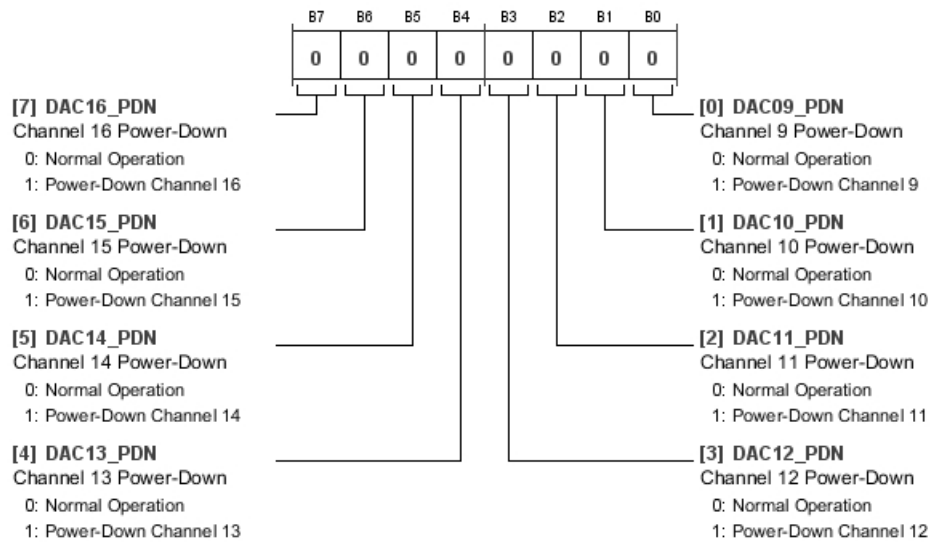


Table 28. Bit Descriptions for PDN\_CTRL3

Bits	Bit Name	Settings	Description	Reset	Access
7	DAC16_PDN	0 1	Channel 16 Power-Down. Normal Operation Power-Down Channel 16	0x0	RW
6	DAC15_PDN	0 1	Channel 15 Power-Down. Normal Operation Power-Down Channel 15	0x0	RW
5	DAC14_PDN	0 1	Channel 14 Power-Down. Normal Operation Power-Down Channel 14	0x0	RW
4	DAC13_PDN	0 1	Channel 13 Power-Down. Normal Operation Power-Down Channel 13	0x0	RW
3	DAC12_PDN	0 1	Channel 12 Power-Down. Normal Operation Power-Down Channel 12	0x0	RW
2	DAC11_PDN	0 1	Channel 11 Power-Down. Normal Operation Power-Down Channel 11	0x0	RW
1	DAC10_PDN	0 1	Channel 10 Power-Down. Normal Operation Power-Down Channel 10	0x0	RW
0	DAC09_PDN	0 1	Channel 9 Power-Down. Normal Operation Power-Down Channel 9	0x0	RW

**THERMAL SENSOR TEMPERATURE READOUT REGISTER**

Address: 0x05, Reset: 0x00, Name: THRM\_TEMP\_STAT

Thermal Sensor Temperature Readout. –60°C to +140°C range, 1°C step size. Read this register and convert the hexadecimal or binary TEMP value into decimal form; then subtract 60 from this decimal conversion. The result is the temperature in degrees Celsius.

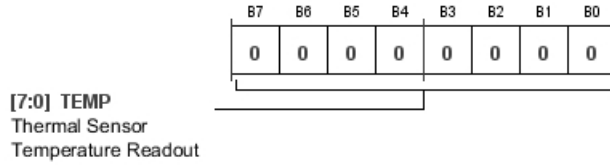


Table 29. Bit Descriptions for THRM\_TEMP\_STAT

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	TEMP		Thermal Sensor Temperature Readout. –60°C to +140°C range, 1°C step size. To convert TEMP code to temperature, use the equation (TEMP – 60).	0x00	R

**DAC CONTROL 0 REGISTER**

Address: 0x06, Reset: 0x01, Name: DAC\_CTRL0

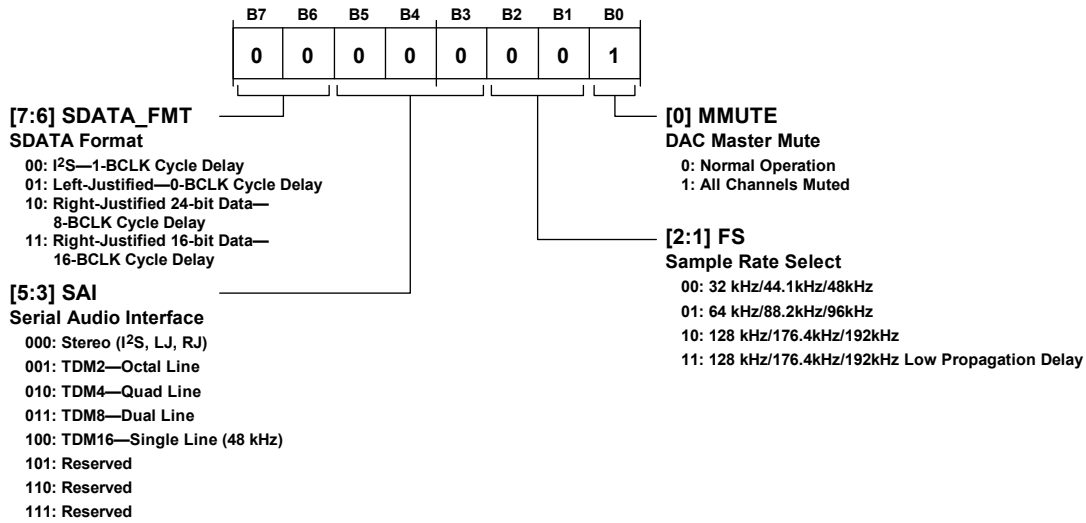
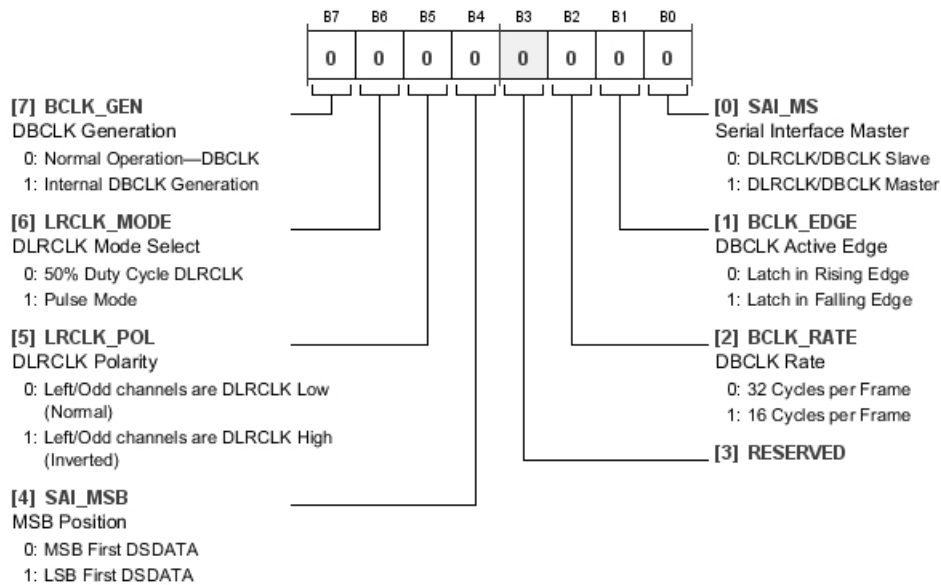


Table 30. Bit Descriptions for DAC\_CTRL0

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	SDATA_FMT	00 01 10 11	SDATA Format. Only used when SAI = 000. I <sup>2</sup> S—1-BCLK Cycle Delay Left-Justified—0-BCLK Cycle Delay Right-Justified 24-bit Data—8-BCLK Cycle Delay Right-Justified 16-bit Data—16-BCLK Cycle Delay	0x0	RW
[5:3]	SAI	000 001 010 011 100 101 110 111	Serial Audio Interface. When SAI = 000, the SDATA_FMT bits control stereo SDATA format. Stereo (I <sup>2</sup> S, LJ, RJ) TDM2—Octal Line TDM4—Quad Line TDM8—Dual Line TDM16—Single Line (48 kHz) Reserved Reserved Reserved	0x0	RW
[2:1]	FS	00 01 10 11	Sample Rate Select. 32 kHz/44.1 kHz/48 kHz 64 kHz/88.2 kHz/96 kHz 128 kHz/176.4 kHz/192 kHz 128 kHz/176.4 kHz/192 kHz Low Propagation Delay	0x0	RW
0	MMUTE	0 1	DAC Master Mute. Normal Operation All Channels Muted	0x1	RW

**DAC CONTROL 1 REGISTER**

Address: 0x07, Reset: 0x00, Name: DAC\_CTRL1



**Table 31. Bit Descriptions for DAC\_CTRL1**

Bits	Bit Name	Settings	Description	Reset	Access
7	BCLK_GEN	0 1	DBCLK Generation. When the PLL is locked to DLRCLK, it is possible to run the ADAU1966 without an external DBCLK. 0 Normal Operation—DBCLK 1 Internal DBCLK Generation	0x0	RW
6	LRCLK_MODE	0 1	DLRCLK Mode Select. Only Valid for TDM modes. 0 50% Duty Cycle DLRCLK 1 Pulse Mode	0x0	RW
5	LRCLK_POL	0 1	DLRCLK Polarity. Allows the swapping of data between channels. 0 Left/Odd channels are DLRCLK Low (Normal) 1 Left/Odd channels are DLRCLK High (Inverted)	0x0	RW
4	SAI_MSB	0 1	MSB Position. 0 MSB First DSDATA 1 LSB First DSDATA	0x0	RW
2	BCLK_RATE	0 1	DBCLK Rate. Number of DBCLK cycles per DLRCLK Frame. Used only for generating DBCLK in Master Mode operation (SAI_MS = 1). 0 32 Cycles per Frame 1 16 Cycles per Frame	0x0	RW
1	BCLK_EDGE	0 1	DBCLK Active Edge. Adjust the polarity of the DBCLK leading edge. 0 Latch in Rising Edge 1 Latch in Falling Edge	0x0	RW
0	SAI_MS	0 1	Serial Interface Master. Both DLRCLK and DBCLK become master when enabled. 0 DLRCLK/DBCLK Slave 1 DLRCLK/DBCLK Master	0x0	RW



**DAC CONTROL 2 REGISTER**

Address: 0x08, Reset: 0x06, Name: DAC\_CTRL2

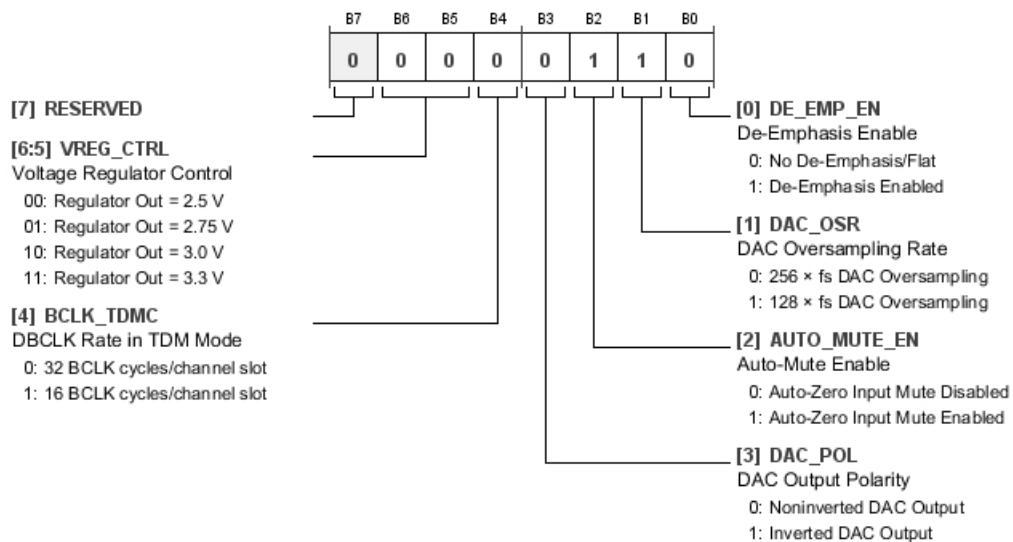


Table 32. Bit Descriptions for DAC\_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[6:5]	VREG_CTRL	00 01 10 11	Voltage Regulator Control. Select the Regulator Output Voltage. Regulator Out = 2.5 V Regulator Out = 2.75 V Regulator Out = 3.0 V Regulator Out = 3.3 V	0x0	RW
4	BCLK_TDMC	0 1	DBCLK Rate in TDM Mode. Number of DBCLK cycles per channel slot when in TDM mode. 32 BCLK cycles/channel slot 16 BCLK cycles/channel slot	0x0	RW
3	DAC_POL	0 1	DAC Output Polarity. This is a global switch of DAC polarity. Noninverted DAC Output Inverted DAC Output	0x0	RW
2	AUTO_MUTE_EN	0 1	Automute Enable. Automatically mutes the DACs when 1024 consecutive zero input samples are received. This is independent per channel. Auto-Zero Input Mute Disabled Auto-Zero Input Mute Enabled	0x1	RW
1	DAC_OSR	0 1	DAC Oversampling Rate. OSR Selection. 256 × $f_s$ DAC Oversampling 128 × $f_s$ DAC Oversampling	0x1	RW
0	DE_EMP_EN	0 1	De-Emphasis Enable. No De-Emphasis/Flat De-Emphasis Enabled	0x0	RW

**DAC INDIVIDUAL CHANNEL MUTES 1 REGISTER**

Address: 0x09, Reset: 0x00, Name: DAC\_MUTE1

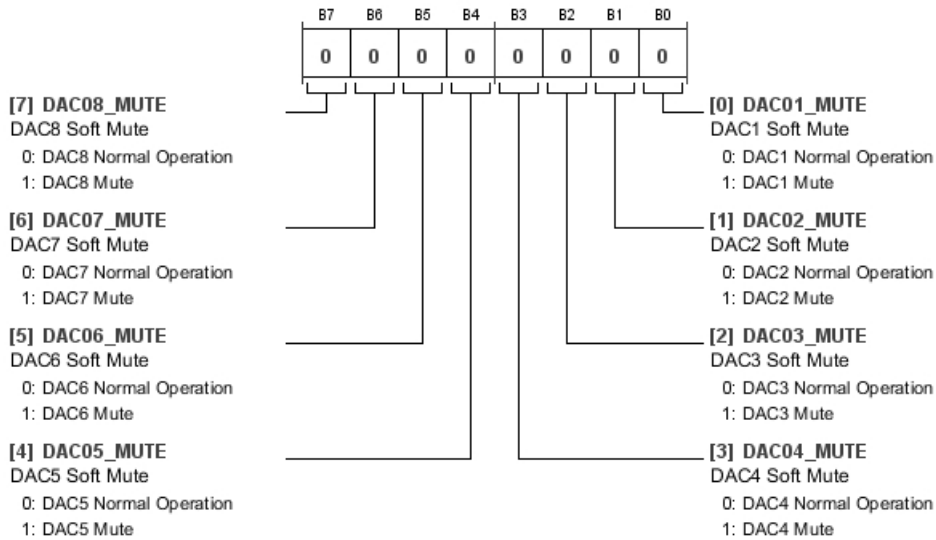


Table 33. Bit Descriptions for DAC\_MUTE1

Bits	Bit Name	Settings	Description	Reset	Access
7	DAC08_MUTE	0 1	DAC8 Soft Mute. DAC8 Normal Operation DAC8 Mute	0x0	RW
6	DAC07_MUTE	0 1	DAC7 Soft Mute. DAC7 Normal Operation DAC7 Mute	0x0	RW
5	DAC06_MUTE	0 1	DAC6 Soft Mute. DAC6 Normal Operation DAC6 Mute	0x0	RW
4	DAC05_MUTE	0 1	DAC5 Soft Mute. DAC5 Normal Operation DAC5 Mute	0x0	RW
3	DAC04_MUTE	0 1	DAC4 Soft Mute. DAC4 Normal Operation DAC4 Mute	0x0	RW
2	DAC03_MUTE	0 1	DAC3 Soft Mute. DAC3 Normal Operation DAC3 Mute	0x0	RW
1	DAC02_MUTE	0 1	DAC2 Soft Mute. DAC2 Normal Operation DAC2 Mute	0x0	RW
0	DAC01_MUTE	0 1	DAC1 Soft Mute. DAC1 Normal Operation DAC1 Mute	0x0	RW

**DAC INDIVIDUAL CHANNEL MUTES 2 REGISTER**

Address: 0x0A, Reset: 0x00, Name: DAC\_MUTE2

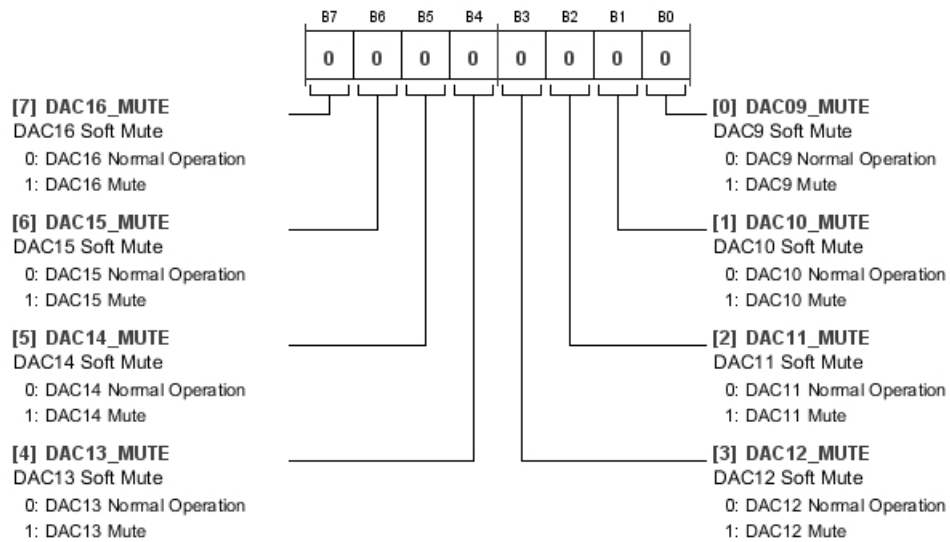


Table 34. Bit Descriptions for DAC\_MUTE2

Bits	Bit Name	Settings	Description	Reset	Access
7	DAC16_MUTE	0 1	DAC16 Soft Mute. DAC16 Normal Operation DAC16 Mute	0x0	RW
6	DAC15_MUTE	0 1	DAC15 Soft Mute. DAC15 Normal Operation DAC15 Mute	0x0	RW
5	DAC14_MUTE	0 1	DAC14 Soft Mute. DAC14 Normal Operation DAC14 Mute	0x0	RW
4	DAC13_MUTE	0 1	DAC13 Soft Mute. DAC13 Normal Operation DAC13 Mute	0x0	RW
3	DAC12_MUTE	0 1	DAC12 Soft Mute. DAC12 Normal Operation DAC12 Mute	0x0	RW
2	DAC11_MUTE	0 1	DAC11 Soft Mute. DAC11 Normal Operation DAC11 Mute	0x0	RW
1	DAC10_MUTE	0 1	DAC10 Soft Mute. DAC10 Normal Operation DAC10 Mute	0x0	RW
0	DAC09_MUTE	0 1	DAC9 Soft Mute. DAC9 Normal Operation DAC9 Mute	0x0	RW

**MASTER VOLUME CONTROL REGISTER**

Address: 0x0B, Reset: 0x00, Name: DACMSTR\_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 57 for a complete list of the volume settings.



**[7:0] DACMSTR\_VOL**  
 Master Volume Control  
 00000000: 0 dB (default)  
 00000001: -0.375 dB  
 00000010: -0.750 dB  
 11111110: -95.250 dB  
 11111111: -95.625 dB

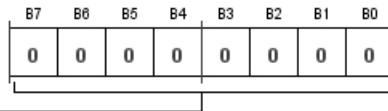
**Table 35. Bit Descriptions for DACMSTR\_VOL**

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DACMSTR_VOL	00000000 00000001 00000010 11111110 11111111	Master Volume Control. 0 dB (default) -0.375 dB -0.750 dB -95.250 dB -95.625 dB	0x00	RW

**DAC 1 VOLUME CONTROL REGISTER**

Address: 0x0C, Reset: 0x00, Name: DAC01\_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 57 for a complete list of the volume settings.



**[7:0] DAC01\_VOL**  
 DAC Volume Control Channel 1  
 00000000: 0 dB (default)  
 00000001: -0.375 dB  
 00000010: -0.750 dB  
 11111110: -95.250 dB  
 11111111: -95.625 dB

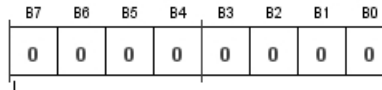
**Table 36. Bit Descriptions for DAC01\_VOL**

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC01_VOL	00000000 00000001 00000010 11111110 11111111	DAC Volume Control Channel 1. 0 dB (default) -0.375 dB -0.750 dB -95.250 dB -95.625 dB	0x00	RW

**DAC 2 VOLUME CONTROL REGISTER**

Address: 0x0D, Reset: 0x00, Name: DAC02\_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 57 for a complete list of the volume settings.



[7:0] DAC02\_VOL

DAC Volume Control Channel 2

00000000: 0 dB (default)  
 00000001: -0.375 dB  
 00000010: -0.750 dB  
 11111110: -95.250 dB  
 11111111: -95.625 dB

Table 37. Bit Descriptions for DAC02\_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC02_VOL	00000000 00000001 00000010 11111110 11111111	DAC Volume Control Channel 2. 0 dB (default) -0.375 dB -0.750 dB -95.250 dB -95.625 dB	0x00	RW

**DAC 3 VOLUME CONTROL REGISTER**

Address: 0x0E, Reset: 0x00, Name: DAC03\_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 57 for a complete list of the volume settings.



[7:0] DAC03\_VOL

DAC Volume Control Channel 3

00000000: 0 dB (default)  
 00000001: -0.375 dB  
 00000010: -0.750 dB  
 11111110: -95.250 dB  
 11111111: -95.625 dB

Table 38. Bit Descriptions for DAC03\_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC03_VOL	00000000 00000001 00000010 11111110 11111111	DAC Volume Control Channel 3. 0 dB (default) -0.375 dB -0.750 dB -95.250 dB -95.625 dB	0x00	RW

**DAC 4 VOLUME CONTROL REGISTER**

Address: 0x0F, Reset: 0x00, Name: DAC04\_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 57 for a complete list of the volume settings.

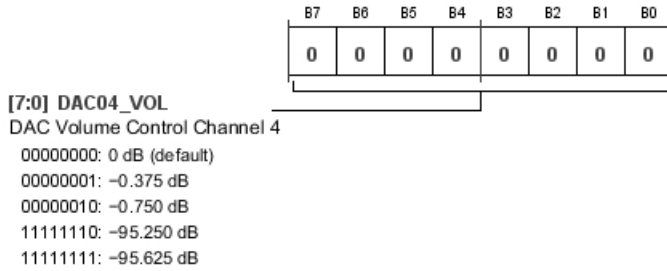


Table 39. Bit Descriptions for DAC04\_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC04_VOL	00000000 00000001 00000010 11111110 11111111	DAC Volume Control Channel 4. 0 dB (default) -0.375 dB -0.750 dB -95.250 dB -95.625 dB	0x00	RW

**DAC 5 VOLUME CONTROL REGISTER**

Address: 0x10, Reset: 0x00, Name: DAC05\_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 57 for a complete list of the volume settings.

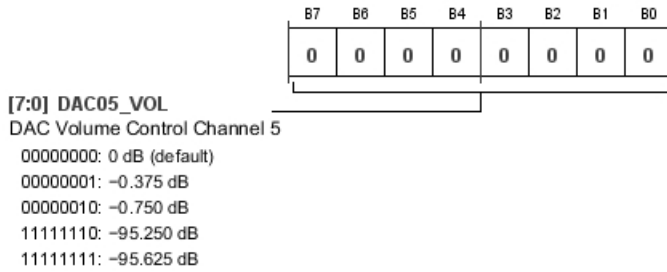


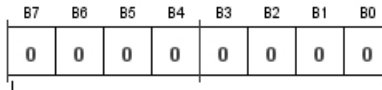
Table 40. Bit Descriptions for DAC05\_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC05_VOL	00000000 00000001 00000010 11111110 11111111	DAC Volume Control Channel 5. 0 dB (default) -0.375 dB -0.750 dB -95.250 dB -95.625 dB	0x00	RW

**DAC 6 VOLUME CONTROL REGISTER**

Address: 0x11, Reset: 0x00, Name: DAC06\_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 57 for a complete list of the volume settings.

**[7:0] DAC06\_VOL**

DAC Volume Control Channel 6

00000000: 0 dB (default)  
 00000001: -0.375 dB  
 00000010: -0.750 dB  
 11111110: -95.250 dB  
 11111111: -95.625 dB

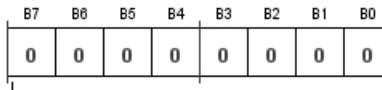
Table 41. Bit Descriptions for DAC06\_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC06_VOL		DAC Volume Control Channel 6.	0x00	RW
		00000000	0 dB (default)		
		00000001	-0.375 dB		
		00000010	-0.750 dB		
		11111110	-95.250 dB		
		11111111	-95.625 dB		

**DAC 7 VOLUME CONTROL REGISTER**

Address: 0x12, Reset: 0x00, Name: DAC07\_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 57 for a complete list of the volume settings.

**[7:0] DAC07\_VOL**

DAC Volume Control Channel 7

00000000: 0 dB (default)  
 00000001: -0.375 dB  
 00000010: -0.750 dB  
 11111110: -95.250 dB  
 11111111: -95.625 dB

Table 42. Bit Descriptions for DAC07\_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC07_VOL		DAC Volume Control Channel 7.	0x00	RW
		00000000	0 dB (default)		
		00000001	-0.375 dB		
		00000010	-0.750 dB		
		11111110	-95.250 dB		
		11111111	-95.625 dB		

**DAC 8 VOLUME CONTROL REGISTER**

Address: 0x13, Reset: 0x00, Name: DAC08\_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 57 for a complete list of the volume settings.

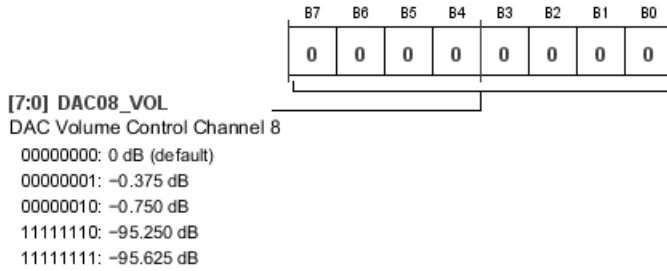


Table 43. Bit Descriptions for DAC08\_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC08_VOL	00000000 00000001 00000010 11111110 11111111	DAC Volume Control Channel 8. 0 dB (default) -0.375 dB -0.750 dB -95.250 dB -95.625 dB	0x00	RW

**DAC 9 VOLUME CONTROL REGISTER**

Address: 0x14, Reset: 0x00, Name: DAC09\_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 57 for a complete list of the volume settings.

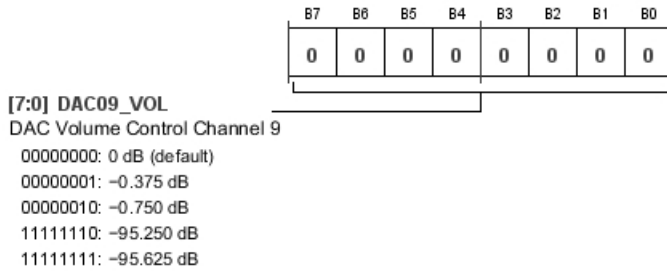


Table 44. Bit Descriptions for DAC09\_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC09_VOL	00000000 00000001 00000010 11111110 11111111	DAC Volume Control Channel 9. 0 dB (default) -0.375 dB -0.750 dB -95.250 dB -95.625 dB	0x00	RW



**DAC 10 VOLUME CONTROL REGISTER**

Address: 0x15, Reset: 0x00, Name: DAC10\_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 57 for a complete list of the volume settings.

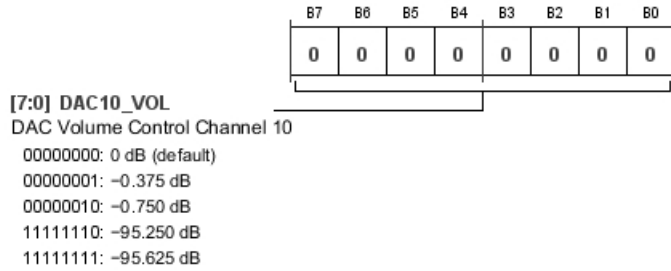


Table 45. Bit Descriptions for DAC10\_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC10_VOL	00000000 00000001 00000010 11111110 11111111	DAC Volume Control Channel 10. 0 dB (default) -0.375 dB -0.750 dB -95.250 dB -95.625 dB	0x00	RW

**DAC 11 VOLUME CONTROL REGISTER**

Address: 0x16, Reset: 0x00, Name: DAC11\_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 57 for a complete list of the volume settings.

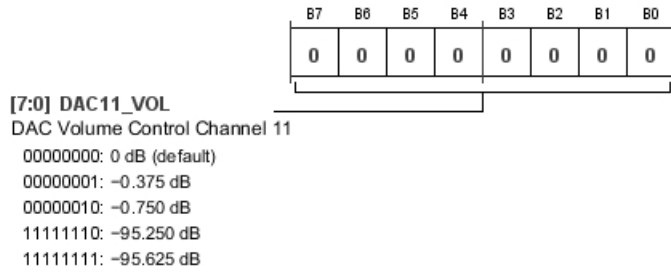


Table 46. Bit Descriptions for DAC11\_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC11_VOL	00000000 00000001 00000010 11111110 11111111	DAC Volume Control Channel 11. 0 dB (default) -0.375 dB -0.750 dB -95.250 dB -95.625 dB	0x00	RW

**DAC 12 VOLUME CONTROL REGISTER**

Address: 0x17, Reset: 0x00, Name: DAC12\_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 57 for a complete list of the volume settings.

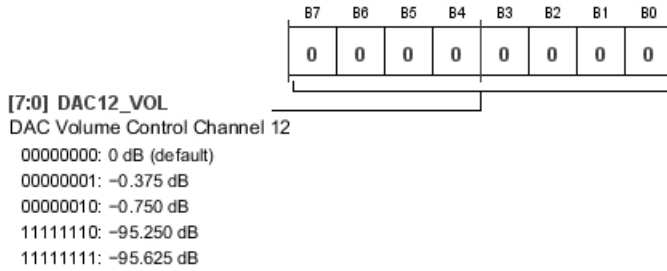


Table 47. Bit Descriptions for DAC12\_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC12_VOL	00000000 00000001 00000010 11111110 11111111	DAC Volume Control Channel 12. 0 dB (default) -0.375 dB -0.750 dB -95.250 dB -95.625 dB	0x00	RW

**DAC 13 VOLUME CONTROL REGISTER**

Address: 0x18, Reset: 0x00, Name: DAC13\_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 57 for a complete list of the volume settings.

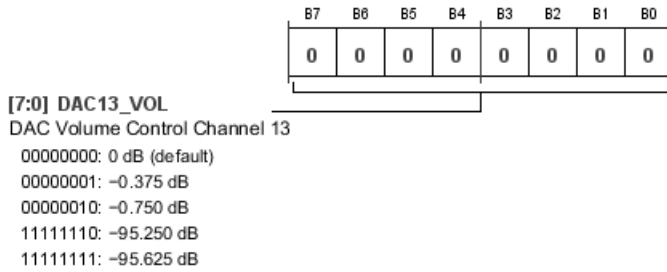


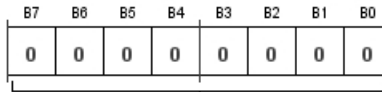
Table 48. Bit Descriptions for DAC13\_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC13_VOL	00000000 00000001 00000010 11111110 11111111	DAC Volume Control Channel 13. 0 dB (default) -0.375 dB -0.750 dB -95.250 dB -95.625 dB	0x00	RW

**DAC 14 VOLUME CONTROL REGISTER**

Address: 0x19, Reset: 0x00, Name: DAC14\_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 57 for a complete list of the volume settings.



[7:0] DAC14\_VOL  
 DAC Volume Control Channel 14  
 00000000: 0 dB (default)  
 00000001: -0.375 dB  
 00000010: -0.750 dB  
 11111110: -95.250 dB  
 11111111: -95.625 dB

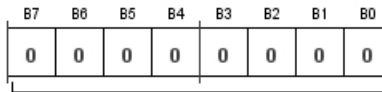
Table 49. Bit Descriptions for DAC14\_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC14_VOL	00000000 00000001 00000010 11111110 11111111	DAC Volume Control Channel 14. 0 dB (default) -0.375 dB -0.750 dB -95.250 dB -95.625 dB	0x00	RW

**DAC 15 VOLUME CONTROL REGISTER**

Address: 0x1A, Reset: 0x00, Name: DAC15\_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 57 for a complete list of the volume settings.



[7:0] DAC15\_VOL  
 DAC Volume Control Channel 15  
 00000000: 0 dB (default)  
 00000001: -0.375 dB  
 00000010: -0.750 dB  
 11111110: -95.250 dB  
 11111111: -95.625 dB

Table 50. Bit Descriptions for DAC15\_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC15_VOL	00000000 00000001 00000010 11111110 11111111	DAC Volume Control Channel 15. 0 dB (default) -0.375 dB -0.750 dB -95.250 dB -95.625 dB	0x00	RW

**DAC 16 VOLUME CONTROL REGISTER**

Address: 0x1B, Reset: 0x00, Name: DAC16\_VOL

Each 1-bit step corresponds to a 0.375 dB change in volume. See Table 57 for a complete list of the volume settings.

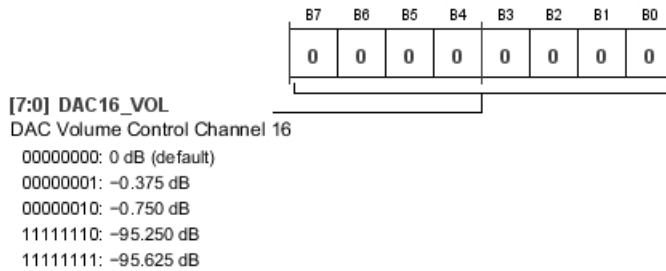


Table 51. Bit Descriptions for DAC16\_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC16_VOL	00000000 00000001 00000010 11111110 11111111	DAC Volume Control Channel 16. 0 dB (default) -0.375 dB -0.750 dB -95.250 dB -95.625 dB	0x00	RW

**COMMON MODE AND PAD STRENGTH REGISTER**

Address: 0x1C, Reset: 0x02, Name: CM\_SEL\_PAD\_STRGTH

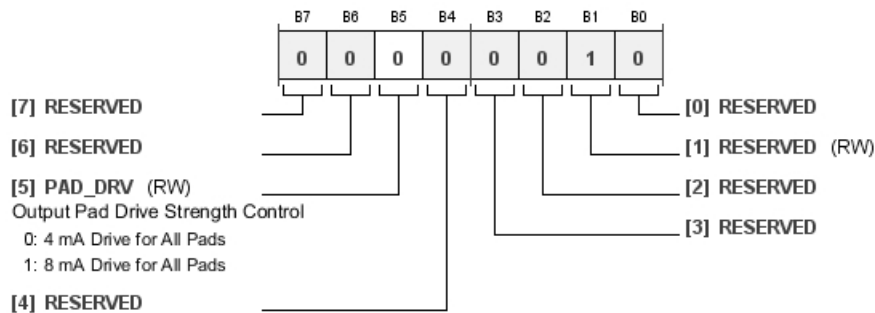
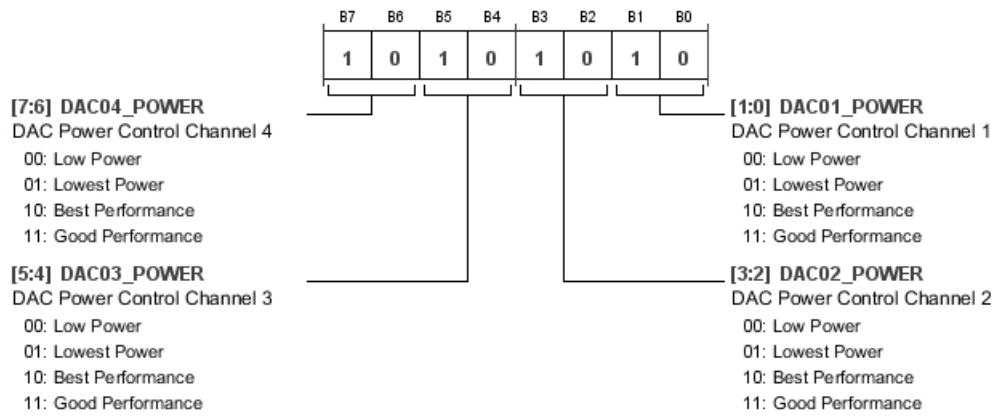


Table 52. Bit Descriptions for CM\_SEL\_PAD\_STRGTH

Bits	Bit Name	Settings	Description	Reset	Access
5	PAD_DRV	0 1	Output Pad Drive Strength Control. Pad strength is stated for IOVDD = 5 V. 4 mA Drive for All Pads 8 mA Drive for All Pads	0x0	RW

**DAC POWER ADJUST 1 REGISTER**

Address: 0x1D, Reset: 0xAA, Name: DAC\_POWER1

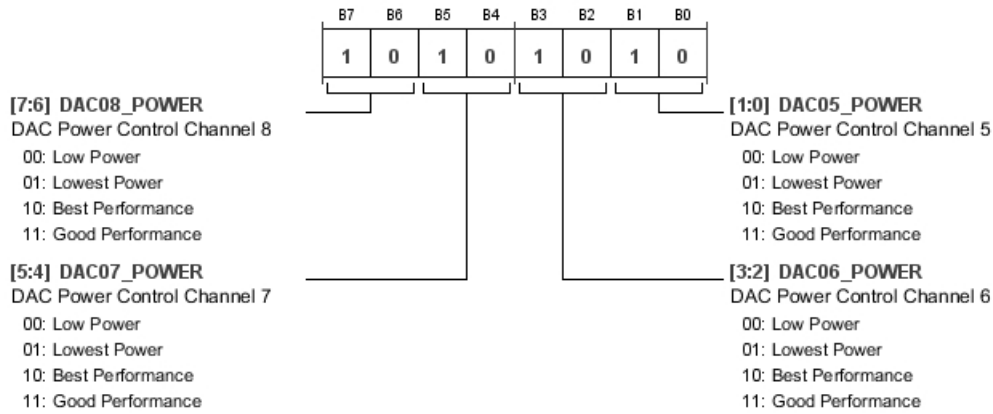


**Table 53. Bit Descriptions for DAC\_POWER1**

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	DAC04_POWER	00 01 10 11	DAC Power Control Channel 4. Low Power Lowest Power Best Performance Good Performance	0x2	RW
[5:4]	DAC03_POWER	00 01 10 11	DAC Power Control Channel 3. Low Power Lowest Power Best Performance Good Performance	0x2	RW
[3:2]	DAC02_POWER	00 01 10 11	DAC Power Control Channel 2. Low Power Lowest Power Best Performance Good Performance	0x2	RW
[1:0]	DAC01_POWER	00 01 10 11	DAC Power Control Channel 1. Low Power Lowest Power Best Performance Good Performance	0x2	RW

**DAC POWER ADJUST 2 REGISTER**

Address: 0x1E, Reset: 0xAA, Name: DAC\_POWER2



**Table 54. Bit Descriptions for DAC\_POWER2**

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	DAC08_POWER	00 01 10 11	DAC Power Control Channel 8. Low Power Lowest Power Best Performance Good Performance	0x2	RW
[5:4]	DAC07_POWER	00 01 10 11	DAC Power Control Channel 7. Low Power Lowest Power Best Performance Good Performance	0x2	RW
[3:2]	DAC06_POWER	00 01 10 11	DAC Power Control Channel 6. Low Power Lowest Power Best Performance Good Performance	0x2	RW
[1:0]	DAC05_POWER	00 01 10 11	DAC Power Control Channel 5. Low Power Lowest Power Best Performance Good Performance	0x2	RW

**DAC POWER ADJUST 3 REGISTER**

Address: 0x1F, Reset: 0xAA, Name: DAC\_POWER3

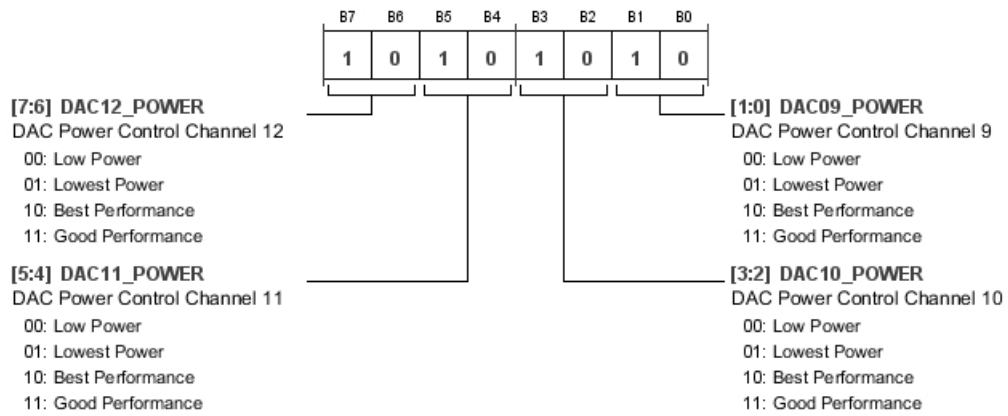
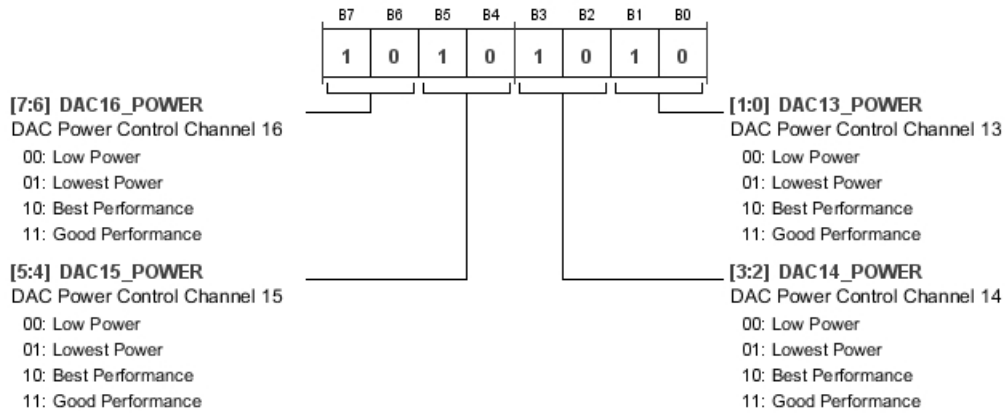


Table 55. Bit Descriptions for DAC\_POWER3

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	DAC12_POWER	00 01 10 11	DAC Power Control Channel 12. Low Power Lowest Power Best Performance Good Performance	0x2	RW
[5:4]	DAC11_POWER	00 01 10 11	DAC Power Control Channel 11. Low Power Lowest Power Best Performance Good Performance	0x2	RW
[3:2]	DAC10_POWER	00 01 10 11	DAC Power Control Channel 10. Low Power Lowest Power Best Performance Good Performance	0x2	RW
[1:0]	DAC09_POWER	00 01 10 11	DAC Power Control Channel 9. Low Power Lowest Power Best Performance Good Performance	0x2	RW

**DAC POWER ADJUST 4 REGISTER**

Address: 0x20, Reset: 0xAA, Name: DAC\_POWER4



**Table 56. Bit Descriptions for DAC\_POWER4**

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	DAC16_POWER	00 01 10 11	DAC Power Control Channel 16. Low Power Lowest Power Best Performance Good Performance	0x2	RW
[5:4]	DAC15_POWER	00 01 10 11	DAC Power Control Channel 15. Low Power Lowest Power Best Performance Good Performance	0x2	RW
[3:2]	DAC14_POWER	00 01 10 11	DAC Power Control Channel 14. Low Power Lowest Power Best Performance Good Performance	0x2	RW
[1:0]	DAC13_POWER	00 01 10 11	DAC Power Control Channel 13. Low Power Lowest Power Best Performance Good Performance	0x2	RW



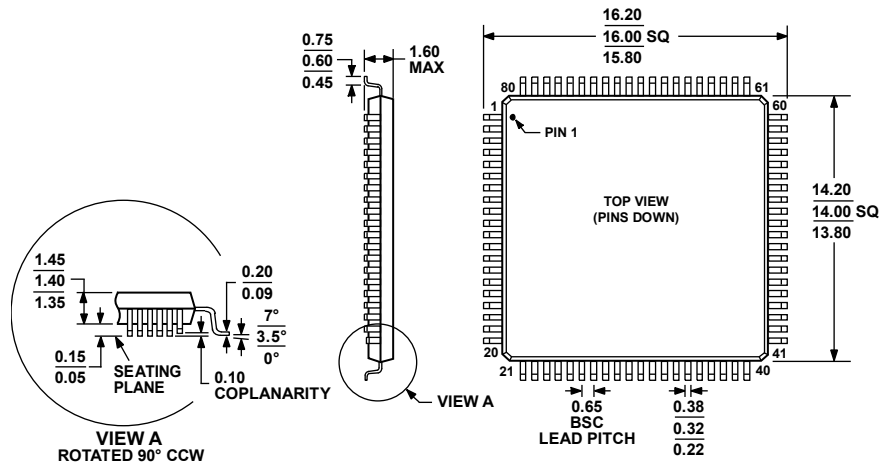
Table 57. Volume Table

Binary Value	Volume Attenuation (dB)	Binary Value	Volume Attenuation (dB)
00000000	0	00101110	-17.25
00000001	-0.375	00101111	-17.625
00000010	-0.75	00110000	-18
00000011	-1.125	00110001	-18.375
00000100	-1.5	00110010	-18.75
00000101	-1.875	00110011	-19.125
00000110	-2.25	00110100	-19.5
00000111	-2.625	00110101	-19.875
00001000	-3	00110110	-20.25
00001001	-3.375	00110111	-20.625
00001010	-3.75	00111000	-21
00001011	-4.125	00111001	-21.375
00001100	-4.5	00111010	-21.75
00001101	-4.875	00111011	-22.125
00001110	-5.25	00111100	-22.5
00001111	-5.625	00111101	-22.875
00010000	-6	00111110	-23.25
00010001	-6.375	00111111	-23.625
00010010	-6.75	01000000	-24
00010011	-7.125	01000001	-24.375
00010100	-7.5	01000010	-24.75
00010101	-7.875	01000011	-25.125
00010110	-8.25	01000100	-25.5
00010111	-8.625	01000101	-25.875
00011000	-9	01000110	-26.25
00011001	-9.375	01000111	-26.625
00011010	-9.75	01001000	-27
00011011	-10.125	01001001	-27.375
00011100	-10.5	01001010	-27.75
00011101	-10.875	01001011	-28.125
00011110	-11.25	01001100	-28.5
00011111	-11.625	01001101	-28.875
00100000	-12	01001110	-29.25
00100001	-12.375	01001111	-29.625
00100010	-12.75	01010000	-30
00100011	-13.125	01010001	-30.375
00100100	-13.5	01010010	-30.75
00100101	-13.875	01010011	-31.125
00100110	-14.25	01010100	-31.5
00100111	-14.625	01010101	-31.875
00101000	-15	01010110	-32.25
00101001	-15.375	01010111	-32.625
00101010	-15.75	01011000	-33
00101011	-16.125	01011001	-33.375
00101100	-16.5	01011010	-33.75
00101101	-16.875	01011011	-34.125

<b>Binary Value</b>	<b>Volume Attenuation (dB)</b>	<b>Binary Value</b>	<b>Volume Attenuation (dB)</b>
01011100	-34.5	10001011	-52.125
01011101	-34.875	10001100	-52.5
01011110	-35.25	10001101	-52.875
01011111	-35.625	10001110	-53.25
01100000	-36	10001111	-53.625
01100001	-36.375	10010000	-54
01100010	-36.75	10010001	-54.375
01100011	-37.125	10010010	-54.75
01100100	-37.5	10010011	-55.125
01100101	-37.875	10010100	-55.5
01100110	-38.25	10010101	-55.875
01100111	-38.625	10010110	-56.25
01101000	-39	10010111	-56.625
01101001	-39.375	10011000	-57
01101010	-39.75	10011001	-57.375
01101011	-40.125	10011010	-57.75
01101100	-40.5	10011011	-58.125
01101101	-40.875	10011100	-58.5
01101110	-41.25	10011101	-58.875
01101111	-41.625	10011110	-59.25
01110000	-42	10011111	-59.625
01110001	-42.375	10100000	-60
01110010	-42.75	10100001	-60.375
01110011	-43.125	10100010	-60.75
01110100	-43.5	10100011	-61.125
01110101	-43.875	10100100	-61.5
01110110	-44.25	10100101	-61.875
01110111	-44.625	10100110	-62.25
01111000	-45	10100111	-62.625
01111001	-45.375	10101000	-63
01111010	-45.75	10101001	-63.375
01111011	-46.125	10101010	-63.75
01111100	-46.5	10101011	-64.125
01111101	-46.875	10101100	-64.5
01111110	-47.25	10101101	-64.875
01111111	-47.625	10101110	-65.25
10000000	-48	10101111	-65.625
10000001	-48.375	10110000	-66
10000010	-48.75	10110001	-66.375
10000011	-49.125	10110010	-66.75
10000100	-49.5	10110011	-67.125
10000101	-49.875	10110100	-67.5
10000110	-50.25	10110101	-67.875
10000111	-50.625	10110110	-68.25
10001000	-51	10110111	-68.625
10001001	-51.375	10111000	-69
10001010	-51.75	10111001	-69.375

Binary Value	Volume Attenuation (dB)	Binary Value	Volume Attenuation (dB)
10111010	-69.75	11011101	-82.875
10111011	-70.125	11011110	-83.25
10111100	-70.5	11011111	-83.625
10111101	-70.875	11100000	-84
10111110	-71.25	11100001	-84.375
10111111	-71.625	11100010	-84.75
11000000	-72	11100011	-85.125
11000001	-72.375	11100100	-85.5
11000010	-72.75	11100101	-85.875
11000011	-73.125	11100110	-86.25
11000100	-73.5	11100111	-86.625
11000101	-73.875	11101000	-87
11000110	-74.25	11101001	-87.375
11000111	-74.625	11101010	-87.75
11001000	-75	11101011	-88.125
11001001	-75.375	11101100	-88.5
11001010	-75.75	11101101	-88.875
11001011	-76.125	11101110	-89.25
11001100	-76.5	11101111	-89.625
11001101	-76.875	11110000	-90
11001110	-77.25	11110001	-90.375
11001111	-77.625	11110010	-90.75
11010000	-78	11110011	-91.125
11010001	-78.375	11110100	-91.5
11010010	-78.75	11110101	-91.875
11010011	-79.125	11110110	-92.25
11010100	-79.5	11110111	-92.625
11010101	-79.875	11111000	-93
11010110	-80.25	11111001	-93.375
11010111	-80.625	11111010	-93.75
11011000	-81	11111011	-94.125
11011001	-81.375	11111100	-94.5
11011010	-81.75	11111101	-94.875
11011011	-82.125	11111110	-95.25
11011100	-82.5	11111111	-95.625

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BEC  
 Figure 22. 80-Lead Low Profile Quad Flat Package [LQFP]  
 (ST-80-2)  
 Dimensions shown in millimeters

051706-A

ORDERING GUIDE

Model <sup>1,2</sup>	Temperature Range	Package Description	Package Option
ADAU1966WBSTZ	-40°C to +105°C	80-Lead LQFP	ST-80-2
ADAU1966WBSTZRL	-40°C to +105°C	80-Lead LQFP, 13" Tape and Reel	ST-80-2
EVAL-ADAU1966Z		Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.  
<sup>2</sup> W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADAU1966W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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[ES9218PQ](#) [PCM5122PWR](#) [PCM5142PWR](#) [PCM5242RHBR](#) [CS4361-CZZ](#) [AD1955ARSZ](#) [AD1866RZ-REEL](#) [AD1955ARSZRL](#)  
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