

Getting Started with the AD-DAC-FMC-ADP Adapter Board

INTRODUCTION

The ADC-DAC-FMC-ADP adapter board allows any of Analog Devices' DPG2-compatible High-Speed DAC Evaluation Boards to be used on a Xilinx® evaluation board with a FMC connector. The adapter board uses the Low Pin Count (LPC) version of the FMC connector, so it can be used on either LPC or HPC hosts (such as the ML605 or SP605).

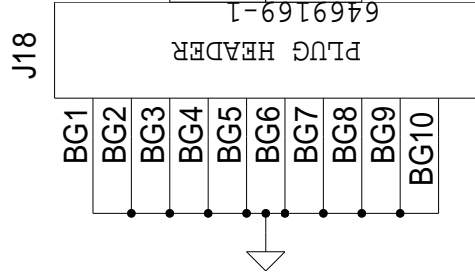
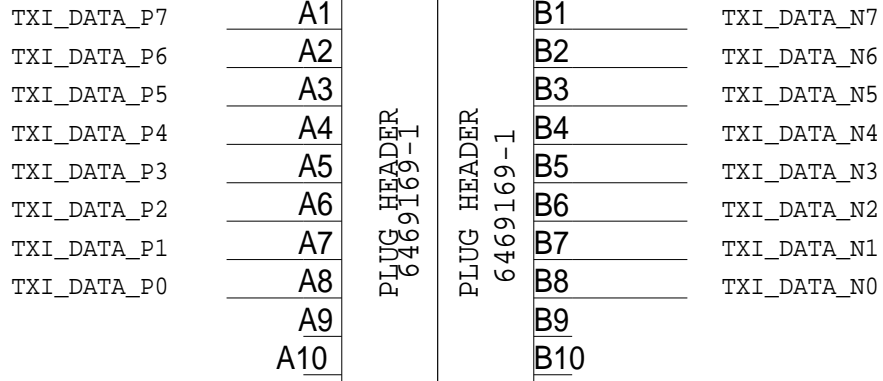
A list of DPG2-compatible evaluation boards can be found at <http://www.analog.com/dpg>

The schematic and layout are included in the following pages of this document. In addition, example UCF files for both the ML605 and SP605 are included as a starting point.

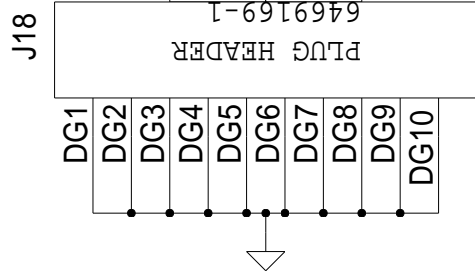
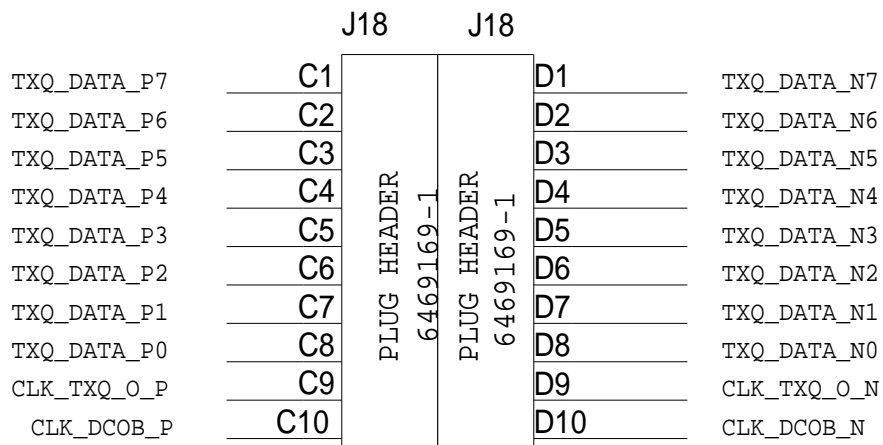
CLOCKING

Every DPG2-compatible evaluation board provides two LVDS clocks to the host. These two clocks are always identical in both frequency and phase. On DACs using an LVDS interface, the host is then expected to output two LVDS clocks that are phase aligned to the data. It is very important that these clocks be generated the same way as the data, so that any delays inside the FPGA are matched. Therefore, this clock should be considered another data bit with a fixed "10101" pattern.

B



A



C



B



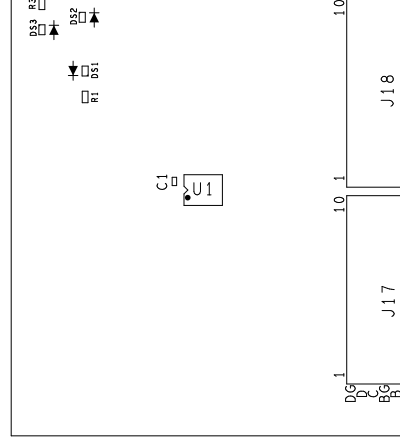
A

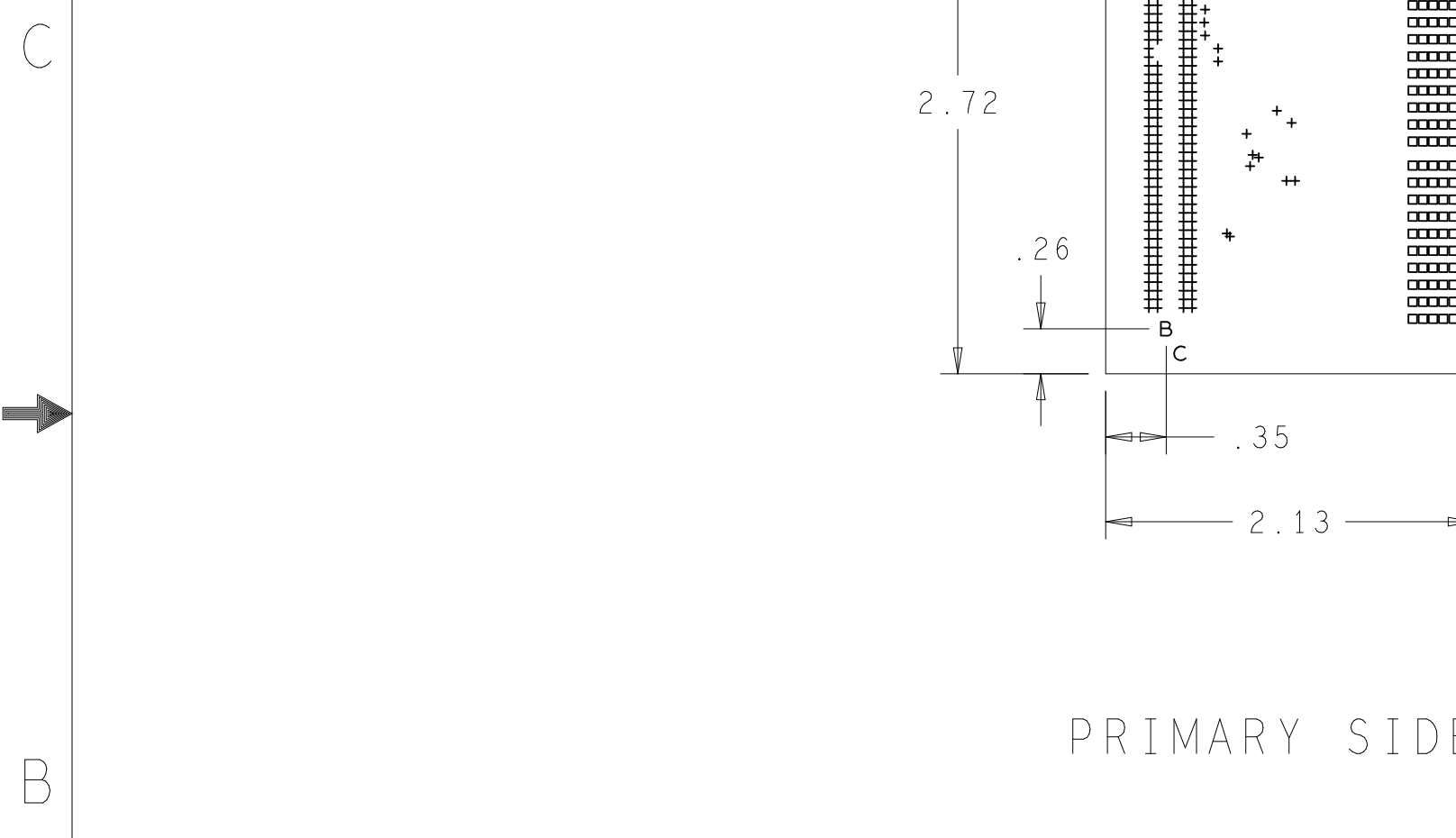
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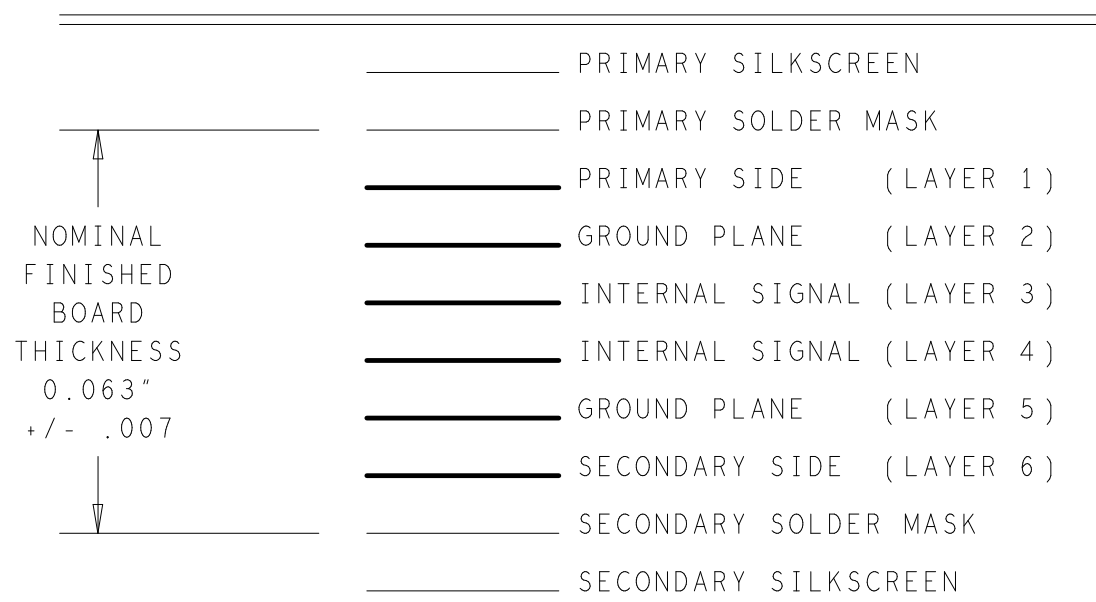
3

PRIMARY SIDE

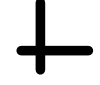
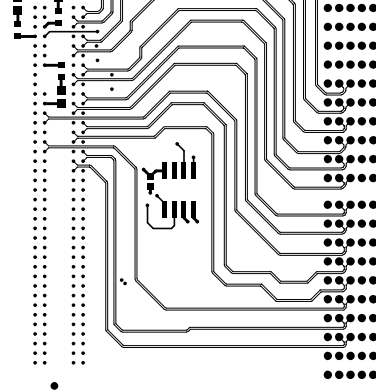


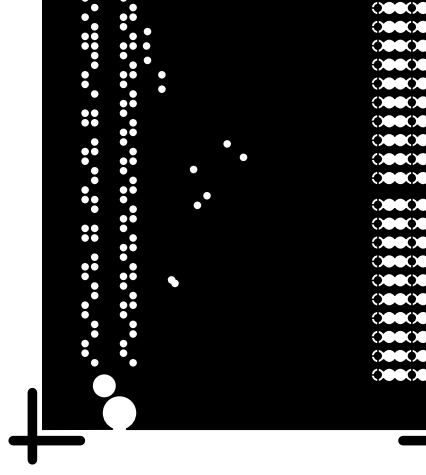


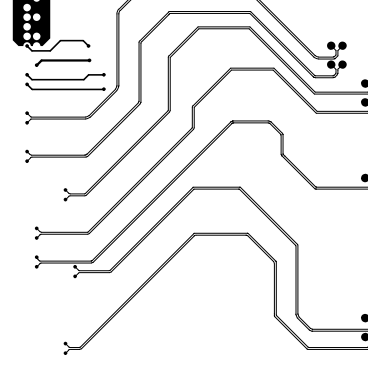
6 LAYER STACKUP

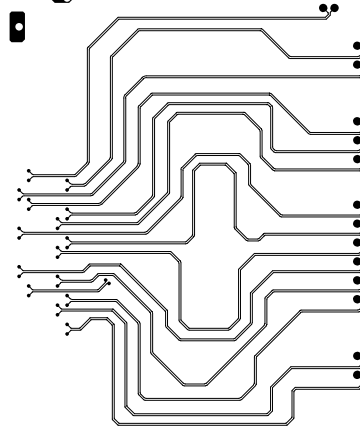


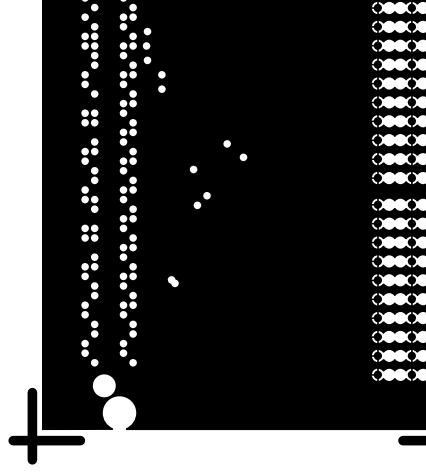
DIFFERENTIAL IMPEDANCE = 100 OHMS +/- 10%
 ARTWORK LINE WIDTH FOR
 IMPEDANCE CONTROLLED LINES = 0.005"

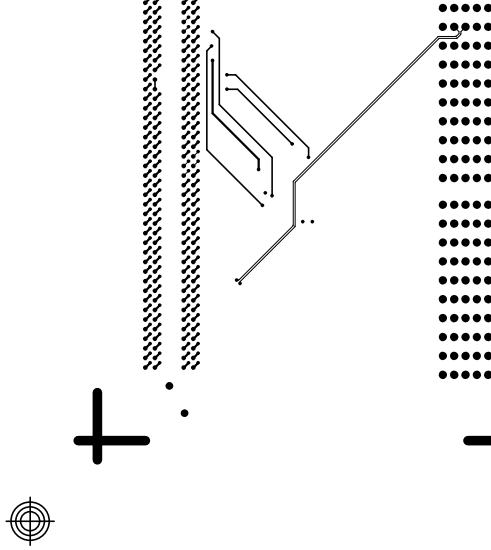














+

12V
P1
0.033
0.033
3.3V
3.3VAUX

C:1
S1



ANALOG DEVICES
AD-DAC-FMC
10033 REV

DG 1
C 1
P1
J17 1
J18 1.0

DEVICES
ANALOG



P1

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