# ANALOG DEVICES

# 6.8 GHz Wideband Synthesizer with Integrated VCO

Data Sheet

## ADF4356

## FEATURES

RF output frequency range: 53.125 MHz to 6800 MHz
   Integer channel: −227 dBc/Hz
   Fractional channel: −225 dBc/Hz
Integrated RMS jitter (1 kHz to 20 MHz): 97 fs for 6 GHz output
Fractional-N synthesizer and integer-N synthesizer
Pin compatible to the ADF4355
High resolution, 52-bit modulus
Phase frequency detector (PFD) operation to 125 MHz
Reference input frequency operation to 600 MHz
Maintains frequency lock over −40°C to +85°C
Low phase noise, voltage controlled oscillator (VCO)
Programmable divide by 1, 2, 4, 8, 16, 32, or 64 output
Analog and digital power supplies: 3.3 V
Charge pump and VCO power supplies: 5.0 V typical
Logic compatibility: 1.8 V
Programmable output power level
RF output mute function
Supported in the ADIsimPLL design tool

## APPLICATIONS

Wireless infrastructure (LTE, W-CDMA, TD-SCDMA,
   WiMAX, GSM, PCS, DCS)
Point to point/point to multipoint microwave links
Satellites/VSATs
Test equipment/instrumentation
Clock generation

## GENERAL DESCRIPTION

The ADF4356 allows implementation of fractional-N or integer-N phase-locked loop (PLL) frequency synthesizers when used with an external loop filter and an external reference frequency. A series of frequency dividers at another frequency output permits operation from 53.125 MHz to 6800 MHz.

The ADF4356 has an integrated VCO with a fundamental output frequency ranging from 3400 MHz to 6800 MHz. In addition, the VCO frequency is connected to divide by 1, 2, 4, 8, 16, 32, or 64 circuits that allow the user to generate RF output frequencies as low as 53.125 MHz. For applications that require isolation, the RF output stage can be muted. The mute function is both pin- and software-controllable.

Control of all on-chip registers is through a simple 3-wire interface. The ADF4356 operates with analog and digital power supplies ranging from 3.15 V to 3.45 V, with charge pump and VCO supplies from 4.75 V to 5.25 V. The ADF4356 also contains hardware and software power-down modes.
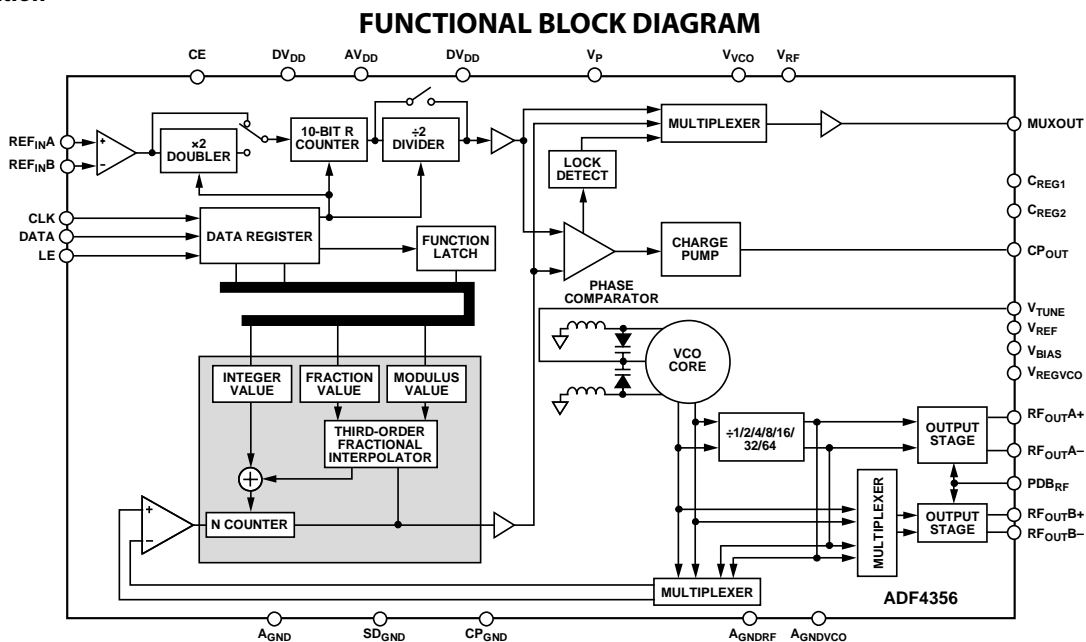
## FUNCTIONAL BLOCK DIAGRAM



Figure 1.

**Document Feedback**

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## REVISION HISTORY

## SPECIFICATIONS

$AV_{DD} = DV_{DD} = V_{RF} = 3.3\ V \pm 5\%$, $4.75\ V \le V_P = V_{VCO} \le 5.25\ V$, $A_{GND} = CP_{GND} = A_{GNDVCO} = SD_{GND} = A_{GNDRF} = 0\ V$, $R_{SET} = 5.1\ k\Omega$, dBm referred to 50 Ω, $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| REF$_{IN}$A/REF$_{IN}$B CHARACTERISTICS | | | | | | |
| Input Frequency Range | | | | | | For f < 10 MHz, ensure slew rate > 21 V/μs |
| Single-Ended Mode | | 10 | | 250 | MHz | |
| Differential Mode | | 10 | | 600 | MHz | |
| Input Sensitivity | | | | | | |
| Single-Ended Mode | | 0.4 | | AV$_{DD}$ | V p-p | REF$_{IN}$A biased at AV$_{DD}$/2; ac coupling ensures AV$_{DD}$/2 bias |
| Differential Mode | | 0.4 | | 1.8 | V p-p | LVDS and LVPECL compatible, REF$_{IN}$A/ REF$_{IN}$B biased at 2.1 V; ac coupling ensures 2.1 V bias |
| Input Capacitance | | | | | | |
| Single-Ended Mode | | | 6.9 | | pF | |
| Differential Mode | | | 1.4 | | pF | |
| Input Current | | | | ±100 | μA | Single-ended reference programmed |
| | | | | ±250 | μA | Differential reference programmed |
| Phase Frequency Detector | | | | 125 | MHz | |
| CHARGE PUMP (CP) | | | | | | |
| CP Current, Sink/Source | I$_{CP}$ | | | | | R$_{SET}$ = 5.1 kΩ, this resistor is internal in the ADF4356 |
| High Value | | | 4.8 | | mA | |
| Low Value | | | 0.3 | | mA | |
| R$_{SET}$ Range | | | 5.1 | | kΩ | Fixed |
| Current Matching | | | 3 | | % | $0.5\ V \le V_{CP}{}^{1} \le V_P - 0.5\ V$ |
| I$_{CP}$ vs. V$_{CP}$ | | | 3 | | % | $0.5\ V \le V_{CP}{}^{1} \le V_P - 0.5\ V$ |
| I$_{CP}$ vs. Temperature | | | 1.5 | | % | $V_{CP}{}^{1}$ = 2.5 V |
| LOGIC INPUTS | | | | | | |
| Input Voltage | | | | | | |
| High | V$_{INH}$ | 1.5 | | DV$_{DD}$ | V | |
| Low | V$_{INL}$ | | | 0.6 | V | |
| Input Current | I$_{INH}$/I$_{INL}$ | | | ±1 | μA | |
| Input Capacitance | C$_{IN}$ | | 3.0 | | pF | |
| LOGIC OUTPUTS | | | | | | |
| Output High Voltage | V$_{OH}$ | DV$_{DD}$ − 0.4 | | | V | |
| | | 1.5 | 1.8 | | V | 1.8 V output selected |
| Output High Current | I$_{OH}$ | | | 500 | μA | |
| Output Low Voltage | V$_{OL}$ | | | 0.4 | V | I$_{OL}$[2] = 500 μA |
| POWER SUPPLIES | | | | | | See Table 7 and Table 8 |
| Analog Power | AV$_{DD}$ | 3.15 | 3.3 | 3.45 | V | |
| Digital Power and RF Supply Voltage | DV$_{DD}$, V$_{RF}$ | | AV$_{DD}$ | | | Voltages must equal AV$_{DD}$ |
| CP and VCO Supply Voltage | V$_P$, V$_{VCO}$ | 4.75 | 5.0 | 5.25 | V | V$_P$ must equal V$_{VCO}$ |
| CP Supply Power Current | I$_P$ | | 8 | 9 | | |
| DI$_{DD}$ + AI$_{DD}$[3] | | | 82 | 92 | mA | |
| Output Dividers | | | 6 to 36 | | mA | Each output divide by 2 consumes 6 mA |
| Supply Current | I$_{VCO}$ | | 70 | 90 | mA | |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| RF$_{OUT}$A+/RF$_{OUT}$A−Supply Current | I$_{RF_{OUT}x\pm}$ | | | | | RF Output A enabled/RF Output B disabled |
| | | | 22 | 27 | mA | −4 dBm setting |
| | | | 33 | 38 | mA | −1 dBm setting |
| | | | 44 | 49 | mA | 2 dBm setting |
| | | | 55 | 60 | mA | 5 dBm setting |
| RF$_{OUT}$A+/RF$_{OUT}$A− Plus RF$_{OUT}$B+/RF$_{OUT}$B− Supply Current | I$_{RF_{OUT}x\pm}$ | | | | | RF Output A enabled/RF Output B enabled |
| | | | 48 | 56 | mA | −4 dBm setting |
| | | | 65 | 74 | mA | −1 dBm setting |
| | | | 82 | 91 | mA | 2 dBm setting |
| | | | 99 | 108 | mA | 5 dBm setting |
| Low Power Sleep Mode | | | 5 | | mA | Hardware power-down selected |
| | | | 20 | | mA | Software power-down selected |
| RF OUTPUT CHARACTERISTICS | | | | | | |
| VCO Frequency Range | | 3400 | | 6800 | MHz | Fundamental VCO range |
| RF Output Frequency | | 53.125 | | 6800 | MHz | |
| VCO Sensitivity | K$_V$ | | 25 | | MHz/V | |
| Frequency Pushing (Open-Loop) | | | 12 | | MHz/V | |
| Frequency Pulling (Open-Loop) | | | 0.5 | | MHz | Voltage standing wave ratio (VSWR) = 2:1 RF$_{OUT}$A+/RF$_{OUT}$A− |
| Harmonic Content | | | | | | |
| Second | | | −26 | | dBc | Fundamental VCO output (RF$_{OUT}$A+) |
| | | | −29 | | dBc | Divided VCO output (RF$_{OUT}$A+) |
| Third | | | −32 | | dBc | Fundamental VCO output (RF$_{OUT}$A+) |
| | | | −14 | | dBc | Divided VCO output (RF$_{OUT}$A+) |
| RF Output A Power[4] | | | 7 | | dBm | RF$_{OUT}$A+ = 1 GHz; 7.4 nH inductor to V$_{RF}$ |
| | | | −2 | | dBm | RF$_{OUT}$A+ = 6.8 GHz; 7.4 nH inductor to V$_{RF}$ |
| Power Variation | | | ±1 | | dB | RF$_{OUT}$A+ = 5 GHz |
| Power Variation over Frequency | | | ±5 | | dB | RF$_{OUT}$A+ = 1 GHz to 6.8 GHz |
| RF Output B Power[4] | | | 4 | | dBm | RF$_{OUT}$B+ = 1 GHz; 7.4 nH inductor to V$_{RF}$ |
| | | | −2 | | dBm | RF$_{OUT}$B+ = 6.8 GHz; 7.4 nH inductor to V$_{RF}$ |
| Power Variation | | | ±1 | | dB | RF$_{OUT}$B+ = 5 GHz |
| Power Variation over Frequency | | | ±5 | | | RF$_{OUT}$B+ = 1 GHz to 6.8 GHz |
| Level of Signal with RF Output Disabled | | | −53 | | dBm | RF$_{OUT}$A+ = 1 GHz |
| | | | −20 | | dBm | RF$_{OUT}$A+= 6.8 GHz |
| NOISE CHARACTERISTICS | | | | | | |
| Fundamental VCO Phase Noise Performance | | | | | | VCO noise in open-loop conditions |
| | | | −115 | | dBc/Hz | 100 kHz offset from 3.4 GHz carrier |
| | | | −135 | | dBc/Hz | 800 kHz offset from 3.4 GHz carrier |
| | | | −137 | | dBc/Hz | 1 MHz offset from 3.4 GHz carrier |
| | | | −155 | | dBc/Hz | 10 MHz offset from 3.4 GHz carrier |
| | | | −113 | | dBc/Hz | 100 kHz offset from 5.0 GHz carrier |
| | | | −133 | | dBc/Hz | 800 kHz offset from 5.0 GHz carrier |
| | | | −135 | | dBc/Hz | 1 MHz offset from 5.0 GHz carrier |
| | | | −153 | | dBc/Hz | 10 MHz offset from 5.0 GHz carrier |
| | | | −110 | | dBc/Hz | 100 kHz offset from 6.8 GHz carrier |
| | | | −130 | | dBc/Hz | 800 kHz offset from 6.8 GHz carrier |
| | | | −132 | | dBc/Hz | 1 MHz offset from 6.8 GHz carrier |
| | | | −150 | | dBc/Hz | 10 MHz offset from 6.8 GHz carrier |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| Normalized In-Band Phase Noise Floor | | | | | | |
|    Fractional Channel[5] | | | −225 | | dBc/Hz | |
|    Integer Channel[6] | | | −227 | | dBc/Hz | |
|    Normalized 1/f Noise, $PN_{1\_f}$[7] | | | −121 | | dBc/Hz | 10 kHz offset; normalized to 1 GHz |
| Integrated RMS Jitter (1 kHz to 20 MHz)[8] | | | 97 | | fs | |
| Spurious Signals Due to PFD Frequency | | | −85 | | dBc | |

[1] $V_{CP}$ is the voltage at the $CP_{OUT}$ pin.
[2] $I_{OL}$ is the output low current.
[3] $T_A$ = 25°C; $AV_{DD}$ = $DV_{DD}$ = $V_{RF}$ = 3.3 V; $V_{VCO}$ = $V_P$ = 5.0 V; prescaler = 4/5; $f_{REFIN}$ = 122.88 MHz; $f_{PFD}$ = 61.44 MHz; and $f_{RF}$ = 1650 MHz.
[4] RF output power using the EV-ADF4356SD1Z evaluation board is measured into a spectrum analyzer. Unused RF output pins are terminated in 50 Ω.
[5] Use this value to calculate the phase noise for any application. To calculate in-band phase noise performance as seen at the VCO output, use the following formula: −225 + 10log($f_{PFD}$) + 20logN. The value given is the lowest noise mode for the fractional channel.
[6] Use this value to calculate the phase noise for any application. To calculate in-band phase noise performance as seen at the VCO output, use the following formula: −227 + 10log($f_{PFD}$) + 20logN. The value given is the lowest noise mode for the integer channel.
[7] The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency ($f_{RF}$) and at a frequency offset (f) is given by PN = $P_{1\_f}$ + 10log(10 kHz/f) + 20log($f_{RF}$/1 GHz). Both the normalized phase noise floor and flicker noise are modeled in the ADIsimPLL design tool.
[8] Integrated RMS jitter using the EV-ADF4356SD1Z evaluation board is measured into a spectrum analyzer. The EV-ADF4356SD1Z evaluation board is configured to accept a single ended REFIN (SMA 100) = 160 MHz, VCO frequency = 6 GHz, PFD frequency = 80 MHz, charge pump current = 0.9 mA, and bleed current is off. The loop filter is configured for an 80 kHz loop filter bandwidth. Unused RF output pins are terminated in 50 Ω.

## TIMING CHARACTERISTICS

$AV_{DD}$ = $DV_{DD}$ = $V_{RF}$ = 3.3 V ± 5%, 4.75 V ≤ $V_P$ = $V_{VCO}$ ≤ 5.25 V, $A_{GND}$ = $CP_{GND}$ = $A_{GNDVCO}$ = $SD_{GND}$ = $A_{GNDRF}$ = 0 V, $R_{SET}$ = 5.1 kΩ, dBm referred to 50 Ω, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 2. Write Timing**

| Parameter | Limit | Unit | Description |
|---|---|---|---|
| $f_{CLK}$ | 50 | MHz max | Serial peripheral interface CLK frequency |
| $t_1$ | 10 | ns min | LE setup time |
| $t_2$ | 5 | ns min | DATA to CLK setup time |
| $t_3$ | 5 | ns min | DATA to CLK hold time |
| $t_4$ | 10 | ns min | CLK high duration |
| $t_5$ | 10 | ns min | CLK low duration |
| $t_6$ | 10 | ns min | CLK to LE setup time |
| $t_7$ | 20 or (2/$f_{PFD}$), whichever is longer | ns min | LE pulse width |

### Write Timing Diagram
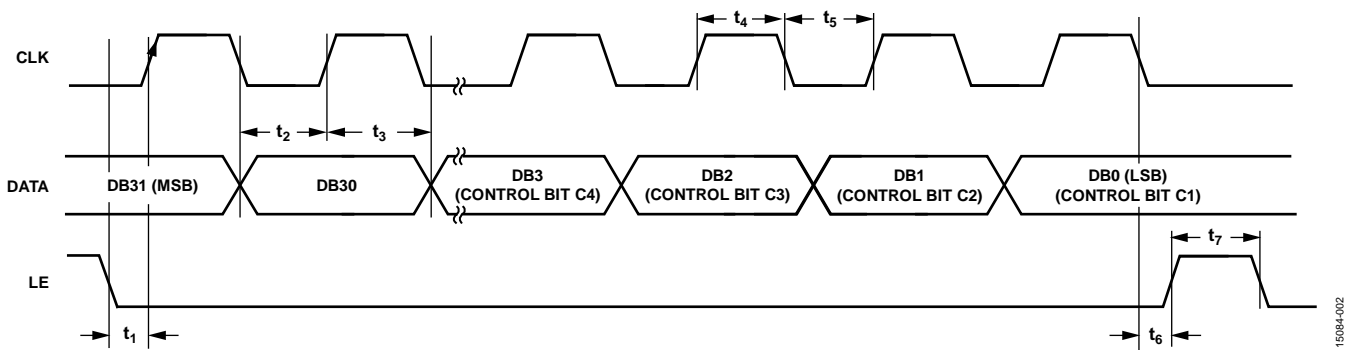


*Figure 2. Write Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$, unless otherwise noted.

**Table 3.**

| Parameter | Rating |
|---|---|
| $V_{RF}$, $DV_{DD}$, $AV_{DD}$ to GND[1] | −0.3 V to +3.6 V |
| $AV_{DD}$ to $DV_{DD}$ | −0.3 V to +0.3 V |
| $V_P$, $V_{VCO}$ to GND[1] | −0.3 V to +5.8 V |
| $CP_{OUT}$ to GND[1] | −0.3 V to $V_P$ + 0.3 V |
| Digital Input/Output Voltage to GND[1] | −0.3 V to $DV_{DD}$ + 0.3 V |
| Analog Input/Output Voltage to GND[1] | −0.3 V to $AV_{DD}$ + 0.3 V |
| $REF_{IN}A$, $REF_{IN}B$ to GND[1] | −0.3 V to $AV_{DD}$ + 0.3 V |
| $REF_{IN}A$ to $REF_{IN}B$ | ±2.1 V |
| Operating Temperature Range | −40°C to +85°C |
| Storage Temperature Range | −65°C to +125°C |
| Maximum Junction Temperature | 150°C |
| Reflow Soldering | |
| Peak Temperature | 260°C |
| Time at Peak Temperature | 40 sec |
| Electrostatic Discharge (ESD) | |
| Charged Device Model | 1000 V |
| Human Body Model | 2000 V |

[1] GND = $A_{GND}$ = $SD_{GND}$ = $A_{GNDRF}$ = $A_{GNDVCO}$ = $CP_{GND}$ = 0 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

The ADF4356 is a high performance RF integrated circuit with an ESD rating of 2 kV and is ESD sensitive. Take proper precautions for handling and assembly.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

**Table 4. Thermal Resistance**

| Package Type | $θ_{JA}$ | Unit |
|---|---|---|
| CP-32-12[1] | 27.3 | °C/W |

[1] Test Condition 1: thermal impedance simulated values are based on use of a PCB with the thermal impedance paddle soldered to GND[1].

## TRANSISTOR COUNT

The transistor count for the ADF4356 is 134,486 (CMOS) and 3874 (bipolar).

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS
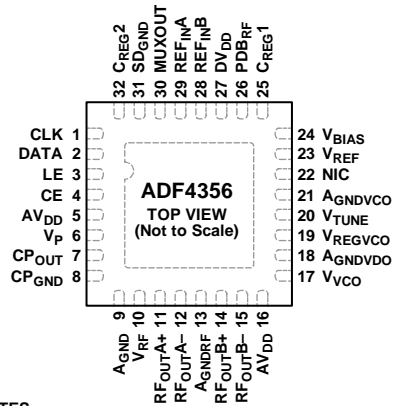


NOTES
1. NIC = NOT INTERNALLY CONNECTED.
2. THE EXPOSED PAD MUST BE CONNECTED TO $A_{GND}$.

*Figure 3. Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | CLK | Serial Clock Input. Data is clocked into the 32-bit shift register on the CLK rising edge. This input is a high impedance CMOS input. |
| 2 | DATA | Serial Data Input. The serial data is loaded most significant bit (MSB) first with the four LSBs as the control bits. This input is a high impedance CMOS input. |
| 3 | LE | Load Enable, CMOS Input. When LE goes high, the data stored in the shift register is loaded into the register that is selected by the four LSBs. |
| 4 | CE | Chip Enable. A logic low on this pin powers down the device and puts the charge pump into three-state mode. A logic high on this pin powers up the device, depending on the status of the power-down bits. |
| 5, 16 | $AV_{DD}$ | Analog Power Supplies. These pins range from 3.15 V to 3.45 V. Connect decoupling capacitors to the analog ground plane as close to these pins as possible. $AV_{DD}$ must have the same value as $DV_{DD}$. |
| 6 | $V_P$ | Charge Pump Power Supply. $V_P$ must have the same value as $V_{VCO}$. Connect decoupling capacitors to the ground plane as close to this pin as possible. |
| 7 | $CP_{OUT}$ | Charge Pump Output. When enabled, this output provides $\pm I_{CP}$ to the external loop filter. The output of the loop filter is connected to $V_{TUNE}$ to drive the internal VCO. |
| 8 | $CP_{GND}$ | Charge Pump Ground. This output is the ground return pin for $CP_{OUT}$. |
| 9 | $A_{GND}$ | Analog Ground. This pin is the ground return pin for $AV_{DD}$. |
| 10 | $V_{RF}$ | Power Supply for the RF Output. Connect decoupling capacitors to the analog ground plane as close to this pin as possible. $V_{RF}$ must have the same value as $AV_{DD}$. |
| 11 | $RF_{OUT}A+$ | VCO Output. The output level is programmable. The VCO fundamental output or a divided down version is available. |
| 12 | $RF_{OUT}A-$ | Complementary VCO Output. The output level is programmable. The VCO fundamental output or a divided down version is available. |
| 13 | $A_{GNDRF}$ | RF Output Stage Ground. This pin is the ground return pin for the RF output stage. |
| 14 | $RF_{OUT}B+$ | Auxiliary VCO Output. The output level is programmable. The VCO fundamental output or a divided down version is available. |
| 15 | $RF_{OUT}B-$ | Complementary Auxiliary VCO Output. The output level is programmable. The VCO fundamental output or a divided down version is available. |
| 17 | $V_{VCO}$ | Power Supply for the VCO. The voltage on this pin ranges from 4.75 V to 5.25 V. Place decoupling capacitors to the analog ground plane as close to this pin as possible. |
| 18, 21 | $A_{GNDVCO}$ | VCO Ground. This pin is the ground return path for the VCO. |
| 19 | $V_{REGVCO}$ | VCO Compensation Node. Connect decoupling capacitors to the ground plane as close to this pin as possible. Connect $V_{REGVCO}$ directly to $V_{VCO}$. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 20 | $V_{TUNE}$ | Control Input to the VCO. This voltage determines the output frequency and is derived from filtering the $CP_{OUT}$ output voltage. The capacitance at this pin ($V_{TUNE}$ input capacitance) is 9 pF. |
| 22 | NIC | No Internal Connection. For existing designs that currently use the ADF4355, to upgrade to the ADF4356, the $R_{SET}$ resistor can be left connected to this pin. |
| 23 | $V_{REF}$ | Internal Compensation Node. DC biased at half the tuning range. Connect decoupling capacitors to the ground plane as close to this pin as possible. |
| 24 | $V_{BIAS}$ | Reference Voltage. Connect a 100 nF decoupling capacitor to the ground plane as close to this pin as possible. |
| 25, 32 | $C_{REG}1, C_{REG}2$ | Outputs from the LDO Regulator. $C_{REG}1$ and $C_{REG}2$ are the supply voltages to the digital circuits. Nominal voltage of 1.8 V. Decoupling capacitors of 100 nF connected to $A_{GND}$ are required for these pins. |
| 26 | $PDB_{RF}$ | RF Power-Down. A logic low on this pin mutes the RF outputs. This mute function is also software-controllable. Do not leave this pin floating. |
| 27 | $DV_{DD}$ | Digital Power Supply. This pin must be at the same voltage as $AV_{DD}$. Place decoupling capacitors to the ground plane as close to this pin as possible. |
| 28 | $REF_{IN}B$ | Complementary Reference Input. If unused, ac couple this pin to $A_{GND}$. |
| 29 | $REF_{IN}A$ | Reference Input. |
| 30 | MUXOUT | Multiplexer Output. The multiplexer output allows the digital lock detect, the analog lock detect, scaled RF, or the scaled reference frequency to be externally accessible. |
| 31 | $SD_{GND}$ | Digital Σ-Δ Modulator Ground. $SD_{GND}$ is the ground return path for the Σ-Δ modulator. |
|  | EP | Exposed Pad. The exposed pad must be connected to $A_{GND}$. |

# TYPICAL PERFORMANCE CHARACTERISTICS
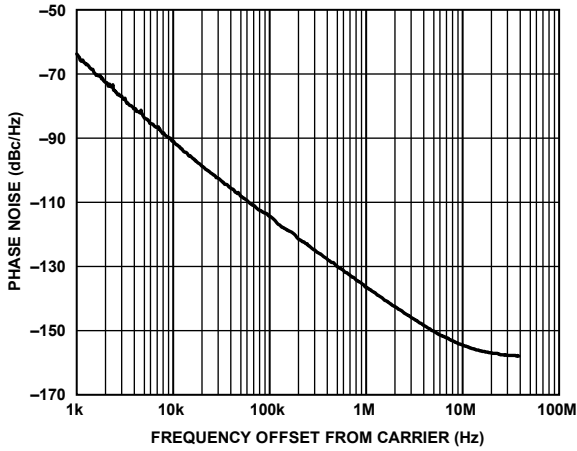


*Figure 4. Open-Loop VCO Phase Noise, 3.4 GHz*



*Figure 5. Open-Loop VCO Phase Noise, 5.0 GHz*



*Figure 6. Open-Loop VCO Phase Noise, 6.8 GHz*



*Figure 7. Closed-Loop Phase Noise, RF_OUTB+ (100 nH Inductors), Fundamental VCO and Dividers, VCO = 3.4 GHz, PFD = 61.44 MHz, Loop Bandwidth = 40 kHz*



*Figure 8. Closed-Loop Phase Noise, RF_OUTB+ (100 nH Inductors), Fundamental VCO and Dividers, VCO = 5.0 GHz, PFD = 61.44 MHz, Loop Bandwidth = 40 kHz*
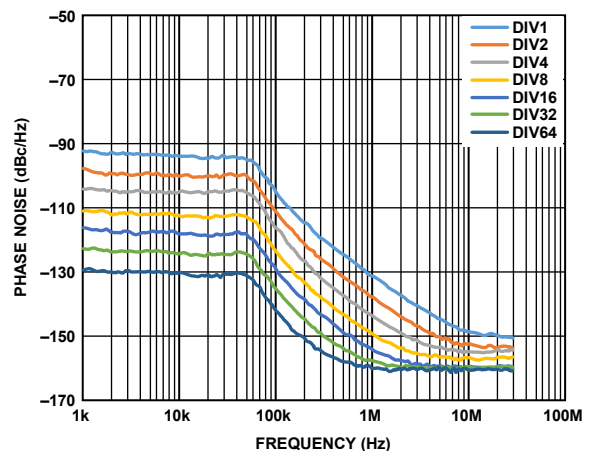


*Figure 9. Closed-Loop Phase Noise, RF_OUTB+ (100 nH Inductors), Fundamental VCO and Dividers, VCO = 6.8 GHz, PFD = 61.44 MHz, Loop Bandwidth = 40 kHz*
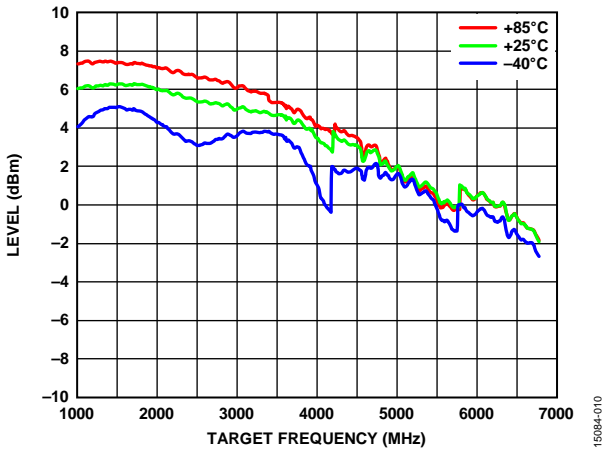
Figure 10. Output Power vs. Frequency, RF<sub>OUT</sub>A+/RF<sub>OUT</sub>A– (7.4 nH Inductors, 10 pF AC Coupling Capacitors, Board Measurement)



Figure 11. RF<sub>OUT</sub>A+/RF<sub>OUT</sub>A– Harmonics vs. Frequency (7.4 nH Inductors, 10 pF AC Coupling Capacitors, Board Measurement)



Figure 12. RF<sub>OUT</sub>B+/RF<sub>OUT</sub>B– Power vs. Frequency (100 nH Inductors, 10 pF AC Coupling Capacitors, Board Measurement)



Figure 13. RF<sub>OUT</sub>A+/RF<sub>OUT</sub>A– Power vs. RF<sub>OUT</sub>B+/RF<sub>OUT</sub>B– Power (7.4 nH Inductors, 10 pF AC Coupling Capacitors, Board Measurement)



Figure 14. RMS Jitter/Noise vs. Output Frequency, PFD Frequency = 61.44 MHz, Loop Filter = 40 kHz
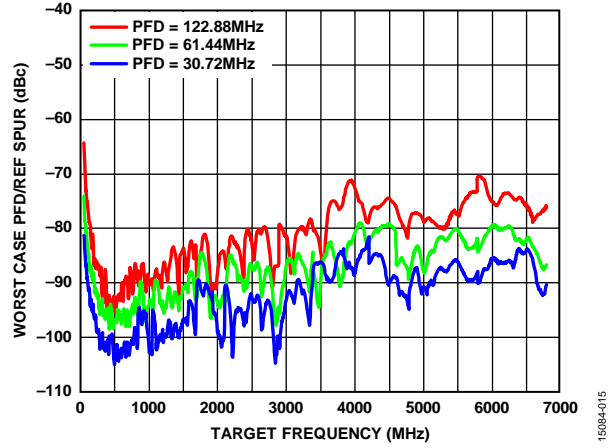


Figure 15. PFD Spur Amplitude vs. RF<sub>OUT</sub>A+/RF<sub>OUT</sub>A– Output Frequency, PFD = 30.72 MHz, PFD = 61.44 MHz, PFD = 122.88 MHz, Loop Filter = 40 kHz

**ADF4356**
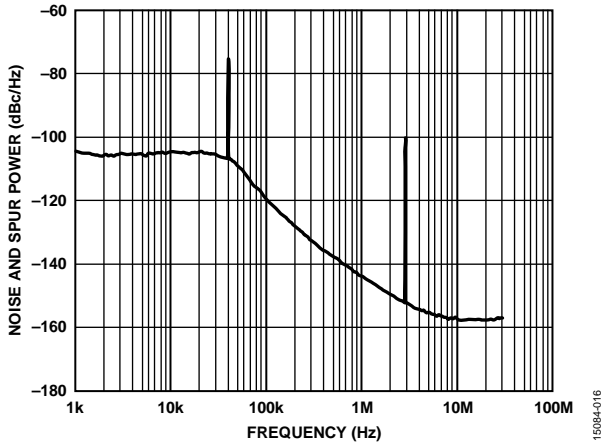


Figure 16. Fractional-N Spur Performance, GSM1800 Band, $RF_{OUT}A+ = 1550.2$ MHz, $REF_{IN} = 122.88$ MHz, PFD = 61.44 MHz, Output Divide by 4 Selected, Loop Filter Bandwidth = 40 kHz, Channel Spacing = 20 kHz
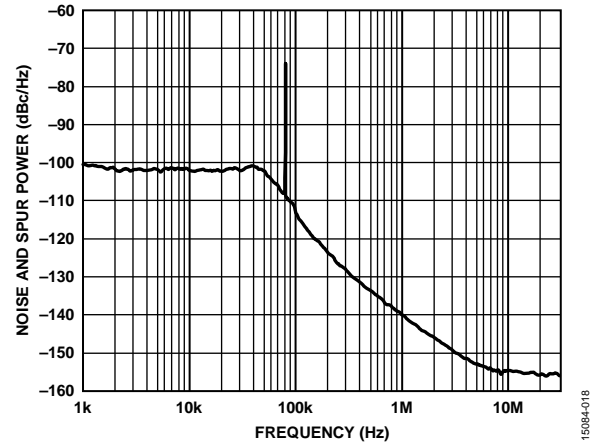


Figure 18. Fractional-N Spur Performance, $RF_{OUT}A+ = 2.591$ GHz, $REF_{IN} = 122.88$ MHz, PFD = 61.44 MHz, Output Divide by 2 Selected, Loop Filter Bandwidth = 40 kHz, Channel Spacing = 20 kHz
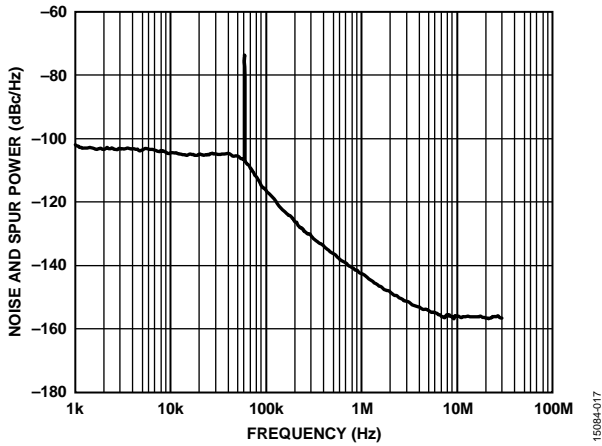


Figure 17. Fractional-N Spur Performance, W-CDMA Band, $RF_{OUT}A+ = 2113.5$ MHz, $REF_{IN} = 122.88$ MHz, PFD = 61.44 MHz, Output Divide by 2 Selected, Loop Filter Bandwidth = 40 kHz, Channel Spacing = 20 kHz
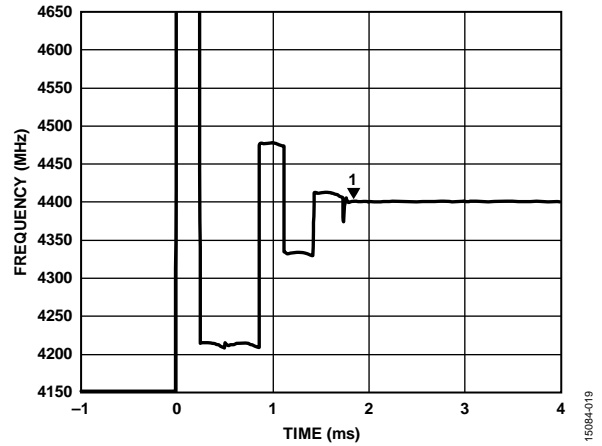


Figure 19. Lock Time for 250 MHz Jump from 4150 MHz to 4400 MHz, Loop Bandwidth = 23 kHz

# THEORY OF OPERATION

## REFERENCE INPUT SECTION

Figure 20 shows the reference input stage. The reference input can accept both single-ended and differential signals. Use the reference mode bit (Register 4, Bit DB9) to select the signal. To use a differential signal on the reference input, program this bit high. In this case, SW1 and SW2 are open, SW3 and SW4 are closed, and the current source that drives the differential pair of transistors switches on. The differential signal buffers and provides an emitter-coupled logic (ECL) to the CMOS converter. When a single-ended signal is used as the reference, program Bit DB9 in Register 4 to 0. Connect the single-ended reference signal to REF$_{IN}$A. In this case, SW1 and SW2 are closed, SW3 and SW4 are open, and the current source that drives the differential pair of transistors switches off.
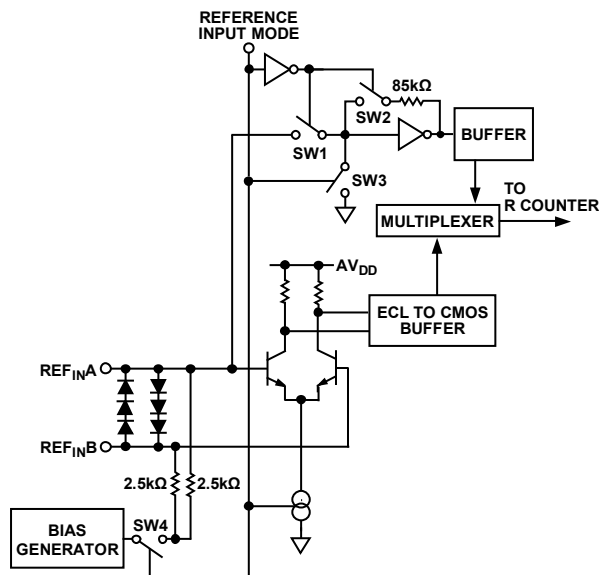


Figure 20. Reference Input Stage, Differential Mode

## RF N DIVIDER

The RF N divider allows a division ratio in the PLL feedback path. Determine the division ratio by the INT, FRAC1, FRAC2, and MOD2 values that this divider comprises.
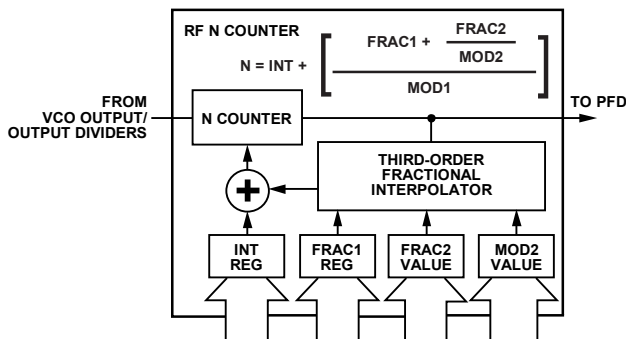


Figure 21. RF N Divider

### INT, FRACx, MODx, and R Counter Relationship

The INT, FRAC1, FRAC2, MOD1, and MOD2 values, in conjunction with the R counter, make it possible to generate output frequencies spaced by fractions of the PFD frequency (f$_{PFD}$). For more information, see the RF Synthesizer—A Worked Example section.

Calculate the RF VCO frequency (VCO$_{OUT}$) by

$$VCO_{OUT} = f_{PFD} \times N \qquad (1)$$

where:
$VCO_{OUT}$ is the output frequency of the VCO (without using the output divider).
$f_{PFD}$ is the frequency of the phase frequency detector.
$N$ is the desired value of the feedback counter, N.

Calculate f$_{PFD}$ by

$$f_{PFD} = REF_{IN} \times ((1 + D)/(R \times (1 + T))) \qquad (2)$$

where:
$REF_{IN}$ is the reference input frequency.
$D$ is the $REF_{IN}$ doubler bit.
$R$ is the preset divide ratio of the binary 10-bit programmable reference counter (1 to 1023).
$T$ is the $REF_{IN}$ divide by 2 bit (0 or 1).

N comprises

$$N = INT + \frac{FRAC1 + \dfrac{FRAC2}{MOD2}}{MOD1} \qquad (3)$$

where:
$INT$ is the 16-bit integer value (23 to 32,767 for the 4/5 prescaler, and 75 to 65,535 for the 8/9 prescaler).
$FRAC1$ is the numerator of the primary modulus (0 to 16,777,215).
$FRAC2$ is the numerator of the 28-bit auxiliary modulus (0 to 268,435,455).
$MOD2$ is the programmable, 28-bit auxiliary fractional modulus (2 to 268,435,455).
$MOD1$ is a 24-bit primary modulus with a fixed value of $2^{24}$ = 16,777,216.

Equation 3 results in a very fine frequency resolution with no residual frequency error. To apply this formula, take the following steps:

1. Calculate N by dividing VCO$_{OUT}$/f$_{PFD}$.
2. The integer value of this number forms INT.
3. Subtract the INT value from the full N value.
4. Multiply the remainder by $2^{24}$.
5. The integer value of this number forms FRAC1.
6. Calculate MOD2 based on the channel spacing (f$_{CHSP}$) by

$$MOD2 = f_{PFD}/GCD(f_{PFD}, f_{CHSP}) \qquad (4)$$

where:
$GCD(f_{PFD}, f_{CHSP})$ is the greatest common divider of the PFD frequency and the channel spacing frequency.
$f_{CHSP}$ is the desired channel spacing frequency.

7. Calculate FRAC2 by the following equation:

$$FRAC2 = ((N - INT) \times 2^{24} - FRAC1)) \times MOD2 \qquad (5)$$

The FRAC2 and MOD2 fraction results in outputs with zero frequency error for channel spacings when

$$f_{PFD}/GCD(f_{PFD}/f_{CHSP}) < 268,435,455 \qquad (6)$$

where:
$f_{PFD}$ is the frequency of the phase frequency detector.
GCD is a greatest common denominator function.
$f_{CHSP}$ is the desired channel spacing frequency.

If zero frequency error is not required, the MOD1 and MOD2 denominators operate together to create a 52-bit resolution modulus.

### INT N Mode

When FRAC1 and FRAC2 are 0, the synthesizer operates in integer-N mode.

### R Counter

The 10-bit R counter allows the input reference frequency ($REF_{IN}$) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 1023 are allowed.

## PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 22 is a simplified schematic of the phase frequency detector. The PFD includes a fixed delay element that sets the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and provides a consistent reference spur level. Set the phase detector polarity to positive on this device because of the positive tuning of the VCO.
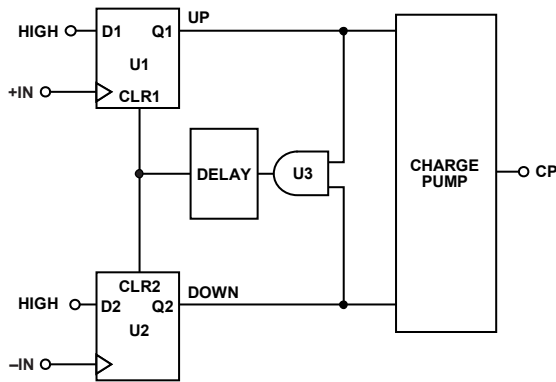
Figure 22. PFD Simplified Schematic

## MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4356 allows the user to access various internal points on the chip. The M3, M2, and M1 bits in Register 4 control the state of MUXOUT. Figure 23 shows the MUXOUT section in block diagram form.
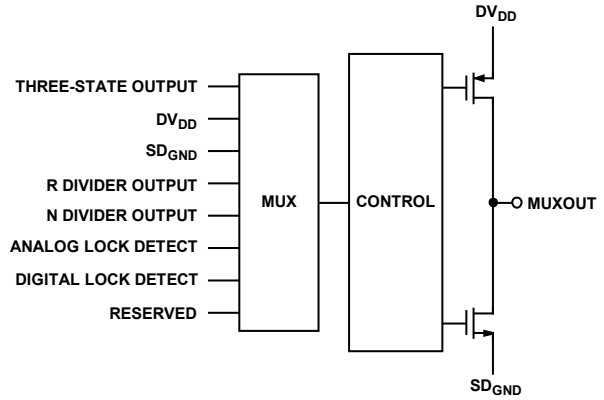
Figure 23. MUXOUT Schematic

## INPUT SHIFT REGISTERS

The ADF4356 digital section includes a 10-bit R counter, a 16-bit RF integer-N counter, a 24-bit FRAC1 counter, a 28-bit auxiliary fractional counter, and a 28-bit auxiliary modulus counter. Data clocks into the 32-bit shift register on each rising edge of CLK. The data clocks in MSB first. Data transfers from the shift register to one of 13 latches on the rising edge of LE. The state of the four control bits (C4, C3, C2, and C1) in the shift register determines the destination latch. As shown in Figure 2, the four least significant bits (LSBs) are DB3, DB2, DB1, and DB0. The truth table for these bits is shown in Table 6. Figure 26 and Figure 27 summarize the programming of the latches.

Table 6. Truth Table for the C4, C3, C2, and C1 Control Bits

| Control Bits | | | | |
|---|---|---|---|---|
| C4 | C3 | C2 | C1 | Register |
| 0 | 0 | 0 | 0 | Register 0 |
| 0 | 0 | 0 | 1 | Register 1 |
| 0 | 0 | 1 | 0 | Register 2 |
| 0 | 0 | 1 | 1 | Register 3 |
| 0 | 1 | 0 | 0 | Register 4 |
| 0 | 1 | 0 | 1 | Register 5 |
| 0 | 1 | 1 | 0 | Register 6 |
| 0 | 1 | 1 | 1 | Register 7 |
| 1 | 0 | 0 | 0 | Register 8 |
| 1 | 0 | 0 | 1 | Register 9 |
| 1 | 0 | 1 | 0 | Register 10 |
| 1 | 0 | 1 | 1 | Register 11 |
| 1 | 1 | 0 | 0 | Register 12 |
| 1 | 1 | 0 | 1 | Register 13 |

## PROGRAM MODES

Table 6 and Figure 28 through Figure 41 show how the program modes must be set up for the ADF4356.

The following settings in the ADF4356 are double-buffered: main fractional value (FRAC1), auxiliary modulus value (MOD2), auxiliary fractional value (FRAC2), reference doubler, reference divide by 2 (RDIV2), R counter value, and charge pump current setting. Two events must occur before the ADF4356 uses a new value for any of the double-buffered settings. First, the new value must latch into the device by writing to the appropriate register, and second, a new write to Register 0 must be performed.

For example, to ensure that the modulus value loads correctly, every time that the modulus value updates, Register 0 must be written to. The RF divider select in Register 6 is also double buffered, but only if DB14 of Register 4 is high.

## VCO

The VCO core in the ADF4356 consists of four separate VCOs, each of which uses 256 overlapping bands, which allows the device to cover a wide frequency range without large VCO sensitivity ($K_V$) and without resulting poor phase noise and spurious performance.

The correct VCO and band are chosen automatically by the VCO and band select logic when Register 0 is updated and auto-calibration is enabled.

The R counter output is used as the clock for the band select logic. After band selection, normal PLL action resumes. The nominal value of $K_V$ is 25 MHz/V when the N divider is driven from the VCO output, or the $K_V$ value is divided by D. D is the output divider value if the N divider is driven from the RF output divider (chosen by programming Bits[DB23:DB21] in Register 6).

The VCO shows variation of $K_V$ as the tuning voltage, $V_{TUNE}$, varies within the band and from band to band. For wideband applications covering a wide frequency range (and changing output dividers), a value of 25 MHz/V provides the most accurate $K_V$, because this value is closest to the average value. Figure 24 shows how $K_V$ varies with fundamental VCO frequency along with an average value for the frequency band. Users may prefer this figure when using narrow-band designs.
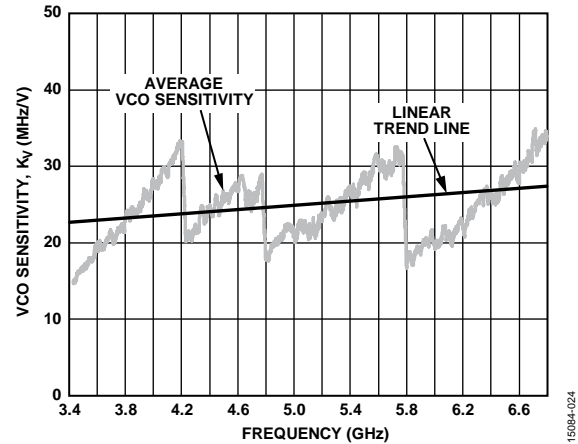


*Figure 24. VCO Sensitivity, $K_V$ vs. Frequency*

## OUTPUT STAGE

The RF$_{OUT}$A+ and RF$_{OUT}$A− pins of the ADF4356 connect to the collectors of an NPN differential pair driven by buffered outputs of the VCO, as shown in Figure 25. In this scheme, the ADF4356 contains internal 50 Ω resistors connected to the $V_{RF}$ pin. To optimize the power dissipation vs. the output power requirements, the tail current of the differential pair is programmable using Bits[DB2:DB1] in Register 6. Four current levels can be set. These levels give approximate output power levels of −4 dBm, −1 dBm, +2 dBm, and +5 dBm, respectively. Levels of −4 dBm, −1 dBm, and +2 dBm can be achieved using a 50 Ω resistor to $V_{RF}$ and ac coupling into a 50 Ω load. For accurate power levels, refer to the Typical Performance Characteristics section. An output power of 5 dBm requires an external shunt inductor to provide higher power levels; however, this addition results in less wideband performance using the internal bias only. Terminate the unused complementary output with a similar circuit to the used output.
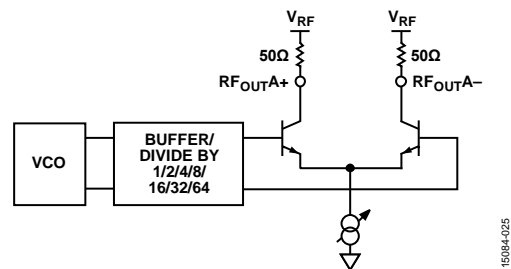


*Figure 25. Output Stage*

Another feature of the ADF4356 is that the supply current to the RF$_{OUT}$A+/RF$_{OUT}$A− output stage can shut down until the ADF4356 achieves lock as measured by the digital lock detect circuitry. The mute till lock detect (MTLD) bit (Bit DB11) in Register 6 enables this function.

The RF$_{OUT}$B+/RF$_{OUT}$B− pins are duplicate outputs that can be used independently or in addition to the RF$_{OUT}$A+/RF$_{OUT}$A− pins.

**Table 7. Total I$_{DD}$ (RF Output A Enabled/RF Output B Disabled)[1]**

| Divide By | RF$_{OUT}$A± Off | RF$_{OUT}$A± = −4 dBm | RF$_{OUT}$A± = −1 dBm | RF$_{OUT}$A± = 2 dBm | RF$_{OUT}$A± = 5 dBm |
|---|---|---|---|---|---|
| 5 V Supply (I$_{VCO}$ and I$_P$) | 78 mA | 78 mA | 78 mA | 78 mA | 78 mA |
| 3.3 V Supply (AI$_{DD}$, DI$_{DD}$, and I$_{RF}$) | | | | | |
| 1 | 84.8 | 106.2 | 117.3 | 128.2 | 138.9 |
| 2 | 94.1 | 114.9 | 125.7 | 136.4 | 146.5 |
| 4 | 103.9 | 124.9 | 136.2 | 147.3 | 158.0 |
| 8 | 111.9 | 132.9 | 144.3 | 155.6 | 166.8 |
| 16 | 116.9 | 138.0 | 149.5 | 160.7 | 171.8 |
| 32 | 120.9 | 142.0 | 153.6 | 164.8 | 176.1 |
| 64 | 123.3 | 144.4 | 156.0 | 167.3 | 178.4 |

[1] RF$_{OUT}$A± refers to RF$_{OUT}$A+/RF$_{OUT}$A−.

**Table 8. Total I$_{DD}$ (RF Output A Enabled/RF Output B Enabled)[1]**

| Divide By | RF$_{OUT}$A±/RF$_{OUT}$B± Off | RF$_{OUT}$A±/RF$_{OUT}$B± = −4 dBm | RF$_{OUT}$A±/RF$_{OUT}$B± = −1 dBm | RF$_{OUT}$A±/RF$_{OUT}$B± = 2 dBm | RF$_{OUT}$A±/RF$_{OUT}$B± = 5 dBm |
|---|---|---|---|---|---|
| 5 V Supply (I$_{VCO}$ and I$_P$) | 78 mA | 78 mA | 78 mA | 78 mA | 78 mA |
| 3.3 V Supply (AI$_{DD}$, DI$_{DD}$, and I$_{RF}$) | | | | | |
| 1 | 84.9 | 133.5 | 150.0 | 166.3 | 182.1 |
| 2 | 94.2 | 142.4 | 159.8 | 177.2 | 193.6 |
| 4 | 104.0 | 151.9 | 169.5 | 187.0 | 204.0 |
| 8 | 112.0 | 159.7 | 177.3 | 194.7 | 211.6 |
| 16 | 117.0 | 164.5 | 182.2 | 199.5 | 216.5 |
| 32 | 121.0 | 168.4 | 186.1 | 203.5 | 220.4 |
| 64 | 123.4 | 170.8 | 188.6 | 205.8 | 222.8 |

[1] RF$_{OUT}$A± refers to RF$_{OUT}$A+/RF$_{OUT}$A− and RF$_{OUT}$B± refers to RF$_{OUT}$B+/RF$_{OUT}$B−.

# REGISTER MAPS

**REGISTER 0**

| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | | | | AUTOCAL | PRESCALER | 16-BIT INTEGER VALUE (INT) | | | | | | | | | | | | | | | | CONTROL BITS | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | AC1 | PR1 | N16 | N15 | N14 | N13 | N12 | N11 | N10 | N9 | N8 | N7 | N6 | N5 | N4 | N3 | N2 | N1 | C4(0) | C3(0) | C2(0) | C1(0) |

**REGISTER 1**

| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESERVED | | | | 24-BIT MAIN FRACTIONAL VALUE (FRAC1) | | | | | | | | | | | | | | | DBR[1] | | | | | | | | | CONTROL BITS | | | |
| 0 | 0 | 0 | 0 | F24 | F23 | F22 | F21 | F20 | F19 | F18 | F17 | F16 | F15 | F14 | F13 | F12 | F11 | F10 | F9 | F8 | F7 | F6 | F5 | F4 | F3 | F2 | F1 | C4(0) | C3(0) | C2(0) | C1(1) |

**REGISTER 2**

| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 14-BIT AUXILIARY FRACTIONAL LSB VALUE (FRAC2_LSB) | | | | | | | | | | | | | | 14-BIT AUXILIARY MODULUS MSB VALUE (MOD2_LSB) | | | | | | | | | | | | | | CONTROL BITS | | | |
| F14 | F13 | F12 | F11 | F10 | F9 | F8 | F7 | F6 | F5 | F4 | F3 | F2 | F1 | M14 | M13 | M12 | M11 | M10 | M9 | M8 | M7 | M6 | M5 | M4 | M3 | M2 | M1 | C4(0) | C3(0) | C2(1) | C1(0) |

**REGISTER 3**

| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESERVED | SD LOAD RESET | PHASE RESYNC | PHASE ADJUST | 24-BIT PHASE VALUE (PHASE) | | | | | | | | | | | | | | | DBR[1] | | | | | | | | | CONTROL BITS | | | |
| 0 | SD1 | PR1 | PA1 | P24 | P23 | P22 | P21 | P20 | P19 | P18 | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 | P9 | P8 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | C4(0) | C3(0) | C2(1) | C1(1) |

**REGISTER 4**

| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESERVED | | MUXOUT | | | REFERENCE DOUBLER DBR[1] | RDIV2 DBR[1] | 10-BIT R COUNTER | | | | | | | | | DBR[1] | DOUBLE BUFF | CURRENT SETTING | | | DBR[1] | REF MODE | MUX LOGIC | PD POLARITY | POWER-DOWN | CP THREE-STATE | COUNTER RESET | CONTROL BITS | | | |
| 0 | 0 | M3 | M2 | M1 | RD2 | RD1 | R10 | R9 | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 | D1 | CP4 | CP3 | CP2 | CP1 | U6 | U5 | U4 | U3 | U2 | U1 | C4(0) | C3(1) | C2(0) | C1(0) |

**REGISTER 5**

| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | | | | | CONTROL BITS | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | C4(0) | C3(1) | C2(0) | C1(1) |

**REGISTER 6**

| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BLEED POLARITY | GATED BLEED | NEGATIVE BLEED | RESERVED | | | RF OUTPUT B SELECT | FEEDBACK SELECT | RF DIVIDER SELECT[2] | | | CHARGE PUMP BLEED CURRENT | | | | | | | | | RESERVED | MTLD | RESERVED | RF OUTPUT B ENABLE | RF OUTPUT B POWER | | RF OUTPUT A ENABLE | RF OUTPUT A POWER | | CONTROL BITS | | | |
| BP1 | BL10 | BL9 | 1 | 0 | 1 | D14 | D13 | D12 | D11 | D10 | BL8 | BL7 | BL6 | BL5 | BL4 | BL3 | BL2 | BL1 | 0 | D8 | 0 | D6 | D5 | D4 | D3 | D2 | D1 | C4(0) | C3(1) | C2(1) | C1(0) |

[1]DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.
[2]DBB = DOUBLE BUFFERED BITS—BUFFERED BY A WRITE TO REGISTER 0 WHEN BIT DB14 OF REGISTER 4 IS HIGH.

*Figure 26.*

**REGISTER 7**

| | | LE SEL SYNC EDGE | RESERVED | LE SYNC | | | | | | | | | | | | | | | | | | | LD CYCLE COUNT | | LOL MODE | FRAC-N LD PRECISION | | LD MODE | CONTROL BITS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | | | | | | RESERVED | | | | | | | | | | | | | | | | | | | | |
| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 0 | LE2 | 1 | LE1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LD5 | LD4 | LOL | LD3 | LD2 | LD1 | C4(0) | C3(1) | C2(1) | C1(1) |

**REGISTER 8**

| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | | | | | CONTROL BITS | | | |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | C4(1) | C3(0) | C2(0) | C1(0) |

**REGISTER 9**

| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VCO BAND DIVISION | | | | | | | | TIMEOUT | | | | | | | | | | AUTOMATIC LEVEL CALIBRATION TIMEOUT | | | | | SYNTHESIZER LOCK TIMEOUT | | | | | CONTROL BITS | | | |
| VC8 | VC7 | VC6 | VC5 | VC4 | VC3 | VC2 | VC1 | TL10 | TL9 | TL8 | TL7 | TL6 | TL5 | TL4 | TL3 | TL2 | TL1 | AL5 | AL4 | AL3 | AL2 | AL1 | SL5 | SL4 | SL3 | SL2 | SL1 | C4(1) | C3(0) | C2(0) | C1(1) |

**REGISTER 10**

| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | | | | | | | | | | | | ADC CLOCK DIVIDER | | | | | | | | ADC CONVERSION | ADC ENABLE | CONTROL BITS | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | AD8 | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AE2 | AE1 | C4(1) | C3(0) | C2(1) | C1(0) |

**REGISTER 11**

| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | VCO BAND HOLD | RESERVED | | | | | | | | | | | | | | | | | | | | CONTROL BITS | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | VH | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | C4(1) | C3(0) | C2(1) | C1(1) |

**REGISTER 12**

| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PHASE RESYNC CLOCK VALUE | | | | | | | | | | | | | | | | | | | | RESERVED | | | | | | | | CONTROL BITS | | | |
| P20 | P19 | P18 | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 | P9 | P8 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | C4(1) | C3(1) | C2(0) | C1(0) |

**REGISTER 13**

| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 14-BIT AUXILIARY FRACTIONAL MSB VALUE (FRAC2_MSB) DBR [1] | | | | | | | | | | | | | | 14-BIT AUXILIARY MODULUS MSB VALUE (MOD2_MSB) DBR [1] | | | | | | | | | | | | | | CONTROL BITS | | | |
| F14 | F13 | F12 | F11 | F10 | F9 | F8 | F7 | F6 | F5 | F4 | F3 | F2 | F1 | M14 | M13 | M12 | M11 | M10 | M9 | M8 | M7 | M6 | M5 | M4 | M3 | M2 | M1 | C4(1) | C3(1) | C2(0) | C1(1) |

*Figure 27. Register Summary (Register 7 to Register 13)*

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*Figure 28. Register 0*

## REGISTER 0

### Control Bits

With Bits[C4:C1] set to 0000, Register 0 is programmed. Figure 28 shows the input data format for programming this register.

### Reserved

Bits[DB31:DB22] are reserved and must be set to 0.

### Automatic Calibration (AUTOCAL)

Write to Register 0 to enact (by default) the VCO automatic calibration, and to choose the appropriate VCO and VCO subband. Write 1 to the AC1 bit (Bit DB21) to enable the automatic calibration, which is the recommended mode of operation.

Set the AC1 bit (Bit DB21) to 0 to disable the automatic calibration, which leaves the ADF4356 in the same band it was already in when Register 0 is updated.

Disable the automatic calibration only for fixed frequency applications, phase adjust applications, or very small (<10 kHz) frequency jumps.

Toggling AUTOCAL is also required when changing frequency. See the Frequency Update Sequence section for more information.

### Prescaler Value

The dual modulus prescaler (P/P + 1), along with the INT, FRACx, and MODx counters, determines the overall division ratio from the VCO output to the PFD input. The PR1 bit (Bit DB20) in Register 0 sets the prescaler value.

Operating at CML levels, the prescaler takes the clock from the VCO output and divides it down for the counters. It is based on a synchronous 4/5 core. When the prescaler is set to 4/5, the maximum RF frequency allowed is 7 GHz. The prescaler limits the INT value; therefore, if P is 4/5, $N_{MIN}$ is 23, and if P is 8/9, $N_{MIN}$ is 75.

### 16-Bit Integer Value

The 16 INT bits (Bits[DB19:DB4]) set the INT value, which determines the integer part of the feedback division factor. The INT value is used in Equation 3 (see the INT, FRACx, MODx, and R Counter Relationship section). All integer values from 23 to 32,767 are allowed for the 4/5 prescaler. For the 8/9 prescaler, the minimum integer value is 75, and the maximum value is 65,535.

| | | | | 24-BIT MAIN FRACTIONAL VALUE (FRAC1) | | | | | | | | | | | | | | | | | | | | DBR[1] | | | | CONTROL BITS | | |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | F24 | F23 | F22 | F21 | F20 | F19 | F18 | F17 | F16 | F15 | F14 | F13 | F12 | F11 | F10 | F9 | F8 | F7 | F6 | F5 | F4 | F3 | F2 | F1 | C4(0) | C3(0) | C2(0) | C1(1) |

| F24 | F23 | .... | F12 | F1 | MAIN FRACTIONAL VALUE (FRAC1) |
|---|---|---|---|---|---|
| 0 | 0 | .... | 0 | 0 | 0 |
| 0 | 0 | .... | 0 | 1 | 1 |
| 0 | 0 | .... | 1 | 0 | 2 |
| 0 | 0 | .... | 1 | 1 | 3 |
| . | . | .... | . | . | . |
| . | . | .... | . | . | . |
| . | . | .... | . | . | . |
| 1 | 1 | .... | 0 | 0 | 16777212 |
| 1 | 1 | .... | 1 | 1 | 16777213 |
| 1 | 1 | .... | 1 | 1 | 16777214 |
| 1 | 1 | .... | 1 | 1 | 16777215 |

[1]DBR = DOUBLE BUFFERED REGISTER–BUFFERED BY THE WRITE TO REGISTER 0.

*Figure 29. Register 1*

| 14-BIT AUXILIARY FRACTIONAL LSB VALUE (FRAC2_LSB) | | | | | | | | | | | | | | 14-BIT AUXILIARY MODULUS MSB VALUE (MOD2_LSB) | | | | | | | | | | | | | | CONTROL BITS | | |
| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| F14 | F13 | F12 | F11 | F10 | F9 | F8 | F7 | F6 | F5 | F4 | F3 | F2 | F1 | M14 | M13 | M12 | M11 | M10 | M9 | M8 | M7 | M6 | M5 | M4 | M3 | M2 | M1 | C4(0) | C3(0) | C2(1) | C1(0) |

| F14 | F13 | .... | F2 | F1 | FRAC2_LSB WORD |
|---|---|---|---|---|---|
| 0 | 0 | .... | 0 | 0 | 0 |
| 0 | 0 | .... | 0 | 1 | 1 |
| 0 | 0 | .... | 1 | 0 | 2 |
| 0 | 0 | .... | 1 | 1 | 3 |
| . | . | .... | . | . | . |
| . | . | .... | . | . | . |
| . | . | .... | . | . | . |
| 1 | 1 | .... | 0 | 0 | 16381 |
| 1 | 1 | .... | 0 | 1 | 16382 |
| 1 | 1 | .... | 1 | 0 | 16382 |
| 1 | 1 | .... | 1 | 1 | 16383 |

| M14 | M13 | .... | M2 | M1 | MOD2_LSB VALUE |
|---|---|---|---|---|---|
| 0 | 0 | .... | 0 | 0 | NOT ALLOWED |
| 0 | 0 | .... | 0 | 1 | NOT ALLOWED |
| 0 | 0 | .... | 1 | 0 | 2 |
| 0 | 0 | .... | 1 | 1 | 3 |
| . | . | .... | . | . | . |
| . | . | .... | . | . | . |
| . | . | .... | . | . | . |
| 1 | 1 | .... | 0 | 0 | 16380 |
| 1 | 1 | .... | 0 | 1 | 16381 |
| 1 | 1 | .... | 1 | 0 | 16382 |
| 1 | 1 | .... | 1 | 1 | 16383 |

[1]DBR = DOUBLE BUFFERED REGISTER–BUFFERED BY THE WRITE TO REGISTER 0.

*Figure 30. Register 2*

## REGISTER 1

### Control Bits

With Bits[C4:C1] set to 0001, Register 1 is programmed. Figure 29 shows the input data format for programming this register.

### Reserved

Bits[DB31:DB28] are reserved and must be set to 0.

### 24-Bit Main Fractional Value

The 24 FRAC1 bits (Bits[DB27:DB4]) set the numerator of the fraction that is input to the Σ-Δ modulator. This fraction, along with the INT value, specifies the new frequency channel that the synthesizer locks to, as shown in the RF Synthesizer—A Worked Example section. FRAC1 values from 0 to (MOD1 − 1) cover channels over a frequency range equal to the PFD reference frequency.
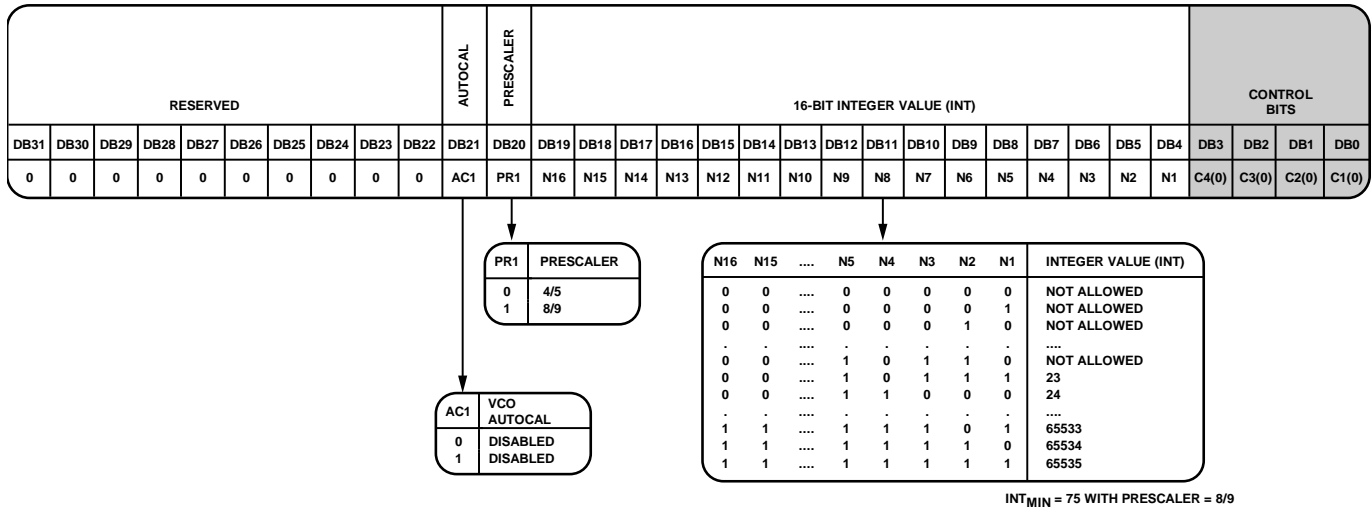
## REGISTER 2

### Control Bits

With Bits[C4:C1] set to 0010, Register 2 is programmed. Figure 30 shows the input data format for programming this register.

### 14-Bit Auxiliary Fractional LSB Value (FRAC2_LSB)

Use this value with the auxiliary fractional MSB value (Register 13, Bits[DB31:DB18]) to generate the total auxiliary fractional value.

$$FRAC2 = (FRAC2\_MSB \times 2^{14}) + FRAC2\_LSB$$

FRAC2 must be less than the MOD2 value programmed in Register 2.

### 14-Bit Auxiliary Modulus LSB Value (MOD2_LSB)

Use this value with the auxiliary modulus MSB value (Register 13, Bits[DB17:DB4]) to generate total auxiliary modulus value.

$$MOD2 = (MOD2\_MSB) \times 2^{14} + MOD2\_LSB$$

Use MOD2 to correct any residual error due to the main fractional modulus.

| RESERVED | SD LOAD RESET | PHASE RESYNC | PHASE ADJUST | 24-BIT PHASE VALUE (PHASE) DBR[1] | | | | | | | | | | | | | | | | | | | | | | | | CONTROL BITS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | SD1 | PR1 | PA1 | P24 | P23 | P22 | P21 | P20 | P19 | P18 | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 | P9 | P8 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | C4(0) | C3(0) | C2(1) | C1(1) |

| PA1 | PHASE ADJUST |
|---|---|
| 0 | DISABLED |
| 1 | ENABLED |

| PR1 | PHASE RESYNC |
|---|---|
| 0 | DISABLED |
| 1 | ENABLED |

| SD1 | SD LOAD RESET |
|---|---|
| 0 | ON REGISTER0 UPDATE |
| 1 | DISABLED |

| P24 | P23 | .... | P2 | P1 | PHASE VALUE (PHASE) |
|---|---|---|---|---|---|
| 0 | 0 | .... | 0 | 0 | 0 |
| 0 | 0 | .... | 0 | 1 | 1 |
| 0 | 0 | .... | 1 | 0 | 2 |
| 0 | 0 | .... | 1 | 1 | 3 |
| . | . | .... | . | . | . |
| . | . | .... | . | . | . |
| . | . | .... | . | . | . |
| 1 | 1 | .... | 0 | 0 | 16777212 |
| 1 | 1 | .... | 0 | 1 | 16777213 |
| 1 | 1 | .... | 1 | 0 | 16777214 |
| 1 | 1 | .... | 1 | 1 | 16777215 |

[1]DBR = DOUBLE BUFFERED REGISTER–BUFFERED BY THE WRITE TO REGISTER 0.

*Figure 31. Register 3*

## REGISTER 3

### Control Bits

With Bits[C4:C1] set to 0011, Register 3 is programmed. Figure 31 shows the input data format for programming this register.

### Reserved

Bit DB31 is reserved and must be set to 0.

### SD Load Reset

When writing to Register 0, the $\Sigma$-$\Delta$ modulator resets. For applications in which the phase is continually adjusted, this may not be desirable; therefore, in these cases, the $\Sigma$-$\Delta$ reset can be disabled by writing a 1 to the SD1 bit (Bit DB30).
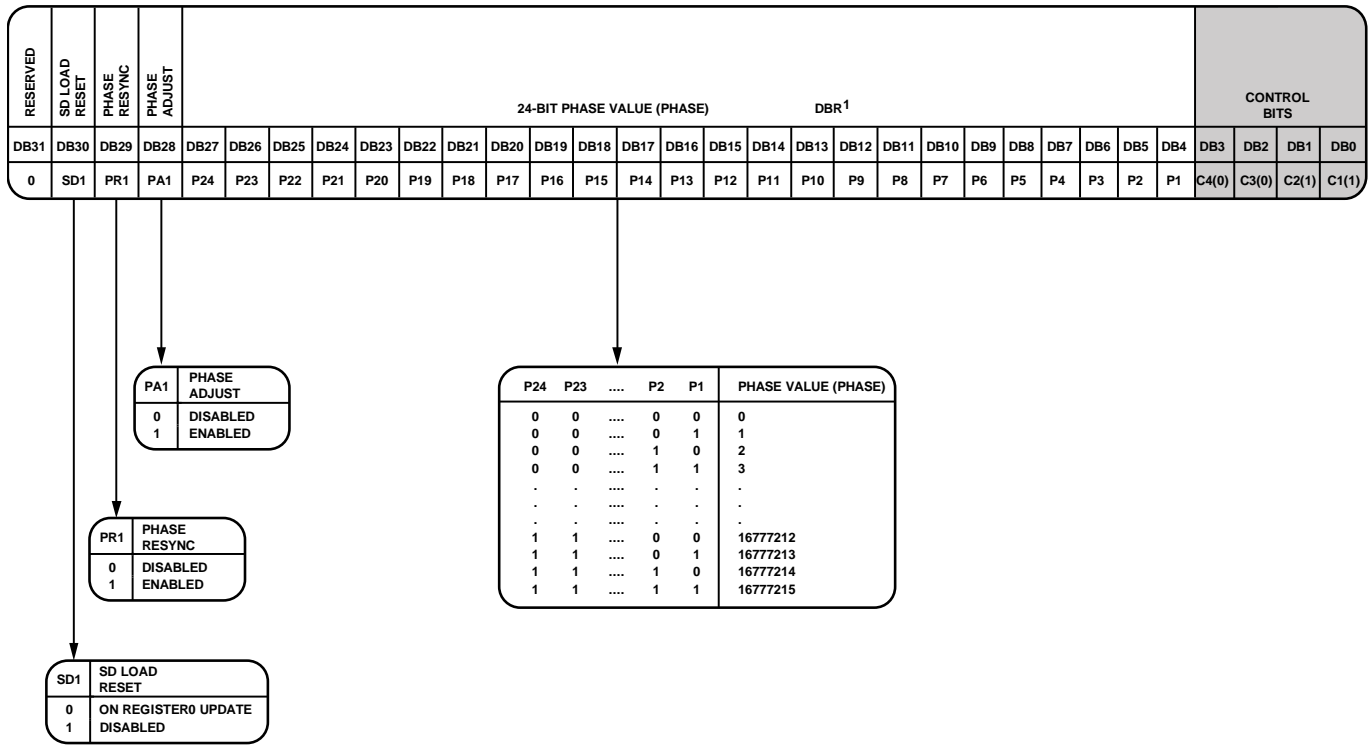
### Phase Resync

To use the phase resynchronization feature, the PR1 bit (Bit DB29) must be set to 1. If unused, the bit can be programmed to 0. The phase resync activation timeout value must also be used in Register 12 to ensure that the resynchronization feature is applied after the PLL settles to the final frequency. If the PLL has not settled to the final frequency, phase resync may not function correctly. Resynchronization is useful in phased array and beam forming applications. It ensures repeatability of output phase when programming the same frequency. In phase critical applications that use frequencies requiring the output divider (<3400 MHz), it is necessary to feed the N divider with the divided VCO frequency as distinct from the fundamental VCO frequency, which is achieved by programming the D13 bit (Bit DB24) in Register 6 to 0, which ensures divided feedback to the N divider.

For resync applications, enable the $\Sigma$-$\Delta$ modulator load reset (SD load reset) in Register 3 by setting DB30 to 0.

The phase of the RF output frequency can be adjusted in 24-bit steps from 0° (0) to 360° ($2^{24} - 1$) relative to the resync phase. For phase adjustment applications, the phase is set by Bits[P24:P1].

$$(Phase\ Value/16{,}777{,}216) \times 360°$$

Practically, this means that repeatable adjustable phase values can be achieved by using the resync feature with different phase values.

### Phase Adjustment

To adjust the relative output phase of the ADF4356 on each Register 0 update, set the PA1 bit (Bit DB28) to 1. This feature differs from the resynchronization feature in that it is useful when adjustments to phase are made continually in an application. For this function, disable the VCO automatic calibration by setting the AC1 bit (Bit DB21) in Register 0 to 1, and disable the SD load reset by setting the SD1 bit (Bit DB30) in Register 3 to 1.

### 24-Bit Phase Value

The phase of the RF output frequency can adjust in 24-bit steps, from 0° (0) to 360° ($2^{24} - 1$). For phase adjust applications, the phase is set by

$$(Phase\ Value/16{,}777{,}216) \times 360°$$

When the phase value is programmed to Register 3, each subsequent adjustment of Register 0 increments the phase by the value in this equation.

| RESERVED | | MUXOUT | | | REFERENCE DOUBLER DBR | RDIV2 DBR | 10-BIT R COUNTER DBR | | | | | | | | | | | | DOUBLE BUFF | CURRENT SETTING DBR | | | | REF MODE | MUX LOGIC | PD POLARITY | POWER-DOWN | CP THREE-STATE | COUNTER RESET | CONTROL BITS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | M3 | M2 | M1 | RD2 | RD1 | R10 | R9 | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 | D1 | CP4 | CP3 | CP2 | CP1 | U6 | U5 | U4 | U3 | U2 | U1 | C4(0) | C3(1) | C2(0) | C1(0) |

| RD2 | REFERENCE DOUBLER |
|---|---|
| 0 | DISABLED |
| 1 | ENABLED |

| RD1 | REFERENCE DIVIDE BY 2 |
|---|---|
| 0 | DISABLED |
| 1 | ENABLED |

| R10 | R9 | ......... | R2 | R1 | R DIVIDER (R) |
|---|---|---|---|---|---|
| 0 | 0 | ......... | 0 | 1 | 1 |
| 0 | 0 | ......... | 1 | 0 | 2 |
| . | . | ......... | . | . | . |
| . | . | ......... | . | . | . |
| . | . | ......... | . | . | . |
| 1 | 1 | ......... | 0 | 0 | 1020 |
| 1 | 1 | ......... | 0 | 1 | 1021 |
| 1 | 1 | ......... | 1 | 0 | 1022 |
| 1 | 1 | ......... | 1 | 1 | 1023 |

| M3 | M2 | M1 | OUTPUT |
|---|---|---|---|
| 0 | 0 | 0 | THREE-STATE OUTPUT |
| 0 | 0 | 1 | DV$_{DD}$ |
| 0 | 1 | 0 | SD$_{GND}$ |
| 0 | 1 | 1 | R DIVIDER OUTPUT |
| 1 | 0 | 0 | N DIVIDER OUTPUT |
| 1 | 0 | 1 | ANALOG LOCK DETECT |
| 1 | 1 | 0 | DIGITAL LOCK DETECT |
| 1 | 1 | 1 | RESERVED |

| D1 | DOUBLE BUFFERED REGISTER 6, BITS[DB23:DB21] |
|---|---|
| 0 | DISABLED |
| 1 | ENABLED |

| CP4 | CP3 | CP2 | CP1 | I$_{CP}$ (mA) 5.1kΩ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0.30 |
| 0 | 0 | 0 | 1 | 0.60 |
| 0 | 0 | 1 | 0 | 0.90 |
| 0 | 0 | 1 | 1 | 1.20 |
| 0 | 1 | 0 | 0 | 1.50 |
| 0 | 1 | 0 | 1 | 1.80 |
| 0 | 1 | 1 | 0 | 2.10 |
| 0 | 1 | 1 | 1 | 2.40 |
| 1 | 0 | 0 | 0 | 2.70 |
| 1 | 0 | 0 | 1 | 3.00 |
| 1 | 0 | 1 | 0 | 3.30 |
| 1 | 0 | 1 | 1 | 3.60 |
| 1 | 1 | 0 | 0 | 3.90 |
| 1 | 1 | 0 | 1 | 4.20 |
| 1 | 1 | 1 | 0 | 4.50 |
| 1 | 1 | 1 | 1 | 4.80 |

| U6 | REFIN |
|---|---|
| 0 | SINGLE |
| 1 | DIFF |

| U5 | LDP |
|---|---|
| 0 | 1.8V |
| 1 | 3.3V |

| U4 | PD POLARITY |
|---|---|
| 0 | NEGATIVE |
| 1 | POSITIVE |

| U1 | COUNTER RESET |
|---|---|
| 0 | DISABLED |
| 1 | ENABLED |

| U2 | CP THREE-STATE |
|---|---|
| 0 | DISABLED |
| 1 | ENABLED |

| U3 | POWER DOWN |
|---|---|
| 0 | DISABLED |
| 1 | ENABLED |

$^1$DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.

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*Figure 32. Register 4*

## REGISTER 4

### Control Bits

With Bits[C4:C1] set to 0100, Register 4 is programmed. Figure 32 shows the input data format for programming this register.

### Reserved

Bits[DB31:DB30] are reserved and must be set to 0.

### MUXOUT

The on-chip multiplexer (MUXOUT) is controlled by Bits[DB29:DB27]. For additional details, see Figure 32.

When changing frequency, that is, writing Register 0, MUXOUT must not be set to N divider output or R divider output. If needed, enable these functions after locking to the new frequency.

### Reference Doubler

Setting the RD2 bit (Bit DB26) to 0 feeds the reference frequency signal directly to the 10-bit R counter, disabling the doubler. Setting this bit to 1 multiplies the reference frequency by a factor of 2 before feeding it into the 10-bit R counter. When the doubler is disabled, the REF$_{IN}$ falling edge is the active edge at the PFD input to the fractional synthesizer. When the doubler is enabled, both the rising and falling edges of the reference frequency become active edges at the PFD input.

The maximum allowable reference frequency when the doubler is enabled is 80 MHz.

### RDIV2

Setting the RDIV2 bit (Bit DB25) to 1 inserts a divide by 2, toggle flip-flop between the R counter and PFD, which extends the maximum reference frequency input rate. This function provides a 50% duty cycle signal at the PFD input.

### 10-Bit R Counter

The 10-bit R counter divides the input reference frequency (REF$_{IN}$) to produce the reference clock to the PFD. Division ratios range from 1 to 1023.

### Double Buffer

The D1 bit (Bit DB14) enables or disables double buffering of the RF divider select bits (Bits[DB23:DB21]) in Register 6. The Program Modes section explains how double buffering works.

### Charge Pump Current Setting

The CP4 to CP1 bits (Bits[DB13:DB10]) set the charge pump current. Set this value to the charge pump current that the loop filter is designed with (see Figure 32). For the lowest spurs, the 0.9 mA setting is recommended.

## Reference Mode

The ADF4356 permits use of either differential or single-ended reference sources.

For optimum integer boundary spur performance, it is recommended to use the single-ended setting for all references up to 250 MHz (even if using a differential reference signal). Use the differential setting for reference frequencies above 250 MHz.

## Level Select

To assist with logic compatibility, MUXOUT is programmable to two logic levels. Set the U5 bit (Bit DB8) to 0 to select 1.8 V logic, and set it to 1 to select 3.3 V logic.

## Phase Detector Polarity

The U4 bit (Bit DB7) sets the phase detector polarity. When a passive loop filter or a noninverting active loop filter is used, set DB7 to 1 (positive). If an active filter with an inverting characteristic is used, set this bit to 0 (negative).

## Power-Down

The U3 bit (Bit DB6) sets the programmable power-down mode. Setting DB6 to 1 performs a power-down. Setting DB6 to 0 returns the synthesizer to normal operation. In software power-down mode, the ADF4356 retains all information in its registers. The register contents are only lost if the supply voltages are removed.

When power-down activates, the following events occur:

- The synthesizer counters are forced to their load state conditions.
- The VCO powers down.
- The charge pump is forced into three-state mode.
- The digital lock detect circuitry resets.
- The RF$_{OUT}$A+/RF$_{OUT}$A− and RF$_{OUT}$B+/RF$_{OUT}$B− output stages are disabled.
- The input registers remain active and capable of loading and latching data.

## Charge Pump Three-State

Setting the U2 bit (Bit DB5) to 1 puts the charge pump into three-state mode. Set DB5 to 0 for normal operation.

## Counter Reset

The U1 bit (Bit DB4) resets the R counter, N counter, and VCO band select of the ADF4356. When DB4 is set to 1, the RF synthesizer N counter, R counter, and VCO band select are reset. For normal operation, set DB4 to 0.

## REGISTER 5

The bits in Register 5 are reserved and must be programmed as described in Figure 33, using a hexadecimal word of 0x00800025.



| | | | | | | | | | | | | | | | | RESERVED | | | | | | | | | | | | CONTROL BITS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | C4(0) | C3(1) | C2(0) | C1(1) |

*Figure 33. Register 5 (0x00800025)*

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BLEED POLARITY | GATED BLEED | NEGATIVE BLEED | RESERVED | | | RF OUTPUT B SELECT | FEEDBACK SELECT | RF DIVIDER SELECT[1] | | | CHARGE PUMP BLEED CURRENT | | | | | | | | | | RESERVED | MTLD | RESERVED | RF OUTPUT B ENABLE | RF OUTPUT B POWER | | RF OUTPUT A ENABLE | RF OUTPUT A POWER | | CONTROL BITS | | | |
| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| BP1 | BL10 | BL9 | 1 | 0 | 1 | D14 | D13 | D12 | D11 | D10 | BL8 | BL7 | BL6 | BL5 | BL4 | BL3 | BL2 | BL1 | 0 | D8 | 0 | D6 | D5 | D4 | D3 | D2 | D1 | C4(0) | C3(1) | C2(1) | C1(0) |

| D14 | RF OUTPUT B SELECT |
|---|---|
| 0 | MIRROR RFOUTA |
| 1 | FUNDAMENTAL |

| D13 | FEEDBACK SELECT |
|---|---|
| 0 | DIVIDED |
| 1 | FUNDAMENTAL |

| BL9 | NEGATIVE BLEED |
|---|---|
| 0 | DISABLED |
| 1 | ENABLED |

| BL10 | GATED BLEED |
|---|---|
| 0 | DISABLED |
| 1 | ENABLED |

| BP1 | BLEED POLARITY |
|---|---|
| 0 | NEGATIVE |
| 1 | POSITIVE |

| D12 | D11 | D10 | RF DIVIDER SELECT |
|---|---|---|---|
| 0 | 0 | 0 | ÷1 |
| 0 | 0 | 1 | ÷2 |
| 0 | 1 | 0 | ÷4 |
| 0 | 1 | 1 | ÷8 |
| 1 | 0 | 0 | ÷16 |
| 1 | 0 | 1 | ÷32 |
| 1 | 1 | 0 | ÷64 |

| D8 | MUTE TILL LOCK DETECT |
|---|---|
| 0 | MUTE DISABLED |
| 1 | MUTE ENABLED |

| BL8 | BL7 | .......... | BL2 | BL1 | BLEED CURRENT | |
|---|---|---|---|---|---|---|
| 0 | 0 | .......... | 0 | 1 | 1 | (3.75µA) |
| 0 | 0 | .......... | 1 | 0 | 2 | (7.5µA) |
| . | . | .......... | . | . | . | |
| . | . | .......... | . | . | . | |
| . | . | .......... | . | . | . | |
| 1 | 1 | .......... | 0 | 0 | 252 | (945µA) |
| 1 | 1 | .......... | 0 | 1 | 253 | (948.75µA) |
| 1 | 1 | .......... | 1 | 0 | 254 | (952.5µA) |
| 1 | 1 | .......... | 1 | 1 | 255 | (956.25µA) |

| D2 | D1 | RF OUTPUT A POWER |
|---|---|---|
| 0 | 0 | −4dBm |
| 0 | 1 | −1dBm |
| 1 | 0 | +2dBm |
| 1 | 1 | +5dBm |

| D3 | RF OUTPUT A ENABLE |
|---|---|
| 0 | DISABLED |
| 1 | ENABLED |

| D5 | D4 | RF OUTPUT B POWER |
|---|---|---|
| 0 | 0 | −4dBm |
| 0 | 1 | −1dBm |
| 1 | 0 | +2dBm |
| 1 | 1 | +5dBm |

| D6 | RF OUTPUT B ENABLE |
|---|---|
| 0 | DISABLED |
| 1 | ENABLED |

[1]BITS[DB23:DB21] ARE BUFFERED BY A WRITE TO REGISTER 0 WHEN THE DOUBLE BUFFER BIT, BIT DB14 OF REGISTER 4, IS ENABLED.

*Figure 34. Register 6*

## REGISTER 6

### Control Bits

With [C4:C1] set to 0110, Register 6 is programmed. Figure 34 shows the input data format for programming this register.

### Bleed Polarity

DB31 sets the polarity of the charge pump bleed current.

### Gated Bleed

Bleed currents can be used for improving phase noise and spurs; however, due to a potential impact on lock time, the gated bleed bit, BL10 (Bit DB30), if set to 1, ensures bleed currents are not switched on until the digital lock detect asserts logic high. Note that this function requires digital lock detect to be enabled.

### Negative Bleed

Use of constant negative bleed is recommended for most fractional-N applications because it improves the linearity of the charge pump, leading to lower noise and spurious signals than leaving it off. To enable negative bleed, write 1 to BL9 (Bit DB29), and to disable negative bleed, write 0 to BL9 (Bit DB29).

Do not use negative bleed when operating in Integer-N mode, that is, FRAC1 = FRAC2 = 0. Do not use negative bleed for $f_{PFD}$ greater than 100 MHz.

### Reserved

Bits[DB28:DB26] are reserved and must be set to 101. Bit DB12 is reserved and must be set to 0. Bit DB10 is reserved and must be set to 0.

### RF Output B Select

D14 (Bit DB25) enables the RF output B (RF$_{OUT}$B+/RF$_{OUT}$B−) to selects the fundamental output from the VCO. When this bit is disabled, RF$_{OUT}$B+/RF$_{OUT}$B− is a duplicate of RF$_{OUT}$A+/RF$_{OUT}$A−.

### Feedback Select

D13 (Bit DB24) selects the feedback from the output of the VCO to the N counter. When D13 is set to 1, the signal is taken directly from the VCO. When this bit is set to 0, the signal is taken from the output of the output dividers. The dividers enable coverage of the wide frequency band (54 MHz to 6800 MHz). When the divider is enabled and the feedback signal is taken from the output, the RF output signals of two separately configured PLLs are in phase. Divided feedback is useful in some applications where the positive interference of signals is required to increase the power.

### Divider Select

D12 to D10 (Bits[DB23:DB21]) select the value of the RF output divider (see Figure 34).

### Charge Pump Bleed Current

BL8 to BL1 (Bits[DB20:DB13]) control the level of the bleed current added to the charge pump output. This current optimizes the phase noise and spurious levels from the device.

Calculate the optimal bleed setting using the following rule.

$$Bleed\ Value = \text{floor}(24 \times (f_{PFD}/61.44\ \text{MHz}) \times (I_{CP}/0.9\ \text{mA}))$$

If $f_{PFD}$ > 100 MHz, disable bleed current using DB29.

where:
$Bleed\ Value$ is the value programmed to Bits[DB20:DB13].
floor() is a function to round down to the nearest integer value.
$f_{PFD}$ is the PFD frequency.
$I_{CP}$ is the value of charge pump current setting, Bits[DB13:DB10] of Register 4.

### Mute Till Lock Detect

When D8 (Bit DB11) is set to 1, the supply current to the RF output stage is shut down until the device achieves lock, as determined by the digital lock detect circuitry.

### RF Output B Enable

D6 (Bit DB9) enables or disables RF Output B (RF$_{OUT}$B+/RF$_{OUT}$B−). If DB10 is set to 0, RF Output B is enabled. If DB10 is set to 1, the RF Output B is disabled.

### RF Output B Power

D5 and D4 (Bits[DB8:DB7]) set the value of the RF Output B (RF$_{OUT}$B+/RF$_{OUT}$B−) power level (see Figure 34).

### RF Output A Enable

D3 (Bit DB6) enables or disables RF Output A (RF$_{OUT}$A+/RF$_{OUT}$A−). If DB3 is set to 0, RF Output A is disabled. If DB6 is set to 1, RF Output A is enabled.

### RF Output A Power

D2 and D1 (Bits[DB5:DB4]) set the value of the RF Output A (RF$_{OUT}$A+/RF$_{OUT}$A−) power level (see Figure 34).
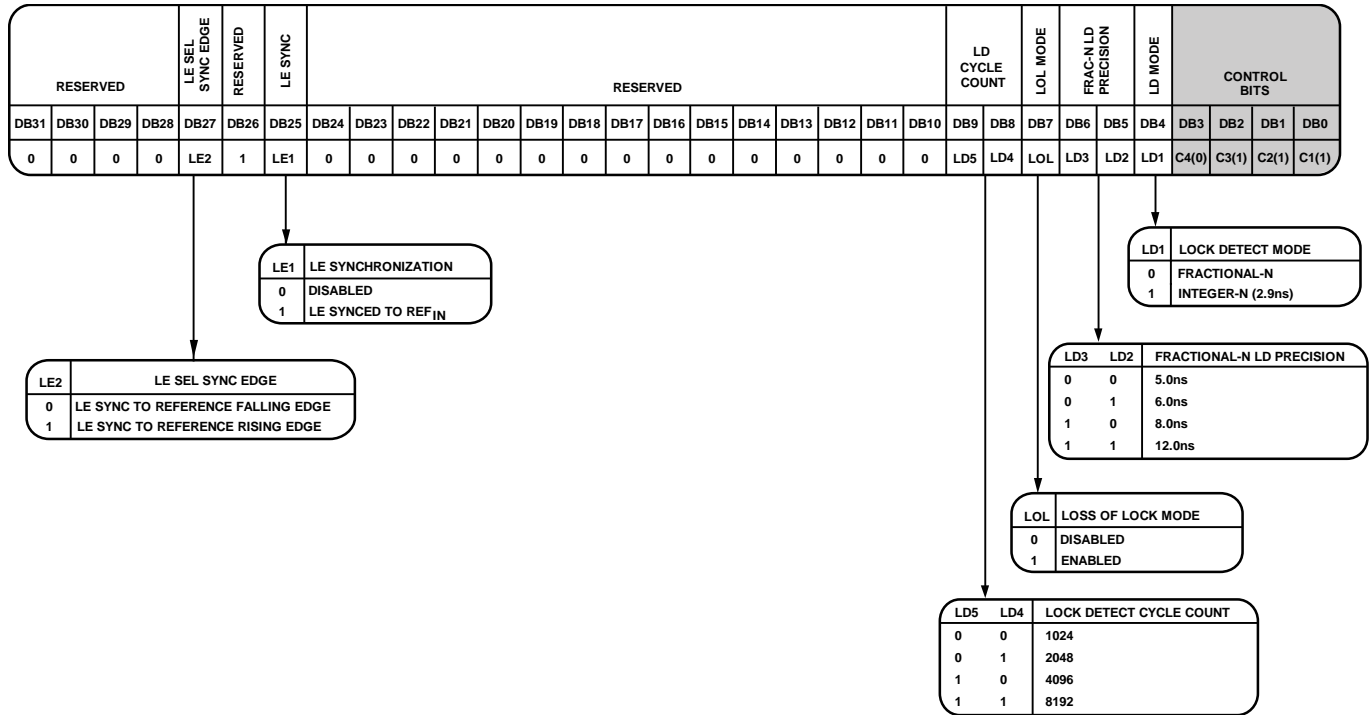
| RESERVED | | | | LE SEL SYNC EDGE | RESERVED | LE SYNC | RESERVED | | | | | | | | | | | | | | | | | LD CYCLE COUNT | | LOL MODE | FRAC-N LD PRECISION | | LD MODE | CONTROL BITS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 0 | LE2 | 1 | LE1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LD5 | LD4 | LOL | LD3 | LD2 | LD1 | C4(0) | C3(1) | C2(1) | C1(1) |

| LE1 | LE SYNCHRONIZATION |
|---|---|
| 0 | DISABLED |
| 1 | LE SYNCED TO REF_IN |

| LE2 | LE SEL SYNC EDGE |
|---|---|
| 0 | LE SYNC TO REFERENCE FALLING EDGE |
| 1 | LE SYNC TO REFERENCE RISING EDGE |

| LD1 | LOCK DETECT MODE |
|---|---|
| 0 | FRACTIONAL-N |
| 1 | INTEGER-N (2.9ns) |

| LD3 | LD2 | FRACTIONAL-N LD PRECISION |
|---|---|---|
| 0 | 0 | 5.0ns |
| 0 | 1 | 6.0ns |
| 1 | 0 | 8.0ns |
| 1 | 1 | 12.0ns |

| LOL | LOSS OF LOCK MODE |
|---|---|
| 0 | DISABLED |
| 1 | ENABLED |

| LD5 | LD4 | LOCK DETECT CYCLE COUNT |
|---|---|---|
| 0 | 0 | 1024 |
| 0 | 1 | 2048 |
| 1 | 0 | 4096 |
| 1 | 1 | 8192 |

*Figure 35. Register 7*

## REGISTER 7

### Control Bits

With Bits[C4:C1] set to 0111, Register 7 is programmed. Figure 35 shows the input data format for programming this register.

### Reserved

Bits[DB31:DB28] are reserved and must be set to 0. DB26 is reserved and must be set to 1. DB26 is reserved and must be set to 1. Bits[DB24:DB10] are reserved and must be set to 0.

### LE SEL Sync Edge

Bit DB27 allows selection of the synchronization load enable (LE) edge to the falling or rising edge of the reference clock, which is useful for applications that require synchronization to a common reference edge (see Figure 35). To use this bit, LE sync (Bit DB25) must be set to 1.

### LE Sync

When set to 1, Bit DB25 ensures that the load enable (LE) edge is synchronized internally with the rising edge of reference input frequency. This synchronization prevents the rare event of reference and RF dividers loading at the same time as a falling edge of the reference frequency, which can lead to longer lock times.

### Fractional-N Lock Detect (LD) Cycle Count

LD5 and LD4 (Bits[DB9:DB8]) set the number of consecutive cycles counted by the lock detect circuitry before asserting lock detect high (see Figure 35 for details).

### Loss of Lock (LOL) Mode

Set the LOL mode bit (Bit DB7) to 1 when the application is a fixed frequency application in which the reference (REF_IN) is likely to be removed, such as a clocking application. The standard lock detect circuit assumes that REF_IN is always present; however, this may not be the case with clocking applications. To enable this functionality, set DB7 to 1.

### Fractional-N Lock Detect (LD) Precision

LD3 and LD2 (Bits[DB6:DB5]) set the precision of the lock detect circuitry in fractional-N mode. LDP is available at 5 ns, 6 ns, 8 ns, or 12 ns. If bleed currents are used, use 12 ns.

### Lock Detect (LD) Mode

When set to 0, lock detect precision is set by fractional-N lock detect precision as described in the Fractional-N Lock Detect (LD) Precision section. If DB4 is set to 1, lock detect precision is 2.9 ns long, which is more appropriate for integer-N applications.

| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | RESERVED | | | | | | | | | | | | | | | | | CONTROL BITS | | | |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | C4(1) | C3(0) | C2(0) | C1(0) |

*Figure 36. Register 8 (0x15596568)*

| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | VCO BAND DIVISION | | | | | | | | | TIMEOUT | | | | | | | | AUTOMATIC LEVEL CALIBRATION TIMEOUT | | | | | SYNTHESIZER LOCK TIMEOUT | | | | CONTROL BITS | | | |
| VC8 | VC7 | VC6 | VC5 | VC4 | VC3 | VC2 | VC1 | TL10 | TL9 | TL8 | TL7 | TL6 | TL5 | TL4 | TL3 | TL2 | TL1 | AL5 | AL4 | AL3 | AL2 | AL1 | SL5 | SL4 | SL3 | SL2 | SL1 | C4(1) | C3(0) | C2(0) | C1(1) |

| TL10 | TL9 | .......... | TL2 | TL1 | TIMEOUT |
|---|---|---|---|---|---|
| 0 | 0 | .......... | 0 | 1 | 1 |
| 0 | 0 | .......... | 1 | 0 | 2 |
| . | . | .......... | . | . | . |
| . | . | .......... | . | . | . |
| . | . | .......... | . | . | . |
| 1 | 1 | .......... | 0 | 0 | 1020 |
| 1 | 1 | .......... | 0 | 1 | 1021 |
| 1 | 1 | .......... | 1 | 0 | 1022 |
| 1 | 1 | .......... | 1 | 1 | 1023 |

| SL5 | SL4 | .......... | SL2 | SL1 | SLC WAIT |
|---|---|---|---|---|---|
| 0 | 0 | .......... | 0 | 1 | 1 |
| 0 | 0 | .......... | 1 | 0 | 2 |
| . | . | .......... | . | . | . |
| . | . | .......... | . | . | . |
| . | . | .......... | . | . | . |
| 1 | 1 | .......... | 0 | 0 | 28 |
| 1 | 1 | .......... | 0 | 1 | 29 |
| 1 | 1 | .......... | 1 | 0 | 30 |
| 1 | 1 | .......... | 1 | 1 | 31 |

| VC8 | VC7 | .......... | VC2 | VC1 | VCO BAND DIV |
|---|---|---|---|---|---|
| 0 | 0 | .......... | 0 | 1 | 1 |
| 0 | 0 | .......... | 1 | 0 | 2 |
| . | . | .......... | . | . | . |
| . | . | .......... | . | . | . |
| . | . | .......... | . | . | . |
| 1 | 1 | .......... | 0 | 0 | 252 |
| 1 | 1 | .......... | 0 | 1 | 253 |
| 1 | 1 | .......... | 1 | 0 | 254 |
| 1 | 1 | .......... | 1 | 1 | 255 |

| AL5 | AL4 | .......... | AL2 | AL1 | ALC WAIT |
|---|---|---|---|---|---|
| 0 | 0 | .......... | 0 | 1 | 1 |
| 0 | 0 | .......... | 1 | 0 | 2 |
| . | . | .......... | . | . | . |
| . | . | .......... | . | . | . |
| . | . | .......... | . | . | . |
| 1 | 1 | .......... | 0 | 0 | 28 |
| 1 | 1 | .......... | 0 | 1 | 29 |
| 1 | 1 | .......... | 1 | 0 | 30 |
| 1 | 1 | .......... | 1 | 1 | 31 |

*Figure 37. Register 9*

## REGISTER 8

The bits in this register are reserved and must be programmed as shown in Figure 36, using a hexadecimal word of (0x15596568).

## REGISTER 9

For a worked example and more information, see the Lock Time section.

### Control Bits

With Bits[C4:C1] set to 1001, Register 9 is programmed. Figure 37 shows the input data format for programming this register.

### VCO Band Division

VC8 to VC1 (Bits[DB31:DB24]) set the value of the VCO band division clock. Determine the value of this clock by

$$VCO\ Band\ Division = \text{Ceiling}(f_{PFD}/1{,}600{,}000)$$

### Timeout

TL10 to TL1 (Bits[DB23:DB14]) set the timeout value for the VCO band select.

### Automatic Level Calibration (ALC) Timeout

AL5 to AL1 (Bits[DB13:DB9]) set the timer value used for the automatic level calibration of the VCO. This function combines the PFD frequency, the timeout variable, and ALC wait variable. Choose the ALC such that the following equation is always greater than 50 μs.

$$ALC\ Wait > (50\ \mu s \times f_{PFD})/Timeout$$

### Synthesizer Lock Timeout

SL5 to SL1 (Bits[DB8:DB4]) set the synthesizer lock timeout value. This value allows the $V_{TUNE}$ force to settle on the $V_{TUNE}$ pin. The value must be 20 μs. Calculate the value using the following equation:

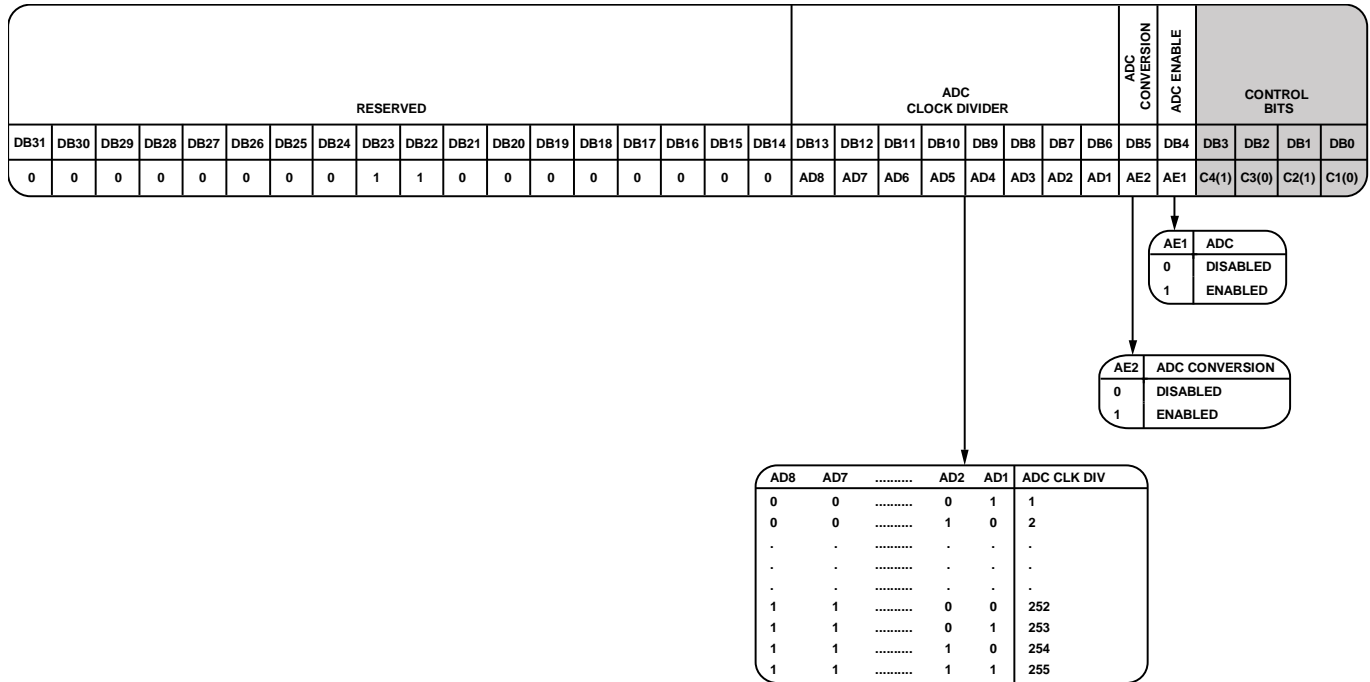$$Synthesizer\ Lock\ Timeout > (20\ \mu s \times f_{PFD})/Timeout$$

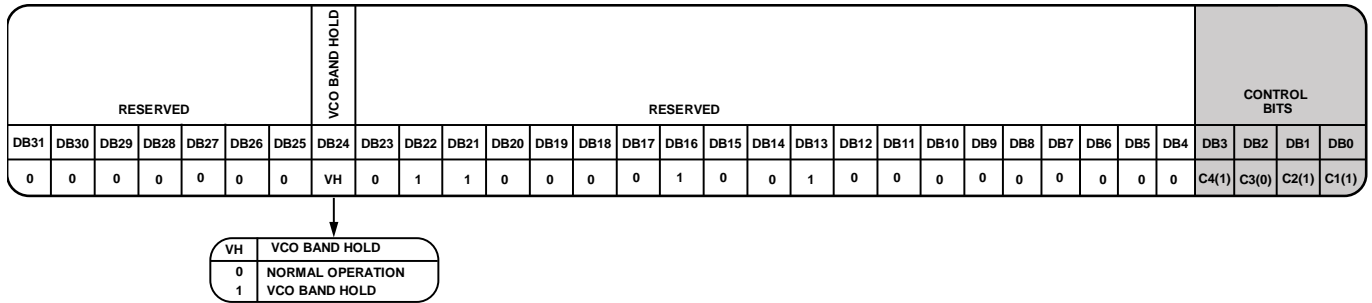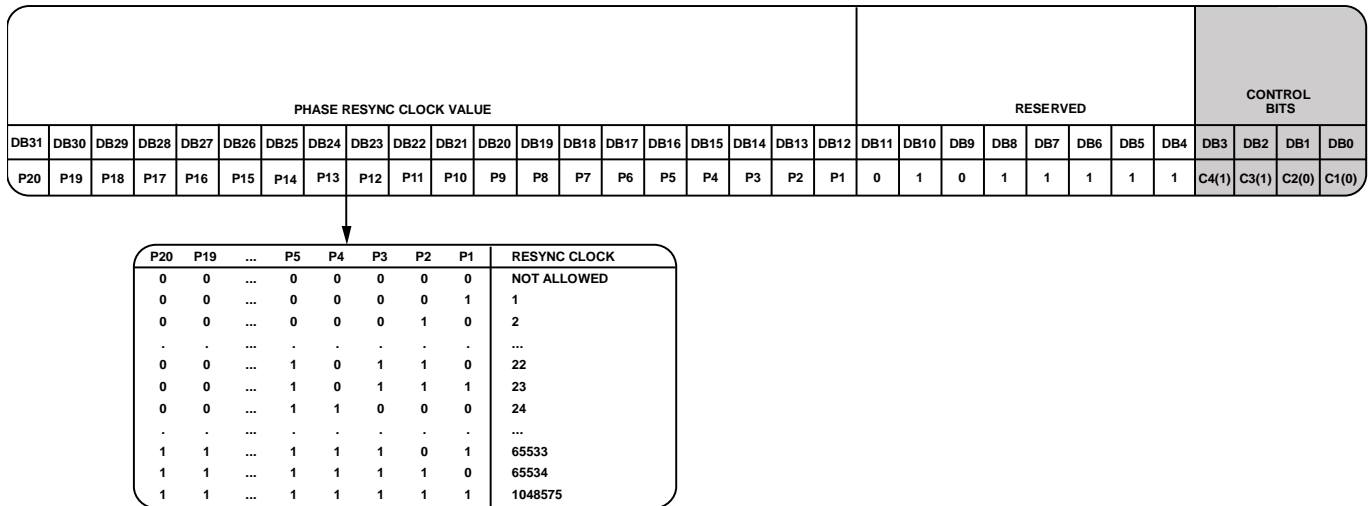*Figure 38. Register 10*

## REGISTER 10

### Control Bits

With Bits[C4:C1] set to 1010, Register 10 is programmed. Figure 38 shows the input data format for programming this register.

### Reserved

Bits[DB31:DB14] are reserved. Bits[DB23:DB22] must be set to 11, and all other bits in this range must be set to 0.

### ADC Clock Divider (ADC_CLK_DIV)

An on-board analog-to-digital converter (ADC) determines the $V_{TUNE}$ setpoint relative to the ambient temperature of the ADF4356 environment. The ADC ensures that the initial tuning voltage in any application is chosen correctly to avoid any temperature drift issues.

The ADC uses a clock that is equal to the output of the R counter (or the PFD frequency) divided by ADC_CLK_DIV.

AD8 to AD1 (Bits[DB13:DB6]) set the value of this divider. On power-up, the R counter is not programmed; however, in these power-up cases, it defaults to R = 1.

Choose the value such that

$ADC\_CLK\_DIV = \text{ceiling}(((f_{PFD}/100,000) - 2)/4)$

where ceiling() is a function that rounds up to the nearest integer.

For example, for $f_{PFD}$ = 61.44 MHz, set ALC_CLK_DIV = 154 so that the ADC clock frequency is 99.417 kHz.

If ADC_CLK_DIV is greater than 255, set it to 255.

### ADC Conversion Enable

AE2 (Bit DB5) ensures that the ADC performs a conversion when a write to Register 10 is performed. It is recommended to enable this mode.

### ADC Enable

AE1 (Bit DB4), when set to 1, powers up the ADC for the temperature dependent $V_{TUNE}$ calibration. It is recommended to always use this function.

*Figure 39. Register 11*



*Figure 40. Register 12*

## REGISTER 11

### Control Bits

With Bits[C4:C1] set to 1011, Register 11 is programmed. Figure 39 shows the input data format for programming this register.

### Reserved

Bits[DB31:DB25] are reserved and must be set to 0. Bit DB22, Bit DB21, Bit DB16, and Bit DB13 must be set to 1, and all other bits in this range (Bits[DB23:DB4]) must be set to 0.

### VCO Band Hold

VH (Bit DB24), when set to 1, prevents a reset of the VCO core, band, and bias during a counter reset. VCO band hold is required for applications that use external PLLs.

## REGISTER 12

### Control Bits

With Bits[C4:C1] set to 1100, Register 12 is programmed. Figure 40 shows the input data format for programming this register.

### Phase Resync Clock Value

P20 to P1 (Bits[DB31:DB12]) set the timeout counter for activation of phase resync. This value must be set such that a resync happens immediately after (and not before) the PLL has achieved lock after reprogramming.

Calculate the timeout value using the following equation:

$$Time\ Out\ Value = Phase\ Resync\ Clock\ Value/f_{PFD}$$

When not using phase resync, set these bits to 1 for normal operation.

### Reserved

Bits [DB11:DB4] are reserved. Bit DB10 and Bits[DB8:DB4] must be set to 1, and all other bits in this range must be set to 0.

| 14-BIT AUXILIARY FRACTIONAL MSB VALUE (FRAC2_LSB) DBR | | | | | | | | | | | | | | 14-BIT AUXILIARY MODULUS MSB VALUE (MOD2_MSB) DBR | | | | | | | | | | | | | | CONTROL BITS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB31 | DB30 | DB29 | DB28 | DB27 | DB26 | DB25 | DB24 | DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| F14 | F13 | F12 | F11 | F10 | F9 | F8 | F7 | F6 | F5 | F4 | F3 | F2 | F1 | M14 | M13 | M12 | M11 | M10 | M9 | M8 | M7 | M6 | M5 | M4 | M3 | M2 | M1 | C4(1) | C3(1) | C2(0) | C1(1) |

| F14 | F13 | .......... | F2 | F1 | FRAC2_MSB WORD |
|---|---|---|---|---|---|
| 0 | 0 | .......... | 0 | 0 | 0 |
| 0 | 0 | .......... | 0 | 1 | 1 |
| 0 | 0 | .......... | 1 | 0 | 2 |
| 0 | 0 | .......... | 1 | 1 | 3 |
| . | . | .......... | . | . | . |
| . | . | .......... | . | . | . |
| . | . | .......... | . | . | . |
| 1 | 1 | .......... | 0 | 0 | 16381 |
| 1 | 1 | .......... | 0 | 1 | 16382 |
| 1 | 1 | .......... | 1 | 0 | 16382 |
| 1 | 1 | .......... | 1 | 1 | 16383 |

| M14 | M13 | .......... | M2 | M1 | MOD2_MSB VALUE |
|---|---|---|---|---|---|
| 0 | 0 | .......... | 0 | 0 | 0 |
| 0 | 0 | .......... | 0 | 1 | 1 |
| 0 | 0 | .......... | 1 | 0 | 2 |
| 0 | 0 | .......... | 1 | 1 | 3 |
| . | . | .......... | . | . | . |
| . | . | .......... | . | . | . |
| . | . | .......... | . | . | . |
| 1 | 1 | .......... | 0 | 0 | 16380 |
| 1 | 1 | .......... | 0 | 1 | 16381 |
| 1 | 1 | .......... | 1 | 0 | 16382 |
| 1 | 1 | .......... | 1 | 1 | 16383 |

[1]DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.

*Figure 41. Register 13*

## REGISTER 13

### Control Bits

With [C4:C1] set to 1101, Register 13 is programmed. Figure 41 shows the input data format for programming this register.

### 14-Bit Auxiliary Fractional MSB Value (FRAC2_MSB)

This value is used with the auxiliary fractional LSB value (Register 2, Bits[DB31:DB18]) to generate the total auxiliary fractional FRAC2 value.

$$FRAC2 = (FRAC2\_MSB \times 2^{14}) + FRAC2\_LSB$$

These bits can be set to all zeros to ensure software compatibility with the ADF4355.

### 14-Bit Auxiliary Modulus MSB Value (MOD2_MSB)

This value is used with the auxiliary fractional MSB value (Register 2, Bits[DB17:DB4]) to generate the total auxiliary modulus MOD2 value.

$$MOD2 = (MOD2\_MSB \times 2^{14}) + MOD2\_LSB$$

## REGISTER INITIALIZATION SEQUENCE

At initial power-up, after the correct application of voltages to the supply pins, the ADF4356 registers must be programmed in sequence. For f ≤ 75 MHz, use the following sequence:

1. Register 13.
2. Register 12.
3. Register 11.
4. Register 10.
5. Register 9.
6. Register 8.
7. Register 7.
8. Register 6.
9. Register 5.
10. Register 4.
11. Register 3.
12. Register 2.
13. Register 1.
14. Ensure that >16 ADC_CLK cycles have elapsed between the write of Register 10 and Register 0. For example, if ADC_CLK = 99.417 kHz, wait 16/99,417 sec = 161 μs. See the Register 10 section for more information.
15. Register 0.

For $f_{PFD}$ > 75 MHz (initially lock with halved $f_{PFD}$), use the following sequence:

1. Register 13 (for halved $f_{PFD}$).
2. Register 12.
3. Register 11.
4. Register 10.
5. Register 4 (with the R divider doubled to halve $f_{PFD}$).
6. Register 9.
7. Register 8.
8. Register 7.
9. Register 6 (for the desired $f_{PFD}$).
10. Register 5.
11. Register 4 (with the R divider doubled to halve $f_{PFD}$).
12. Register 3.
13. Register 2 (for halved $f_{PFD}$).
14. Register 1 (for halved $f_{PFD}$).
15. Ensure that >16 ADC_CLK cycles have elapsed between the write of Register 10 and Register 0. For example, if ADC_CLK = 99.417 kHz, wait 16/99,417 sec = 161 μs. See the Register 10 section for more information.
16. Register 0 (for halved $f_{PFD}$; autocalibration enabled).
17. Register 13 (for the desired $f_{PFD}$).
18. Register 4 (with the R divider set for the desired $f_{PFD}$).
19. Register 2 (for the desired $f_{PFD}$).
20. Register 1 (for the desired $f_{PFD}$).
21. Register 0 (for the desired $f_{PFD}$; autocalibration disabled).

## FREQUENCY UPDATE SEQUENCE

Frequency updates require updating the auxiliary modulator (MOD2) in Register 2, the fractional value (FRAC1) in Register 1, and the integer value (INT) in Register 0. It is recommended to perform a temperature dependent $V_{TUNE}$ calibration by updating Register 10 first. Therefore, for $f_{PFD} \leq 75$ MHz, the sequence must be as follows:

1. Register 13.
2. Register 10.
3. Register 2.
4. Register 1.
5. Ensure that >16 ADC_CLK cycles have elapsed between the write of Register 10 and Register 0. For example, if ADC_CLK = 99.417 kHz, wait 16/99,417 sec = 161 μs. See the Register 10 section for more information.
6. Register 0.

For $f_{PFD} > 75$ MHz (initially lock with halved $f_{PFD}$), the sequence must be as follows:

1. Register 13 (for halved $f_{PFD}$).
2. Register 10.
3. Register 4 (With the R divider doubled to halved $f_{PFD}$).
4. Register 2 (for halved $f_{PFD}$).
5. Register 1 (for halved $f_{PFD}$).
6. Ensure that >16 ADC_CLK cycles have elapsed between the write of Register 10 and Register 0. For example, if ADC_CLK = 99.417 kHz, wait 16/99,417 sec = 161 μs. See the Register 10 section for more information.
7. Register 0 (for halved $f_{PFD}$; autocalibration enabled).
8. Register 13 (for the desired $f_{PFD}$).
9. Register 4 (With the R divider set for the desired $f_{PFD}$).
10. Register 2 (for the desired $f_{PFD}$).
11. Register 1 (for the desired $f_{PFD}$).
12. Register 0 (for desired $f_{PFD}$; autocalibration disabled).

The frequency change occurs on the write to Register 0.

## RF SYNTHESIZER—A WORKED EXAMPLE

Use the following equations to program the ADF4356 synthesizer:

$$RF_{OUT} = INT + \frac{FRAC1 + \dfrac{FRAC2}{MOD2}}{MOD1} \times (f_{PFD}) / RF\ Divider \qquad (7)$$

where:
$RF_{OUT}$ is the RF output frequency.
$INT$ is the integer division factor.
$FRAC1$ is the fractionality.
$FRAC2$ is the auxiliary fractionality (FRAC2 = (FRAC2_MSB × $2^{14}$) + FRAC2_LSB).
$MOD2$ is the auxiliary modulus (MOD2 = (MOD2_MSB × $2^{14}$) + MOD2_LSB).
$MOD1$ is the fixed 24-bit modulus.
$RF\ Divider$ is the output divider that divides down the VCO frequency.

$$f_{PFD} = REF_{IN} \times ((1 + D)/(R \times (1 + T))) \qquad (8)$$

where:
$REF_{IN}$ is the reference frequency input.
$D$ is the $REF_{IN}$ doubler bit.
$R$ is the $REF_{IN}$ reference division factor.
$T$ is the reference divide by 2 bit (0 or 1).

For example, in a universal mobile telecommunication system (UMTS) where a 2112.8 MHz RF frequency output ($RF_{OUT}$) is required, a 122.88 MHz reference frequency input ($REF_{IN}$) is available. Note that the ADF4356 VCO operates in the frequency range of 3400 MHz to 6800 MHz. Therefore, the RF divider of 2 must be used (VCO frequency = 4225.6 MHz, RFOUT = VCO frequency/RF divider = 4225.6 MHz/2 = 2112.8 MHz).

The feedback path is also important. In this example, the VCO output is fed back before the output divider (see Figure 42). In this example, the 122.88 MHz reference signal is divided by 2 to generate $f_{PFD}$ of 61.44 MHz. The desired channel spacing is 200 kHz.
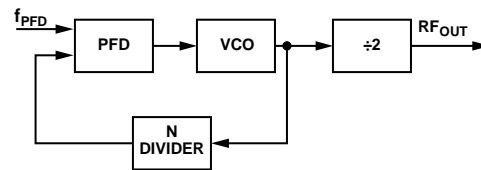


Figure 42. Loop Closed Before Output Divider

The worked example is as follows:

$N = VCO_{OUT}/f_{PFD}$ = 4225.6 MHz/61.44 MHz = 68.7760416666666667

$INT$ = int($VCO\ frequency/f_{PFD}$) = 68

$FRAC$ = 0.7760416666666667

$MOD1$ = 16,777,216

$FRAC1$ = int($MOD1 \times FRAC$) = 13,019,818

$Remainder$ = 0.6666666667 or 2/3

$MOD2 = f_{PFD}/GCD(f_{PFD}, f_{CHSP})$ = 61.44 MHz/GCD(61.44 MHz, 200 kHz) = 1536

$FRAC2 = Remainder \times 1536$ = 1024

From Equation 8,

$$f_{PFD} = (122.88\ \text{MHz} \times (1 + 0)/2) = 61.44\ \text{MHz} \qquad (9)$$

$$2112.8\ \text{MHz} = 61.44\ \text{MHz} \times ((INT + (FRAC1 + FRAC2/MOD2)/2^{24}))/2 \qquad (10)$$

where:
$INT$ = 68
$FRAC1$ = 13,019,818
$FRAC2$ = 1024
$MOD2$ = 1536
$RF\ Divider$ = 2

## REFERENCE DOUBLER AND REFERENCE DIVIDER

The on-chip reference doubler allows the input reference signal to be doubled. The doubler is useful for increasing the PFD comparison frequency. To improve the noise performance of the system, increase the PFD frequency. Doubling the PFD frequency typically improves noise performance by 3 dB.

The reference divide by 2 divides the reference signal by 2, resulting in a 50% duty cycle PFD frequency.

## SPURIOUS OPTIMIZATION AND FAST LOCK

Narrow loop bandwidths can filter unwanted spurious signals; however, these bandwidths typically have a long lock time. A wider loop bandwidth achieves faster lock times but may lead to increased spurious signals inside the loop bandwidth.

## OPTIMIZING JITTER

For lowest jitter applications, use the highest possible PFD frequency to minimize the contribution of in-band noise from the PLL. Set the PLL filter bandwidth such that the in-band noise of the PLL intersects with the open-loop noise of the VCO, minimizing the contribution of both to the overall noise.

Use the ADIsimPLL design tool for this task.

## SPUR MECHANISMS

This section describes the two different spur mechanisms that arise with a fractional-N synthesizer and how to minimize them in the ADF4356.

### Integer Boundary Spurs

One mechanism for fractional spur creation is the interactions between the RF VCO frequency and the reference frequency. When these frequencies are not integer related (the purpose of a fractional-N synthesizer), spur sidebands appear on the VCO output spectrum at an offset frequency that corresponds to the beat note or the difference in frequency between an integer multiple of the reference and the VCO frequency. These spurs are attenuated by the loop filter and are more noticeable on channels close to integer multiples of the reference where the difference frequency can be inside the loop bandwidth (thus the name, integer boundary spurs).

### Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers because the reference offset is far outside the loop bandwidth. However, any reference feedthrough mechanism that bypasses the loop can cause a problem. Feedthrough of low levels of on-chip reference switching noise, through the prescaler back to the VCO, can result in reference spur levels as high as −85 dBc.

## LOCK TIME

The PLL lock time divides into a number of settings. All of these settings are modeled in the ADIsimPLL design tool.

Much faster lock times than those detailed in this data sheet are possible; contact Analog Devices for more information.

### Lock Time—A Worked Example

Assume that $f_{PFD}$ = 61.44 MHz,

$VCO\ Band\ Div$ = ceiling($f_{PFD}$/1,600,000) = 39

where ceiling() is a function that rounds up to the nearest integer.

By combining

$ALC\ Wait > (50\ \mu s \times f_{PFD})/Timeout$

$Synthesizer\ Lock\ Timeout > (20\ \mu s \times f_{PFD})/Timeout$

It is found that

$ALC\ Wait = 2.5 \times Synthesizer\ Lock\ Timeout$

The ALC wait and synthesizer lock timeout values must be set to fulfill this equation. Both values are 5 bits wide; therefore, the maximum value for either is 31. There are several suitable values.

The following values meet the criteria:

$ALC\ Wait$ = 30

$Synthesizer\ Lock\ Timeout$ = 12

Finally, ALC wait > (50 μs × $f_{PFD}$)/Timeout, is rearranged for

$Timeout$ = ceiling(($f_{PFD} \times 50\ \mu s$)/$ALC\ Wait$)

$Timeout$ = ceiling((61.44 MHz × 50 μs)/30) = 103

### Synthesizer Lock Timeout

The synthesizer lock timeout ensures that the VCO calibration DAC, which forces $V_{TUNE}$, has settled to a steady value for the band select circuitry.

The timeout and synthesizer lock timeout variables programmed in Register 9 select the length of time the DAC is allowed to settle to the final voltage, before the VCO calibration process continues to the next phase, which is VCO band selection. The PFD frequency is the clock for this logic, and the duration is set by

$$\frac{Timeout \times Synthesizer\ Lock\ Timeout}{f_{PFD}}$$

The calculated time must be equal to or greater than 20 μs.

### VCO Band Selection

Use the PFD frequency again as the clock for the band selection process. Calculate this value by

$f_{PFD}$/($VCO\ Band\ Selection \times 16$) < 100 kHz

The band selection takes 11 cycles of the previously calculated value. Calculate the duration by

$11 \times (VCO\ Band\ Selection \times 16)/f_{PFD}$

### Automatic Level Calibration Timeout

Use the automatic level calibration (ALC) function to choose the correct bias current in the ADF4356 VCO core. Calculate the time taken by

$30 \times ALC\ Wait \times Timeout/f_{PFD}$

### PLL Low-Pass Filter Settling Time

The time taken for the loop to settle is inversely proportional to the low-pass filter bandwidth. The settling time is also modeled in the ADIsimPLL design tool.

The total lock time for changing frequencies is the sum of the four separate times (synthesizer lock, VCO band selection, ALC timeout, and PLL settling time) and is all modeled in the ADIsimPLL design tool.

# APPLICATIONS INFORMATION

## POWER SUPPLIES

The ADF4356 contains four multiband VCOs that cover an octave range of frequencies. To ensure the best performance, it is vital to connect a low noise regulator, such as the ADM7150 or the ADM7170 to the $V_{VCO}$ pin. Connect the same regulator to package pins $V_{VCO}$, $V_{REGVCO}$, and $V_P$.

For the 3.3 V supply pins, use two ADM7170 regulators, one for the $DV_{DD}$ and $AV_{DD}$ supplies and one for $V_{RF}$. Figure 43 shows the recommended connections.

## PRINTED CIRCUIT BOARD (PCB) DESIGN GUIDELINES FOR A CHIP-SCALE PACKAGE

The lands on the 32-lead, lead frame chip scale package are rectangular. The PCB pad for these lands must be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. Center each land on the pad to maximize the solder joint size.

The bottom of the chip scale package has a central exposed thermal pad. The thermal pad on the PCB must be at least as large as the exposed pad.

On the PCB, there must be a minimum clearance of 0.25 mm between the thermal pad and the inner edges of the pad pattern. This clearance ensures the avoidance of shorting.

To improve the thermal performance of the package, use thermal vias on the PCB thermal pad. If vias are used, incorporate them into the thermal pad at the 1.2 mm pitch grid. The via diameter must be between 0.3 mm and 0.33 mm, and the via barrel must be plated with 1 oz. of copper to plug the via.

For a microwave PLL and VCO synthesizer, such as the ADF4356, take care with the board stack-up and layout. Do not consider using FR4 material because it is too lossy above 3 GHz. Instead, Rogers 4350, Rogers 4003, or Rogers 3003 dielectric material is suitable.

Take care with the RF output traces to minimize discontinuities and ensure the best signal integrity. Via placement and grounding are critical.
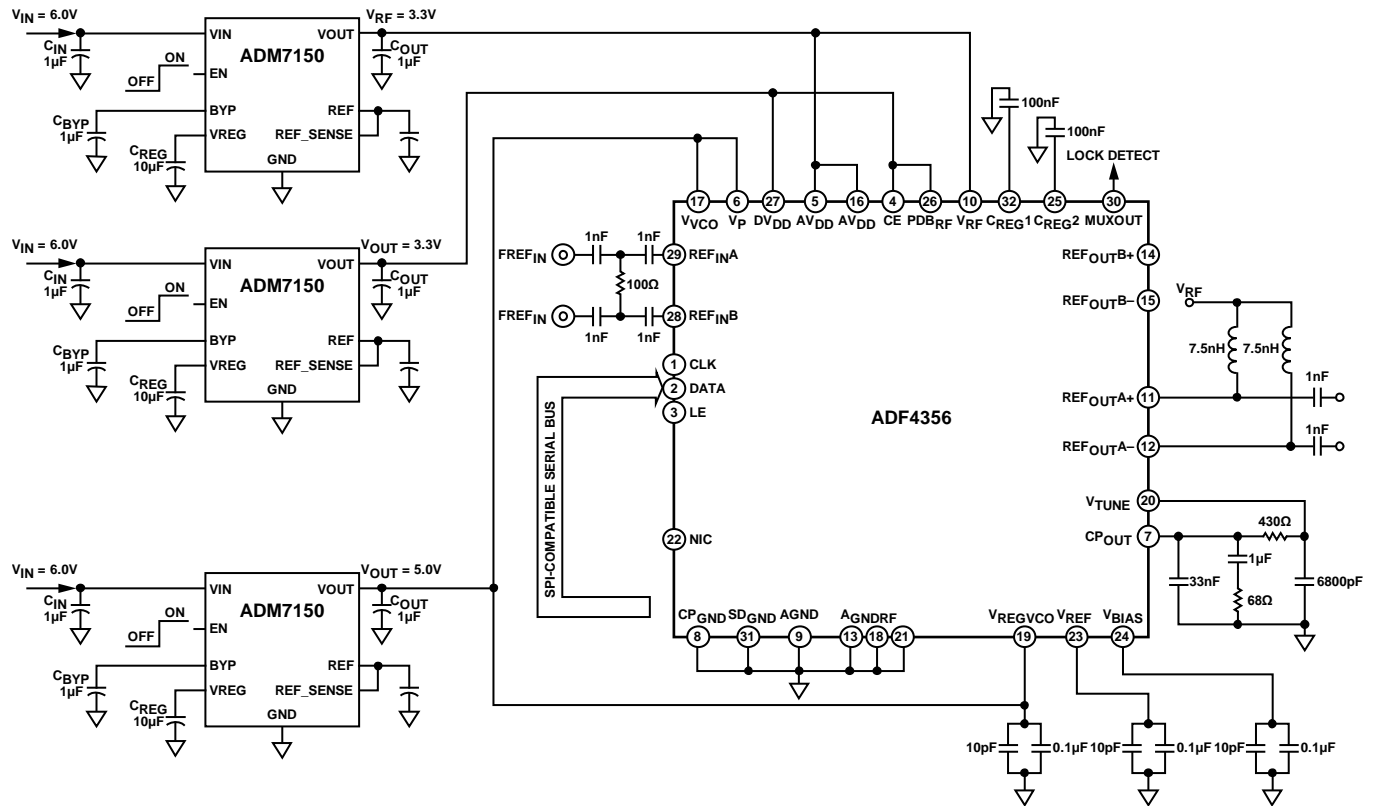


*Figure 43. Power Supplies*

## OUTPUT MATCHING

The low frequency output can simply be ac-coupled to the next circuit, if desired; however, if a higher output power is required, use a pull-up inductor to increase the output power level.
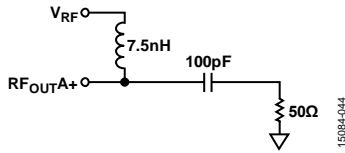


*Figure 44. Optimum Output Stage*

When differential outputs are not required, terminate the unused output or combine it with both outputs using a balun.

For lower frequencies below 2 GHz, it is recommended to use a 100 nH inductor on the RF$_{OUT}$A+/RF$_{OUT}$A− pins and a 100 pF ac coupling capacitor.

The RF$_{OUT}$A+/RF$_{OUT}$A− pins are a differential circuit. Provide each output with the same (or similar) components where possible, such as the same shunt inductor value, bypass capacitor, and termination.

The RF$_{OUT}$B+/RF$_{OUT}$B− outputs can be treated the same as the RF$_{OUT}$A+/RF$_{OUT}$A− outputs. If unused, leave both RF$_{OUT}$B+/RF$_{OUT}$B− pins open.

## OUTLINE DIMENSIONS
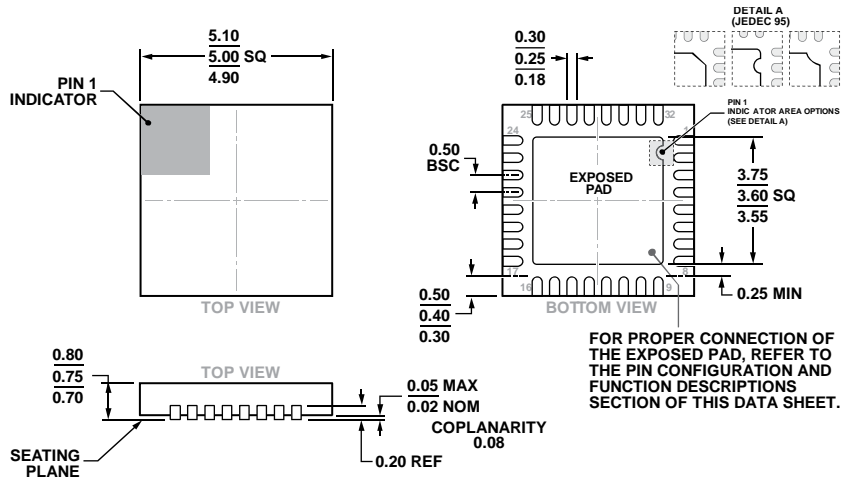


COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-5.

*Figure 45. 32-Lead Lead Frame Chip Scale Package [LFCSP]*
*5 mm × 5 mm Body and 0.75 mm Package Height*
*(CP-32-12)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADF4356BCPZ | −40°C to +85°C | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-12 |
| ADF4356BCPZ-RL7 | −40°C to +85°C | 32-Lead Lead Frame Chip Scale Package [LFCSP] | CP-32-12 |
| EV-ADF4356SD1Z | | Evaluation Board | |

[1] Z = RoHS Compliant Part.

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