Microwave Wideband Synthesizer with Integrated VCO

FEATURES

- Output frequency range: 800 MHz to 12.8 GHz
- Jitter < 30 fs_{RMS} f_{OUT} = 9.001 GHz, f_{REF} = f_{PFD} = 250 MHz, fractional mode
- Wideband phase noise floor: −160 dBc/Hz at 12.8 GHz
- PLL specifications
  - Normalized in-band phase noise floor
    - −239 dBc/Hz: integer, −237 dBc/Hz: fractional mode
  - Normalized 1/f phase noise floor
    - −287 dBc/Hz: normalized to 1 Hz
    - −147 dBc/Hz: normalized to 1 GHz at 10 kHz
  - 625 MHz phase detector frequency integer mode
  - 250 MHz phase detector frequency fractional mode
  - 25-bit fixed, 49-bit combined fractional modulus
  - 4 GHz reference input frequency
  - Typical −95 dBc PFD spurs
- Reference to output delay specifications
  - Temperature coefficient: 0.06 ps/°C
  - Adjustment step size: <1 ps
- Multichip output phase alignment
  - Through SYNC pin or by EZSync method
- 3.3 V and 5 V power supplies
- ADIsimPLL™ loop filter design tool support
- Available in 48-lead, 7 mm × 7 mm LGA package
- −40°C to +125°C operating junction temperature

APPLICATIONS

- Wireless infrastructure (MC-GSM, 5G)
- Test and measurement
- Aerospace and defense

GENERAL DESCRIPTION

The ADF4368 is a high performance, ultra-low jitter, integer-N and fractional-N phase-locked loop (PLL) with integrated VCO ideally suited for frequency conversion applications.

The high performance PLL has a figure of merit of −239 dBc/Hz, very low 1/f noise of normalized −287 dBc/Hz and high PFD frequency that can achieve ultra-low in-band noise and integrated jitter. The ADF4368 can generate any frequency from 800 MHz to 12.8 GHz without an internal doubler, which eliminates the need for sub-harmonic filters. The Σ-Δ modulator includes a 25-bit fixed modulus that allows hertz frequency resolution and an additional 17-bit variable modulus, which allows even finer resolution and flexibility for frequency planning. The 9 dBm output power at 12.8 GHz in single-ended configuration with 16 step power adjust feature makes it very useful for any application.

For multiple frequency conversion applications, such as phase array radar or massive MIMO systems, the outputs of multiple ADF4368 can be aligned by using the SYNC input or EZSync™. The EZSync method is used when it is difficult to distribute the SYNC signal to all devices precisely. For applications that require deterministic delay or delay adjustment capability, a programmable reference to output delay with <1 ps resolution is provided. The reference to output delay is guaranteed across multiple devices and temperature, allowing for predictable and precise multichip alignment.

The simplicity of the ADF4368 block diagram eases development time with a simplified serial-peripheral interface (SPI) register map, external SYNC input, and repeatable multichip phase alignment both in integer mode and fractional mode.

FUNCTIONAL BLOCK DIAGRAM

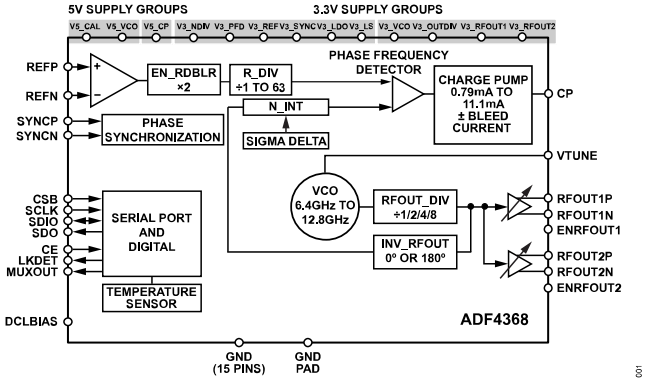

Figure 1. ADF4368 Block Diagram

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REVISION HISTORY

3/2023—Revision 0: Initial Version

SPECIFICATIONS

$V_{3.3V\_1}$ = $V_{3.3V\_2}$ = 3.15 V to 3.45 V, V_{V5_VCO} = V_{V5_CP} = V_{V5_CAL} = 4.75 V to 5.25 V, all voltages are with respect to GND, T_A = −40°C to 105°C operating temperature range, unless otherwise noted.

Table 1. Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUTS (REFP, REFN)						
Input Frequency	f_{REF}	10		4000	MHz	
Input Signal Level	V_{REF}	0.5		2.6	V p-p	Differential
Min Input Slew Rate			100		V/µs	
Input Duty Cycle			50		%	
Self-Bias Voltage			1.85		V	
Input Resistance			3		kΩ	Differential
Input Capacitance			1		pF	Differential
Input Current			2		µA	
REFERENCE PEAK DETECTOR						
Input Frequency		10		4000	MHz	
Minimum Input Signal Detected (REF_OK = 1)			200		mV_{pp}	f_{REF} = 100 MHz, single-ended sine wave
Maximum Input Signal Not Detected (REF_OK = 0)			160		mV_{pp}	f_{REF} = 100 MHz, single-ended sine wave
SYNC INPUTS (SYNCP, SYNCN)						
Input Signal Level	V_{REF}	0.4[1]		2.6[1]	V p-p	LVDS mode, differential
	V_{REF}	0.5[1]		2.6[1]	V p-p	CML mode, differential
Self-Bias Voltage			1.3		V	LVDS mode
			1.85		V	CML mode
Input Resistance			3		kΩ	Differential
Input Capacitance			1		pF	Differential
Input Current			3		µA	
REFERENCE DIVIDER (R)						
R		1		63		All integers included
REFERENCE DOUBLER						
Input Frequency	f_{RDBL}	10		250	MHz	EN_RDBLR = 1
PHASE/FREQUENCY DETECTOR (PFD)						
Input Frequency	f_{PFD}					
		3[1]		625	MHz	Integer mode
		3[1]		250	MHz	Fractional mode sync or non-sync applications
		3[1]		250[1]	MHz	Fractional mode phase resync applications when f_{OUT} ≥ 3 GHz
		75[1]		250[1]	MHz	Fractional mode phase resync applications when f_{OUT} < 3 GHz
CHARGE PUMP (CP)						
Output Current Range	I_{CP}		0.79 to 11.1		mA	Set by CP_I
Output Current Source/Sink Accuracy			±2		%	All setting, = V_{CP} = V_{V5_CP} /2
Output Current Source/Sink Matching			±2		%	All setting, V_{CP} = V_{V5_CP} /2
Output Current vs. Output Volt Sensitivity			0.2		%V/V	1.4 V < V_{V5_CP} < V_{CP-5V} − 1.6 V
Output Current vs. Temperature			400		ppm/C	V_{CP} = V_{V5_CP} /2
Output High-Z Leakage Current			−0.01		µA	Minimum I_{CP}, 1.4 V < V_{V5_CP} < V_{CP-5V} − 1.6 V
Output High-Z Leakage Current			−0.3		µA	Maximum I_{CP}, 1.4 V < V_{V5_CP} < V_{CP-5V} − 1.6 V
VCO						
Frequency Range	f_{VCO}	6.4		12.8	GHz	
Tuning Sensitivity[2, 3]	K_{VCO}		0.75 to 1.25		%Hz/V	

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DIV_RCLK VCO Calibration Frequency	f_{DIV_RCLK}			125	MHz	Must set DCLK_MODE = 1, when f_{DIV_RCLK} > 80 MHz
FEEDBACK (N) AND OUTPUT DIVIDER (O)						
N		4		4095		Integer mode
		19		4095		Fractional mode
O		1		8		1, 2, 4, 8
RF OUTPUTS (RFOUT1P/N, RFOUT2P/N)						Differential termination = 100 Ω for all RF output specifications, unless noted
Output Frequency	f_{OUT}	0.8		12.8	GHz	
Output Single-Ended Power	V_{OD}		9		dBm	CLK1_OPWR = CLK2_OPWR = 15, f_{OUT} = 4 GHz to 12.8 GHz
			5.5		dBm	CLK1_OPWR = CLK2_OPWR = 10, f_{OUT} = 4 GHz to 12.8 GHz
			1.5		dBm	CLK1_OPWR = CLK2_OPWR = 5, f_{OUT} = 4 GHz to 12.8 GHz
			−2		dBm	CLK1_OPWR = CLK2_OPWR = 0, f_{OUT} = 4 GHz to 12.8 GHz
Output Resistance			100		Ω	Differential
Output Common Mode			$V_{3.3V\_2}$ − V_{OD}		V	No pull-up inductor
			$V_{3.3V\_2}$		V	With pull-up inductor
Output Rise Time	t_R		18		ps	20%-80%, CLK1_OPWR = CLK2_OPWR = 10,
Output Fall Time	t_F		18		ps	80%-20%, CLK1_OPWR = CLK2_OPWR = 10,
Output Duty Cycle			50		%	
Skew, RFOUT1 to RFOUT2			3 ± 1		ps	One ADF4368 device
			3 ± 1		ps	Across multiple ADF4368 devices, T_J within 10°C, same R_DIV, CLKOUT_DIV, EN_RDBLR used
REFERENCE INPUT TO OUTPUT DELAY						Device setup for all delay specifications, unless noted, measure rising reference edge at REFP input to rising edge at RFOUT1P output
Propagation Delay	t_{PD}		190		ps	REF_SEL = 0, R = 1, doubler = disabled
Propagation Delay Temperature Coefficient	t_{PD}		0.06		ps/°C	REF_SEL = 0
LOGIC INPUTS (CSB, SCLK, SDIO, ENCLK1, ENCLK2)						
Input High Voltage	V_{INH}	1.2			V	
Input Low Voltage	V_{INL}			0.6	V	
Input Current (High, Low)	I_{IH}/I_{IL}			±1	μA	
Input Capacitance	C_{IN}		2		pF	
LOGIC INPUT (CE)						
Input High Voltage	V_{INH-3V}	1.8			V	
Input Low Voltage	V_{INL-3V}			0.8	V	
Input Current (High, Low)	I_{IH-3V}/I_{IL-3V}			±1	μA	
Input Capacitance	C_{IN-3V}		1		pF	
LOGIC OUTPUTS (SDIO, SDO, LKDET, MUXOUT)						
Output High Voltage	V_{OH}	1.5	1.8		V	I_{OH} = 500 μA, 1.8 V output selected (default setting)
Output High Voltage	V_{OH-3V}	$V_{3.3V}$ − 0.4				I_{OH} = 500 μA, 3.3 V output selected, set by voltage on V_LDO pin

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 500 µA
SDO High-Z Leakage	I_{ZH}/I_{ZL}			±1	µA	
POWER SUPPLIES						Device setup is default configuration for all supply current specifications, unless noted
V5_VCO Supply Range	V_{V5_VCO}	4.75	5	5.25	V	
V5_CAL Supply Range	V_{V5_CAL}	4.75	5	5.25	V	
V5_CP Supply Range	V_{V5_CP}	4.75	5	5.25	V	
$V_{3.3V\_1}$ Supply Range	$V_{3.3V\_1}$	3.15	3.3	3.45	V	Group 1: V3_LS, V3_LDO, V3_REF, V3_PFD, V3_NDIV, V3_SYNC
$V_{3.3V\_2}$ Supply Range	$V_{3.3V\_2}$	3.15	3.3	3.45	V	Group 2: V3_RFOUT1, V3_RFOUT2, V3_VCO, V3_CLKDIV
V5_VCO Supply Current	I_{V5_VCO}		98		mA	f_{OUT} = 12.8 GHz
			173	220	mA	f_{OUT} = 6.4 GHz
V5_CAL Supply Current	I_{V5_CAL}		50		µA	
			8		mA	During VCO calibration
V5_CP Supply Current	I_{V5_CP}		58	67	mA	I_{CP} = 11.1 mA, CP_I = 15
			41		mA	I_{CP} = 0.79 mA, CP_I = 0
			3.2		mA	Additional current when EN_BLEED = 1, BLEED_I = 8191
$V_{3.3V\_1}$ Supply Current	$I_{3.3V\_1}$		185	210	mA	f_{REF} = 122.88 MHz, f_{PFD} = 245.76 MHz, fractional mode, CP_I = 15, PD_SYNC = 1 (sync disabled)
			4		mA	Additional current when PD_LD = 0
			4		mA	Additional current when PD_RDET = 1
V3_SYNC Supply Current	I_{V3_SYNC}		15		mA	PD_SYNC = 0 (synchronization is enabled)
V3_RFOUTx Supply Current	I_{V3_RFOUT}		35		mA	CLKx_OPWR = 0
			47		mA	CLKx_OPWR = 4
			65		mA	CLKx_OPWR = 8
			90		mA	CLKx_OPWR = 12
			105		mA	CLKx_OPWR = 15
V3_OUTDIV Supply Current	I_{V3_OUTDIV}		108		mA	CLKOUT_DIV = 0 (divide by 1)
			132		mA	CLKOUT_DIV = 3 (divide by 8)
$V_{3.3V\_2}$ Supply Current	$I_{3.3V\_2}$		149		mA	ENRFOUT1 = low, CLK2_OPWR = 0 (minimum power), CLKOUT_DIV = 0, f_{OUT} = 9.6 GHz
			218		mA	ENRFOUT1 = low, CLK2_OPWR = 15 (maximum power), CLKOUT_DIV = 0, f_{OUT} = 9.6 GHz
			172		mA	ENRFOUT1 = low, CLK2_OPWR = 0 (minimum power), CLKOUT_DIV = 1, f_{OUT} = 5.6 GHz
			241		mA	ENRFOUT1 = low, CLK2_OPWR = 15 (maximum power), CLKOUT_DIV = 1, f_{OUT} = 5.6 GHz
Typical Power Dissipation	P_{DIS}		2.3		W	ENRFOUT1 = low, CLK2_OPWR = 15 (maximum power), CLKOUT_DIV = 0, f_{OUT} = 9.6 GHz, SYNC block powered down, fractional mode
			2.1		W	ENRFOUT1 = low, CLK2_OPWR = 15 (maximum power), CLKOUT_DIV = 1, f_{OUT}

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
						= 5.6 GHz, SYNC block powered down, fractional mode
Typical Power Down Current, 3.3 V			11	15	mA	PD_ALL = 1, $I_{3.3V\_1}$ + $I_{3.3V\_2}$
Typical Power Down Current, 5 V Supplies			350	750	µA	PD_ALL = 1, I_{V5_VCO} + I_{V5_CAL} + I_{V5_CP}
Typical Disable Current, 3.3 V Supplies			100	1500	µA	CE = low, $I_{3.3V\_1}$ + $I_{3.3V\_2}$
Typical Disable Current, 5 V Supplies			350	750	µA	CE = low, I_{V5_VCO} + I_{V5_CAL} + I_{V5_CP}
RF OUTPUT NOISE CHARACTERISTICS						
12.8 GHz Output Frequency						f_{REF} = f_{PFD} = 250 MHz, fractional mode, CP_I = 15
Phase Noise Floor			−160		dBc/Hz	
RMS Jitter, 100 Hz to 100 MHz Integration			32		fs_{RMS}	
9.001 GHz Output Frequency						f_{REF} = f_{PFD} = 250 MHz, fractional mode, CP_I = 15
Phase Noise Floor			−160		dBc/Hz	
RMS Jitter, 100 Hz to 100 MHz Integration			29		fs_{RMS}	
7.6 GHz Output Frequency						f_{REF} = f_{PFD} = 250 MHz, fractional mode, CP_I = 15
Phase Noise Floor			−160		dBc/Hz	
RMS Jitter, 100 Hz to 100 MHz Integration			31		fs_{RMS}	
6.4 GHz Output Frequency						f_{REF} = f_{PFD} = 250 MHz, fractional mode, CP_I = 15
Phase Noise Floor			−161		dBc/Hz	
RMS Jitter, 100 Hz to 100 MHz Integration			30		fs_{RMS}	
5.025 GHz Output Frequency						f_{REF} = f_{PFD} = 250 MHz, fractional mode, CP_I = 15
Phase Noise Floor			−163		dBc/Hz	
RMS Jitter, 100 Hz to 100 MHz Integration			33		fs_{RMS}	
Normalized In-Band Phase Noise Floor[4]						
$L_{NORM-INT}$			−239		dBc/Hz	
$L_{NORM-FRC}$			−237		dBc/Hz	
Normalized 1/f Phase Noise Floor[4, 5]						
$L_{1/f}$[5]			−287		dBc/Hz	Normalized to 1 Hz
L_{1/f_1G_10k}[5]			−147		dBc/Hz	Normalized to 1 GHz at 10 kHz offset
Integer Boundary Spurs (Filtered)	IBS		−95		dBc	Spur is out of the loop bandwidth
Integer Boundary Spurs (Unfiltered)	IBS		−60		dBc	Measured at 5 kHz offset from integer channel
PFD Spur			−95		dBc	
TEMPERATURE SENSOR (ADC)						
ADC Clock Frequency	f_{ADC_CLK}			400	kHz	ADC clock divider output
ADC Clock Divider Frequency	f_{ADC_CLKDIV}			125	MHz	ADC clock divider input
Resolution				8	Bits	

[1] Based on design and characterization.

[2] Valid for 1.60 V ≤ V_{VTUNE} ≤ 2.85 V with device calibrated after a power cycle or software power-on reset.

[3] Based on characterization.

[4] These numbers are modeled in ADIsimPLL.

[5] Integration Range 1 kHz to f_{OUT}.

SPECIFICATIONS

SERIAL INTERFACE TIMING CHARACTERISTICS

$V_{3.3V\_1}$ = $V_{3.3V\_2}$ = 3.15 V to 3.45 V, V_{V5_VCO} = V_{V5_CP} = V_{V5_CAL} = 4.75 V to 5.25 V, all voltages are with respect to GND, T_A = −40°C to +105°C operating temperature range, unless otherwise noted.

Table 2. Serial Interface Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL INTERFACE (CSB, SCLK, SDIO, SDO)						See Figure 2, Figure 3, and Figure 4
SCLK Frequency	f_{SCLK}			65	MHz	
SCLK Pulse Width High	t_{HIGH}	7.6			ns	
SCLK Pulse Width Low	t_{LOW}	7.6			ns	
SDIO Setup Time	t_{DS}	3			ns	
SDIO Hold Time	t_{DH}	3			ns	
SCLK Fall Edge to SDIO Valid Prop Delay	t_{ACCESS_SDIO}	7.6			ns	
SCLK Fall Edge to SDO Valid Prop Delay	t_{ACCESS_SDO}	7.6			ns	
CSB Rising Edge to SDIO High-Z	t_Z	7.6			ns	
CSB Falling Edge to SCLK Rise Setup Time	t_S	3			ns	
SCLK Rising Edge to CSB Rise Hold Time	t_H	3			ns	

TIMING DIAGRAMS

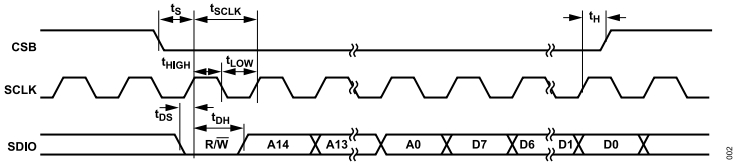

Figure 2. Write Timing Diagram

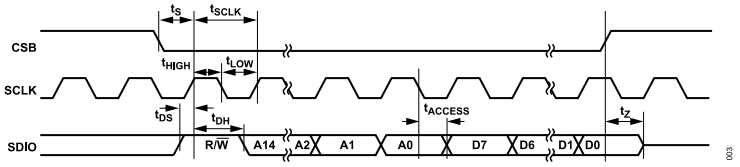

Figure 3. 3-Wire Read Timing Diagram (SDO_ACTIVE = 0)

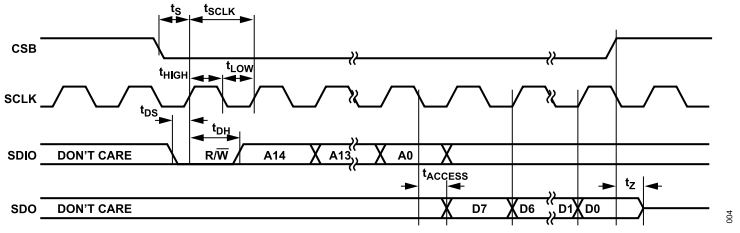

Figure 4. 4-Wire Read Timing Diagram (SDO_ACTIVE = 1)

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3. Absolute Maximum Ratings

Parameter	Rating
$V_{3.3V\_1}$ (V3_LS, V3_LDO, V3_REF, V3_PFD, V3_NDIV) to GND	−0.3 V to +3.6 V
$V_{3.3V\_2}$ (V3_VCO, V3_OUTDIV, V3_RFOUT1, V3_FOUT2) to GND	−0.3 V to +3.6 V
V_{5V} (V5_CAL, V5_VCO, V5_CP) to GND	−0.3 V to +5.5 V
Voltage on CP Pin	−0.3 V to V5_CP + 0.3 V
Digital Outputs (MUXOUT, LKDET, SDO, SDIO)	5 mA
RFOUT1P, RFOUT1N, RFOUT2P, RFOUT2N	Maximum (GND − 0.3 V, $V_{3.3V\_2}$ − 1.2 V) to $V_{3.3V\_2}$ + 0.3 V
REFP, REFN	−0.65 V to $V_{3.3V\_1}$ + 0.65 V
Voltage on all Other Pins	−0.3 V to $V_{3.3V\_1}$ + 0.3 V
REFP to REFN and SYNCP to SYNCN	±1.35 V
Temperature	
Operating Junction Range[1]	−40°C to +125°C
Storage Range	−65°C to +125°C
Maximum Junction	125°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	30 sec

[1] Device is guaranteed to meet the specified performance limits over the full operating junction temperature range.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

TRANSISTOR COUNT

The transistor count for the ADF4368 is 199076 (CMOS) and 3366 (bipolar).

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction-to-case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	$\theta_{JC\text{-}TOP}$	$\theta_{JC\text{-}BOTTOM}$	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
CC-48-13[1]	22.38	16.86	5.1	8.33	1.35	7.89	°C/W

[1] Test Condition 1: thermal impedance simulated values are based on use of a 4-layer PCB with the thermal impedance paddle soldered to a ground plane.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDDEC JS-001.
Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADF4368

Table 5. ESD Ratings for ADF4368

ESD Model	Withstand Threshold (V)	Class
HBM	4000	3A
CDM	1000	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

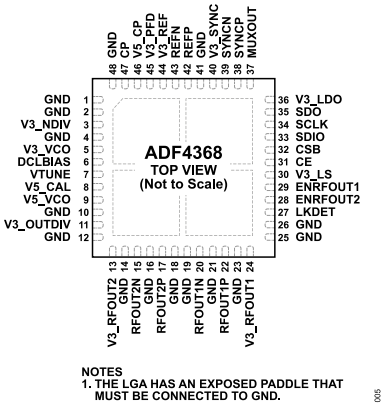

Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

Pin Number	Mnemonic	Description
1, 2, 4, 10, 12, 14, 16, 18, 19, 21, 23, 25, 26, 41, 48	GND	Negative Power Supply (Ground). These pins must be tied directly to the ground pad.
3	V3_NDIV	3.15 V to 3.45 V Positive Power Supply Pin for the PLL Feedback Divider Circuitry. Short this pin to the other pins in 3.3 V power supply group 1.
5	V3_VCO	3.15 V to 3.45 V Positive Power Supply Pin for the 3.3 V Portion of the VCO Circuitry. Short this pin to the other pins in 3.3 V power supply group 2.
6	DCLBIAS	Do not connect to this pin.
7	VTUNE	VCO Tuning Input. This frequency control pin is normally connected to the external loop filter.
8	V5_CAL	4.75 V to 5.25 V Positive Power Supply Pin for VCO Calibration Circuitry. This pin can be shorted to the V5_VCO supply plane.
9	V5_VCO	4.75 V to 5.25 V Positive Power Supply Pin for the 5 V Portion of the VCO Circuitry.
11	V3_OUTDIV	3.15 V to 3.45 V Positive Power Supply Pin for the Output Divider Circuitry. Short this pin to the other pins in 3.3 V power supply group 2.
13	V3_RFOUT2	3.15 V to 3.45 V Positive Power Supply Pin for the RF Output 2 Buffer Circuitry. Short this pin to the other pins in 3.3 V power supply group 2.
15, 17	RFOUT2N, RFOUT2P	RF Output 2 Signal. The VCO output divider is buffered and presented differentially on these pins. The outputs have 50 Ω (typical) output resistance per side (100 Ω differential). The far end of the transmission line is typically terminated with 100 Ω connected across the outputs. The output amplitude is programmable via the serial port.
20, 22	RFOUT1N, RFOUT1P	RF Output 1 Signal. The VCO Output Divider is buffered and presented differentially on these pins. The outputs have 50 Ω (typical) output resistance per side (100 Ω differential). The far end of the transmission line is typically terminated with 100 Ω connected across the outputs. The output amplitude is programmable via the serial port.
24	V3_RFOUT1	3.15 V to 3.45 V Positive Power Supply Pin for the RF Output 1 Buffer Circuitry. Short this pin to the other pins in 3.3 V power supply group 2.
27	LKDET	PLL Lock Detect. This output presents the lock status of the PLL. PLL is locked when LKDET is a logic high.
28	ENRFOUT2	Enable RF Output 2 Buffer. 3.3 V CMOS input. When ENRFOUT2 = high, the RFOUT2P and RFOUT2N output buffer is active. When ENRFOUT2 = low, RFOUT2P and RFOUT2N are powered down.
29	ENRFOUT1	Enable RF Output 1 Buffer. 3.3 V CMOS input. When ENRFOUT1 = high, the RFOUT1P and RFOUT1N output buffer is active. When ENRFOUT2 = low, RFOUT1P and RFOUT1N are powered down.
30	V3_LS	3.15 V to 3.45 V Positive Power Supply Pin for the Internal Level Shift Circuitry. Short this pin to the other pins in 3.3 V power supply group 1.
31	CE	Chip-Enable. Does not support 1.8 V CMOS levels. This CMOS input enables the device when driven high. A logic low disables the device, putting the device in a full power down state causing the register to reset. Conversely, the PD_ALL bit powers down the device, but does not reset the registers.
32	CSB	Serial Port Chip Select. 1.8 V and 3.3 V compatible CMOS input. This CMOS input initiates a serial port communication burst when driven low, ending the burst when driven back high.
33	SDIO	Serial Data Input/Output. 1.8 V and 3.3 V programmable CMOS input/output. When configured as an input, the serial port uses this CMOS input for data. In 3-wire readback mode (default mode), this pin outputs data from the serial port during a read communication burst.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Pin Number	Mnemonic	Description
34	SCLK	Serial Port Clock. 1.8 V and 3.3 V compatible. This CMOS input clocks serial port input data on its rising edge.
35	SDO	Optional Serial Data Output. 1.8 V and 3.3 V programmable CMOS output. In 3-wire mode (default mode), this three-state CMOS pin remains in a high impedance state. In 4-wire readback mode, this pin presents data from the serial port during a read communication burst. When the CSB is deasserted, SDO returns to a high impedance. Optionally, attach a resistor of >200 kΩ to prevent a floating output.
36	V3_LDO	3.15 V to 3.45 V Positive Power Supply Pin for the Internal LDO Circuitry. Short this pin to the other pins in 3.3 V power supply group 1.
37	MUXOUT	Internal Device Mux Output. This output pin can be connected to multiple internal nodes for factory test and debug purposes.
38, 39	SYNCP, SYNCN	Synchronization Input Signals. Both RF output signals are synchronized to an input signal at this pin. It is used for multichip phase synchronization. This differential input can accept both high and low common mode input signals (based on a SPI bit setting).
40	V3_SYNC	3.15 V to 3.45 V Positive Power Supply for the Synchronization Circuitry. Short this pin to the other pins in 3.3 V power supply group 1.
42, 43	REFP, REFN	Reference Input Signal. This differential input is buffered with a delay matched amplifier (DMA) for well controlled reference to output propagation delays (default mode, REF_SEL = 0). For low slew rate reference input signals, an alternate low noise amplifier (LNA) can be selected via the serial port (REF_SEL = 1). Reference inputs are self-biased and must be AC-coupled with 1 µF capacitors. Reference inputs accept differential or single-ended inputs.
44	V3_REF	3.15 V to 3.45 V Positive Power Supply Pin for the PLL Reference Circuitry. Short this pin to the other pins in 3.3 V power supply group 1.
45	V3_PFD	3.15 V to 3.45 V Positive Power Supply Pin for PFD Circuitry. Short this pin to the other pins in 3.3 V power supply group 1.
46	V5_CP	4.75 V to 5.25 V Positive Power Supply Pin for Charge Pump Circuitry. Isolate this pin from the V5_VCO supply plane.
47	CP	Charge Pump Output. This bidirectional current output is normally connected to the external loop filter.
Exposed Pad	EP	Exposed Pad. The LGA has an exposed paddle that must be connected to GND (Negative power supply). The exposed pad must be soldered directly to the PCB land. The PCB land pattern must have multiple thermal vias to the ground plane for both low ground inductance and also low thermal resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

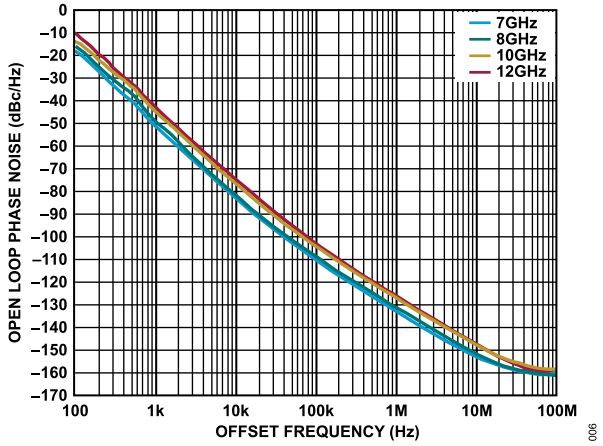

Figure 6. Open Loop VCO Phase Noise vs. Offset Frequency at Various Frequencies

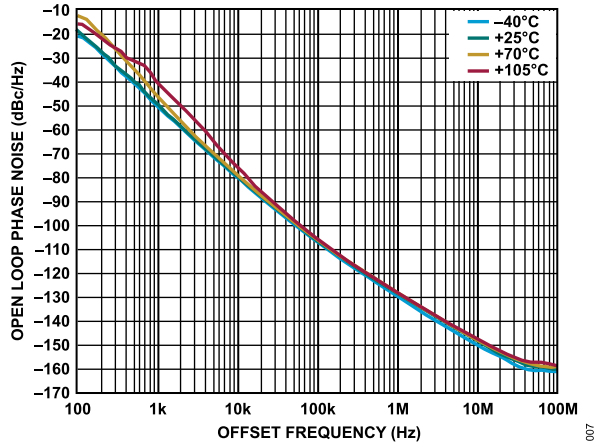

Figure 7. 12 GHz Open Loop VCO Phase Noise vs. Offset Frequency at Various Temperatures

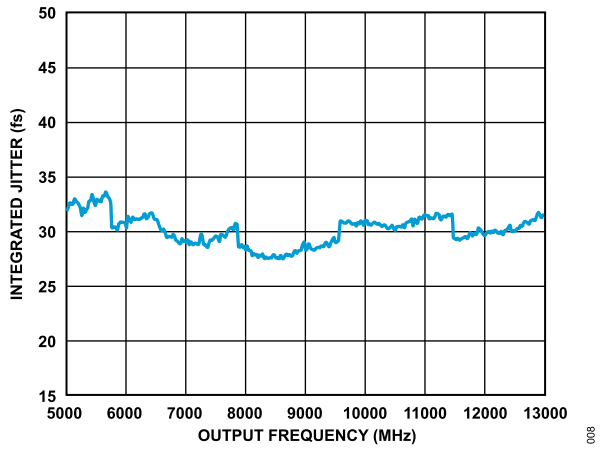

Figure 8. 1 kHz to 100 MHz Integrated Jitter in Fractional Mode f_{PFD} = 250 MHz

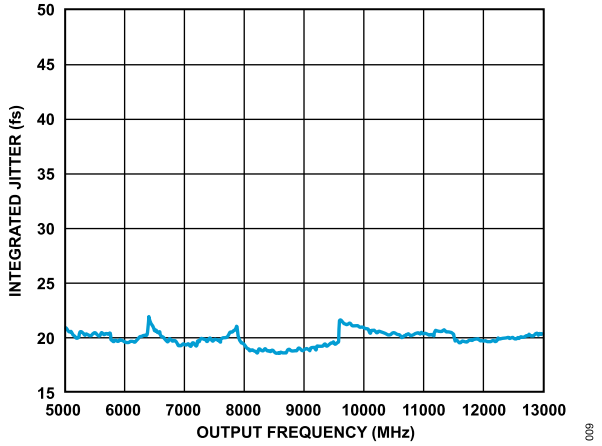

Figure 9. 1 kHz to 100 MHz Integrated Jitter in Integer Mode f_{PFD} = 500 MHz

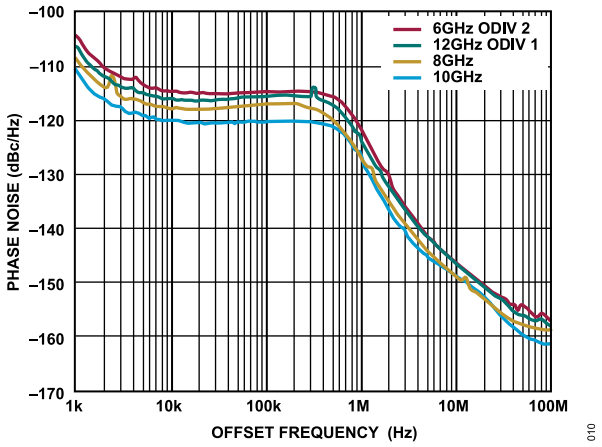

Figure 10. Close Loop Phase Noise at Various Frequencies

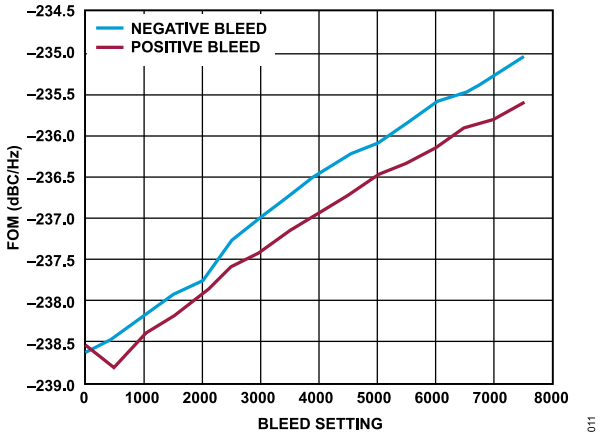

Figure 11. $L_{NORM-INT}$ vs. Bleed Setting

TYPICAL PERFORMANCE CHARACTERISTICS

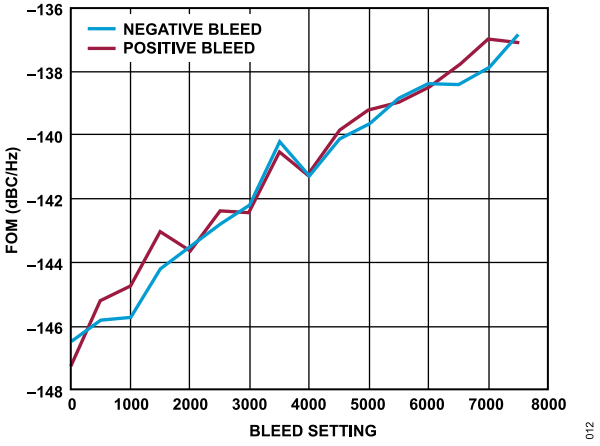

Figure 12. $L_{1/f}$ vs. Bleed Setting

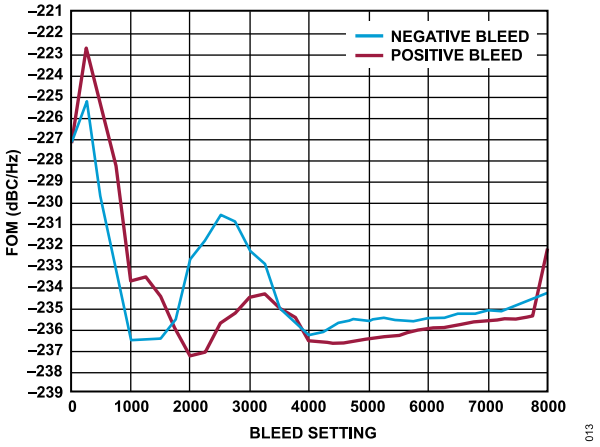

Figure 13. $L_{NORM-FRC}$, f_{REF} = 500 MHz, f_{PFD} = 250 MHz, RF_{Out} = 12,001 MHz vs. Bleed Setting

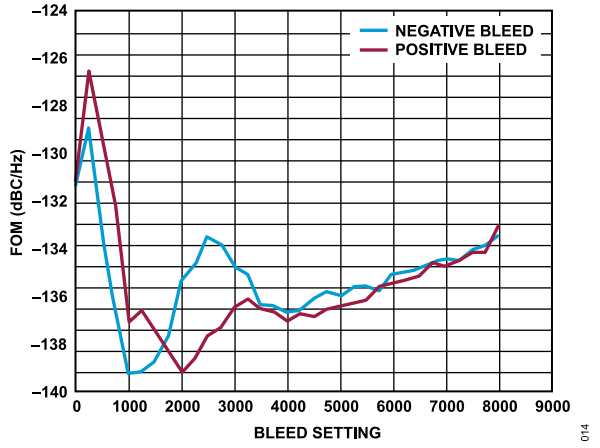

Figure 14. $L_{NORM-FRC}$ vs. Bleed Setting

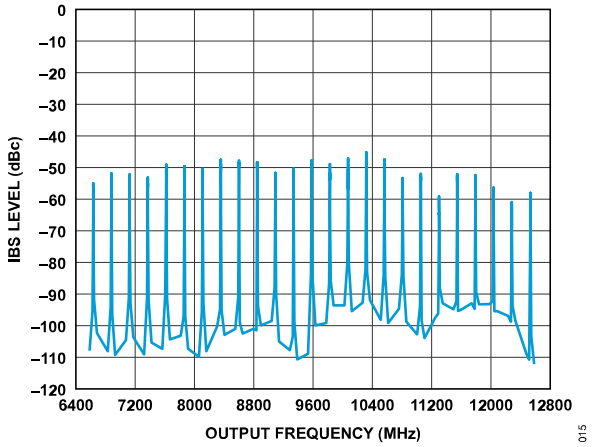

Figure 15. Worst Case IBS measured at 5 kHz, 50 kHz, 200 kHz, 300 kHz, 400 kHz, 960 kHz, 10 MHz offsets, f_{PFD} = 245.76 MHz

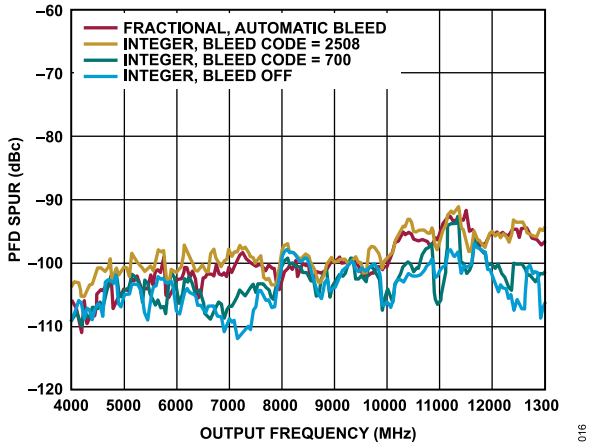

Figure 16. PFD Spurs vs. Output Frequency

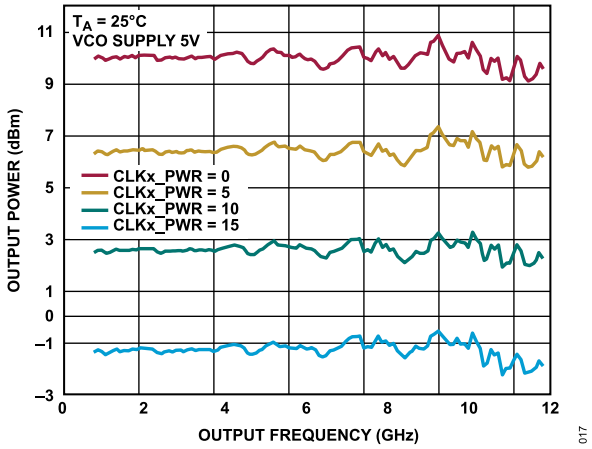

Figure 17. De-Embedded Single-Ended Output Power at Various Output Power Settings

TYPICAL PERFORMANCE CHARACTERISTICS

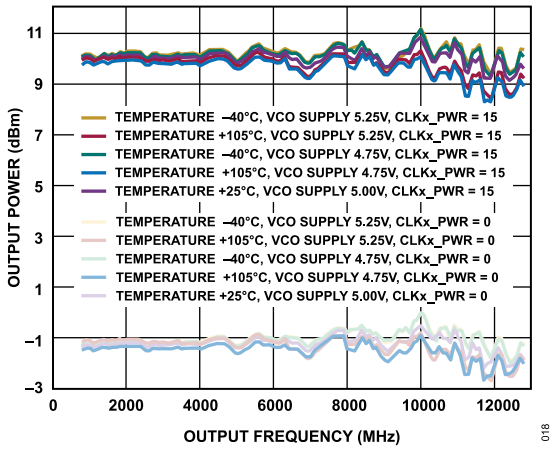

Figure 18. De-Embedded Single-Ended Output Power vs. Output Frequency over Temperature and Supply

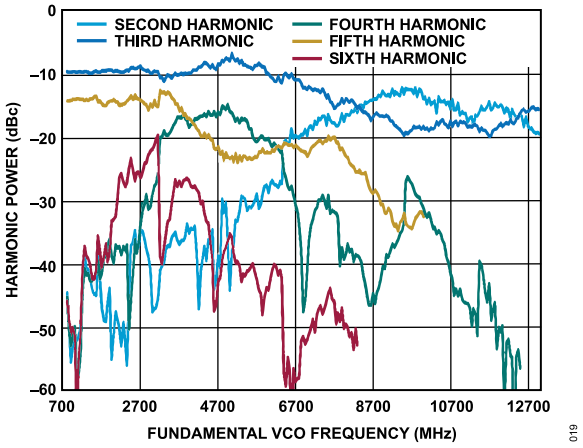

Figure 19. Output Harmonics vs. VCO Frequency

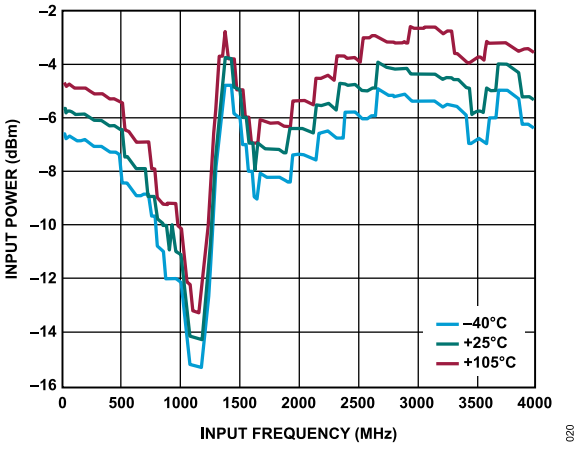

Figure 20. Minimum Input Signal for REF_OK = 1 for DMA Buffer

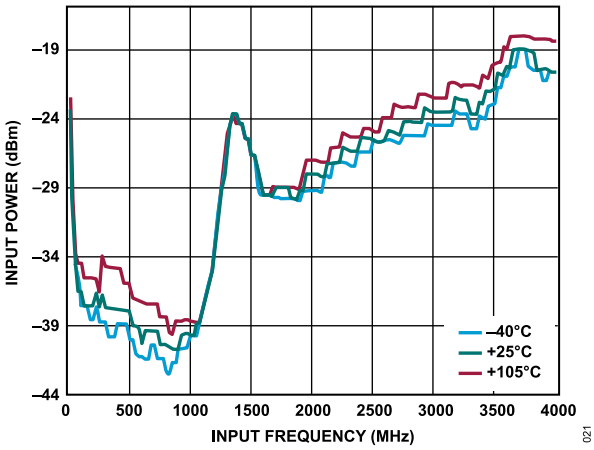

Figure 21. LNA Reference Input Sensitivity vs. Temperature

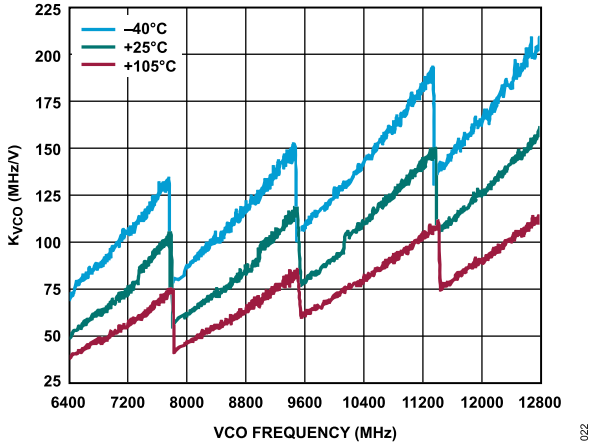

Figure 22. K_{VCO} vs. VCO Frequency at Various Temperatures

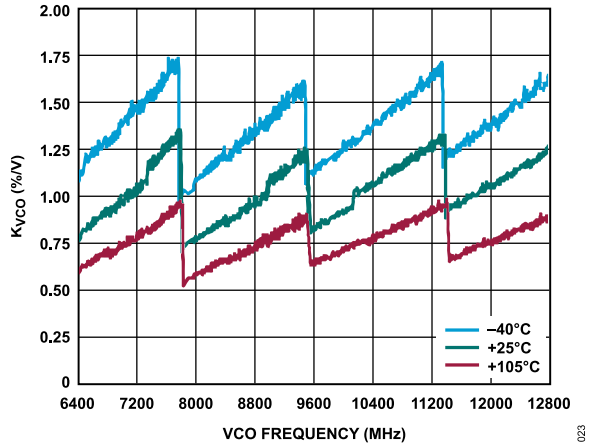

Figure 23. K_{VCO} Sensitivity Percentage vs. VCO Frequency at Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

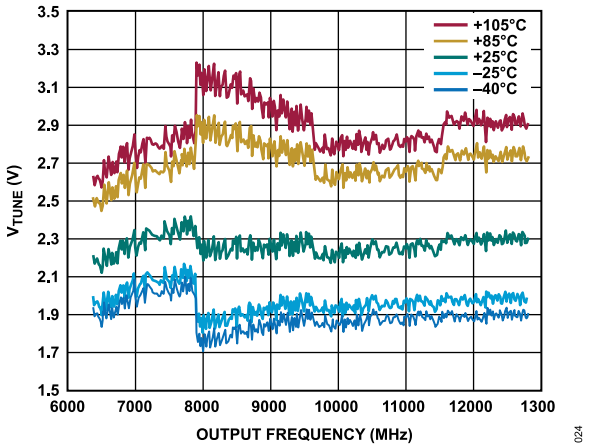

Figure 24. V_{TUNE} vs. Output Frequency when Part Locked at 25°C

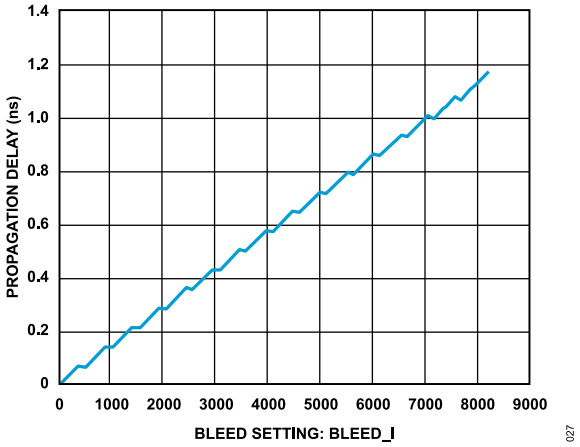

Figure 27. Propagation Delay vs. Bleed Setting

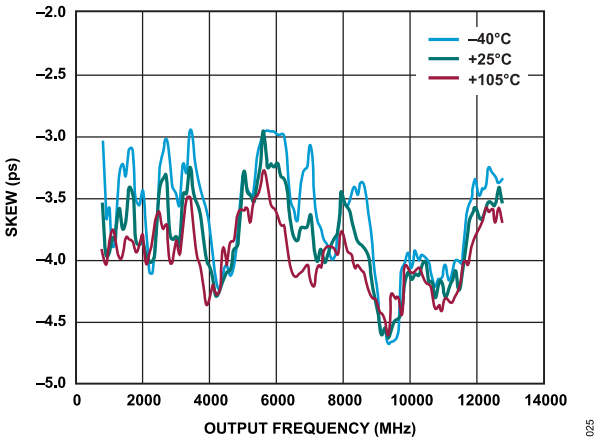

Figure 25. Skew Between Outputs

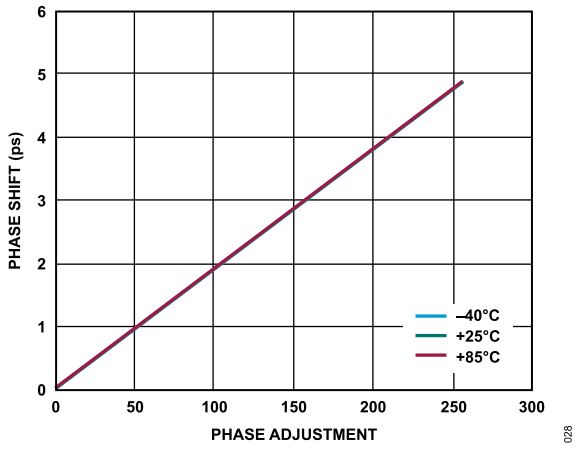

Figure 28. Phase Shift vs. Phase Adjustment, RF_{Out} = 12,775 MHz at Various Temperatures

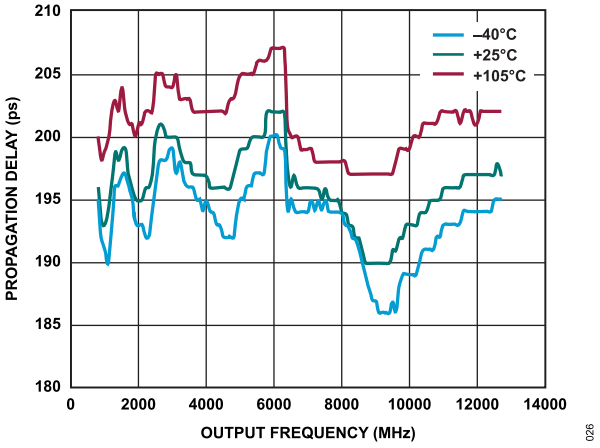

Figure 26. Propagation Delay

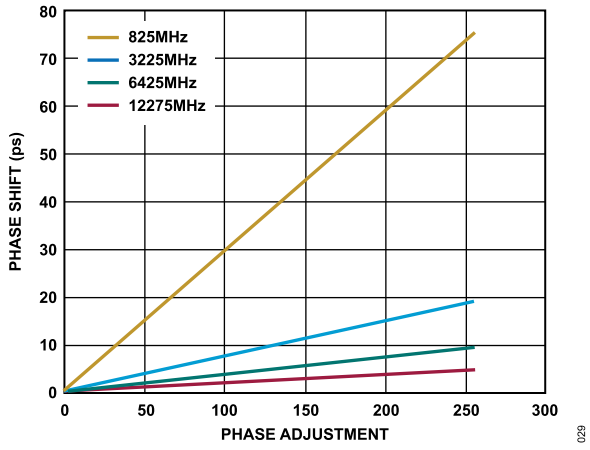

Figure 29. Phase Shift vs. Phase Adjustment at Various Frequencies

TYPICAL PERFORMANCE CHARACTERISTICS

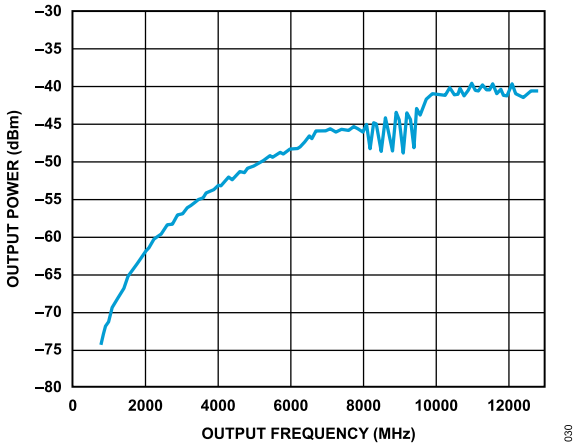

Figure 30. Output Power When Buffer Is Powered Down (PD_CLKOUTx = 1)

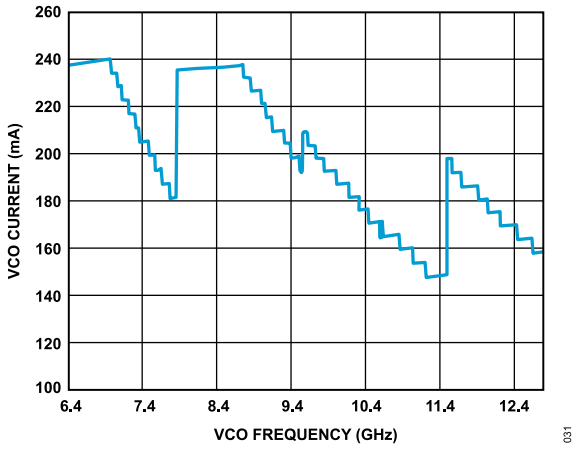

Figure 31. VCO Current vs. VCO Frequency

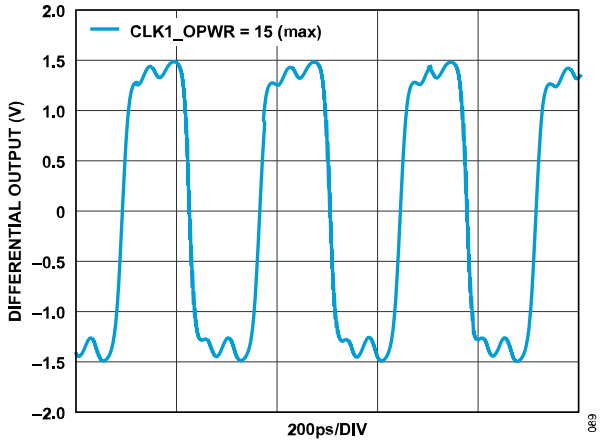

Figure 32. Differential Output at 3 GHz

THEORY OF OPERATION

INTRODUCTION

A PLL is a complex feedback system that may conceptually be considered a frequency multiplier. The system multiplies the frequency input at REFP and REFN and outputs a higher frequency at RFOUT1P, RFOUT2P, RFOUT1N, and RFOUT2N. The PFD, charge pump, output divider, feedback divider, VCO, and external loop filter forms a feedback loop to accurately control the output frequency (see Figure 33). The reference divider or reference doubler is used to set the frequency resolution.

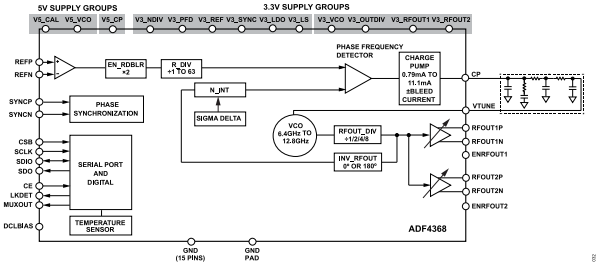

Figure 33. PLL Loop Diagram

OUTPUT FREQUENCY

When the loop is locked, the f_{VCO} (in Hz) produced at the output of the VCO is determined by the reference frequency (f_{REF}) and the O, R, and N values given by the following equation.

$$f_{VCO} = f_{REF} \times \frac{D \times N \times O}{R} \quad (1)$$

Where N is given by:

$$N = N_{INT} + \frac{FRAC1WORD + \frac{FRAC2WORD}{MOD2WORD}}{MOD1WORD} \quad (2)$$

Here, the PFD frequency (f_{PFD}) produced is given by:

$$f_{PFD} = \frac{f_{REF} \times D}{R} \quad (3)$$

f_{VCO} may be alternatively expressed as:

$$f_{VCO} = f_{PFD} \times N \times O \quad (4)$$

The output frequency, f_{RFOUT}, produced at the output of the output divider is given by:

$$f_{RFOUT} = \frac{f_{VCO}}{O} \quad (5)$$

CIRCUIT DESCRIPTION

Reference Input Buffer

The reference frequency of the PLL is applied differentially on the REFP and REFN pin. These high impedance inputs are self-biased and must be AC-coupled with 1 µF capacitors (for a simplified schematic, see Figure 34). Alternatively, the inputs may be used as single-ended by applying the reference frequency at REFP and bypassing REFN to GND with a 1 µF capacitor.

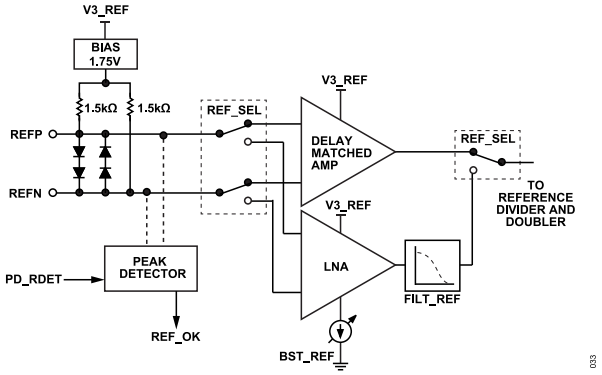

Figure 34. Reference Input Stage

A high quality signal must be applied to the REFP and REFN inputs because they provide the frequency reference to the entire PLL. To achieve the in-band phase noise performance of the device, apply a continuous wave signal or a square wave with a slew rate of at least 1000 V/µs. For more information on reference input signal requirements and interfacing, see the Applications Information section.

When the REF_SEL bit is set to 0, the DMA buffer is selected. The DMA is optimized for high slew rate signals, such as square waves or higher frequency and higher amplitude sine waves. The DMA has a controlled propagation delay from the reference input to clock output, which eases time zero and over temperature multichip clock alignment.

When the REF_SEL bit is set to 1, the LNA is selected. The LNA is optimized for low slew rate signals, such as lower frequency or lower amplitude sine waves.

The REF_SEL bit must be set correctly to optimize the in-band phase noise performance and propagation delay. For recommended settings, see Table 7.

Table 7. REF_SEL Programming

REF_SEL	Sine Wave Slew Rate (V/µs)	Square Wave	Optimized t_{PD}
0	≥1000	Preferred	Yes
1	<1000	Not applicable	Not applicable

To calculate the slew rate of sine wave:

$$Slew\ Rate = 2 \times \pi \times f \times V \quad (6)$$

Where:

f = sine wave frequency

V = sine wave amplitude (in V_{PK})

The FILT_REF bit controls the low-pass filter of the reference input LNA and must be set for sine wave signals based on f_{REF} to limit the wideband noise of the reference. The FILT_REF bit must be set correctly to reach the L_{NORM} normalized in-band phase noise floor. For recommended settings, see Table 8. Square wave inputs have FILT_REF set to 0.

THEORY OF OPERATION

Table 8. FILT_REF Programming

FILT_REF	Sine Wave f_{REF}	Square Wave f_{REF}
0	≥ 20 MHz	All f_{REF}
1	< 20 MHz	Not applicable

The BST_REF bit must be set based on the input signal level to prevent the LNA reference input buffer from saturating. The BST_REF programming is the same whether the input is a sine wave or a square wave. For recommended settings, see Table 9 and for programming examples, see the Applications Information section.

Table 9. BST_REF Programming

BST_REF	Sine Wave f_{REF}
0	≥ 1.6 V_{PP}
1	< 1.6 V_{PP}

Reference Peak Detector

A reference input peak detection circuit is provided on the REFP and REFN inputs to detect the presence of a reference signal and provides the REF_OK status flag available through serial port register REG0058. The circuit has hysteresis to prevent the REF_OK flag from chattering at the detection threshold.

The peak detector approximates an RMS detector. Therefore, sine and square wave inputs give different detection thresholds by a factor of 4/π. For REF_OK detection values, see Table 10.

Table 10. REF_OK Status Output vs. REF INPUT

REF_OK	Sine Wave f_{REF}	Square Wave f_{REF}
1	≥ 200 mV_{PP}	≥ 155 mV_{PP}
0	< 180 mV_{PP}	< 140 mV_{PP}

Reference Divider (R) and Doubler (D)

When the EN_RDBLR bit is set to 1, a frequency multiplier is used to double the frequency driven to the reference divider. A 6-bit divider, R_DIV, in series with the reference doubler is used to reduce the frequency seen at the PFD. The reference divide ratio, R, may be set to any integer from 1 to 63. Use the R_DIV bits found in REG0020 to directly program the R divide ratio. For the relationship between R, D, and the f_{REF}, f_{PFD}, f_{VCO}, and f_{OUT} frequencies, see the Output Frequency section.

Phase/Frequency Detector (PFD)

The phase/frequency detector (PFD), with the charge pump, produces source and sink current pulses proportional to the phase difference between the outputs of the reference divider or reference doubler and the feedback divider. This action provides the necessary feedback to phase lock the loop, forcing a phase alignment at the inputs of the PFD. For a simplified schematic of the PFD, see Figure 35.

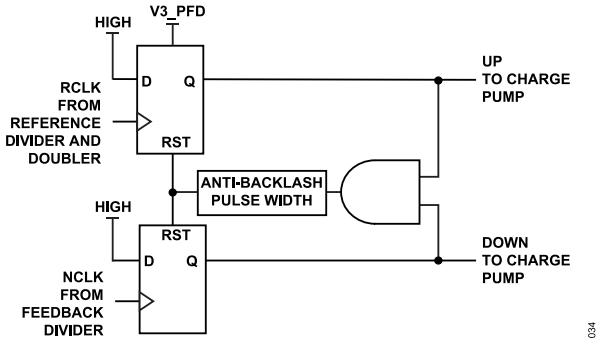

Figure 35. Simplified PFD Schematic

Charge Pump

The charge pump, controlled by the PFD, forces sink (down) or source (up) current pulses onto the CP pin, which must be connected to an appropriate loop filter. For a simplified schematic of the charge pump, see Figure 36.

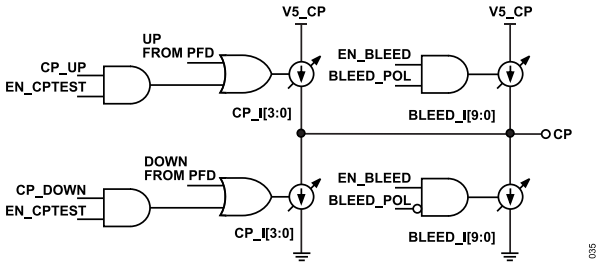

Figure 36. Simplified Charge Pump Schematic

The output current magnitude (I_{CP}) may be set from 0.79 mA to 11.1 mA using the CP_I bits found in REG001F. A larger I_{CP} can result in lower in-band noise due to the lower impedance of the loop filter components, and a smaller I_{CP} can result in better spurious performance. For programming specifics, see Table 11, and for information on designing a loop filter, see the Applications Information section.

Table 11. CP Programming

CP_I	I_{CP}
0	0.79 mA
1	0.99 mA
2	1.19 mA
3	1.38 mA
4	1.59 mA
5	1.98 mA
6	2.39 mA
7	2.79 mA
8	3.18 mA
9	3.97 mA
10	4.77 mA
11	5.57 mA
12	6.33 mA

THEORY OF OPERATION

Table 11. CP Programming (Continued)

CP_I	I_{CP}
13	7.91 mA
14	9.51 mA
15	11.1 mA

Charge Pump Functions

When the EN_CPTEST bit is set to 1, the CP_UP bit and CP_DOWN bit can be programmed to force a constant I_{CP} source or sink current, respectively, on the CP pin. EN_CPTEST or CP_UP and CP_DOWN must be set to 0 to allow the loop to lock. These bits are commonly used as an aid to debug PLL related issues during the hardware and software development phase of a project. For normal operation, set EN_CPTEST, CP_UP, and CP_DOWN to 0.

Charge Pump Bleed Current Optimization

A small programmable constant charge pump current, known as bleed current (I_{BLEED}), can be used to optimize the phase noise and fractional spurious signals in fractional mode. To enable the bleed current, set the EN_BLEED bit to 1. When the BLEED_POL bit is set to 1, a small constant source current is forced onto the CP pin. When the BLEED_POL bit is set to 0, a small constant sink current is forced from the CP pin.

The 13-bits bleed current setting consists of 4-bit MSB for coarse setting and 9-bit LSB for fine setting. The coarse step is 180 µA and the fine setting step is 490 nA.

The optimized bleed current value for fractional mode is calculated based on the charge pump current (I_{CP}), f_{PFD}, and bleed delay (t_{BLEED}). The recommended t_{BLEED} and BLEED_POL are shown in Table 12 and Table 13.

Table 12. t_{BLEED} and BLEED_POL for f_{PFD} ≥ 120 MHz

Output Frequency	t_{BLEED}	BLEED_POL
f_{RFOUT} ≥ 4.2 GHz	390 ps	0
3.0 GHz ≤ f_{RFOUT} < 4.2 GHz	900 ps	0
1.8 GHz ≤ f_{RFOUT} < 3.0 GHz	1200 ps	0
f_{RFOUT} < 1.8 GHz	1400 ps	0

The bleed current and BLEED_I bit are calculated by the following equations:

$$I_{BLEED} = T_{BLEED} \times f_{PFD} \times I_{CP} \quad (7)$$

$$CoarseBleed = INT\left(\frac{I_{BLEED}}{180\mu}\right) \quad (8)$$

$$FineBleed = Round\left(512 \times \frac{I_{BLEED} - 180\mu \times CoarseBleed}{250\mu}\right) \quad (9)$$

$$BLEED\_I = 512 \times CoarseBleed + FineBleed \quad (10)$$

Table 13. t_{BLEED} and BLEED_POL for f_{PFD} <120 MHz

	N ≥ 35		N < 35	
RF Frequency	t_{BLEED}	BLEED_POL	t_{BLEED}	BLEED_POL
f_{RFOUT} ≥ 4.2 GHz	390 ps	0	390 ps	0
3.0 GHz ≤ f_{RFOUT} < 4.2 GHz	1200 ps	1	900 ps	0
1.8 GHz ≤ f_{RFOUT} < 3.0 GHz	1200 ps	0	1200 ps	1
1.2 GHz ≤ f_{RFOUT} < 1.8 GHz	1400 ps	0	1400 ps	1
f_{RFOUT} < 1.2 GHz	1400 ps	0	2000 ps	1

Bleed current also changes the propagation delay from the REFP and REFN input pins to the RFOUTxP and RFOUTxN output pins. In integer mode, bleed current can be used to shift the output in both directions. If BLEED_POL = 0, the propagation delay from the REFP and REFN input pins to the RFOUTxP and RFOUTxN output pins increases.

In fractional mode, after setting the bleed current for the best performance, the output can be shifted by using the PHASE_ADJUSTMENT bits in REG0024, which are effectively used in sigma-delta modulator (SDM). Phase adjustment does not cause any phase noise degradation.

Lock Detector

The lock detector uses internal signals from the PFD to measure phase coincidence between RCLK and NCLK. It is enabled by setting both the EN_LOL bit and EN_LDWIN bit to 1 in REG002D and presents the lock detector output on the LKDET pin and the LOCKED bit in REG0058. The lock detector output can also be presented on the MUXOUT pin by programming the MUXOUT bits in REG002E.

The PFD phase difference must be less than the phase difference lock window time (t_{LDWIN}) for a set number of PFD cycles before the lock detector output indicates that the PLL has locked. The user sets the t_{LDWIN} for a valid lock condition with the LDWIN_PW bits depending on the operation mode, f_{PFD}, and f_{RFOUT}. The recommended settings for the LDWIN_PW bits are given in Table 14.

Table 14. LDWIN_PW Programming

LDWIN_PW	Configuration
0	Integer PLL, t_{BLEED} ≤ 85 ps
1	Integer PLL, 85 ps > t_{BLEED} < 250 ps
10	Fractional PLL, f_{PFD} > 200 MHz and RF > 6.4 GHz
11	Fractional PLL, f_{PFD} > 200 MHz and RF > 5 GHz
100	Fractional PLL, f_{PFD} < 200 MHz
101	Fractional PLL, f_{PFD} < 100 MHz
110	Fractional PLL, f_{PFD} < 50 MHz
111	Fractional PLL, f_{PFD} < 40 MHz

THEORY OF OPERATION

The desired number of PFD cycles varies if a designer prioritizes lock detect accuracy or speed. Five loop filter time constants can be used as an initial estimate of the desired number of PFD cycles, as shown in Equation 11. The desired number of PFD cycles is set by the LD_COUNT bits in REG002C as with and the formula shown in the Register Details section. The user sets the LD_COUNT such that actual PFDcycles is greater than desired PFD cycles. For more details, see Figure 37 and Table 16.

$$Desired\ PFD\ Cycles = \frac{5}{2 \times \pi \times LPBW} \quad (11)$$

Where LPBW is loop filter bandwidth.

Table 15. LD_COUNT Programming

LD_COUNT	Actual PFD Cycles
0	27
1	35
2	51
3	67
4	99
5	131
6	195
7	259
8	387
9	515
10	771
11	1027
12	1539
13	2051
14	3075
15	4099
16	6147
17	8195
18	12291
19	16387
20	24579
21	32771
22	49155
23	65539
24	98307
25	131075
26	196611
27	262147
28	393219
29	524291
30	786435
31	1048579

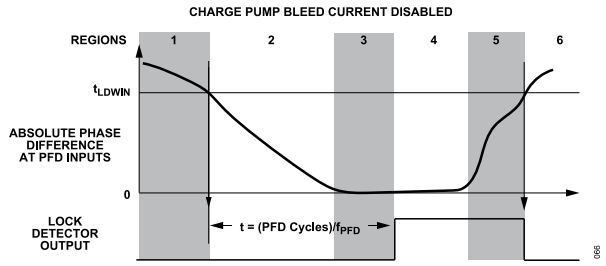

Figure 37. Lock Detector Timing, Bleed Current Disabled

Table 16. Lock Detector Timing, Bleed Current Disabled

Region	Absolute Phase Difference at PFD	Lock Detector State
1	> t_{LDWIN}	Low
2	< t_{LDWIN}	Low, counts PFD cycles
3	~0	
4	~0	High, > desired PFD cycle count
5	< t_{LDWIN}	High
6	> t_{LDWIN}	Low (immediately)

When the charge pump bleed current is enabled, a phase offset is applied to the PFD inputs. This phase offset (t_{IDEL}) is proportional to the amount of bleed current. Region 3 and Region 4 in Figure 37 and Figure 38 highlight the PFD phase difference that the PLL settles to when the charge pump bleed current is disabled or enabled, respectively.

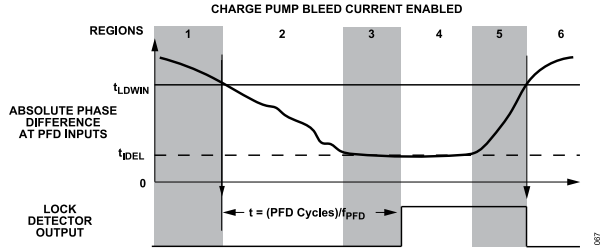

Figure 38. Lock Detector Timing, Bleed Current Enabled

VCO

The VCO core consists of four separate VCOs, each of which uses 256 overlapping bands, which allows the device to cover a wide frequency range without large VCO sensitivity (K_V). The output frequency can be further extended by using the output divider.

THEORY OF OPERATION

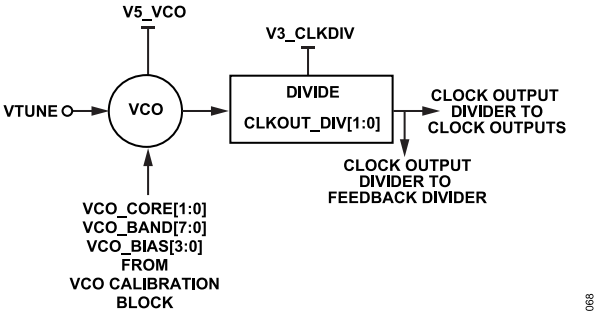

Figure 39. VCO and Clock Output Divider

The correct register values for the VCO_CORE, VCO_BAND, and VCO_BIAS settings are determined by performing a VCO calibration. After a VCO calibration is performed for a specific device and frequency, the VCO_CORE, VCO_BAND, and VCO_BIAS values can be recorded. These recorded values may be programmed manually on subsequent power ups when the same device and frequency are used, thereby avoiding the VCO calibration time.

VCO Calibration

A VCO calibration is required to select the correct VCO core, band, and bias settings for a specific VCO frequency. This procedure assumes that the device is powered up, the desired reference frequency is present on the REFP and REFN pins, and all other registers are programmed correctly. Figure 40 and Figure 41 show the visual aids for this procedure.

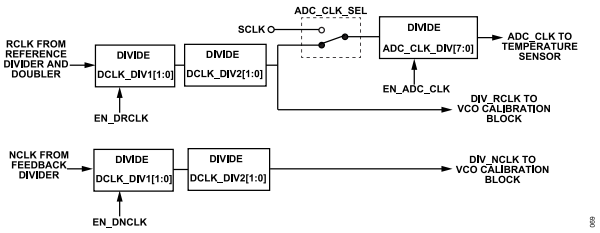

Figure 40. VCO Calibration Dividers

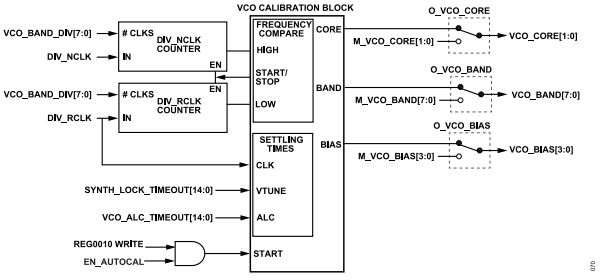

Figure 41. VCO Calibration Block

To perform a VCO calibration, set up several registers as outlined in the following procedure:

1. Set DCLK_DIV1, , and DCLK_MODE to the values in Table 17. Record f_{DIV_RCLK} for later use.
2. Calculate and set the minimum values for the SYNTH_LOCK_TIMEOUT bit fields, Bits[14:0], the VCO_ALC_TIMEOUT bit fields, Bits[14:0], and VCO_BAND_DIV bits. Typical automatic VCO calibration times are 3 ms to 9 ms when minimum values are chosen for these parameters. Larger values produce longer VCO calibration times.

$$SYNTH\_LOCK\_TIMEOUT \geq Ceiling\left(200\mu s \times f_{DIV\_RCLK}\right) \quad (12)$$

$$VCO\_ALC\_TIMEOUT \geq Ceiling\left(50\mu s \times f_{DIV\_RCLK}\right) \quad (13)$$

$$VCO\_BAND\_DIV \geq Ceiling\left(\frac{15\mu s \times f_{DIV\_RCLK}}{16 \times 2^{DCLK\_MODE}}\right) \quad (14)$$

3. Ensure that the ADC_CLK_DIV bits are set so that the desired ADC clock frequency is <400 kHz:

$$ADC\_CLK\_DIV > Ceiling\left(\frac{\left(\frac{f_{DIV\_RCLK}}{400kHz} - 2\right)}{4}\right) \quad (15)$$

4. Set the N_INT, CLKOUT_DIV bits, R_DIV bits, and the EN_RDBLR bit by programming REG0010 last. Any write to REG0010 starts the VCO autocalibration.
5. Monitor the ADC_BUSY bit and FSM_BUSY bit. The calibration is finished when ADC_BUSY transitions from high to low, followed with FSM_BUSY transitioning from high to low.
6. After the VCO calibration is complete, disable the calibration clocks to limit unwanted spurious content by setting EN_DRCLK = EN_DNCLK = EN_ADC_CLK = 0.
7. This is an optional step. Read back and record the VCO_CORE bits, VCO_BAND bits, and VCO_BIAS bits. These values can be used to bypass calibration and manually program the M_VCO_CORE bits, M_VCO_BAND bits, and M_VCO_BIAS bits for a given device and frequency.

Table 17. DCLK_DIV1 and DCLK_MODE Setup

f_{PFD} (MHz)	DCLK_DIV1	DCLK_MODE	f_{DIV_RCLK} (MHz)
≤160	0	1	$f_{PFD}/2$
>160 and ≤320	1	1	$f_{PFD}/4$
>320	2	1	$f_{PFD}/8$

Clock Output Divider

A 2-bit divider, CLKOUT_DIV, is used to reduce the frequency seen at the output buffer and feedback divider. Its divide ratio, O, may be set to 1, 2, 4, or 8. Use the CLKOUT_DIV bits found in REG0011 to directly program the O divide ratio. CLKOUT_DIV is located inside the PLL loop. Therefore, any change to CLKOUT_DIV results in the PLL losing lock for few loop time constants.

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Output Invert (INV_CLKOUT)

The output invert (INV_CLKOUT) is used to shift the output signal 180°. INV_CLKOUT is located inside the PLL loop. Any change to INV_CLKOUT results in the PLL losing lock for few loop time constants. Use the INV_CLKOUT bit found in register REG0011 to directly program the output phase.

Feedback Divider (N)

The feedback divider allows a division ratio in the PLL feedback path. Determine the division ratio by the N_INT bit fields, Bits[11:0] (REG0011 and REG0010), the FRAC1WORD bit fields, Bits[24:0] (REG0015, REG0014, REG0013, and REG0012), the FRAC2WORD bit fields, Bits[23:0] (REG0019, REG0018, and REG0017), and the MOD2WORD bit fields, Bits[23:0] (REG001C, REG001B, and REG001A) values that this divider comprises together with the fixed modulus MOD1WORD, which is equal to 2^{25}. The 24-bit variable MOD2WORD and the 25-bit fixed MOD1WORD forms a 49-bit combined fractional modulus. For the relationship between the N_INT bit fields, Bits[11:0], the FRAC1WORD bit fields, Bits[24:0], MOD1WORD, the FRAC2WORD bit fields, Bits[23:0], the MOD2WORD bit fields, Bits[23:0], and the CLKOUT_DIV bits, together with R, D, and the f_{REF}, f_{PFD}, f_{VCO}, and f_{OUT} frequencies, see the Output Frequency section.

RF Output Buffer

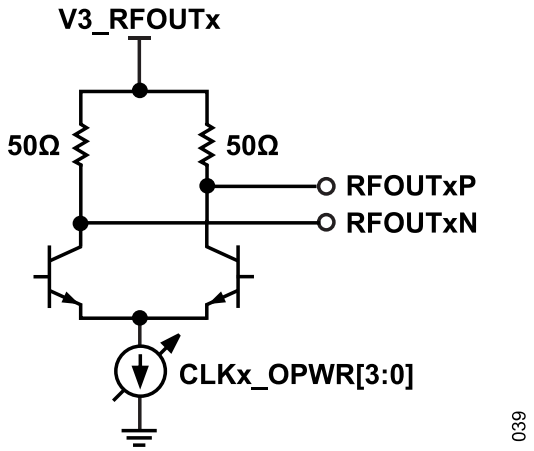

Figure 42. Simplified RF Output Buffer Schematic

The low noise, differential output buffer in Figure 42 a differential output voltage. The output amplitude level and common mode voltage are settable with the CLK1_OPWR bits and the CLK2_OPWR bits. Each output can be either AC-coupled or DC-coupled and terminated with 100 Ω differentially. If a single-ended output is desired, each side of the output must be individually AC-coupled and terminated with 50 Ω.

The lowest four CLKx_OPWR settings can be used without any external pull-up inductor. External inductors are required to achieve the higher output power. A 3.4 nH 0302 package or smaller inductor is recommended. For more details on the evaluation board schematic, refer to the EVAL-ADF4368 user guide.

APPLICATIONS INFORMATION

LOOP FILTER DESIGN

A stable loop filter design requires care in selecting the loop filter components of the ADF4368. It is recommended to download and install ADIsimPLL™ for loop filter design and simulation. ADIsimPLL™ has an integrated tutorial for first time users and a help manual for more complex topics. There are also several ADIsimPLL training videos available on www.analog.com. After a loop filter is designed and simulated, it is recommended to verify the new loop filter using the ADF4368 evaluation hardware.

A full loop filter design tutorial is beyond the scope of this data sheet. However, some best practices are shown in the following lists. ADIsimPLL aids in defining and simulating these parameters. Any significant change to these items requires a new loop filter design.

A stable loop filter must meet the following criteria:

- Loop filter phase margin > 45°
- Loop filter bandwidth < f_{PFD} ÷ 10

The desired loop filter bandwidth is determined by the following features of the ADF4368:

- I_{CP}
- K_{VCO}
- PFD frequency
- Reference input phase noise (see the Reference Phase Noise section)
- Trade-off between minimizing jitter or settling time (see the Output Phase Noise Characteristics section and Equation 12, respectively)

The VTUNE pin has an internal 30 pf capacitor to GND that must be included in the loop filter design. ADIsimPLL™ takes this internal capacitance into account automatically.

REFERENCE SOURCE CONSIDERATIONS

Reference Input Network

The reference input buffer of the ADF4368, shown in Figure 34, provides a flexible interface to either differential or single-ended frequency sources. Figure 43 to Figure 48 show recommended interfaces for different reference signal types. All Z_0 signal traces are 50 Ω transmission lines in Figure 43, Figure 44, Figure 45, Figure 46, Figure 47, and Figure 48.

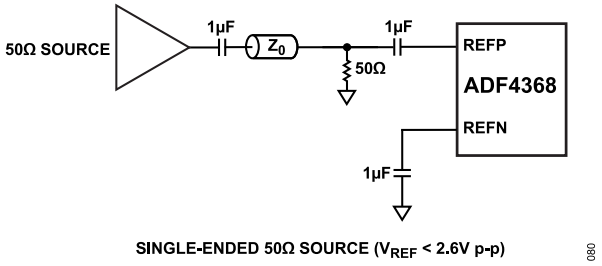

Figure 43. Single-Ended 50 Ω Source (V_{REF} < 2.6 V p-p)

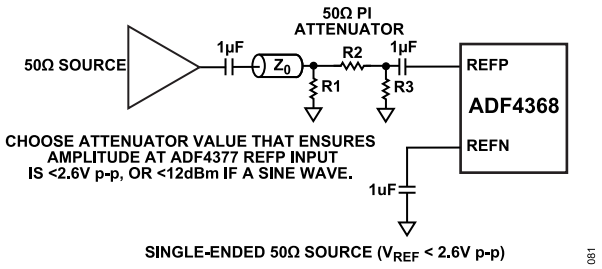

Figure 44. Single-Ended 50 Ω Source (V_{REF} > 2.6 V p-p)

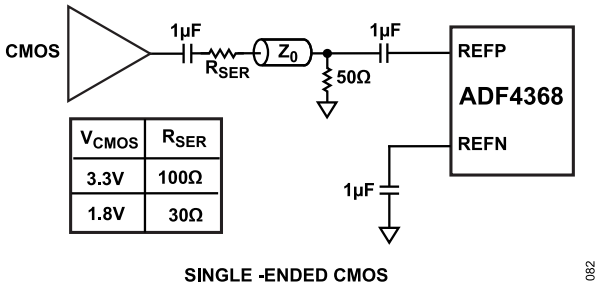

Figure 45. Single-Ended CMOS

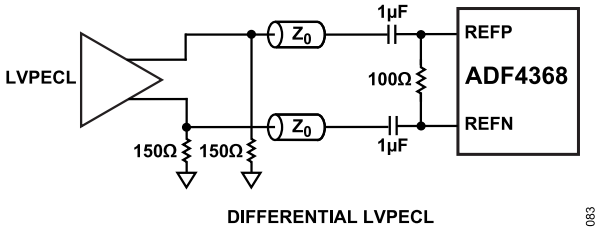

Figure 46. Differential LVPECL

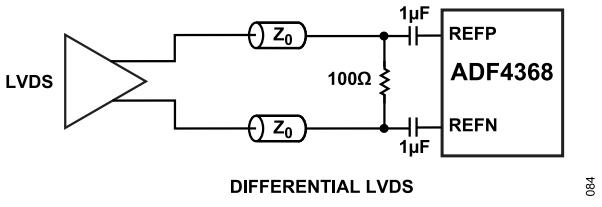

Figure 47. Differential LVDS

APPLICATIONS INFORMATION

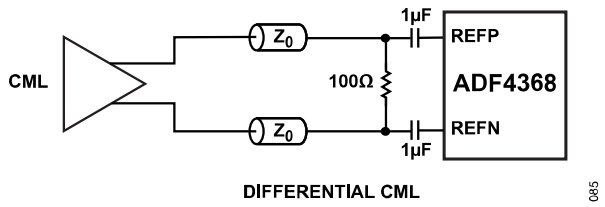

Figure 48. Differential CML

Reference Phase Noise

The ADF4368 achieves an in-band normalized phase noise floor of L_{NORM} = −239 dBc/Hz in integer mode and L_{NORM} = −237 dBc/Hz typical in fractional mode. To calculate the equivalent input phase noise floor (L_{IN}), use the following Equation 16.

$$L_{IN} = L_{NORM} + 10 \times \log_{10}(f_{REF}) \quad (16)$$

For example, a 100 MHz reference input frequency gives an L_{IN} of −157 dBc/Hz in fractional mode. The phase noise of the reference frequency source must be at least 6 dB less than L_{IN} to avoid impacting and increasing the overall system phase noise.

To maintain typical L_{NORM} performance, Table 7 provides criteria for selecting the optimal REF_SEL setting based on the input reference signal type and amplitude.

OUTPUT PHASE NOISE CHARACTERISTICS

In-Band Output Phase Noise

The in-band phase noise floor (L_{OUT}) produced at f_{OUT} can be calculated by Equation 17 and Equation 18.

$$L_{OUT} = L_{NORM} + 10 \times \log_{10}(f_{PFD}) + 20 \times \log_{10}\left(\frac{f_{OUT}}{f_{PFD}}\right) \quad (17)$$

Or

$$L_{OUT} = L_{NORM} + 10 \times \log_{10}(f_{PFD}) + 20 \times \log_{10}\left(\frac{N}{O}\right) \quad (18)$$

Output Phase Noise Due to 1/f Noise

In-band phase noise at very low offset frequencies can be influenced by the 1/f noise of the ADF4368, depending on the f_{PFD}. Use the normalized in-band 1/f noise ($L_{1/f}$) of −287 dBc/Hz with Equation 19 to approximate the output 1/f phase noise at a given frequency offset (f_{OFFSET}).

$$L_{OUT(1/f)} = L_{1/f} + 20 \times \log_{10}(f_{OUT}) - 10 \times \log_{10}(f_{OFFSET}) \quad (19)$$

Unlike the in-band noise floor (L_{OUT}), the 1/f noise ($L_{OUT(1/f)}$) does not change with f_{PFD} and is not constant over offset frequency. For an example of in-band phase noise for f_{PFD} equal to 100 MHz and 500 MHz for integer mode, see Figure 49. The total phase noise is the summation of L_{OUT} and $L_{OUT(1/f)}$, calculated by Equation 20.

$$L_{OUT(TOTAL)} = 10 \times \log_{10}\left(10^{L_{OUT}/10} + 10^{L_{OUT}(1/f)/10}\right) \quad (20)$$

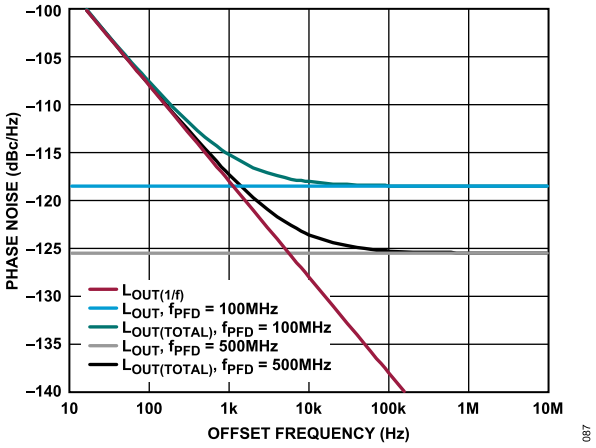

Figure 49. Theoretical In-Band Phase Noise, f_{OUT} = 10 GHz

POWER-UP AND INITIALIZATION SEQUENCE

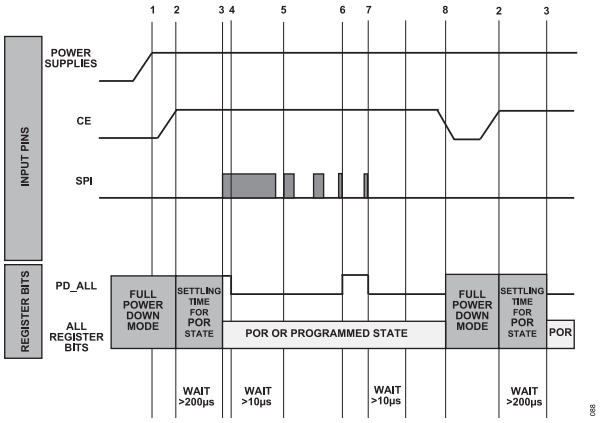

Figure 50. Power-Up and Initialization Sequence

The following steps describe the recommended power-up and initialization sequence of the ADF4368:

1. Apply specified voltages to the 5V, 3.3V_1, and 3.3V_2 power supply groups. The ADF4368 is in full power-down mode at this point and SPI programming is not possible.
2. Set the CE pin to a logic high. It is acceptable to connect the CE pin to the V3_LDO pin via a pull-up resistor. Therefore, Step 1 and Step 2 are performed coincidentally.
3. After waiting ≥200 µs for all SPI register bits to settle to their power-on reset state (POR), begin programming the SPI to configure the ADF4368 to a desired state. The following is the recommended SPI programming sequence:

APPLICATIONS INFORMATION

   a. Set the SDO_ACTIVE and CMOS_OV bits to a desired state for future readback operations.
   b. Program all register addresses in descending order, REG0053 to REG0010. There are several required reserved register field settings provided in Table 19 that are required for proper device operation.
4. The ADF4368 remains in power-down mode until the PD_ALL bit is programmed to 0. After PD_ALL is disabled, wait at least 10 µs for the VCO calibration circuitry and other circuit blocks to settle before starting a VCO calibration.
5. A write to REG0010 starts a VCO autocalibration. At this point, the device is fully operational and new frequencies can be programmed as often as desired. The following steps are information for PD_ALL and CE pin.
6. Setting PD_ALL to 1 power down the ADF4368, retaining the latest programmed SPI settings and full SPI programming capability.
7. If only the state of PD_ALL was modified in Step 6, setting PD_ALL to 0 returns the ADF4368 to the frequency programmed in Step 5. After a 10 µs wait, all circuit blocks are completely powered up internally. This 10 µs wait does not include the frequency settling time associated with the loop filter bandwidth.
8. Toggling the CE pin level causes the ADF4368 to return to full power-down mode and return the SPI registers to the POR state (see Step 2 and Step 3).

Programming Procedure

There are two different methods to power up the ADF4368. The most commonly used method provided in the Standard Power-Up and Initialization Sequence, Automatic VCO Calibration section is mandatory on the initial device power-up.

The method provided in the Fast Power-Up and Initialization, Manually Programmed VCO Calibration Settings (Optional) section is an optional power-up procedure after the initial power-up.

Standard Power-Up and Initialization Sequence, Automatic VCO Calibration

The following standard power-up and initialization sequence is the recommended procedure to power up and program the ADF4368:

1. Follow Step 1 through Step 5 in the Power-Up and Initialization Sequence section.
2. It is optional to monitor the status of the VCO calibration bits, ADC_BUSY and FSM_BUSY. A VCO calibration is completed when ADC_BUSY transitions from high to low, followed by FSM_BUSY transitioning from high to low. Typical automatic VCO calibration times range from 3 ms to 9 ms.
3. After the VCO calibration is complete, disable the VCO calibration clocks by setting EN_DRCLK = EN_DNCLK = EN_ADC_CLK = 0. Disabling the VCO calibration clocks reduces unwanted spurious content.
4. The PLL is locked when the lock detector sets the LKDET pin and the LOCKED bit high.
5. When changing the frequency, do the following steps:
   a. Program only the modified registers in the descending order.
   b. Write REG0010 to start a new VCO autocalibration as the final step whether it is modified or not.

Fast Power-Up and Initialization, Manually Programmed VCO Calibration Settings (Optional)

The purpose of the fast power-up and initialization method is to avoid the automatic VCO calibration time, which is typically 3 ms to 9 ms. For fixed clock frequency converter applications, automatic VCO calibration times are typically acceptable. For fast frequency hopping applications, much shorter lock time is needed.

The following list provides the steps to record the VCO calibration results on the initial power-up and then to manually program VCO calibration settings on subsequent power ups:

1. On initial power up, follow the procedure in the Standard Power-Up and Initialization Sequence, Automatic VCO Calibration section.
2. Record calibration results from the VCO_CORE, VCO_BAND, and VCO_BIAS bit fields for each target frequency and store the recorded results in memory. Note that each unique device and frequency combination generates different VCO_CORE, VCO_BAND, and VCO_BIAS values.
3. Subsequent power-up and initialization sequences (see the Power-Up and Initialization Sequence section) can bypass the automatic VCO calibration procedure by programming the override (O_VCO_CORE, O_VCO_BAND, and O_VCO_BIAS) and manual (M_VCO_CORE, M_VCO_BAND, and M_VCO_BIAS) VCO bits with the register settings provided in Table 18. All other bit fields are programmed as usual.
4. When changing the frequency, program only the modified registers in descending order.

Table 18. Manually Programmed VCO Calibration Settings

Bit Fields	Value
EN_AUTOCAL	0x0
EN_DRCLK	0x0
EN_DNCLK	0x0
EN_ADC_CLK	0x0
O_VCO_CORE	0x1
O_VCO_BAND	0x1
O_VCO_BIAS	0x1
M_VCO_CORE	Program with recorded values
M_VCO_BAND	Program with recorded values
M_VCO_BIAS	Program with recorded values

APPLICATIONS INFORMATION

Synchronizing Multiple ADF4368 Output Phases

Multiple ADF4368 can be synchronized in two ways, timed sync method through the SYNC pin and EZSync method through SPI programming, which eliminates the need for distributing the SYNC signal to all ADF4368 devices.

The ADF4368 also supports a unique feature called phase resync. After multiple devices are synchronized, any additional resyncing (for example, after a frequency change) is not needed because of the phase resync feature of the device. When the phase resync mode is enabled, the outputs are automatically synchronized when changing frequency (as long as R_DIV bits is unchanged).

The synchronization relies on setting the output phase of the ADF4368 to a known phase relative to its reference input. Therefore, any phase difference in the reference inputs of multiple ADF4368 devices is directly reflected to the output. This residual phase difference can be compensated by using the phase adjust feature.

Timed Synchronization Method

The traditional method by using the SYNC pin. A rising edge on the SYNC pin triggers the synchronization process and puts the device into a reset state. Then, with a falling edge on the SYNC pin, the synchronization process starts. The output phase is aligned to a known phase with respect to the reference input.

This method is straightforward, but requires an additional well aligned synchronization signal.

EZSync Method

The EZSync method is useful when synchronizing a huge number of ADF4368 devices, such as massive multiple-input multiple-output (MIMO) or phase array applications. This method eliminates the need for an additional synchronization signal.

The main concept of the EZSync method is sending a synchronization request through the SPI by writing to the SW_SYNC bit instead of the SYNC pin. The problems with sending the request over the SPI are that the SPI is a very slow protocol and does not have any time accuracy. Sending the request in the same reference period is also another challenge and even impossible for a huge number of ADF4368 devices used.

These problems are solved easily by stopping and starting the reference signals so that they leave enough setup and hold time for sending the request over the SPI. The reference signals must stop and start very accurately and without any glitch or without any runt pulse. The clock generation/distribution devices from Analog Devices, such as the LTC6953 or LTC6954, are recommended when using EZSync.

Phase Resynchronization

In frequency hopping systems, another challenge is resynchronizing the multiple devices after changing frequency. This causes a dead time in operation and also causes process load on the controller.

The following sequence is the procedure for the Phase ReSync method:

1. Power up all ADF4368 devices
2. Program all ADF4368 devices to the same frequency
3. Perform an initial synchronization (timed synchronization or EZSync)
4. Enable phase resynchronization mode and perform the synchronization once more

From this point on, any frequency changes are automatically synchronized. No additional synchronization request is needed. The timing of this SPI command to change frequency is not critical. Therefore, the user can change the frequency of multiple devices at different times.

When Phase ReSync method is enabled, the value of the FRAC2WORD and MOD2WORD should be less than 2^{17} (they should be considered as 17 bit).

Phase Shift

The output phase of the ADF4368 can be shifted by the following two methods:

- Shifting the phase on SDM block
- Bleed current

The first method requires the SDM to be enabled and has a very high accuracy and very fine step size, which makes it very useful when the device is in fractional mode. The amount of phase adjust is set by the PHASE_ADJUSTMENT bits (REG0024) and the output is shifted with this amount every time when PHASE_ADJ (REG001F) is written.

When the ADF4368 is in integer mode, because SDM is disabled, this method does not work. Bleed current can be used to shift in this mode (see the Charge Pump Bleed Current Optimization section). In fractional mode, bleed current is mainly used for phase noise and spur optimization.

It is possible to enable the SDM and shift the output by using the first method. Note that this puts the device into fractional mode although the output is an integer multiple of f_{PFD}.

APPLICATIONS INFORMATION

POWER SUPPLY AND BYPASSING

The ADF4368 is a high performance, low noise device. Phase noise and spurious performance may be degraded by noisy power supplies. To achieve maximum performance and ensure that power supply noise does not degrade the performance of the ADF4368, it is recommended to use the Analog Devices low noise, high power supply rejection ratio (PSRR) regulators. Preferred regulators include the LT3045, ADM7150, and the ADM7151. Additional external supply bypass capacitors are also recommended. For more details, refer to the EVAL-ADF4368 evaluation board design.

REGISTER MAPS

The reset column refers to the initial register state on power up or after the SOFT_RESET bit is toggled. The bit columns provide bit names or the required programmed state of write-able reserved registers for proper device operation. Register bit fields labeled RESERVED are read only.

Table 19. ADF4368 Register Summary

Reg	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	SOFT_RESET_R	LSB_FIRST_R	ADDRESS_ASCENSION_R	SDO_ACTIVE_R	SDO_ACTIVE	ADDRESS_ASCENSION	LSB_FIRST	SOFT_RESET	0x00	R/W
0x01	SINGLE_INSTRUCTION	REG01_RSV6	MAIN_READBACK_CONTROL	REG01_RSV4	RESERVED	REG01_RSV1	REG01_RSV0	RESERVED	0x00	R/W
0x02	RESERVED				CHIP_STATUS				0x00	R
0x03	RESERVED				CHIP_TYPE				0x00	R
0x04	PRODUCT_ID[7:0]								0x00	R
0x05	PRODUCT_ID[15:8]								0x00	R
0x06	PRODUCT_GRADE				DEVICE_REVISION				0x00	R
0x0A	SCRATCHPAD								0x00	R/W
0x0B	SPI_REVISION								0x00	R
0x0C	VENDOR_ID[7:0]								0x56	R
0x0D	VENDOR_ID[15:8]								0x04	R
0x0F	RESERVED							0	0x00	R/W
0x10	N_INT[7:0]								0x80	R/W
0x11	CLKOUT_DIV		INT_MODE	INV_CLKOUT	N_INT[11:8]				0x00	R/W
0x12	FRAC1WORD[7:0]								0x00	R/W
0x13	FRAC1WORD[15:8]								0x00	R/W
0x14	FRAC1WORD[23:16]								0x00	R/W
0x15	M_VCO_CORE		M_VCO_BIAS				CMOS_OV	FRAC1WORD[24]	0x00	R/W
0x16	M_VCO_BAND								0x00	R/W
0x17	FRAC2WORD[7:0]								0x00	R/W
0x18	FRAC2WORD[15:8]								0x00	R/W
0x19	FRAC2WORD[23:16]								0x00	R/W
0x1A	MOD2WORD[7:0]								0x00	R/W
0x1B	MOD2WORD[15:8]								0x00	R/W
0x1C	MOD2WORD[23:16]								0x00	R/W
0x1D	BLEED_I[7:0]								0x00	R/W
0x1E	EN_PHASE_RESYNC	EN_REF_RST	TIMED_SYNC	BLEED_I[12:8]					0x00	R/W
0x1F	SW_SYNC	PHASE_ADJ	BLEED_POL	EN_BLEED	CP_I				0x00	R/W
0x20	EN_AUTOCAL	EN_RDBLR	R_DIV						0x01	R/W
0x21	PHASE_WORD[7:0]								0x00	R/W
0x22	PHASE_WORD[15:8]								0x00	R/W
0x23	PHASE_WORD[23:16]								0x00	R/W
0x24	PHASE_ADJUSTMENT								0x00	R/W
0x25	RESYNC_WAIT[7:0]								0x00	R/W
0x26	RESYNC_WAIT[15:8]								0x00	R/W
0x27	RESYNC_WAIT[23:16]								0x00	R/W
0x28	0	LSB_P1	VAR_MOD_EN	0	0	0	0	0	0x00	R/W
0x29	CLK2_OPWR				CLK1_OPWR				0x00	R/W
0x2A	0	PHASE_ADJ_POL	0	PD_SYNC	0	PD_RDET	0	0	0x04	R/W

REGISTER MAPS

Table 19. ADF4368 Register Summary (Continued)

Reg	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x2B	PD_ALL	0	0	0	PD_LD	0	PD_CLKOUT1	PD_CLKOUT2	0x83	R/W
0x2C	LDWIN_PW				LD_COUNT				0x00	R/W
0x2D	EN_DNCLK	EN_DRCLK	EN_LOL	EN_LDWIN	0	RST_LD	0	1	0x00	R/W
0x2E	MUXOUT				0	EN_CPTEST	CP_DOWN	CP_UP	0x00	R/W
0x2F	BST_REF	FILT_REF	REF_SEL	0	0	1	1	1	0x00	R/W
0x30	MUTE_NCLK	0	DRCLK_DEL			DNCLK_DEL			0x00	R/W
0x31	SYNC_DEL			RST_SYS	EN_ADC_CLK	0	0	1	0x00	R/W
0x32	1	1	0	1	0	0	1	1	0x00	R/W
0x33	0	0	1	1	0	0	1	0	0x00	R/W
0x34	1	0	0	1	1	0	0	0	0x00	R/W
0x35	0	0	0	0	0	DCLK_MODE	0	0	0x00	R/W
0x36	CLKODIV_DB	DCLK_DIV_DB	0	1	0	1	1	0	0x00	R/W
0x37	VCO_BAND_DIV								0x00	R/W
0x38	SYNTH_LOCK_TIMEOUT[7:0]								0x00	R/W
0x39	O_VCO_DB	SYNTH_LOCK_TIMEOUT[14:8]							0x00	R/W
0x3A	VCO_ALC_TIMEOUT[7:0]								0x00	R/W
0x3B	DEL_CTRL_DB	VCO_ALC_TIMEOUT[14:8]							0x00	R/W
0x3C	0	0	0	0	0	0	0	0	0x00	R/W
0x3D	1	1	0	0	0	0	0	0	0x00	R/W
0x3E	ADC_CLK_DIV								0x00	R/W
0x3F	EN_ADC_CNV	0	0	0	0	0	EN_ADC	ADC_A_CONV	0x00	R/W
0x40	0	0	MUTE_CLKOUT2			MUTE_CLKOUT1			0x00	R/W
0x41	0	0	0	0	0	0	0	0	0x00	R/W
0x42	0	0	0	0	1	0	0	1	0x00	R/W
0x43	0	ADC_CLK_SEL	0	0	1	0	0	1	0x00	R/W
0x44	0	0	0	1	1	0	0	0	0x00	R/W
0x45	0	0	0	0	1	0	0	0	0x00	R/W
0x46	0	0	0	0	0	0	0	0	0x00	R/W
0x47	0	0	0	0	0	0	0	0	0x00	R/W
0x48	0	0	0	0	0	0	0	0	0x00	R/W
0x49	0	0	0	0	0	0	0	0	0x00	R
0x4A	0	0	0	0	0	0	0	0	0x00	R/W
0x4B	0	1	0	1	1	1	0	1	0x00	R/W
0x4C	0	0	1	0	1	0	1	1	0x00	R/W
0x4D	0	0	0	0	0	0	0	0	0x00	R/W
0x4E	0	0	DCLK_DIV1		O_VCO_BAND	O_VCO_CORE	O_VCO_BIAS	0	0x00	R/W
0x4F	0	0	0	0	0	0	0	0	0x00	R/W
0x50	0	0	0	0	0	0	0	0	0x00	R/W
0x51	0	0	0	0	0	0	0	0	0x00	R/W
0x52	0	0	0	0	0	0	0	0	0x00	R/W
0x53	0	PD_SYNC_MON	SYNC_SEL	RST_SYNC_MON	0	1	0	1	0x00	R/W
0x54	RESERVED							ADC_ST_CNV	0x00	R/W

REGISTER MAPS

Table 19. ADF4368 Register Summary (Continued)

Reg	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x55	0	0	0	0	0	0	0	0	0x00	R
0x56	0	0	0	0	0	0	0	0	0x00	R
0x57	0	0	0	0	0	0	0	0	0x00	R
0x58	EN_CLK2	EN_CLK1	SYNC_OK	0	REF_OK	ADC_BUSY	FSM_BUSY	LOCKED	0x00	R
0x59	0	0	0	0	0	0	0	0	0x00	R
0x5A	RESERVED						VCO_CORE		0x00	R
0x5B	CHIP_TEMP[7:0]								0x00	R
0x5C	RESERVED							CHIP_TEMP[8]	0x00	R
0x5D	0	0	0	0	0	0	0	0	0x00	R
0x5E	VCO_BAND								0x00	R
0x5F	0	0	0	0	0	0	0	0	0x00	R
0x60	RESERVED				VCO_BIAS				0x00	R
0x61	RESERVED				0	0	0	0	0x00	R
0x62	RESERVED					0	0	0	0x00	R
0x63	VERSION								0x00	R

REGISTER DETAILS

Address: 0x00, Reset: 0x00, Name: REG0000

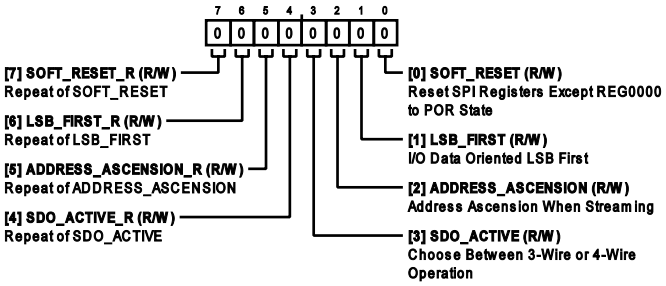

Figure 51.

Table 20. Bit Descriptions for REG0000

Bits	Bit Name	Description	Reset	Access
7	SOFT_RESET_R	Repeat of SOFT_RESET.	0x0	R/W
6	LSB_FIRST_R	Repeat of LSB_FIRST.	0x0	R/W
5	ADDRESS_ASCENSION_R	Repeat of ADDRESS_ASCENSION.	0x0	R/W
4	SDO_ACTIVE_R	Repeat of SDO_ACTIVE.	0x0	R/W
3	SDO_ACTIVE	Choose Between 3-Wire or 4-Wire Operation. 0: 3-wire 1: 4-wire SPI (enables SDO and SDIO becomes an input only)	0x0	R/W
2	ADDRESS_ASCENSION	Address Ascension When Streaming. 0: address auto-decrements when streaming. 1: address auto-increments when streaming.	0x0	R/W
1	LSB_FIRST	I/O Data Oriented LSB First. 0: MSB first. 1: LSB first.	0x0	R/W
0	SOFT_RESET	Reset SPI Registers Except REG0000 to POR State. Self-clearing reset. 0: Normal operation. 1: Soft reset.	0x0	R/W

Address: 0x01, Reset: 0x00, Name: REG0001

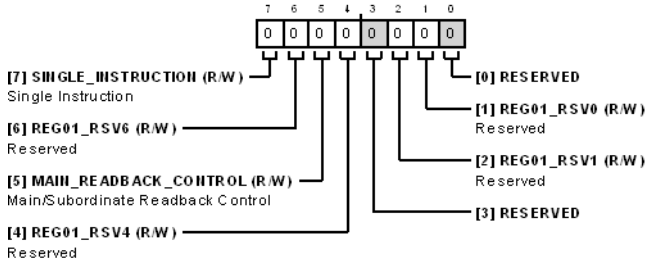

Figure 52.

Table 21. Bit Descriptions for REG0001

Bits	Bit Name	Description	Reset	Access
7	SINGLE_INSTRUCTION	Single Instruction. 0: SPI streaming enabled. 1: SPI streaming disabled.	0x0	R/W
6	REG01_RSV6	Reserved.	0x0	R/W

REGISTER DETAILS

Table 21. Bit Descriptions for REG0001 (Continued)

Bits	Bit Name	Description	Reset	Access
5	MAIN_READBACK_CONTROL	Main/Subordinate Readback Control. 0: double buffering, readback subordinate register. 1: double buffering, readback main register.	0x0	R/W
4	REG01_RSV4	Reserved.	0x0	R/W
3	RESERVED	Reserved.	0x0	R
2	REG01_RSV1	Reserved.	0x0	R/W
1	REG01_RSV0	Reserved.	0x0	R/W
0	RESERVED	Reserved.	0x0	R

Address: 0x02, Reset: 0x00, Name: REG0002

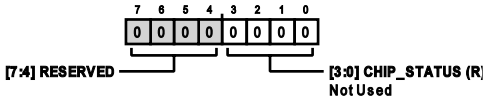

Figure 53.

Table 22. Bit Descriptions for REG0002

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHIP_STATUS	Not Used.	0x0	R

Address: 0x03, Reset: 0x00, Name: REG0003

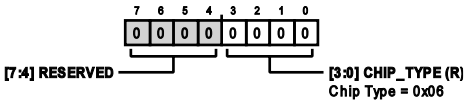

Figure 54.

Table 23. Bit Descriptions for REG0003

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHIP_TYPE	Chip Type = 0x06.	0x0	R

Address: 0x04, Reset: 0x00, Name: REG0004

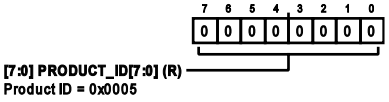

Figure 55.

Table 24. Bit Descriptions for REG0004

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product ID = 0x0007.	0x0	R

Address: 0x05, Reset: 0x00, Name: REG0005

REGISTER DETAILS

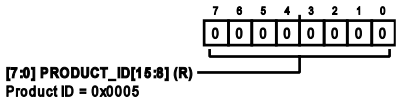

Figure 56.

Table 25. Bit Descriptions for REG0005

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product ID = 0x0007.	0x0	R

Address: 0x06, Reset: 0x00, Name: REG0006

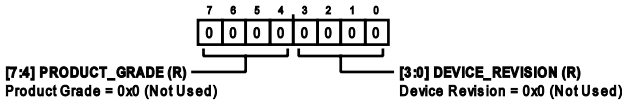

Figure 57.

Table 26. Bit Descriptions for REG0006

Bits	Bit Name	Description	Reset	Access
[7:4]	PRODUCT_GRADE	Product Grade = 0x0 (Not Used).	0x0	R
[3:0]	DEVICE_REVISION	Device Revision = 0x0 (Not Used).	0x0	R

Address: 0x0A, Reset: 0x00, Name: REG000A

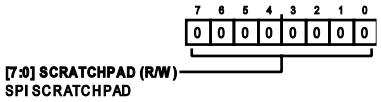

Figure 58.

Table 27. Bit Descriptions for REG000A

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCHPAD	SPI SCRATCHPAD.	0x0	R/W

Address: 0x0B, Reset: 0x00, Name: REG000B

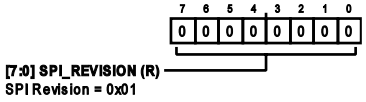

Figure 59.

Table 28. Bit Descriptions for REG000B

Bits	Bit Name	Description	Reset	Access
[7:0]	SPI_REVISION	SPI Revision = 0x01.	0x0	R

Address: 0x0C, Reset: 0x56, Name: REG000C

REGISTER DETAILS

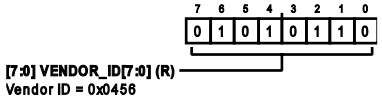

Figure 60.

Table 29. Bit Descriptions for REG000C

Bits	Bit Name	Description	Reset	Access
[7:0]	VENDOR_ID[7:0]	Vendor ID = 0x0456.	0x56	R

Address: 0x0D, Reset: 0x04, Name: REG000D

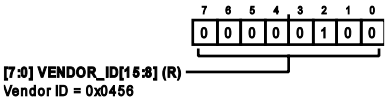

Figure 61.

Table 30. Bit Descriptions for REG000D

Bits	Bit Name	Description	Reset	Access
[7:0]	VENDOR_ID[15:8]	Vendor ID = 0x0456.	0x4	R

Address: 0x0F, Reset: 0x00, Name: REG000F

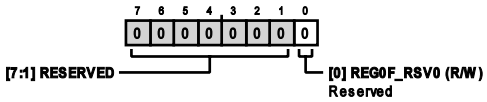

Figure 62.

Table 31. Bit Descriptions for REG000F

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	REG0F_RSV0	Reserved.	0x0	R/W

Address: 0x10, Reset: 0x80, Name: REG0010

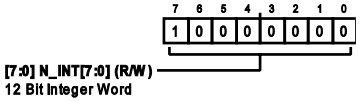

Figure 63.

Table 32. Bit Descriptions for REG0010

Bits	Bit Name	Description	Reset	Access
[7:0]	N_INT[7:0]	12 Bit Integer Word. Writing to Reg10 triggers autocalibration when EN_AUTOCAL = 1	0x80	R/W

Address: 0x11, Reset: 0x00, Name: REG0011

REGISTER DETAILS

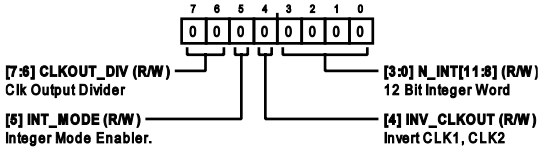

Figure 64.

Table 33. Bit Descriptions for REG0011

Bits	Bit Name	Description	Reset	Access
[7:6]	CLKOUT_DIV	Clk Output Divider. 00: Divide by 1. 01: Divide by 2. 10: Divide by 4. 11: Divide by 8.	0x0	R/W
5	INT_MODE	Integer Mode Enabler. 0: Fractional Mode. 1: Integer Mode.	0x0	R/W
4	INV_CLKOUT	Invert CLK1, CLK2. 0: RFCLK1, RFCLK2 Not Inverted. 1: RFCLK1, RFCLK2 Inverted.	0x0	R/W
[3:0]	N_INT[11:8]	12 Bit Integer Word. Writing to Reg10 triggers autocalibration when EN_AUTOCAL = 1	0x0	R/W

Address: 0x12, Reset: 0x00, Name: REG0012

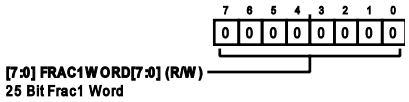

Figure 65.

Table 34. Bit Descriptions for REG0012

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC1WORD[7:0]	25 Bit Frac1 Word.	0x0	R/W

Address: 0x13, Reset: 0x00, Name: REG0013

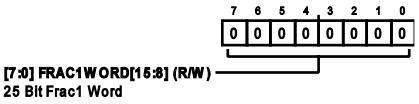

Figure 66.

Table 35. Bit Descriptions for REG0013

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC1WORD[15:8]	25 Bit Frac1 Word.	0x0	R/W

Address: 0x14, Reset: 0x00, Name: REG0014

REGISTER DETAILS

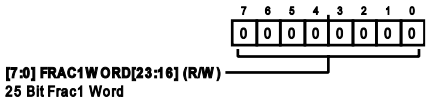

Figure 67.

Table 36. Bit Descriptions for REG0014

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC1WORD[23:16]	25 Bit Frac1 Word.	0x0	R/W

Address: 0x15, Reset: 0x00, Name: REG0015

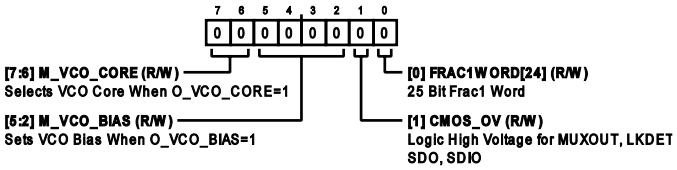

Figure 68.

Table 37. Bit Descriptions for REG0015

Bits	Bit Name	Description	Reset	Access
[7:6]	M_VCO_CORE	Selects VCO Core When O_VCO_CORE = 1. 00: VCO 0 Lowest Frequency. 01: VCO 1. 10: VCO 2. 11: VCO 3 Highest Frequency.	0x0	R/W
[5:2]	M_VCO_BIAS	Sets VCO Bias When O_VCO_BIAS = 1. 0000: Bias = 0. 0001: Bias = 1. 0010: Bias = 2. 0011: Bias = 3. 0100: Bias = 4. 0101: Bias = 5. 0110: Bias = 6. 0111: Bias = 7. 1000: Bias = 8. 1001: Bias = 9. 1010: Bias = 10. 1011: Bias = 11. 1100: Bias = 12. 1101: Bias = 13. 1110: Bias = 14. 1111: Bias = 15.	0x0	R/W
1	CMOS_OV	Logic High Voltage for MUXOUT, LKDET, SDO, SDIO. 0: 1.8 V Logic. 1: 3.3 V Logic.	0x0	R/W
0	FRAC1WORD[24]	25 Bit Frac1 Word.	0x0	R/W

Address: 0x16, Reset: 0x00, Name: REG0016

REGISTER DETAILS

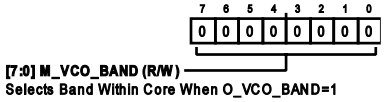

Figure 69.

Table 38. Bit Descriptions for REG0016

Bits	Bit Name	Description	Reset	Access
[7:0]	M_VCO_BAND	Selects Band Within Core When O_VCO_BAND = 1. 255 = lowest Frequency, 0 = highest Frequency	0x0	R/W

Address: 0x17, Reset: 0x00, Name: REG0017

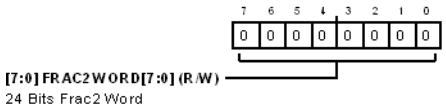

Figure 70.

Table 39. Bit Descriptions for REG0017

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC2WORD[7:0]	24 Bits Frac2 Word.	0x0	R/W

Address: 0x18, Reset: 0x00, Name: REG0018

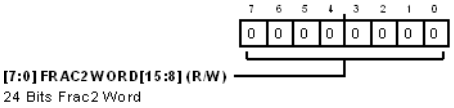

Figure 71.

Table 40. Bit Descriptions for REG0018

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC2WORD[15:8]	24 Bits Frac2 Word.	0x0	R/W

Address: 0x19, Reset: 0x00, Name: REG0019

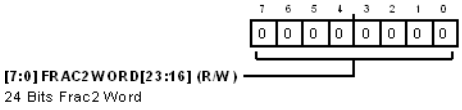

Figure 72.

Table 41. Bit Descriptions for REG0019

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC2WORD[23:16]	24 Bits Frac2 Word	0x0	R/W

Address: 0x1A, Reset: 0x00, Name: REG001A

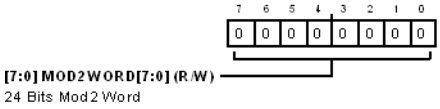

Figure 73.

REGISTER DETAILS

Table 42. Bit Descriptions for REG001A

Bits	Bit Name	Description	Reset	Access
[7:0]	MOD2WORD[7:0]	24 Bits Mod2 Word.	0x0	R/W

Address: 0x1B, Reset: 0x00, Name: REG001B

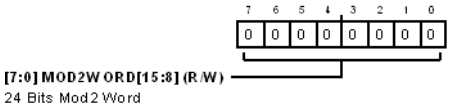

Figure 74.

Table 43. Bit Descriptions for REG001B

Bits	Bit Name	Description	Reset	Access
[7:0]	MOD2WORD[15:8]	24 Bits Mod2 Word.	0x0	R/W

Address: 0x1C, Reset: 0x00, Name: REG001C

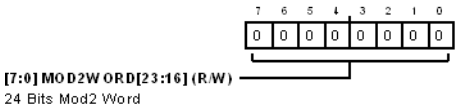

Figure 75.

Table 44. Bit Descriptions for REG001C

Bits	Bit Name	Description	Reset	Access
[7:0]	MOD2WORD[23:16]	24 Bits Mod2 Word	0x0	R/W

Address: 0x1D, Reset: 0x00, Name: REG001D

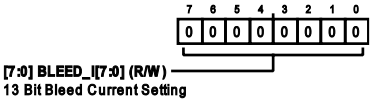

Figure 76.

Table 45. Bit Descriptions for REG001D

Bits	Bit Name	Description	Reset	Access
[7:0]	BLEED_I[7:0]	13 Bit Bleed Current Setting. 4-bit MSB for coarse setting and 9-bit LSB for fine setting	0x0	R/W

Address: 0x1E, Reset: 0x00, Name: REG001E

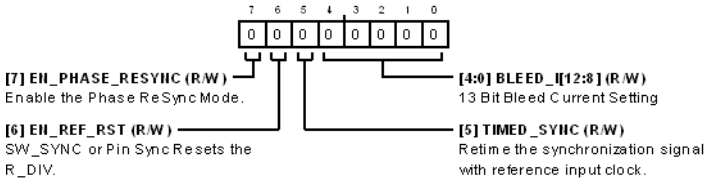

Figure 77.

REGISTER DETAILS

Table 46. Bit Descriptions for REG001E

Bits	Bit Name	Description	Reset	Access
7	EN_PHASE_RESYNC	Enable the Phase ReSync Mode.	0x0	R/W
6	EN_REF_RST	SW_SYNC or Pin Sync Resets the R_DIV.	0x0	R/W
5	TIMED_SYNC	Retime the synchronization signal with reference input clock. 0: RDIV are Reset Asynchronously. 1: The synchronization signal is retimed with reference input clock.	0x0	R/W
[4:0]	BLEED_I[12:8]	13 Bit Bleed Current Setting. 4-bit MSB for coarse setting and 9-bit LSB for fine setting	0x0	R/W

Address: 0x1F, Reset: 0x00, Name: REG001F

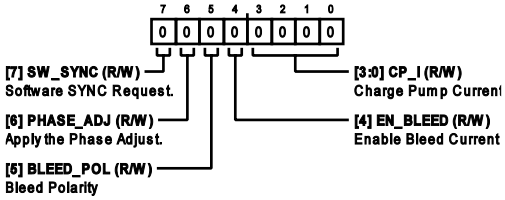

Figure 78.

Table 47. Bit Descriptions for REG001F

Bits	Bit Name	Description	Reset	Access
7	SW_SYNC	Software SYNC Request.	0x0	R/W
6	PHASE_ADJ	Apply the Phase Adjust.	0x0	R/W
5	BLEED_POL	Bleed Polarity. 0: Current Sink. 1: Current Source.	0x0	R/W
4	EN_BLEED	Enable Bleed Current. 0: Bleed Current Disabled. 1: Bleed Current Enabled.	0x0	R/W
[3:0]	CP_I	Charge Pump Current. For corresponding current values, see Table 11.	0x0	R/W

Address: 0x20, Reset: 0x01, Name: REG0020

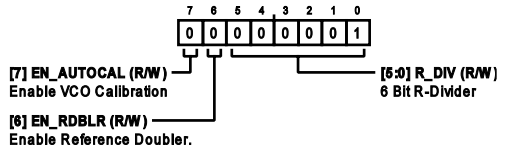

Figure 79.

Table 48. Bit Descriptions for REG0020

Bits	Bit Name	Description	Reset	Access
7	EN_AUTOCAL	Enable VCO Calibration. 0: VCO Calibration Disabled. 1: VCO Calibration Enabled.	0x0	R/W
6	EN_RDBLR	Enable Reference Doubler. 0: Doubler Disabled. 1: Doubler Enabled.	0x0	R/W
[5:0]	R_DIV	6 Bit R-Divider.	0x1	R/W

REGISTER DETAILS

Address: 0x21, Reset: 0x00, Name: REG0021

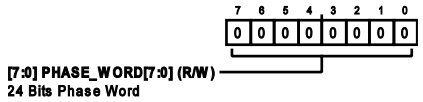

Figure 80.

Table 49. Bit Descriptions for REG0021

Bits	Bit Name	Description	Reset	Access
[7:0]	PHASE_WORD[7:0]	24 Bits Phase Word.	0x0	R/W

Address: 0x22, Reset: 0x00, Name: REG0022

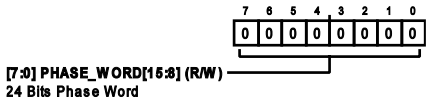

Figure 81.

Table 50. Bit Descriptions for REG0022

Bits	Bit Name	Description	Reset	Access
[7:0]	PHASE_WORD[15:8]	24 Bits Phase Word.	0x0	R/W

Address: 0x23, Reset: 0x00, Name: REG0023

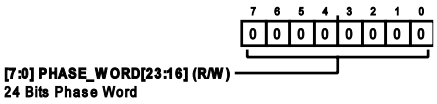

Figure 82.

Table 51. Bit Descriptions for REG0023

Bits	Bit Name	Description	Reset	Access
[7:0]	PHASE_WORD[23:16]	24 Bits Phase Word.	0x0	R/W

Address: 0x24, Reset: 0x00, Name: REG0024

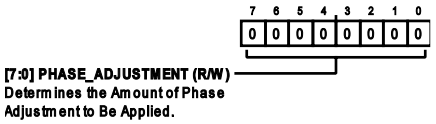

Figure 83.

Table 52. Bit Descriptions for REG0024

Bits	Bit Name	Description	Reset	Access
[7:0]	PHASE_ADJUSTMENT	Determines the Amount of Phase Adjustment to Be Applied. PHASE_ADJUSTMENT = Phase(deg) × 2^{12}/360.	0x0	R/W

Address: 0x25, Reset: 0x00, Name: REG0025

REGISTER DETAILS

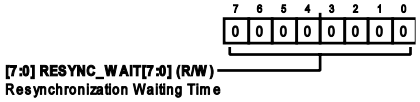

Figure 84.

Table 53. Bit Descriptions for REG0025

Bits	Bit Name	Description	Reset	Access
[7:0]	RESYNC_WAIT[7:0]	Resynchronization Waiting Time. Sets the Waiting Time After the Write of the Register 10 to Apply the Resynchronization (RESYNC_WAIT × PFD).	0x0	R/W

Address: 0x26, Reset: 0x00, Name: REG0026

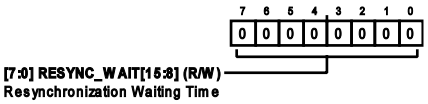

Figure 85.

Table 54. Bit Descriptions for REG0026

Bits	Bit Name	Description	Reset	Access
[7:0]	RESYNC_WAIT[15:8]	Resynchronization Waiting Time. Sets the Waiting Time After the Write of the Register 10 to Apply the Resynchronization (RESYNC_WAIT × PFD).	0x0	R/W

Address: 0x27, Reset: 0x00, Name: REG0027

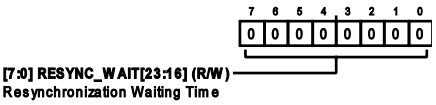

Figure 86.

Table 55. Bit Descriptions for REG0027

Bits	Bit Name	Description	Reset	Access
[7:0]	RESYNC_WAIT[23:16]	Resynchronization Waiting Time. Sets the Waiting Time After the Write of the Register 10 to Apply the Resynchronization (RESYNC_WAIT × PFD).	0x0	R/W

Address: 0x28, Reset: 0x00, Name: REG0028

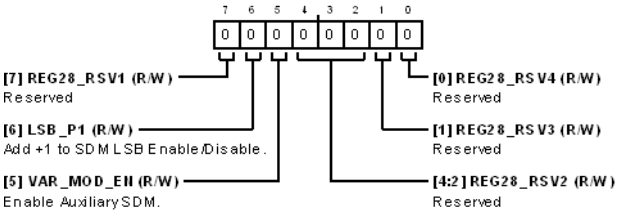

Figure 87.

Table 56. Bit Descriptions for REG0028

Bits	Bit Name	Description	Reset	Access
7	REG28_RSV1	Reserved.	0x0	R/W
6	LSB_P1	Add +1 to SDM LSB Enable/Disable.	0x0	R/W
5	VAR_MOD_EN	Enable Auxiliary SDM.	0x0	R/W

REGISTER DETAILS

Table 56. Bit Descriptions for REG0028 (Continued)

Bits	Bit Name	Description	Reset	Access
[4:2]	REG28_RSV2	Reserved.	0x0	R/W
1	REG28_RSV3	Reserved.	0x0	R/W
0	REG28_RSV4	Reserved.	0x0	R/W

Address: 0x29, Reset: 0x00, Name: REG0029

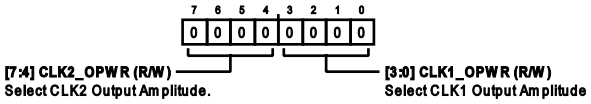

Figure 88.

Table 57. Bit Descriptions for REG0029

Bits	Bit Name	Description	Reset	Access
[7:4]	CLK2_OPWR	Select CLK2 Output Amplitude. 0000: Min Power Setting. 1111: Max Power Setting.	0x0	R/W
[3:0]	CLK1_OPWR	Select CLK1 Output Amplitude. 0000: Min Power Setting. 1111: Max Power Setting.	0x0	R/W

Address: 0x2A, Reset: 0x04, Name: REG002A

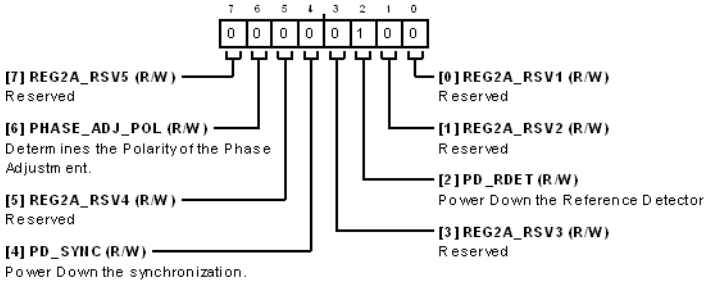

Figure 89.

Table 58. Bit Descriptions for REG002A

Bits	Bit Name	Description	Reset	Access
7	REG2A_RSV5	Reserved.	0x0	R/W
6	PHASE_ADJ_POL	Determines the Polarity of the Phase Adjustment. 0: Adds The Selected Phase Value. 1: Subtract The Selected Phase Value.	0x0	R/W
5	REG2A_RSV4	Reserved.	0x0	R/W
4	PD_SYNC	Power Down the synchronization.	0x0	R/W
3	REG2A_RSV3	Reserved.	0x0	R/W
2	PD_RDET	Power Down the Reference Detector. 0: Normal Operation. 1: Power Down the Reference Detector.	0x1	R/W
1	REG2A_RSV2	Reserved.	0x0	R/W
0	REG2A_RSV1	Reserved.	0x0	R/W

REGISTER DETAILS

Address: 0x2B, Reset: 0x83, Name: REG002B

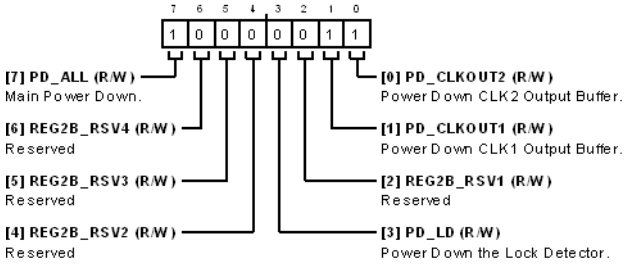

Figure 90.

Table 59. Bit Descriptions for REG002B

Bits	Bit Name	Description	Reset	Access
7	PD_ALL	Main Power Down. 0: Normal Operation. 1: Power Down.	0x1	R/W
6	REG2B_RSV4	Reserved.	0x0	R/W
5	REG2B_RSV3	Reserved.	0x0	R/W
4	REG2B_RSV2	Reserved.	0x0	R/W
3	PD_LD	Power Down the Lock Detector. 0: Normal Operation. 1: Power Down the Lock Detector.	0x0	R/W
2	REG2B_RSV1	Reserved.	0x0	R/W
1	PD_CLKOUT1	Power Down CLK1 Output Buffer. 0: Normal Operation. 1: Power Down CLK1 Output.	0x1	R/W
0	PD_CLKOUT2	Power Down CLK2 Output Buffer. 0: Normal Operation. 1: Power Down CLK2 Output.	0x1	R/W

Address: 0x2C, Reset: 0x00, Name: REG002C

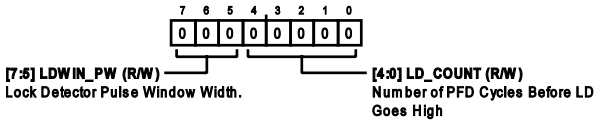

Figure 91.

Table 60. Bit Descriptions for REG002C

Bits	Bit Name	Description	Reset	Access
[7:5]	LDWIN_PW	Lock Detector Pulse Window Width. The details are given in Table 14.	0x0	R/W
[4:0]	LD_COUNT	Number of PFD Cycles Before LD Goes High. Cycles = $24 \times \sqrt{2}^{LD\_COUNT} + 3$ if LD_COUNT is even $32 \times \sqrt{2}^{LD\_COUNT - 1} + 3$ if LD_COUNT is odd	0x0	R/W

Address: 0x2D, Reset: 0x00, Name: REG002D

REGISTER DETAILS

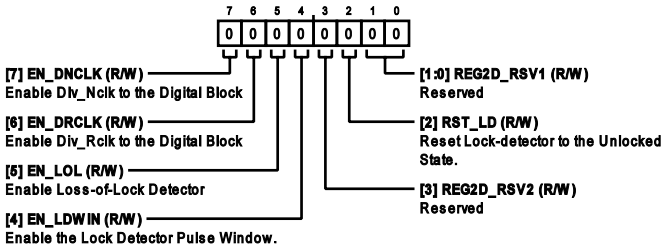

Figure 92.

Table 61. Bit Descriptions for REG002D

Bits	Bit Name	Description	Reset	Access
7	EN_DNCLK	Enable Div_Nclk to the Digital Block. 0: Div_Nclk off. 1: Div_Nclk on.	0x0	R/W
6	EN_DRCLK	Enable Div_Rclk to the Digital Block. 0: DIv_Rclk off. 1: Div_Rclk on.	0x0	R/W
5	EN_LOL	Enable Loss-of-Lock Detector. 0: Disable loss-of-lock detector. 1: Enable loss-of-lock detector.	0x0	R/W
4	EN_LDWIN	Enable the Lock Detector Pulse Window. 0: Lock detector pulse window disabled. 1: Lock detector pulse window enabled.	0x0	R/W
3	REG2D_RSV2	Reserved.	0x0	R/W
2	RST_LD	Reset Lock Detector to the Unlocked State. 0: Reset inactive. 1: Reset active.	0x0	R/W
[1:0]	REG2D_RSV1	Reserved.	0x0	R/W

Address: 0x2E, Reset: 0x00, Name: REG002E

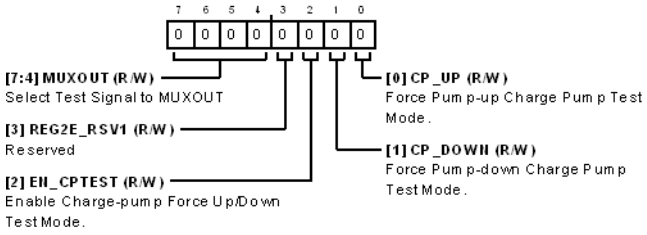

Figure 93.

Table 62. Bit Descriptions for REG002E

Bits	Bit Name	Description	Reset	Access
[7:4]	MUXOUT	Select Test Signal to MUXOUT. 0000: High-Z. 0001: LKDET. 0010: low. 0011: low. 0100: Div_Rclk/2. 0101: Div_Nclk/2.	0x0	R/W

REGISTER DETAILS

Table 62. Bit Descriptions for REG002E (Continued)

Bits	Bit Name	Description	Reset	Access
		0110: reserved. 0111: low. 1000: high. 1001: reserved. 1010: reserved. 1011: low. 1100: low. 1101: low. 1110: reserved. 1111: reserved.		
3	REG2E_RSV1	Reserved.	0x0	R/W
2	EN_CPTEST	Enable Charge Pump Force Up/Down Test Mode. 0: charge-pump force up/down test mode off (normal operation). 1: charge-pump force up/down test mode on.	0x0	R/W
1	CP_DOWN	Force Pump Down Charge Pump Test Mode. 0: force pump down off. 1: force pump down on.	0x0	R/W
0	CP_UP	Force Pump Up Charge Pump Test Mode. 0: force pump up off. 1: force pump up on.	0x0	R/W

Address: 0x2F, Reset: 0x00, Name: REG002F

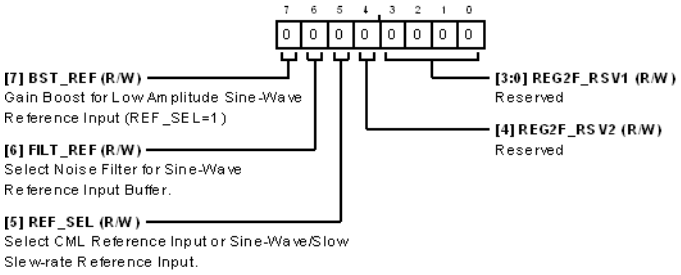

Figure 94.

Table 63. Bit Descriptions for REG002F

Bits	Bit Name	Description	Reset	Access
7	BST_REF	Gain Boost for Low Amplitude Sine-Wave Reference Input (REF_SEL = 1). 0: use for large reference input signals > 1.6 V p-p when REF_SEL = 1. 1: use for large reference input signals < 1.6 V p-p when REF_SEL = 1.	0x0	R/W
6	FILT_REF	Select Noise Filter for Sine-Wave Reference Input Buffer. 0: noise filter off. 1: noise filter on.	0x0	R/W
5	REF_SEL	Select CML Reference Input or Sine Wave/Slow Slew Rate Reference Input. 0: DMA. Delay matched amplifier (DMA), for improved reference to clock output delay. 1: LNA. Low noise amplifier (LNA), for low slew rate signals/low frequency sine waves.	0x0	R/W
4	REG2F_RSV2	Reserved.	0x0	R/W
[3:0]	REG2F_RSV1	Reserved.	0x0	R/W

Address: 0x30, Reset: 0x00, Name: REG0030

REGISTER DETAILS

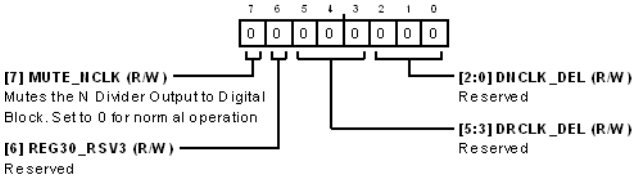

Figure 95.

Table 64. Bit Descriptions for REG0030

Bits	Bit Name	Description	Reset	Access
7	MUTE_NCLK	Mutes the N Divider Output to Digital Block. Set to 0 for normal operation.	0x0	R/W
6	REG30_RSV3	Reserved.	0x0	R/W
[5:3]	DRCLK_DEL	Reserved.	0x0	R/W
[2:0]	DNCLK_DEL	Reserved.	0x0	R/W

Address: 0x31, Reset: 0x00, Name: REG0031

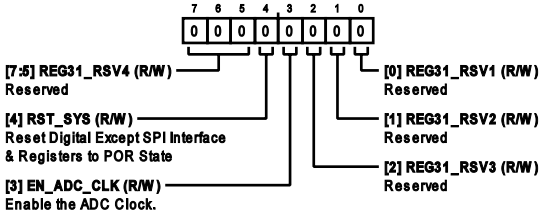

Figure 96.

Table 65. Bit Descriptions for REG0031

Bits	Bit Name	Description	Reset	Access
[7:5]	REG31_RSV4	Reserved.	0x0	R/W
4	RST_SYS	Reset Digital Except SPI Interface and Registers to POR State. 0: reset inactive. 1: reset active.	0x0	R/W
3	EN_ADC_CLK	Enable the ADC Clock. 0: disable ADC clock. 1: enable ADC clock.	0x0	R/W
2	REG31_RSV3	Reserved.	0x0	R/W
1	REG31_RSV2	Reserved.	0x0	R/W
0	REG31_RSV1	Reserved.	0x0	R/W

Address: 0x35, Reset: 0x00, Name: REG0035

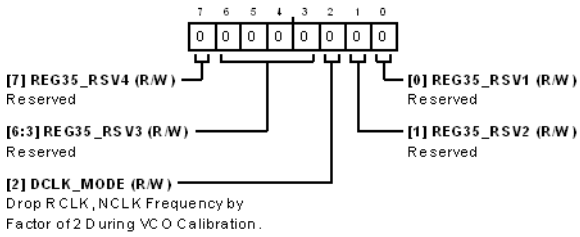

Figure 97.

REGISTER DETAILS

Table 66. Bit Descriptions for REG0035

Bits	Bit Name	Description	Reset	Access
7	REG35_RSV4	Reserved.	0x0	R/W
[6:3]	REG35_RSV3	Reserved.	0x0	R/W
2	DCLK_MODE	Drop RCLK, NCLK Frequency by Factor of 2 During VCO Calibration. 0: disable frequency reduction. 1: enable frequency reduction.	0x0	R/W
1	REG35_RSV2	Reserved.	0x0	R/W
0	REG35_RSV1	Reserved.	0x0	R/W

Address: 0x36, Reset: 0x00, Name: REG0036

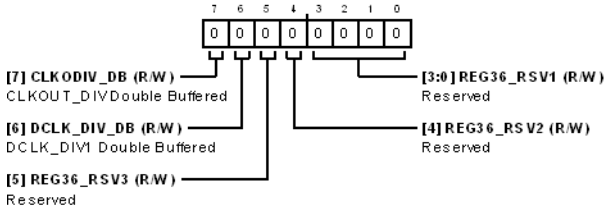

Figure 98.

Table 67. Bit Descriptions for REG0036

Bits	Bit Name	Description	Reset	Access
7	CLKODIV_DB	CLKOUT_DIV Double Buffered. 0: CLKOUT_DIV not double buffered. 1: CLKOUT_DIV double buffered.	0x0	R/W
6	DCLK_DIV_DB	DCLK_DIV1 Double Buffered. 0: not double buffered. 1: double buffered.	0x0	R/W
5	REG36_RSV3	Reserved.	0x0	R/W
4	REG36_RSV2	Reserved.	0x0	R/W
[3:0]	REG36_RSV1	Reserved.	0x0	R/W

Address: 0x37, Reset: 0x00, Name: REG0037

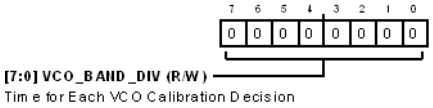

Figure 99.

Table 68. Bit Descriptions for REG0037

Bits	Bit Name	Description	Reset	Access
[7:0]	VCO_BAND_DIV	Time for Each VCO Calibration Decision. VCO calibration time per Decision = 16 × VCO_BAND_DIV/(Div_Rclk frequency)	0x0	R/W

Address: 0x38, Reset: 0x00, Name: REG0038

REGISTER DETAILS

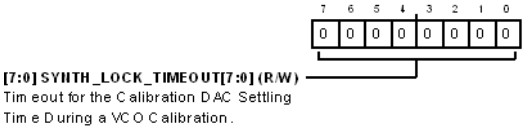

Figure 100.

Table 69. Bit Descriptions for REG0038

Bits	Bit Name	Description	Reset	Access
[7:0]	SYNTH_LOCK_TIMEOUT[7:0]	Timeout for the Calibration DAC Settling Time During a VCO Calibration. Time = SYNTH_LOCK_TIMEOUT/(f_{DIV_RCLK} Frequency)	0x0	R/W

Address: 0x39, Reset: 0x00, Name: REG0039

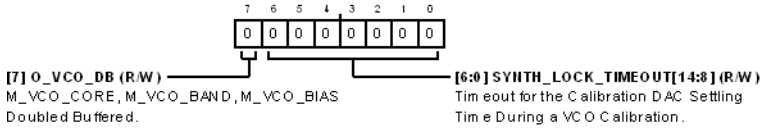

Figure 101.

Table 70. Bit Descriptions for REG0039

Bits	Bit Name	Description	Reset	Access
7	O_VCO_DB	M_VCO_CORE, M_VCO_BAND, M_VCO_BIAS Doubled Buffered. 0: core, bias, and band not double buffered. 1: core, bias, and band double buffered.	0x0	R/W
[6:0]	SYNTH_LOCK_TIMEOUT[14:8]	Timeout for the Calibration DAC Settling Time During a VCO Calibration. Time = SYNTH_LOCK_TIMEOUT/(f_{DIV_RCLK} Frequency)	0x0	R/W

Address: 0x3A, Reset: 0x00, Name: REG003A

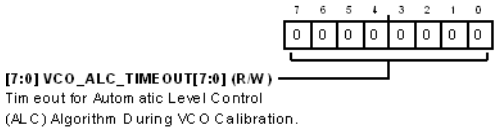

Figure 102.

Table 71. Bit Descriptions for REG003A

Bits	Bit Name	Description	Reset	Access
[7:0]	VCO_ALC_TIMEOUT[7:0]	Timeout for Automatic Level Control (ALC) Algorithm During VCO Calibration. Time = VCO_ALC_TIMEOUT[14:0]/(f_{DIV_RCLK} Frequency)	0x0	R/W

Address: 0x3B, Reset: 0x00, Name: REG003B

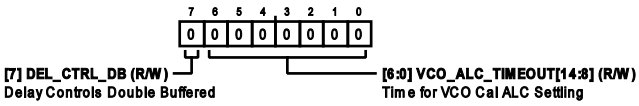

Figure 103.

Table 72. Bit Descriptions for REG003B

Bits	Bit Name	Description	Reset	Access
7	DEL_CTRL_DB	Delay Controls Double Buffered. INV_CLKOUT, BLEED_I, BLEED_POL double buffered.	0x0	R/W

REGISTER DETAILS

Table 72. Bit Descriptions for REG003B (Continued)

Bits	Bit Name	Description	Reset	Access
		0: not double buffered. 1: double buffered.		
[6:0]	VCO_ALC_TIMEOUT[14:8]	Timeout for Automatic Level Control (ALC) Algorithm During VCO Calibration. Time = VCO_ALC_TIMEOUT[14:0]/(f_{DIV_RCLK} Frequency)	0x0	R/W

Address: 0x3E, Reset: 0x00, Name: REG003E

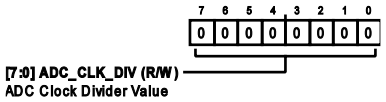

Figure 104.

Table 73. Bit Descriptions for REG003E

Bits	Bit Name	Description	Reset	Access
[7:0]	ADC_CLK_DIV	ADC Clock Divider Value. Desired ADC clock frequency < 400 kHz. If ADC_CLK_DIV = round up (((f_{DIV_RCLK})/(Desired ADC Clock Frequency))−2)/4.	0x0	R/W

Address: 0x3F, Reset: 0x00, Name: REG003F

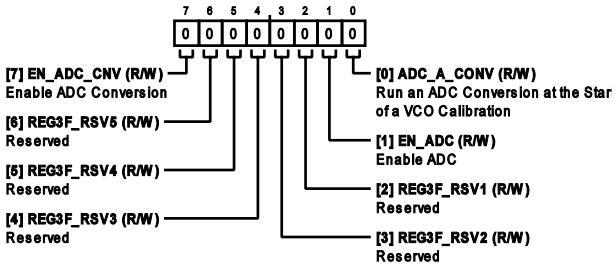

Figure 105.

Table 74. Bit Descriptions for REG003F

Bits	Bit Name	Description	Reset	Access
7	EN_ADC_CNV	Enable ADC Conversion. 0: no ADC conversion. 1: enabled. Normal operation.	0x0	R/W
6	REG3F_RSV5	Reserved.	0x0	R/W
5	REG3F_RSV4	Reserved.	0x0	R/W
4	REG3F_RSV3	Reserved.	0x0	R/W
3	REG3F_RSV2	Reserved.	0x0	R/W
2	REG3F_RSV1	Reserved.	0x0	R/W
1	EN_ADC	Enable ADC. 0: ADC Disabled. 1: ADC Enabled.	0x0	R/W
0	ADC_A_CONV	Run an ADC Conversion at the Start of a VCO Calibration. 0: ADC conversion only possible with write to ADC_ST_CNV bit field. 1: enabled. Normal operation. Automatically begins ADC conversion at the start of a VCO calibration or with write to ADC_ST_CNV bit field.	0x0	R/W

Address: 0x40, Reset: 0x00, Name: REG0040

REGISTER DETAILS

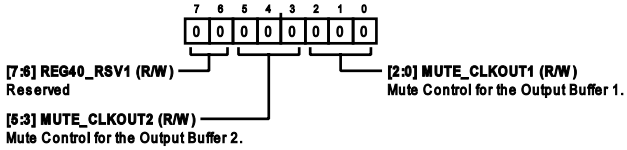

Figure 106.

Table 75. Bit Descriptions for REG0040

Bits	Bit Name	Description	Reset	Access
[7:6]	REG40_RSV1	Reserved.	0x0	R/W
[5:3]	MUTE_CLKOUT2	Mute Control for the Output Buffer 2.	0x0	R/W
[2:0]	MUTE_CLKOUT1	Mute Control for the Output Buffer 1.	0x0	R/W

Address: 0x43, Reset: 0x00, Name: REG0043

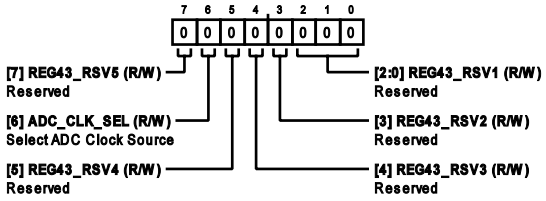

Figure 107.

Table 76. Bit Descriptions for REG0043

Bits	Bit Name	Description	Reset	Access
7	REG43_RSV5	Reserved.	0x0	R/W
6	ADC_CLK_SEL	Select ADC Clock Source. 0: Use Rclk as ADC Clock Source (normal Operation). 1: Use SPI SCLK as ADC Clock Source (test Mode).	0x0	R/W
5	REG43_RSV4	Reserved.	0x0	R/W
4	REG43_RSV3	Reserved.	0x0	R/W
3	REG43_RSV2	Reserved.	0x0	R/W
[2:0]	REG43_RSV1	Reserved.	0x0	R/W

Address: 0x4E, Reset: 0x00, Name: REG004E

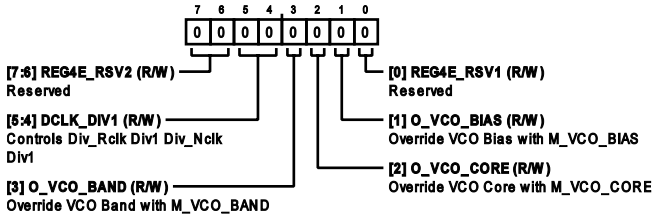

Figure 108.

Table 77. Bit Descriptions for REG004E

Bits	Bit Name	Description	Reset	Access
[7:6]	REG4E_RSV2	Reserved.	0x0	R/W
[5:4]	DCLK_DIV1	Controls Div_Rclk Div1 Div_Nclk Div1.	0x0	R/W

REGISTER DETAILS

Table 77. Bit Descriptions for REG004E (Continued)

Bits	Bit Name	Description	Reset	Access
		00: Divide by 1. 01: Divide by 2. 10: Divide by 4. 11: Divide by 8.		
3	O_VCO_BAND	Override VCO Band with M_VCO_BAND. 0: VCO Band Code from VCO Calibration State-machine. 1: VCO Band Code from M_VCO_BAND.	0x0	R/W
2	O_VCO_CORE	Override VCO Core with M_VCO_CORE. 0: VCO Core Select from VCO Calibration State-machine. 1: VCO Core Select from M_VCO_CORE.	0x0	R/W
1	O_VCO_BIAS	Override VCO Bias with M_VCO_BIAS. 0: VCO Bias Code from VCO Calibration State-machine. 1: VCO Bias Code from M_VCO_VBIAS.	0x0	R/W
0	REG4E_RSV1	Reserved.	0x0	R/W

Address: 0x53, Reset: 0x00, Name: REG0053

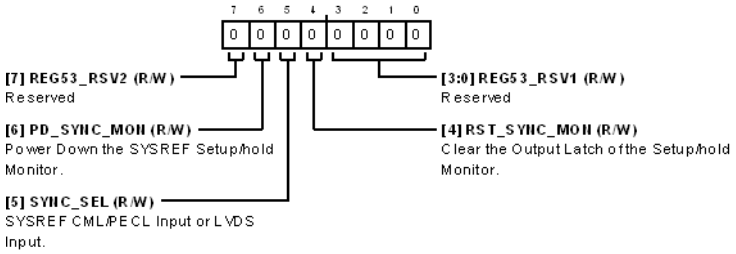

Figure 109.

Table 78. Bit Descriptions for REG0053

Bits	Bit Name	Description	Reset	Access
7	REG53_RSV2	Reserved.	0x0	R/W
6	PD_SYNC_MON	Power Down the SYSREF Setup/hold Monitor. 0: Normal Operation. 1: Power Down the SYSREF Setup/hold Monitor.	0x0	R/W
5	SYNC_SEL	SYSREF CML/PECL Input or LVDS Input. 0: CML/PECL Input. 1: LVDS Input.	0x0	R/W
4	RST_SYNC_MON	Clear the Output Latch of the Setup/hold Monitor. 0: Reset Inactive. 1: Reset Active.	0x0	R/W
[3:0]	REG53_RSV1	Reserved.	0x0	R/W

Address: 0x54, Reset: 0x00, Name: REG0054

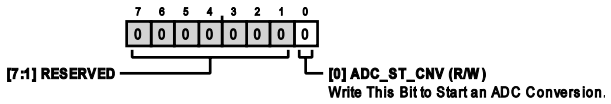

Figure 110.

REGISTER DETAILS

Table 79. Bit Descriptions for REG0054

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	ADC_ST_CNV	Write This Bit to Start an ADC Conversion.	0x0	R/W

Address: 0x58, Reset: 0x00, Name: REG0058

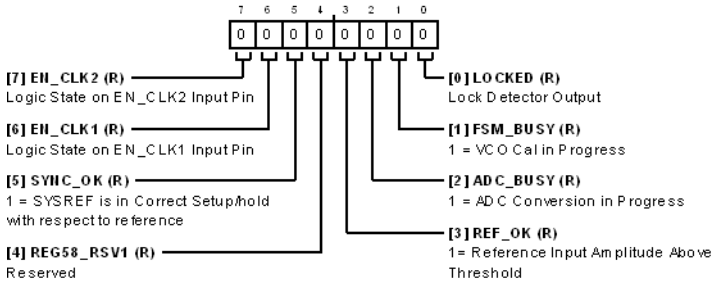

Figure 111.

Table 80. Bit Descriptions for REG0058

Bits	Bit Name	Description	Reset	Access
7	EN_CLK2	Logic State on EN_CLK2 Input Pin.	0x0	R
6	EN_CLK1	Logic State on EN_CLK1 Input Pin.	0x0	R
5	SYNC_OK	1 = SYSREF is in Correct Setup/hold with respect to reference.	0x0	R
4	REG58_RSV1	Reserved.	0x0	R
3	REF_OK	1= Reference Input Amplitude Above Threshold.	0x0	R
2	ADC_BUSY	1 = ADC Conversion in Progress.	0x0	R
1	FSM_BUSY	1 = VCO Cal in Progress.	0x0	R
0	LOCKED	Lock Detector Output.	0x0	R

Address: 0x5A, Reset: 0x00, Name: REG005A

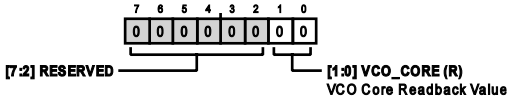

Figure 112.

Table 81. Bit Descriptions for REG005A

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	VCO_CORE	VCO Core Readback Value.	0x0	R

Address: 0x5B, Reset: 0x00, Name: REG005B

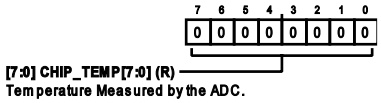

Figure 113.

REGISTER DETAILS

Table 82. Bit Descriptions for REG005B

Bits	Bit Name	Description	Reset	Access
[7:0]	CHIP_TEMP[7:0]	Temperature Measured by the ADC. Bit[8] = Sign Bits[7:0] = Magnitude	0x0	R

Address: 0x5C, Reset: 0x00, Name: REG005C

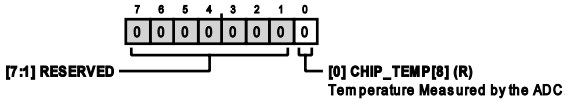

Figure 114.

Table 83. Bit Descriptions for REG005C

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	CHIP_TEMP[8]	Temperature Measured by the ADC. Bit[8] = Sign Bits[7:0] = Magnitude	0x0	R

Address: 0x5E, Reset: 0x00, Name: REG005E

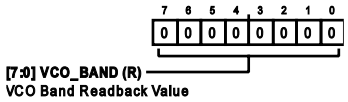

Figure 115.

Table 84. Bit Descriptions for REG005E

Bits	Bit Name	Description	Reset	Access
[7:0]	VCO_BAND	VCO Band Readback Value.	0x0	R

Address: 0x60, Reset: 0x00, Name: REG0060

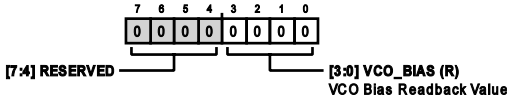

Figure 116.

Table 85. Bit Descriptions for REG0060

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	VCO_BIAS	VCO Bias Readback Value.	0x0	R

Address: 0x63, Reset: 0x00, Name: REG0063

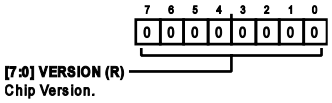

Figure 117.

REGISTER DETAILS

Table 86. Bit Descriptions for REG0063

Bits	Bit Name	Description	Reset	Access
[7:0]	VERSION	Chip Version.	0x0	R

OUTLINE DIMENSIONS

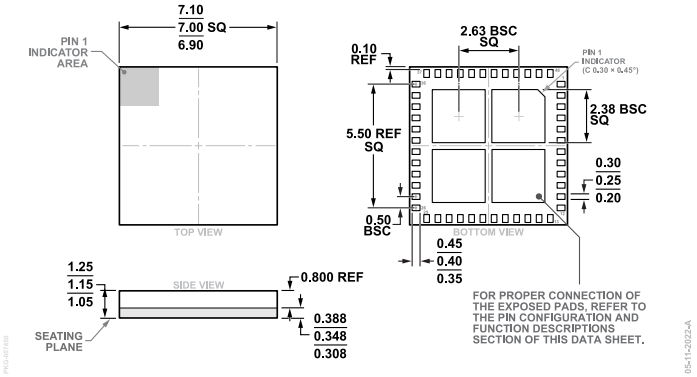

Figure 118. 48-Lead Land Grid Array Package [LGA]
7 mm × 7 mm Body
CC-48-13
Dimensions Shown in millimeters

Updated: March 17, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADF4368BCCZ	−40°C to +105°C	48-Terminal Land Grid Array [LGA] (7 mm x 7 mm)	Tray, 260	CC-48-13
ADF4368BCCZ-RL7	−40°C to +105°C	48-Terminal Land Grid Array [LGA] (7 mm x 7 mm)	Reel, 500	CC-48-13

[1] Z = RoHS-Compliant Part.

EVALUATION BOARDS

Model[1]	Description
EV-ADF4368SD1Z	Evaluation Board

[1] Z = RoHS-Compliant Part.

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