Microwave Wideband Synthesizer with Integrated VCO

Data Sheet

ADF4371

FEATURES

RF output frequency range: 62.5 MHz to 32,000 MHz
Fractional-N synthesizer and Integer N synthesizer
High resolution 39-bit fractional modulus
Typical spurious PFD: −90 dBc
Integrated rms jitter: 38 fs (1 kHz to 100 MHz)
Normalized phase noise floor: −234 dBc/Hz
PFD operation to 250 MHz
Reference frequency operation to 600 MHz
Programmable divide by 1, 2, 4, 8, 16, 32, or 64 output
62.5 MHz to 8,000 MHz output at RF8x and RFAUX8x
8,000 MHz to 16,000 MHz output at RF16x
16,000 MHz to 32,000 MHz output at RF32x
Lock time approximately 3 ms with automatic calibration
Lock time <30 μs with autocalibration bypassed
Analog and digital power supplies: 3.3 V
VCO power supply: 3.3 V and 5 V
RF output mute function
7mm × 7mm, 48-terminal LGA package

APPLICATIONS

Wireless infrastructure (multicarrier global system for mobile communication (MC-GSM), 5 G)
Test equipment and instrumentation
Clock generation
Aerospace and defense

GENERAL DESCRIPTION

The ADF4371 allows implementation of fractional-N or Integer N phase-locked loop (PLL) frequency synthesizers when used with an external loop filter and an external reference frequency. The wideband microwave voltage controlled oscillator (VCO) design allows frequencies from 62.5 MHz to 32 GHz to be generated.

The ADF4371 has an integrated VCO with a fundamental output frequency ranging from 4000 MHz to 8000 MHz. In addition, the VCO frequency is connected to divide by 1, 2, 4, 8, 16, 32, or 64 circuits that allows the user to generate radio frequency (RF) output frequencies as low as 62.5 MHz at RF8x. A frequency multiplier at RF16x generates from 8 GHz to 16 GHz. A frequency quadrupler generates frequencies from 16 GHz to 32 GHz at RF32x. RFAUX8x duplicates the frequency range of RF8x or permits direct access to the VCO output. To suppress the unwanted products of frequency multiplication, a harmonic filter exists between the multipliers and the output stages of RF16x and RF32x.

Control of all on-chip registers is through a 3-wire interface. The ADF4371 operates with analog and digital power supplies ranging from 3.15 V to 3.45 V, and 5 V for the VCO power supply. The ADF4371 also contains hardware and software power-down modes.

FUNCTIONAL BLOCK DIAGRAM

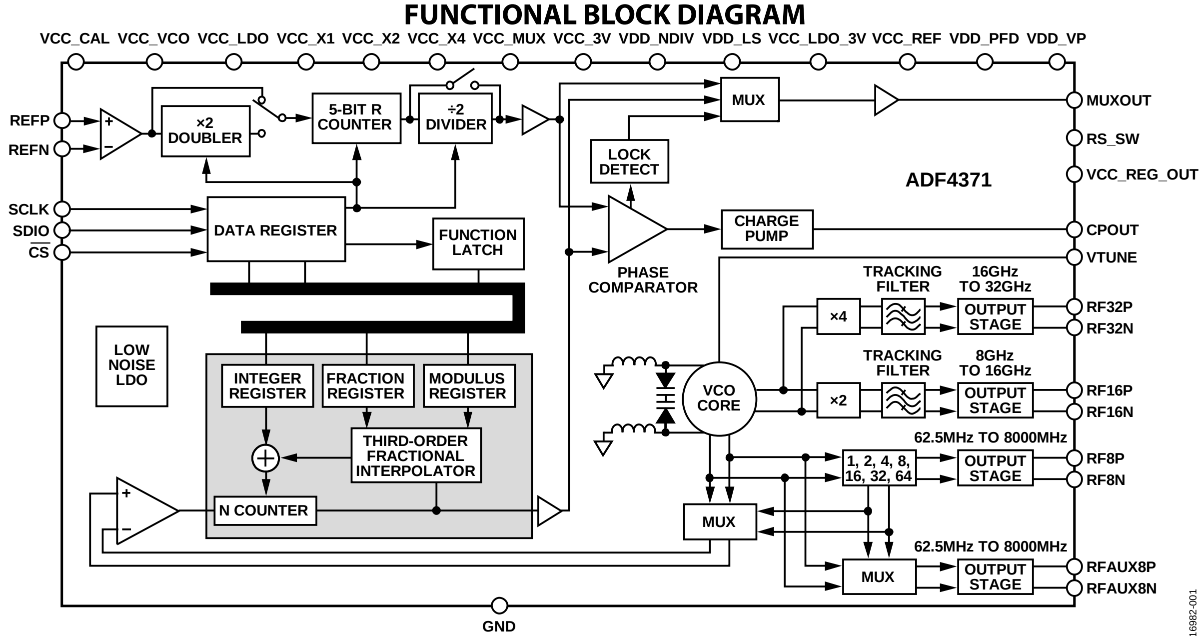

Figure 1.

Rev. A

Document Feedback

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REVISION HISTORY

9/2021—Rev. 0 to Rev. A

1/2019—Revision 0: Initial Version

SPECIFICATIONS

4.75 V ≤ VCC_VCO ≤ 5.25 V, all other supply pins (AV_{DD}) = 3.3 V ± 5%, GND = 0 V, dBm referred to 50 Ω, T_A = whole operating temperature range, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
REFP AND REFN CHARACTERISTICS						
Input Frequency						
Single-Ended Mode		10		500	MHz	Doubler disabled
Differential Mode		10		600	MHz	Doubler disabled
Single-Ended or Differential Mode		10		125	MHz	Doubler enabled
Input Sensitivity						
Single-Ended Mode		0.4		AV_{DD}	V p-p	REFP biased at AV_{DD}/2, ac coupling ensures AV_{DD}/2 bias
Differential Mode		0.4		1.8	V p-p	Low voltage differential signal (LVDS) and low voltage positive emitter coupled logic (LVPECL) compatible, REFP and REFN biased at 2.1 V, ac coupling ensures 2.1 V bias
Input Capacitance						
Single-Ended Mode			6.9		pF	
Differential Mode			1.4		pF	
Input Current				±150	µA	Single-ended reference programmed
				300	µA	Differential reference programmed
Phase Detector Frequency				160	MHz	Fractional mode
				250	MHz	Integer mode
CHARGE PUMP						
Charge Pump Current, Sink and Source	I_{CP}					
High Value			5.6		mA	
Low Value			0.35		mA	
Current Matching			3		%	0.5 V ≤ voltage at the CPOUT pin (V_{CP}) ≤ VDD_VP − 0.5 V
I_{CP} vs. V_{CP}			3		%	0.5 V ≤ V_{CP} ≤ VDD_VP − 0.5 V
I_{CP} vs. Temperature			1.5		%	V_{CP} = 2.5 V
LOGIC INPUTS						$\overline{CS}$, SDIO, SCLK, and CE is 3 V logic
Input High Voltage	V_{INH}	1.17			V	
Input Low Voltage	V_{INL}			0.63	V	
Input Current	I_{INH}/I_{INL}			±1	µA	
Input Capacitance	C_{IN}		3.0		pF	
LOGIC OUTPUTS						
Output High Voltage	V_{OH}	AV_{DD} − 0.4			V	3.3 V output selected
		1.5	1.875		V	1.8 V output selected
Output High Current	I_{OH}			500	µA	
Output Low Voltage	V_{OL}			0.4	V	Output low current (I_{OL}) = 500 µA
SYNTHESIZER DIVIDER RANGE						
Reference Divider	R	1		32	Count	
VCO Divider	N	16		32,767	Count	Integer mode prescaler = 4/5
		64		65,535	Count	Integer mode prescaler = 8/9
		23		32,767	Count	Fractional mode prescaler = 4/5
		75		65,535	Count	Fractional mode prescaler = 8/9

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLIES						
Supply Voltage (Except VCO)[1]	AV_{DD}	3.15		3.45	V	VCC_CAL, VCC_X4, VDD_X4, VCC_X1, VDD_X1, VCC_X2, VCC_MUX, VCC_3V, VDD_NDIV, VDD_LS, VCC_LDO_3V, VCC_REF, VDD_PFD, VDD_VP are grouped as AV_{DD}, and are at the same voltage
Supply Current (Except VCO)	AI_{DD}		190	260	mA	All outputs are disabled
Output Dividers						
Divider = 2			14	20	mA	Each divide by 2 will consume additional typical 7 mA current
Divider = 64			50	65	mA	
VCO Supply Voltage	VCC_VCO					
		3.15	3.3	3.45	V	3.3 V condition
		4.75	5	5.25	V	5 V condition
VCO Supply Current	I_{VCO}		80	120	mA	3.3 V condition
			135	200	mA	5 V condition
RF8x Supply Current						RF8P and RF8N output stage is programmable, extra current is drawn in VCC_X1
			25		mA	−4 dBm setting
			39		mA	−1 dBm setting
			52		mA	2 dBm setting
			65		mA	5 dBm setting
RFAUX8x Supply Current			42		mA	−4 dBm setting
			56		mA	−1 dBm setting
			70		mA	2 dBm setting
			84		mA	5 dBm setting
RF16x Supply Current			90	120	mA	
RF32x Supply Current			160	210	mA	
Low Power Sleep Mode			5.1	6.2	mA	Hardware power-down 3.3 V VCO case
			8	9.5	mA	Hardware power-down 5 V VCO case
			21.5	25	mA	Software power-down 3.3 V VCO case
			23.7	28	mA	Software power-down 5 V VCO case
RF OUTPUT CHARACTERISTICS						
VCO Frequency Range		4000		8000	MHz	Fundamental VCO range
RF8P and RF8N Output Frequency		62.5		8000	MHz	
RFAUX8P and RFAUX8N Output Frequency		62.5		8000	MHz	
RF16P and RF16N Output Frequency		8000		16000	MHz	2 × VCO output
RF32P and RF32N Output Frequency		16000		32000	MHz	4 × VCO output
VCO Sensitivity	K_V					
For 5 V			80		MHz/V	VCO frequency = 6 GHz, see Figure 39 for K_V plot
For 3.3 V			60		MHz/V	VCO frequency = 6 GHz, see Figure 40 for K_V plot
Frequency Pushing (Open-Loop)			8		MHz/V	
Frequency Pulling (Open-Loop)			0.5		MHz	Voltage standing wave ratio (VSWR) = 2:1 RF8P and RF8N
			30		MHz	VSWR = 2:1 RF16x
Maintain Lock Temperature Range[2]				125	°C	Maintains lock without reprogramming device

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Harmonic Content						
Second Harmonic RF8P and RF8N			−25		dBc	Fundamental VCO output (RF8P)
			−25		dBc	Divided VCO output (RF8P)
Third Harmonic RF8P and RF8N			−12		dBc	Fundamental VCO output (RF8P)
			−15		dBc	Divided VCO output (RF8P)
Second Harmonic RF16P and RF16N			−30		dBc	Measured at 20 GHz
Third Harmonic RF16P and RF16N			−30		dBc	Measured at 30 GHz
Second Harmonic RF32P and RF32N			−30		dBc	Measured at 40 GHz
Third Harmonic RF32P and RF32N			−30		dBc	Measured at 60 GHz
Fundamental VCO Feedthrough			−62		dBc	RF16x = 10 GHz, VCO frequency = 5 GHz
			−30		dBc	RF8P and RF8N = 1 GHz, VCO frequency = 4 GHz
RF Output Power Maximum Setting[3]			7		dBm	RF8P = 4 GHz, 7.5 nH inductor to VCC_X1
			5		dBm	RF8P = 8 GHz, 7.5 nH inductor to VCC_X1
			0		dBm	RF16x = 8 GHz
			4		dBm	RF16x = 16 GHz
			−1		dBm	RF32x = 16 GHz
			−7		dBm	RF32x = 32 GHz
RF Output Power Variation			±1		dB	RF8P and RF8N = 5 GHz
			±1		dB	RF16x = 10 GHz
			±1		dB	RF32x = 20 GHz
RF Output Power Variation (over Frequency)			±2		dB	RF8x and RFAUX8x = 4 GHz to 8 GHz
			±2.5		dB	RF16x = 8 GHz to 16 GHz
			±5		dB	RF32x = 16 GHz to 32 GHz
Level of Signal with RF Output Disabled			−50		dBm	RF8P and RF8N = 1 GHz
			−44		dBm	RF8P and RF8N = 8 GHz
			−41		dBm	RF8P and RF8N = 8 GHz, 5 V VCO case
			−75		dBm	RF16P = 8 GHz
			−55		dBm	RF16P = 16 GHz
			−85		dBm	RF32P = 16 GHz
			−70		dBm	RF32P = 32 GHz
NOISE CHARACTERISTICS						
Fundamental VCO Phase Noise Performance Where VCC VCO = 5 V						VCO noise in open-loop conditions, VCC_VCO = 5 V
			−117		dBc/Hz	100 kHz offset from 4.0 GHz carrier
			−139		dBc/Hz	1 MHz offset from 4.0 GHz carrier
			−156		dBc/Hz	10 MHz offset from 4.0 GHz carrier
			−112		dBc/Hz	100 kHz offset from 5.7 GHz carrier
			−136		dBc/Hz	1 MHz offset from 5.7 GHz carrier
			−153		dBc/Hz	10 MHz offset from 5.7 GHz carrier
			−109		dBc/Hz	100 kHz offset from 8.0 GHz carrier
			−133		dBc/Hz	1 MHz offset from 8.0 GHz carrier
			−152		dBc/Hz	10 MHz offset from 8.0 GHz carrier
RF16x Output Phase Noise Performance Where VCC_VCO = 5 V						VCC_VCO = 5 V
			−106		dBc/Hz	100 kHz offset from 11.4 GHz carrier
			−130		dBc/Hz	1 MHz offset from 11.4 GHz carrier
			−146		dBc/Hz	10 MHz offset from 11.4 GHz carrier

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
			−103		dBc/Hz	100 kHz offset from 16 GHz carrier
			−127		dBc/Hz	1 MHz offset from 16 GHz carrier
			−145		dBc/Hz	10 MHz offset from 16 GHz carrier
RF32x Output Phase Noise Performance Where VCC_VCO = 5 V						VCC_VCO = 5 V
			−100		dBc/Hz	100 kHz offset from 24 GHz carrier
			−123		dBc/Hz	1 MHz offset from 24 GHz carrier
			−140		dBc/Hz	10 MHz offset from 24 GHz carrier
			−97		dBc/Hz	100 kHz offset from 32 GHz carrier
			−121		dBc/Hz	1 MHz offset from 32 GHz carrier
			−137		dBc/Hz	10 MHz offset from 32 GHz carrier
Fundamental VCO Phase Noise Performance Where VCC_VCO = 3.3 V						VCO noise in open-loop conditions, VCC_VCO = 3.3 V
			−116		dBc/Hz	100 kHz offset from 4.0 GHz carrier
			−137		dBc/Hz	1 MHz offset from 4.0 GHz carrier
			−156		dBc/Hz	10 MHz offset from 4.0 GHz carrier
			−111		dBc/Hz	100 kHz offset from 5.7 GHz carrier
			−133		dBc/Hz	1 MHz offset from 5.7 GHz carrier
			−153		dBc/Hz	10 MHz offset from 5.7 GHz carrier
			−109		dBc/Hz	100 kHz offset from 8.0 GHz carrier
			−132		dBc/Hz	1 MHz offset from 8.0 GHz carrier
			−153		dBc/Hz	10 MHz offset from 8.0 GHz carrier
Normalized Inband Phase Noise Floor						
Fractional Channel[4]			−233		dBc/Hz	
Integer Channel[5]			−234		dBc/Hz	
Normalized 1/f Noise[6]	PN1_f		−127		dBc/Hz	10 kHz offset; normalized to 1 GHz
Integrated RMS Jitter			38		fs	Wenzel oven controlled crystal oscillators (OCXO) as the reference frequency input (REF_{IN}), integer-N mode, phase frequency detector (PFD) = 245.76 MHz, 300 kHz loop filter bandwidth, 1 kHz to 100 MHz
Integer Boundary Spurs (Filtered)			−90		dBc	960 kHz offset from integer channel
Inband Integer Boundary Spur (Unfiltered)			−55		dBc	Measured at 5 kHz offset from integer channel
Spurious Signals Due to PFD Frequency			−90		dBc	
FREQUENCY LOCK TIME[7]						
Lock Time with Automatic Calibration			3		ms	
Lock Time with Automatic Calibration Bypassed			30		µs	

[1] T_A = 25°C, AV_{DD} = 3.3 V, VCC_VCO = 5.0 V, prescaler = 4/5, reference frequency (f_{REFP}) = 50 MHz, PFD frequency (f_{PFD}) = 50 MHz, and RF frequency (f_{RF}) = 5001 MHz. RF8x enabled. All RF outputs are disabled.
[2] Guaranteed by design and characterization.
[3] RF output power using the EV-ADF4371SD2Z evaluation board differential outputs combined using a Marki BAL-0036 balun, and measured by a spectrum analyzer with the evaluation board and cable losses de-embedded. Highest power output selected for RF8P, RF8N, RFAUX8P, and RFAUX8N.
[4] Use this value to calculate the phase noise for any application. To calculate inband phase noise performance as seen at the VCO output, use the following formula: −233 + 10log(f_{PFD}) + 20logN. The value given is the lowest noise mode for the fractional channel.
[5] Use this value to calculate the phase noise for any application. To calculate inband phase noise performance as seen at the VCO output, use the following formula: −234 + 10log(f_{PFD}) + 20logN. The value given is the lowest noise mode for the integer channel.
[6] The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at RF; (f_{RF}) and at a frequency offset (f) is given by PN1_f + 10log(10 kHz/f) + 20log(f_{RF}/1 GHz). Both the normalized phase noise floor and flicker noise are modeled in the ADIsimPLL design tool.
[7] Lock time is measured for 100 MHz jump with standard evaluation board configuration.

TIMING SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Serial Port Interface (SPI) Timing		See Figure 2, Figure 3, and Figure 4				
SCLK Frequency	f_{SCLK}				50	MHz
SCLK Period	t_{SCLK}		20			ns
SCLK Pulse Width High	t_{HIGH}		10			ns
SCLK Pulse Width Low	t_{LOW}		10			ns
SDIO Setup Time	t_{DS}		2			ns
SDIO Hold Time	t_{DH}		2			ns
SCLK Falling Edge to SDIO Valid Propagation Delay	t_{ACCESS}		10			ns
$\overline{CS}$ Rising Edge to SDIO High-Z	t_Z		10			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_S		2			ns
SCLK Fall to $\overline{CS}$ Rise Hold Time	t_H		2			ns

Timing Diagrams

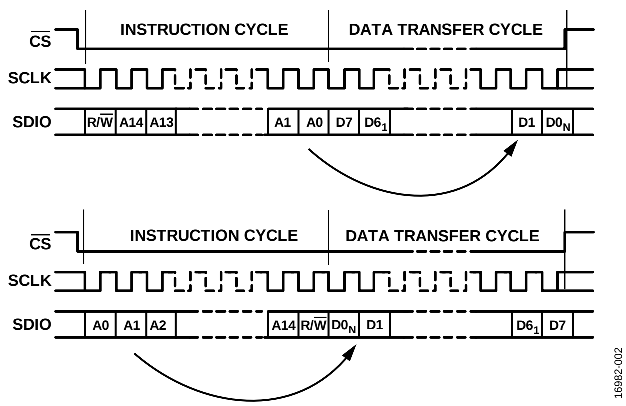


Figure 2. SPI Timing, MSB First (Upper) and LSB First (Lower)

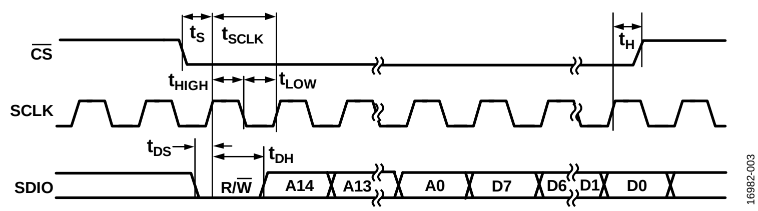


Figure 3. SPI Write Operation Timing

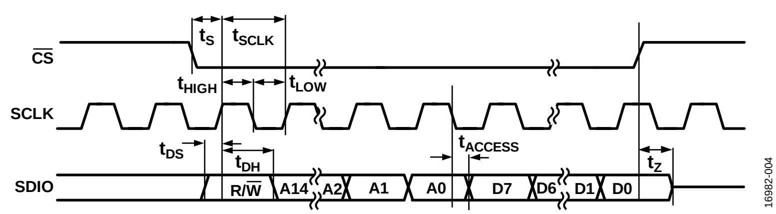


Figure 4. SPI Read Operation Timing

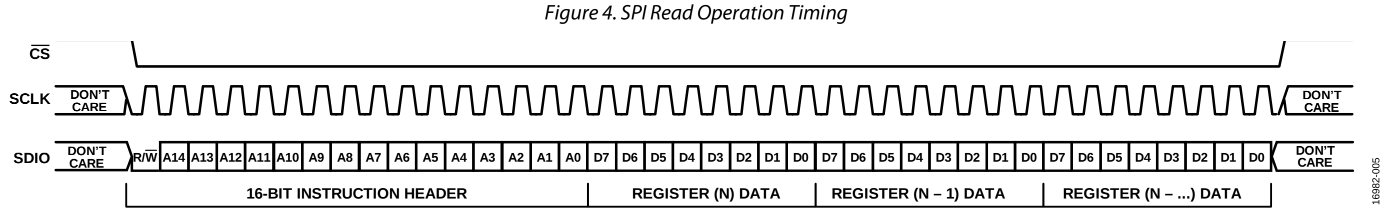


Figure 5. 3-Wire, MSB First, Descending Data, Streaming

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} Rails to GND[1]	−0.3 V to +3.6 V
AV_{DD} Rails to Each Other	−0.3 V to +0.3 V
VCC_VCO to GND[1]	−0.3 V to +5.5 V
VCC_VCO to AV_{DD}	−0.3 V to AV_{DD} + 2.8 V
CPOUT to GND[1]	−0.3 V to AV_{DD} + 0.3 V
VTUNE to GND	−0.3 V to AV_{DD} + 0.3 V
Digital Input and Output Voltage to GND[1]	−0.3 V to AV_{DD} + 0.3 V
Analog Input and Output Voltage to GND[1]	−0.3 V to AV_{DD} + 0.3 V
REFP and REFN to GND[1]	−0.3 V to AV_{DD} + 0.3 V
REFP to REFN	±2.1 V
Temperature	
Operating Range	−40°C to +105°C
Storage Range	−65°C to +125°C
Maximum Junction	125 °C
Reflow Soldering	
Peak	260°C
Time at Peak	30 sec
Transistor Count	
Complementary Metal-Oxide Semiconductor (CMOS)	131439
Bipolar	4063

[1] GND = 0 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance top and bottom.

Table 4. Thermal Resistance

Package Type	θ_{JA}	$\theta_{JC\text{-}TOP}$	$\theta_{JC\text{-}BOTTOM}$	Unit
CC-48-4[1]	25	14.4	3.7	°C/W

[1] Test Condition 1: thermal impedance simulated values are based on JESD-51 standard.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

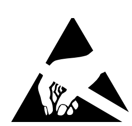
Charged devices model per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADA4371

Table 5. ADA4371, 48-Terminal LGA

ESD Model	Withstand Threshold	Class
HBM, All Pins	4.0 kV	3A
CDM		
RF32P and RF32N	500 V	C2A
All Other Pins	750 V	C2B

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

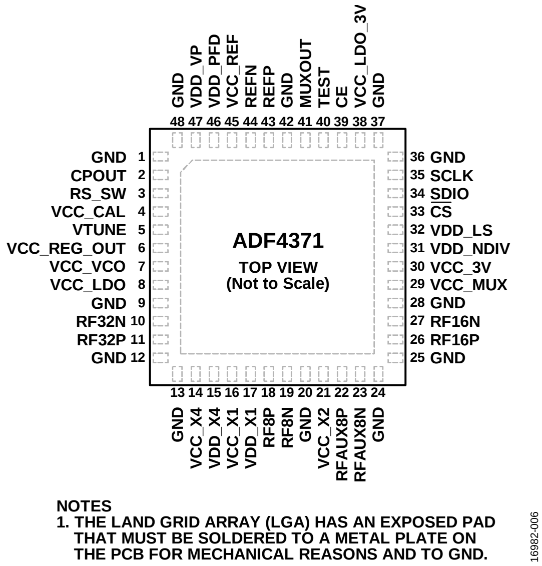


Figure 6. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 9, 12, 13, 20, 24, 25, 28, 36, 37, 42, 48	GND	Ground Return.
2	CPOUT	Charge Pump Output. When enabled, this output provides $\pm I_{CP}$ to the external loop filter. The output of the loop filter is connected to VTUNE to drive the internal VCO.
3	RS_SW	Factory Test Pin. Leave floating.
4	VCC_CAL	Power Supply for Internal Calibration Monitor Circuit. The voltage on this pin ranges from 3.15 V to 3.45 V. VCC_CAL must have the same value as AV_{DD}, nominally 3.3 V.
5	VTUNE	Control Input to the VCO. This voltage determines the output frequency and is derived from filtering the CPOUT output voltage.
6	VCC_REG_OUT	VCO Supply Regulator Out. The output supply voltage of the VCO regulator is available at this pin, and must be decoupled to GND with a 10 µF capacitor and shorted to the VCC_VCO pin. Leave this pin open if an external LDO regulator is connected to VCC_VCO.
7	VCC_VCO	Power Supply for the VCO. The voltage on this pin ranges from 4.75 V to 5.25 V. Place decoupling capacitors to the analog ground plane as close to this pin as possible. For optimal performance, this supply must be clean and have low noise.
8	VCC_LDO	Supply Pin to the VCO Regulator. If the internal regulator is used, connect the voltage supply to VCC_LDO. The voltage on this pin ranges from 4.75 V to 5.25 V. If the external regulator is used, short this pin to VCC_VCO.
10	RF32N	Quadrupler Output. AC or dc couple this pin to the next stage. This pin can be powered off when not in use. If unused, this pin can be left open.
11	RF32P	Complementary Quadrupler Output. AC or dc couple this pin to the next stage. This pin can be powered off when not in use. If unused, this pin can be left open.
14	VCC_X4	Power Supply for the Quadrupler RF Output. The voltage on this pin must have the same value as AV_{DD}.
15	VDD_X4	Digital Supply for the Quadrupler Circuit. The voltage on this pin must have the same value as AV_{DD}.
16	VCC_X1	Power Supply for the Main RF Output. The voltage on this pin must have the same value as AV_{DD}.
17	VDD_X1	Digital Supply for the Main RF Circuit. The voltage on this pin must have the same value as AV_{DD}.
18	RF8P	Main RF Output. AC couple to the next stage. The output level is programmable. The VCO fundamental output or a divided down version is available. This pin can be powered off when not in use. If unused, this pin can be left open.

Pin No.	Mnemonic	Description
19	RF8N	Complementary Main RF Output. AC couple this pin to the next stage. The output level is programmable. The VCO fundamental output or a divided down version is available. This pin can be powered off when not in use. If unused, this pin can be left open.
21	VCC_X2	Power Supply for the Doubled RF Output. The voltage on this pin must have the same value as AV_{DD}.
22	RFAUX8P	Auxiliary RF Output. AC couple to the next stage. This pin can be powered off when not in use. If unused, this pin can be left open.
23	RFAUX8N	Complementary Auxiliary RF Output. AC couple this pin to the next stage. This pin can be powered off when not in use. If unused, this pin can be left open.
26	RF16P	Doubled VCO Output. AC or dc couple this pin to the next stage. This pin can be powered off when not in use. If unused, this pin can be left open.
27	RF16N	Complementary Doubled VCO Output. AC or dc couple this pin to the next stage. This pin can be powered off when not in use. If unused, this pin can be left open.
29	VCC_MUX	Power Supply for the VCO Mux. The voltage on this pin must have the same value as AV_{DD}.
30	VCC_3V	Analog Power Supply. The voltage on this pin must have the same value as AV_{DD}.
31	VDD_NDIV	N Divider Power Supply. The voltage on this pin must have the same value as AV_{DD}.
32	VDD_LS	Level Shifter Power Supply. The voltage on this pin must have the same value as AV_{DD}.
33	$\overline{CS}$	Chip Select, CMOS Input. When $\overline{CS}$ goes high, the data stored in the shift register is loaded into the register that is selected by the address bits.
34	SDIO	Serial Data Input Output. This input is a high impedance CMOS input.
35	SCLK	Serial Clock Input. Data is clocked into the 24-bit shift register on the clock rising (or falling) edge. This input is a high impedance CMOS input.
38	VCC_LDO_3V	Regulator Input for 1.8 V Digital Logic. The voltage on this pin must have the same value as AV_{DD}.
39	CE	Chip Enable. Connect to 3.3 V or AV_{DD}.
40	TEST	Factory Test Pin. Connect this pin to ground.
41	MUXOUT	Mux Output. The mux output allows the digital lock detect, the analog lock detect, scaled RF, or the scaled reference frequency to be externally accessible. This pin can be programmed to output the register settings in 4-wire SPI mode.
43	REFP	Reference Input. If driving the device with a single-ended reference, ac couple the signal to the REFP pin.
44	REFN	Complementary Reference Input. If unused, ac couple this pin to GND. REFP and REFN must be ac-coupled if driven differentially. If driven single-ended, the reference signal must be connected to REFP, and the REFN must be ac-coupled to GND. In differential configuration, the differential impedance is 100 Ω.
45	VCC_REF	Power Supply to the Reference Buffer. The voltage on this pin must have the same value as AV_{DD}.
46	VDD_PFD	Power Supply to the PFD. The voltage on this pin must have the same value as AV_{DD}.
47	VDD_VP	Charge Pump Power Supply. The voltage on this pin must have the same value as AV_{DD}. A 1 µF decoupling capacitor to GND must be included to minimize spurious signals.
	EP	Exposed Pad. The land grid array (LGA) has an exposed pad that must be soldered to a metal plate on the PCB for mechanical reasons and to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

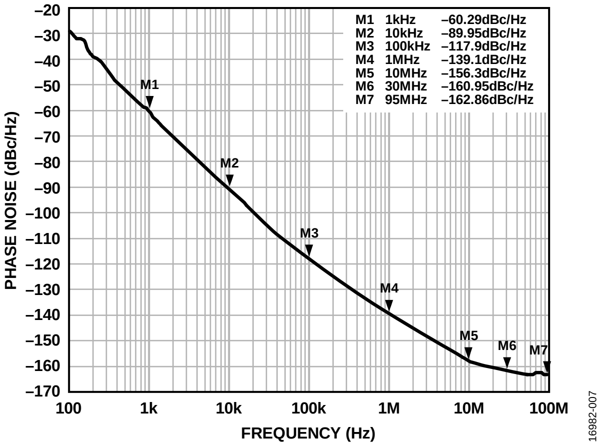


Figure 7. Open-Loop VCO Phase Noise, 4.0 GHz, VCC_VCO = 5 V

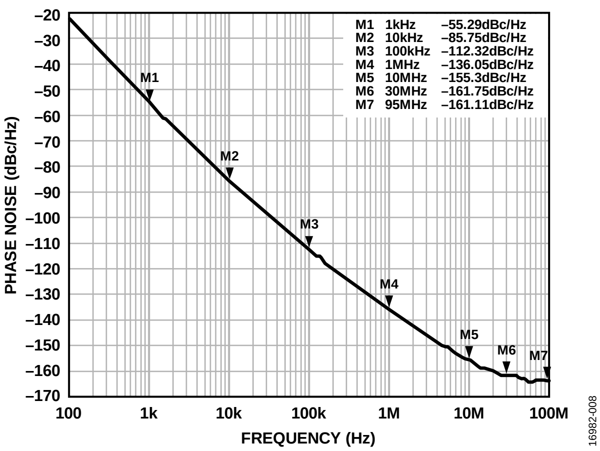


Figure 8. Open-Loop VCO Phase Noise, 5.7 GHz, VCC_VCO = 5 V

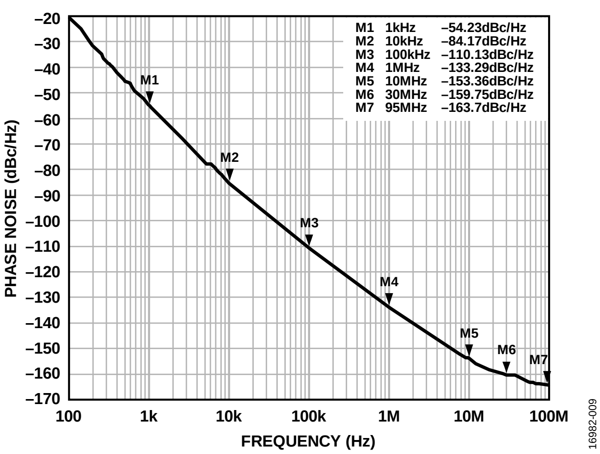


Figure 9. Open-Loop VCO Phase Noise, 8.0 GHz, VCC_VCO = 5 V

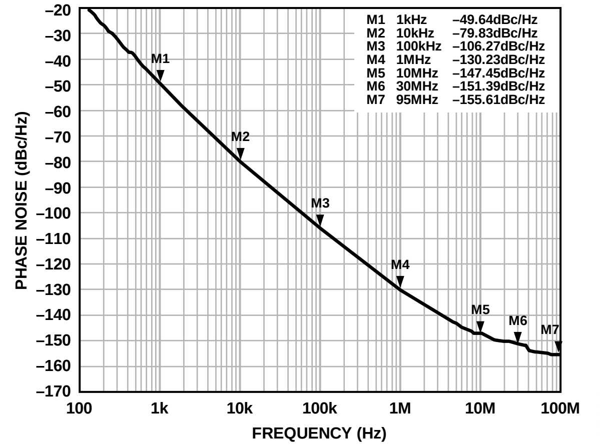


Figure 10. Open-Loop VCO Phase Noise at RF16x Output, 11.4 GHz, VCC_VCO = 5 V

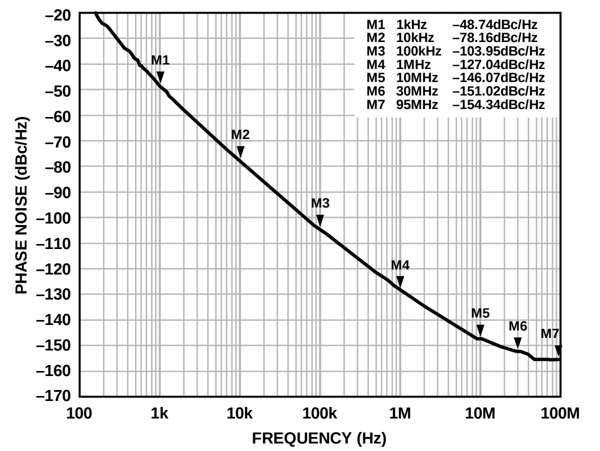


Figure 11. Open-Loop VCO Phase Noise at RF16x Output, 16.0 GHz, VCC_VCO = 5 V

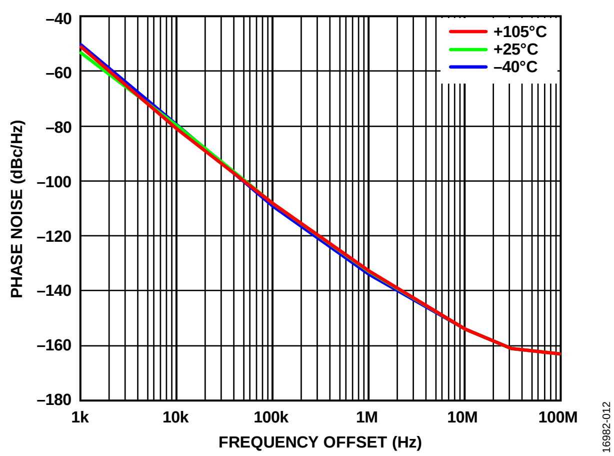


Figure 12. Open-Loop VCO Phase Noise over Temperature, 8.0 GHz, VCC_VCO = 5 V

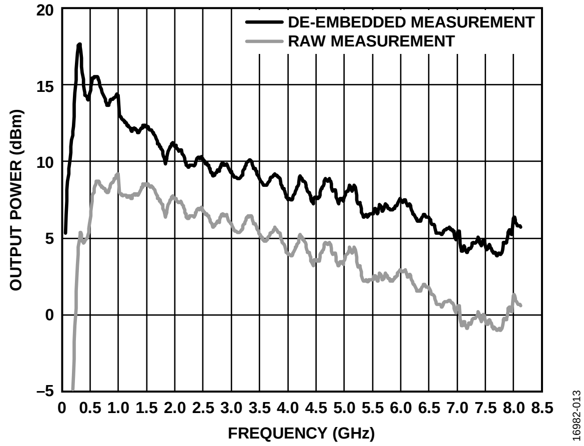


Figure 13. RF8P and RF8N Output Power, De-Embedded Board and Cable Measurement, Combined Using Balun (7.4 nH Inductors, 10 pF AC Coupling Capacitors Limit Power at Low Frequencies)

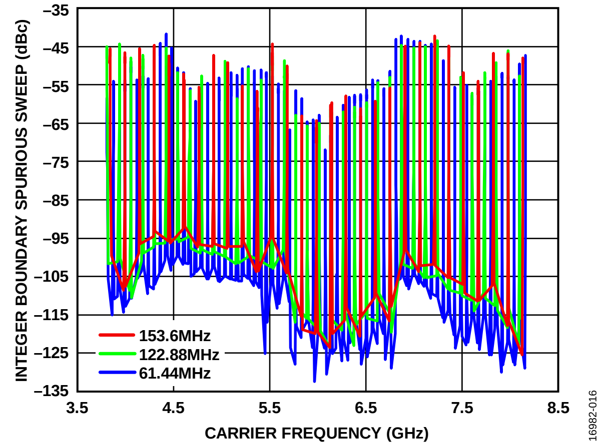


Figure 16. Integer Boundary Spurious Sweep vs. Carrier Frequency, PFD Frequencies = 61.44 MHz, 122.88 MHz, and 153.6 MHz, Loop Filter Bandwidth = 100 kHz

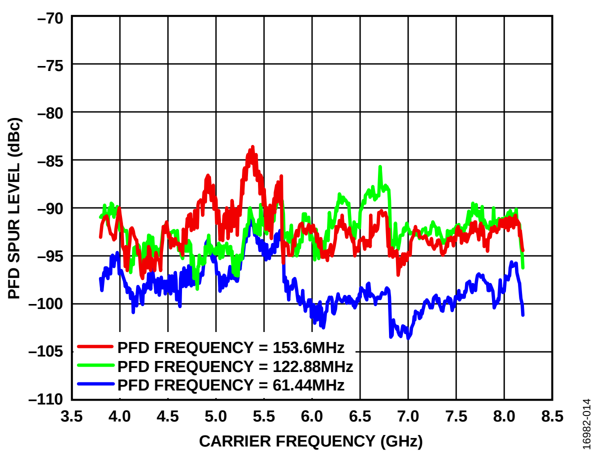


Figure 14. PFD Spurious Sweep, PFD Frequency = 61.44 MHz, Loop Filter Bandwidth = 100 kHz

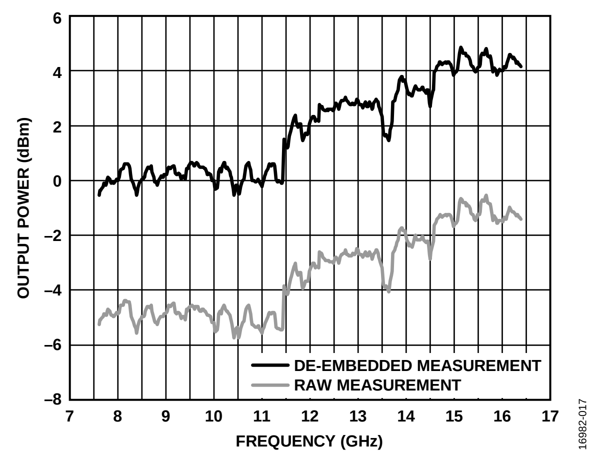


Figure 17. RF16P and RF16N Output Power, De-Embedded Board and Cable Measurement, Combined Using Balun

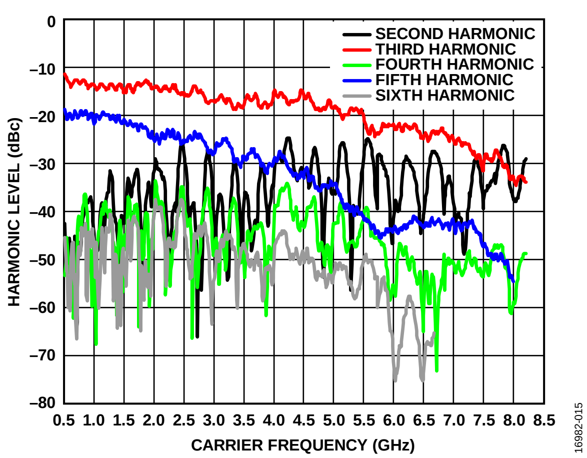


Figure 15. RF8P and RF8N Output Harmonics, De-Embedded Board and Cable Measurement, Combined Using Balun

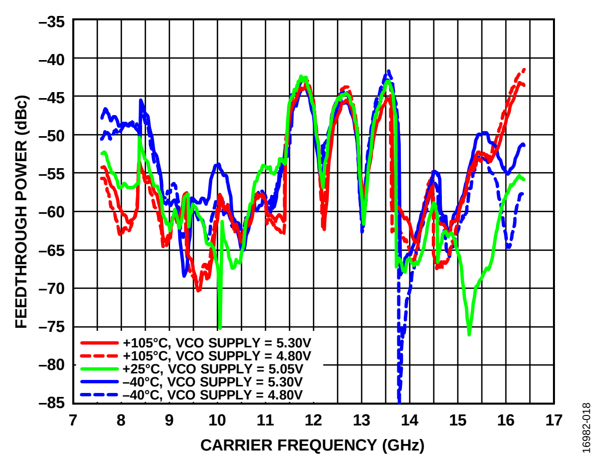


Figure 18. RF16P and RF16N VCO Feedthrough, De-Embedded Board and Cable Measurement, Combined Using Balun

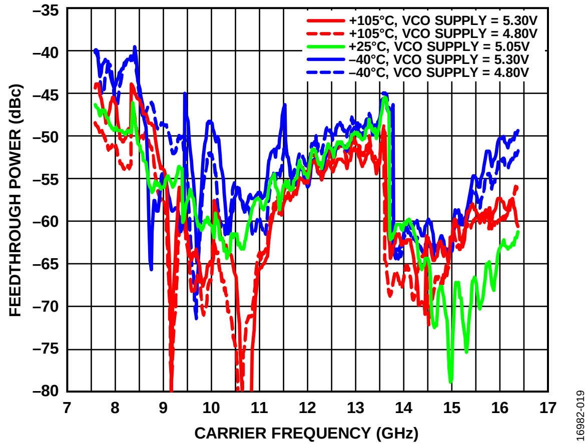


Figure 19. RF16P and RF16N VCO × 3 Feedthrough, De-Embedded Board and Cable Measurement, Combined Using Balun

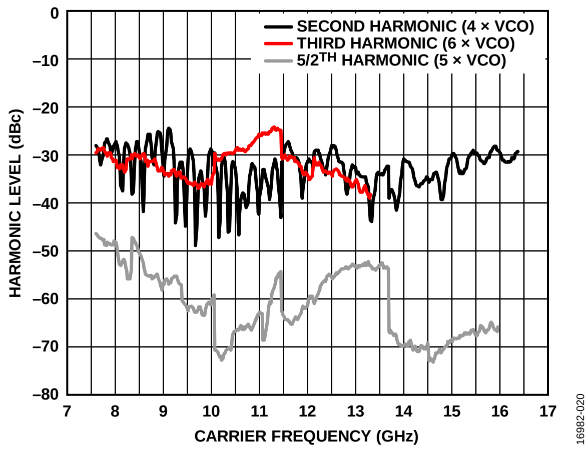


Figure 20. RF16P and RF16N Output Harmonics, De-Embedded Board and Cable Measurement, Combined Using Balun

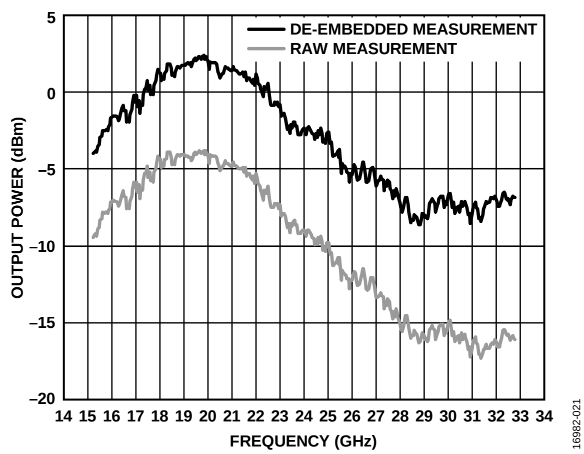


Figure 21. RF 32P and RF32N Output Power, De-Embedded Board and Cable Measurement, Combined Using Balun

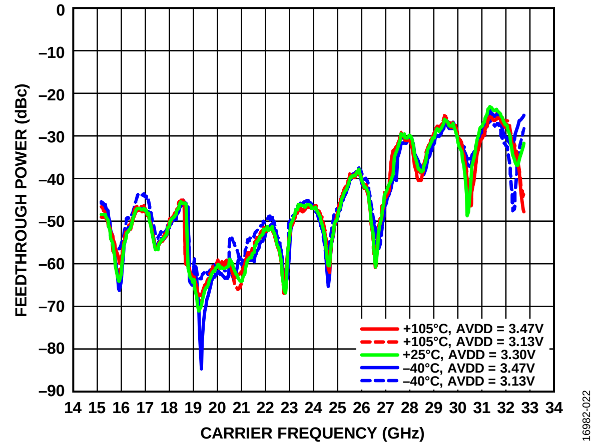


Figure 22. RF32P and RF32N VCO Feedthrough, De-Embedded Board and Cable Measurement, Combined Using Balun

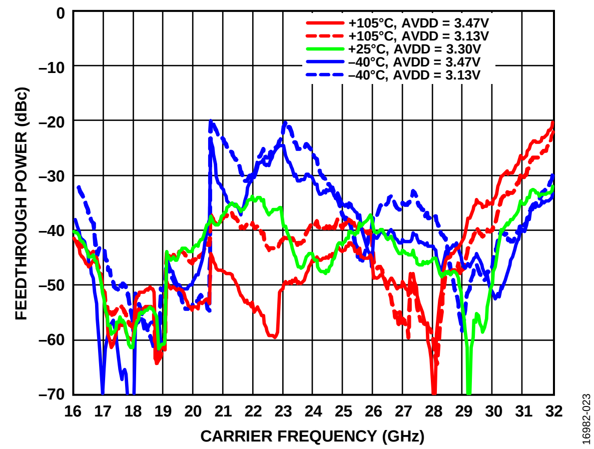


Figure 23. RF32P and RF32N VCO × 2 Feedthrough, De-Embedded Board and Cable Measurement, Combined Using Balun

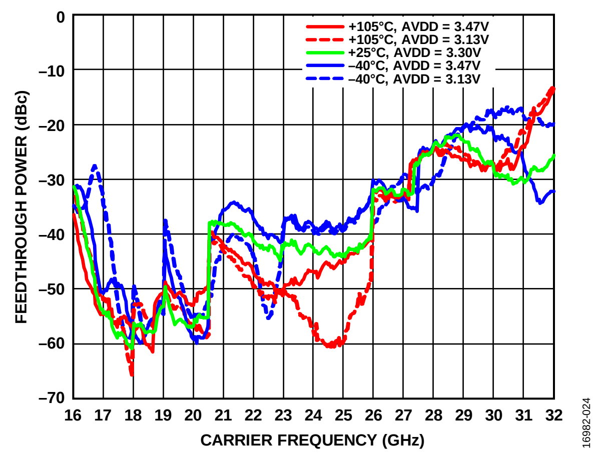


Figure 24. RF32P and RF32N VCO × 3 Feedthrough, De-Embedded Board and Cable Measurement, Combined Using Balun

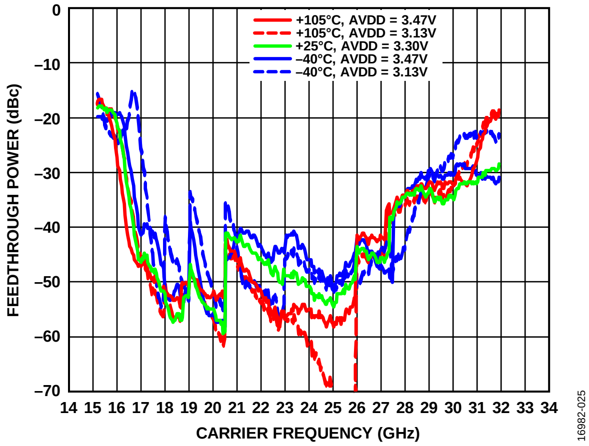


Figure 25. RF32P and RF32N VCO × 5 Feedthrough, De-Embedded Board and Cable Measurement, Combined Using Balun

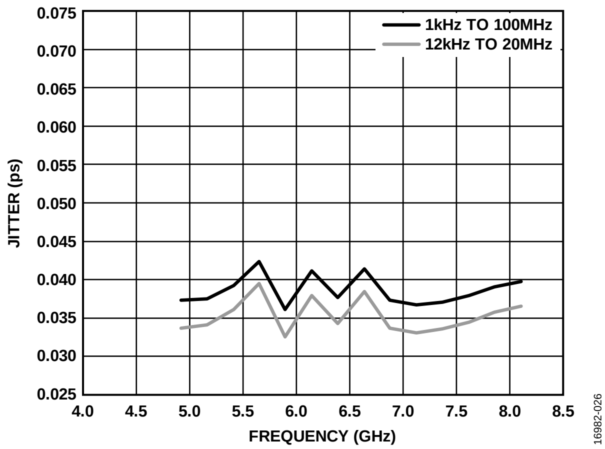


Figure 26. RMS Jitter, Integer N, PFD Frequency (f_{PFD}) = 245.76 MHz, Loop Filter Bandwidth = 220 kHz, VCC_VCO = 5 V

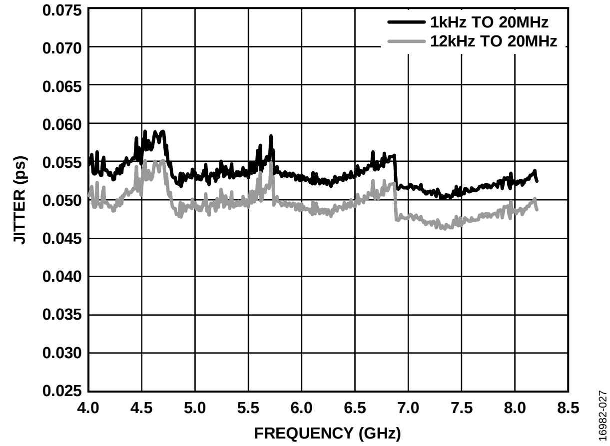


Figure 27. RMS Jitter, Fractional-N, f_{PFD} = 153.6 MHz, VCC_VCO = 5 V

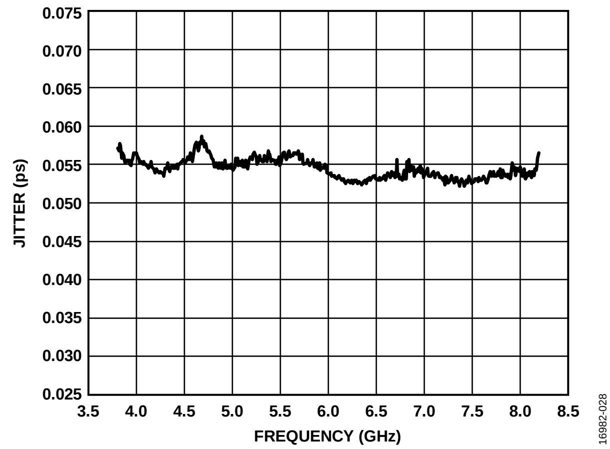


Figure 28. RMS Jitter Integrated from 1 kHz to 100 MHz, Fractional-N, f_{PFD} = 153.6 MHz, VCC_VCO = 3.3 V

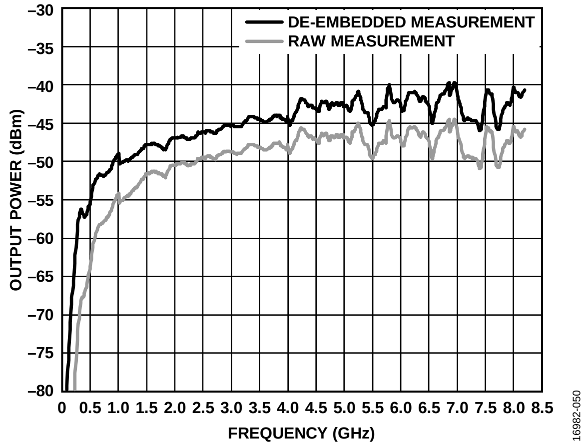


Figure 29. RF8P and RF8N Output Power When Disabled, De-Embedded Board and Cable Measurement, Combined Using Balun

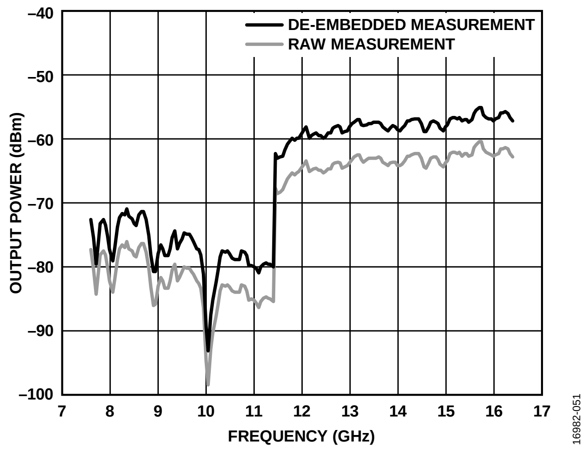


Figure 30. RF16P and RF16N Output Power When Disabled, De-Embedded Board and Cable Measurement, Combined Using Balun

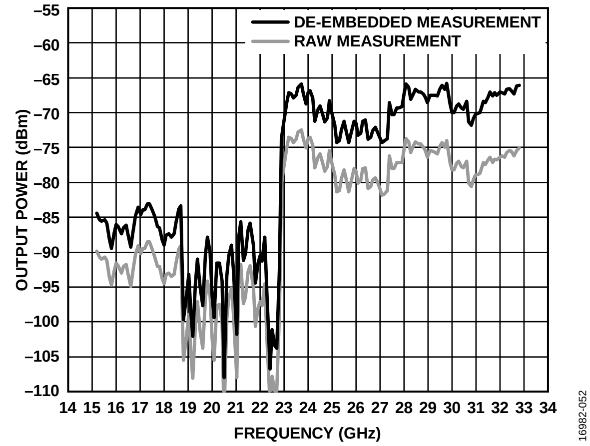


Figure 31. RF 32P and RF32N Output Power When Disabled, De-Embedded Board and Cable Measurement, Combined Using Balun

THEORY OF OPERATION

RF SYNTHESIZER, A WORKED EXAMPLE

Use the following equations to program the ADF4371 synthesizer:

$$f_{RFOUT} = \left(INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1} \right) \times \frac{f_{PFD}}{RF\ Divider} \quad (1)$$

where:
f_{RFOUT} is the RF output frequency.
INT is the integer division factor.
FRAC1 is the fractionality.
FRAC2 is the auxiliary fractionality.
MOD1 is the fixed 25-bit modulus.
MOD2 is the auxiliary modulus.
RF Divider is the output divider that divides down the VCO frequency.

$$f_{PFD} = REF_{IN} \times ((1 + D)/(R \times (1 + T))) \quad (2)$$

where:
REF_{IN} is the reference frequency input.
D is the REF_{IN} doubler bit.
R is the reference division factor.
T is the reference divide by 2 bit (0 or 1).

For example, in a universal mobile telecommunication system (UMTS) where a 2112.8 MHz f_{RFOUT} is required, a 122.88 MHz REF_{IN} is available. The ADF4371 VCO operates in the frequency range of 4 GHz to 8 GHz. Therefore, the RF divider of 2 must be used (VCO frequency = 4225.6 MHz, f_{RFOUT} = VCO frequency/RF divider = 4225.6 MHz/2 = 2112.8 MHz).

The feedback path is also important. In this example, the VCO output is fed back before the output divider (see Figure 32).

In this example, the 122.88 MHz reference signal is divided by 2 to generate a f_{PFD} of 61.44 MHz. The desired channel spacing is 200 kHz.

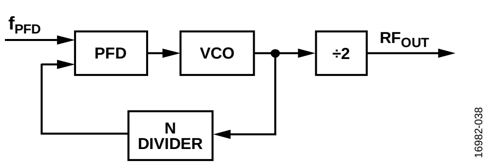


Figure 32. Loop Closed Before Output Divider

The values used in this worked example are as follows:

$$N = f_{VCO\_OUT}/f_{PFD} = 4225.6\text{ MHz}/61.44\text{ MHz} = 68.7760416666666667 \quad (3)$$

where:
N is the desired value of the feedback counter, N.
f_{VCO_OUT} is the output frequency of the VCO voltage controlled oscillator without using the output divider.
f_{PFD} is the frequency of the phase frequency detector.

$$INT = INT(VCO\ frequency/f_{PFD}) = 68 \quad (4)$$

$$FRAC = 0.7760416666666667 \quad (5)$$

where:
FRAC is the fractional part of the N.

$$MOD1 = 33{,}554{,}432 \quad (6)$$

$$FRAC1 = INT(MOD1 \times FRAC) = 26{,}039{,}637 \quad (7)$$

$$\text{Remainder} = 0.3333333333 \text{ or } 1/3 \quad (8)$$

$$MOD2 = f_{PFD}/GCD(f_{PFD}, f_{CHSP}) = 61.44\text{ MHz}/\text{GCD}(61.44\text{ MHz}, 200\text{ kHz}) = 1536 \quad (9)$$

where:
GCD is the greatest common divider operant.

$$FRAC2 = \text{Remainder} \times 1536 = 512 \quad (10)$$

From Equation 2,

$$f_{PFD} = (122.88\text{ MHz} \times (1 + 0)/2) = 61.44\text{ MHz} \quad (11)$$

$$2112.8\text{ MHz} = 61.44\text{ MHz} \times ((INT + (FRAC1 + FRAC2/MOD2)/2^{25}))/2 \quad (12)$$

where:
INT = 68.
FRAC1 = 26,039,637.
MOD2 = 1536.
FRAC2 = 512.
RF Divider = 2.

REFERENCE INPUT SENSITIVITY

The slew rate of the input reference signal significantly affects the performance. The device is functional with signals of very low amplitude down to 0.4 V p-p and with a slew rate of 21 V/μs. However, the optimal performance is achieved with slew rates as high as 1000 V/μs. Achieving this slew rate with sinusoidal waves requires high amplitudes and may not be possible at low frequencies. The jitter and phase noise performance of the ADF4371 is shown in Figure 33 and Figure 34 for PFD frequencies of 250 MHz and 100 MHz, respectively. A high performance square wave signal with a high slew rate is recommended as the reference input signal to achieve the best performance.

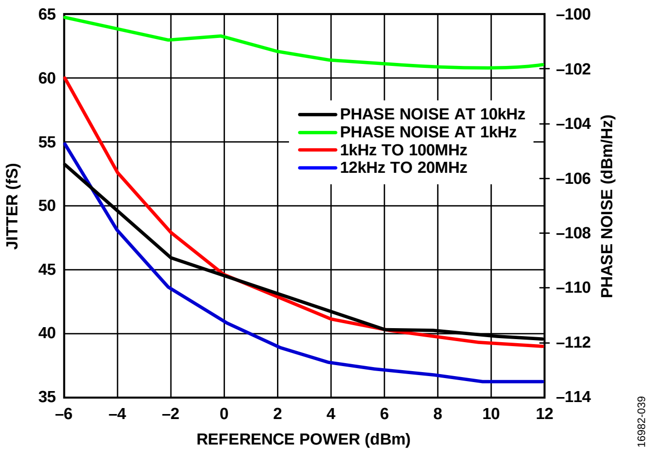


Figure 33. Jitter and Phase Noise, f_{PFD} = 250 MHz

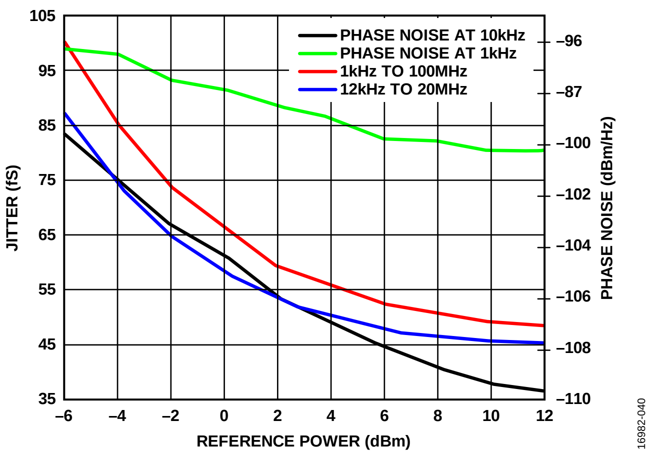


Figure 34. Jitter and Phase Noise, f_{PFD} = 100 MHz

REFERENCE DOUBLER AND REFERENCE DIVIDER

The on-chip reference doubler allows the input reference signal to be doubled. The doubler is useful for increasing the PFD comparison frequency. To improve the noise performance of the system, increase the PFD frequency. Doubling the PFD frequency typically improves noise performance by 3 dB.

The reference divide by 2 divides the reference signal by 2, resulting in a 50% duty cycle PFD frequency.

SPURIOUS OPTIMIZATION AND FAST LOCK

Narrow loop bandwidths can filter unwanted spurious signals. However, these bandwidths typically have a long lock time. A wider loop bandwidth achieves faster lock times, but can lead to increased spurious signals inside the loop bandwidth.

OPTIMIZING JITTER

For lowest jitter applications, use the highest possible PFD frequency to minimize the contribution of inband noise from the PLL. Set the PLL filter bandwidth such that the inband noise of the PLL intersects with the open-loop noise of the VCO, minimizing the contribution of both to the overall noise.

Use the ADIsimPLL design tool for this task.

Additional Optimization on Loop Filter

The PLL filter is designed to find an optimum bandwidth for the reference, PFD, and VCO noise, depending on the system requirements. In addition to this design, when the Σ-Δ modulator (SDM) is enabled, further optimization may be necessary to filter SDM noise.

Reducing Sigma Delta Modulator Noise

In fractional mode, SDM noise becomes apparent and starts to contribute to overall phase noise. This noise can be reduced to insignificant levels by using a series resistor between the CPOUT pin and the loop filter. Place this resistor close to the CPOUT pin. A reasonable resistor value does not affect the loop bandwidth and phase margin of the designed loop filter. In most cases, 91 Ω gives the best results. This resistor is not required in integer mode (SDM not enabled) or when a narrow-band loop filter is used (SDM noise attenuated).

SPUR MECHANISMS

This section describes the two different spur mechanisms that arise with a fractional-N synthesizer and how to minimize them in the ADF4371.

Integer Boundary Spurs

One mechanism for fractional spur creation is the interactions between the RF VCO frequency and the reference frequency. When these frequencies are not integer related (which is the purpose of a fractional-N synthesizer), spur sidebands appear on the VCO output spectrum at an offset frequency that corresponds to the beat note or the difference in frequency between an integer multiple of the reference and the VCO frequency. These spurs are attenuated by the loop filter and are more noticeable on channels close to integer multiples of the reference where the difference frequency can be inside the loop bandwidth.

Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers because the reference offset is far outside the loop bandwidth. However, any reference feedthrough mechanism that bypasses the loop can cause a problem. Feedthrough of low levels of on-chip reference switching noise through the prescaler back to the VCO can result in reference spur levels as high as −100 dBc.

LOCK TIME

The PLL lock time divides into a number of settings. The total lock time for changing frequencies is the sum of the four separate times: synthesizer lock, VCO band selection, automatic level calibration (ALC), and PLL settling time.

Synthesizer Lock

The synthesizer lock timeout ensures that the VCO calibration DAC, which forces the VCO tune voltage (V_{TUNE}), has settled to a steady value for the band select circuitry. SYNTH_LOCK_TIMEOUT and TIMEOUT select the length of time the DAC is allowed to settle to the final voltage before the VCO calibration process continues to the next phase (VCO band selection).

The PFD frequency is the clock for this logic, and the duration is set using the following equation:

$$\frac{SYNTH\_LOCK\_TIMEEOUT \times 1024 + TIMEOUT}{f_{PFD}} \quad (13)$$

where:
SYNTH_LOCK_TIMEOUT is programmed in REG0033.
TIMEOUT is programmed in REG0031 and REG0032.

The calculated time must be greater than or equal to 20 µs.

For the SYNTH_LOCK_TIMEOUT bit, the minimum value is 2 and the maximum value is 31. For Timeout, the minimum value is 2 and the maximum value is 1023.

VCO Band Selection

VCO_BAND_DIV (programmed in REG0030) and PFD frequency are used to generate the VCO band selection clock as follows:

$$f_{BSC} = \frac{f_{PFD}}{VCO\_BAND\_DIV} \quad (14)$$

The calculated time must be less than 2.4 MHz.

16 clock cycles are required for one VCO core and band calibration step and the total band selection process takes 11 steps, resulting in the following equation:

$$11 \times \frac{16 \times VCO\_BAND\_DIV}{f_{PFD}} \quad (15)$$

The minimum value for VCO_BAND_DIV is 1 and the maximum value is 255.

Automatic Level Calibration (ALC)

Use the ALC function to choose the correct bias current in the ADF4371 VCO core. The duration required for VCO bias voltage to settle for each step. This duration is set by the following equation:

$$\frac{VCO\_ALC\_TIMEOUT \times 1024 + TIMEOUT}{f_{PFD}} \quad (16)$$

where
VCO_ALC_TIMEOUT and *Timeout* are programmed in REG0034, REG0032, and REG0031.

The calculated time must be greater than or equal to 50 µs.

The total ALC takes 63 steps:

$$63 \times \frac{VCO\_ALC\_TIMEOUT \times 1024 + TIMEOUT}{f_{PFD}} \quad (17)$$

The minimum value for VCO_ALC_TIMEOUT is 2 and the maximum value is 31.

PLL Settling Time

The time taken for the loop to settle is inversely proportional to the low-pass filter bandwidth. The settling time is accurately modeled in the ADIsimPLL design tool.

Lock Time, a Worked Example

Assume that f_{PFD} = 61.44 MHz,

$$VCO\_BAND\_DIV = \text{Ceiling}(f_{PFD}/2{,}400{,}000) = 26 \quad (18)$$

where Ceiling*()* rounds up to the nearest integer.

$$SYNTH\_LOCK\_TIMEOUT \times 1024 + TIMEOUT > 1228.8 \quad (19)$$

$$VCO\_ALC\_TIMEOUT \times 1024 + TIMEOUT > 3072 \quad (20)$$

There are several suitable values that meet these criteria. By considering the minimum specifications, the following values are the most suitable:

- SYNTH_LOCK_TIMEOUT = 2 (minimum value)
- VCO_ALC_TIMEOUT = 3
- TIMEOUT = 2

Much faster lock times than those detailed in this data sheet are possible by bypassing the calibration processes. Contact Analog Devices, Inc., for more information.

CIRCUIT DESCRIPTION

REFERENCE INPUT

Figure 35 shows the reference input stage. The reference input can accept both single-ended and differential signals. Use the reference mode bit (Bit 6 in REG0022) to select the signal. To use a differential signal on the reference input, program this bit high. In this case, SW1 and SW2 are open, SW3 and SW4 are closed, and the current source that drives the differential pair of transistors switches on. The differential signal is buffered, and it is provided to an emitter coupled logic (ECL) to the CMOS converter.

When a single-ended signal is used as the reference, connect the reference signal to REFP and program Bit 6 in REG0022 to 0. In this case, SW1 and SW2 are closed, SW3 and SW4 are open, and the current source that drives the differential pair of transistors switches off.

For optimum integer boundary spur and phase noise performance, use the single-ended setting for all references up to 500 MHz (even if using a differential signal). Use the differential setting for reference frequencies greater than 500 MHz.

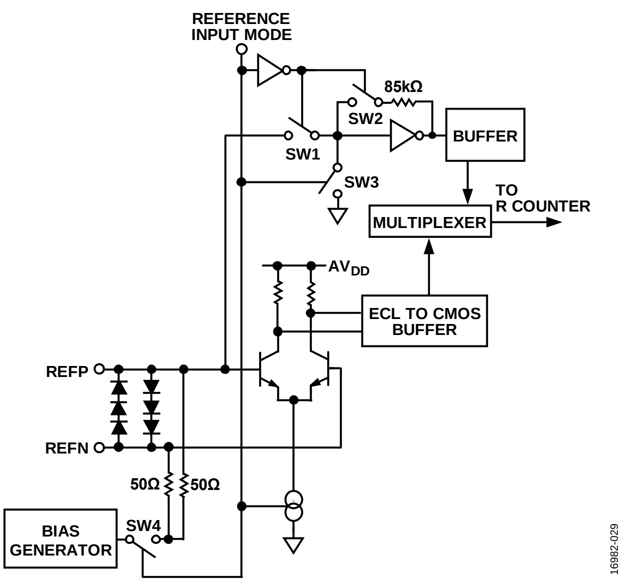


Figure 35. Reference Input Stage, Differential Mode

RF N DIVIDER

The RF N divider allows a division ratio in the PLL feedback path. Determine the division ratio by the INT, FRAC1, FRAC2, and MOD2 values that this divider comprises.

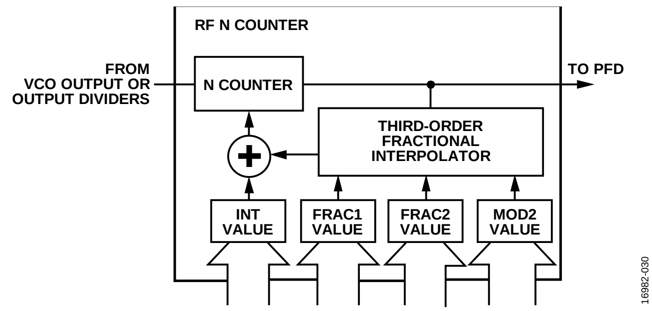


Figure 36. RF N Divider

INT, FRAC, MOD, and R Counter Relationship

The INT, FRAC1, FRAC2, MOD1, and MOD2 values, in conjunction with the R counter, make it possible to generate output frequencies that are spaced by fractions of f_{PFD}. For more information, see the RF Synthesizer, a Worked Example section.

Calculate f_{VCO_OUT} using the following equation:

$$f_{VCO\_OUT} = f_{PFD} \times N \quad (21)$$

Calculate f_{PFD} using the following equation:

$$f_{PFD} = REF_{IN} \times \frac{1+D}{R \times (1+T)} \quad (22)$$

where:
REF_{IN} is the reference frequency input.
D is the REF_{IN} doubler bit.
R is the preset divide ratio of the binary 5-bit programmable reference counter.
T is the REF_{IN} divide by 2 bit (0 or 1)

Calculate the desired value of the feedback counter N using the following equation:

$$N = INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1} \quad (23)$$

where:
INT is the 16-bit integer value. In integer mode, INT = 20 to 32,767 for the 4/5 prescaler, and 64 to 65,535 for the 8/9 prescaler. In fractional mode, INT= = 23 to 32,767 for the 4/5 prescaler, and 75 to 65,535 for the 8/9 prescaler.
FRAC1 is the numerator of the primary modulus (0 to 33,554,431).
FRAC2 is the numerator of the 14-bit auxiliary modulus (0 to 16,383).
MOD2 is the programmable, 14-bit auxiliary fractional modulus (2 to 16,383).
MOD1 is a 25-bit primary modulus with a fixed value of 2^{25} = 33,554,432.

These calculations result in a very low frequency resolution with no residual frequency error. To apply Equation 23, perform the following steps:

1. Calculate N by dividing VCO_{OUT}/f_{PFD}. The integer value of this number forms INT.
2. Subtract INT from the full N value.
3. Multiply the remainder by 2^{25}. The integer value of this number forms FRAC1.
4. Calculate MOD2 based on the channel spacing (f_{CHSP}) using the following equation:

$$MOD2 = fPFD/GCD(fPFD, fCHSP) \quad (24)$$

where:
f_{CHSP} is the desired channel spacing frequency.
$GCD(f_{PFD}, f_{CHSP})$ is the greatest common divisor of the PFD frequency and the channel spacing frequency.

5. Calculate FRAC2 using the following equation:

$$FRAC2 = ((N - INT) \times 2^{25} - FRAC1) \times MOD2 \quad (25)$$

The FRAC2 and MOD2 fraction result in outputs with zero frequency error for channel spacing when

$$f_{PFD}/\text{GCD}(f_{PFD}, f_{CHSP}) = MOD2 < 16{,}383 \quad (26)$$

If zero frequency error is not required, the MOD1 and MOD2 denominators operate together to create a 39-bit resolution modulus.

INT N Mode

When FRAC1 and FRAC2 are equal to 0, the synthesizer operates in integer N mode. It is recommended that the SD_EN_FRAC0 bit in REG002B be set to 1 to disable the SDMs, which gives an improvement in the inband phase noise, and reduces any additional ΣΔ noise.

R Counter

The 5-bit R counter allows the input reference frequency (input to REFP and REFN) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 32 are allowed.

PFD AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 37 is a simplified schematic of the phase frequency detector. The PFD includes a fixed delay element that sets the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and provides a consistent reference spur level. Set the phase detector polarity to positive on this device because of the positive tuning of the VCO.

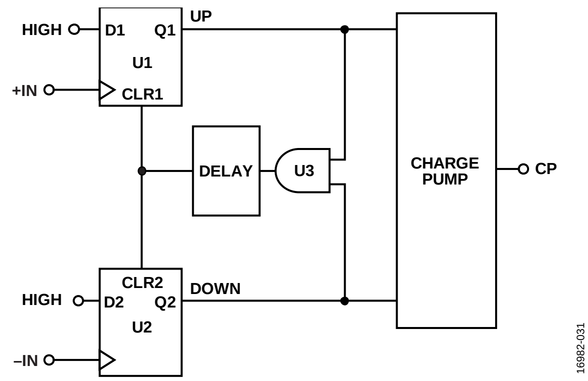


Figure 37. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4371 allows the user to access various internal points on the chip. Figure 38 shows the MUXOUT section in block diagram form.

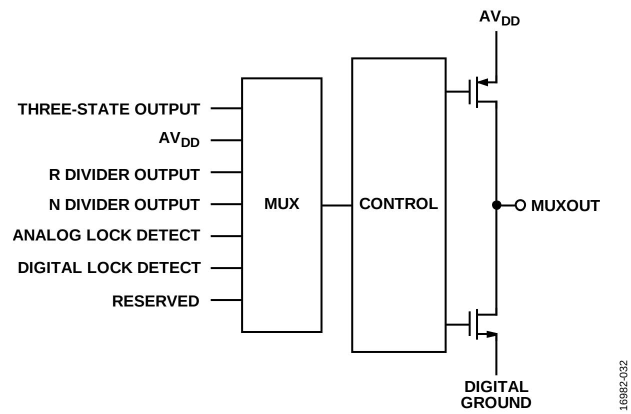


Figure 38. MUXOUT Schematic

DOUBLE BUFFERS

The main fractional value (FRAC1), auxiliary modulus value (MOD2), auxiliary fractional value (FRAC2), reference doubler, reference divide by 2 (RDIV2), R counter value, and charge pump current setting are double buffered in the ADF4371. Two events must occur before the ADF4371 uses a new value for any of the double buffered settings. First, the new value must latch into the device by writing to the appropriate register, and second, a new write to REG0010 must be performed.

For example, to ensure that the modulus value loads correctly, every time that the modulus value updates, REG0010 must be written to.

VCO

The VCO in the ADF4371 consists of four separate VCO cores: Core A, Core B, Core C, and Core D, each of which uses 256 overlapping bands, which allows the device to cover a wide frequency range without large VCO sensitivity (K_V) and without resultant poor phase noise and spurious performance.

The correct VCO and band are chosen automatically by the VCO and band select logic whenever REG0010 is updated, and automatic calibration is enabled. The V_{TUNE} is disconnected from the output of the loop filter and is connected to an internal reference voltage.

The R counter output is used as the clock for the band select logic. After band selection, normal PLL action resumes. The nominal value of K_V is 50 MHz/V when the N divider is driven from the VCO output, or the K_V value is divided by D. D is the output divider value if the N divider is driven from the RF output divider.

The VCO shows variation of K_V as the tuning voltage, VTUNE, varies within the band and from band to band. For wideband applications covering a wide frequency range (and changing output dividers), a value of 50 MHz/V provides the most accurate K_V, because this value is closest to the average value. Figure 39 and Figure 40 shows how K_V varies with fundamental VCO frequency along with an average value for the frequency band. Users may prefer Figure 39 and Figure 40 when using narrow-band designs.

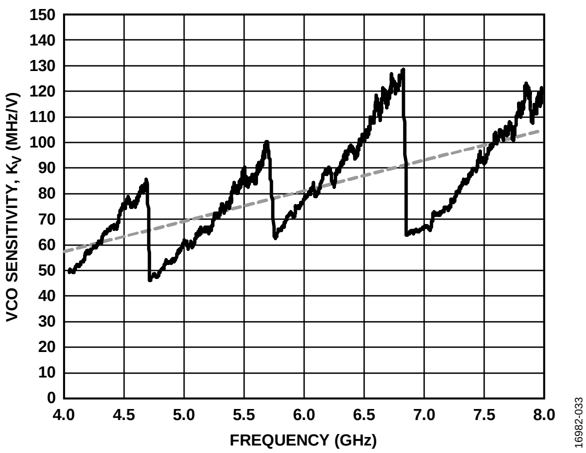


Figure 39. VCO Sensitivity, K_V vs. Frequency VCC_VCO = 5 V

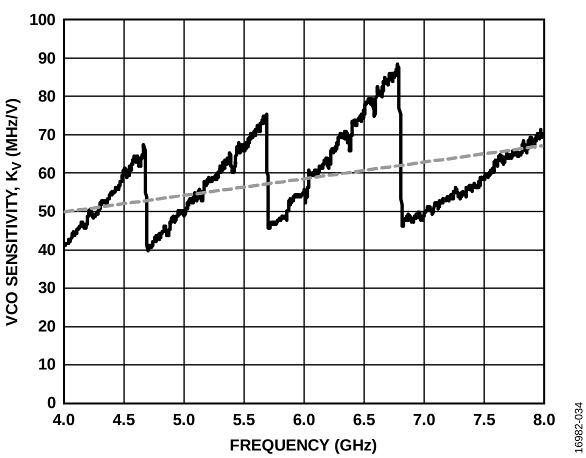


Figure 40. VCO Sensitivity, K_V vs. Frequency VCC_VCO = 3.3 V

VCO ALC THRESHOLD

Different VCO ALC threshold values are used for different device revisions for the best performance. The device revision is checked by reading the DEVICE_REVISION bits in Address 0x06. The default register values for the latest device revision (DEVICE_REVISION = 0x0A) are given in the register tables. When using the older device revision (DEVICE_REVISION = 0x09), the following settings are recommended:

- For 3.3 V VCO operation, Address 0x2D, Bits[2:0] = 0x1
- For 5 V VCO operation, Address 0x2E, Bits[2:0] = 0x2 and Address 0x2F, Bits[2:0] = 0x4

All other register settings are the same, and there is no difference in performance specifications between the two revisions.

OUTPUT STAGE

The RF8P and RF8N pins of the ADF4371 connect to the collectors of a bipolar negative positive negative (NPN) differential pair driven by buffered outputs of the VCO, as shown in Figure 41. The ADF4371 contains internal 50 Ω resistors connected to the VCC_X1 pin. To optimize the power dissipation vs. the output power requirements, the tail current of the differential pair is programmable using Bits[1:0] in REG0025. Four current levels can be set. These levels give approximate output power levels of −4 dBm, −1 dBm, 2 dBm, and 5 dBm. Levels of −4 dBm and −1 dBm can be achieved by ac coupling into a 50 Ω load. Levels of 2 dBm and 5 dBm require an external shunt inductor connected to the VCC_X1 pin. Do not use these two higher levels without an inductor because not using an inductor can cause the compression of the output stage. An inductor has a narrower operating frequency than a 50 Ω resistor. For accurate power levels, refer to the Typical Performance Characteristics section. Add an external shunt inductor to provide higher power levels, which is less wideband than the internal bias only. Terminate the unused complementary output with a circuit similar to the used output.

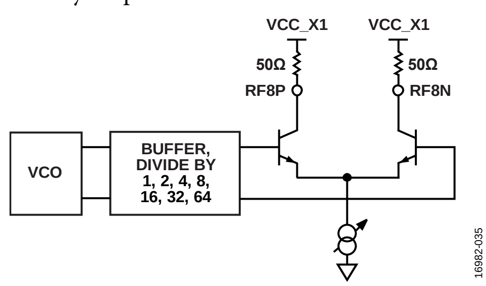


Figure 41. Output Stage

RFAUX8P and RFAUX8N provides the same functionality as the RF8P and RF8N output, but can also output the divided RF8x frequency or the VCO frequency if desired.

These outputs can be powered down when not in use, and the pins can be left open if unused.

The doubled VCO output (8 GHz to 16 GHz) is available on the RF16 pin, which can be directly connected to the next circuit. The quadrupled output is available on the RF32P and RF32N pins, which can also be directly connected to the next circuit.

DOUBLER

The VCO frequency multiplied by 2 is available at the RF16P and RF16N pins. This output can be powered down when not in use, and the pins RF16P and RF16N can be left open if unused.

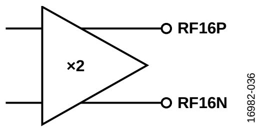


Figure 42. Doubler Output Stage

An automatic tracking filter on the ADF4371 that suppresses the VCO and other unwanted frequency products ensures the doubled output is maximized and that the VCO and 3 × VCO frequencies are suppressed regardless of the output frequency. Suppression of <50 dB is typical. The optimum values are set automatically by the automatic tracking when it is enabled using Bit 1 in REG0023.

It is possible to set coefficients manually (in REG0070), such as when both the quadrupler and doubler are enabled together. The settings for optimum output power, phase noise, and harmonic rejection are given in Table 7.

Table 7. Filter and Bias Settings for Doubled Output

Frequency (GHz)	Filter	Bias
<8.4	7	3
8.4 to 9.4	6	3
9.4 to 10	5	3
10 to 11.5	4	3
11.5 to 12.2	3	3
12.2 to 13.7	2	3
13.7 to 14.5	1	3
>14.5	0	3

QUADRUPLER

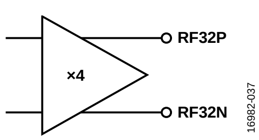


Figure 43. Quadrupler Output Stage

The VCO frequency multiplied by 4 is available at the RF32P and RF32N pins. This output can be powered down when not in use, and the RF32P and RF32N pins can be left open if unused.

The ADF4371 has an automatic tracking filter that suppresses VCO, 2 × VCO, 3 × VCO, 5 × VCO, and other unwanted frequency products, regardless of the output frequency. Suppression of <30 dB is typical. The automatic tracking does not set the optimum coefficients for quadrupled output. For optimum output power, phase noise, and harmonic rejection, disable automatic selection mode (Bit 1 in REG0023) and manually load the settings in Table 8 to REG0071.

Table 8. Filter and Bias Settings for Quadrupled Output

Frequency (GHz)	Filter	Bias
<18	7	3
18 to 19	3	3
19 to 20.5	1	0
20.5 to 26	0	0
>26	0	1

Automatic tracking mode (Bit 1 in REG0023) is common for doubler and quadrupler outputs. When they are enabled together, load the filter and bias coefficients for both outputs manually for optimum performance.

PHASE ADJUST AND SPUR OPTIMIZATION BY USING PHASE_WORD

The phase of the VCO output frequency can be adjusted in 24-bit steps which is set by Register 0x001B, Register 0x001C, and Register 0x001D (PHASE_WORD). To adjust the phase, take the following steps:

1. Lock the desired frequency, as usual.
2. Disable the autocalibration from REG0012, Bit 6 (EN_AUTOCAL).
3. Enable the phase adjust from REG001A, Bit 6 (PHASE_ADJ).
4. Set PHASE_WORD to the desired value.
5. Write to Register 0x10 (each write shifts the output by the amount defined in the previous step).

When fine tuning on the phase shift is required, set the phase word to another value, and write to REG0010 again.

PHASE_WORD can optimize spur levels. While locking to a new frequency, the PHASE_WORD value (phase adjust is disabled at this stage) affects the spur levels. A prime number close to 45°, 90°, or 180° is recommended. (An 8388617 value shows good performance for most cases). Because this value is only important while locking to a new frequency, the phase adjust can be enabled, and the output phase can be adjusted as previously explained after lock is achieved.

SPI

The SPI of the ADF4371 allows the user to configure the device as required via a 3-wire or 4-wire SPI port. This interface provides users with added flexibility and customization. The serial port interface consists of four control lines: SCLK, SDIO, $\overline{CS}$, and MUXOUT (not used in 3-wire SPI). The timing requirements for the SPI port are detailed in Table 2.

The SPI protocol consists of a read and write bit and 15 register address bits, followed by eight data bits. Both the address and data fields are organized with the MSB first and end with the LSB by default. The timing diagrams for write and read are shown in Figure 3 and Figure 4, respectively. The significant bit order can be changed via the REG0000 register, Bit 1 (LSB_FIRST) setting, and the related timing diagram is shown in Figure 2.

The ADF4371 input logic level for the write cycle is compatible with 1.8 V logic level (see the logic parameters in Table 1). On a read cycle, both the SDIO and MUXOUT pins are configurable for 1.8 V (default) or 3.3 V output levels by the LEV_SEL bit setting.

SPI Stream Mode

The ADF4371 supports stream mode, where data bits are loaded to or read from registers serially without writing the register address (instruction word). This mode is useful in time critical applications, when a large amount of data must be transferred or when some registers must be updated repeatedly.

The slave device starts reading or writing data to this address and continues as long as $\overline{CS}$ is asserted and single-byte writes are not enabled (Bit 7 in REG0001). The slave device automatically increments or decrements the address depending on the setting of the address ascension bit (Bit 2 in REG0000).

The diagram of 3-byte streaming is shown in Figure 5. The instruction header starts with a Logic 0 to indicate a write sequence and addresses the register. Then, the data for registers (N, N − 1, and N − 2) are loaded consecutively without any assertion in $\overline{CS}$.

The registers are organized into eight bits, and if a register requires more than eight bits, sequential register addresses are used. This organization enables using stream mode and simplifies loading. For example, FRAC1WORD is stored in REG0016, REG0015, and REG0014 (MSB to LSB). These registers can be loaded by using REG0016 and sending the whole 24-bit data afterward, as shown in Figure 5.

DEVICE SETUP

The recommended sequence of steps to set up the ADF4371 are as follows:

1. Set up the SPI interface.
2. Perform the initialization sequence.
3. Perform the frequency update sequence.

STEP 1: SET UP THE SPI INTERFACE

First, initialize the SPI. Write the values in Table 9 to REG0000 and REG0001.

Table 9. SPI Interface Setup

Address	Setting	Notes
0x00	0x18	4-wire SPI
0x01	0x00	Stalling, master readback control

STEP 2: INITIALIZATION SEQUENCE

Write to each register in reverse order from Address 0x7C to Address 0x10. Choosing appropriate values to generate the desired frequency. The frequency update sequence follows to generate the desired output frequency.

STEP 3: FREQUENCY UPDATE SEQUENCE

Frequency updates require updating R, MOD2, FRAC1, FRAC2, and INT. The autocalibration process works reliably when $f_{PFD} \leq 125$ MHz.

Therefore, the update sequence must be as follows for $f_{PFD} \leq$ 125 MHz:

1. REG001F (new R_WORD[4:0])
2. REG001A (new MOD2WORD[13:8])
3. REG0019 (new MOD2WORD[7:0])
4. REG0018 (new FRAC2WORD[13:7])
5. REG0017 (new FRAC2WORD[6:0])
6. REG0016 (new FRAC1WORD[23:16])
7. REG0015 (new FRAC1WORD[15:8])
8. REG0014 (new FRAC1WORD[7:0])
9. REG0011 (new BIT_INTEGER_WORD[15:8])
10. REG0010 (new BIT_INTEGER_WORD[7:0])

The frequency change occurs on the write to REG0010.

When using a higher f_{PFD} in normal operation, use half of the f_{PFD} routine in the autocalibration process. The routine can be described shortly as follows: if $f_{PFD} > 125$MHz; use autocalibration with half of the f_{PFD} by doubling the R value and doubling the N value. Once the lock is achieved, disable the autocalibration and set the desired R and N values.

Therefore, the updated sequence must be as follows for $f_{PFD} >$ 125 MHz:

1. REG001F (with doubled R_WORD[4:0] for halved f_{PFD})
2. REG001A (MOD2WORD[13:8] for halved f_{PFD})
3. REG0019 (MOD2WORD[7:0] for halved f_{PFD})
4. REG0018 (FRAC2WORD[13:7] for halved f_{PFD})
5. REG0017 (FRAC2WORD[6:0] for halved f_{PFD})
6. REG0016 (FRAC1WORD[23:16] for halved f_{PFD})
7. REG0015 (FRAC1WORD[15:8] for halved f_{PFD})
8. REG0014 (FRAC1WORD[7:0] for halved f_{PFD})
9. REG0012 (enable autocalibration: EN_AUTOCAL = 1)
10. REG0011 (BIT_INTEGER_WORD[15:8] for halved f_{PFD})
11. REG0010 (BIT_INTEGER_WORD[7:0] for halved f_{PFD})
12. Ensure the device is locked by checking lock detect.
13. REG001F (R_WORD[4:0] for desired f_{PFD})
14. REG001A (MOD2WORD[13:8] for desired f_{PFD})
15. REG0019 (MOD2WORD[7:0] for desired f_{PFD})
16. REG0018 (FRAC2WORD[13:7] for desired f_{PFD})
17. REG0017 (FRAC2WORD[6:0] for desired f_{PFD})
18. REG0016 (FRAC1WORD[23:16] for desired f_{PFD})
19. REG0015 (FRAC1WORD[15:8] for desired f_{PFD})
20. REG0014 (FRAC1WORD[7:0] for desired f_{PFD})
21. REG0012 (disable autocalibration: EN_AUTOCAL = 0)
22. REG0011 (BIT_INTEGER_WORD[15:8] for desired f_{PFD})
23. REG0010 (BIT_INTEGER_WORD[7:0] for desired f_{PFD})

The frequency change occurs on the second write to REG0010.

Because halved f_{PFD} is used with autocalibration, use the half of the f_{PFD} value in the calculation of the timeout values explained in Lock Time section.

The unchanged registers do not need to be updated. For example, for an integer-N PLL configuration (fractional devices are not used), skip Step 1 to Step 8. In this case, the only required updates are REG0011 and REG0010.

APPLICATIONS INFORMATION

POWER SUPPLIES

The ADF4371 contains four multiband VCOs that together cover an octave range of frequencies. To achieve optimal VCO phase noise performance, it is recommended to connect a low noise regulator, such as the ADM7150 or LT3045 to the VCC_VCO pin. Connect the same regulator to the VCC_VCO and VCC_LDO pins. 1 µF decoupling capacitors connected to the 5 V VCO supply are recommended.

For all other the 3.3 V supply pins, use one ADM7150 or one LT3045 regulator. 1 µF is also recommended for the VDD_VP pin. Additional decoupling to other supply pins is not required.

PCB DESIGN GUIDELINES FOR AN LGA PACKAGE

The bottom of the chip scale package has a central exposed thermal pad. The thermal pad on the PCB must be at least as large as the exposed pad. On the PCB, there must be a minimum clearance of 0.25 mm between the thermal pad and the inner edges of the pad pattern. This clearance ensures the avoidance of shorting.

To improve the thermal performance of the package, use thermal vias on the PCB thermal pad. If vias are used, incorporate them into the thermal pad at the 1.2 mm pitch grid. The via diameter must be between 0.3 mm and 0.33 mm, and the via barrel must be plated with 1 oz. of copper to plug the via.

For a microwave PLL and VCO synthesizer, such as the ADF4371, take care with the board stackup and layout. Do not consider using FR4 material because it causes an amplitude decrease in signals greater than 3 GHz. Instead, Rogers 4350, Rogers 4003, or Rogers 3003 dielectric material is suitable.

Take care with the RF output traces to minimize discontinuities and ensure the best signal integrity. Via placement and grounding are critical.

OUTPUT MATCHING

The low frequency output can be ac-coupled to the next circuit, if desired. However, if higher output power is required, use a pull-up inductor to increase the output power level.

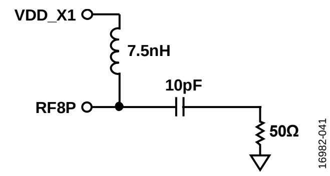


Figure 44. Optimum Output Stage

When differential outputs are not needed, terminate the unused output or combine it with both outputs using a balun.

For lower frequencies less than 1 GHz, it is recommended to use a 100 nH inductor on the RF8P and RF8N pins.

The RF8P and RF8N pins form a differential circuit. Provide each output with the same (or similar) components where possible, including the same shunt inductor value, bypass capacitor, and termination.

The RFAUX8P and RFAUX8N pins are effectively the same as RF8P and RF8N and must be treated in the manner as outlined for RF8P and RF8N.

The RF16P and RF16N pins and the RF32P and RF32N pins can be directly connected to the next circuit stage. These pins are internally matched to 50 Ω and do not require additional decoupling.

REGISTER SUMMARY

Table 10. ADF4371 Register Summary

Reg	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	RW
0x00	[7:0]	SOFT_RESET_R	LSB_FIRST_R	ADDRESS_ASCENSION_R	SDO_ACTIVE_R	SDO_ACTIVE	ADDRESS_ASCENSION	LSB_FIRST	SOFT_RESET	0x18	R/W
0x01	[7:0]	SINGLE_INSTRUCTION	STALLING	MASTER_READBACK_CONTROL	RESERVED					0x00	R/W
0x03	[7:0]	RESERVED				CHIP_TYPE				0x0X	R
0x04	[7:0]	PRODUCT_ID[7:0]								0xXX	R/W
0x05	[7:0]	PRODUCT_ID[15:8]								0xXX	R/W
0x06	[7:0]	PRODUCT_GRADE				DEVICE_REVISION				0xXX	R
0x10	[7:0]	BIT_INTEGER_WORD[7:0]								0x32	R/W
0x11	[7:0]	BIT_INTEGER_WORD[15:8]								0x00	R/W
0x12	[7:0]	RESERVED	EN_AUTOCAL	PRE_SEL	RESERVED					0x40	R/W
0x14	[7:0]	FRAC1WORD[7:0]								0x00	R/W
0x15	[7:0]	FRAC1WORD[15:8]								0x00	R/W
0x16	[7:0]	FRAC1WORD[23:16]								0x00	R/W
0x17	[7:0]	FRAC2WORD[6:0]							FRAC1WORD[24]	0x00	R/W
0x18	[7:0]	RESERVED	FRAC2WORD[13:7]							0x00	R/W
0x19	[7:0]	MOD2WORD[7:0]								0xE8	R/W
0x1A	[7:0]	RESERVED	PHASE_ADJ	MOD2WORD[13:8]						0x03	R/W
0x1B	[7:0]	PHASE_WORD[7:0]								0x00	R/W
0x1C	[7:0]	PHASE_WORD[15:8]								0x00	R/W
0x1D	[7:0]	PHASE_WORD[23:16]								0x00	R/W
0x1E	[7:0]	CP_CURRENT				PD_POL	PD	RESERVED	CNTR_RESET	0x48	R/W
0x1F	[7:0]	RESERVED			R_WORD					0x01	R/W
0x20	[7:0]	MUXOUT				MUXOUT_EN	LEV_SEL	RESERVED		0x14	R/W
0x22	[7:0]	RESERVED	REFIN_MODE	REF_DOUB	RDIV2	RESERVED				0x00	R/W
0x23	[7:0]	RESERVED		CLK_DIV_MODE		RESERVED		TRACKING_FILTER_MUX_SEL	RESERVED	0x00	R/W
0x24	[7:0]	FB_SEL	DIV_SEL			RESERVED				0x80	R/W
0x25	[7:0]	MUTE_LD	RESERVED	RF_DIVSEL_DB	X4_EN	X2_EN	RF_EN	RF_OUT_POWER		0x07	R/W
0x26	[7:0]	BLEED_ICP								0x32	R/W
0x27	[7:0]	LD_BIAS		LDP	BLEED_GATE	BLEED_EN	VCOLDO_PD	RF_PBS		0xC5	R/W
0x28	[7:0]	RESERVED					LD_COUNT		LOL_EN	0x03	R/W
0x2A	[7:0]	RESERVED		BLEED_POL	RESERVED	LE_SEL	RESERVED		READ_SEL	0x00	R/W
0x2B	[7:0]	RESERVED		LSB_P1	VAR_MOD_EN	RESERVED	SD_LOAD_ENB	RESERVED	SD_EN_FRAC0	0x01	R/W
0x2C	[7:0]	RESERVED	ALC_RECT_SELECT_VCO1	ALC_REF_DAC_LO_VCO1	ALC_REF_DAC_NOM_VCO1			VTUNE_CALSET_EN	DISABLE_ALC	0x44	R/W
0x2D	[7:0]	RESERVED			ALC_RECT_SELECT_VCO2	ALC_REF_DAC_LO_VCO2	ALC_REF_DAC_NOM_VCO2			0x11	R/W
0x2E	[7:0]	RESERVED			ALC_RECT_SELECT_VCO3	ALC_REF_DAC_LO_VCO3	ALC_REF_DAC_NOM_VCO3			0x10	R/W
0x2F	[7:0]	SWITCH_LDO_3P3V_5V	RESERVED		ALC_RECT_SELECT_VCO4	ALC_REF_DAC_LO_VCO4	ALC_REF_DAC_NOM_VCO4			0x92	R/W
0x30	[7:0]	VCO_BAND_DIV								0x3F	R/W
0x31	[7:0]	TIMEOUT[7:0]								0xA7	R/W
0x32	[7:0]	ADC_MUX_SEL	RESERVED	ADC_FAST_CONV	ADC_CTS_CONV	ADC_CONVERSION	ADC_ENABLE	TIMEOUT[9:8]		0x04	R/W
0x33	[7:0]	RESERVED			SYNTH_LOCK_TIMEOUT					0x0C	R/W
0x34	[7:0]	VCO_FSM_TEST_MODES			VCO_ALC_TIMEOUT					0x9E	R/W
0x35	[7:0]	ADC_CLK_DIVIDER								0x4C	R/W
0x36	[7:0]	ICP_ADJUST_OFFSET								0x30	R/W
0x37	[7:0]	SI_BAND_SEL								0x00	R/W
0x38	[7:0]	SI_VCO_SEL				SI_VCO_BIAS_CODE				0x00	R/W
0x39	[7:0]	RESERVED	VCO_FSM_TEST_MUX_SEL			SI_VTUNE_CAL_SET				0x07	R/W

Reg	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	RW
0x3A	[7:0]	ADC_OFFSET								0x55	R/W
0x3D	[7:0]	RESERVED	SD_RESET	RESERVED						0x00	R/W
0x3E	[7:0]	RESERVED				CP_TMODE		RESERVED		0x0C	R/W
0x3F	[7:0]	CLK1_DIV[7:0]								0x80	R/W
0x40	[7:0]	RESERVED	TRM_IB_VCO_BUF			CLK1_DIV[11:8]				0x50	R/W
0x41	[7:0]	CLK2_DIVIDER_1[7:0]								0x28	R/W
0x42	[7:0]	CLK2_DIVIDER_2[3:0]				CLK2_DIVIDER_1[11:8]				0x00	R/W
0x47	[7:0]	TRM_RESD_VCO_MUX			RESERVED					0xC0	R/W
0x52	[7:0]	TRM_RESD_VCO_BUF			TRM_RESCI_VCO_BUF			RESERVED		0xF4	R/W
0x6E	[7:0]	VCO_DATA_READBACK[7:0]								0x00	R
0x6F	[7:0]	VCO_DATA_READBACK[15:8]								0x00	R
0x70	[7:0]	BAND_SEL_X2			RESERVED			BIAS_SEL_X2		0x03	R/W
0x71	[7:0]	BAND_SEL_X4			RESERVED			BIAS_SEL_X4		0x60	R/W
0x72	[7:0]	RESERVED	AUX_FREQ_ SEL	POUT_AUX		PDB_AUX	RESERVED	COUPLED_ VCO	RESERVED	0x32	R/W
0x73	[7:0]	RESERVED					ADC_CLK_ DISABLE	PD_NDIV	LD_DIV	0x00	R/W
0x7C	[7:0]	RESERVED							LOCK_ DETECT_ READBACK	0x00	R

REGISTER DETAILS

Address: 0x00, Default: 0x18, Name: REG0000

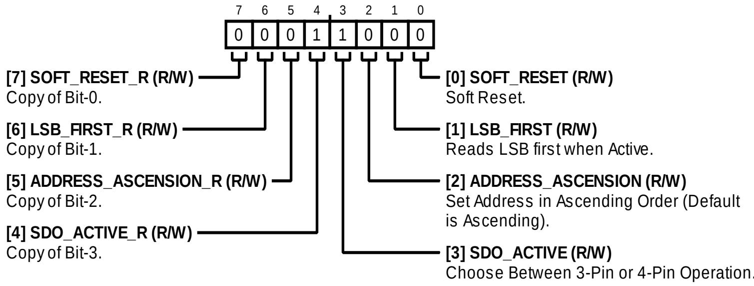


Table 11. Bit Descriptions for REG0000

Bit(s)	Bit Name	Description	Default	Access
7	SOFT_RESET_R	Copy of Bit 0.	0x0	R/W
6	LSB_FIRST_R	Copy of Bit 1.	0x0	R/W
5	ADDRESS_ASCENSION_R	Copy of Bit 2.	0x0	R/W
4	SDO_ACTIVE_R	Copy of Bit 3.	0x1	R/W
3	SDO_ACTIVE	Choose Between 3-Pin or 4-Pin Operation. 0: 3-pin. 1: 4-pin. Enables SDIO pin and the SDIO pin becomes an input only.	0x1	R/W
2	ADDRESS_ASCENSION	Set Address in Ascending Order (Default Is Ascending). 0: descending. 1: ascending.	0x0	R/W
1	LSB_FIRST	Reads LSB First when Active.	0x0	R/W
0	SOFT_RESET	Soft Reset. 0: normal operation. 1: soft reset.	0x0	R/W

Address: 0x01, Default: 0x00, Name: REG0001

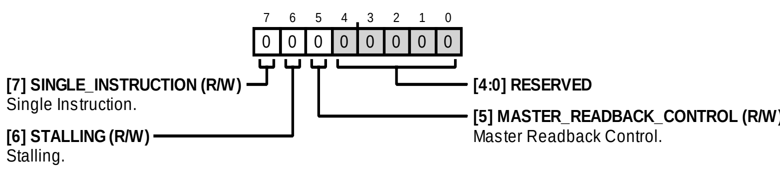


Table 12. Bit Descriptions for REG0001

Bit(s)	Bit Name	Description	Default	Access
7	SINGLE_INSTRUCTION	Single Instruction. SPI stream mode is disabled if this bit is set to 1.	0x0	R/W
6	STALLING	Stalling.	0x0	R/W
5	MASTER_READBACK_CONTROL	Master Readback Control.	0x0	R/W
[4:0]	RESERVED	Reserved.	0x0	R

Address: 0x03, Default: 0x0X, Name: REG0003

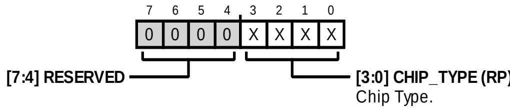


Table 13. Bit Descriptions for REG0003

Bit(s)	Bit Name	Description	Default	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHIP_TYPE	Chip Type.	Prog	RP

Address: 0x04, Default: 0xXX, Name: REG0004

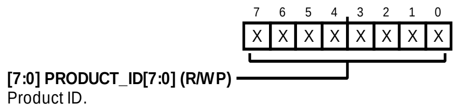


Table 14. Bit Descriptions for REG0004

Bit(s)	Bit Name	Description	Default	Access
[7:0]	PRODUCT_ID[7:0]	Product ID.	Prog	R/WP

Address: 0x05, Default: 0xXX, Name: REG0005

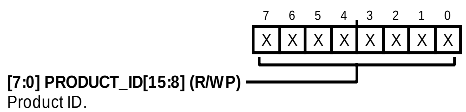


Table 15. Bit Descriptions for REG0005

Bit(s)	Bit Name	Description	Default	Access
[7:0]	PRODUCT_ID[15:8]	Product ID.	Prog	R/WP

Address: 0x06, Default: 0xXX, Name: REG0006

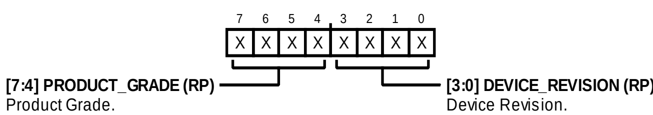


Table 16. Bit Descriptions for REG0006

Bit(s)	Bit Name	Description	Default	Access
[7:4]	PRODUCT_GRADE	Product Grade.	Prog	RP
[3:0]	DEVICE_REVISION	Device Revision.	Prog	RP

Address: 0x10, Default: 0x32, Name: REG0010

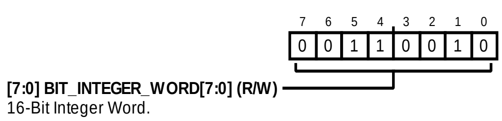


Table 17. Bit Descriptions for REG0010

Bit(s)	Bit Name	Description	Default	Access
[7:0]	BIT_INTEGER_WORD[7:0]	16-Bit Integer Word. Sets the integer value of N. Updates to the PLL N counter, including FRAC1, FRAC2, and MOD2, are double buffered by this bitfield.	0x32	R/W

Address: 0x11, Default: 0x00, Name: REG0011

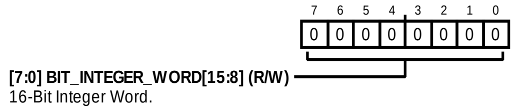


Table 18. Bit Descriptions for REG0011

Bit(s)	Bit Name	Description	Default	Access
[7:0]	BIT_INTEGER_WORD[15:8]	16-Bit Integer Word. Sets the integer value of N.	0x0	R/W

Address: 0x12, Default: 0x40, Name: REG0012

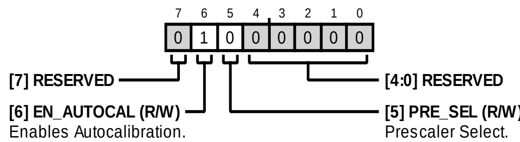


Table 19. Bit Descriptions for REG0012

Bit(s)	Bit Name	Description	Default	Access
7	RESERVED	Reserved.	0x0	R
6	EN_AUTOCAL	Enables Autocalibration. 0: VCO autocalibration disabled. 1: VCO autocalibration enabled.	0x1	R/W
5	PRE_SEL	Prescaler Select. The dual modulus prescaler is set by this bit. The prescaler, at the input to the N divider, divides down the VCO signal so the N divider can handle it. The prescaler setting affects the RF frequency and the minimum and maximum INT value. 0: 4/5 prescaler. 1: 8/9 prescaler.	0x0	R/W
[4:0]	RESERVED	Reserved.	0x0	R

Address: 0x14, Default: 0x00, Name: REG0014

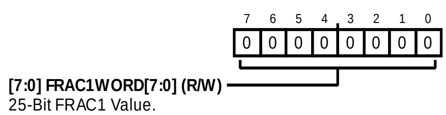


Table 20. Bit Descriptions for REG0014

Bit(s)	Bit Name	Description	Default	Access
[7:0]	FRAC1WORD[7:0]	25-Bit FRAC1 Value. Sets the FRAC1 value.	0x0	R/W

Address: 0x15, Default: 0x00, Name: REG0015

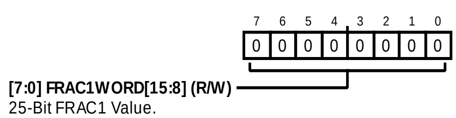


Table 21. Bit Descriptions for REG0015

Bit(s)	Bit Name	Description	Default	Access
[7:0]	FRAC1WORD[15:8]	25-Bit FRAC1 Value. Sets the FRAC1 value.	0x0	R/W

Address: 0x16, Default: 0x00, Name: REG0016

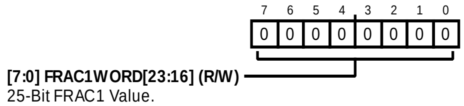


Table 22. Bit Descriptions for REG0016

Bit(s)	Bit Name	Description	Default	Access
[7:0]	FRAC1WORD[23:16]	25-Bit FRAC1 Value. Sets the FRAC1 value.	0x0	R/W

Address: 0x17, Default: 0x00, Name: REG0017

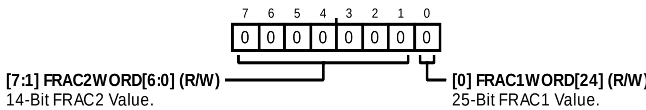


Table 23. Bit Descriptions for REG0017

Bit(s)	Bit Name	Description	Default	Access
[7:1]	FRAC2WORD[6:0]	14-Bit FRAC2 Value. Sets the FRAC2 value.	0x0	R/W
0	FRAC1WORD[24:24]	25-Bit FRAC1 Value. Sets the FRAC1 value.	0x0	R/W

Address: 0x18, Default: 0x00, Name: REG0018

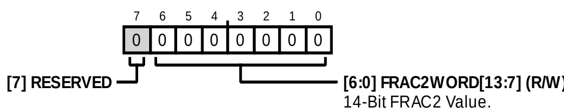


Table 24. Bit Descriptions for REG0018

Bit(s)	Bit Name	Description	Default	Access
7	RESERVED	Reserved.	0x0	R
[6:0]	FRAC2WORD[13:7]	14-Bit FRAC2 Value. Sets the FRAC2 value.	0x0	R/W

Address: 0x19, Default: 0xE8, Name: REG0019

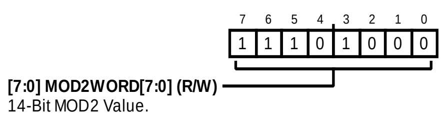


Table 25. Bit Descriptions for REG0019

Bit(s)	Bit Name	Description	Default	Access
[7:0]	MOD2WORD[7:0]	14-Bit MOD2 Value. Sets the MOD2 value.	0xE8	R/W

Address: 0x1A, Default: 0x03, Name: REG001A

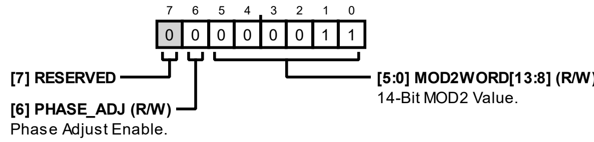


Table 26. Bit Descriptions for REG001A

Bit(s)	Bit Name	Description	Default	Access
7	RESERVED	Reserved.	0x0	R
6	PHASE_ADJ	Phase Adjust Enable. Set to 1 to enable phase adjust. Phase adjust increases the phase of the output relative to the current phase. 0: phase adjust disabled. 1: phase adjust enabled.	0x0	R/W
[5:0]	MOD2WORD[13:8]	14-Bit MOD2 Value. Sets the MOD2 value.	0x3	R/W

Address: 0x1B, Default: 0x00, Name: REG001B

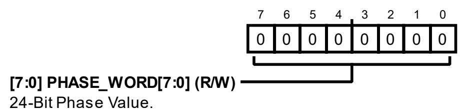


Table 27. Bit Descriptions for REG001B

Bit(s)	Bit Name	Description	Default	Access
[7:0]	PHASE_WORD[7:0]	24-Bit Phase Value. Sets the phase word for phase adjust. The phase of the RF output frequency can be adjusted in 24-bit steps. Phase Step = Phase Word ÷ 16,777,216 × 360°.	0x0	R/W

Address: 0x1C, Default: 0x00, Name: REG001C

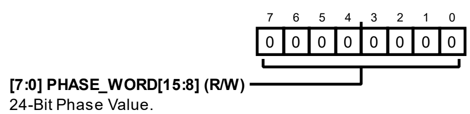


Table 28. Bit Descriptions for REG001C

Bit(s)	Bit Name	Description	Default	Access
[7:0]	PHASE_WORD[15:8]	24-Bit Phase Value. Sets the phase word for phase adjust. The phase of the RF output frequency can be adjusted in 24-bit steps. Phase Step = Phase Word ÷ 16,777,216 × 360°.	0x0	R/W

Address: 0x1D, Default: 0x00, Name: REG001D

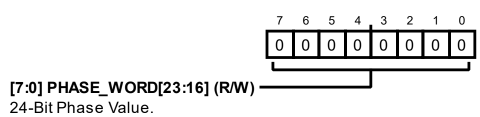


Table 29. Bit Descriptions for REG001D

Bit(s)	Bit Name	Description	Default	Access
[7:0]	PHASE_WORD[23:16]	24-Bit Phase Value. Sets the phase word for phase adjust. The phase of the RF output frequency can be adjusted in 24-bit steps. Phase Step = Phase Word ÷ 16,777,216 × 360°.	0x0	R/W

Address: 0x1E, Default: 0x48, Name: REG001E

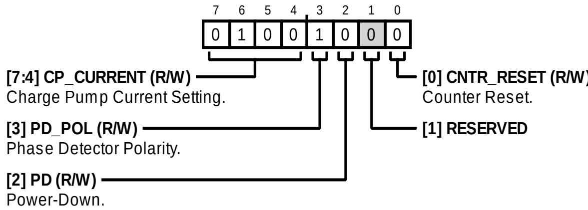


Table 30. Bit Descriptions for REG001E

Bit(s)	Bit Name	Description	Default	Access
[7:4]	CP_CURRENT	Charge Pump Current Setting. Sets the charge pump current. Set these bits to the charge pump current that the loop filter is designed for. 0: 0.35 mA. 1: 0.70 mA. 10: 1.05 mA. 11: 1.4 mA. 100: 1.75 mA. 101: 2.1 mA. 110: 2.45 mA. 111: 2.8 mA. 1000: 3.15 mA. 1001: 3.5 mA. 1010: 3.85 mA. 1011: 4.2 mA. 1100: 4.55 mA. 1101: 4.9 mA. 1110: 5.25 mA. 1111: 5.6 mA.	0x4	R/W
3	PD_POL	Phase Detector Polarity. If using a noninverting loop filter and a VCO with positive tuning slope, set phase detector polarity to positive. If using an inverting loop filter and a VCO with a negative tuning slope, set phase detector polarity to positive. If using a noninverting loop filter and a VCO with a negative tuning slope, set phase detector polarity to negative. If using an inverting loop filter and a VCO with a positive tuning slope, set phase detector polarity to negative. 0: negative phase detector polarity. 1: positive phase detector polarity.	0x1	R/W
2	PD	Power-Down. Setting to 1 powers down all internal PLL blocks of the ADF4371. The VCO and multipliers remain powered up. The registers do not lose their values. After bringing the ADF4371 out of power-down (setting to 0) a write to REG0010 is required to relock the loop. 0: normal operation. 1: power-down.	0x0	R/W
1	RESERVED	Reserved.	0x0	R
0	CNTR_RESET	Counter Reset. Setting to 1 holds the N divider and R counter in reset. There are no signals entering the PFD. 0: normal operation. 1: counter reset.	0x0	R/W

Address: 0x1F, Default: 0x01, Name: REG001F

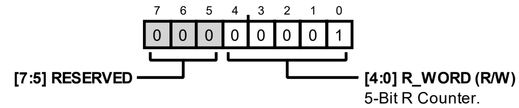


Table 31. Bit Descriptions for REG001F

Bit(s)	Bit Name	Description	Default	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	R_WORD	5-Bit R Counter. 0: 32 1: 1 10: 2 11: 3 … 11111: 31	0x1	R/W

Address: 0x20, Default: 0x14, Name: REG0020

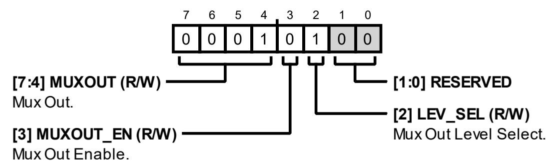


Table 32. Bit Descriptions for REG0020

Bit(s)	Bit Name	Description	Default	Access
[7:4]	MUXOUT	Mux Out. Is used to set the mux out signal when MUXOUT_EN = 1. 0: tristate, high impedance output (only works when MUXOUT_EN = 0). 1: digital lock detect. 10: charge pump up. 11: charge pump down. 100: R divider/2. 101: N divider/2. 110: VCO test modes. 111: Reserved. 1000: high. 1001: VCO calibration R band/2. 1010: VCO calibration N band/2.	0x1	R/W
3	MUXOUT_EN	Mux Out Enable. Set to 0 if using 4-wire SPI. 0: MUXOUT pin is configured as the serial data output for 4-wire SPI. Mux out functionality is disabled. 1: MUXOUT pin is configured for mux out functionality.	0x0	R/W
2	LEV_SEL	Mux Out Level Select. Select the voltage level of the logic at the mux out. 0: 1.8 V logic. 1: 3.3 V logic.	0x1	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x22, Default: 0x00, Name: REG0022

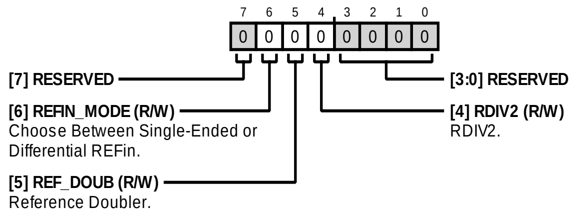


Table 33. Bit Descriptions for REG0022

Bit(s)	Bit Name	Description	Default	Access
7	RESERVED	Reserved.	0x0	R
6	REFIN_MODE	Choose Between Single-Ended or Differential REF_{IN}. 0: single-ended REF_{IN}. 1: differential REF_{IN}.	0x0	R/W
5	REF_DOUB	Reference Doubler. Controls the reference doubler block. 0: doubler disabled. 1: doubler enabled.	0x0	R/W
4	RDIV2	RDIV2. Controls the reference divide by 2 clock. This feature can be used to provide a 50% duty cycle signal to the PFD. 0: RDIV2 disabled. 1: RDIV2 enabled.	0x0	R/W
[3:0]	RESERVED	Reserved.	0x0	R

Address: 0x23, Default: 0x00, Name: REG0023

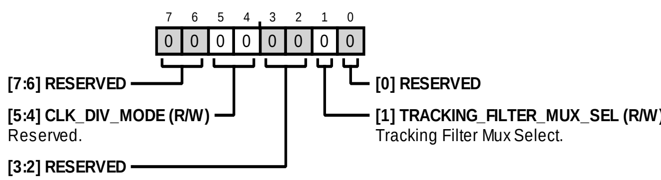


Table 34. Bit Descriptions for REG0023

Bit(s)	Bit Name	Description	Default	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:4]	CLK_DIV_MODE	Reserved.	0x0	R/W
[3:2]	RESERVED	Reserved.	0x0	R
1	TRACKING_FILTER_MUX_SEL	Tracking Filter Mux Select. 0: normal, tracking filter coefficients set automatically. 1: tracking filter coefficients set manually from SPI (REG0070 and REG0071).	0x0	R/W
0	RESERVED	Reserved.	0x0	R

Address: 0x24, Default: 0x80, Name: REG0024

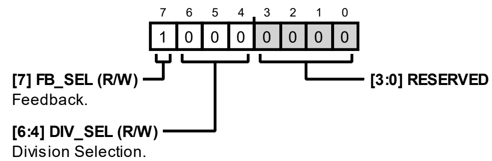


Table 35. Bit Descriptions for REG0024

Bit(s)	Bit Name	Description	Default	Access
7	FB_SEL	Feedback. 0: divider feedback to N counter. 1: fundamental feedback to N counter.	0x1	R/W
[6:4]	DIV_SEL	Division Selection. 0: divide 1. 1: divide 2. 10: divide 4. 11: divide 8. 100: divide 16. 101: divide 32. 110: divide 64. 111: reserved.	0x0	R/W
[3:0]	RESERVED	Reserved.	0x0	R

Address: 0x25, Default: 0x07, Name: REG0025

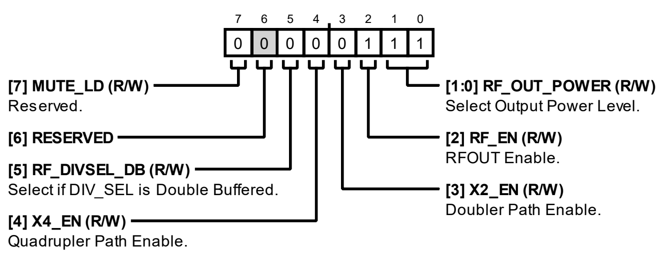


Table 36. Bit Descriptions for REG0025

Bit(s)	Bit Name	Description	Default	Access
7	MUTE_LD	Reserved.	0x0	R/W
6	RESERVED	Reserved.	0x0	R
5	RF_DIVSEL_DB	Select if DIV_SEL is Double Buffered.	0x0	R/W
4	X4_EN	Quadrupler Path Enable. 0: RF quadrupler off. 1: RF quadrupler on.	0x0	R/W
3	X2_EN	Doubler Path Enable. 0: RF doubler off. 1: RF doubler on.	0x0	R/W
2	RF_EN	RF_{OUT} Enable. 0: RF8P and RF8N are disabled. 1: RF8P and RF8N are enabled.	0x1	R/W
[1:0]	RF_OUT_POWER	Select Output Power Level. 0: −4 dBm. 1: −1 dBm. 10: 2 dBm. 11: 5 dBm.	0x3	R/W

Address: 0x26, Default: 0x32, Name: REG0026

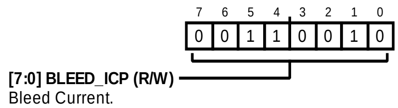


Table 37. Bit Descriptions for REG0026

Bit(s)	Bit Name	Description	Default	Access
[7:0]	BLEED_ICP	Bleed Current. Sets the bleed current. The optimum bleed current is set by $((4/N) \times I_{CP})/3.75$, where I_{CP} is the charge pump current in µA.	0x32	R/W

Address: 0x27, Default: 0xC5, Name: REG0027

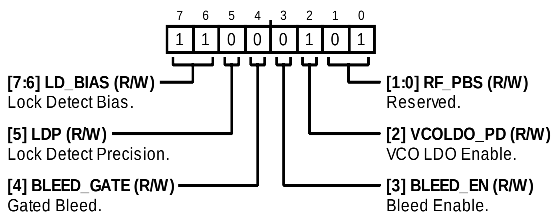


Table 38. Bit Descriptions for REG0027

Bit(s)	Bit Name	Description	Default	Access
[7:6]	LD_BIAS	Lock Detect Bias. The lock detector window size is set by adjusting the lock detector bias in conjunction with the lock detector precision. 0: 5 ns lock detect delay if LDP = 0. 1: 6 ns. 10: 8 ns. 11: 12 ns lock detect delay (for large values of bleed)	0x3	R/W
5	LDP	Lock Detect Precision. Controls the sensitivity of the digital lock detector, depending on INT or FRAC operation selected. 0: FRAC Mode (5 ns). 1: INT Mode (2.4 ns).	0x0	R/W
4	BLEED_GATE	Gated Bleed. 0: gate bleed disabled. 1: gate bleed on, digital lock detect (digital lock detect must be enabled)	0x0	R/W
3	BLEED_EN	Bleed Enable. Bleed current applies to a current inside the charge pump to improve the linearity of the charge pump. This current leads to lower phase noise and improved spurious performance. Set to 1 to enable negative bleed. 0: negative bleed disabled. 1: negative bleed enabled.	0x0	R/W
2	VCOLDO_PD	VCO LDO Enable. For optimal spurious and phase noise performance, disable VCO LDO. 0:VCO LDO enabled. 1: VCO LDO disabled.	0x1	R/W
[1:0]	RF_PBS	Reserved.	0x1	R/W

Address: 0x28, Default: 0x03, Name: REG0028

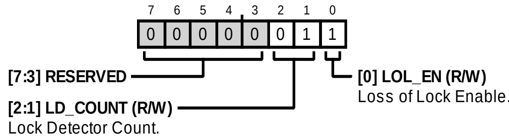


Table 39. Bit Descriptions for REG0028

Bit(s)	Bit Name	Description	Default	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:1]	LD_COUNT	Lock Detector Count. Initial value of the lock detector. This field sets the number of counts of PFD within lock window before asserting digital lock detect high. 0: 1024 cycles. 1: 2048 cycles. 10: 4096 cycles. 11: 8192 cycles.	0x1	R/W
0	LOL_EN	Loss of Lock Enable. When loss of lock is enabled, if digital lock detect is asserted, and the reference signal is removed, digital lock detect goes low. It is recommended to set to 1 to enable loss of lock. 0: disabled. 1: loss of lock enabled.	0x1	R/W

Address: 0x2A, Default: 0x00, Name: REG002A

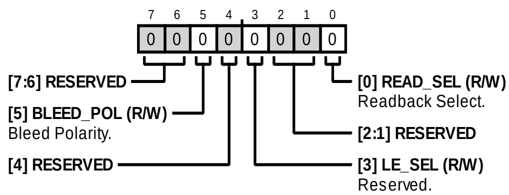


Table 40. Bit Descriptions for REG002A

Bit(s)	Bit Name	Description	Default	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	BLEED_POL	Bleed Polarity. Controls the polarity of the bleed current. Negative is typical usage. 0: negative bleed. 1: positive bleed (not recommended).	0x0	R/W
4	RESERVED	Reserved.	0x0	R
3	LE_SEL	Reserved.	0x0	R/W
[2:1]	RESERVED	Reserved.	0x0	R
0	READ_SEL	Readback Select. Selects the value to be read back. 0: readback VCO, band, and bias compensation data. 1: readback device version ID.	0x0	R/W

Address: 0x2B, Default: 0x01, Name: REG002B

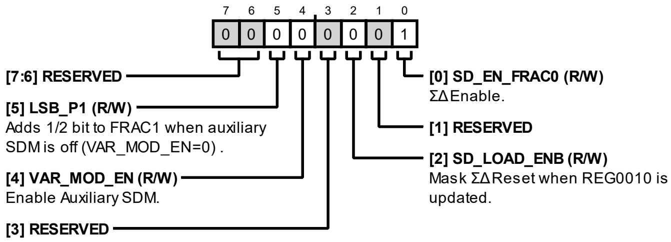


Table 41. Bit Descriptions for REG002B

Bit(s)	Bit Name	Description	Default	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	LSB_P1	Adds a half bit to FRAC1 when auxiliary SDM is off (VAR_MOD_EN = 0). Set to 0 for normal operation.	0x0	R/W
4	VAR_MOD_EN	Enable Auxiliary SDM. If FRAC2 is different than 0, programmed this bit to 1. 0: normal operation. 1: enable auxiliary SDM.	0x0	R/W
3	RESERVED	Reserved.	0x0	R
2	SD_LOAD_ENB	Mask ΣΔ Reset when REG0010 is updated. 0: reset ΣΔ when REG0010 is updated. 1: do not reset ΣΔ when REG0010 is updated.	0x0	R/W
1	RESERVED	Reserved.	0x0	R
0	SD_EN_FRAC0	ΣΔ Enable. Set to 1 when in INT mode (when FRAC1 = FRAC2 = 0), and set to 0 when in FRAC mode. 0: ΣΔ enabled (for fractional mode). 1: ΣΔ disabled (for integer mode).	0x1	R/W

Address: 0x2C, Default: 0x44, Name: REG002C

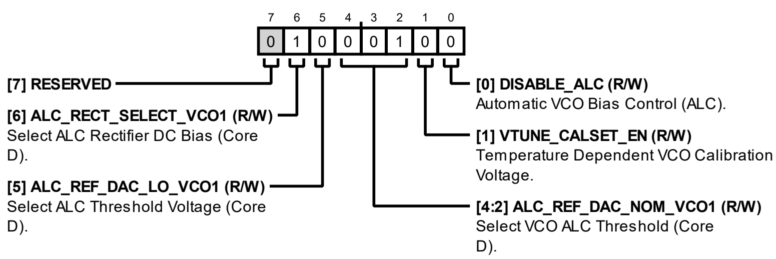


Table 42. Bit Descriptions for REG002C

Bit(s)	Bit Name	Description	Default	Access
7	RESERVED	Reserved.	0x0	R
6	ALC_RECT_SELECT_VCO1	Select ALC Rectifier DC Bias (Core D). 0: 3.3 V VCO operation. 1: 5 V VCO operation.	0x1	R/W
5	ALC_REF_DAC_LO_VCO1	Select ALC Threshold Voltage (Core D). 0: 5 V VCO operation. 1: 3.3 V VCO operation.	0x0	R/W
[4:2]	ALC_REF_DAC_NOM_VCO1	Select VCO ALC Threshold (Core D). 001: 3.3 V and 5 V VCO operation.	0x1	R/W
1	VTUNE_CALSET_EN	Temperature Dependent VCO Calibration Voltage. 0: disable temperature dependent VCO calibration voltage. 1: enable temperature dependent VCO calibration voltage.	0x0	R/W
0	DISABLE_ALC	Automatic VCO Bias Control (ALC). 0: ALC enabled. 1: ALC disabled.	0x0	R/W

Address: 0x2D, Default: 0x11, Name: REG002D

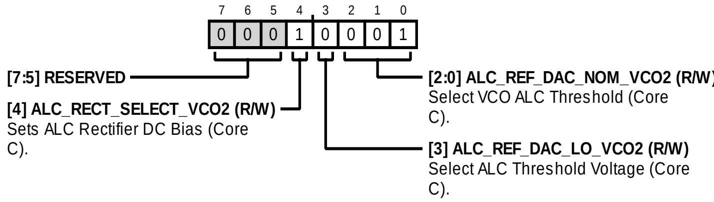


Table 43. Bit Descriptions for REG002D

Bit(s)	Bit Name	Description	Default	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	ALC_RECT_SELECT_VCO2	Sets ALC Rectifier DC Bias (Core C). 0: 3.3 V VCO operation. 1: 5 V VCO operation.	0x1	R/W
3	ALC_REF_DAC_LO_VCO2	Select ALC Threshold Voltage (Core C). 0: 5 V VCO operation. 1: 3.3 V VCO operation.	0x0	R/W
[2:0]	ALC_REF_DAC_NOM_VCO2	Select VCO ALC Threshold (Core C). 001: 5 V VCO operation. 010: 3.3 V VCO operation.	0x1	R/W

Address: 0x2E, Default: 0x10, Name: REG002E

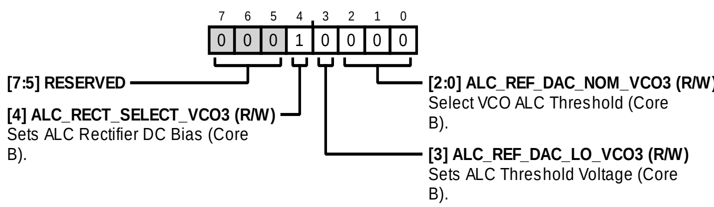


Table 44. Bit Descriptions for REG002E

Bit(s)	Bit Name	Description	Default	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	ALC_RECT_SELECT_VCO3	Sets ALC Rectifier DC Bias (Core B). 0: 3.3 V VCO operation. 1: 5 V VCO operation.	0x1	R/W
3	ALC_REF_DAC_LO_VCO3	Sets ALC Threshold Voltage (Core B). 0: 5 V VCO operation. 1: 3.3 V VCO operation.	0x0	R/W
[2:0]	ALC_REF_DAC_NOM_VCO3	Select VCO ALC Threshold (Core B). 000: 5 V VCO operation. 010: 3.3 V VCO operation.	0x0	R/W

Address: 0x2F, Default: 0x92, Name: REG002F

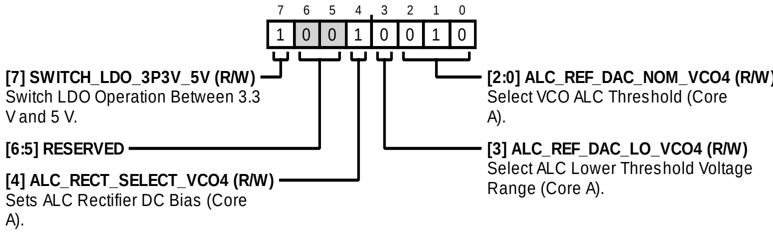


Table 45. Bit Descriptions for REG002F

Bit(s)	Bit Name	Description	Default	Access
7	SWITCH_LDO_3P3V_5V	Switch LDO Operation Between 3.3 V and 5 V. 0: 3.3 V VCO operation. 1: 5 V VCO operation.	0x1	R/W
[6:5]	RESERVED	Reserved.	0x0	R
4	ALC_RECT_SELECT_VCO4	Sets ALC Rectifier DC Bias (Core A). 0: 3.3 V VCO operation. 1: 5 V VCO operation.	0x1	R/W
3	ALC_REF_DAC_LO_VCO4	Select ALC Lower Threshold Voltage Range (Core A). 0: 5 V VCO operation. 1: 3.3 V VCO operation.	0x0	R/W
[2:0]	ALC_REF_DAC_NOM_VCO4	Select VCO ALC Threshold (Core A). 010: 3.3 V and 5 V VCO operation.	0x2	R/W

Address: 0x30, Default: 0x3F, Name: REG0030

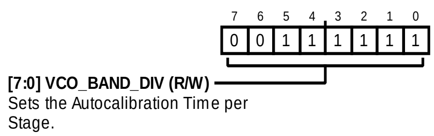


Table 46. Bit Descriptions for REG0030

Bit(s)	Bit Name	Description	Default	Access
[7:0]	VCO_BAND_DIV	Sets the Autocalibration Time per Stage. See the Lock Time section for details.	0x3F	R/W

Address: 0x31, Default: 0xA7, Name: REG0031

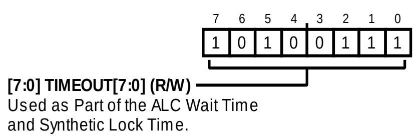


Table 47. Bit Descriptions for REG0031

Bit(s)	Bit Name	Description	Default	Access
[7:0]	TIMEOUT[7:0]	Used as Part of the ALC Wait Time and Synthetic Lock Time. See the Lock Time section for details.	0xA7	R/W

Address: 0x32, Default: 0x04, Name: REG0032

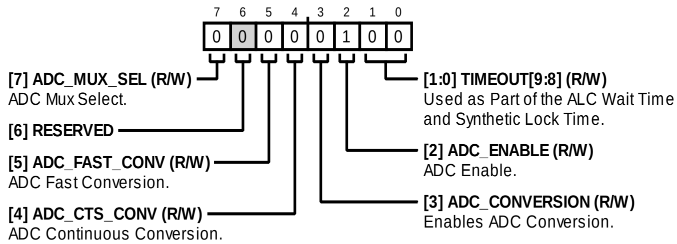


Table 48. Bit Descriptions for REG0032

Bit(s)	Bit Name	Description	Default	Access
7	ADC_MUX_SEL	Analog-to-Digital Converter (ADC) Mux Select. 0: proportional to absolute temperature (PTAT) voltage muxed to ADC input. 1: scaled VTUNE voltage muxed to ADC input.	0x0	R/W
6	RESERVED	Reserved.	0x0	R
5	ADC_FAST_CONV	ADC Fast Conversion. 0: disabled. 1: enabled.	0x0	R/W
4	ADC_CTS_CONV	ADC Continuous Conversion. 0: disabled. 1: enabled.	0x0	R/W
3	ADC_CONVERSION	Enables ADC Conversion. 0: no ADC conversion. 1: perform ADC conversion on REG0000 write if ADC is enabled.	0x0	R/W
2	ADC_ENABLE	ADC Enable. 0: disabled. 1: enabled.	0x1	R/W
[1:0]	TIMEOUT[9:8]	Used as Part of the ALC Wait Time and Synthetic Lock Time. See the Lock Time section for details.	0x0	R/W

Address: 0x33, Default: 0x0C, Name: REG0033

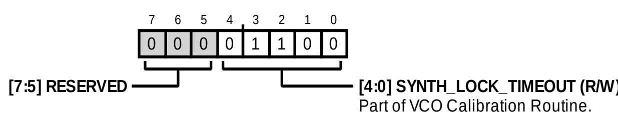


Table 49. Bit Descriptions for REG0033

Bit(s)	Bit Name	Description	Default	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	SYNTH_LOCK_TIMEOUT	Part of VCO Calibration Routine. See the Lock Time section for details.	0xC	R/W

Address: 0x34, Default: 0x9E, Name: REG0034

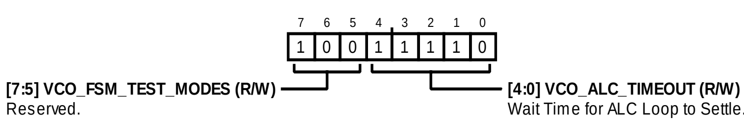


Table 50. Bit Descriptions for REG0034

Bit(s)	Bit Name	Description	Default	Access
[7:5]	VCO_FSM_TEST_MODES	Reserved.	0x4	R/W
[4:0]	VCO_ALC_TIMEOUT	Wait Time for ALC Loop to Settle. See the Lock Time section for details.	0x1E	R/W

Address: 0x35, Default: 0x4C, Name: REG0035

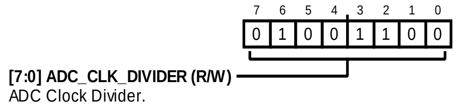


Table 51. Bit Descriptions for REG0035

Bit(s)	Bit Name	Description	Default	Access
[7:0]	ADC_CLK_DIVIDER	ADC Clock Divider. ADC_CLK = f_{PFD}/((ADC_CLK_DIV × 4) + 2). Target 100 kHz for ADC_CLK. Refer to AN-2005 for more details.	0x4C	R/W

Address: 0x36, Default: 0x30, Name: REG0036

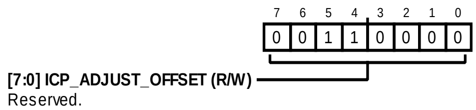


Table 52. Bit Descriptions for REG0036

Bit(s)	Bit Name	Description	Default	Access
[7:0]	ICP_ADJUST_OFFSET	Reserved.	0x30	R/W

Address: 0x37, Default: 0x00, Name: REG0037

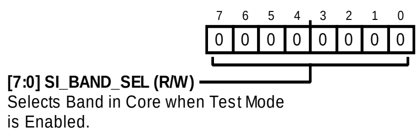


Table 53. Bit Descriptions for REG0037

Bit(s)	Bit Name	Description	Default	Access
[7:0]	SI_BAND_SEL	Selects Band in Core when Test Mode is Enabled.	0x0	R/W

Address: 0x38, Default: 0x00, Name: REG0038

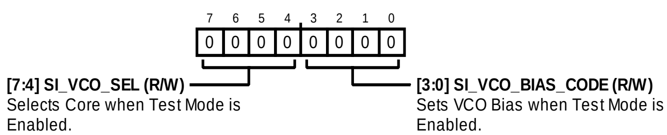


Table 54. Bit Descriptions for REG0038

Bit(s)	Bit Name	Description	Default	Access
[7:4]	SI_VCO_SEL	Selects Core when Test Mode is Enabled. 0: all cores off. 1: VCO Core D. 10: VCO Core C. 100: VCO Core B. 1000: VCO Core A.	0x0	R/W
[3:0]	SI_VCO_BIAS_CODE	Sets VCO Bias when Test Mode is Enabled. 0000: maximum VCO bias (approximately 3.2 V). 1111: minimum VCO bias (approximately 1.8 V).	0x0	R/W

Address: 0x39, Default: 0x07, Name: REG0039

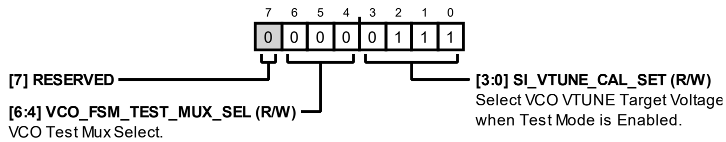


Table 55. Bit Descriptions for REG0039

Bit(s)	Bit Name	Description	Default	Access
7	RESERVED	Reserved.	0x0	R
[6:4]	VCO_FSM_TEST_MUX_SEL	VCO Test Mux Select. 0: busy. 1: N band. 10: R band. 11: reserved. 100: timeout clock. 101: bias minimum. 110: ADC busy. 111: logic low.	0x0	R/W
[3:0]	SI_VTUNE_CAL_SET	Select VCO VTUNE Target Voltage when Test Mode is Enabled. 0: 1.18 V. 1: 1.18 V. 10: 1.18 V. 11: 1.18 V. 100: 1.33 V. 101: 1.48 V. 110: 1.63 V. 111: 1.78 V. 1000: 1.93 V. 1001: 2.08 V. 1010: 2.23 V. 1011: 2.38 V. 1100: 2.53 V. 1101: 2.53 V. 1110: 2.53 V. 1111: 2.53 V.	0x7	R/W

Address: 0x3A, Default: 0x55, Name: REG003A

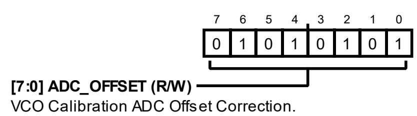


Table 56. Bit Descriptions for REG003A

Bit(s)	Bit Name	Description	Default	Access
[7:0]	ADC_OFFSET	VCO Calibration ADC Offset Correction.	0x55	R/W

Address: 0x3D, Default: 0x00, Name: REG003D

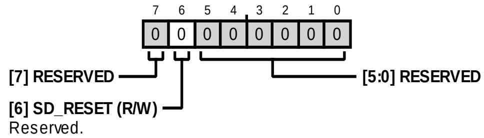


Table 57. Bit Descriptions for REG003D

Bit(s)	Bit Name	Description	Default	Access
7	RESERVED	Reserved.	0x0	R
6	SD_RESET	Reserved.	0x0	R/W
[5:0]	RESERVED	Reserved.	0x0	R

Address: 0x3E, Default: 0x0C, Name: REG003E

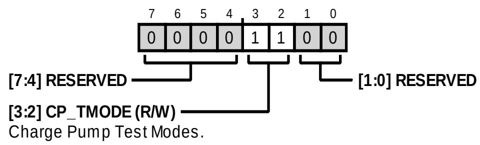


Table 58. Bit Descriptions for REG003E

Bit(s)	Bit Name	Description	Default	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:2]	CP_TMODE	Charge Pump (CP) Test Modes 0: CP tristate 11: normal operation	0x3	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x3F, Default: 0x80, Name: REG003F

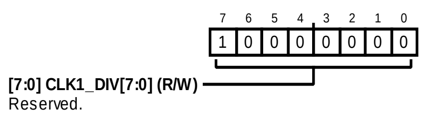


Table 59. Bit Descriptions for REG003F

Bit(s)	Bit Name	Description	Default	Access
[7:0]	CLK1_DIV[7:0]	Reserved.	0x80	R/W

Address: 0x40, Default: 0x50, Name: REG0040

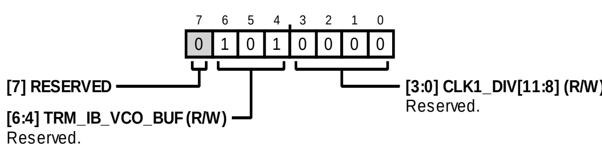


Table 60. Bit Descriptions for REG0040

Bit(s)	Bit Name	Description	Default	Access
7	RESERVED	Reserved.	0x0	R
[6:4]	TRM_IB_VCO_BUF	Reserved.	0x5	R/W
[3:0]	CLK1_DIV[11:8]	Reserved.	0x0	R/W

Address: 0x41, Default: 0x28, Name: REG0041

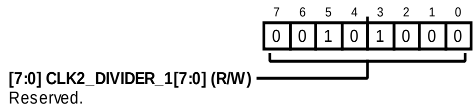


Table 61. Bit Descriptions for REG0041

Bit(s)	Bit Name	Description	Default	Access
[7:0]	CLK2_DIVIDER_1[7:0]	Reserved.	0x28	R/W

Address: 0x42, Default: 0x00, Name: REG0042

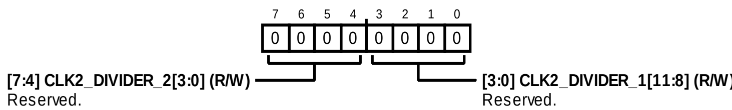


Table 62. Bit Descriptions for REG0042

Bit(s)	Bit Name	Description	Default	Access
[7:4]	CLK2_DIVIDER_2	Reserved.	0x0	R/W
[3:0]	CLK2_DIVIDER_1[11:8]	Reserved.	0x0	R/W

Address: 0x47, Default: 0xC0, Name: REG0047

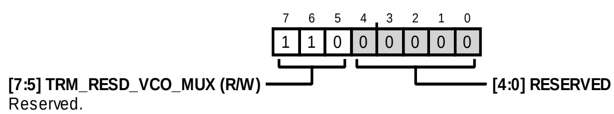


Table 63. Bit Descriptions for REG0047

Bit(s)	Bit Name	Description	Default	Access
[7:5]	TRM_RESD_VCO_MUX	Reserved.	0x6	R/W
[4:0]	RESERVED	Reserved.	0x0	R

Address: 0x52, Default: 0xF4, Name: REG0052

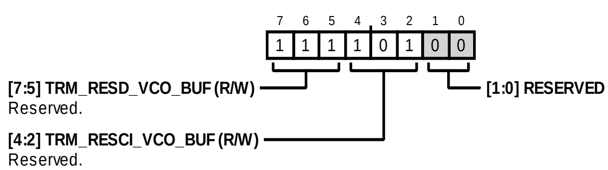


Table 64. Bit Descriptions for REG0052

Bit(s)	Bit Name	Description	Default	Access
[7:5]	TRM_RESD_VCO_BUF	Reserved. VCO buffer trim.	0x7	R/W
[4:2]	TRM_RESCI_VCO_BUF	Reserved.	0x5	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x6E, Default: 0x00, Name: REG006E

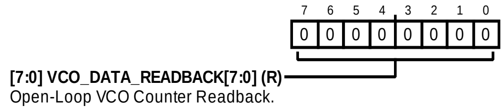


Table 65. Bit Descriptions for REG006E

Bit(s)	Bit Name	Description	Default	Access
[7:0]	VCO_DATA_READBACK[7:0]	Open-Loop VCO Counter Readback.	0x0	R

Address: 0x6F, Default: 0x00, Name: REG006F

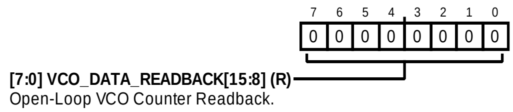


Table 66. Bit Descriptions for REG006F

Bit(s)	Bit Name	Description	Default	Access
[7:0]	VCO_DATA_READBACK[15:8]	Open-Loop VCO Counter Readback.	0x0	R

Address: 0x70, Default: 0x03, Name: REG0070

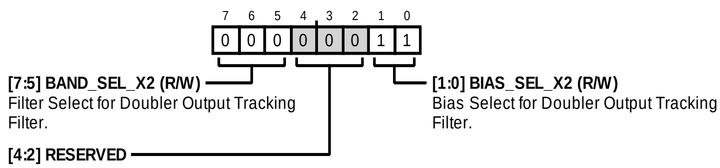


Table 67. Bit Descriptions for REG0070

Bit(s)	Bit Name	Description	Default	Access
[7:5]	BAND_SEL_X2	Filter Select for Doubler Output Tracking Filter.	0x0	R/W
[4:2]	RESERVED	Reserved.	0x0	R
[1:0]	BIAS_SEL_X2	Bias Select for Doubler Output Tracking Bias.	0x3	R/W

Address: 0x71, Default: 0x60, Name: REG0071

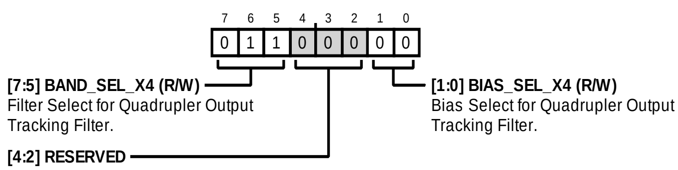


Table 68. Bit Descriptions for REG0071

Bit(s)	Bit Name	Description	Default	Access
[7:5]	BAND_SEL_X4	Filter Select for Quadrupler Output Tracking Filter.	0x3	R/W
[4:2]	RESERVED	Reserved.	0x0	R
[1:0]	BIAS_SEL_X4	Bias Select for Quadrupler Output Tracking Bias.	0x0	R/W

Address: 0x72, Default: 0x32, Name: REG0072

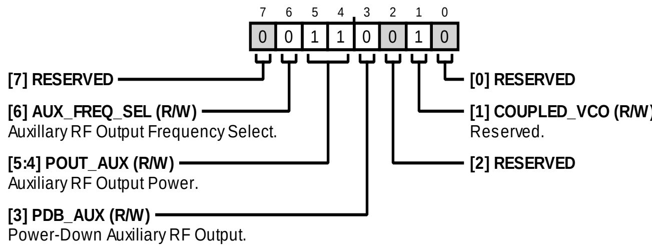


Table 69. Bit Descriptions for REG0072

Bit(s)	Bit Name	Description	Default	Access
7	RESERVED	Reserved.	0x0	R
6	AUX_FREQ_SEL	Auxiliary RF Output Frequency Select. 0: divided output. 1: VCO output.	0x0	R/W
[5:4]	POUT_AUX	Auxiliary RF Output Power. Sets the output power at the auxiliary RF output ports. 0: −4.5 dBm single-ended ÷ −1.5 dBm differential. 1: 1 dBm single-ended ÷ 4 dBm differential. 10: 4 dBm single-ended ÷ 7 dBm differential. 11: 6 dBm single-ended ÷ 9 dBm differential.	0x3	R/W
3	PDB_AUX	Power-Down Auxiliary RF Output. 0: auxiliary RF off. 1: auxiliary RF on.	0x0	R/W
2	RESERVED	Reserved.	0x0	R
1	COUPLED_VCO	Reserved.	0x1	R/W
0	RESERVED	Reserved.	0x0	R

Address: 0x73, Default: 0x00, Name: REG0073

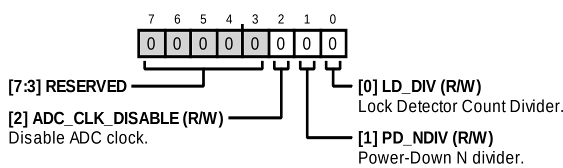


Table 70. Bit Descriptions for REG0073

Bits	Bit Name	Description	Default	Access
[7:3]	RESERVED	Reserved.	0x0	R
2	ADC_CLK_DISABLE	Disable ADC Clock. ADC_ENABLE setting overwrites this bit.	0x0	R/W
1	PD_NDIV	Power-Down N Divider.	0x0	R/W
0	LD_DIV	Lock Detector Count Divider. Divides the lock detector count cycles by 32 so that the LD_COUNT bits in REG0028 can be selected as 32, 64, 128, and 256.	0x0	R/W

Address: 0x7C, Default: 0x00, Name: REG007C

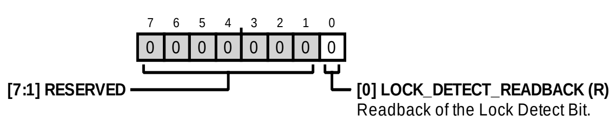


Table 71. Bit Descriptions for REG007C

Bit(s)	Bit Name	Description	Default	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	LOCK_DETECT_READBACK	Readback of the Lock Detect Bit.	0x0	R

OUTLINE DIMENSIONS

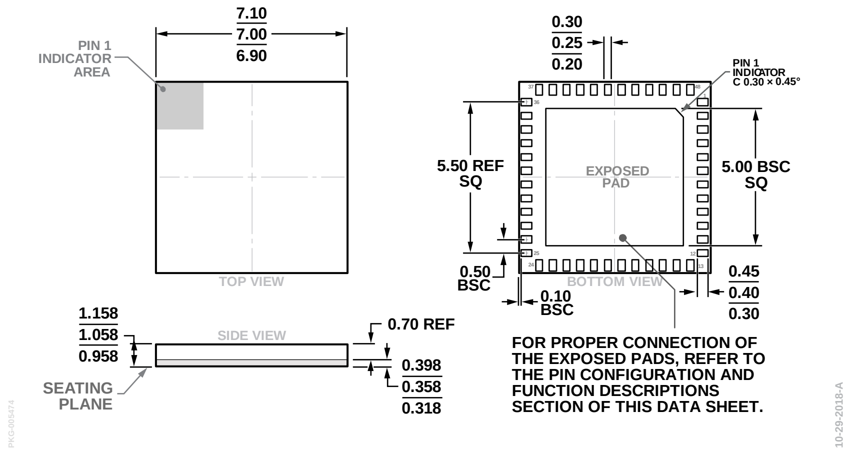


Figure 45. 48-Terminal Land Grid Array [LGA]
(CC-48-4)
Dimensions shown in millimeters

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Model[1]	Temperature Range	Package Description	Package Option
ADF4371BCCZ	−40°C to +105°C	48-Terminal Land Grid Array [LGA]	CC-48-4
ADF4371BCCZ-RL7	−40°C to +105°C	48-Terminal Land Grid Array [LGA]	CC-48-4
EV-ADF4371SD2Z		Evaluation Board	

[1] Z = RoHS Compliant Part.