

## FEATURES

- 1 pF off capacitance
- 2.6 pF on capacitance
- <1 pC charge injection
- 33 V supply range
- 120  $\Omega$  on resistance
- Fully specified at  $\pm 15$  V, +12 V
- No  $V_L$  supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 16-lead TSSOP and 16-lead LFCSP
- Typical power consumption: <0.03  $\mu$ W

## APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Audio signal routing
- Video signal routing
- Communication systems

## GENERAL DESCRIPTION

The [ADG1211/ADG1212/ADG1213](#) are monolithic complementary metal-oxide semiconductor (CMOS) devices containing four independently selectable switches designed on an *i*CMOS<sup>®</sup> (industrial CMOS) process. *i*CMOS is a modular manufacturing process combining high voltage CMOS and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage devices has been able to achieve.

Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth make the devices suitable for video signal switching.

*i*CMOS construction ensures ultralow power dissipation, making the devices ideally suited for portable and battery-powered instruments.

## FUNCTIONAL BLOCK DIAGRAM

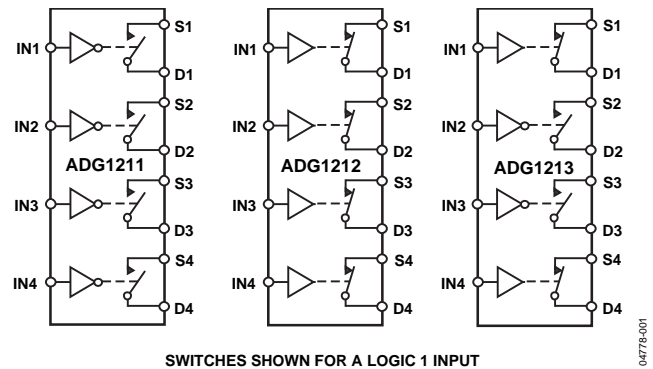


Figure 1.

The [ADG1211/ADG1212/ADG1213](#) contain four independent single-pole/single-throw (SPST) switches. The [ADG1211](#) and [ADG1212](#) differ only in that the digital control logic is inverted. The [ADG1211](#) switches are turned on with Logic 0 on the appropriate control input, while Logic 1 is required for the [ADG1212](#). The [ADG1213](#) has two switches with digital control logic similar to that of the [ADG1211](#); the logic is inverted on the other two switches. The [ADG1213](#) exhibits break-before-make switching action for use in multiplexer applications.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

## PRODUCT HIGHLIGHTS

1. Ultralow capacitance.
2. <1 pC charge injection.
3. 3 V logic-compatible digital inputs:  $V_{IH} = 2.0$  V,  $V_{IL} = 0.8$  V.
4. No  $V_L$  logic power supply required.
5. Ultralow power dissipation: <0.03  $\mu$ W.
6. 16-lead TSSOP and 3 mm  $\times$  3 mm LFCSP packages.

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**REVISION HISTORY**

<b>11/2016—Rev. C to Rev. D</b>		<b>2/2009—Rev. 0 to Rev. A</b>	
Change to VDD Parameter, Table 2 .....	5	Changes to Power Requirements, I <sub>DD</sub> , Digital Inputs = 5 V	
		Parameter, Table 1 .....	4
<b>3/2016—Rev. B to Rev. C</b>		Changes to Power Requirements, I <sub>DD</sub> , Digital Inputs = 5 V	
Changes to Figure 3 .....	7	Parameter, Table 2 .....	5
Updated Outline Dimensions .....	14		
Changes to Ordering Guide .....	15	<b>7/2005—Revision 0: Initial Version</b>	
<b>8/2012—Rev. A to Rev. B</b>			
Changes to Table 1 .....	3		
Changes to Table 2.....	5		
Change to Table 6 .....	7		
Updated Outline Dimensions .....	14		
Changes to Ordering Guide .....	15		

## SPECIFICATIONS

## DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

Table 1.

Parameter	Y Version <sup>1</sup>			Unit	Test Conditions/Comments
	25°C	-40°C to +85°C	-40°C to +125°C		
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	
On Resistance ( $R_{ON}$ )	120			$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -1\text{ mA}$ ; see Figure 20
	190	230	260	$\Omega$ max	$V_{DD} = +13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	2.5			$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -1\text{ mA}$
On Resistance Flatness ( $R_{FLAT(ON)}$ )	6	10	11	$\Omega$ max	
	20			$\Omega$ typ	$V_S = -5\text{ V}/0\text{ V}/+5\text{ V}$ ; $I_S = -1\text{ mA}$
	57	72	79	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.02$			nA typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$
	$\pm 0.1$	$\pm 0.6$	$\pm 1$	nA max	$V_S = \pm 10\text{ V}$ , $V_D = \mp 10\text{ V}$ ; see Figure 21
Drain Off Leakage, $I_D$ (Off)	$\pm 0.02$			nA typ	$V_S = \pm 10\text{ V}$ , $V_D = \mp 10\text{ V}$ ; see Figure 21
	$\pm 0.1$	$\pm 0.6$	$\pm 1$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.02$			nA typ	$V_S = V_D = \pm 10\text{ V}$ ; see Figure 22
	$\pm 0.1$	$\pm 0.6$	$\pm 1$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	2.5			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
$t_{ON}$	110			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	130	160	195	ns max	$V_S = 10\text{ V}$ ; see Figure 23
$t_{OFF}$	85			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	115	130	150	ns max	$V_S = 10\text{ V}$ ; see Figure 23
Break-Before-Make Time Delay, $t_D$ (ADG1213 Only)	25		10	ns typ ns min	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 10\text{ V}$ ; see Figure 24
Charge Injection	-0.3			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 25
Off Isolation	80			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 26
Channel-to-Channel Crosstalk	90			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 27
Total Harmonic Distortion + Noise	0.15			% typ	$R_L = 10\text{ k}\Omega$ , $5\text{ V rms}$ , $f = 20\text{ Hz}$ to $20\text{ kHz}$
-3 dB Bandwidth	1000			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 28
$C_S$ (Off)	0.9			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
	1.1			pF max	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	1			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
	1.2			pF max	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	2.6			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
	3			pF max	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$

Parameter	25°C	Y Version <sup>1</sup>		Unit	Test Conditions/Comments
		-40°C to +85°C	-40°C to +125°C		
POWER REQUIREMENTS					$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$
$I_{DD}$	0.001		1.0	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 0 V or $V_{DD}$
$I_{DD}$	220		380	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 5 V
$I_{SS}$	0.001		1.0	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 0 V or $V_{DD}$
$I_{SS}$	0.001		1.0	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 5 V
VDD/VSS			$\pm 4.5/\pm 16.5$	V min/max	

<sup>1</sup> Temperature range for Y version is -40°C to +125°C.

<sup>2</sup> Guaranteed by design, not subject to production test.

**SINGLE SUPPLY**

$V_{DD} = 12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 2.**

Parameter	Y Version <sup>1</sup>			Unit	Test Conditions/Comments
	25°C	–40°C to +85°C	–40°C to +125°C		
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	300			$\Omega$ typ	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -1\text{ mA}$ ; see Figure 20
	475	567	625	$\Omega$ max	$V_{DD} = 10.8\text{ V}$ , $V_{SS} = 0\text{ V}$
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	4.5			$\Omega$ typ	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -1\text{ mA}$
	12	26	27	$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	60			$\Omega$ typ	$V_S = 3\text{ V}/6\text{ V}/9\text{ V}$ , $I_S = -1\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.02$			nA typ	$V_{DD} = 13.2\text{ V}$ , $V_{SS} = 0\text{ V}$
	$\pm 0.1$	$\pm 0.6$	$\pm 1$	nA max	$V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ ; see Figure 21
Drain Off Leakage, $I_D$ (Off)	$\pm 0.02$			nA typ	$V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ ; see Figure 21
	$\pm 0.1$	$\pm 0.6$	$\pm 1$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.02$			nA typ	$V_S = V_D = 1\text{ V or }10\text{ V}$ ; see Figure 22
	$\pm 0.1$	$\pm 0.6$	$\pm 1$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.001			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	3			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
$t_{ON}$	130			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	170	210	240	ns max	$V_S = 8\text{ V}$ ; see Figure 23
$t_{OFF}$	95			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	120	145	180	ns max	$V_S = 8\text{ V}$ ; see Figure 23
Break-Before-Make Time Delay, $t_D$ (ADG1213 Only)	50		10	ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
				ns min	$V_{S1} = V_{S2} = 8\text{ V}$ ; see Figure 24
Charge Injection	0			pC typ	$V_S = 6\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 25
Off Isolation	80			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 26
Channel-to-Channel Crosstalk	90			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 27
–3 dB Bandwidth	900			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 28
$C_S$ (Off)	1.2			pF typ	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
	1.4			pF max	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	1.3			pF typ	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
	1.5			pF max	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	3.2			pF typ	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
	3.9			pF max	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = 13.2\text{ V}$
			1.0	$\mu\text{A}$ max	Digital inputs = 0 V or $V_{DD}$
$I_{DD}$	220			$\mu\text{A}$ typ	Digital inputs = 5 V
			1.0	$\mu\text{A}$ max	
VDD			5/16.5	V min/max	$V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$

<sup>1</sup> Temperature range for Y version is –40°C to +125°C.

<sup>2</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameter	Rating
$V_{DD}$ to $V_{SS}$	35 V
$V_{DD}$ to GND	-0.3 V to +25 V
$V_{SS}$ to GND	+0.3 V to -25 V
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs <sup>1</sup>	GND - 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current per Channel, S or D	25 mA
Operating Temperature Range Automotive (Y Version)	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, $\theta_{JA}$ Thermal Impedance (4-Layer Board)	112°C/W
16-Lead LFCSP, $\theta_{JA}$ Thermal Impedance	72.7°C/W
Reflow Soldering Peak Temperature, Pb free	260°C

<sup>1</sup> Overvoltages at IN, S, or D are clamped by internal diodes. Current must be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

**Table 4. ADG1211/ADG1212 Truth Table**

ADG1211 INx	ADG1212 INx	Switch Condition
0	1	On
1	0	Off

**Table 5. ADG1213 Truth Table**

ADG1213 INx	Switch 1, 4	Switch 2, 3
0	Off	On
1	On	Off

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

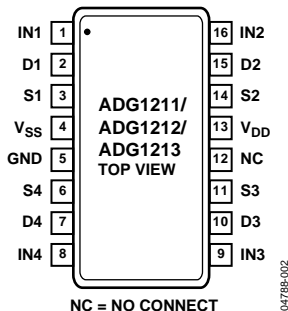
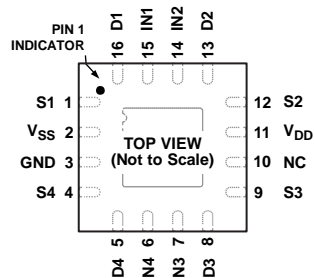


Figure 2. TSSOP Pin Configuration

ADG1211/ADG1212/ADG1213



- NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
  2. THE EXPOSED PAD MUST BE TIED TO SUBSTRATE,  $V_{SS}$ .

Figure 3. LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	15	IN1	Logic Control Input.
2	16	D1	Drain Terminal. Can be an input or output.
3	1	S1	Source Terminal. Can be an input or output.
4	2	$V_{SS}$	Most Negative Power Supply Potential.
5	3	GND	Ground (0 V) Reference.
6	4	S4	Source Terminal. Can be an input or output.
7	5	D4	Drain Terminal. Can be an input or output.
8	6	IN4	Logic Control Input.
9	7	IN3	Logic Control Input.
10	8	D3	Drain Terminal. Can be an input or output.
11	9	S3	Source Terminal. Can be an input or output.
12	10	NC	No Internal Connection.
13	11	$V_{DD}$	Most Positive Power Supply Potential.
14	12	S2	Source Terminal. Can be an input or output.
15	13	D2	Drain Terminal. Can be an input or output.
16	14	IN2	Logic Control Input.

## TERMINOLOGY

<b>I<sub>DD</sub></b>	The positive supply current.		
<b>I<sub>SS</sub></b>	The negative supply current.		
<b>V<sub>D</sub> (V<sub>S</sub>)</b>	The analog voltage on Terminals D and S.		
<b>R<sub>ON</sub></b>	The ohmic resistance between D and S.		
<b>R<sub>FLAT(ON)</sub></b>	Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.		
<b>I<sub>S</sub> (Off)</b>	The source leakage current with the switch off.		
<b>I<sub>D</sub> (Off)</b>	The drain leakage current with the switch off.		
<b>I<sub>D</sub>, I<sub>S</sub> (On)</b>	The channel leakage current with the switch on.		
<b>V<sub>INL</sub></b>	The maximum input voltage for Logic 0.		
<b>V<sub>INH</sub></b>	The minimum input voltage for Logic 1.		
<b>I<sub>INL</sub> (I<sub>INH</sub>)</b>	The input current of the digital input.		
<b>C<sub>S</sub> (Off)</b>	The off switch source capacitance, measured with reference to ground.		
<b>C<sub>D</sub> (Off)</b>	The off switch drain capacitance, measured with reference		
			to ground.
		<b>C<sub>D</sub>, C<sub>S</sub> (On)</b>	The on switch capacitance, measured with reference to ground.
		<b>C<sub>IN</sub></b>	The digital input capacitance.
		<b>t<sub>ON</sub></b>	The delay between applying the digital control input and the output switching on. See Figure 23.
		<b>t<sub>OFF</sub></b>	The delay between applying the digital control input and the output switching off. See Figure 23.
		<b>Charge Injection</b>	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
		<b>Off Isolation</b>	A measure of unwanted signal coupling through an off switch.
		<b>Crosstalk</b>	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
		<b>Bandwidth</b>	The frequency at which the output is attenuated by 3 dB.
		<b>On Response</b>	The frequency response of the on switch.
		<b>Insertion Loss</b>	The loss due to the on resistance of the switch.
		<b>THD + N</b>	The ratio of the harmonic amplitude plus noise of the signal to the fundamental.



TYPICAL PERFORMANCE CHARACTERISTICS

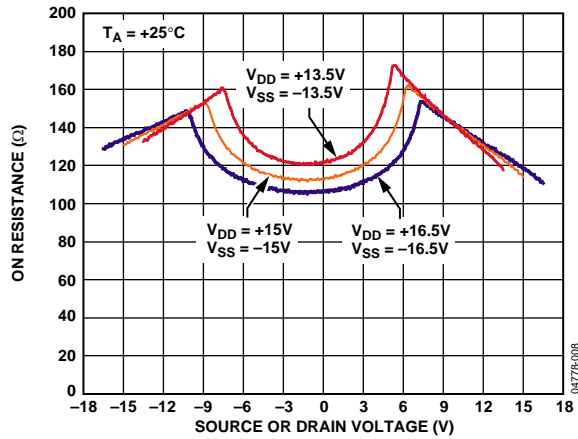


Figure 4. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Dual Supply

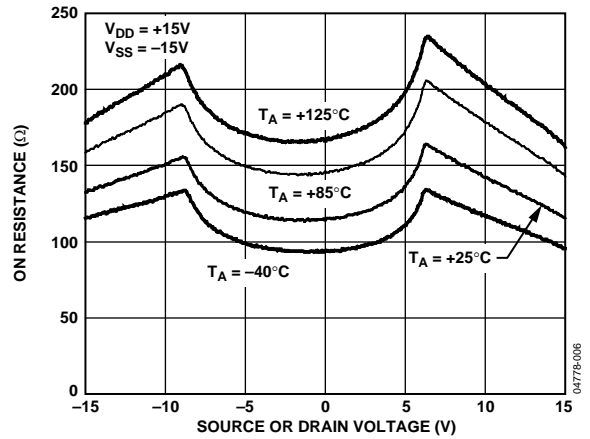


Figure 7. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, Dual Supply

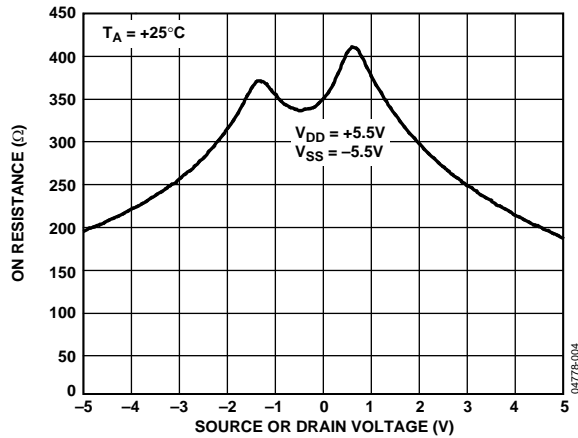


Figure 5. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Dual Supply

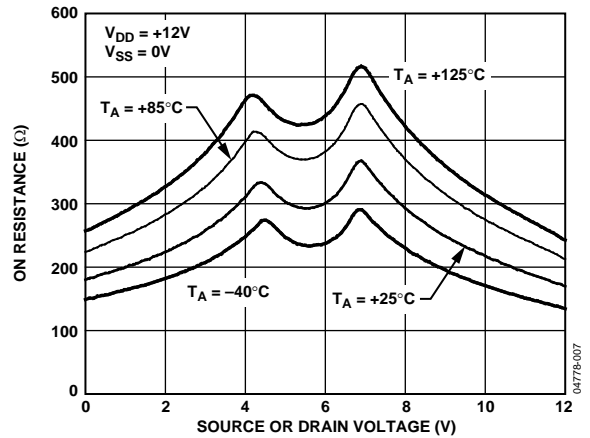


Figure 8. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, Single Supply

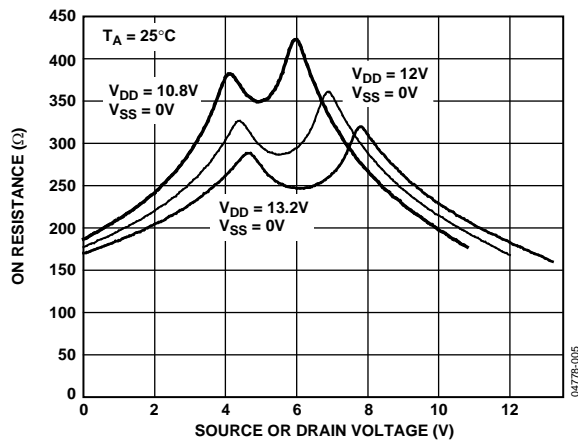


Figure 6. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Single Supply

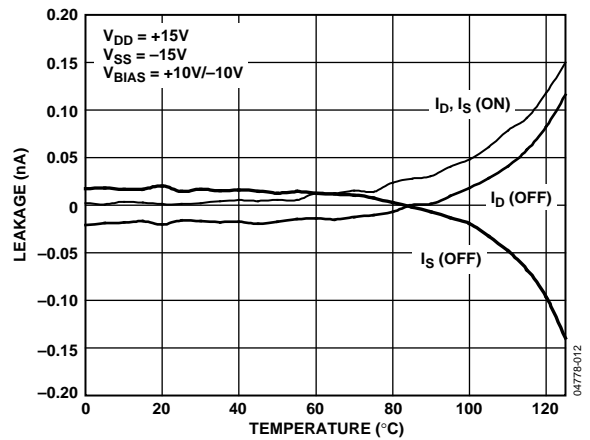


Figure 9. Leakage Currents as a Function of Temperature, Dual Supply

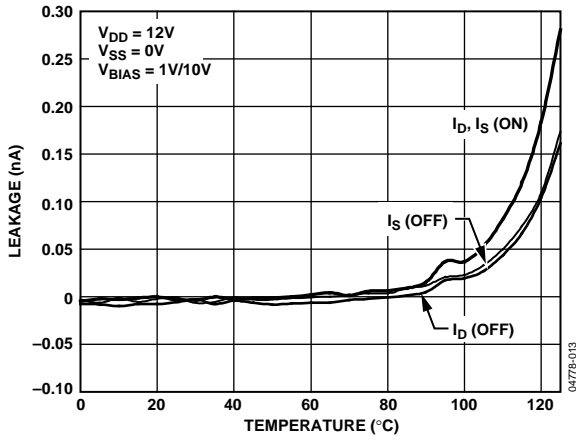


Figure 10. Leakage Currents as a Function of Temperature, Single Supply

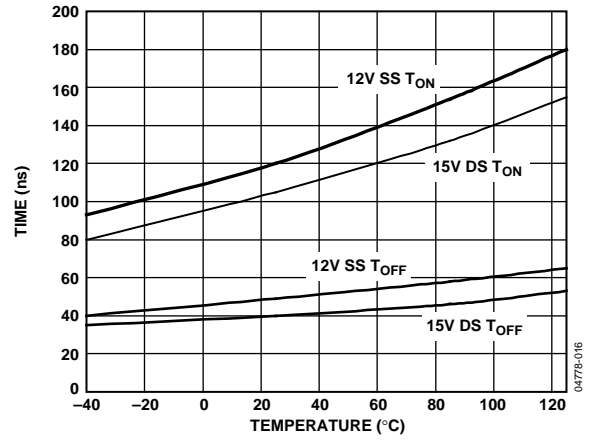


Figure 13.  $T_{ON}/T_{OFF}$  Times vs. Temperature

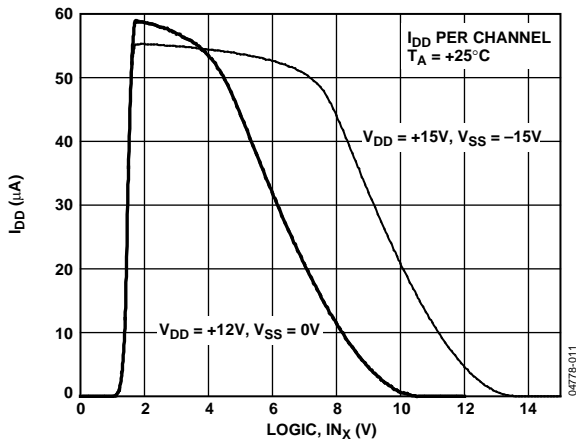


Figure 11.  $I_{DD}$  vs. Logic Level

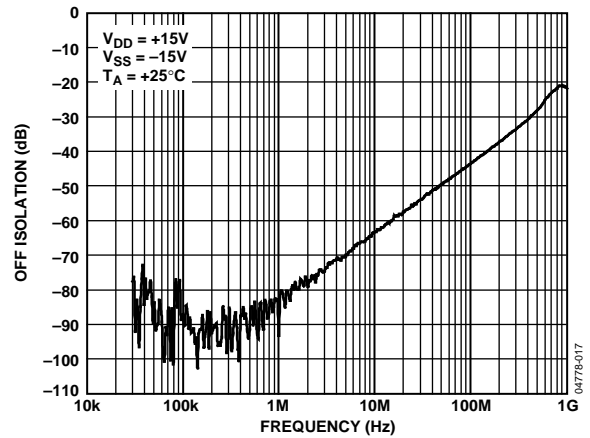


Figure 14. Off Isolation vs. Frequency

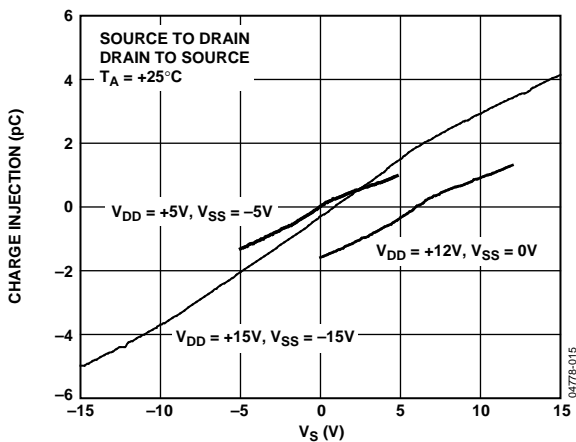


Figure 12. Charge Injection vs. Source Voltage

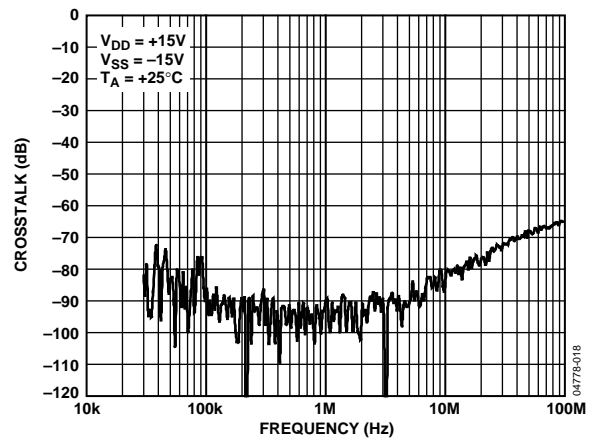


Figure 15. Crosstalk vs. Frequency

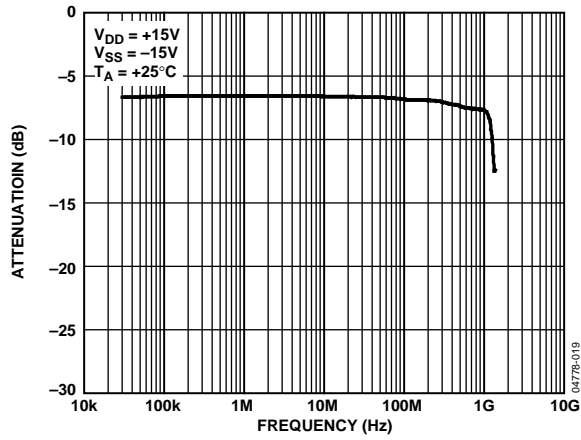


Figure 16. On Response vs. Frequency

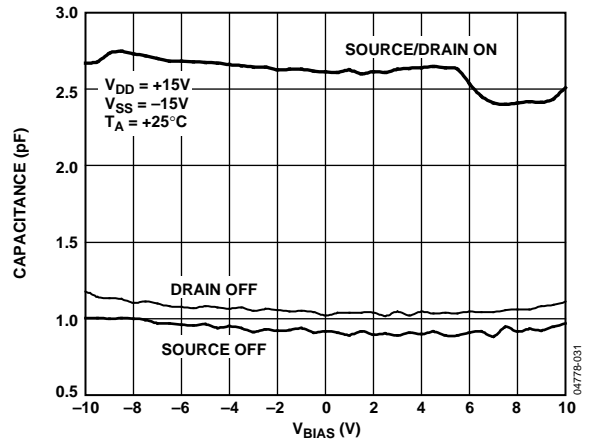


Figure 18. Capacitance vs. Source Voltage, Dual Supply

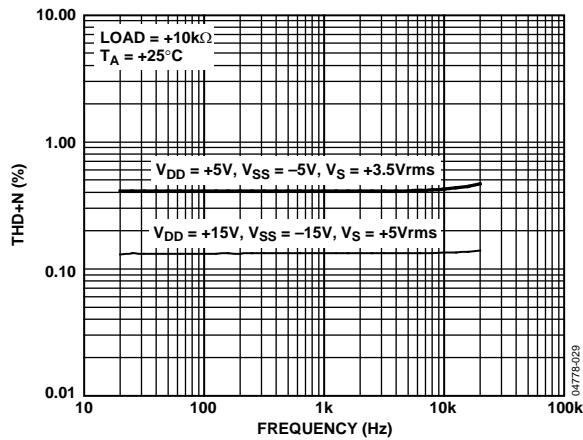


Figure 17. THD + N vs. Frequency

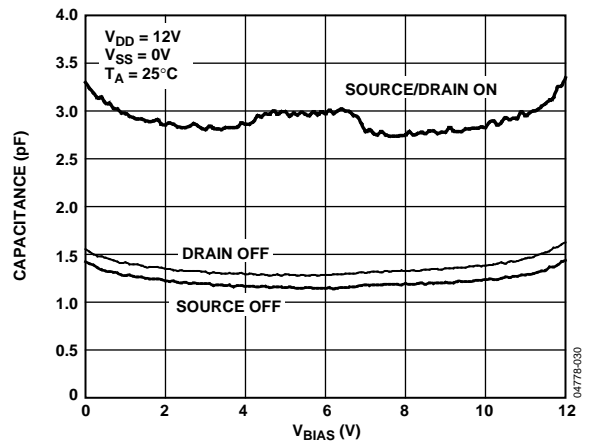


Figure 19. Capacitance vs. Source Voltage, Single Supply

TEST CIRCUITS

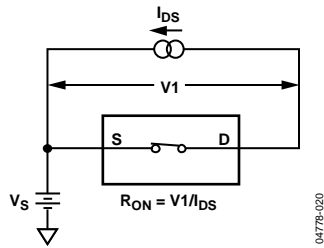


Figure 20. On Resistance

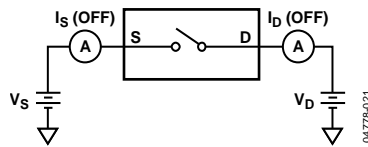


Figure 21. Off Leakage

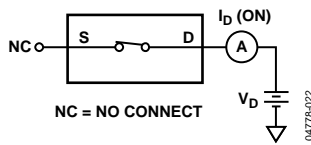


Figure 22. On Leakage

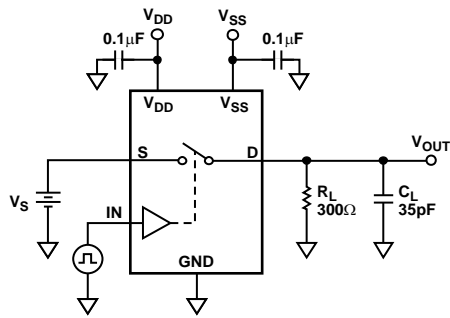


Figure 23. Switching Times

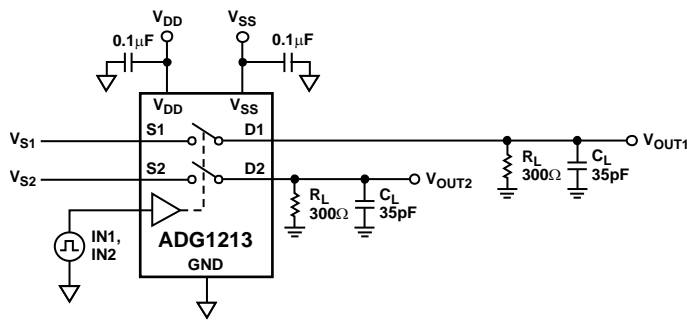
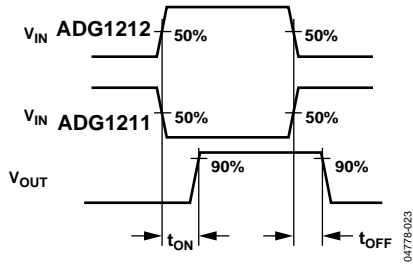
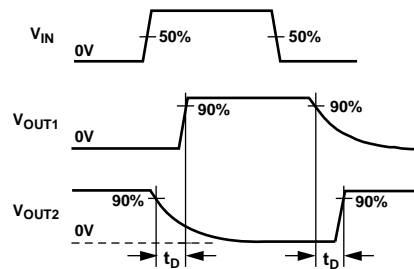


Figure 24. Break-Before-Make Time Delay



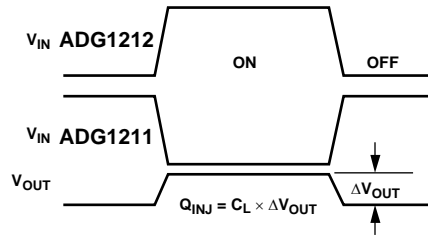
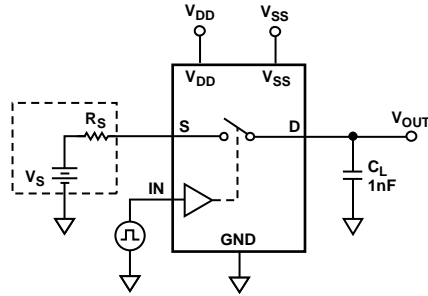
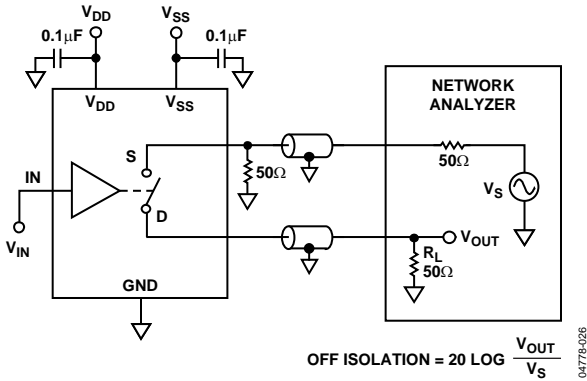
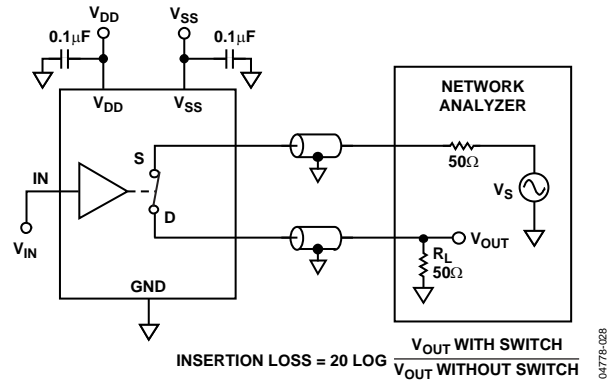


Figure 25. Charge Injection



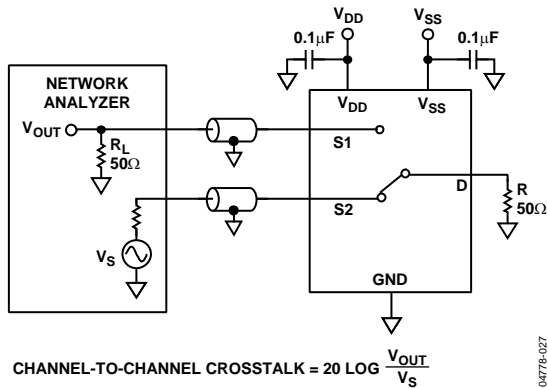
OFF ISOLATION = 20 LOG  $\frac{V_{OUT}}{V_S}$

Figure 26. Off Isolation



INSERTION LOSS = 20 LOG  $\frac{V_{OUT\ WITH\ SWITCH}}{V_{OUT\ WITHOUT\ SWITCH}}$

Figure 28. Bandwidth



CHANNEL-TO-CHANNEL CROSSTALK = 20 LOG  $\frac{V_{OUT}}{V_S}$

Figure 27. Channel-to-Channel Crosstalk

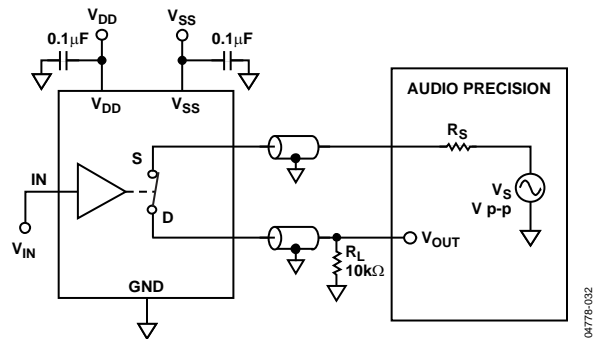
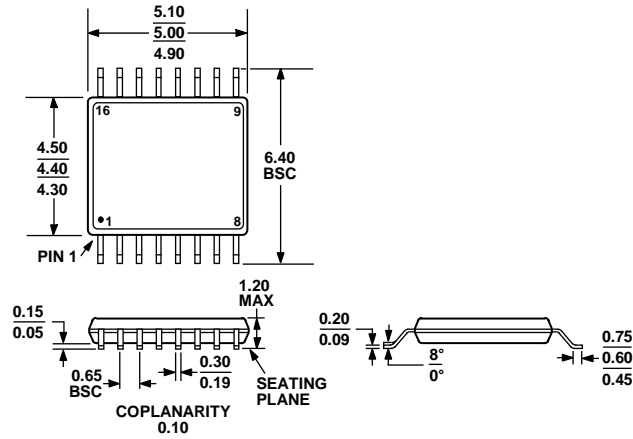


Figure 29. THD + Noise

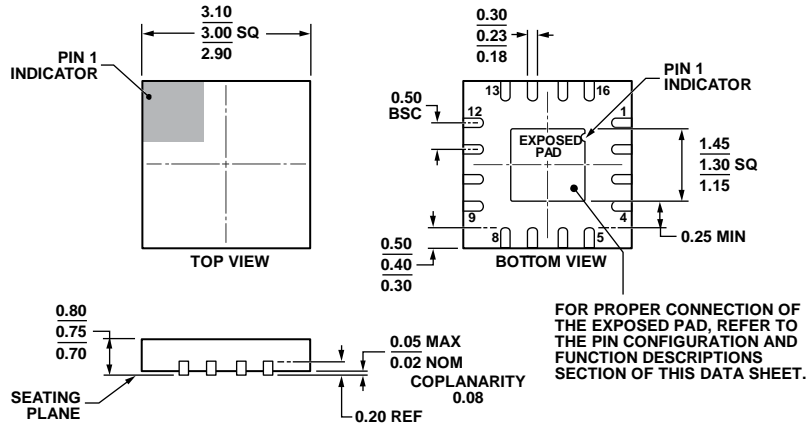
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 30. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters



FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

COMPLIANT TO JEDEC STANDARDS MO-220-WEED.

Figure 31. 16-Lead Lead Frame Chip Scale Package [LFCSP] 3 mm x 3 mm Body and 0.75 mm Package Height (CP-16-21)

Dimensions shown in millimeters

111898-A

**ORDERING GUIDE**

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding
ADG1211YRUZ	-40°C to +125°C	Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1211YRUZ-REEL	-40°C to +125°C	Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1211YRUZ-REEL7	-40°C to +125°C	Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1211YCPZ-500RL7	-40°C to +125°C	Lead Frame Chip Scale Package [LFCSP]	CP-16-21	S07
ADG1211YCPZ-REEL7	-40°C to +125°C	Lead Frame Chip Scale Package [LFCSP]	CP-16-21	S07
ADG1212YRUZ	-40°C to +125°C	Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1212YRUZ-REEL7	-40°C to +125°C	Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1212YCPZ-500RL7	-40°C to +125°C	Lead Frame Chip Scale Package [LFCSP]	CP-16-21	S08
ADG1212YCPZ-REEL7	-40°C to +125°C	Lead Frame Chip Scale Package [LFCSP]	CP-16-21	S08
ADG1213YRUZ	-40°C to +125°C	Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1213YRUZ-REEL7	-40°C to +125°C	Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG1213YCPZ-500RL7	-40°C to +125°C	Lead Frame Chip Scale Package [LFCSP]	CP-16-21	S09
ADG1213YCPZ-REEL7	-40°C to +125°C	Lead Frame Chip Scale Package [LFCSP]	CP-16-21	S09

<sup>1</sup>Z = RoHS Compliant Part.

NOTES



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[NLAST4599DTT1G](#) [DG403DY-T1-E3](#) [MAX4714EXTT](#) [MAX392CPE](#) [BGSX22G2A10E6327XTSA1](#) [ADG1611BRUZ-REEL7](#)