

FEATURES

- 4.7 Ω maximum on resistance at 25°C
- 0.5 Ω on-resistance flatness
- Up to 190 mA continuous current
- Fully specified at ± 15 V/ $+12$ V/ ± 5 V
- 3 V logic-compatible inputs
- Rail-to-rail operation
- Break-before-make switching action
- 16-lead TSSOP and 4 mm \times 4 mm LFCSP

APPLICATIONS

- Relay replacement
- Audio and video routing
- Automatic test equipment
- Data acquisition systems
- Temperature measurement systems
- Avionics
- Battery-powered systems
- Communication systems
- Medical equipment

GENERAL DESCRIPTION

The [ADG1408/ADG1409](#) are monolithic *i*CMOS[®] analog multiplexers comprising eight single channels and four differential channels, respectively. The [ADG1408](#) switches one of eight inputs to a common output, as determined by the 3-bit binary address lines, A0, A1, and A2. The [ADG1409](#) switches one of four differential inputs to a common differential output, as determined by the 2-bit binary address lines, A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched off.

The industrial CMOS (*i*CMOS) modular manufacturing process combines high voltage complementary metal-oxide semiconductor (CMOS) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no other generation of high voltage devices has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

FUNCTIONAL BLOCK DIAGRAMS

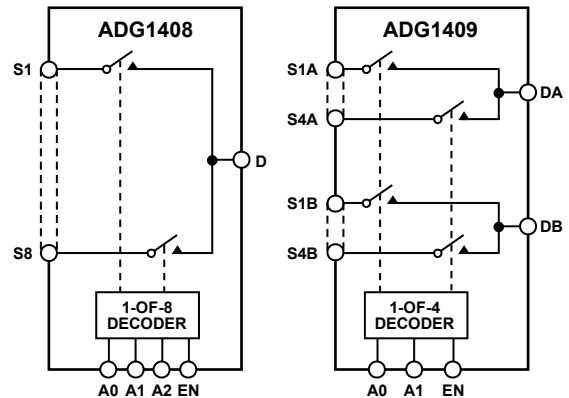


Figure 1.

The ultralow on resistance and on resistance flatness of these switches make them ideal solutions for data acquisition and gain switching applications where low distortion is critical. *i*CMOS construction ensures ultralow power dissipation, making the devices ideally suited for portable and battery-powered instruments.

PRODUCT HIGHLIGHTS

1. 4 Ω on resistance.
2. 0.5 Ω on-resistance flatness.
3. 3 V logic compatible digital input, $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V.
4. 16-lead TSSOP and 4 mm \times 4 mm LFCSP.

Table 1. Related Devices

| Device No. | Description |
|---------------------------------|---|
| ADG1208/ADG1209 | Low capacitance, low charge injection, and low leakage 4-/8-channel ± 15 V multiplexers |

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REVISION HISTORY

6/2016—Rev. C to Rev. D

| | |
|---|---|
| Changes to Analog Inputs Parameter, Table 6 | 9 |
| Added Digital Inputs Parameter, Table 6 | 9 |

5/2016—Rev. B to Rev. C

| | |
|------------------------------------|------------|
| Changed CP-16-13 to CP-16-26 | Throughout |
| Changes to Figure 3 | 10 |
| Changes to Figure 5 | 11 |
| Updated Outline Dimensions | 19 |
| Changes to Ordering Guide | 20 |

3/2009—Rev. A to Rev. B

| | |
|--|---|
| Change to I _{DD} Parameter, Table 2 | 4 |
| Change to I _{DD} Parameter, Table 3 | 6 |

8/2008—Rev. 0 to Rev. A

| | |
|--|----|
| Changes to Features | 1 |
| Added Table 5; Renumbered Sequentially | 8 |
| Changes to Table 6 | 9 |
| Added Exposed Pad Notation to Figure 3 | 10 |
| Added Exposed Pad Notation to Figure 5 | 11 |
| Added Exposed Pad Notation to Outline Dimensions | 19 |

8/2006—Revision 0: Initial Version

SPECIFICATIONS

15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 2.

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C ¹ | Unit | Test Conditions/Comments |
|--|-------------|----------------|------------------------------|-------------------|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | V_{SS} to V_{DD} | V | |
| On Resistance (R_{ON}) | 4 | | | Ω typ | $V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 26 |
| | 4.7 | 5.7 | 6.7 | Ω max | $V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$ |
| On Resistance Match Between Channels (ΔR_{ON}) | 0.2 | | | Ω typ | $V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$ |
| | 0.78 | 0.85 | 1.1 | Ω max | |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | 0.5 | | | Ω typ | $V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$ |
| | 0.72 | 0.77 | 0.92 | Ω max | |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.04 | | | nA typ | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ |
| | ± 0.2 | ± 0.6 | ± 5 | nA max | $V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 27 |
| Drain Off Leakage, I_D (Off) | ± 0.04 | | | nA typ | $V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 27 |
| | ± 0.45 | ± 2 | ± 30 | nA max | |
| Channel On Leakage, I_D , I_S (On) | ± 0.1 | | | nA typ | $V_S = V_D = \pm 10\text{ V}$; see Figure 28 |
| | ± 1.5 | ± 3 | ± 30 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current | ± 0.005 | | | μA typ | $V_{IN} = V_{GND}$ or V_{DD} |
| | | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 4 | | | pF typ | |
| DYNAMIC CHARACTERISTICS² | | | | | |
| Transition Time, $t_{TRANSITION}$ | 140 | | | ns typ | $R_L = 100\ \Omega$, $C_L = 35\text{ pF}$ |
| | 170 | 210 | 240 | ns max | $V_S = 10\text{ V}$, see Figure 29 |
| Break-Before-Make Time Delay, t_{BBM} | 50 | | | ns typ | $R_L = 100\ \Omega$, $C_L = 35\text{ pF}$ |
| | | | 30 | ns min | $V_{S1} = V_{S2} = 10\text{ V}$; see Figure 30 |
| t_{ON} (EN) | 100 | | | ns typ | $R_L = 100\ \Omega$, $C_L = 35\text{ pF}$ |
| | 120 | 150 | 165 | ns max | $V_S = 10\text{ V}$; see Figure 31 |
| t_{OFF} (EN) | 100 | | | ns typ | $R_L = 100\ \Omega$, $C_L = 35\text{ pF}$ |
| | 120 | 150 | 170 | ns max | $V_S = 10\text{ V}$; see Figure 31 |
| Charge Injection | -50 | | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 32 |
| Off Isolation | -70 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 33 |
| Channel-to-Channel Crosstalk | -70 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 34 |
| Total Harmonic Distortion Plus Noise (THD + N) | 0.025 | | | % typ | $R_L = 110\ \Omega$, 15 V p-p, $f = 20\text{ Hz}$ to 20 kHz; see Figure 36 |
| -3 dB Bandwidth | | | | | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 35 |
| ADG1408 | 60 | | | MHz typ | |
| ADG1409 | 115 | | | MHz typ | |
| Insertion Loss | 0.24 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 35 |
| C_S (Off) | 14 | | | pF typ | $f = 1\text{ MHz}$ |
| C_D (Off) | | | | | $f = 1\text{ MHz}$ |
| ADG1408 | 80 | | | pF typ | |
| ADG1409 | 40 | | | pF typ | |

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C ¹ | Unit | Test Conditions/Comments |
|--------------------------------------|-------|----------------|------------------------------|-----------|--|
| C _D , C _S (On) | | | | | f = 1 MHz |
| ADG1408 | 135 | | | pF typ | |
| ADG1409 | 90 | | | pF typ | |
| POWER REQUIREMENTS | | | | | |
| I _{DD} | 0.002 | | | μA typ | V _{DD} = +16.5 V, V _{SS} = -16.5 V |
| | | | 1 | μA max | Digital inputs = 0 V or V _{DD} |
| | 220 | | | μA typ | Digital inputs = 5 V |
| | | | 380 | μA max | |
| I _{SS} | 0.002 | | | μA typ | Digital inputs = 0 V, 5 V or V _{DD} |
| | | | 1 | μA max | |
| V _{DD} /V _{SS} | | | ±4.5/±16.5 | V min/max | |

¹ Temperature range: Y version: -40°C to +125°C.

² Guaranteed by design, not subject to production test.

12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 3.

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C ¹ | Unit | Test Conditions/Comments |
|--|-------------|----------------|------------------------------|-------------------|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 to V_{DD} | V | |
| On Resistance (R_{ON}) | 6 | | | Ω typ | $V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 26 |
| | 8 | 9.5 | 11.2 | Ω max | $V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$ |
| On-Resistance Match Between Channels (ΔR_{ON}) | 0.2 | | | Ω typ | $V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$ |
| | 0.82 | 0.85 | 1.1 | Ω max | |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | 1.5 | | | Ω typ | $V_S = 0\text{ V to }10\text{ V}$, $I_S = -10\text{ mA}$ |
| | 2.5 | 2.5 | 2.8 | Ω max | |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.04 | | | nA typ | $V_{DD} = 13.2\text{ V}$ $V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 27 |
| | ± 0.2 | ± 0.6 | ± 5 | nA max | |
| Drain Off Leakage, I_D (Off) | ± 0.04 | | | nA typ | $V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 27 |
| | ± 0.45 | ± 1 | ± 37 | nA max | |
| Channel On Leakage, I_D , I_S (On) | ± 0.06 | | | nA typ | $V_S = V_D = 1\text{ V or }10\text{ V}$; see Figure 28 |
| | ± 0.44 | ± 1.3 | ± 32 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current | ± 0.005 | | | μA typ | $V_{IN} = V_{GND}$ or V_{DD} |
| | | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 5 | | | pF typ | |
| DYNAMIC CHARACTERISTICS² | | | | | |
| Transition Time, $t_{TRANSITION}$ | 200 | | | ns typ | $R_L = 100\ \Omega$, $C_L = 35\text{ pF}$ |
| | 260 | 330 | 380 | ns max | $V_S = 8\text{ V}$; see Figure 29 |
| Break-Before-Make Time Delay, t_{BBM} | 90 | | | ns typ | $R_L = 100\ \Omega$, $C_L = 35\text{ pF}$ |
| | | | 40 | ns min | $V_{S1} = V_{S2} = 8\text{ V}$; see Figure 30 |
| t_{ON} (EN) | 160 | | | ns typ | $R_L = 100\ \Omega$, $C_L = 35\text{ pF}$ |
| | 210 | 250 | 285 | ns max | $V_S = 8\text{ V}$; see Figure 31 |
| t_{OFF} (EN) | 115 | | | ns typ | $R_L = 100\ \Omega$, $C_L = 35\text{ pF}$ |
| | 145 | 180 | 200 | ns max | $V_S = 8\text{ V}$; see Figure 31 |
| Charge Injection | -12 | | | pC typ | $V_S = 6\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 32 |
| Off Isolation | -70 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 33 |
| Channel-to-Channel Crosstalk | -70 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 34 |
| -3 dB Bandwidth | | | | | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 35 |
| ADG1408 | 36 | | | MHz typ | |
| ADG1409 | 72 | | | MHz typ | |
| Insertion Loss | 0.5 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 35 |
| C_S (Off) | 25 | | | pF typ | $f = 1\text{ MHz}$ |
| C_D (Off) | | | | | $f = 1\text{ MHz}$ |
| ADG1408 | 165 | | | pF typ | |
| ADG1409 | 80 | | | pF typ | |
| C_D , C_S (On) | | | | | $f = 1\text{ MHz}$ |
| ADG1408 | 200 | | | pF typ | |
| ADG1409 | 120 | | | pF typ | |

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C ¹ | Unit | Test Conditions/Comments |
|--------------------|-------|----------------|------------------------------|-------------------|--|
| POWER REQUIREMENTS | | | | | $V_{DD} = 13.2\text{ V}$ |
| I_{DD} | 0.002 | | 1 | $\mu\text{A typ}$ | Digital inputs = 0 V or V_{DD} |
| | 220 | | 380 | $\mu\text{A max}$ | Digital inputs = 5 V |
| V_{DD} | | | 5/16.5 | V min/max | $V_{SS} = 0\text{ V}, \text{GND} = 0\text{ V}$ |

¹ Temperature range for Y version: -40°C to +125°C.

² Guaranteed by design, not subject to production test.

5 V DUAL SUPPLY

$V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 4.

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C ¹ | Unit | Test Conditions/Comments |
|--|-------------|----------------|------------------------------|-------------------|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | V_{SS} to V_{DD} | V | |
| On Resistance (R_{ON}) | 7 | | | Ω typ | $V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$; see Figure 26 |
| | 9 | 10.5 | 12 | Ω max | $V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$ |
| On-Resistance Match Between Channels (ΔR_{ON}) | 0.3 | | | Ω typ | $V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$ |
| | 0.78 | 0.91 | 1.1 | Ω max | |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | 1.5 | | | Ω typ | $V_S = \pm 4.5\text{ V}$; $I_S = -10\text{ mA}$ |
| | 2.5 | 2.5 | 3 | Ω max | |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.02 | | | nA typ | $V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ |
| | ± 0.2 | ± 0.6 | ± 5 | nA max | $V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$; see Figure 27 |
| Drain Off Leakage, I_D (Off) | ± 0.02 | | | nA typ | $V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$; see Figure 27 |
| | ± 0.45 | ± 0.8 | ± 20 | nA max | |
| Channel On Leakage, I_D , I_S (On) | ± 0.04 | | | nA typ | $V_S = V_D = \pm 4.5\text{ V}$; see Figure 28 |
| | ± 0.3 | ± 1.1 | ± 22 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current | ± 0.005 | | | μA typ | $V_{IN} = V_{GND}$ OR V_{DD} |
| | | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 5 | | | pF typ | |
| DYNAMIC CHARACTERISTICS² | | | | | |
| Transition Time, $t_{TRANSITION}$ | 330 | | | ns typ | $R_L = 100\ \Omega$, $C_L = 35\text{ pF}$ |
| | 440 | 530 | 550 | ns max | $V_S = 5\text{ V}$; see Figure 29 |
| Break-Before-Make Time Delay, t_{BBM} | 100 | | | ns typ | $R_L = 100\ \Omega$, $C_L = 35\text{ pF}$ |
| | | | 50 | ns min | $V_{S1} = V_{S2} = 5\text{ V}$; see Figure 30 |
| t_{ON} (EN) | 245 | | | ns typ | $R_L = 100\ \Omega$, $C_L = 35\text{ pF}$ |
| | 330 | 400 | 440 | ns max | $V_S = 5\text{ V}$; see Figure 31 |
| t_{OFF} (EN) | 215 | | | ns typ | $R_L = 100\ \Omega$, $C_L = 35\text{ pF}$ |
| | 285 | 335 | 370 | ns max | $V_S = 5\text{ V}$; see Figure 31 |
| Charge Injection | -10 | | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 32 |
| Off Isolation | -70 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 33 |
| Channel-to-Channel Crosstalk | -70 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 34 |
| Total Harmonic Distortion Plus Noise (THD + N) | 0.06 | | | % typ | $R_L = 110\ \Omega$, 5 V p-p, $f = 20\text{ Hz}$ to 20 kHz; see Figure 36 |
| -3 dB Bandwidth | | | | | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 35 |
| ADG1408 | 40 | | | MHz typ | |
| ADG1409 | 80 | | | MHz typ | |
| Insertion Loss | 0.5 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 35 |
| C_S (Off) | 20 | | | pF typ | $f = 1\text{ MHz}$ |
| C_D (Off) | | | | | $f = 1\text{ MHz}$ |
| ADG1408 | 130 | | | pF typ | |
| ADG1409 | 65 | | | pF typ | |
| C_D , C_S (On) | | | | | $f = 1\text{ MHz}$ |
| ADG1408 | 180 | | | pF typ | |
| ADG1409 | 120 | | | pF typ | |

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C ¹ | Unit | Test Conditions/Comments |
|---------------------------|-------|----------------|------------------------------|--|--|
| POWER REQUIREMENTS | | | | | |
| I_{DD} | 0.001 | | 1 | $\mu\text{A typ}$ $\mu\text{A max}$ | $V_{DD} = +5.5\text{ V}, V_{SS} = -5.5\text{ V}$ Digital inputs = 0 V or V_{DD} |
| I_{SS} | 0.001 | | 1 | $\mu\text{A typ}$ $\mu\text{A max}$ | Digital inputs = 0 V, 5 V or V_{DD} |
| V_{DD}/V_{SS} | | | $\pm 4.5/\pm 16.5$ | V min/max | |

¹ Temperature range for Y version: -40°C to +125°C.

² Guaranteed by design, not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, S OR D

Table 5.

| Parameter | 25°C | 85°C | 125°C | Unit | Test Conditions/Comments |
|---|------|------|-------|--------|--|
| CONTINUOUS CURRENT, S or D¹ | | | | | |
| 15 V Dual Supply | | | | | $V_{DD} = +13.5\text{ V}, V_{SS} = -13.5\text{ V}$ |
| ADG1408 | 190 | 105 | 50 | mA max | |
| ADG1409 | 140 | 85 | 45 | mA max | |
| 12 V Single Supply | | | | | $V_{DD} = 10.8\text{ V}, V_{SS} = 0\text{ V}$ |
| ADG1408 | 160 | 95 | 50 | mA max | |
| ADG1409 | 120 | 75 | 40 | mA max | |
| 5 V Dual Supply | | | | | $V_{DD} = +4.5\text{ V}, V_{SS} = -4.5\text{ V}$ |
| ADG1408 | 155 | 90 | 45 | mA max | |
| ADG1409 | 115 | 70 | 40 | mA max | |

¹ Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 6.

| Parameter | Rating |
|---|--|
| V_{DD} to V_{SS} | 35 V |
| V_{DD} to GND | -0.3 V to +25 V |
| V_{SS} to GND | +0.3 V to -25 V |
| Analog Inputs ¹ | $V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first |
| Digital Inputs ¹ | GND - 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first |
| Continuous Current, S or D | Table 5 data + 10% |
| Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Maximum) | 350 mA |
| Operating Temperature Range Industrial (Y Version) | -40°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| Reflow Soldering Peak Temperature (RoHS Compliant) | 260(+0/-5)°C |

¹ Overvoltages at A, EN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

| Package Type | θ_{JA} | θ_{JC} | Unit |
|---------------|---------------|---------------|------|
| 16-Lead TSSOP | 150.4 | 50 | °C/W |
| 16-Lead LFCSP | 30.4 | | °C/W |

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

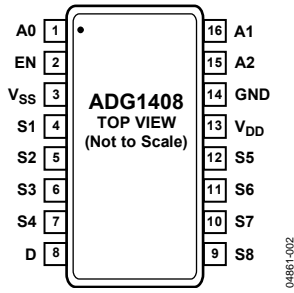
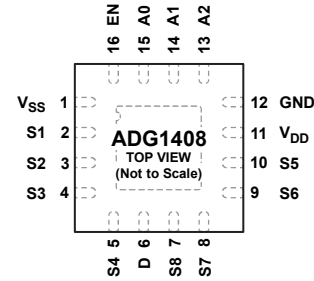


Figure 2. ADG1408 Pin Configuration (TSSOP)



NOTES
 1. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE SUBSTRATE, V_{SS}.

Figure 3. ADG1408 Pin Configuration (LFCSP)

Table 8. ADG1408 Pin Function Descriptions

| Pin No. | | Mnemonic | Description |
|----------------|-------|-----------------|---|
| TSSOP | LFCSP | | |
| 1 | 15 | A0 | Logic Control Input. |
| 2 | 16 | EN | Active High Digital Input. When low, the device is disabled and all switches are off. When high, A _x logic inputs determine on switches. |
| 3 | 1 | V _{SS} | Most Negative Power Supply Potential. In single supply applications, it can be connected to ground. |
| 4 | 2 | S1 | Source Terminal 1. Can be an input or an output. |
| 5 | 3 | S2 | Source Terminal 2. Can be an input or an output. |
| 6 | 4 | S3 | Source Terminal 3. Can be an input or an output. |
| 7 | 5 | S4 | Source Terminal 4. Can be an input or an output. |
| 8 | 6 | D | Drain Terminal. Can be an input or an output. |
| 9 | 7 | S8 | Source Terminal 8. Can be an input or an output. |
| 10 | 8 | S7 | Source Terminal 7. Can be an input or an output. |
| 11 | 9 | S6 | Source Terminal 6. Can be an input or an output. |
| 12 | 10 | S5 | Source Terminal 5. Can be an input or an output. |
| 13 | 11 | V _{DD} | Most Positive Power Supply Potential. |
| 14 | 12 | GND | Ground (0 V) Reference. |
| 15 | 13 | A2 | Logic Control Input. |
| 16 | 14 | A1 | Logic Control Input. |
| Not applicable | 0 | EPAD | Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V _{SS} . |

Table 9. ADG1408 Truth Table

| A2 | A1 | A0 | EN | On Switch |
|----|----|----|----|-----------|
| X | X | X | 0 | None |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 2 |
| 0 | 1 | 0 | 1 | 3 |
| 0 | 1 | 1 | 1 | 4 |
| 1 | 0 | 0 | 1 | 5 |
| 1 | 0 | 1 | 1 | 6 |
| 1 | 1 | 0 | 1 | 7 |
| 1 | 1 | 1 | 1 | 8 |

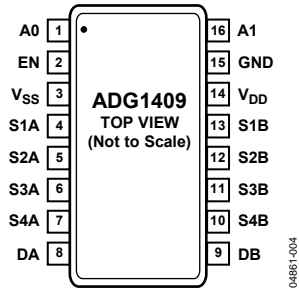
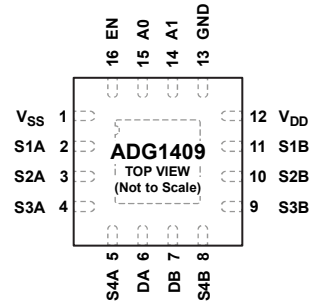


Figure 4. ADG1409 Pin Configuration (TSSOP)



NOTES
 1. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE SUBSTRATE, V_{SS}.

Figure 5. ADG1409 Pin Configuration (LFCSP)

Table 10. ADG1409 Pin Function Descriptions

| Pin No. | | Mnemonic | Description |
|----------------|-------|-----------------|---|
| TSSOP | LFCSP | | |
| 1 | 15 | A0 | Logic Control Input. |
| 2 | 16 | EN | Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches. |
| 3 | 1 | V _{SS} | Most Negative Power Supply Potential. In single supply applications, it can be connected to ground. |
| 4 | 2 | S1A | Source Terminal 1A. Can be an input or an output. |
| 5 | 3 | S2A | Source Terminal 2A. Can be an input or an output. |
| 6 | 4 | S3A | Source Terminal 3A. Can be an input or an output. |
| 7 | 5 | S4A | Source Terminal 4A. Can be an input or an output. |
| 8 | 6 | DA | Drain Terminal A. Can be an input or an output. |
| 9 | 7 | DB | Drain Terminal B. Can be an input or an output. |
| 10 | 8 | S4B | Source Terminal 4B. Can be an input or an output. |
| 11 | 9 | S3B | Source Terminal 3B. Can be an input or an output. |
| 12 | 10 | S2B | Source Terminal 2B. Can be an input or an output. |
| 13 | 11 | S1B | Source Terminal 1B. Can be an input or an output. |
| 14 | 12 | V _{DD} | Most Positive Power Supply Potential. |
| 15 | 13 | GND | Ground (0 V) Reference. |
| 16 | 14 | A1 | Logic Control Input. |
| Not applicable | 0 | EPAD | Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V _{SS} . |

Table 11. ADG1409 Truth Table

| A1 | A0 | EN | On Switch Pair |
|----|----|----|----------------|
| X | X | 0 | None |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 2 |
| 1 | 0 | 1 | 3 |
| 1 | 1 | 1 | 4 |

TYPICAL PERFORMANCE CHARACTERISTICS

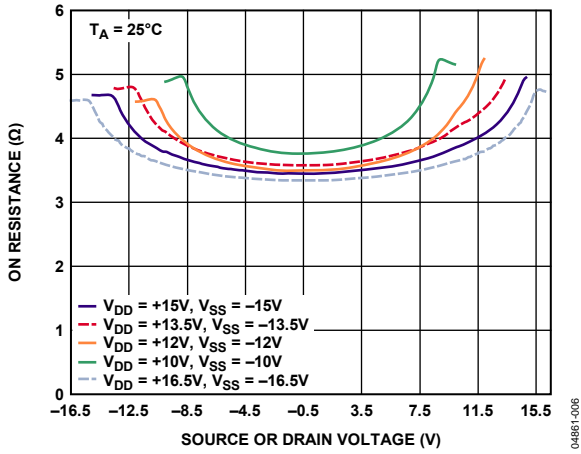


Figure 6. On Resistance vs. V_D, V_S ; Dual Supply

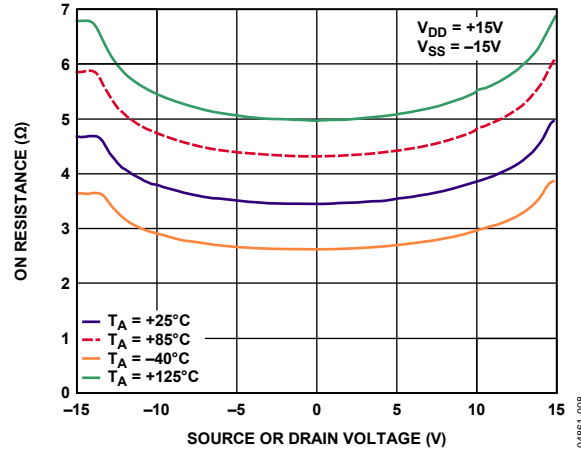


Figure 9. On Resistance vs. V_D, V_S for Different Temperatures; 15 V Dual Supply

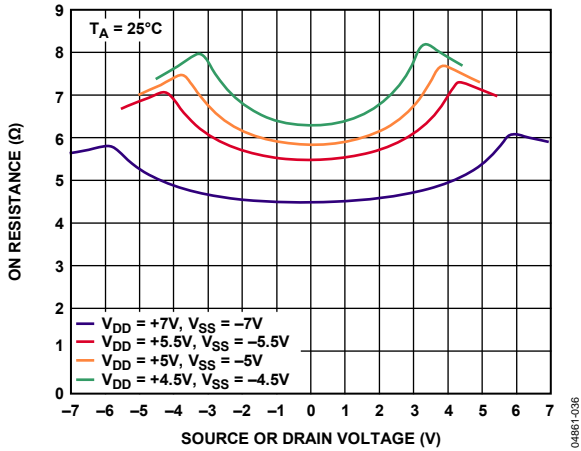


Figure 7. On Resistance vs. V_D, V_S ; Dual Supply

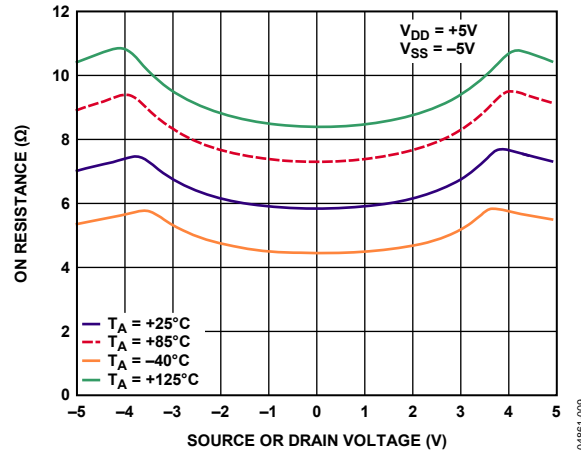


Figure 10. On Resistance vs. V_D, V_S for Different Temperatures; 5 V Dual Supply

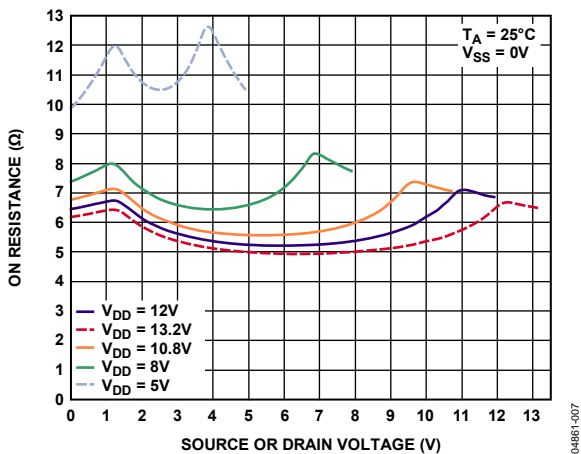


Figure 8. On Resistance vs. V_D, V_S ; Single Supply

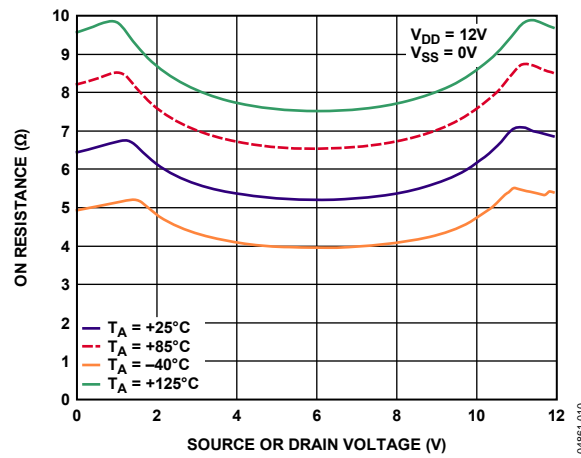


Figure 11. On Resistance vs. V_D, V_S for Different Temperatures; 12 V Single Supply

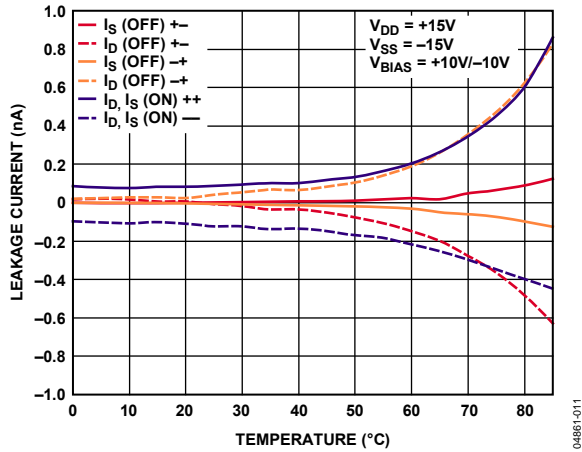


Figure 12. Leakage Current vs. Temperature; 15 V Dual Supply

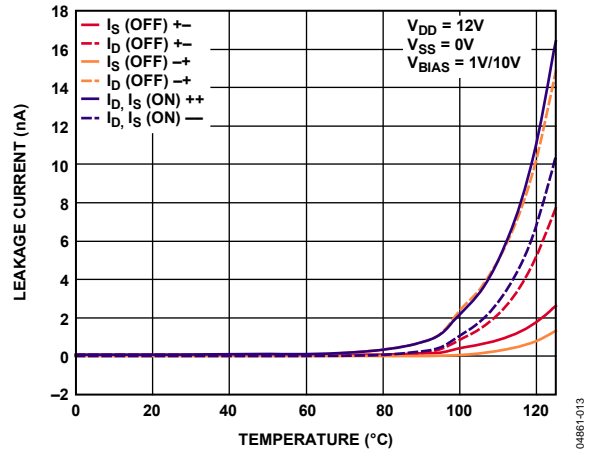


Figure 15. Leakage Current vs. Temperature; 12 V Single Supply

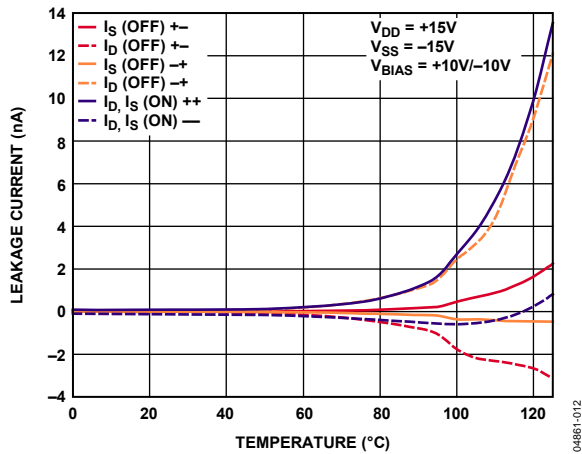


Figure 13. Leakage Current vs. Temperature; 15 V Dual Supply

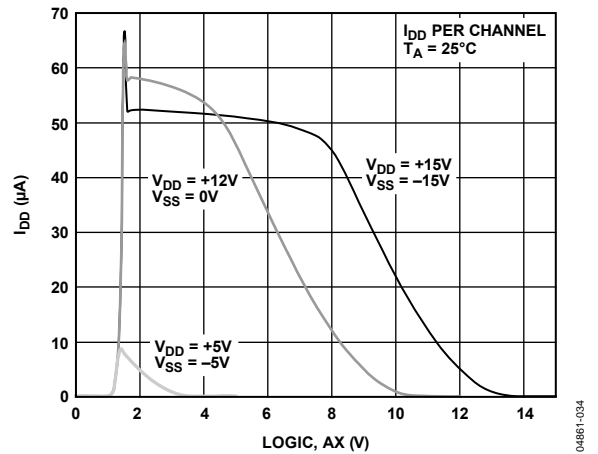


Figure 16. Positive Supply Current vs. Logic Level

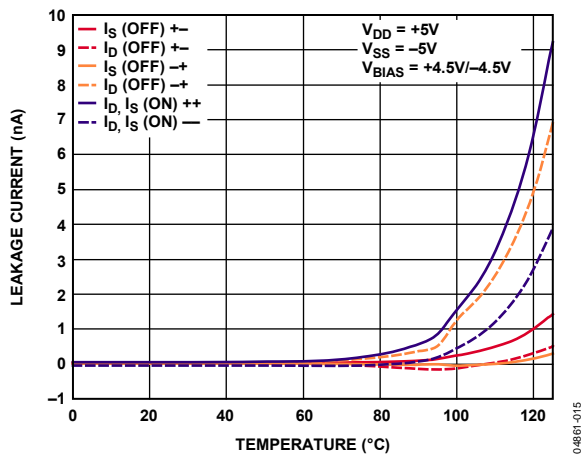


Figure 14. Leakage Current vs. Temperature; 5 V Dual Supply

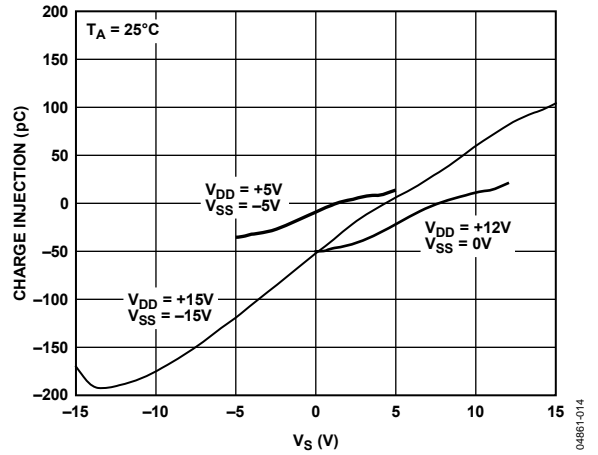


Figure 17. Charge Injection vs. Source Voltage

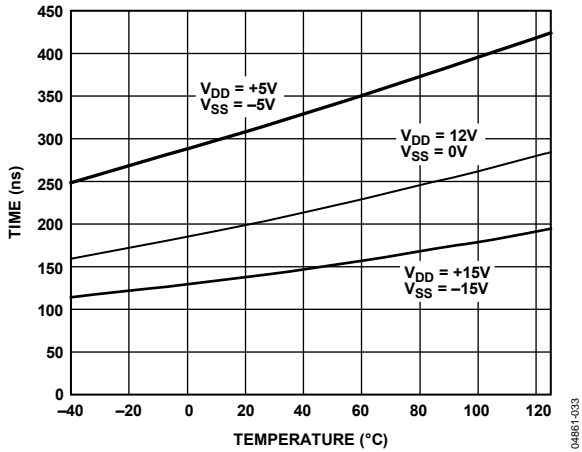


Figure 18. Transition Time vs. Temperature

04861-023

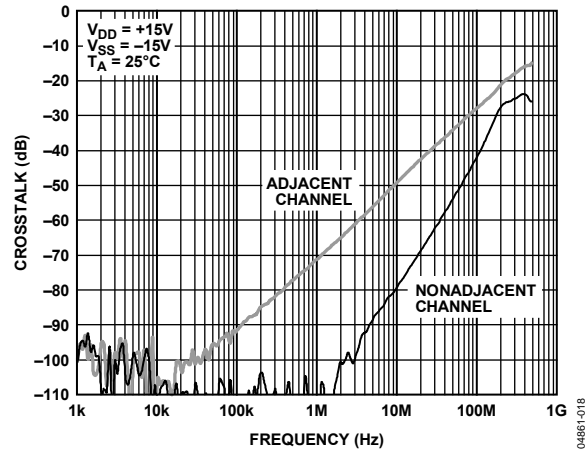


Figure 21. ADG1409 Crosstalk vs. Frequency

04861-018

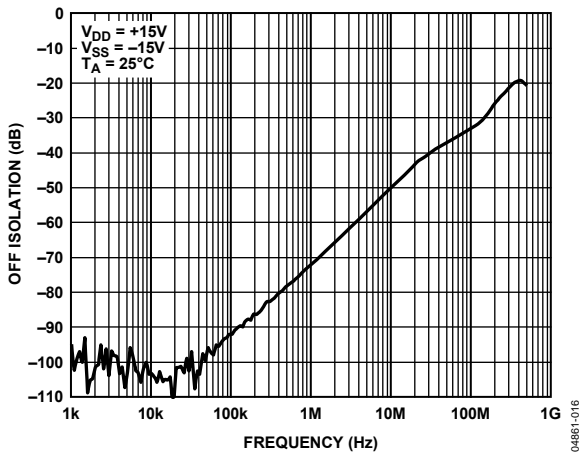


Figure 19. Off Isolation vs. Frequency

04861-016

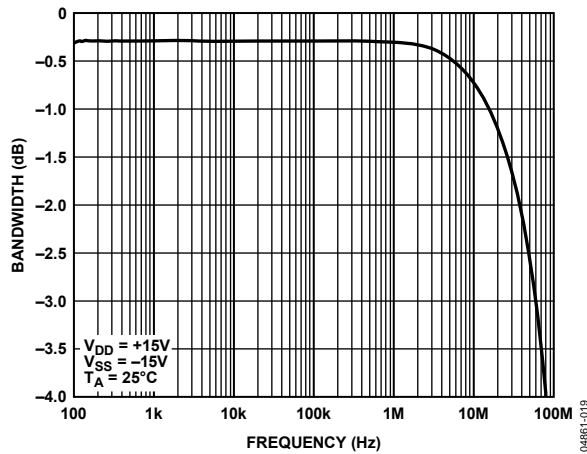


Figure 22. ADG1408 On Response vs. Frequency

04861-019

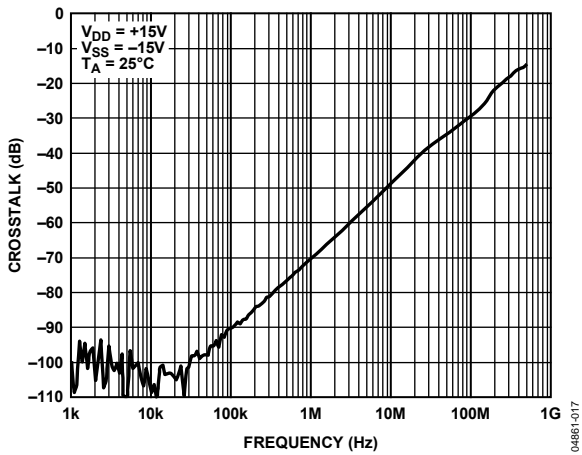


Figure 20. ADG1408 Crosstalk vs. Frequency

04861-017

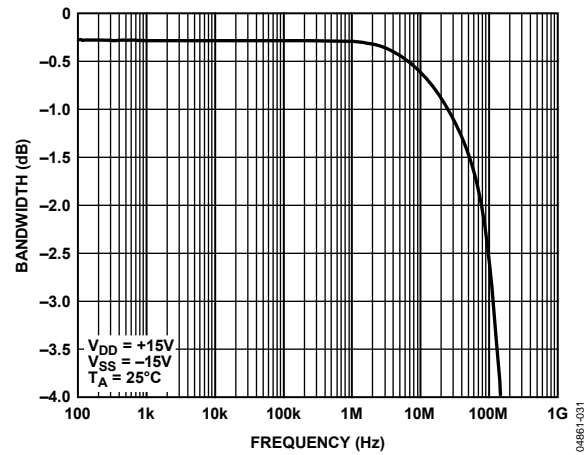


Figure 23. ADG1409 On Response vs. Frequency

04861-031

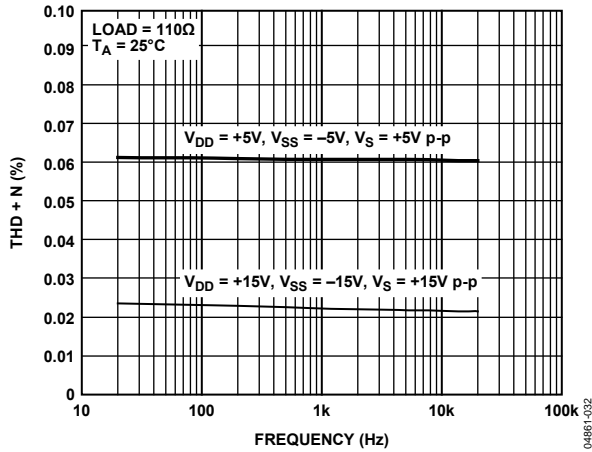


Figure 24. Total Harmonic Distortion Plus Noise vs. Frequency

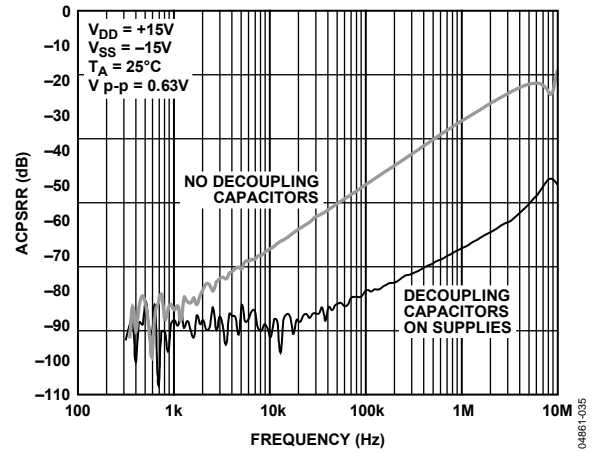


Figure 25. AC Power Supply Rejection Ratio vs. Frequency

TERMINOLOGY

R_{ON}

Ohmic resistance between D and S.

ΔR_{ON}

Difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured.

I_S (Off)

Source leakage current when the switch is off.

I_D (Off)

Drain leakage current when the switch is off.

I_D, I_S (On)

Channel leakage current when the switch is on.

V_D (V_S)

Analog voltage on Terminal D and Terminal S.

C_S (Off)

Channel input capacitance for off condition.

C_D (Off)

Channel output capacitance for off condition.

C_D, C_S (On)

On switch capacitance.

C_{IN}

Digital input capacitance.

t_{ON} (EN)

Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)

Delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_{BBM}

Off time measured between the 80% point of both switches when switching from one address state to another.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL}, I_{INH}

Input current of the digital input.

I_{DD}

Positive supply current.

I_{SS}

Negative supply current.

Off Isolation

A measure of unwanted signal coupling through an off channel.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Bandwidth

Frequency at which the output is attenuated by 3 dB.

On Response

Frequency response of the on switch.

Total Harmonic Distortion Plus Noise (THD + N)

Ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)

A measure of the ability of a device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

TEST CIRCUITS

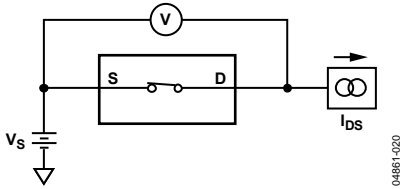


Figure 26. On Resistance

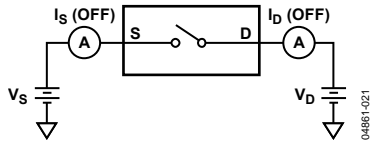


Figure 27. Off Leakage

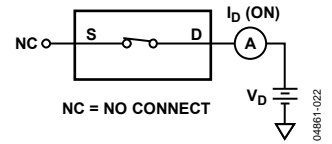


Figure 28. On Leakage

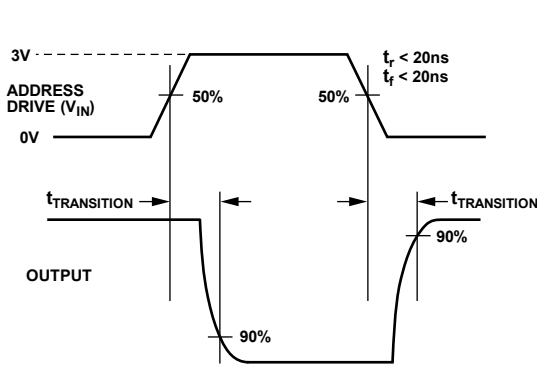
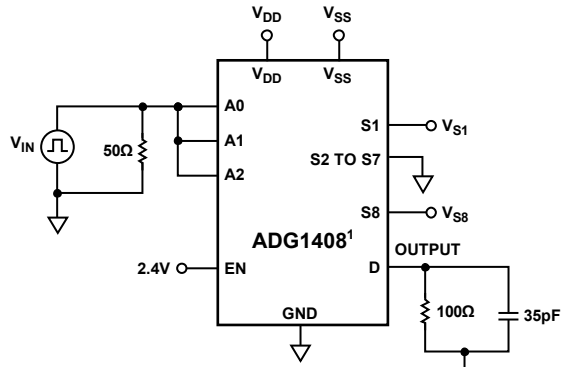


Figure 29. Address to Output Switching Times, $t_{TRANSITION}$



¹SIMILAR CONNECTION FOR ADG1409.

04861-023

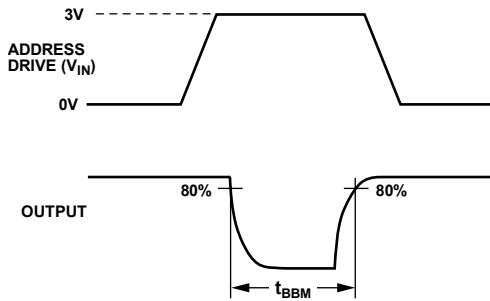
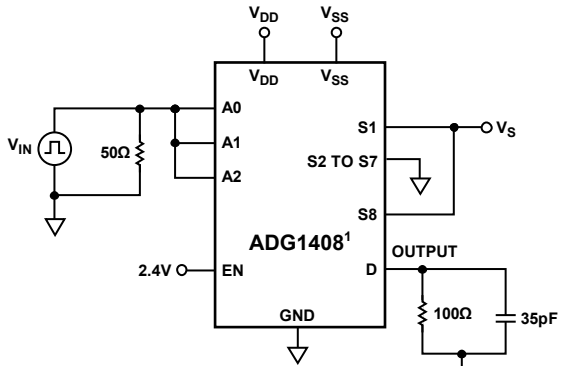


Figure 30. Break-Before-Make Delay, t_{BBM}



¹SIMILAR CONNECTION FOR ADG1409.

04861-024

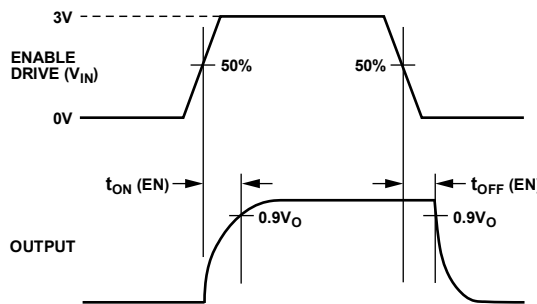
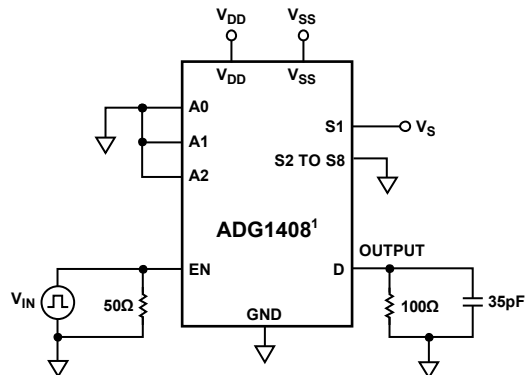


Figure 31. Enable Delay, $t_{ON} (EN)$, $t_{OFF} (EN)$



¹SIMILAR CONNECTION FOR ADG1409.

04861-025

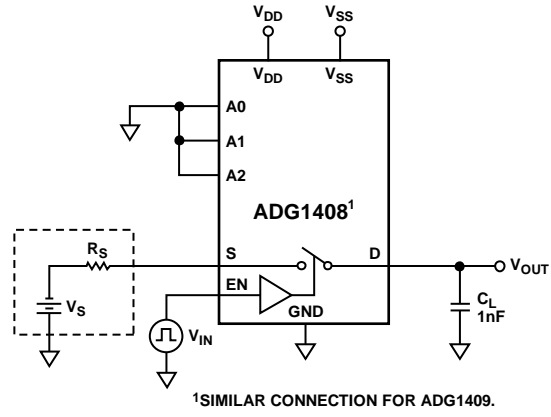
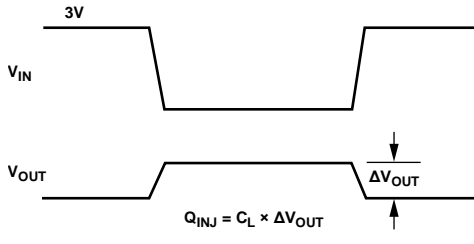


Figure 32. Charge Injection

04861-026

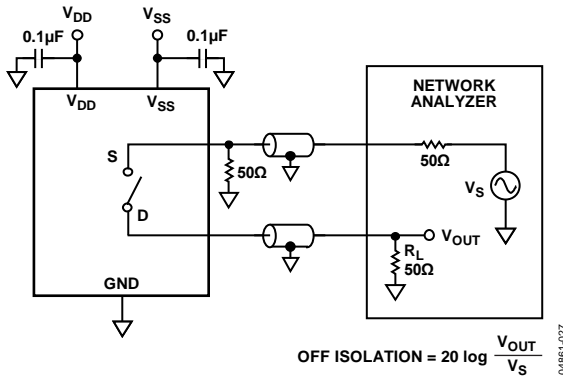


Figure 33. Off Isolation

04861-027

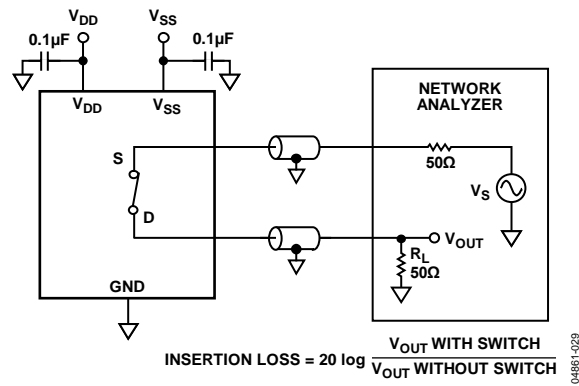


Figure 35. Insertion Loss

04861-028

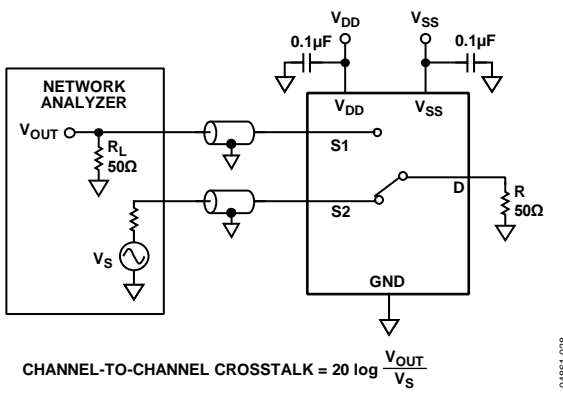


Figure 34. Channel-to-Channel Crosstalk

04861-029

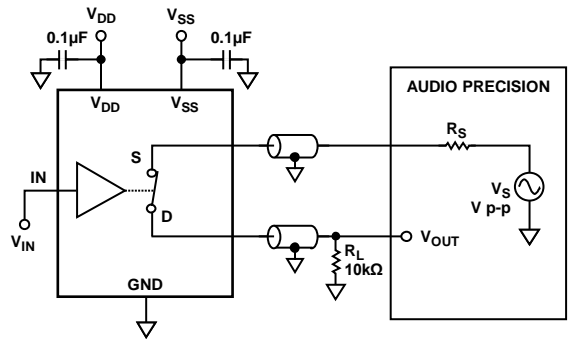
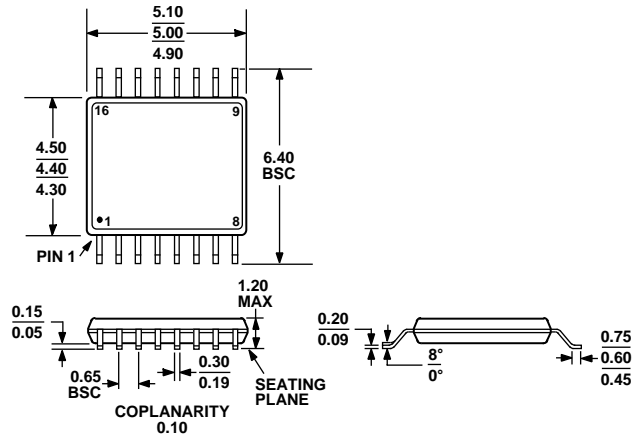


Figure 36. THD + N

04861-030

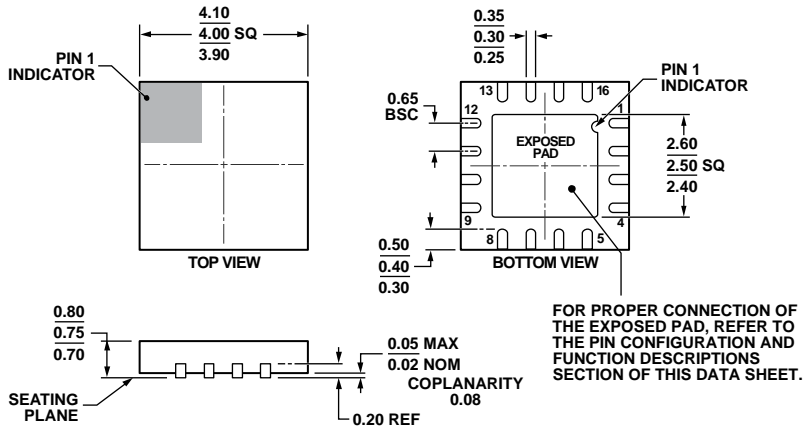
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 37. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 38. 16-Lead Lead Frame Chip Scale Package [LFCS] 4 mm x 4 mm Body and 0.75 mm Package Height (CP-16-26)

Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---|----------------|
| ADG1408YRUZ | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG1408YRUZ-REEL | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG1408YRUZ-REEL7 | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG1408YCPZ-REEL7 | -40°C to +125°C | 16-Lead Lead Frame Chip Scale Package [LFCS] | CP-16-26 |
| ADG1409YRUZ | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG1409YRUZ-REEL | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG1409YRUZ-REEL7 | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG1409YCPZ-REEL7 | -40°C to +125°C | 16-Lead Lead Frame Chip Scale Package [LFCS] | CP-16-26 |

¹ Z = RoHS Compliant Part.

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[74LVC1G3157GM,132](#) [74LVC2G53DC,125](#) [TC7PCI3215MT,LF](#) [ADG1407BCPZ-REEL7](#) [ADG1407BRUZ](#) [ADG1409SRU-EP](#)