

### FEATURES

- 1.8 V to 5.5 V single supply
- 2.5  $\Omega$  (typical) on resistance
- Low on-resistance flatness
- Guaranteed leakage performance over  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- $-3$  dB bandwidth  $> 200$  MHz
- Rail-to-rail operation
- 10-lead MSOP package
- Fast switching times
- $t_{\text{ON}}$  16 ns
- $t_{\text{OFF}}$  8 ns
- Typical power consumption ( $< 0.01$   $\mu\text{W}$ )
- TTL/CMOS compatible

### APPLICATIONS

- USB 1.1 signal switching circuits
- Cell phones
- PDA's
- Battery-powered systems
- Communication systems
- Sample-and-hold systems
- Audio signal routing
- Audio and video switching
- Mechanical reed relay replacement

### GENERAL DESCRIPTION

The ADG736L is a monolithic device comprising two independently selectable CMOS single pole, double throw (SPDT) switches. The switches are designed using a submicron process that provides low power dissipation, yet gives high switching speed, low on resistance, low leakage currents, and wide input signal bandwidth.

The on resistance profile is very flat over the full analog signal range. This ensures excellent linearity and low distortion when switching audio signals. Fast switching speed also makes the part suitable for video signal switching.

The ADG736L operates from a single 1.8 V to 5.5 V supply, making it ideally suited to portable and battery-powered instruments.

Each switch conducts equally well in both directions when on; each has an input signal range that extends to the power supplies. The ADG736L exhibits break-before-make switching action.

The ADG736L is available in a 10-lead MSOP.

### FUNCTIONAL BLOCK DIAGRAM

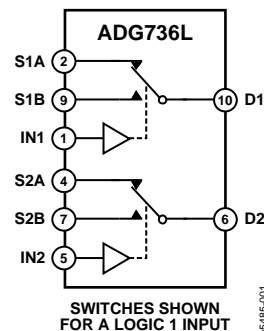


Figure 1.

### PRODUCT HIGHLIGHTS

1. 1.8 V to 5.5 V Single-Supply Operation.
2. Guaranteed Leakage Performance.
3. Very Low  $R_{\text{ON}}$  (4.5  $\Omega$  Maximum at 5 V, 8  $\Omega$  Maximum at 3 V).
4. Low On Resistance Flatness.
5.  $-3$  dB Bandwidth  $> 200$  MHz.
6. Low Power Dissipation.

#### Rev. 0

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## REVISION HISTORY

1/07—Revision 0: Initial Version

## SPECIFICATIONS

$V_{DD} = 5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ ; all specifications  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise noted.

Table 1.

Parameter	B Version <sup>1</sup>		Unit	Test Conditions/Comments
	25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>				
Analog Signal Range		0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	2.5		$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = -10\text{ mA}$ ; see Figure 10
	4	4.5	$\Omega$ max	
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.1		$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = -10\text{ mA}$
		0.4	$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	0.5		$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_{DS} = -10\text{ mA}$
		1.2	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>				
Source Off Leakage $I_S$ (OFF)	$\pm 0.01$		nA typ	$V_{DD} = 5.5\text{ V}$
	$\pm 0.1$	$\pm 0.3$	nA max	$V_S = 4.5\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/4.5\text{ V}$ ; see Figure 11
Channel On Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$		nA typ	$V_S = V_D = 1\text{ V}$ or $4.5\text{ V}$ ; see Figure 12
	$\pm 0.1$	$\pm 0.3$	nA max	
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.005		$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		$\pm 0.1$	$\mu\text{A}$ max	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
$t_{ON}$	12		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
		16	ns max	$V_S = 3\text{ V}$ ; see Figure 13
$t_{OFF}$	5		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
		8	ns max	$V_S = 3\text{ V}$ ; see Figure 13
Break-Before-Make Time Delay, $t_D$	7		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
		1	ns min	$V_{S1} = V_{S2} = 3\text{ V}$ ; see Figure 14
Off Isolation	-62		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$
	-82		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 15
Channel-to-Channel Crosstalk	-62		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$
	-82		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 16
Bandwidth (-3 dB)	200		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 17
$C_S$ (OFF)	9		pF typ	
$C_D$ , $C_S$ (ON)	32		pF typ	
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.001		$\mu\text{A}$ typ	$V_{DD} = 5.5\text{ V}$
		1.0	$\mu\text{A}$ max	Digital inputs = 0 V or 5 V

<sup>1</sup> Temperature range is  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  for the B version.

<sup>2</sup> Guaranteed by design; not subject to production test.

# ADG736L

$V_{DD} = 3\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ . All specifications  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise noted.

**Table 2.**

Parameter	B Version <sup>1</sup>		Unit	Test Conditions/Comments
	25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>				
Analog Signal Range		0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	5	5.5	$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = -10\text{ mA}$ ; see Figure 10
		8	$\Omega$ max	
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.1		$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = -10\text{ mA}$
		0.4	$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )		2.5	$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = -10\text{ mA}$
<b>LEAKAGE CURRENTS</b>				
Source Off Leakage $I_S$ (OFF)	$\pm 0.01$		nA typ	$V_{DD} = 3.3\text{ V}$
	$\pm 0.1$	$\pm 0.3$	nA max	$V_S = 3\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/3\text{ V}$ ; see Figure 11
Channel On Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$		nA typ	$V_S = V_D = 1\text{ V or }3\text{ V}$ ; see Figure 12
	$\pm 0.1$	$\pm 0.3$	nA max	
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.0	V min	
Input Low Voltage, $V_{INL}$		0.4	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.005		$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		$\pm 0.1$	$\mu\text{A}$ max	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
$t_{ON}$	14		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
		20	ns max	$V_S = 2\text{ V}$ ; see Figure 13
$t_{OFF}$	6		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
		10	ns max	$V_S = 2\text{ V}$ ; see Figure 13
Break-Before-Make Time Delay, $t_D$	7		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
		1	ns min	$V_{S1} = V_{S2} = 2\text{ V}$ ; see Figure 14
Off Isolation	-62		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$
	-82		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 15
Channel-to-Channel Crosstalk	-62		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$
	-82		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 16
Bandwidth (-3 dB)	200		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 17
$C_S$ (OFF)	9		pF typ	
$C_D$ , $C_S$ (ON)	32		pF typ	
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.001		$\mu\text{A}$ typ	$V_{DD} = 3.3\text{ V}$
		1.0	$\mu\text{A}$ max	Digital inputs = 0 V or 3 V

<sup>1</sup> Temperature range is  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  for the B version.

<sup>2</sup> Guaranteed by design; not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameter	Rating
$V_{DD}$ to GND	-0.3 V to +6 V
Analog, Digital Inputs <sup>1</sup>	-0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Continuous Current, S or D	30 mA
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% duty cycle maximum)
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
MSOP Package, Power Dissipation	315 mW
$\theta_{JA}$ Thermal Impedance	205°C/W
Lead Temperature (Soldering, 10 sec)	300°C
IR Reflow (Peak Temperature, <20 sec)	235°C
Lead-Free Reflow	
Peak Temperature	260(+0/-5)°C
Time at Peak Temperature	10 sec to 40 sec
ESD	2 kV

<sup>1</sup> Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# ADG736L

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

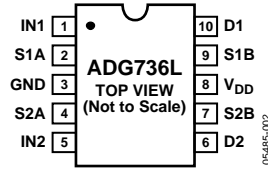


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN1	Logic Control Input.
2	S1A	Source Terminal. May be an input or an output.
3	GND	Ground (0 V) Reference.
4	S2A	Source Terminal. May be an input or an output.
5	IN2	Logic Control Input.
6	D2	Drain Terminal. May be an input or an output.
7	S2B	Source Terminal. May be an input or an output.
8	V <sub>DD</sub>	Most Positive Power Supply Potential.
9	S1B	Source Terminal. May be an input or an output.
10	D1	Drain Terminal. May be an input or an output.

Table 5. Truth Table

Logic	Switch A	Switch B
0	Off	On
1	On	Off

# TYPICAL PERFORMANCE CHARACTERISTICS

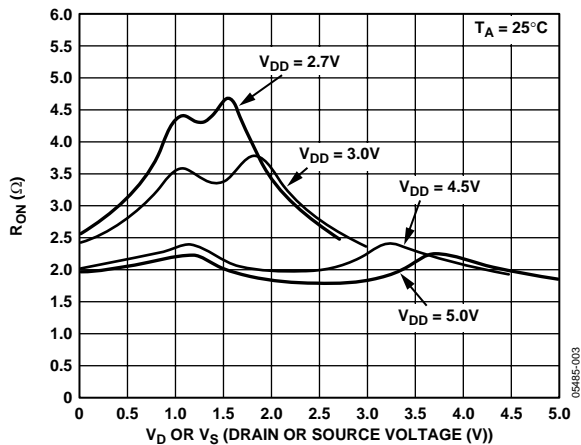


Figure 3. On Resistance as a Function of  $V_D$  ( $V_S$ ) Single Supplies

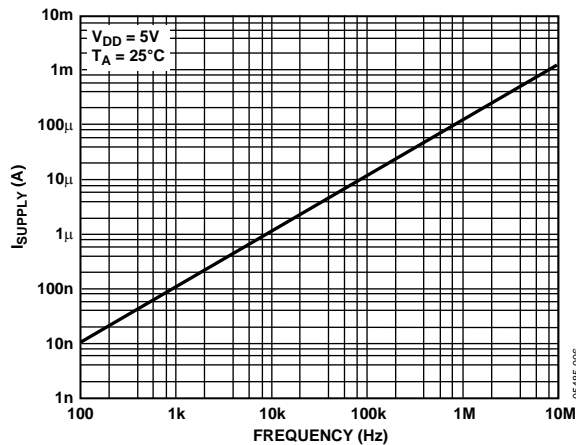


Figure 6. Supply Current vs. Input Switching Frequency

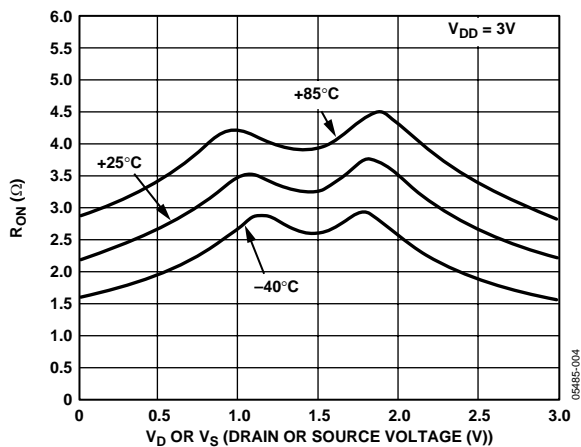


Figure 4. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures  
 $V_{DD} = 3V$

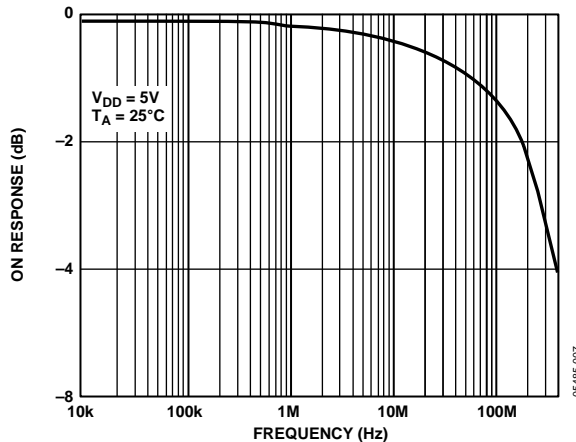


Figure 7. Bandwidth

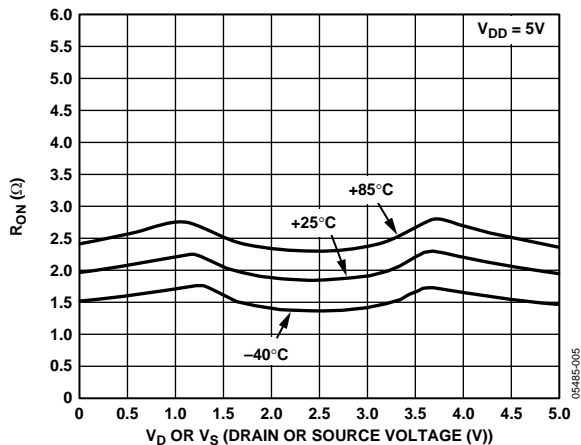


Figure 5. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures  
 $V_{DD} = 5V$

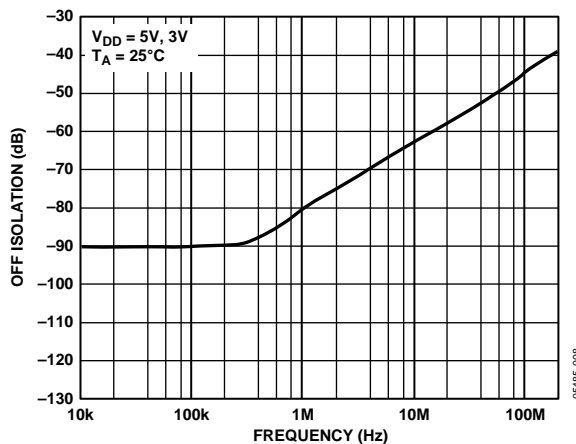


Figure 8. Off Isolation vs. Frequency

# ADG736L

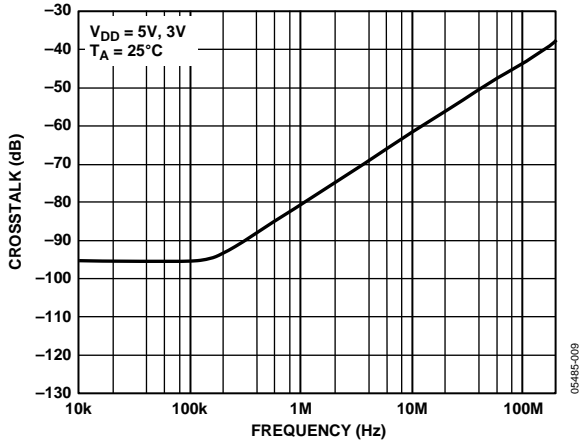


Figure 9. Crosstalk vs. Frequency



# TEST CIRCUITS

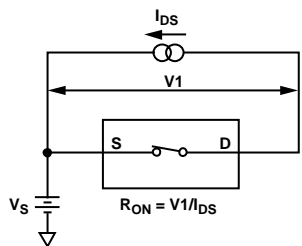


Figure 10. On Resistance

05485-011

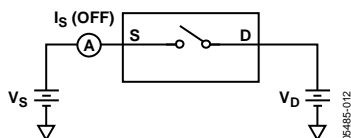


Figure 11. Off Leakage

05485-012

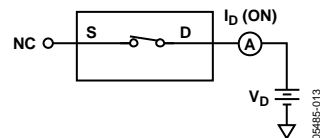


Figure 12. On Leakage

05485-013

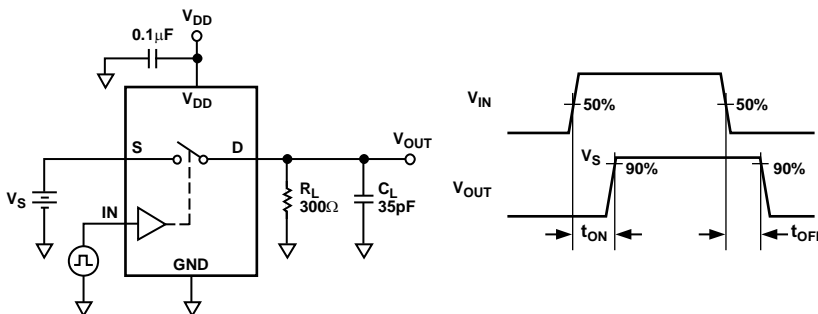


Figure 13. Switching Times

05485-014

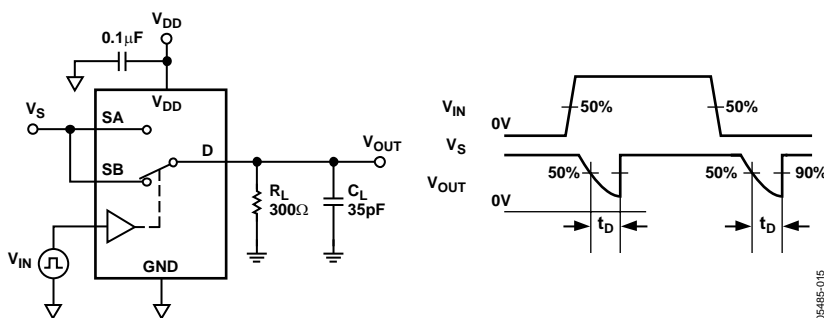


Figure 14. Break-Before-Make Time Delay,  $t_D$

05485-015

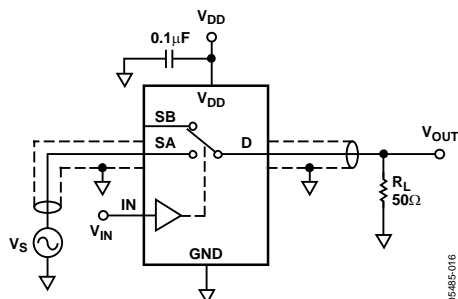
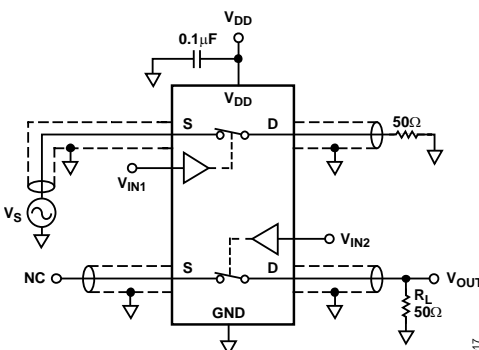


Figure 15. Off Isolation

05485-016



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \times \text{LOG} |V_S/V_{OUT}|$$

Figure 16. Channel-to-Channel Crosstalk

05485-017

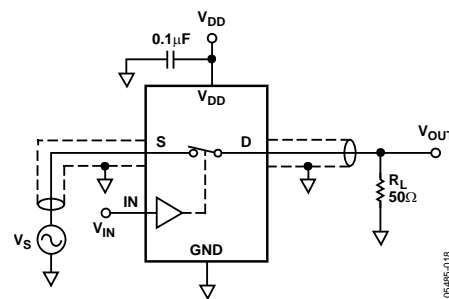


Figure 17. Bandwidth

05485-018

## TERMINOLOGY

### $R_{ON}$

Ohmic resistance between D and S.

### $\Delta R_{ON}$

On resistance match between any two channels, such as  $R_{ON}$  maximum –  $R_{ON}$  minimum.

### $R_{FLAT(ON)}$

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

### $I_S$ (OFF)

Source leakage current with the switch off.

### $I_D, I_S$ (ON)

Channel leakage current with the switch on.

### $V_D$ ( $V_S$ )

Analog voltage on Terminal D and Terminal S.

### $C_S$ (OFF)

Off switch source capacitance.

### $C_D, C_S$ (ON)

On switch capacitance.

### $t_{ON}$

Delay between applying the digital control input and the output switching on (see Figure 13).

### $t_{OFF}$

Delay between applying the digital control input and the output switching off.

### $t_D$

Off time or on time measured between the 90% points of both switches, when switching from one address state to another (see Figure 14).

### Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

### Off Isolation

A measure of unwanted signal coupling through an off switch.

### Bandwidth

The frequency at which the output is attenuated by –3 dB.

### On Response

The frequency response of the on switch.

### On Loss

The voltage drop across the on switch, seen on the On Response vs. Frequency plot (see Figure 7) as how many decibels the signal is away from 0 dB at very low frequencies.

APPLICATIONS INFORMATION

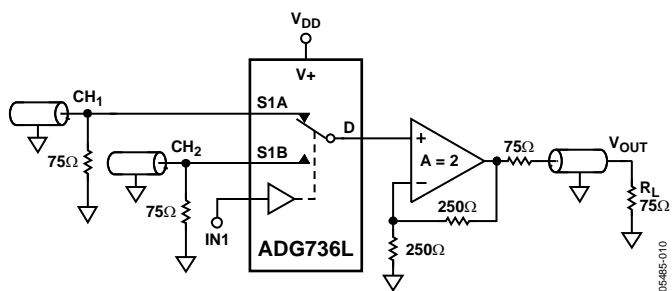
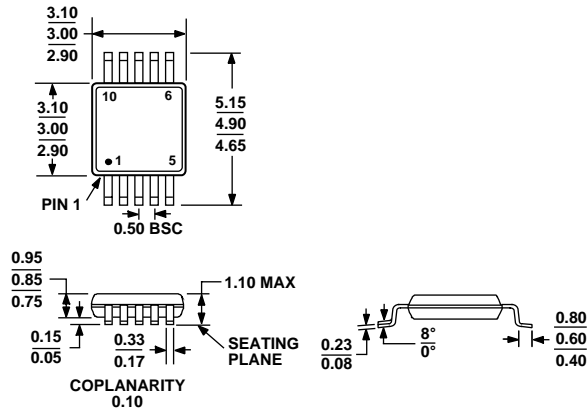


Figure 18. Using the ADG736L to Select Between Two Video Signals

05F485-010

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 19. 10-Lead Mini Small Outline Package [MSOP]  
(RM-10)

Dimensions shown in millimeters

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADG736LBRM	-40°C to +85°C	10-Lead Mini Small Outline Package (MSOP)	RM-10	SOY
ADG736LBRM-REEL	-40°C to +85°C	10-Lead Mini Small Outline Package (MSOP)	RM-10	SOY
ADG736LBRM-REEL7	-40°C to +85°C	10-Lead Mini Small Outline Package (MSOP)	RM-10	SOY
ADG736LBRMZ <sup>1</sup>	-40°C to +85°C	10-Lead Mini Small Outline Package (MSOP)	RM-10	SOZ
ADG736LBRMZ-REEL <sup>1</sup>	-40°C to +85°C	10-Lead Mini Small Outline Package (MSOP)	RM-10	SOZ
ADG736LBRMZ-REEL7 <sup>1</sup>	-40°C to +85°C	10-Lead Mini Small Outline Package (MSOP)	RM-10	SOZ

<sup>1</sup> Z = Pb-free part.

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[TC4W53FU\(TE12L,F\)](#) [74HC2G66DC.125](#) [ADG619BRMZ-REEL](#) [ADG1611BRUZ-REEL7](#) [LTC201ACN#PBF](#) [74LV4066DB,118](#)  
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