

FEATURES

Bandwidth: 300 MHz

Low insertion loss and on resistance: 5 Ω typical

On-resistance flatness: 0.7 Ω typical

Single 3.3 V/5 V supply operation

Low quiescent supply current: 1 nA typical

Fast switching times

t_{ON} , 7 ns

t_{OFF} , 5 ns

TTL/CMOS compatible

ESD protection

2 kV human body model (HBM)

200 V machine model (MM)

1 kV field-induced charged device model (FICDM)

APPLICATIONS

RGB switches

HDTV

DVD-R

Audio/video switches

GENERAL DESCRIPTION

The ADG794 is a monolithic CMOS device comprising four 2:1 multiplexers/demultiplexers with high impedance outputs. The CMOS process provides low power dissipation yet gives high switching speed and low on resistance. The on-resistance variation is less than 1.2 Ω over the input signal range.

The wide bandwidth of the ADG794 (300 MHz typical), coupled with low distortion (0.18% typical), makes the part suitable for switching analog audio/video signals.

The ADG794 operates from a single 3.3 V/5 V supply and is TTL logic compatible. The switches are controlled by the logic inputs IN and EN, as shown in Table 4. The \overline{EN} pin allows the user to disable all switches.

These switches conduct equally well in both directions when on. In the off condition, signal levels up to the supplies are blocked. The ADG794 switches exhibit break-before-make switching action. The ADG794 is available in a 16-lead QSOP.

FUNCTIONAL BLOCK DIAGRAM

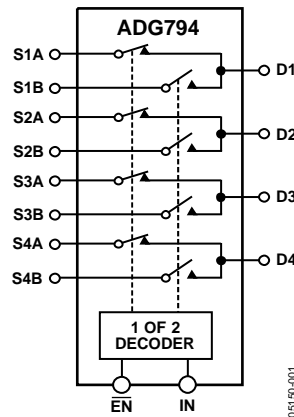


Figure 1.

PRODUCT HIGHLIGHTS

1. Wide bandwidth: 300 MHz.
2. Ultralow power dissipation.
3. Crosstalk: -70 dB (typical) at 10 MHz.
4. Off isolation: -65 dB (typical) at 10 MHz.
5. ESD protection tested as per ESD Association Standards:
 - 2 kV HBM (ANSI/ESD STM5.1-2001)
 - 200 V MM (ANSI/ESD STM5.2-1999)
 - 1 kV FICDM (ANSI/ESD STM5.3.1-1999)

Rev. B

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TABLE OF CONTENTS

Features1
Applications.....1
Functional Block Diagram1
General Description1
Product Highlights1
Revision History2
Specifications.....3
 Single Supply3
Absolute Maximum Ratings.....5

ESD Caution5
Pin Configuration and Function Descriptions6
Terminology.....7
Typical Performance Characteristics8
Typical Application9
Test Circuits10
Outline Dimensions.....12
 Ordering Guide12

REVISION HISTORY

2/08—Rev A to Rev B

Changes to Absolute Maximum Ratings Section, Table 3 5
Updated Outline Dimensions 12
Changes to Ordering Guide 12

4/06—Rev. 0 to Rev. A

Changes to Features Section 1
Changes to Product Highlights Section 1
Changes to Specifications Section.....3
Changes to Typical Performance Characteristics8

10/04—Revision 0: Initial Version

SPECIFICATIONS

SINGLE SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 1.

Parameter	B Version ¹		Unit	Test Conditions/Comments
	25°C	T_{MIN} to T_{MAX}		
ANALOG SWITCH				
Analog Signal Range		0 to 2.5	V	
On Resistance, R_{ON}	5		Ω typ	$V_D = 0\text{ V}$ to 1 V ; $I_S = -10\text{ mA}$; Figure 8
	7	8	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	0.4		Ω typ	$V_D = 0\text{ V}$ to 1 V ; $I_S = -10\text{ mA}$
		1.2	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.7		Ω typ	$V_D = 0\text{ V}$ to 1 V ; $I_S = -10\text{ mA}$
		1.35	Ω max	
LEAKAGE CURRENTS				
Source Off Leakage, I_S (Off)	± 0.001		nA typ	$V_S = 3\text{ V}/1\text{ V}$; $V_D = 1\text{ V}/3\text{ V}$; Figure 9
Drain Off Leakage, I_D (Off)	± 0.001		nA typ	$V_S = 3\text{ V}/1\text{ V}$; $V_D = 1\text{ V}/3\text{ V}$; Figure 9
Channel On Leakage, I_D, I_S (On)	± 0.001		nA typ	$V_D = V_S = 3\text{ V}/1\text{ V}$; Figure 10
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.001		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.1	μA max	
Digital Input Capacitance, C_{IN}		3	pF typ	
DYNAMIC CHARACTERISTICS²				
$t_{ON}, t_{ON}(\overline{EN})$	7		ns typ	$C_L = 35\text{ pF}$; $R_L = 50\ \Omega$
		14	ns max	$V_S = 2\text{ V}$; Figure 11
$t_{OFF}, t_{OFF}(\overline{EN})$	5		ns typ	$C_L = 35\text{ pF}$; $R_L = 50\ \Omega$
		8	ns max	$V_S = 2\text{ V}$; Figure 11
Break-Before-Make Time Delay, t_D	3		ns typ	$C_L = 35\text{ pF}$; $R_L = 50\ \Omega$
		1	ns min	$V_{S1} = V_{S2} = 2\text{ V}$; Figure 12
Off Isolation	-65		dB typ	$f = 10\text{ MHz}$; $R_L = 50\ \Omega$; Figure 14
Channel-to-Channel Crosstalk	-70		dB typ	$f = 10\text{ MHz}$; $R_L = 50\ \Omega$; Figure 15
Bandwidth -3 dB	300		MHz typ	$R_L = 50\ \Omega$; Figure 13
THD + N	0.18		% typ	$R_L = 100\ \Omega$
Charge Injection	7.5		pC typ	$C_L = 1\text{ nF}$; $V_S = 0\text{ V}$; Figure 16
C_S (Off)	8		pF typ	
C_D (Off)	14		pF typ	
C_D, C_S (On)	23		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.001		μA typ	$V_{DD} = 5.5\text{ V}$; digital inputs = 0 V or V_{DD}
		1	μA max	

¹ Temperature range for B version is -40°C to $+85^\circ\text{C}$.

² Guaranteed by design, not subject to production test.

ADG794

$V_{DD} = 3\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 2.

Parameter	B Version ¹		Unit	Test Conditions/Comments
	25°C	T_{MIN} to T_{MAX}		
ANALOG SWITCH				
Analogue Signal Range		0 to 1.5	V	
On Resistance, R_{ON}	7		Ω typ	$V_D = 0\text{ V}$ to 1 V ; $I_S = -10\text{ mA}$; Figure 8
	9.5	11	Ω max	
On-Resistance Match between Channels, ΔR_{ON}	0.3		Ω typ	$V_D = 0\text{ V}$ to 1 V ; $I_S = -10\text{ mA}$
		0.9	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	2.6		Ω typ	$V_D = 0\text{ V}$ to 1 V ; $I_S = -10\text{ mA}$
		5	Ω max	
LEAKAGE CURRENTS				
Source Off Leakage, I_S (Off)	± 0.001		nA typ	$V_S = 2\text{ V}/1\text{ V}$; $V_D = 1\text{ V}/2\text{ V}$; Figure 9
Drain Off Leakage, I_D (Off)	± 0.001		nA typ	$V_S = 2\text{ V}/1\text{ V}$; $V_D = 1\text{ V}/2\text{ V}$; Figure 9
Channel On Leakage, I_D, I_S (On)	± 0.001		nA typ	$V_D = V_S = 2\text{ V}/1\text{ V}$; Figure 10
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.001		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.1	μA max	
Digital Input Capacitance, C_{IN}		3	pF typ	
DYNAMIC CHARACTERISTICS²				
$t_{ON}, t_{ON}(\overline{EN})$	10		ns typ	$C_L = 35\text{ pF}$; $R_L = 50\ \Omega$
		16	ns max	$V_S = 1.5\text{ V}$; Figure 11
$t_{OFF}, t_{OFF}(\overline{EN})$	6		ns typ	$C_L = 35\text{ pF}$; $R_L = 50\ \Omega$
		10	ns max	$V_S = 1.5\text{ V}$; Figure 11
Break-Before-Make Time Delay, t_D	3		ns typ	$C_L = 35\text{ pF}$; $R_L = 50\ \Omega$
		1	ns min	$V_{S1} = V_{S2} = 1.5\text{ V}$; Figure 12
Off Isolation	-65		dB typ	$f = 10\text{ MHz}$; $R_L = 50\ \Omega$; Figure 14
Channel-to-Channel Crosstalk	-70		dB typ	$f = 10\text{ MHz}$; $R_L = 50\ \Omega$; Figure 15
Bandwidth -3 dB	300		MHz typ	$R_L = 50\ \Omega$; Figure 13
THD + N	0.18		% typ	$R_L = 100\ \Omega$
Charge Injection	4		pC typ	$C_L = 1\text{ nF}$; $V_S = 0\text{ V}$; Figure 16
C_S (Off)	8		pF typ	
C_D (Off)	14		pF typ	
C_D, C_S (On)	23		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.001		μA typ	$V_{DD} = 3.3\text{ V}$; digital inputs = 0 V or V_{DD}
		1	μA max	

¹ Temperature range for B version is -40°C to $+85^\circ\text{C}$.

² Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameters	Ratings
V_{DD} to GND	–0.3 V to +6 V
Analog, Digital Inputs ¹	–0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Continuous Current, S or D	100 mA
Peak Current, S or D	300 mA (pulsed at 1 ms, 10% duty cycle maximum)
Operating Temperature Range Industrial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
QSOP Package, Power Dissipation	566 mW
θ_{JA} Thermal Impedance	149.97°C/W
Lead Temperature, Soldering Reflow, Peak Temperature	260(+0/–5)°C
Time at Peak Temperature	20 sec to 40 sec

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

Table 4. Truth Table

EN	IN	D1	D2	D3	D4	Function
1	X	High-Z	High-Z	High-Z	High-Z	Disable
0	0	S1A	S2A	S3A	S4A	IN = 0
0	1	S1B	S2B	S3B	S4B	IN = 1

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

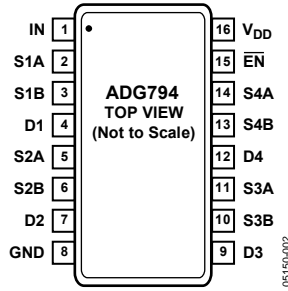


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin NO.	Mnemonic	Description
1	IN	Logic Control Input. The logic level at this input controls the operation of the multiplexers (see Table 4).
2	S1A	A-Side Source Terminal of Mux1. Can be an input or an output.
3	S1B	B-Side Source Terminal of Mux1. Can be an input or an output.
4	D1	Drain Terminal of Mux1. Can be an input or an output.
5	S2A	A-Side Source Terminal of Mux2. Can be an input or an output.
6	S2B	B-Side Source Terminal of Mux2. Can be an input or an output.
7	D2	Drain Terminal of Mux2. Can be an input or an output.
8	GND	Ground Reference.
9	D3	Drain Terminal of Mux3. Can be an input or an output.
10	S3B	B-Side Source Terminal of Mux3. Can be an input or an output.
11	S3A	A-Side Source Terminal of Mux3. Can be an input or an output.
12	D4	Drain Terminal of Mux4. Can be an input or an output.
13	S4B	B-Side Source Terminal of Mux4. Can be an input or an output.
14	S4A	A-Side Source Terminal of Mux4. Can be an input or an output.
15	$\overline{\text{EN}}$	Mux Enable Logic Input. Enables or disables the multiplexers (see Table 4).
16	V _{DD}	Positive Power Supply Voltage.

TERMINOLOGY

V_{DD}

Most positive power supply potential.

I_{DD}

Positive supply current.

GND

Ground (0 V) reference.

S

Source terminal. Can be either an input or an output.

D

Drain terminal. Can be either an input or an output.

IN

Logic control input.

V_D (V_S)

Analog voltage on Terminal D and Terminal S.

R_{ON}

Ohmic resistance between Terminal D and Terminal S.

$R_{FLAT (ON)}$

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured.

ΔR_{ON}

On-resistance match between any two channels.

I_S (Off)

Source leakage current with the switch off.

I_D (Off)

Drain leakage current with the switch off.

I_D, I_S (On)

Channel leakage current with the switch on.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL} (I_{INH})

Input current of the digital input.

C_S (Off)

Off switch source capacitance. Measured with reference to ground.

C_D (Off)

Off switch drain capacitance. Measured with reference to ground.

C_D, C_S (On)

On switch capacitance. Measured with reference to ground.

C_{IN}

Digital input capacitance.

t_{ON}

Delay time between the 50% and the 90% points of the digital input and switch on condition.

t_{OFF}

Delay time between the 50% and the 90% points of the digital input and switch off condition.

t_{BBM}

On or off time measured between the 80% points of both switches when switching from one to another.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during on/off switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

-3 dB Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

THD + N

The ratio of the harmonic amplitudes plus the noise of a signal to the fundamental.

TYPICAL PERFORMANCE CHARACTERISTICS

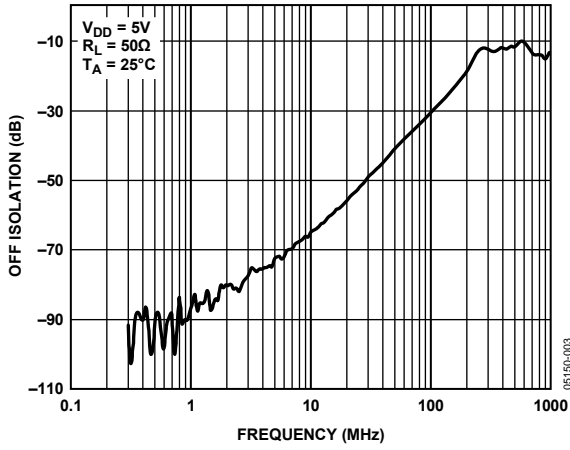


Figure 3. Off Isolation vs. Frequency

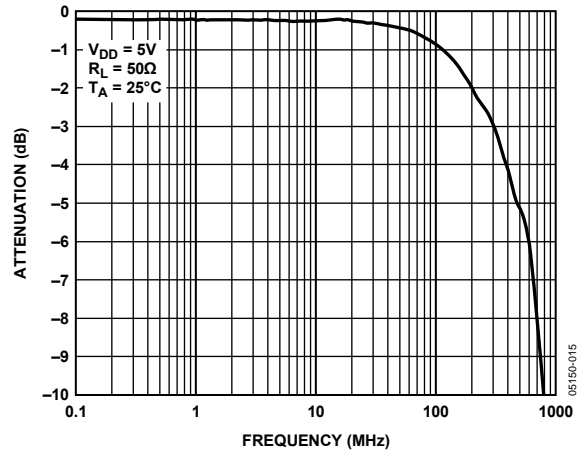


Figure 5. Bandwidth

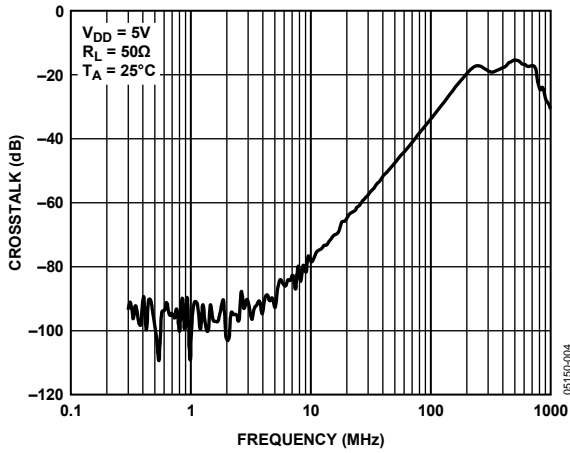


Figure 4. Crosstalk vs. Frequency

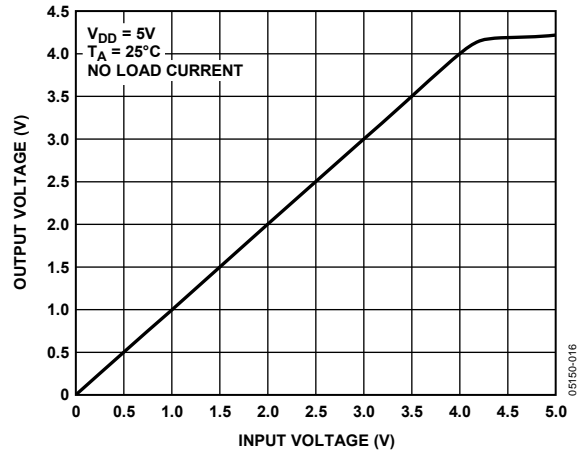


Figure 6. Output Voltage vs. Input Voltage

TYPICAL APPLICATION

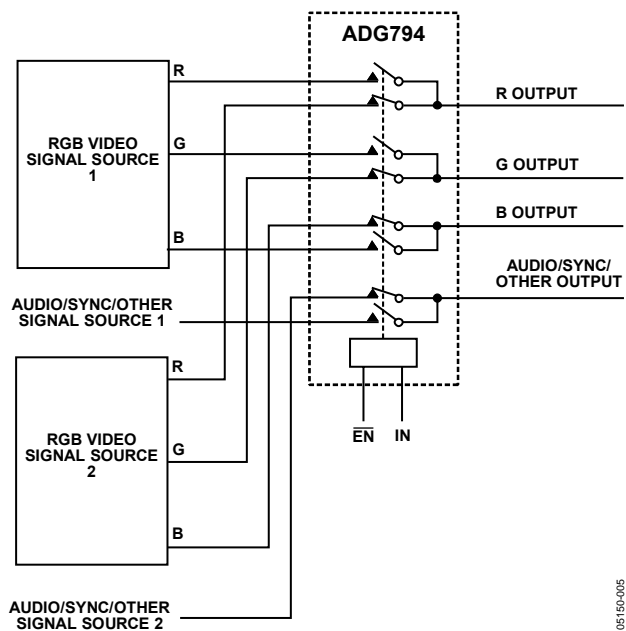


Figure 7. Audio/Video Switch

05150-005

TEST CIRCUITS

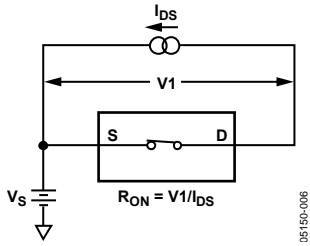


Figure 8. On Resistance

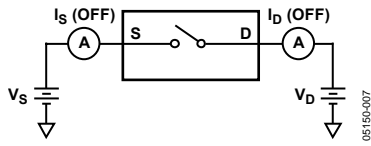


Figure 9. Off Leakage

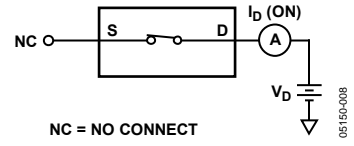


Figure 10. On Leakage

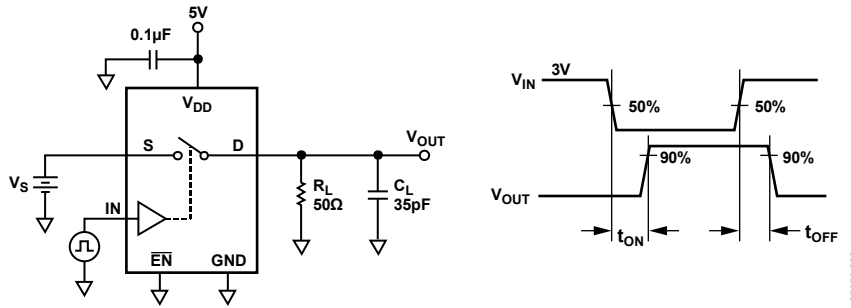


Figure 11. Switching Times

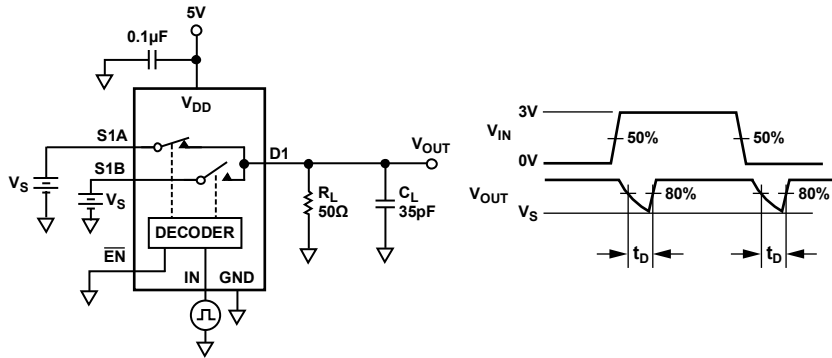


Figure 12. Break-Before-Make Time Delay

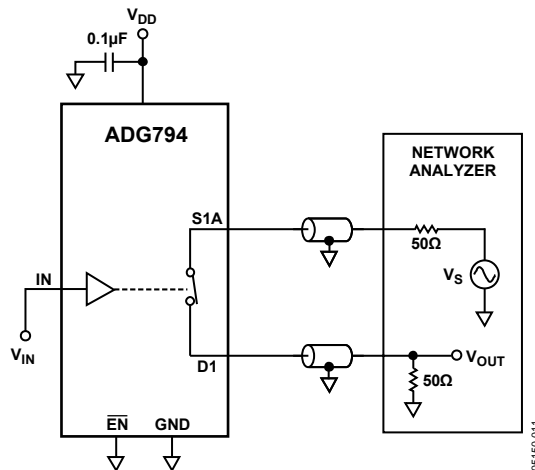


Figure 13. Bandwidth

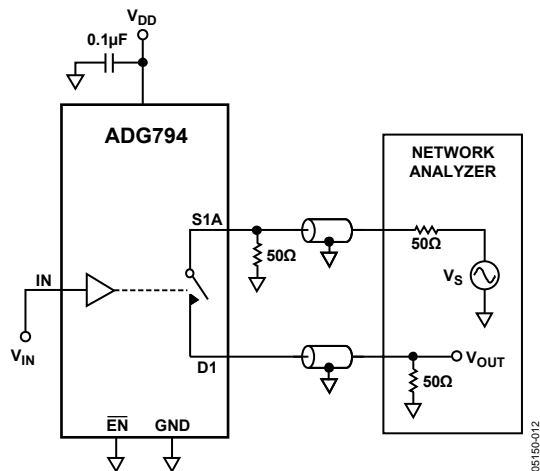


Figure 14. Off Isolation

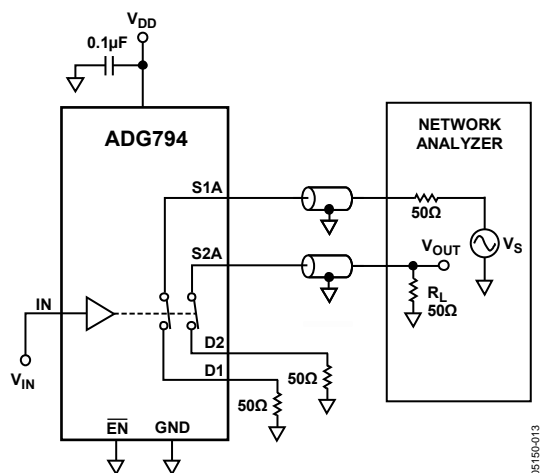


Figure 15. Channel-to-Channel Crosstalk

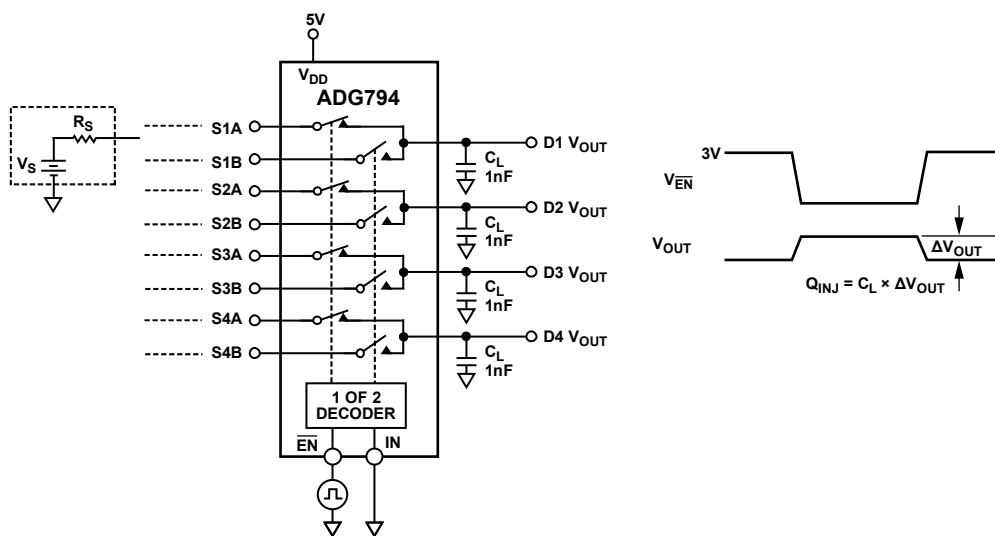
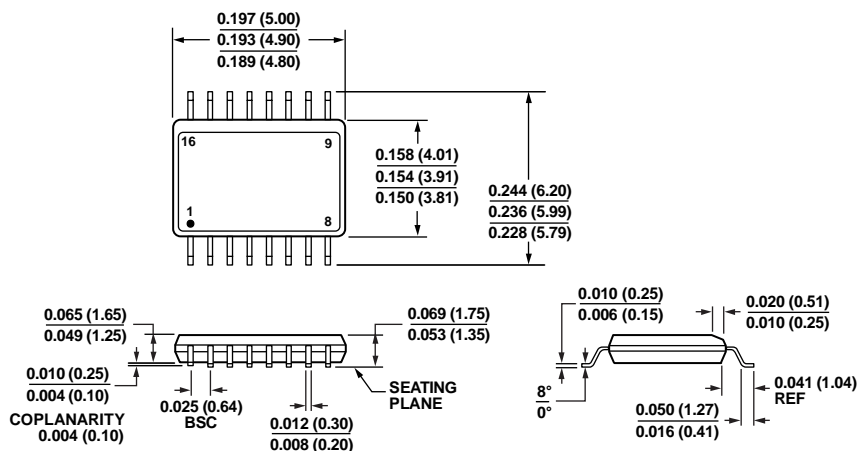


Figure 16. Charge Injection

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137-AB
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 17. 16-Lead Shrink Small Outline Package [QSOP]
 (RQ-16)

Dimensions shown in inches and (millimeters)

012808-A

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG794BRQZ ¹	-40°C to +85°C	16-Lead Shrink Small Outline Package (QSOP)	RQ-16
ADG794BRQZ-500RL7 ¹	-40°C to +85°C	16-Lead Shrink Small Outline Package (QSOP)	RQ-16
ADG794BRQZ-REEL ¹	-40°C to +85°C	16-Lead Shrink Small Outline Package (QSOP)	RQ-16
ADG794BRQZ-REEL7 ¹	-40°C to +85°C	16-Lead Shrink Small Outline Package (QSOP)	RQ-16

¹ Z = RoHS Compliant Part.

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[MUX36S16IRSNR](#) [74LVC1G3157GM-Q10X](#) [TC7W53FK,LF](#) [CD4053BM96](#) [MC74HC4053ADWR2G](#) [SN74LV4051APWR](#)
[HEF4053BT.653](#) [ADG5408BRUZ-REEL7](#) [ADG1404YRUZ-REEL7](#) [ADG1208YRZ-REEL7](#) [MAX4704EUB+T](#) [ADG1406BRUZ-REEL7](#)
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[74HCT4351D.112](#) [74LV4051PW.112](#) [FSA1256L8X_F113](#) [PI5V330QE](#) [PI5V331QE](#) [5962-8771601EA](#) [5962-87716022A](#) [ADG5249FBRUZ](#)
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