Robust, Industrial, Low Latency and Low Power 10 Mbps,100 Mbps, and 1 Gbps Ethernet PHY

Data Sheet **ADIN1300**

FEATURES

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE® 802.3™ compliant
- MII, RMII, and RGMII MAC interfaces
- 1000BASE-T RGMII latency transmit < 68 ns, receive < 226 ns
- 100BASE-TX MII latency transmit< 52 ns, receive < 248 ns
- EMC test standards
  - IEC 61000-4-5 surge (±4 kV)
  - IEC 61000-4-4 electrical fast transient (EFT) (±4 kV)
  - IEC 61000-4-2 ESD (±6 kV contact discharge)
  - IEC 61000-4-6 conducted immunity (10 V)
  - EN55032 radiated emissions (Class A)
  - EN55032 conducted emissions (Class A)
- Unmanaged configuration using multilevel pin strapping
- EEE in accordance with IEEE 802.3az
- Start of packet detection for IEEE 1588 time stamp support
- Enhanced link detection
- Configurable LED
- Crystal oscillator frequency/25 MHz clock input frequency (50 MHz for RMII)
- 25 MHz/125 MHz synchronous clock output
- Small package and wide temperature range
  - 40-lead, 6 mm × 6 mm LFCSP
  - Specified for −40°C to +105°C ambient operation
- Low power consumption
  - 330 mW for 1000BASE-T
  - 140 mW for 100BASE-TX
  - 3.3 V/2.5 V/1.8 V MAC interface VDDIO supply
  - Integrated power supply monitoring and POR

APPLICATIONS

- Industrial automation
- Process control
- Factory automation
- Robotics/motion control
- Time sensitive networking (TSN)
- Building automation
- Test and measurement
- Industrial internet of things (IoT)

GENERAL DESCRIPTION

The ADIN1300 is a low power, single port, Gigabit Ethernet transceiver with low latency and power consumption specifications primarily designed for industrial Ethernet applications.

This design integrates an energy efficient Ethernet (EEE) physical layer device (PHY) core with all associated common analog circuitry, input and output clock buffering, management interface and subsystem registers, and MAC interface and control logic to manage the reset and clock control and pin configuration.

The ADIN1300 is available in a 6 mm × 6 mm, 40-lead lead frame chip scale package (LFCSP). The device operates with a minimum of 2 power supplies, 0.9 V and 3.3 V, assuming the use of a 3.3 V MAC interface supply. For maximum flexibility in system level design, a separate VDDIO supply enables the management data input/output (MDIO) and MAC interface supply voltages to be configured independently of the other circuitry on the ADIN1300, allowing operation at 1.8 V, 2.5 V, or 3.3 V. At power-up, the ADIN1300 is held in hardware reset until each of the supplies has crossed its minimum rising threshold value. Brown-out protection is provided by monitoring the supplies to detect if one or more supply drops below a minimum falling threshold (see Table 17), and holding the device in hardware reset until the power supplies return and satisfy the power-on reset (POR) circuit.

The MII management interface (also referred to as MDIO interface) provides a 2-wire serial interface between a host processor or MAC (also known as management station (STA)) and the ADIN1300, allowing access to control and status information in the PHY core management registers. The interface is compatible with both the IEEE 802.3 Standard Clause 22 and Clause 45 management frame structures.

The ADIN1300 can support cable lengths up to 150 meters at Gigabit speeds and 180 meters when operating at 100 Mbps or 10 Mbps.

Note that throughout this data sheet, multifunction pins, such as XTAL_I/CLK_IN/REF_CLK, are referred to either by the entire pin name or by a single function of the pin, for example, XTAL_I/CLK_IN, when only that function is relevant.

Rev. 0 Document Feedback

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REVISION HISTORY

10/2019—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

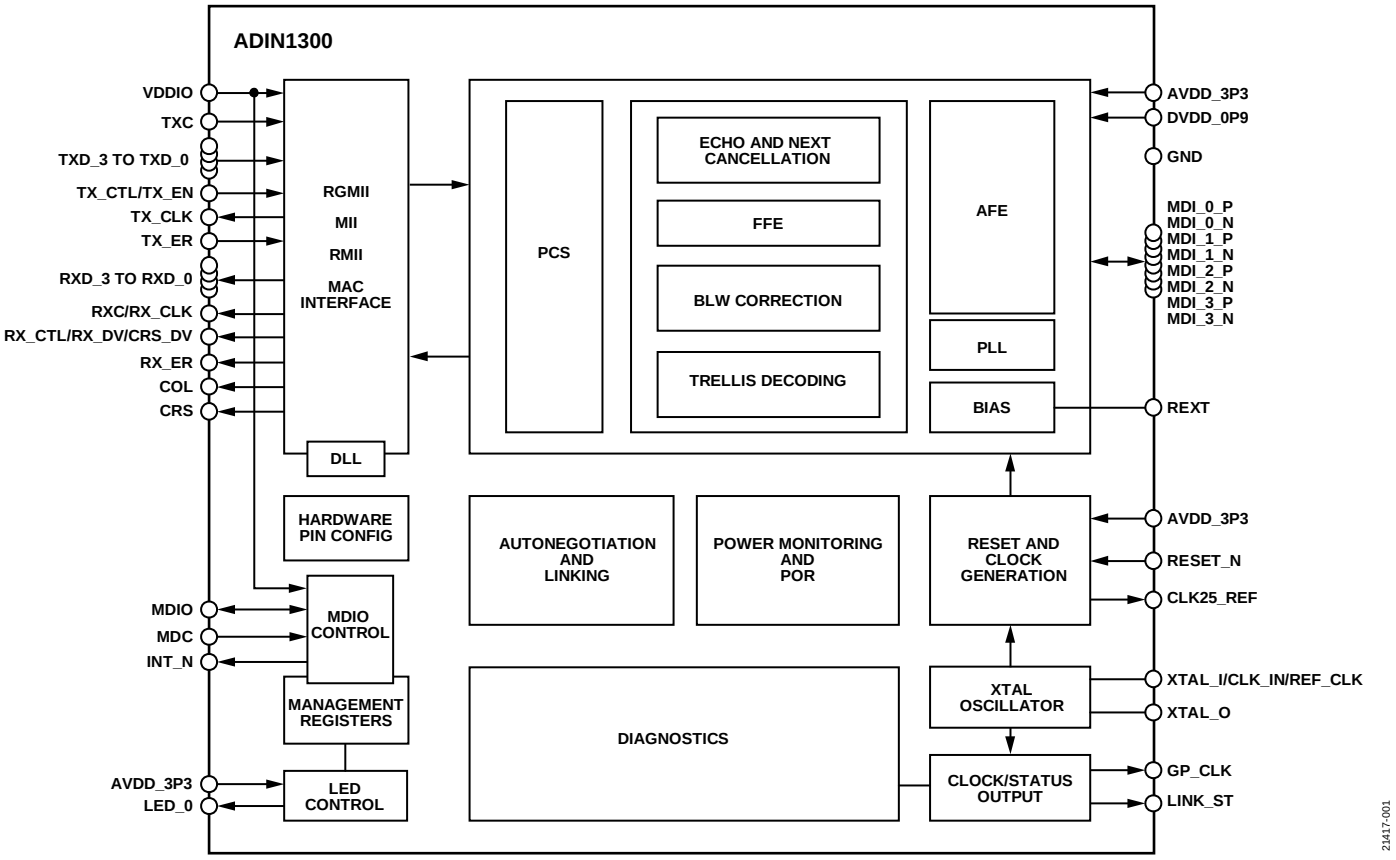


Figure 1.

SPECIFICATIONS

AVDD_3P3 = 3.3 V, VDDIO = 1.8 V, DVDD_0P9 = 0.9 V, all specifications at −40°C to +105°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
Supply Voltages					
AVDD_3P3	3.14	3.3	3.46	V	
DVDD_0P9	0.855	0.9	0.945	V	
VDDIO	3.14	3.3	3.46	V	
	2.25	2.5	2.75	V	
	1.71	1.8	1.89	V	
POWER CONSUMPTION[1]					100% data throughput, full activity
Supply Current RGMII 1000BASE-T					
AVDD_3P3 Current (I_{AVDD_3P3})		70.5		mA	
DVDD_0P9 Current (I_{DVDD_0P9})		38		mA	
VDDIO Current (I_{VDDIO})		48		mA	VDDIO = 3.3 V
		41		mA	VDDIO = 2.5 V
		35		mA	VDDIO = 1.8 V
Supply Current 100BASE-TX					RGMII, RMII, MII interfaces
I_{AVDD_3P3}		35		mA	
I_{DVDD_0P9}		12		mA	
I_{VDDIO}		11		mA	VDDIO = 3.3 V
		10		mA	VDDIO = 2.5 V
		9		mA	VDDIO = 1.8 V
Power					100% data throughput, full activity
1000BASE-T, RGMII		425		mW	VDDIO = 3.3 V
		370		mW	VDDIO = 2.5 V
		330		mW	VDDIO = 1.8 V
100BASE-TX		159		mW	VDDIO = 3.3 V
		148		mW	VDDIO = 2.5 V
		140		mW	VDDIO = 1.8 V
TIMING/LATENCY[2]					
1000BASE-T RGMII					
Transmit	60	64	68	ns	
Receive			226	ns	
Total	286	290	294	ns	
100BASE-TX MII					
Transmit			52	ns	
Receive			248	ns	
Total			300	ns	
100BASE-TX RGMII[3]					
Transmit	84	88	92	ns	
Receive			250	ns	
Total	334	338	342	ns	
100BASE-TX RGMII[4]					
Transmit	84	104	124	ns	
Receive			250	ns	
Total	334	354	374	ns	
100BASE-TX RMII[5]					
Transmit	72		92	ns	
Receive	328	348	368	ns	
Total	400	430	460	ns	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUTS/OUTPUTS					Applies to MAC interface, MDC pin, MDIO pin, and INT_N pin
VDDIO = 3.3 V					
Input Low Voltage (V_{IL})			0.8	V	
Input High Voltage (V_{IH})	2.0			V	
Output Low Voltage (V_{OL})			0.4	V	Output low current (I_{OL}) (min) = 4 mA
Output High Voltage (V_{OH})	2.4			V	Output high current (I_{OH}) (min) = 4 mA
VDDIO = 2.5 V					
V_{IL}			0.7	V	
V_{IH}	1.7			V	
V_{OL}			0.4	V	I_{OL} (min) = 4 mA
V_{OH}	2.0			V	I_{OH} (min) = 2 mA
	1.7				I_{OH} (min) = 4 mA
VDDIO = 1.8 V					
V_{IL}			0.35 × VDDIO	V	
V_{IH}	0.65 × VDDIO			V	
V_{OL}			0.45	V	I_{OL} (min) = 2 mA
V_{OH}	VDDIO − 0.45			V	I_{OH} (min) = 2 mA
AVDD_3P3					Applies to COL/TX_ER function of the LED_0/COL/TX_ER/PHY_CFG0 pin
V_{IL}			0.8	V	
V_{IH}	2.0			V	
V_{OL}			0.4	V	I_{OL} (min) = 4 mA
V_{OH}	2.4			V	I_{OH} (min) = 4 mA
Input Leakage Current High (I_{IH}) and Input Leakage Current Low (I_{IL})			10	µA	Except pins with internal pull-down resistors
LED OUTPUT					Applies to LED_0
Output Drive Current	8			mA	AVDD_3P3 = 3.3 V
CLOCKS					
External Crystal (XTAL)					Requirements for external crystal used on XTAL_I pin and XTAL_O pin
Crystal Frequency		25		MHz	
Crystal Frequency Tolerance	−50		+50	ppm	
Crystal Output Drive Level		<200		µW	
Crystal ESR		20	100	Ω	
Crystal Load Capacitance (C_L)[6]		10		pF	
XTAL_I Jitter			80	ps	Over frequency range 10 kHz to 5 MHz
Clock Input Frequency (CLK_IN)		25		MHz	Requirements for external clock applied to XTAL_I pin, MII, RGMII modes
		50		MHz	RMII mode
Clock Input Voltage Range (CLK_IN)			2.5	V	

[1] MAC interface capacitive load of 5 pF, REFCLK is disabled.
[2] The DPTH_MII_BYTE register defines whether the programmed transmit first in, first out (FIFO) depth is bytes or nibbles for MII modes (10BASE-Te and 100BASE-TX). The register defaults to 1, which corresponds to bytes. In MII mode, because the interface is nibble based, the internal prefill in the transmit FIFO is larger and is observed as longer latency times. The latency specifications in Table 1 have this bit set to 0 for MII.
[3] This 100BASE-TX RGMII transmit latency is where the transit FIFO is programmed for synchronous operation (MAC transmit clock must be synchronous with the ADIN1300 reference clock), see the FIFO_SYNC register.
[4] This 100BASE-TX RGMII transmit latency is where the MAC transmit clock does not have to be synchronous with the ADIN1300 reference clock and the transmit FIFO takes care of any phase difference.
[5] The RMII transmit latency depends on the phase relationship between the 50 MHz reference clock and the internal 25 MHz clock. The transmit latency is fixed for a given link.
[6] Where load capacitance (C_L) = ((C1 × C2)/(C1 + C2) + C_{STRAY}), where C_{STRAY} is the stray capacitance including routing and package parasitics.

TIMING CHARACTERISTICS

Power-Up Timing

Table 2. Power-Up Timing

Parameter	Description	Min	Typ	Max	Unit
t_{RAMP}	Power supply ramp time			40	ms
t_1	Minimum time interval to internal power good[1]		6.8		ms
t_2	XTAL_I crystal settling time		1.5	2	ms
	XTAL_I external clock settling time			20	µs
t_3	Hardware configuration latch time			64	µs
t_4	Management interface active			5	ms

[1] The minimum time interval is referenced to the last supply to reach its rising threshold. There is no specific power supply sequencing required.

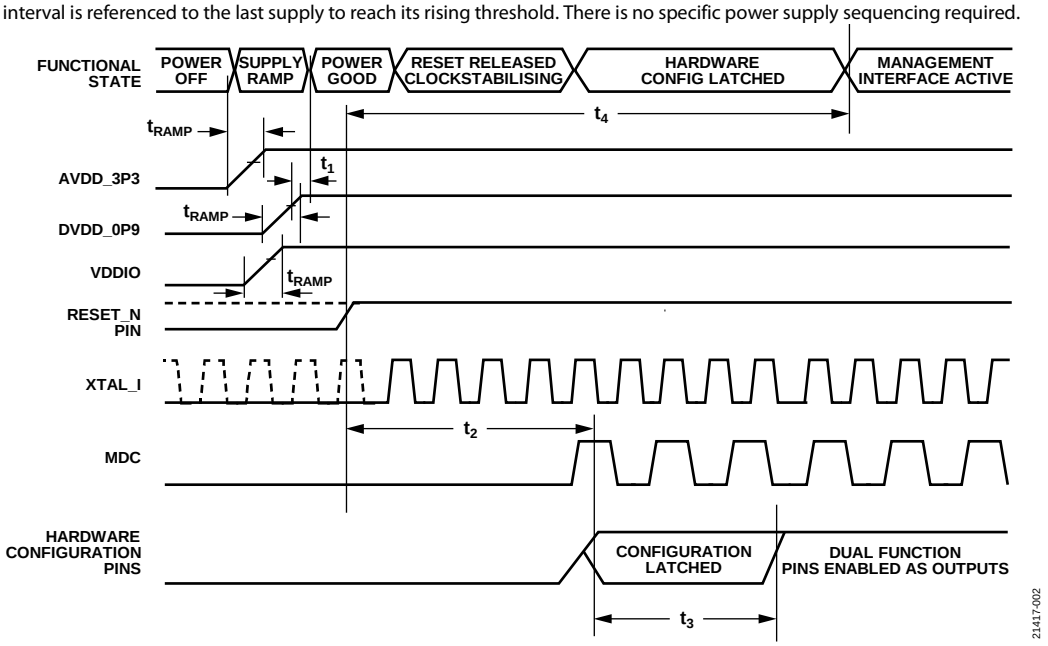


Figure 2. Power-Up Timing

Hardware Reset Timing

Table 3. Hardware Reset Timing

Parameter	Description	Min	Typ	Max	Unit
t_1	RESET_N low time	10			µs
t_2	XTAL_I crystal settling time		1.5		ms
	XTAL_I external clock settling time		0		ms
t_3	Hardware configuration latch time			64	µs
t_4	Management interface active			5	ms

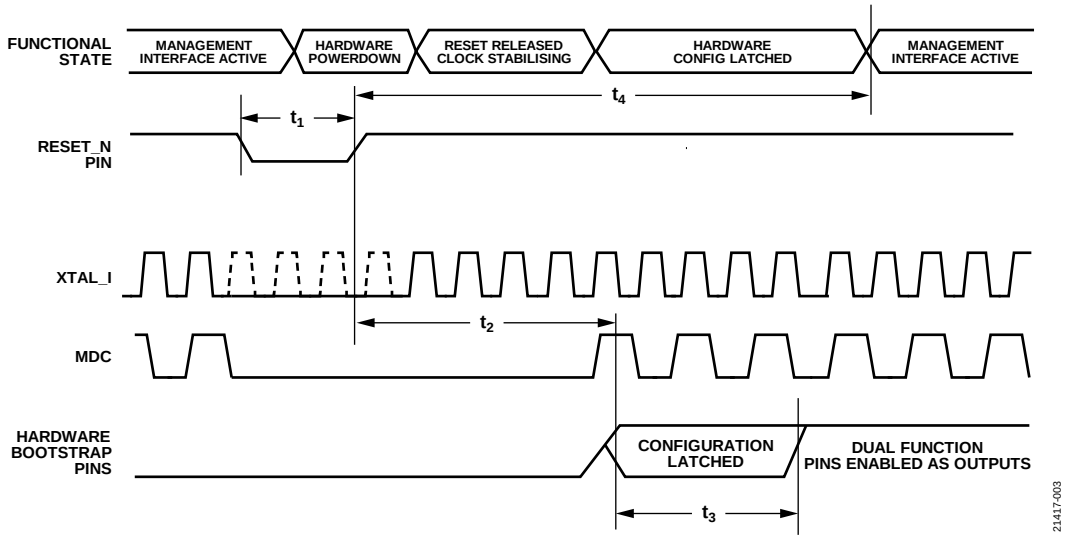


Figure 3. Hardware Reset Timing

Management Interface Timing

Table 4. Management Interface Timing

Parameter	Description	Min	Typ	Max	Unit
t_1	MDC period	180			ns
t_2	MDC high time	70			ns
t_3	MDC low time	70			ns
t_4	MDC rise/fall time			5	ns
t_5	MDIO signal setup time to MDC	10			ns
t_6	MDIO signal hold time to MDC	10			ns
t_7	MDIO delay time to MDC	0		60	ns

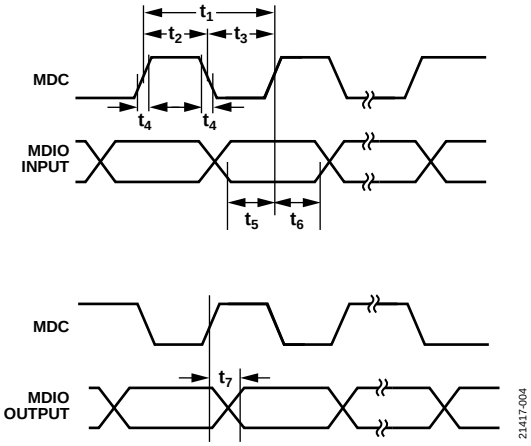


Figure 4. Management Interface Timing

MII Transmit and Receive Timing

Table 5. MII 100BASE-TX Transmit Timing

Parameter	Description	Min	Typ	Max	Unit
t_1	TX_CLK period		40		ns
t_2	TX_CLK high time	14	20	26	ns
t_3	TX_CLK low time	14	20	26	ns
t_4	TX_CLK rise/fall time		5		ns
t_5	MII input signal (TXD_0 to TXD_3, TX_EN, TX_ER) setup time to TX_CLK	10			ns
t_6	MII input signal (TXD_0 to TXD_3, TX_EN, TX_ER) hold time to TX_CLK	0			ns

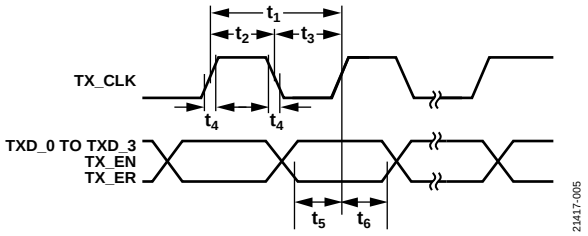


Figure 5. MII Transmit Timing

Table 6. MII 100BASE-TX Receive Timing

Parameter	Description	Min	Typ	Max	Unit
t_1	RX_CLK period		40		ns
t_2	RX_CLK high time	16	20	24	ns
t_3	RX_CLK low time	16	20	24	ns
t_4	RX_CLK rise/fall time			1	ns
t_5	MII output signal (RXD_0 to RXD_3, RX_EN, RX_ER) setup time to RX_CLK	10			ns
t_6	MII output signal (RXD_0 to RXD_3, RX_EN, RX_ER) hold time to RX_CLK	10			ns

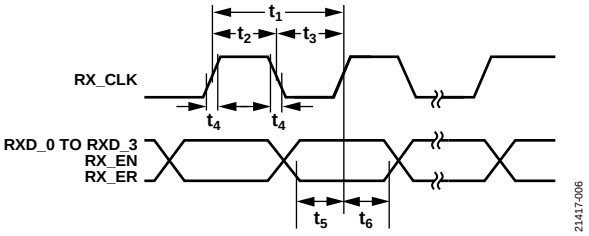


Figure 6. MII Receive Timing

Table 7. MII 10BASE-Te Transmit Timing (see Figure 5)

Parameter	Description	Min	Typ	Max	Unit
t_1	TX_CLK period		400		ns
t_2	TX_CLK high time	140	200	260	ns
t_3	TX_CLK low time	140	200	260	ns
t_4	TX_CLK rise/fall time		1		ns
t_5	MII input signal (TXD_0 to TXD_3, TX_EN, TX_ER) setup time to TX_CLK	10			ns
t_6	MII input signal (TXD_0 to TXD_3, TX_EN, TX_ER) hold time to TX_CLK	0			ns

Table 8. MII 10BASE-Te Receive Timing (see Figure 6)

Parameter	Description	Min	Typ	Max	Unit
t_1	RX_CLK period		400		ns
t_2	RX_CLK high time	140	200	260	ns
t_3	RX_CLK low time	140	200	260	ns
t_4	RX_CLK rise/fall time		1	1	ns
t_5	MII output signal (RXD_0 to RXD_3, RX_EN, RX_ER) setup time to RX_CLK	10			ns
t_6	MII output signal (RXD_0 to RXD_3, RX_EN, RX_ER) hold time to RX_CLK	10			ns

RGMII Transmit/Receive

Table 9. RGMII Timing

Parameter	Description	Min	Typ	Max	Unit
t_1	Data to clock output skew (at transmitter)[1]	−500	0	+500	ps
t_2	Data to clock input skew (at receiver)[1]	1	1.8	2.6	ns
t_3	Data to clock output setup time (at transmitter – internal delay)[2]	1.2	2.0		ns
t_4	Clock to data output hold time (at transmitter – internal delay)[2]	1.2	2.0		ns
t_5	Data to clock input setup time (at receiver – internal delay)[2]	1.0	2.0		ns
t_6	Clock to data input hold time (at receiver – internal delay)[2]	1.0	2.0		ns
t_{CYC}	Clock cycle duration[3]	7.2	8	8.8	ns

Parameter	Description	Min	Typ	Max	Unit
Duty_G	Duty cycle for Gigabit	45	50	55	%
Duty_T	Duty cycle for 10/100 Mbps	40	50	60	%
t_R/t_F	Rise/fall time (20% to 80%)			0.75	ns

[1] When operating without RGMII internal delay, the printed circuit board (PCB) design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal. For 10/100 Mbps, the max value is unspecified.
[2] Hardware and software programmable internal delay may be enabled or disabled.
[3] For 10 Mbps and 100 Mbps, t_{CYC} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.

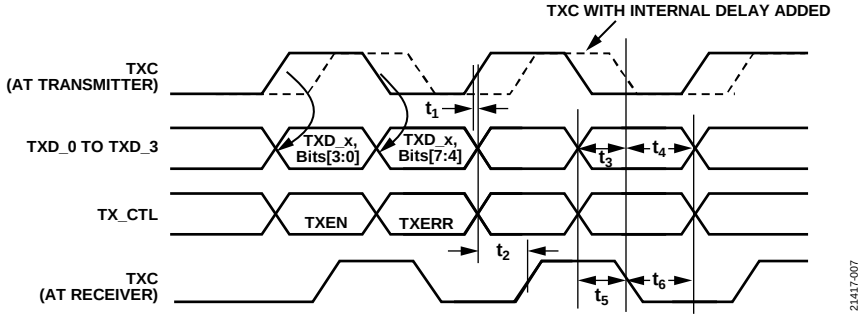


Figure 7. RGMII Transmit Timing

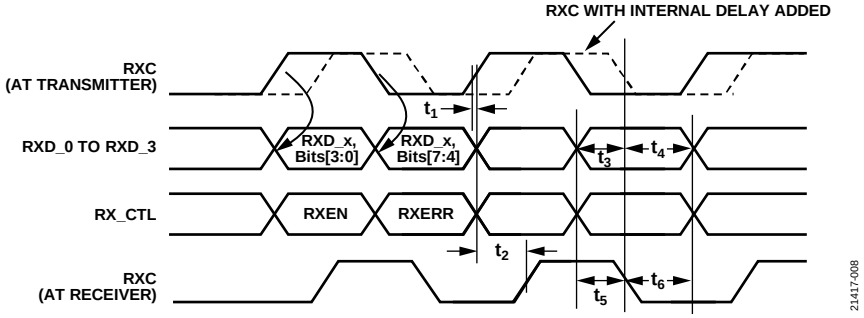


Figure 8. RGMII Receive Timing

RMII Transmit/Receive

Table 10. RMII Timing

Parameter	Description	Min	Typ	Max	Unit
REF_CLK Frequency	Frequency of the REF_CLK		50		MHz
REF_CLK Duty Cycle	Duty Cycle of the REF_CLK	35		65	%
t_1	TXD_0, TXD_1, TX_EN, RXD_0, RXD_1, CRS_DV, RX_ER data setup to REF_CLK rising edge	4			ns
t_2	TXD_0, TXD_1, TX_EN, RXD_0, RXD_1, CRS_DV, RX_ER data hold from REF_CLK rising edge	2			ns
t_3	Output rise/fall time	1		5	ns

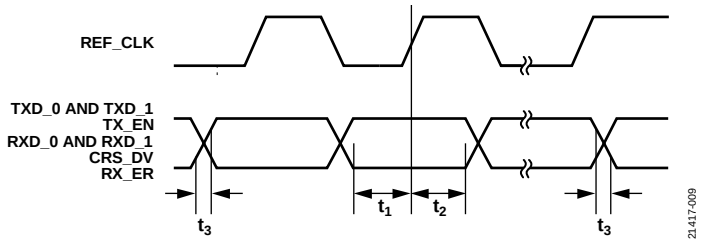


Figure 9. RMII Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 11.

Parameter	Rating
VDDIO to GND	−0.3 V to +3.63 V
DVDD_0P9 to GND	−0.3 V to +1.1 V
AVDD_3P3 to GND	−0.3 V to +3.63 V
MAC Interface to GND	−0.3 V to VDDIO + 0.3 V
LINK_ST, GP_CLK	−0.3 V to VDDIO + 0.3 V
MDIO, MDC, INT_N to GND	−0.3 V to +3.63 V
MDI_x_x to GND	−0.3 V to AVDD_3P3 + 0.3 V
LED_0, RESET_N, XTAL_I/CLK_IN/REF_CLK, XTAL_O, CLK25_REF	−0.3 V to AVDD_3P3 + 0.3 V
Operating Temperature Range (T_A)	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Maximum)	125°C
Power Dissipation	(T_J maximum − T_A)/θ_{JA}
Lead Temperature	JEDEC industry-standard
Soldering	J-STD-020
Electrostatic Discharge (ESD)	
Human Body Model (HBM)	
MDI_x_x Pins	4 kV
All Other Pins	2 kV
Machine Model (MM)	200 V
Field Induced Charged Device Model (FICDM)	1.25 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 12. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-40-26	45[1]	25[1]	°C/W
	30[2]		°C/W

[1] Based on simulated data using a JEDEC 2s2p thermal test board with a 3 × 3 array of thermal vias in a JEDEC natural convection environment. See JEDEC specification JESD-51 for details.
[2] Test Condition 1: thermal impedance measured on Analog Devices, Inc., hardware, 2S2P with 4 × 4 via array.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

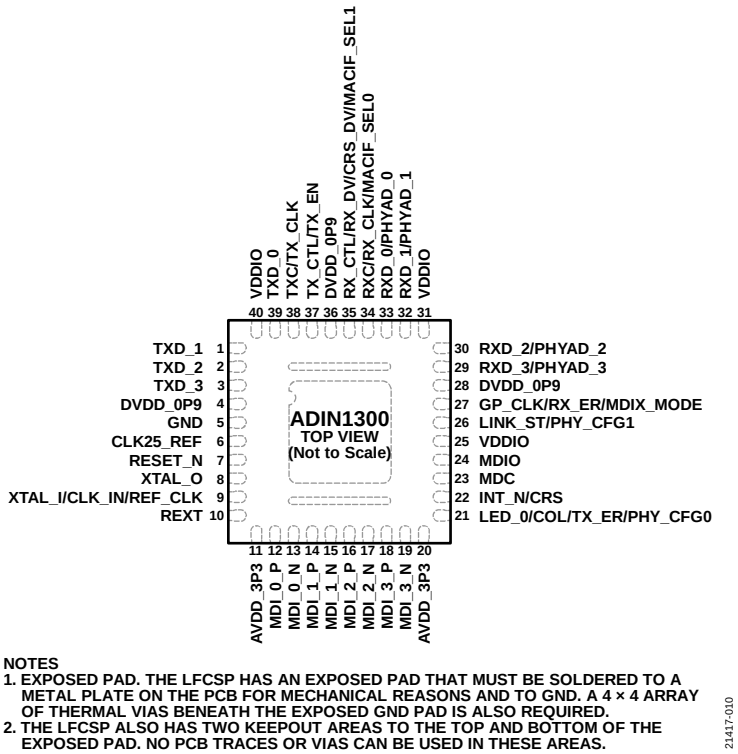


Figure 10. Pin Configuration

Table 13. Pin Function Descriptions

Pin No.	Mnemonic	Description
Clock Interface		
8	XTAL_O	Second Terminal for Crystal Connection. If using a single-ended reference clock on XTAL_I/CLK_IN/REF_CLK, leave XTAL_O open circuit.
9	XTAL_I/CLK_IN/REF_CLK	Input for Crystal (XTAL_I). Single-Ended 25 MHz Reference Clock (CLK_IN). 50 MHz RMII Reference Clock Input in RMII Mode (REF_CLK).
Management Interface		
22	INT_N/CRS	Management Interface Interrupt Pin Output (INT_N). Active low output. A low on INT_N indicates an unmasked management interrupt. This pin requires a 1.5 kΩ pull-up resistor to VDDIO. MII Carrier Sense Output (CRS). Indicates the presence of a carrier to MAC.
23	MDC	Management Data Clock Input up to 5.5 MHz.
24	MDIO	Management Data Open-Drain Input/Output Synchronous to the MDC Clock. This pin requires a 1.5 kΩ pull-up resistor to VDDIO.
Reset		
7	RESET_N	Active Low Input. Hold low for >10 µs. This pin requires a1 kΩ pull-up resistor to AVDD_3P3.
Media Dependent Interface (MDI)		
12	MDI_0_P	Transmit/Receive Differential Pair 0 Supporting 10 Mbps, 100 Mbps, and 1 Gbps.
13	MDI_0_N	Transmit/Receive Differential Pair 0 Supporting 10 Mbps, 100 Mbps, and 1 Gbps.
14	MDI_1_P	Transmit/Receive Differential Pair 1 Supporting 10 Mbps, 100 Mbps, and 1 Gbps.
15	MDI_1_N	Transmit/Receive Differential Pair 1 Supporting 10 Mbps, 100 Mbps, and 1 Gbps.
16	MDI_2_P	Transmit/Receive Differential Pair 2 for 1000BASE-T Mode. Unused in other modes.
17	MDI_2_N	Transmit/Receive Differential Pair 2 for 1000BASE-T Mode. Unused in other modes.

Pin No.	Mnemonic	Description
18	MDI_3_P	Transmit/Receive Differential Pair 3 for 1000BASE-T Mode. Unused in other modes.
19	MDI_3_N	Transmit/Receive Differential Pair 3 for 1000BASE-T Mode. Unused in other modes.
MAC Interface		
1	TXD_1	RGMII/RMII/MII Transmit Data 1 Input. See the MAC Interface section.
2	TXD_2	RGMII/MII Transmit Data 2 Input. See the MAC Interface section.
3	TXD_3	RGMII/MII Transmit Data 3 Input. See the MAC Interface section.
29	RXD_3/PHYAD_3[1]	RGMII/MII Receive Data 3 Output (RXD_3). See the MAC Interface section. PHY Address Hardware Configuration Pin (PHYAD_3).
30	RXD_2/PHYAD_2[1]	RGMII/MII Receive Data 2 Output (RXD_2). See the MAC Interface section. PHY Address Hardware Configuration Pin (PHYAD_2).
32	RXD_1/PHYAD_1[1]	RGMII/RMII/MII Receive Data 1 Output (RXD_1). See the MAC Interface section. PHY Address Hardware Configuration Pin (PHYAD_1).
33	RXD_0/PHYAD_0[1]	RGMII/RMII/MII Receive Data 0 Output (RXD_0). See the MAC Interface section. PHY Address Hardware Configuration Pin (PHYAD_0).
34	RXC/RX_CLK/MACIF_SEL0[1]	RGMII Receive Clock Output (RXC). 125 MHz at 1 Gbps, 25 MHz at 100 Mbps, 2.5 MHz at 10 Mbps. MII Receive Clock Output (RX_CLK). 25 MHz at 100 Mbps, 2.5 MHz at 10 Mbps. MAC Interface Selection Hardware Configuration Pin (MACIF_SEL0). See Table 25.
35	RX_CTL/RX_DV/ CRS_DV/MACIF_SEL1[1]	RGMII Receive Control Signal (RX_CTL). This is a combination of the RX_DV and RX_ER signals using both edges of RXC. MII Mode Received Data Valid Output (RX_DV). When asserted high, it indicates that valid data is present on the RXD_0 pin to RXD_3 pin in MII mode. RMII Mode Carrier Sense/Received Data Valid Signal (CRS_DV). This is a combination of the CRS and RX_DV signals and is asserted while the receive medium is nonidle. See the RMII Interface Mode section. MAC Interface Selection Hardware Configuration Pin (MACIF_SEL1). See Table 25.
37	TX_CTL/TX_EN	RGMII Transmit Control Signal (TX_CTL). This is a combination of the TX_EN and TX_ER signals using both edges of TXC. RMII/MII Mode Transmit Enable Input from the MAC to the PHY (TX_EN). This indicates that transmission data is available on the TXD_x lines.
38	TXC/TX_CLK	RGMII Transmit Clock Input (TXC). 125 MHz at 1 Gbps, 25 MHz at 100 Mbps, 2.5 MHz at 10 Mbps from MAC to PHY. MII Output Clock from PHY to MAC (TX_CLK). The TX_CLK frequency is 2.5 MHz in 10BASE-Te mode and 25 MHz in 100BASE-TX mode. TX_CLK has a constant phase relationship to the XTAL_I/CLK_IN clock.
39	TXD_0	RGMII/RMII/MII Transmit Data 0 Input. See the MAC Interface section.
LED Interface		
21	LED_0/COL/TX_ER/ PHY_CFG0[1]	Programmable LED Indicator for General-Purpose LED with 8 mA Drive Capability (LED_0). The LED can be active high or active low. Recommended use is active low. The ADIN1300 automatically senses the connection of the LED during power-up and reset. By default, LED_0 is on when a link is established and blinking when there is activity (this behavior can be changed by software). MII Collision Detect Output (COL). This indicates a collision condition. MII Transmit Error Detected Input from the MAC to the PHY (TX_ER). Only available by default when EEE advertisement is enabled using the hardware pin configuration (see Table 23). 4-Level Hardware Configuration Pin for PHY Configuration (PHY_CFG0) (see Table 23).
Other Pins		
6	CLK25_REF	Analog Reference Clock Output. The 25 MHz, 3.3 V reference clock from the crystal oscillator is available on the CLK25_REF pin.
10	REXT	External Bias Reference Resistor. Connect a 1% 3.01 kΩ resistor (1% tolerance, 100 ppm/°C temperature coefficient (TC)) to GND.
26	LINK_ST/PHY_CFG1[1]	General-Purpose Output Used to Output Link Status (LINK_ST). This indicates whether a valid link has been established. LINK_ST is active high by default (this can be changed by software). 4-Level Hardware Configuration Pin for PHY Configuration (PHY_CFG1) (see Table 23).

Pin No.	Mnemonic	Description
27	GP_CLK/RX_ER/ MDIX_MODE[1]	General-Purpose Output on which PHY Clocks can be Made Available (GP_CLK). RMII/MII Mode Receive Error Detected Output (RX_ER). When asserted high, it indicates that the PHY has detected a receive error. 4-Level Hardware Configuration Pin for Auto-MDIX Configuration (MDIX_MODE). See Table 24.
Power and Ground Pins		
4, 28, 36	DVDD_0P9	0.9 V Digital Core Power Supply Input. Connect 0.1 µF and 0.01 µF capacitors to GND as close as possible to these pins.
5	GND	This pin must be connected to GND on the board.
11, 20	AVDD_3P3	3.3 V Power Supply Input for the PHY Interface, Analog Circuitry, Crystal Oscillator, DLL, RESET_N, CLK25_REF Generation, and LED Circuitry. Connect 0.1 µF and 0.01 µF capacitors to GND as close as possible to these pins.
25, 31, 40	VDDIO	3.3 V/2.5 V/1.8 V MDIO and MAC Interface Power Supply Input. Connect 0.1 µF and 0.01 µF capacitors to GND as close as possible to these pins. If using 3.3 V, to minimize power supplies, VDDIO and AVDD_3P3 can be connected to the same supply.
	EP	Exposed Pad. The LFCSP package has an exposed pad that must be soldered to a metal plate on the PCB for mechanical reasons and to GND. A 4 × 4 array of thermal vias beneath the exposed GND pad is also required.

[1] In cases where a pin is shared between a functional signal(s) and a hardware pin configuration signal(s), the hardware pin configuration signal(s) is the last name in the mnenomic and the pin is referred to using the functional signal(s) name throughout the data sheet.

Table 14. Pin Function Descriptions For Each MAC Interface Option

		MAC Interface Pin Function[2]			
Pin No.	Mnemonic[1]	RGMII	MII and EEE Advertisement Disabled[3]	MII and EEE Advertisement Enabled[3,4]	RMII
1	TXD_1	TXD_1	TXD_1	TXD_1	TXD_1
2	TXD_2	TXD_2	TXD_2	TXD_2	
3	TXD_3	TXD_3	TXD_3	TXD_3	
9	XTAL_I/CLK_IN/REF_CLK				REF_CLK[5]
21	LED_0[6]/COL/TX_ER		COL	TX_ER[7]	
22	INT_N[6]/CRS		CRS		
27	GP_CLK[6]/RX_ER		RX_ER	RX_ER	RX_ER
29	RXD_3	RXD_3	RXD_3	RXD_3	
30	RXD_2	RXD_2	RXD_2	RXD_2	
32	RXD_1	RXD_1	RXD_1	RXD_1	RXD_1
33	RXD_0	RXD_0	RXD_0	RXD_0	RXD_0
34	RXC/RX_CLK	RXC	RX_CLK	RX_CLK	
35	RX_CTL/RX_DV/CRS_DV	RX_CTL	RX_DV	RX_DV	CRS_DV
37	TX_CTL/TX_EN	TX_CTL	TX_EN	TX_EN	TX_EN
38	TXC/TX_CLK	TXC	TX_CLK	TX_CLK	
39	TXD_0	TXD_0	TXD_0	TXD_0	TXD_0

[1] Hardware pin configuration signal(s) have been omitted for clarity.
[2] Wherever the field is left blank, the pin function is the first function listed in the Mnemonic column.
[3] EEE advertisement enabled/disabled using the hardware pin configuration. See the Hardware Configuration Pins section.
[4] EEE does not support half duplex. Therefore, no CRS pin or COL pin is required.
[5] A 50 MHz reference clock must be supplied on the XTAL_I/CLK_IN/REF_CLK pin when using the RMII MAC interface option.
[6] These pin functions can also be reconfigured via software.
[7] Because TX_ER shares a pin with COL, this pin is grouped with the PHY output pins, even though TX_ER is actually a PHY input pin.

TYPICAL PERFORMANCE CHARACTERISTICS

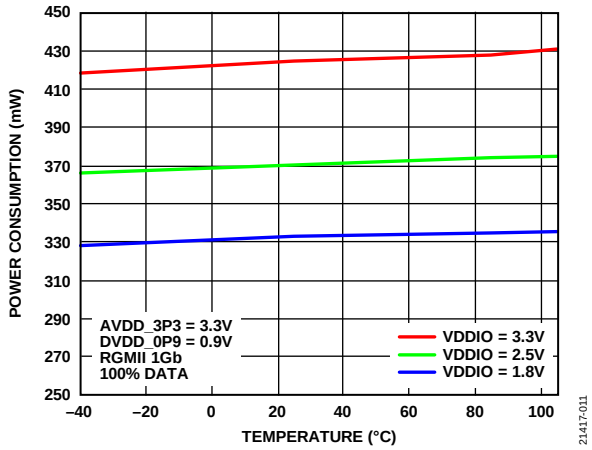


Figure 11. Power Consumption vs. Temperature, VDDIO Supply, 1 Gb, 100% Data

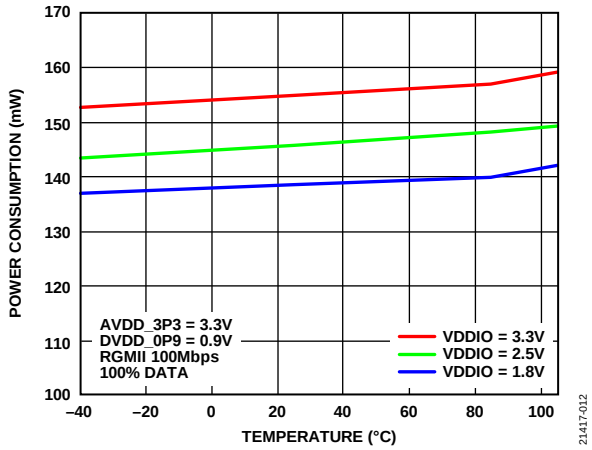


Figure 12. Power Consumption vs. Temperature, VDDIO Supply, 100 Mbps, 100% Data

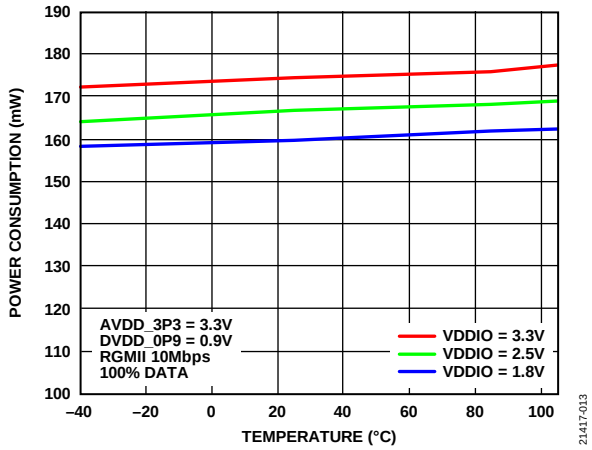


Figure 13. Power Consumption vs. Temperature, VDDIO Supply, 10 Mbps, 100% Data

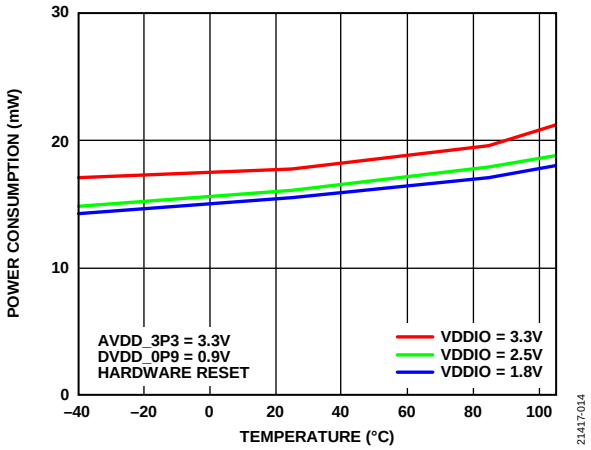


Figure 14. Power Consumption vs. Temperature, VDDIO Supply, Hardware Reset

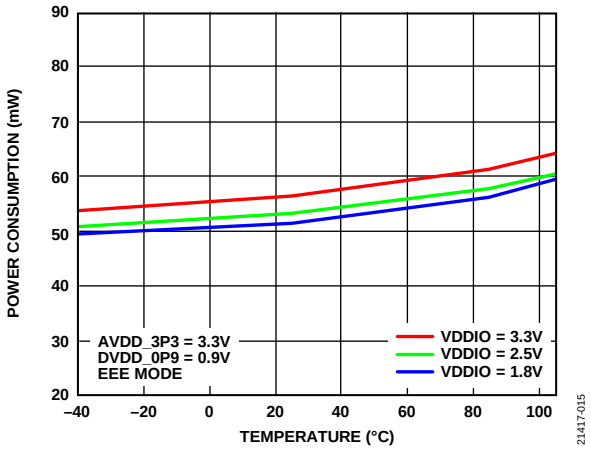


Figure 15. Power Consumption vs. Temperature, VDDIO Supply, EEE Mode

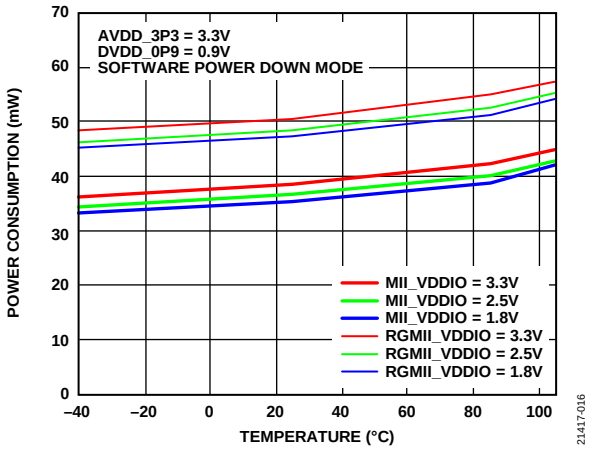


Figure 16. Power Consumption vs. Temperature, MAC Interface and VDDIO Supply

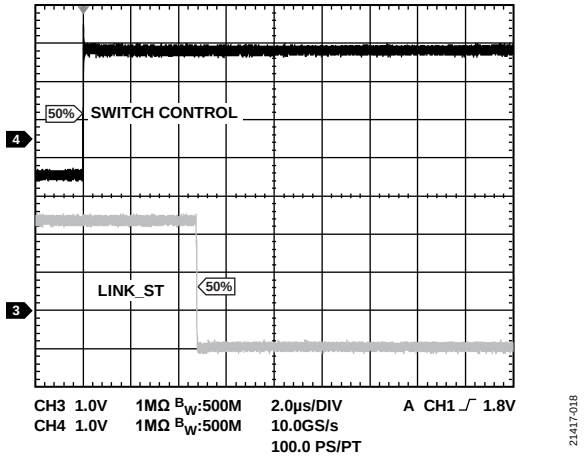


Figure 17. Enhanced Link Detection, 1 Gbps, 100 m Cable with Single Wire Break

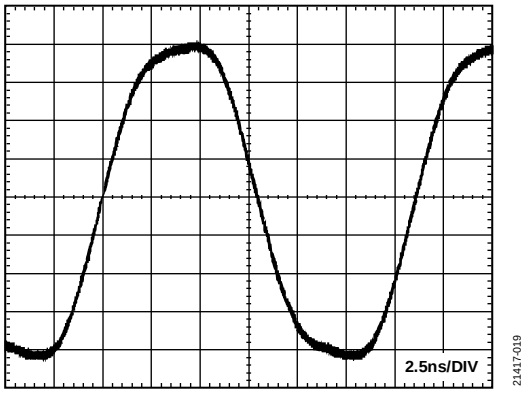


Figure 18. 1000BASE-T Test Mode 2 Output

THEORY OF OPERATION

OVERVIEW

The ADIN1300 is a low power, single port, Gigabit Ethernet transceiver with low latency specifications primarily designed for industrial Ethernet applications. This design integrates an EEE PHY core and all associated common analog circuitry, input and output clock buffering, management interface and subsystem registers, and MAC interface and control logic to manage the reset and clock control and hardware pin configuration.

The ADIN1300 interfaces directly to twisted pair media through an external transformer and is capable of supporting cable lengths up to 150 meters at Gigabit speeds and 180 meters when operating at 100 Mbps or 10 Mbps speeds.

When the 10 Mbps speed is selected, the device operates by default in 10BASE-Te mode using the 10BASE-Te transmit levels. The ADIN1300 can be configured via software (using the B10eEn bit, see Table 100) to operate 10BASE-T mode using the larger 10BASE-T transmit levels. The only difference between 10BASE-Te and 10BASE-T is the transmit level. A PHY configured as 10BASE-Te interoperates with a 10BASE-T PHY, assuming a normal Cat-5 cable is used.

The ADIN1300 provides a suite of diagnostic features enabling the user to analyze the quality of the link during operation or while the link is down.

Figure 19 shows a simplified overview of the main channel blocks. The following sections describe each block.

ANALOG FRONT END (AFE)

The AFE stage consists of a hybrid stage, a programmable gain amplifier (PGA), and an analog-to-digital convertor (ADC). The function of the hybrid stage is to remove the transmitted signal from the input signal, thereby allowing full-duplex operation on the twisted pair. The PGA stage scales the incoming signal before it reaches the ADC. The gain stage is controlled and adjusted based on the output of the ADC to ensure the signal applied to the ADC is maximized but within range of the ADC.

Physical Media Attachment (PMA)

The PMA block consists of the feed forward equalizer (FFE) stage, which removes intersymbol interference (ISI).

The twisted pairs of Ethernet cables are not internally shielded from each other, so signals transmitted on one pair couple across to the other pairs. When a transmitter does not match to the line due to mismatches or cable connectors, reflections are observed as an echo. The echo and crosstalk estimates are subtracted from the equalizer output.

Baseline wander is an artifact of the external transformer that attenuates at low frequencies. When there are many symbols with the same sign transmitted consecutively, the signal at the receiver reduces. The baseline wander block monitors and corrects to ensure the likelihood of receiving a symbol error is reduced.

Transmit Functions

1000BASE-T Mode

In 1000BASE-T, the PHY core encodes 8-bit data for transmission by the PMA as a 4D five-level pulse amplitude modulation (PAM) signal over the four pairs of cable.

100BASE-TX Mode

For the 100BASE-TX mode, the 4-bit data is first encoded into a 5-bit serial bit stream running at 125 Mbps. This is then sent to the scrambler where it is encoded to a three-level multilevel transmit (MLT3) format for transmission by the PMA.

10BASE-Te Mode

For the 10BASE-Te mode, the PHY transmits and receives Manchester-encoded data.

Receive Functions

1000BASE-T Mode

The PMA decodes the incoming 4D PAM signals into 8-bit data. After performing compensation and after additional cleanup, the PMA outputs the data to the receive pins of the MAC interface.

100BASE-TX Mode

The PMA decodes the incoming 3-level MLT3 sequence into 4-bit data after descrambling and 5-bit to 4-bit decoding.

10BASE-Te Mode

The core decodes the Manchester-encoded received signal.

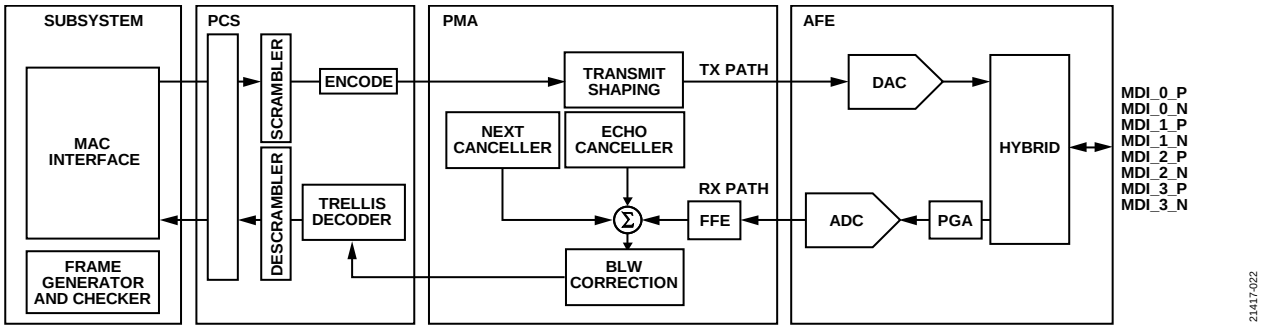


Figure 19. Simplified Channel Block Diagram

MAC INTERFACE

The ADIN1300 provides the option of RGMII, MII, or RMII MAC interface. The MAC interface is selected using hardware configuration pins (see Table 25) or via software.

RGMII Interface Mode

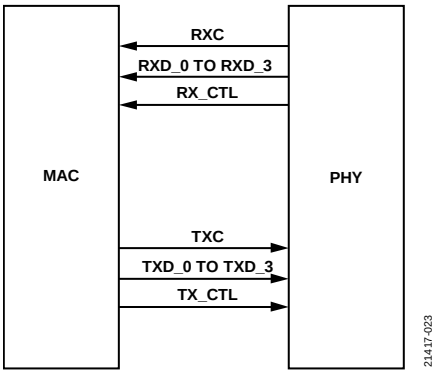


Figure 20. RGMII MAC-PHY Interface Signals

The RGMII interface is capable of supporting data rates of 1 Gbps, 100 Mbps, and 10 Mbps. For the receive interface, the ADIN1300 generates a 125 MHz, 25 MHz, or 2.5 MHz RXC signal to synchronize the RXD_x pin receive data in 1000BASE-T, 100BASE-TX, or 10BASE-Te modes, respectively. The RX_CTL is a combination of the RX_DV and RX_ER signals (as described in the MII Interface Mode section) using both edges of the RXC signal. The ADIN1300 transmits the RX_DV signal on the positive edge of RXC and a combination (XOR function) of RX_DV and RX_ER on the negative edge of RXC.

For the transmit interface, when operating in 1000BASE-T mode, the MAC drives TXC with a 125 MHz clock signal. The MAC transmits the TXD_x pin data, Bits[3:0] on the positive edge of TXC and TXD_x pin data, Bits[7:4] on the negative edge of TXC. In 100BASE-TX and 10BASE-Te modes, TXC is at 25 MHz and 2.5 MHz, respectively, and the MAC transmits the TXD_x pin data, Bits[3:0] on both edges of TXC. TX_CTL is a combination of the TX_EN and TX_ER signals using both edges of TXC. TX_EN is transmitted on the positive edge of TXC, and TX_EN XOR TX_ER is transmitted on the negative edge of TXC. Due to the fact that data is transmitted on both edges of the clock, an accurate delay requirement of 2 ns is required on both clock edges (see Figure 21) to ensure that the delayed clock is at the center of the data window, ensuring accurate data capture. It is possible to enable this 2 ns delay on RXC only or on both RXC and TXC using hardware pin configuration settings (see Table 25). These delays can also be configured in software. In Figure 21, the 8 ns period refers to 1000BASE-T operation, which is 40 ns or 400 ns in the case of 100BASE-TX and 10BASE-Te, respectively. The 2 ns delay is valid for 10BASE-Te, 100BASE-TX, and 1000BASE-T.

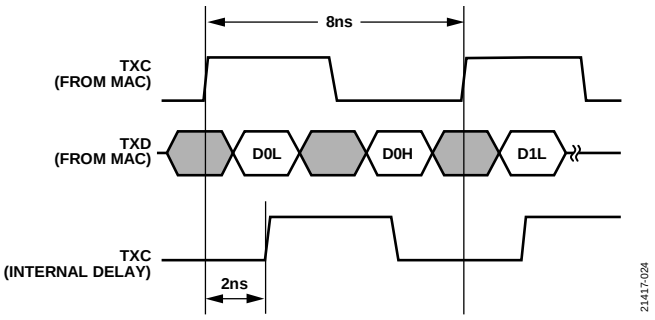


Figure 21. DLL Waveform

MII Interface Mode

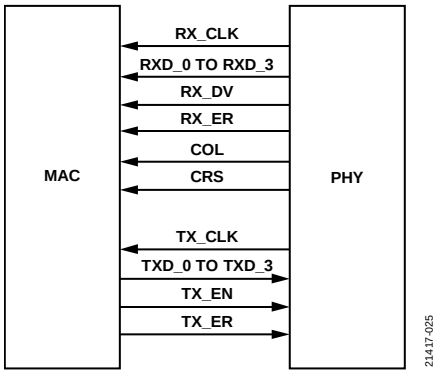


Figure 22. MII MAC to PHY Interface Signals

The MII interface is capable of supporting data rates of 100 Mbps and 10 Mbps. For the receive interface, the ADIN1300 generates a 25 MHz or 2.5 MHz RX_CLK signal to synchronize the RXD_x pin receive data in 100BASE-TX or 10BASE-Te modes, respectively. RX_DV indicates to the MAC that there is valid data present on the RXD_x receive pin. RX_ER is driven high by the ADIN1300 if an error is detected in the frame that was received from the MDI interface and is being transmitted to the MAC, or during a false carrier event (in 100BASE-TX mode). The CRS pin indicates the presence of a carrier to the MAC, while the COL pin is asserted in a collision condition.

For the transmit interface, the PHY generates a 25 MHz or 2.5 MHz reference clock on TX_CLK. The MAC transmits data on the TXD_x transmit pin that is synchronized with TX_CLK. The MAC asserts the TX_EN pin to indicate to the ADIN1300 that transmission data is available on the TXD_x transmit data lines. Because the TX_ER pin is not used in 10BASE-Te mode, and it is only used in 100BASE-TX mode for forward error propagation and for EEE low power idle (LPI) request, TX_ER is only supported when EEE is enabled via the hardware configuration pins (see Table 14).

RMII Interface Mode

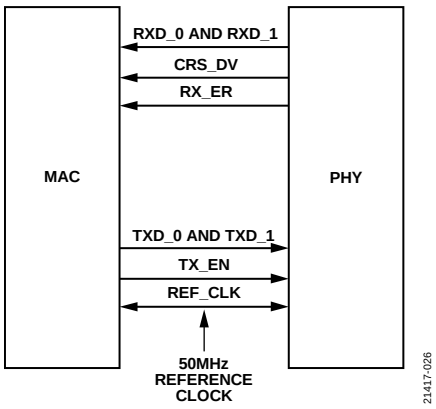


Figure 23. RMII MAC-PHY Interface Signals

This interface is capable of supporting 10 Mbps and 100 Mbps data rates. A single 50 MHz reference clock (REF_CLK) is sourced from the MAC to PHY (or from an external source) to the XTAL_I/CLK_IN/REF_CLK pin for both the transmit and receive interfaces.

The receive data (RXD_0 pin and RXD_1 pin), transitions synchronously to the reference clock (REF_CLK). The carrier sense/received data valid signal (CRS_DV) is a combination of the CRS and RX_DV signals and is asserted while the receive medium is nonidle. The CRS_DV is asserted asynchronously to REF_CLK and deasserted synchronously. RX_ER is also synchronous to REF_CLK, and is asserted when an error is detected in the received frame or when a false carrier is detected in 100BASE-TX. RX_ER assertion on a false carrier can be disabled by software.

The MAC transmits the TXD_0 pin and TXD_1 pin synchronously to REF_CLK, and asserts TX_EN to indicate to the ADIN1300 that transmission data is available on the TXD_0 pin and TXD_1 pin lines.

AUTONEGOTIATION

The ADIN1300 includes autonegotiation capability in accordance with IEE 802.3 Clause 28, providing a mechanism for exchanging information between PHYs to allow link partners to agree to a common mode of operation at the highest supported speed. During the autonegotiation process, the PHYs advertise their own capabilities and compares to those received from the link partner. The concluded operating mode is the highest speed capability and duplex setting common across the two devices.

In the event of the link being dropped, the autonegotiation process restarts automatically.

Autonegotiation can be restarted by request through a write to the RESTART_ANEG bit field in the MII register.

The autonegotiation process takes some time to complete, depending on the number of pages exchanged. Clause 28 of the IEEE 802.3 standard details the timers related to autonegotiation.

Master/Slave Resolution

For 1000BASE-T links, autonegotiation is also used to resolve master or slave status. The PHY can be configured to prefer master or slave through the hardware configuration or manually configured for fixed master or slave through the MSTR_SLV_CONTROL register, Bit 11 and Bit 12 (MAN_MSTR_ADV bit and MAN_MSTR_SLV_EN_ADV bit, respectively). If the user choses to manually fix this configuration, they must configure each side of the link differently.

Polarity Inversion Correction

The ADIN1300 is capable of detecting if the proper polarity is present on the cable and adjust the polarity if not. If polarity inversion has been detected, it is identified in the PHY_STATUS_1 register (see Table 53).

Automatic MDI Crossover

The ADIN1300 is capable of distinguishing if a straight or crossover cable is connected between the link partners. The ADIN1300 automatically detects and sets the MDI configuration to match its receiver to that of the remote transmitter, thereby avoiding need for crossover cables or cross-wired cables. Details on the automatic MDI/MDIX process is included in Clause 40, Section 40.8.2. This feature is configured through the hardware strapping configuration (see Table 24) or, alternatively, can be changed through software access via the MDIO interface.

AUTONEGOTIATION DISABLED

Autonegotiation is always used for a 1000BASE-T link, as required by the IEEE standards. 10BASE-Te or 100BASE-TX can use or disable autonegotiation. When autonegotiation is disabled, the PHY is configured for a single speed and the user must ensure that both sides of the link are configured properly. See Table 23 for more details on configuring the device with autonegotiation enabled or disabled.

If the ADIN1300 has autonegotiation enabled and the other side of the link has autonegotiation disabled, the ADIN1300 detects this and parallel detects, as per the IEEE standard, and attempts to bring up a link at the speed the remote PHY is configured to.

MANAGEMENT INTERFACE

The MII management interface provides a two-wire serial interface between a host processor or MAC and the ADIN1300, allowing access to control and status information in the subsystem and PHY core management registers.

The MII management interface consists of the following:

- MDC, clock line
- MDIO, bidirectional data line
- PHYAD_0 pin to PHYAD_3 pin, which configures device addresses for each PHY
- INT_N, management interrupt

The interface is compatible with both IEEE Standard 802.3 Clause 22 and Clause 45 management frame structures, as shown in Table 15 and Table 16, respectively, and defined as the following:

- Preamble: establishes synchronization at beginning of frame.
- Start of frame:
  - 01 indicates start of Clause 22 frame.
  - 00 indicates start of Clause 45 frame.
- OP: the operation code indicates type of frame transaction.
- PHYAD/PRTAD: PHY address. MSB first, only the PHY with matching PHY address hardware configuration responds.
- REG ADDR/DEVAD: register address, MSB first.
- TA: used to avoid contention during a read transition, 2-bit time spacing between register address field and data field.
- DATA: 16-bit field, MSB first.
- ADDRESS/DATA: 16-bit field, MSB first.
- IDLE: high-Z state, the MDIO line is pulled high by the pull-up resistor.

The PHY core registers at Address 0x00 to Address 0x01F can be accessed using the interface specified under Clause 22. The PHY core extended management interface (EMI) registers and subsystem registers can be accessed at Address 0x1E using the interface specified under Clause 45. However, for systems that do not support this interface, the registers at Address 0x1E can be accessed via Register 0x0010 and Register 0x0011 using Clause 22 access.

Interrupt (INT_N)

The ADIN1300 is capable of generating an interrupt to a host processor or MAC using the INT_N pin in response to a variety of user-selectable conditions (IRQ_MASK register, Address 0x0018). The following conditions can be selected to generate an interrupt:

- Speed change
- Link status change
- Receive status change
- MAC interface FIFO overflow/underflow
- Idle error counter saturated
- Autonegotiation page received
- Autonegotiation status change
- MDIO synchronization lost
- Cable diagnostic change

When an interrupt occurs, the system can poll the status of the interrupt status register (IRQ_STATUS register, Address 0x0019) on each device to determine the origin of the interrupt.

Table 15. Clause 22 Management Interface Frame Format

Operation	Preamble	Start of Frame	OP	PHYAD[4:0]	REG ADDR[4:0]	TA	DATA[15:0]	IDLE
Read	32 1s	01	10	AAAAA	RRRRR	Z0	d….d	Z
Write	32 1s	01	01	AAAAA	RRRRR	10	d….d	Z

Table 16. Clause 45 Management Interface Frame Format

Operation	Preamble	Start of Frame	OP	PRTAD[4:0]	DEVAD[4:0]	TA	ADDRESS/DATA[15:0]	IDLE
Address	32 1s	00	00	PPPPP	EEEEE	10	A…...A	Z
Write	32 1s	00	01	PPPPP	EEEEE	10	d….d	Z
Read	32 1s	00	11	PPPPP	EEEEE	Z0	d….d	Z
Post read Increment Address	32 1s	00	10	PPPPP	EEEEE	Z0	d….d	Z

MDI INTERFACE

The MDI connects the ADIN1300 to the Ethernet network via a transformer, as shown in Figure 24. In 1000BASE-T mode, transmit and receive occur simultaneously on each of the MDI_x_x pairs. In 10BASE-Te and 100BASE-TX modes, MDI_0_x are used to transmit when operating in MDI configuration and to receive when operating in MDIX configuration. The opposite is true of MDI_1_x in 10BASE-Te mode and 100BASE-TX mode. For example, MDI_1_x are used to receive when operating in MDI configuration and to transmit when operating in MDIX configuration. If auto MDIX is enabled, the ADIN1300 automatically determines if the MDI or MDIX configuration must be used. Otherwise, it is forced to the chosen MDI or MDIX configuration. In 10BASE-Te mode and 100BASE-TX mode, MDI_2_x and MDI_3_x are unused.

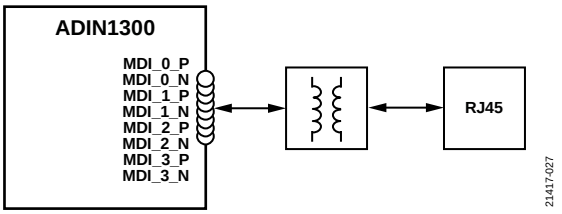


Figure 24. Media Dependent Interface

RESET OPERATION

The ADIN1300 supports a number of resets that include power-on reset, hardware reset, and multiple software reset types. All of these put the ADIN1300, including the PHY core, in a known state. Whenever the PHY core is reset, the MAC interface output pins (output pins with respect to the ADIN1300) are driven to a known idle state. All outputs except RXC/RX_CLK are driven low and RXC/RX_CLK is driven high.

Power-On Reset

The ADIN1300 includes power monitoring circuitry to monitor all of the supplies. At power-up, the ADIN1300 is held in hardware reset until each of the supplies has crossed its minimum rising threshold value.

Brown-out protection is provided by monitoring the supplies to detect if one or more of the supplies drops below a minimum falling threshold value and holding the device in hardware reset until the power is valid again.

Table 17. Brown-Out Protection Threshold Values

Supply	Minimum Falling Threshold Value (V)
AVDD_3P3	2.35
VDDIO	1.35
DVDD_0P9	0.7

Hardware Reset

A hardware reset is initiated by the POR circuitry or by asserting the RESET_N pin low. Bring the pin low for a minimum of 10 µs. Deglitch circuitry is included on this pin to reject pulses shorter than ~1 µs.

When the RESET_N pin is deasserted, the crystal oscillator circuit is enabled and the clock is given time to stabilize. The state of the hardware configuration pins is read and latched, the digital and analog circuits are initialized, and the PHY core clock multiplier unit (CMU) is reset. After 5 ms from the deassertion of RESET_N, the management interface registers are accessible and the device can be programmed. This time is significantly shorter if a single-ended clock rather than a crystal is used and the management interface registers are accessible 3 ms after the deassertion of RESET_N. If the ADIN1300 is configured to enter software power-down after a reset (see Table 23), the ADIN1300 enters software power-down mode and an interrupt is generated to indicate that a hardware reset occurred.

The following events occur after a hardware reset:

- The crystal oscillator circuit is enabled and time is allowed for the clock to stabilize.
- The hardware configuration pins are read and the values latched. These set the default values of the pin-dependent registers in the subsystem and PHY core registers.
- The MAC interface block is reset.
- The PHY core is reset.
- The PHY core CMU is reset.
- An interrupt to indicate that a hardware reset occurred is generated depending on the pin configuration (if the ADIN1300 was configured to enter software power-down mode after reset).

Software Reset

The ADIN1300 supports the following different software resets that reset specific circuit blocks under software control:

- Subsystem software reset with pin configuration
- Subsystem software reset
- PHY core software reset

Subsystem Software Reset with Pin Configuration

The ADIN1300 supports a software reset capability that behaves in a similar way to a hardware reset (see Table 18) (see the Subsystem Register Summary section). A subsystem reset with a pin configuration can be initiated by setting the GE_SFT_RST_CFG_EN bit (Address 0xFF0D) to 1 before setting GE_SFT_RST bit (Address 0xFF0C) to 1. This subsystem software reset follows the same reset sequence as the POR and hardware reset, except the crystal oscillator is not disabled and the clock stabilization step is skipped. The state of the hardware configuration pins is read and latched. These configuration pins set the default values of the pin dependent registers in the subsystem and PHY core registers. The MAC interface block and PHY core are reset. If a 125 MHz clock is selected as the PHY output clock, the GP_CLK pin, the PHY core CMU is not reset. Otherwise, the CMU is reset. The main difference between this type of reset and a hardware reset is that the crystal oscillator is not disabled.

Note that the GE_SFT_RST_CFG_EN bit is reset to its default value of 0 by this type of reset.

The following events occur after a subsystem software reset with pin configuration:

- The crystal oscillator circuit is not disabled during this type of reset.
- The hardware configuration pins are read and the values latched. These set the default values of the pin dependent registers in the subsystem and PHY core registers.
- The MAC interface block is reset.
- The PHY core is reset.
- The PHY core CMU is reset.
- The output reference clock is not available on the CLK25_REF pin during this reset.
- If a 125 MHz clock is selected as the PHY output clock it is not available on the GP_CLK pin during this reset.

Subsystem Software Reset

The subsystem can be reset by setting the GE_SFT_RST bit, Address 0xFF0C to 1. This bit is self clearing. Setting this bit resets the subsystem and PHY core registers, the MAC interface block, and the PHY core. The hardware configuration pins are not reread, and previously latched values of the hardware configuration pins are used to set the default values of the pin dependent registers in the subsystem and PHY core registers.

The following events occur after a subsystem software reset:

- The crystal oscillator circuit is not disabled during this type of reset.
- The hardware configuration pins are not reread. The pin dependent registers in the subsystem registers and PHY core registers are reset to the default values defined by the previously latched values of the hardware configuration pins.
- The MAC interface block is reset.
- The PHY core is reset.
- If a 125 MHz clock is selected as the PHY output clock, the GP_CLK pin, the PHY core CMU is not reset. Otherwise, the CMU is reset.
- The output reference clock (if enabled) is available on the CLK25_REF pin during this reset.
- The selected PHY output clock (if enabled) is available on the GP_CLK pin during this reset.

PHY Core Software Reset

The PHY core registers can be reset by setting the SFT_RST bit in the MII_CONTROL register, Address 0x0000 to 1. This bit is self clearing. Setting this bit resets the PHY core registers, the MAC interface block, and the PHY core. The hardware configuration pins are not reread, and previously latched values of the hardware configuration pins are used to set the default values of the pin dependent registers in the PHY core registers. The subsystem registers are not reset to default values. This is a useful way to reset the PHY core registers to a known configuration defined by software without resetting the rest of the ADIN1300 circuitry.

The following events occur after a PHY core software reset:

- The crystal oscillator circuit is not disabled during this type of reset.
- The hardware configuration pins are not reread. The pin dependent registers in PHY core registers are reset to the default values defined by the previously latched values of the hardware configuration pins. The subsystem registers are not reset to their default values.
- The MAC interface block is not reset.
- The PHY core is reset.
- If a 125 MHz clock is selected as the PHY output clock, the GP_CLK pin, the PHY core CMU is not reset. Otherwise, the CMU is reset.
- The reference clock (if enabled) is available on the CLK25_REF pin during this reset.
- The selected PHY output clock (if enabled) is available on the GP_CLK pin during this reset.

Table 18. ADIN1300 Reset Options Summary

	Reset Type	Hardware Pin Configuration Values Latched Following Reset	Subsystem Registers Reset	PHY Core Registers Reset	MAC Interface Block Reset	XTAL Oscillator Disabled During Reset	CLK25_REF (if Enabled) Available During Reset	GP_CLK Output (if Enabled) Available During Reset
1	Hardware Reset	Yes	Yes	Yes	Yes	Yes	No	No
2	Subsystem Software Reset with Pin Configuration	Yes	Yes	Yes	Yes	No	No	No
3	Subsystem Software Reset	No	Yes	Yes	Yes	No	Yes	Yes
5	PHY Core Software Reset	No	No	Yes	No	No	Yes	Yes

POWER-DOWN MODES

The ADIN1300 supports a number of power-down modes: hardware, software, and energy detect power-down, and EEE LPI mode. The lowest power mode is hardware power-down mode where the device is turned fully off and is not accessible.

Hardware Power-Down Mode

Hardware power-down mode is useful when operation of the ADIN1300 is not required and power must be minimized. The ADIN1300 enters hardware power-down mode when the RESET_N pin is asserted and held low. In this mode, all analog and digital circuits are disabled, the CMU is disabled, the clocks are gated off, and the only power is the leakage power of the circuits. The management interface registers are not accessible in this mode.

The following events occur in hardware power-down mode:

- All analog and digital circuits are disabled.
- The MAC interface output pins (output pins with respect to the ADIN1300) are tristated. Internally, these pins have a weak pull-down resistor, so these outputs are pulled low. This assumes no external pull-up resistors connected to these pins.
- All internal clocks are gated off.
- The PHY output clock (available on the GP_CLK pin) is disabled.
- The output reference clock (available on the CLK25_REF pin) is disabled.
- The management interface registers are not accessible.

Software Power-Down Mode

In software power-down mode, the ADIN1300 is powered down, the management interface can be accessed, and the ADIN1300 can be configured. The ADIN1300 does not attempt to bring up links until enabled.

Software power-down mode is useful when the device is being configured by software before links are brought up. The ADIN1300 can be configured to enter software power-down mode after reset using the appropriate pull-up/pull-down resistors on the LINK_ST pin and LED_0 pin, which sets the default value of the SFT_PD bit, Address 0x0000, to 1. The ADIN1300 also enters software power-down mode when the SFT_PD bit is set to 1. In software power-down mode, the analog and digital circuits are in a low power state. Typically, the CMU is disabled, most clocks are gated off, and the clock for the remaining digital circuitry runs at 25 MHz. Any signal or energy on the MDI pins (MDI_x_x) is ignored and no links are brought up. The management interface registers are accessible and the device can be configured using software. If the ADIN1300 is configured to output a 125 MHz clock on the GP_CLK pin, the CMU is enabled and the power in this mode is higher.

The following events occur in software power-down mode:

- All analog transmit and receive circuits are disabled.
- The MAC interface output pins (output pins with respect to the ADIN1300) are driven to a known idle state. All outputs except RXC/RX_CLK are driven low and RXC/RX_CLK is driven high.
- Most internal clocks are gated off.
- The output reference clock (if enabled) is available on the CLK25_REF pin.
- The selected PHY output clock (if enabled) is available on the GP_CLK pin.
- The management interface registers are accessible.

The ADIN1300 exits software power-down mode when the SFT_PD bit is cleared. At this point, the PHY attempts to bring up links according to its configuration. For example, if autonegotiation is enabled and all speeds are enabled, it advertises all speeds and starts to send autonegotiation link pulses.

Energy Detect Power-Down Mode

In energy detect power-down mode, the ADIN1300 is powered down but still monitors the line for signal energy. Typically, the ADIN1300 enters this mode when there is no cable plugged in and remains in this mode until a remote link partner is available.

Energy detect power-down mode can be enabled using the appropriate pull-up/pull-down resistors on the LINK_ST pin and LED_0 pin (see Table 23) or by setting the NRG_PD_EN bit (PHY_CTRL_STATUS_2 register, Address 0x0015) to 1. When the PHY is in normal operation (not software power-down) and energy detect power-down mode is enabled, the PHY enters energy detect power-down mode after a number of seconds of silence on the line. This is a very low power mode in which the analog and digital circuits are in a low power state. Typically, the CMU is disabled and most clocks are gated off. If the ADIN1300 is configured to output a 125 MHz clock on the GP_CLK pin, the CMU is enabled and the power in this mode is higher. The PHY monitors the line for signal energy and sends a link pulse once every second. If signal energy is detected, the PHY exits energy detect power-down mode and starts sending link pulses.

The following events occur when in energy detect power-down mode:

- All analog and digital circuits are disabled.
- Most internal clocks are gated off.
- The output reference clock (if enabled) is available on the CLK25_REF pin.
- The selected PHY output clock (if enabled) is available on the GP_CLK pin.
- The management interface registers are accessible.
- The PHY monitors the line for signal energy.

Typically, the PHY enters energy detect power-down mode when the cable is unplugged and exits this mode when a cable is plugged in and a remote link partner appears. In this mode, the PHY periodically wakes up and transmits a link pulse on the MDI_0 and MDI_1 pins to ensure that a lock out is avoided where both local and remote PHY are in an energy detect power-down mode.

EEE, Low Power Idle Mode

The ADIN1300 supports EEE and is compliant with the IEEE 802.3 standard. EEE can be used to reduce power consumption when no data is being transmitted by either the local or remote end. Both devices must have EEE enabled and advertised. If EEE is advertised by the local and remote PHYs, an EEE link is brought up. If there is no data to be sent, the MAC requests the ADIN1300 to enter EEE low power idle mode. When the MAC or remote PHY wishes to send data, the ADIN1300 PHY wakes up (within 16 µs for 1000BASE-T and 20 µs for 100BASE-TX) and can send or receive data.

The transitions between lower power consumption and normal operation is handled such that all frames remain intact and transmitted as normal, and the upper layer protocols are unaware of any changes at the PHY level. When data is transmitted, it continues to transmit at the fastest link speed established. See the Typical Power Consumption section for more details on the power savings in this mode.

EEE mode can be enabled using the appropriate pull-up/pull-down resistors on the LINK_ST pin and LED_0 pin (see Table 23) or by setting the EEE_1000_ADV or EEE_100_ADV bits (EEE_ADV register, Address 0x8001) to 1. During link autonegotiation, the local and remote PHYs advertise the speeds supported, including if they are EEE capable and, the PHYs then attempt to bring up a link at the highest speed supported by both sides. If EEE is advertised by both the local and remote PHYs for the established link speed, the link is an EEE link. If there is an EEE link and if at some point in time there is no data to be sent, the MAC requests the ADIN1300 to enter EEE LPI mode, which is almost as low power as energy detect power-down mode. The ADIN1300 wakes up periodically to transmit refresh signals that are used by the link partner to update adaptive filters and timing circuits to maintain link integrity.

The following events occur when in EEE LPI mode:

- All analog and digital circuits are in a low power mode.
- Most internal clocks are gated off.
- The output reference clock (if enabled) is available on the CLK25_REF pin.
- The selected PHY output clock (if enabled) is available on the GP_CLK pin.
- The management interface registers are accessible.
- The PHY monitors the line for an LPI wake signal.

When the local or remote PHY wishes to send data, the PHY initiates an LPI wake sequence and the PHYs can then start to send or receive data within 16 µs for 1000BASE-T (20 µs for 100BASE-TX).

STATUS LED

The ADIN1300 provides a configurable status LED. The LED can be used to indicate the speed of operation, link status, and duplex mode. The LED pin can be configured to be active high or active low. The recommendation is to use the LED as active low. The ADIN1300 automatically senses the connection of the LED during power up and reset. For example, if it senses that the pin is pulled to a supply, it configures the LED for active low operation. By default, LED_0 illuminates when a link is established and blinks when there is activity. The default LED operation can be overwritten in software using the PHY LED control registers, LED_CTRL_1, LED_CTRL_2, and LED_CTRL_3 (Register Address 0x001B, Register Address 0x001C, and Register Address 0x001D, respectively). See Table 54, Table 55, and Table 56.

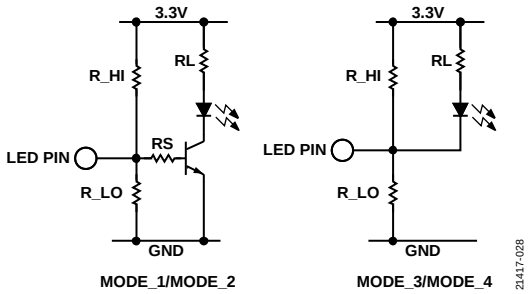


Figure 25. LED_0 Hardware Configuration Pin Interaction

The LED_0 pin is also shared with pin configuration functions as defined in Table 23, and it can be necessary for the voltage level on the pin to be at a certain value on power-on and reset to configure the ADIN1300 as required (set by a pull-up resistor from the pin to the supply (R_HI) and a pull-down resistor from the pin to GND (R_LO) in Figure 25).

The default operation of the LED is active low. So, if the default configuration setting is MODE_4, an external LED circuit using an active low LED results in a Logic 1 being read at the pin, and so the LED behaves as expected. For example, the LED does not turn on at power-on and reset.

An active low LED circuit is functional for a configuration setting of MODE_3 where the sense voltage is such that an active low LED is still off during power-on and reset, because there is insufficient forward voltage.

For configuration settings of MODE_1 or MODE_2, an external transistor must drive the LED as an active high LED, as shown in Figure 25. It is also be possible to drive an active high LED directly from the pin. However, this necessitates the use of an LED with a low forward voltage and, depending on the LED chosen, the LED may be quite dim.

PHY OUTPUT CLOCKS

The following internal PHY clock signals can be made available at the GP_CLK pin:

- 125 MHz free running clock
- 125 MHz recovered clock
- 25 MHz clock
- 25 MHz or 125 MHz free running clock
- 25 MHz or 125 MHz recovered clock

This is configured in through register writes via the GE_CLK_CFG register, Address 0xFF1F. By default, the PHY clock is off. Note that selecting the 125 MHz free running clock has an impact on power consumption, as the CMU is always powered up except during reset and power up.

POWER SUPPLY DOMAINS

The ADIN1300 has the following three power supply domains and requires a minimum of two supply sources, 0.9 V and 3.3 V:

- DVDD_0P9 is the 0.9 V digital core power supply input.
- AVDD_3P3 is the 3.3 V analog power supply input for the PHY MDI interface, analog circuitry, XTAL oscillator, DLL, RESET_N, CLK25_REF generation, and LED circuitry.
- VDDIO enables the MDIO and MAC interface voltage supply to be configured independently of the other circuitry on the ADIN1300. In most cases, RMII/MII is operated at 3.3 V and RGMII is operated at 2.5 V, but the MAC interface can operate at 3.3 V, 2.5 V, or 1.8 V to allow the MAC interface to run at a lower voltage and power if the MAC supports this.

There are no power supply sequencing requirements around the order of power being applied to the device. See the Power-Up Timing section for more details.

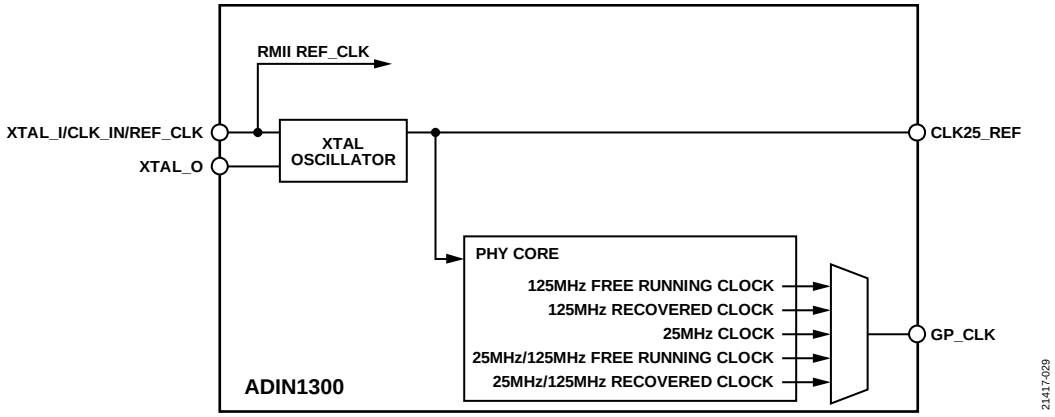


Figure 26. PHY Output Clocks Simplified Diagram

HARDWARE CONFIGURATION PINS

The ADIN1300 can operate in unmanaged or managed applications. In unmanaged applications, the desired operation of the PHY is configured from hardware configuration pins without any software intervention. For unmanaged applications, do not configure the PHY to enter software power-down after reset to ensure that the PHY immediately attempts to bring up links as configured by the PHY_CFG1 and PHY_CFG0 hardware configuration pins after power is applied to the device.

In managed applications, software is available to configure the PHY via the management interface (MDIO/MDC). In this case, it is possible to configure the PHY to enter software power-down mode after reset, such that the PHY can be configured before linking is attempted.

Hardware configuration pins are pins shared with functional pins and the voltage level on the pin is sensed and latched upon exiting from a reset. Some hardware configuration pins are multilevel sense, while others are two-level sense. Using two resistors, R_LO and R_HI (see Figure 27), four different voltage levels can be sensed, as shown in Table 19. Only MODE_1 (L) and MODE_4 (H) are relevant to the two-level sense pins and these are implemented with a 10 kΩ pull-down resistor or a 10 kΩ pull-up resistor, respectively. Note that LED_0 must be pulled up to the AVDD_3P3 rail rather than VDDIO.

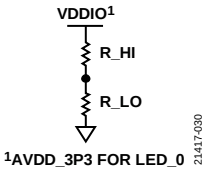


Figure 27. Hardware Configuration Pin Implementation

Note that the values listed in Table 19 assume no extra loading from circuitry external to the ADIN1300. It is likely that some configuration pins can be connected to a field-programmable gate array (FPGA) input that can have its own internal pull-up/pull-down resistor. This loads the resistor divider voltage. Assuming a pull-up resistor >43 kΩ and a pull-down resistor >37 kΩ, replace the 10 kΩ resistor used in MODE_1 and MODE_4 with a 2.5 kΩ resistor.

Table 19. Configuration Modes

Mode	R_LO	R_HI	Voltage Threshold
MODE_1	10 kΩ	Open	
MODE_2	10 kΩ	56 kΩ	>0.1 × VDDIO[1]
MODE_3	56 kΩ	10 kΩ	>0.5 × VDDIO[1]
MODE_4	Open	10 kΩ	>0.9 × VDDIO[1]

[1] Note that the supply rail for the LED_0 pin is AVDD_3P3 rather than VDDIO. Therefore, pull up any pull-up on the LED_0 pin to AVDD_3P3.

Table 19 shows recommended resistor values for the multistrap pins with the corresponding voltage threshold range required for each mode. Table 20 shows the voltage ranges involved for each mode vs. VDDIO voltage. The voltage levels shown were chosen to steer clear of standard VIH/VIL voltage levels to avoid any shoot-through currents (and unknown voltage levels) in the input driver of disabled devices connected to the pins. VIH/VIL voltage levels do have voltage and device dependencies. Therefore, it may not always be possible to avoid such artifacts.

Table 20. Voltage Levels for Modes vs. VDDIO Voltage

VDDIO[1] Mode	1.8 V (V)	2.5 V (V)	3.3 V (LED_0 = 3.3 V) (V)
MODE_1	<0.18	<0.25	<0.33
MODE_2	>0.18	>0.25	>0.33
MODE_3	>0.9	>1.25	>1.65
MODE_4	>1.62	>2.25	>2.97

[1] Note that the supply rail for the LED_0 pin is AVDD_3P3 rather than VDDIO. Therefore, pull up any pull-up on the LED_0 pin to AVDD_3P3.

The large resistor values recommended in Table 19 were chosen to minimize power consumption from the resistor ladder. Smaller value resistors can also be used, but the user must maintain the same resistor ratios for the values used.

HARDWARE CONFIGURATION PIN FUNCTIONS

The following functions are configurable from the ADIN1300 hardware pins (see Table 21 for pin details):

- PHY address
- Forced/advertised PHY speed
- Software power-down mode after reset
- Downspeed enable
- Energy detect power-down mode
- EEE enable
- Auto MDIX
- MAC interface selection (RGMII/RMII/MII)

Table 21. Hardware Configuration Pins

Configuration Function	Functional Pin/Hardware Configuration Mnemonic[1]	Pin Levels	Internal Pull-Down[2]	Default Configuration
PHYAD_0 to PHYAD_3 Configuration	RXD_3/PHYAD_3	2	Yes	PHY Address 0x0
	RXD_2/PHYAD_2	2	Yes	
	RXD_1/PHYAD_1	2	Yes	
	RXD_0/PHYAD_0	2	Yes	
Forced/Advertised PHY Speed, Software Power-Down Mode after Reset, Downspeed Enable, Energy Detect Power-Down Mode, Energy Efficient Ethernet	LINK_ST/PHY_CFG1	4	None	Unknown (external resistors are required)
	LED_0/COL/TX_ER/PHY_CFG0	4	None	
Auto MDIX	GP_CLK/RX_ER/MDIX_MODE	4	None	Unknown (external resistors are required)
MAC Interface Selection	RX_CTL/RX_DV/CRS_DV/MACIF_SEL1	2	Yes	RGMII RXC/TXC 2 ns delay
	RXC/RX_CLK/MACIF_SEL0	2	Yes	

[1] Hardware configuration pin is the last pin name in the pin mnemonic.
[2] The internal pull-down has a typical value of 45 kΩ.

PHY Address Configuration

PHY address configuration is shared with the RXD_3 pin to RXD_0 pin and can be configured according to Table 22. Four of the ADIN1300 pins are available for configuring the PHY address. These are two-level configuration pins, which means that it is possible to configure the ADIN1300 to any of the 16 available PHY addresses. In many applications, the default address of 0x0 is used and, in that case, it may not be necessary to configure these pins externally because the RXD_3 pin to RXD_0 pin have weak internal pull-down resistors. This assumes that no other system level circuitry attached to these nodes, such as the MAC or Ethernet switch, has internal pull-up resistors on these pins.

Table 22. PHY Address Configuration

PHY Address	PHYAD_3 Pin	PHYAD_2 Pin	PHYAD_1 Pin	PHYAD_0 Pin
0	Low	Low	Low	Low
1	Low	Low	Low	High
2	Low	Low	High	Low
3	Low	Low	High	High
4	Low	High	Low	Low
5	Low	High	Low	High
6	Low	High	High	Low
7	Low	High	High	High
8	High	Low	Low	Low
9	High	Low	Low	High
10	High	Low	High	Low
11	High	Low	High	High
12	High	High	Low	Low
13	High	High	Low	High
14	High	High	High	Low
15	High	High	High	High

PHY Configuration

The PHY_CFG1 and PHY_CFG0 hardware configuration pins are shared with the LINK_ST and LED_0 functional pins, respectively. These hardware configuration pins cover the following functions and can be configured according to Table 23:

- Forced/advertised PHY speed
- Software power-down mode after reset
- Downspeed enable
- Energy detect power-down (EDPD) mode
- EEE enable

The PHY_CFG1 pin and PHY_CFG0 pin have no internal pull-up resistors, so external resistors must be used to configure these functions.

Table 23. PHY Configuration

Forced/ Advertised	PHY Speed Configuration	Other Functions Enabled[1]	PHY_CFG1	PHY_CFG0	Row No.
Advertised Speeds (Autonegotiation Enabled)	10 half duplex (HD)/full duplex (FD), 100 HD/FD, and 1000 FD slave	Downspeed, EDPD, and EEE	MODE_4	MODE_4	1
	10 HD/FD, 100 HD/FD, and 1000 FD slave		MODE_1	MODE_4	2
	10 HD/FD, 100 HD/FD, and 1000 FD master		MODE_2	MODE_4	3
	10 HD/FD, 100 HD/FD, and 1000 FD slave	Software power-down mode after reset	MODE_3	MODE_4	4
	10 HD/FD and 100 HD/FD		MODE_4	MODE_2	5
	10 FD and 100 FD		MODE_4	MODE_3	6
	100 FD and 1000 FD slave		MODE_4	MODE_1	7
	100 FD and 1000 FD master		MODE_3	MODE_1	8
	100 FD		MODE_1	MODE_1	9
	1000 FD slave		MODE_2	MODE_1	10
	1000 FD master		MODE_3	MODE_2	11
Forced Speed (Autonegotiation Disabled)	10 FD		MODE_1	MODE_2	12
	100 HD		MODE_2	MODE_2	13
	100 FD		MODE_3	MODE_3	14

[1] If no function is listed in this column, then only the PHY speed is configured using this row.

Forced/Advertised PHY Speed

As outlined in Table 23, it is possible to advertise all or a subset of PHY speed capabilities, select preferred slave or master, set half duplex or full duplex mode, and enable or disable autonegotiation.

Autonegotiation is enabled for the first 11 rows in Table 23, such as in the case of advertised speeds modes. It is also possible to configure forced speed modes where autonegotiation is disabled and the speed is forced (Row 12 to Row 14 of Table 23).

Referring to Table 23, three of the PHY_CFG1 and PHY_CFG0 hardware configuration pin settings result in the same link speed configuration (Row 1, Row 2, and Row 4). However, Row 1 also enables three other functions, Row 2 does not enable any extra functions, and in Row 4, the ADIN1300 is configured to enter software power-down mode after reset. The enabling or disabling of autonegotiation and advertised speed settings can also be set using the standard IEEE registers, MII_CONTROL (Address 0x0000), AUTONEG_ADV (Address 0x0004), and MSTR_SLV_CONTROL (Address 0x0009).

Software Power-Down after Reset

If the ADIN1300 is configured so that it does not enter software power-down mode after reset, the ADIN1300 attempts to bring up links at the configured speeds and MDI/MDIX configuration after it exits reset. If the ADIN1300 is configured so that it enters software power-down mode after reset (Row 4), the ADIN1300 waits in software power-down until it is configured over the MDIO interface, at which point the PHY configuration can be set to exit software power-down by software. The ADIN1300 can also be put into software power-down mode by setting the SFT_PD bit (MII_CONTROL register, Address 0x0000).

Downspeed Configuration

If downspeed is enabled, the PHY down speeds to a lower speed after a number of attempts if it cannot link at the highest speed advertised. The use of downspeed requires autonegotiation to be enabled with multiple speeds advertised. The default operation of downspeed can be overwritten in software by writing to DN_SPEED_TO_100_EN (PHY_CTRL_2 register, Address 0x0016, Bit 11), DN_SPEED_TO_10_EN (PHY_CTRL_2 register, Address 0x0016, Bit 10), and NUM_SPEED_RETRY (PHY_CTRL_3 register, Address 0x0017, Bits[12:10]).

Energy Detect Power-Down Configuration

If energy detect power-down is enabled and no energy is detected at the MDI pins, the ADIN1300 enters a low power mode. Therefore, this mode saves power where there is no cable connected or the remote PHY is powered down.

Energy Efficient Ethernet

If EEE is enabled and also advertised by the remote PHY, the ADIN1300 can enter a low power mode (low power idle) when no data is being transmitted by either end. See the EEE, Low Power Idle Mode section for more details.

Auto MDIX Configuration

Auto MDIX configuration mode is shared with the GP_CLK pin and can be configured according to Table 24. This pin does not have an internal pull-up resistor, so external resistors must be used to set the MDI/MDIX mode.

Table 24. Auto MDIX Configuration

Configuration	MDIX_MODE
Manual MDI	MODE_1
Manual MDIX	MODE_2
Auto MDIX, Prefer MDIX	MODE_3
Auto MDIX, Prefer MDI	MODE_4

If auto MDIX is enabled (MODE_3 or MODE_4), the ADIN1300 automatically determines if the MDI or MDIX configuration must be used. Otherwise, the ADIN1300 is forced to the chosen MDI or MDIX configuration.

If enabling auto MDIX, the ADIN1300 supports auto MDIX with a preference for MDI or MDIX. This determines which MDI/MDIX setting is first in the autocrossover algorithm. To achieve a faster MDI/MDIX resolution in some cases, set both PHYs to the same preferred configuration (MDI or MDIX) when a crossover cable is used, and to opposite preferred configurations if a straight-through cable is used, which has the advantage of still being able to work with a mismatch of wiring and optimize the time to resolve auto MDIX.

The default operation of auto MDIX can be overwritten in software by writing to the AUTO_MDI_EN bit (PHY_CTRL_1 register, Address 0x0012) and the MAN_MDIX bit (PHY_CTRL_1 register, Address 0x0012).

MAC Interface Selection

The MAC interface selection is shared with the RX_CTL/RX_DV/CRS_DV pin and RXC/RX_CLK pin, and can be configured according to Table 25. In RGMII mode, it is possible to enable a 2 ns internal delay on RXC only or on both RXC and TXC. The RX_CTL/RX_DV/CRS_DV pin and RXC/RX_CLK pin have weak internal pull-down resistors. Therefore, by default, the ADIN1300 is configured in RGMII mode with a 2 ns delay on RXC and TXC. External resistors must be used to select any of the remaining MAC interface modes.

The MAC interface selection can also be done via software (GE_RGMII_CFG and GE_RMII_CFG registers) with the internal 2 ns delay configured via the GE_RGMII_RXLD_EN bit and GE_RGMII_TXLD_EN bit within the GE_RGMII_CFG register (Address 0xFF23). Put the PHY in software power-down by setting the SFT_PD bit (MII_CONTROL register, Address 0x0000) before any changes are made to the MAC interface configuration registers. Because RMII mode requires a 50 MHz reference clock, do not use software to configure the MAC interface to RMII.

Table 25. MAC Interface Selection

MAC Interface Selection	MACIF_SEL1	MACIF_SEL0
RGMII RXC/TXC 2 ns Delay	Low	Low
RGMII RXC Only, 2 ns Delay	High	Low
MII	Low	High
RMII	High	High

ON-CHIP DIAGNOSTICS

LOOPBACK MODES

The PHY core provides several loopback modes: all digital loopback, MII loopback, external cable loopback, line driver loopback, and remote loopback (see Figure 28). These loopback modes test and verify various functional blocks within the PHY. The use of frame generators and frame checkers allow completely self contained in-circuit testing of the digital and analog data paths within the PHY core.

All Digital Loopback

The default loopback mode is all digital loopback mode. This loops the data within the PHY at the analog/digital boundary to check for proper operation of the PHY, but does not require the external analog components, connections, or analog supplies to be accurate. In all digital loopback mode, it is possible to also transmit to the MDI pins, which can be useful for transmit testing. By default, the LB_ALL_DIG_SEL bit (PHY_CTRL_STATUS_1 register, Address 0x0013) is set, which selects all digital loopback mode and the LB_TX_SUP bit (Bit 6 within the PHY_CTRL_STATUS_1 register) is also set, which suppresses the transmission of the signal to the MDI pins. Setting the PHY_CTRL_STATUS_1 register to a value of 0x1001 selects digital loopback with transmission to the MDI pins. The loopback bit (MII_CONTROL register, Address 0x0000, Bit 14) also needs to be set to enable all digital loopback mode.

External Cable Loopback

External cable loopback verifies the whole analog and digital path, including the external components and cable. This requires that Pair 0 and Pair 1, and Pair 2 and Pair 3 are shorted together to provide an analog loopback at the end of the cable. The signal processing is adjusted so that the transmitted signal is not cancelled. Setting the LB_EXT_EN bit (PHY_CTRL_STATUS_1 register, Address 0x0013) enables external cable loopback.

Line Driver Loopback

For line driver loopback, leave the MDI pins open-circuit, thereby transmitting into an unterminated connector/cable. The PHY can then operate by receiving the reflection from its own transmission. This provides similar capabilities to the external cable loopback without the need to create any wire shorts by unplugging the cable. Setting the LB_LD_SEL bit (PHY_CTRL_STATUS_1 register, Address 0x0013) selects line driver loopback. The loopback bit (MII_CONTROL register, Address 0x0000, Bit 14) also needs to be set to enable line driver loopback.

Remote Loopback

Remote loopback requires a link up with a remote PHY and to loop the data received from the remote PHY back to the remote PHY. This linking allows a remote PHY to verify a complete link by ensuring that the PHY receives the proper data. Setting the PHY_CTRL_STATUS_1 register to a value of 0x0241 selects remote loopback where the data received by the PHY is also sent to the MAC. Setting the LB_TX_SUP bit within the PHY_CTRL_STATUS register, which sets the register value to 0x0341, selects remote loopback, where the data received by the PHY is not sent to the MAC. For this type of loopback, do not set the loopback bit (MII_CONTROL register, Address 0x0000, Bit 14).

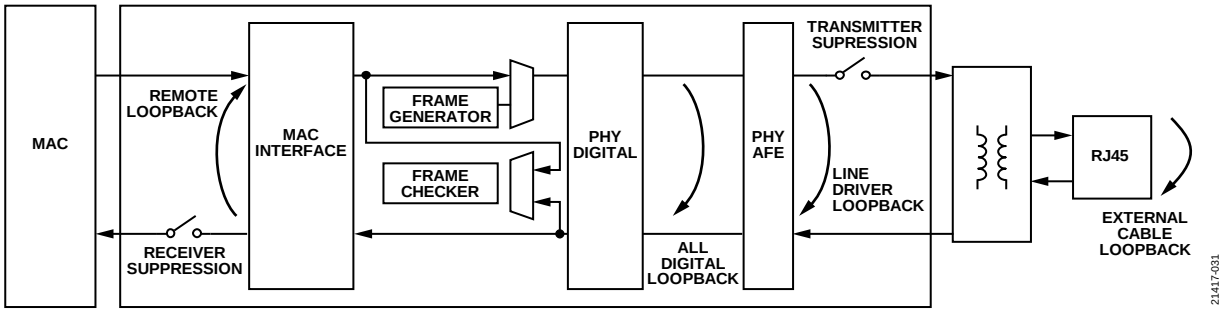


Figure 28. ADIN1300 Loopback Modes

FRAME GENERATOR AND CHECKER

The ADIN1300 can be configured to generate frames and to check received frames (see Figure 28). The frame generator and checker can be used independently to just generate frames or just check frames or can be used together to simultaneously generate frames and check frames. If frames are looped back at the remote end, the frame checker can be used to check frames generated by the ADIN1300.

When the frame generator is enabled, the source of data for the PHY comes from the frame generator and not the MAC interface. To use the frame generator, the diagnostic clock must also be enabled (DIAG_CLK_EN bit, PHY_CTRL_1 register, Address 0x0012).

The frame generator control registers configure the type of frames to be sent (random data, all 1s), the frame length, and the number of frames to be generated. The generation of the requested frames starts by enabling the frame generator (set the FG_EN bit, Address 0x9415). When the generation of the frames is completed, the frame generator done bit is set (FG_DONE bit, Address 0x941E).

The frame checker is enabled using the frame checker enable bit (FC_EN bit, Address 0x9403). The frame checker can be configured to check and analyze received frames from either the MAC interface or the PHY, which is configured using the frame checker transmit select bit (FC_TX_SEL bit, Address 0x9407). The frame checker reports the number of frames received, cyclic redundancy check (CRC) errors, and various other frame errors. The frame checker frame counter register and frame checker error counter register count these events.

The frame checker counts the number of CRC errors and these are reported in the receive error counter register (RX_ERR_CNT register, Address 0x0014). To ensure synchronization between the frame checker error counter and frame checker frame counters, all of the counters are latched when the receive error counter register is read. Therefore, when using the frame checker, read the receive error counter first, and then read all other frame counters and error counters. A latched copy of the receive frame counter register is available in the FC_FRM_CNT_H register and FC_FRM_CNT_L register (Address 0x940A and Address 0x940B, respectively).

In addition to CRC errors, the frame checker counts frame length errors, frame alignment errors, symbol errors, oversized frame errors, and undersized frame errors. In addition to the received frames, the frame checker counts frames with an odd number of nibbles in the frame in 100BASE-TX mode or 10BASE-Te mode, and counts frames with an odd number of nibbles in the preamble in 100BASE-TX mode. The frame checker also counts frames with a noninteger number of nibbles in 10BASE-Te mode and the number of false carrier events, which is a count of the number of times the bad start of stream delimiter (SSD) state is entered.

Frame Generator and Checker used with Remote Loopback with Two PHYs

Using two PHY devices, the user can configure a convenient self contained validation of the PHY to PHY connection. Figure 29 shows an overview of how each PHY is configured. An external Ethernet cable is connected between both devices, and PHY1 is generating frames using the frame generator. PHY2 has remote loopback enabled on the MAC side. The frames issued by PHY1 are sent through the cable, through the PHY2 signal chain returned by PHY2 remote loopback, back again through the Ethernet cable, and checked by the PHY1 frame checker.

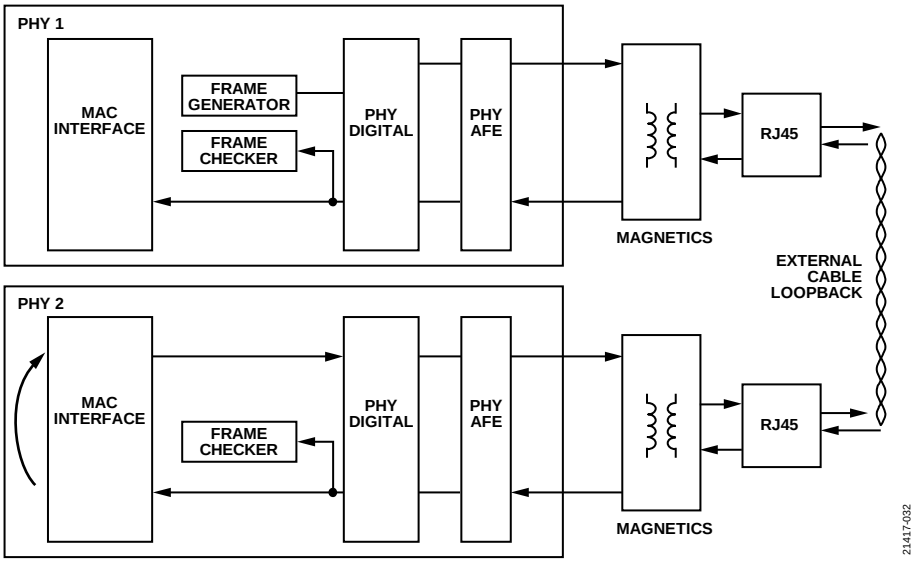


Figure 29. Remote Loopback used across Two PHYs for Self Check Purposes

CABLE DIAGNOSTICS

The ADIN1300 has on-chip cable diagnostics capabilities. This cable analysis can be used to detect cable impairments that may be preventing the establishment of a gigabit link or degrading performance and can be performed both when the link is up or when the link is down.

Each time a 100BASE-TX or 1000BASE-T link is brought up, the ADIN1300 reports an estimate of the cable length based on the signal processing. This can be read in the cable diagnostics cable length estimate register (CDIAG_CBL_LEN_EST register, Address 0xBA25). This estimate is not available for a 10BASE-Te link. A polarity inversion on each pair is reported in the pair polarity inversion register bits (PHY_2_STATUS register, Address 0x001F, Bits[13:10]) and the B_10_POL_INV bit (PHY_STATUS_1 register, Address 0x001A). Pair swaps are reported in the pair swap register bits (PAIR_23_SWAP bit, Address 0x001F and PAIR_01_SWAP bit, Address 0x001A). When the link is up, the signal quality on each pair is indicated in the mean square error register for each pair (MSE_A, MSE_B, MSE_C, and MSE_D registers, Address 0x8402 to Address 0x8405, Bits[7:0]).

When the link is down, the ADIN1300 can run cable fault detection using time domain reflectometry (TDR). By transmitting pulses and analyzing the reflections, the PHY can detect cable faults like opens, shorts, cross pair shorts, and the distance to the nearest fault. The PHY can also determine that the pair is well terminated and does not have any faults. Put the remote PHY in a power-down state or disconnect the PHY to run cable fault detection because remote PHY link pulses can interfere with the analysis of the reflected pulses and can return a pair busy result.

The cable fault detection is automatically run on all four pairs looking at all combinations of pair faults by first putting the PHY in standby (clear the LINK_EN bit, PHY_CTRL_3 register, Address 0x0017) and then enabling the diagnostic clock (set the DIAG_CLK_EN bit, PHY_CTRL_1 register, Address 0x0012). Cable diagnostics can then be run (set the CDIAG_RUN bit in the CDIAG_RUN register, Address 0xBA1B). The results are reported for each pair in the cable diagnostics results registers, CDIAG_DTLD_RSLTS_0, CDIAG_DTLD_RSLTS_1, CDIAG_DTLD_RSLTS_2, and CDIAG_DTLD_RSLTS_3, Address 0xBA1D to Address 0xBA20). The distance to the first fault for each pair is reported in the cable fault distance registers, CDIAG_FLT_DIST_0, CDIAG_FLT_DIST_1, CDIAG_FLT_DIST_2, and CDIAG_FLT_DIST_3, Address 0xBA21 to Address 0xBA24).

ENHANCED LINK DETECTION

The ADIN1300 supports enhanced link detection, which is early detection and indication of link loss. This is a feature where the received signal is monitored, and if a significant number of consecutive samples of the signal are not as expected, early indication of link down is indicated. The ADIN1300 can simultaneously monitor for a significant number of consecutive 0s, a significant number of consecutive 1s, or a significant number of consecutive invalid levels.

If enhanced link detection is enabled, the ADIN1300 typically reacts to a break in the cable within 10 µs and indicates link down via the LINK_ST pin. If enhanced link detection is not enabled, the ADIN1300 follows the IEEE standard, and in 100BASE-TX, it can take more than either 350 ms or 750 ms in 1000BASE-T, depending if the PHY is 1000BASE-T master or 1000BASE-T slave.

Enhanced link detection is enabled for 100BASE-TX via the enhanced link detection 100BASE-TX enable register bits (FLD_EN register, Address 0x8E27, Bit 5, Bit 3, and Bit 1) and for 1000BASE-T via the 1000BASE-T enhanced link detection enable register bits (FLD_EN register, Address 0x8E27, Bit 6, Bit 4, Bit 2, and Bit 0).

Do not enable 1000BASE-T retrain (clear the B_1000_RTRN_EN bit, Address 0xA001) if enhanced link detection is enabled for 1000BASE-T.

The latched status of the enhanced link detection function can be read via the enhanced link detection status bit, FAST_LINK_DOWN_LAT (Address 0x8E38).

START OF PACKET INDICATION

The ADIN1300 includes the detection and indication of the start of packets (SOP) on the transmit and receive side to support IEEE 1588 time stamp controls and give the MAC more accurate timing information.

The transmit and receive SOP indication can be made available at any of the following pins under software configuration: GP_CLK, LINK_ST, INT_N, and LED_0 using the following override control registers:

- GE_IO_GP_CLK_OR_CNTRL bits, Address 0xFF3C
- GE_IO_GP_OUT_OR_CNTRL bits, Address 0xFF3D
- GE_IO_INT_N_OR_CNTRL bits, Address 0xFF3E
- GE_IO_LED_A_OR_CNTRL bits, Address 0xFF40

The detection of the transmit SOP is done after internal PHY FIFO so there is a fixed delay between the SOP indication at the pin to the actual SOP at the MDI pins.

Start of packet indication is enabled via the SOP transmit and receive enables, (set the SOP_TX_EN bit, and the SOP_RX_EN bit, Address 0x9428).

The SOP is asserted by default on the first byte or nibble of the frame. The SOP can be configured to be asserted when the start frame delimitator (SFD) is detected in the frame. This is configured by setting the SOP SFD enable bit (SOP_SFD_EN, Address 0x9428).

The SOP indication, by default, is asserted for the duration of the frame. The SOP can be configured to be asserted for a programmable number of cycles. This is configured by setting the SOP N-cycle enable bit (SOP_NCYC_EN, Address 0x9428), and the number of cycles in this case is configured via the SOP

N by 8 minus 1 cycles register (SOP_N_8_CYC_M_1_D_EN register, Address 0x9428, Bits[6:4]).

The ADIN1300 start of packet detection and indication circuit includes the ability to delay each of the SOP transmit and receive indications by a programmable number of clock cycles. The purpose of this on the receive side is to support MAC interfaces with long latency so that the received frame SOP indication is not asserted before the MAC receives the frame.

The purpose of this on the transmit side is to align the transmit SOP indication assertion close to the reference point set on the MDI pins (so that the time stamping point does not have to be adjusted at the MAC/switch side). There are programmable registers for the delays for 1000BASE-T mode, 100BASE-TX mode, and 10BASE-T mode for transmit and receive. These are programmed via the SOP_RX_DEL register and SOP_TX_DEL register, Address 0x9429 and Address 0x942A, respectively.

TYPICAL POWER CONSUMPTION

Table 1 and the Typical Performance Characteristics section capture high level detail of the power consumption of the ADIN1300 under nominal conditions and across the device temperature range. Power consumption of a PHY depends heavily on power supply, speed established, operating condition, and capacitive loading on digital pins.

Power Supplies

The most significant contributor to power consumption is the supply voltage choice and speed of operation.

The ADIN1300 can operate from a minimum of two power supply rails, where AVDD_3P3 = VDDIO = 3.3 V and DVDD_0P9 = 0.9 V. The VDDIO voltage requirements are dictated by the MAC interface. While two power supply rails result in a more simplified power strategy, the higher digital supply voltage translates directly to higher power consumption needs. This can be seen in Table 26, Table 27, and Table 28, which describe the various VDDIO voltages. Using the lowest VDDIO supply rail can achieve a savings close to 100 mW at Gb speeds with full throughput.

Speed of Link Established

The next biggest contributor to power consumption is the speed of the link. The ADIN1300 PHY has leading edge power consumption figures for Gb data. Lower data links run at lower power consumption numbers. This PHY was designed for low power consumption when operating at Gb speeds. As a result, 10 Mbps power consumption may not be as low as comparable offerings in the industry.

Lower Power Modes

The ADIN1300 has a number of means to lower power consumption under conditions where the PHY is not active or when it is linked and there is no data transmitting. Full details on these modes are captured in the Power-Down Modes section. Two key modes of operation to minimize power are energy detect power-down mode, when no link is present, and EEE low power idle mode, where a link is established but the line is idle. The power consumption under this state is significantly reduced compared to other idle states. Configuration of these modes is available through the hardware configuration pins or directly through the MDI interface. Typical power consumption for hardware reset, EEE, and EDPD are captured in Table 26, Table 27, and Table 28 as EEE.

Data Utilization

Table 26, Table 27, and Table 28 also capture the variation for data utilization for the various speeds. Data is shown for 100% data to 0% or idle state. In the idle state, the PHY is linked, but no data transfer is taking place. The power consumption in this state is lower than full utilization.

Table 26. Typical Current and Power Consumption for VDDIO = 1.8 V[1]

Mode	DVDD_0P9 Core Supply, 0.9 V (mA)	VDDIO Digital I/O Supply, 1.8 V (mA)	AVDD_3P3 PHY AFE, LED Circuit, 3.3 V (mA)	Total Power (mW)
Gb, 100% Data	38	35	70.5	330
Gb, Idle	38	28	70.5	317
100 Mbps, 100% Data	12	9	35	140
100 Mbps, Idle	11	8	35	138
10 Mbps, 100% Data	7	8	42	158
10 Mbps, Idle	6	7	30	117
EEE	4	1	14	52
Cable Unplug	3	1	6	25
COMA	3	0	1	7

[1] T_A = 25°C, cable length = 100 meters.

Table 27. Typical Current and Power Consumption for VDDIO = 2.5 V[1]

Mode	DVDD_0P9 Core Supply, 0.9 V (mA)	VDDIO Digital I/O Supply, 2.5 V (mA)	AVDD_3P3 PHY AFE, LED Circuit, 3.3 V (mA)	Total Power (mW)
Gb, 100% Data	38	41	70.5	370
Gb, Idle	38	30	70.5	342
100 Mbps, 100% Data	12	10	35	148
100 Mbps, Idle	11	9	35	145
10 Mbps, 100% Data	7	8	42	165
10 Mbps, Idle	6	7	30	123
EEE	4	1	14	53
Cable Unplug	3	1	6	25
COMA	3	0	1	7

[1] T_A = 25°C, cable length = 100 meters.

Table 28. Typical Current and Power Consumption for VDDIO = 3.3 V[1]

Mode	DVDD_0P9 Core Supply, 0.9 V (mA)	VDDIO Digital I/O Supply, 3.3 V (mA)	AVDD_3P3 PHY AFE, LED Circuit, 3.3 V (mA)	Total Power (mW)
Gb, 100% Data	38	48	70.5	425
Gb, Idle	38	32	70.5	372
100 Mbps, 100% Data	12	11	35	159
100 Mbps, Idle	11	10	35	155
10 Mbps, 100% Data	7	9	42	173
10 Mbps, Idle	6	7	30	129
EEE	4	1	14	53
Cable Unplug	3	1	6	26
COMA	3	0	1	7

[1] T_A = 25°C, cable length = 100 meters.

APPLICATIONS INFORMATION

SYSTEM OVERVIEW

The ADIN1300 is a low power, single port Gigabit Ethernet transceiver with latency specifications primarily designed for industrial Ethernet applications. Figure 30 shows a basic system block diagram. Note that the MAC Interface section must be consulted for specific information on each MAC interface configuration mode.

The following section captures some of the key requirements for external component selection for use with the ADIN1300.

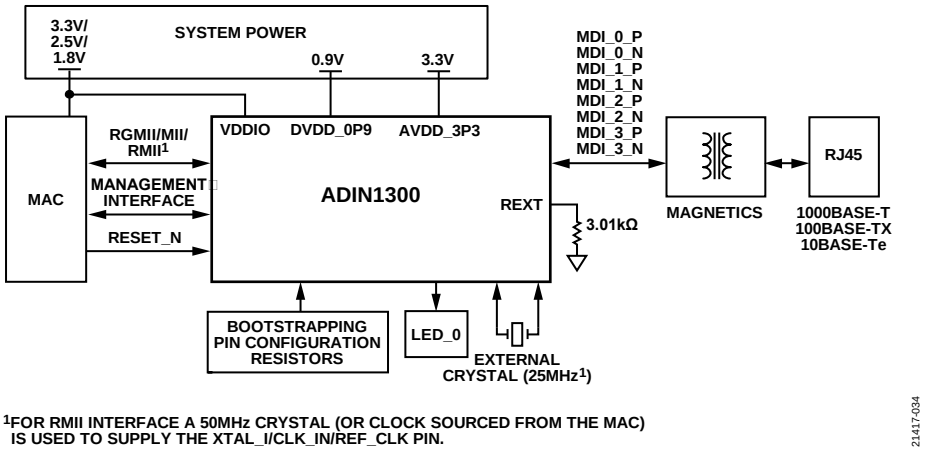


Figure 30. Simplified Typical Application Block Diagram

COMPONENT RECOMMENDATIONS

Crystal

The typical connection for an external crystal (XTAL) is shown in Figure 31. To ensure minimum current consumption and to minimize stray capacitances, make connections between the crystal, capacitors, and ground as close to the ADIN1300 as possible. Consult individual crystal vendors for recommended load information and crystal performance specifications.

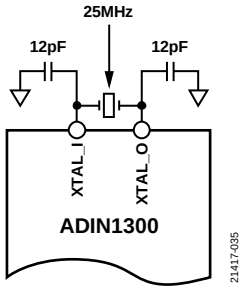


Figure 31. Crystal Oscillator Connection

External Clock Input

If using a single-ended reference clock on XTAL_I/CLK_IN/REF_CLK, leave XTAL_O open-circuit. This clock must be a unipolar 2.5 V, 25 MHz sinewave or square wave signal. The CLK_IN can also be driven by a 1.8 V square wave signal. When using the RMII MAC interface, a single, 50 MHz reference clock (REF_CLK) is required, which can be sourced from the MAC or from an external source.

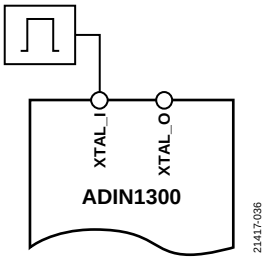


Figure 32. External Clock Connection

Magnetics

Galvanic isolation is necessary between any two point-to-point communication nodes in applications using the Ethernet protocol to transmit/receive data to protect against faults and transients, and achieve the best electromagnetic compatibility performance. Magnetic coupling between the PHY and the RJ45 is the most common way of achieving this isolation.

The magnetics can be discrete or integrated and there are strengths and weaknesses to both. Choosing the discrete option typically occupies more board space, but gives more freedom in terms of layout, tends to be cheaper than integrated magnetics, and offers better performance overall.

The integrated approach is a combined RJ45 connector jack with the magnetics built in, which provides a more compact solution due to fewer components and, in applications where space is at a premium, condenses the required footprint, but tends to cost more. Magnetics cores tend to be smaller and closer to each other, which can compromise EMC performance, increase the likelihood of crosstalk, and have impacts on performance by increasing losses and introducing nonlinear distortion.

For optimum performance, a discrete transformer with integrated common-mode choke is recommended for use with the ADIN1300 PHY. The common-mode choke is important because it attenuates any common-mode signals picked up by the twisted pair cable from the environment, improving the signal-to-noise ratio of the system. Transformers with an autotransformer stage following the common-mode choke provide additional attenuation of common-mode noise.

The ADIN1300 transmit drivers are voltage mode with on-chip terminations. Therefore, connect each of the center tap pins on the transformer on the ADIN1300 side separately to ground through a 0.1 µF capacitor.

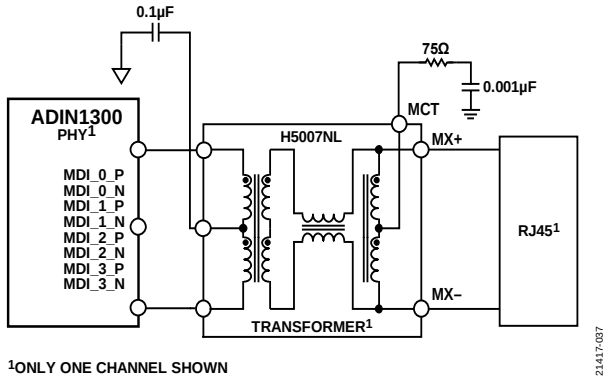


Figure 33. Isolation Using Discrete Magnetics, Only One Channel Shown, Each Channel has Separate Components to Ground

The key considerations for the magnetics are outlined in Table 29.

Table 29. Magnetics Selection

Parameter	Value	Conditions
Turns Ratio	1CT:1CT	
Open-Circuit Inductance	350 µH	Min: 100 mV, 100 kHz, 8 mA
Insertion loss	−1 dB	Max: 0 MHz to 100 MHz

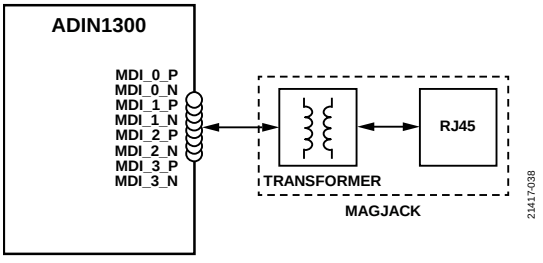


Figure 34. Magnetics Connection

POWER REQUIREMENTS

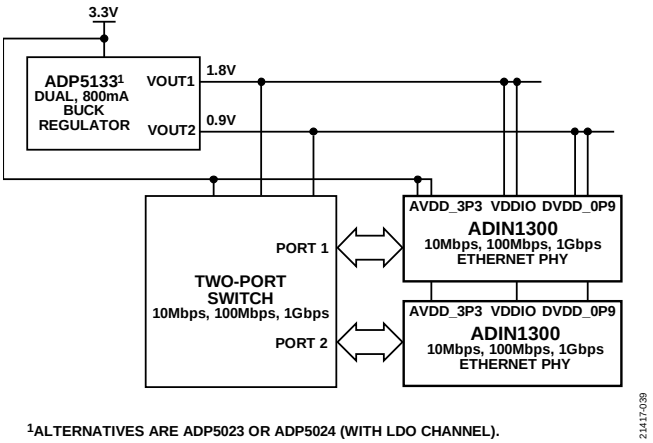
The ADIN1300 has the following three power supply domains and requires a minimum of two supply sources, 0.9 V and 3.3 V:

- DVDD_0P9 is the 0.9 V digital core power supply input.
- AVDD_3P3 is the 3.3 V analog power supply input for the PHY MDI interface, analog circuitry, crystal oscillator, DLL, RESET_N, CLK25_REF generation, and LED circuitry.

- VDDIO enables the MDIO and MAC interface voltage supply to be configured independently of the other circuitry on the ADIN1300.

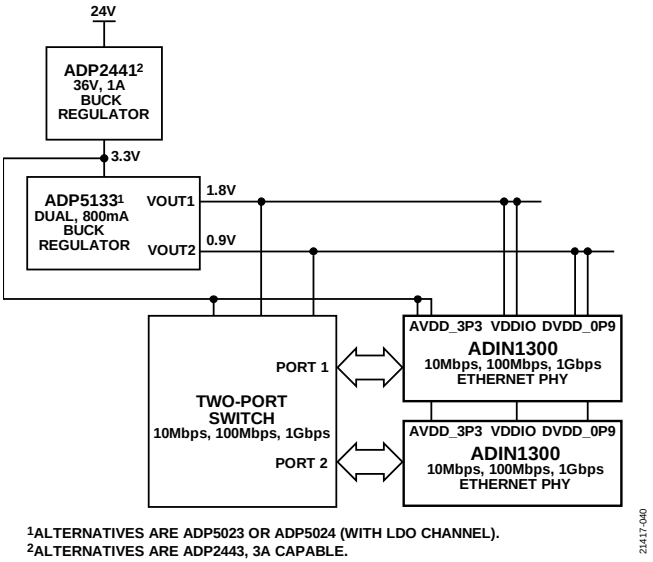
There are no power supply sequencing requirements around the order of power being applied to the device. See the Power-Up Timing section for more details.

The following simplified system level power solutions show three recommended arrangements for powering the ADIN1300 PHY and companion two-port switch (note that depending on the choice of two-port switch, there may be differing power supply requirements to what is shown).



[1]ALTERNATIVES ARE ADP5023 OR ADP5024 (WITH LDO CHANNEL).

Figure 35. Recommended Power Solution for 3.3 V with RGMI Operating at VDDIO = 1.8 V



[1]ALTERNATIVES ARE ADP5023 OR ADP5024 (WITH LDO CHANNEL).
[2]ALTERNATIVES ARE ADP2443, 3A CAPABLE.

Figure 36. Recommended Power Solution with 24 V System Power, where RGMI is Operating at VDDIO = 1.8 V

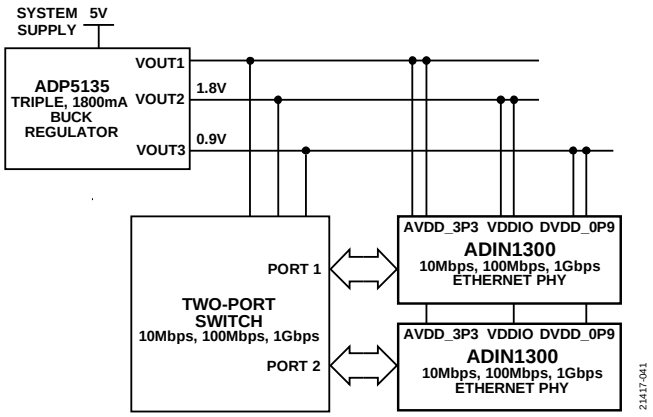


Figure 37. Recommended Power Solution using ADP5135 Triple Buck Regulator to Supply all Three Voltage Rails

SUPPLY DECOUPLING

It is recommended to decouple each of the AVDD_3P3, VDDIO, and DVDD_0P9 supply pins with 0.1 µF in parallel with 0.01 µF capacitors to ground. Place decoupling capacitors as close to the relevant pins as possible and ensure that the capacitor ground is routed directly into the plane.

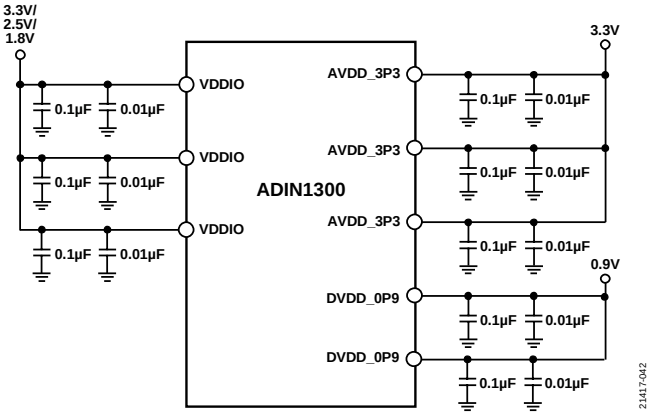


Figure 38. Supply Decoupling Overview

REGISTER SUMMARY

The MII management interface provides a 2-wire serial interface between a host processor or MAC and the ADIN1300 allowing access to control and status information in the subsystem and PHY core management registers. The interface is compatible with both IEEE Standard 802.3 Clause 22 and Clause 45 management frame structures.

The device supplements the registers specified in IEEE Standard 802.3 with an additional set of registers that are accessed indirectly. These registers are referred to as extended management interface (EMI) registers. The EMI registers can be accessed using the interface specified under Clause 45. However, for systems that do not support this interface, an alternative access mechanism is provided using the interface specified under Clause 22.

The PHY Core Register Summary section and the Subsystem Register Summary section list the PHY core and subsystem registers.

PHY CORE REGISTER SUMMARY

The PHY core registers are made up of the following three register groupings:

- 0x0000 to 0x000F, IEEE standard registers
- 0x0010 to 0x001F, vendor specific registers
- PHY core EMI registers at Device Address 0x1E

The IEEE standard registers and vendor specific registers are accessed using Clause 22 access, and the EMI registers are accessed using Clause 45 access. The ADIN1300 supports the IEEE Clause 45 MDIO manageable device (MMD) registers associated with EEE. These registers are all remapped to the Device Address 0x1E, so they are available at the same device address as the rest of the PHY extended management registers. For systems that do not support the interface specified under Clause 45, the EMI registers can be accessed using Clause 22 access via Register 0x0010 and Register 0x0011.

The default value of some of the registers are determined by the value of the hardware configuration pins, which are read just after the RESET_N pin is deasserted (see the Hardware Configuration Pins section). This allows the default operation of the ADIN1300 to be configured in unmanaged applications. The default values in Table 30 assume the ADIN1300 is configured as follows:

- Auto MDIX, prefer MDI
- Autonegotiation enabled
- All speeds advertised
- EEE, energy detect power-down, and downspeed disabled
- ADIN1300 is not configured to enter software power-down after reset
- RGMII MAC interface selected with 2 ns internal delay on RXC and TXC

Table 30. MDIOMAP_GEPHY Register Summary

Address	Name	Description	Reset	Access
0x0000	MII_CONTROL	MII Control Register.	0x1040	R/W
0x0001	MII_STATUS	MII Status Register.	0x7949	R
0x0002	PHY_ID_1	PHY Identifier 1 Register.	0x0283	R
0x0003	PHY_ID_2	PHY Identifier 2 Register.	0xBC30	R
0x0004	AUTONEG_ADV	Autonegotiation Advertisement Register.	0x01E1	R/W
0x0005	LP_ABILITY	Autonegotiation Link Partner Base Page Ability Register.	0x0000	R
0x0006	AUTONEG_EXP	Autonegotiation Expansion Register.	0x0064	R
0x0007	TX_NEXT_PAGE	Autonegotiation Next Page Transmit Register.	0x2001	R/W
0x0008	LP_RX_NEXT_PAGE	Autonegotiation Link Partner Received Next Page Register.	0x0000	R
0x0009	MSTR_SLV_CONTROL	Master Slave Control Register.	0x0200	R/W
0x000A	MSTR_SLV_STATUS	Master Slave Status Register.	0x0000	R
0x000F	EXT_STATUS	Extended Status Register.	0x3000	R
0x0010	EXT_REG_PTR	Extended Register Pointer Register.	0x0000	R/W
0x0011	EXT_REG_DATA	Extended Register Data Register.	0x0000	R/W
0x0012	PHY_CTRL_1	PHY Control 1 Register.	0x0002	R/W
0x0013	PHY_CTRL_STATUS_1	PHY Control Status 1 Register.	0x1041	R/W
0x0014	RX_ERR_CNT	Receive Error Count Register.	0x0000	R
0x0015	PHY_CTRL_STATUS_2	PHY Control Status 2 Register.	0x0000	R/W
0x0016	PHY_CTRL_2	PHY Control 2 Register.	0x0308	R/W
0x0017	PHY_CTRL_3	PHY Control 3 Register.	0x3048	R/W
0x0018	IRQ_MASK	Interrupt Mask Register.	0x0000	R/W
0x0019	IRQ_STATUS	Interrupt Status Register.	0x0000	R
0x001A	PHY_STATUS_1	PHY Status 1 Register.	0x0300	R
0x001B	LED_CTRL_1	LED Control 1 Register.	0x0001	R/W

Address	Name	Description	Reset	Access
0x001C	LED_CTRL_2	LED Control 2 Register.	0x210A	R/W
0x001D	LED_CTRL_3	LED Control 3 Register.	0x1855	R/W
0x001F	PHY_STATUS_2	PHY Status 2 Register.	0x03FC	R
0x8000	EEE_CAPABILITY	Energy Efficient Ethernet Capability Register.	0x0006	R
0x8001	EEE_ADV	Energy Efficient Ethernet Advertisement Register.	0x0000	R/W
0x8002	EEE_LP_ABILITY	Energy Efficient Ethernet Link Partner Ability Register.	0x0000	R
0x8008	EEE_RSLVD	Energy Efficient Ethernet Resolved Register.	0x0000	R
0x8402	MSE_A	Mean Square Error A Register.	0x0000	R
0x8403	MSE_B	Mean Square Error B Register.	0x0000	R
0x8404	MSE_C	Mean Square Error C Register.	0x0000	R
0x8405	MSE_D	Mean Square Error D Register.	0x0000	R
0x8E27	FLD_EN	Enhanced Link Detection Enable Register.	0x003D	R/W
0x8E38	FLD_STAT_LAT	Enhanced Link Detection Latched Status Register.	0x0000	R
0x9400	RX_MII_CLK_STOP_EN	Receive MII Clock Stop Enable Register.	0x0400	R/W
0x9401	PCS_STATUS_1	Physical Coding Sublayer (PCS) Status 1 Register.	0x0040	R
0x9403	FC_EN	Frame Checker Enable Register.	0x0001	R/W
0x9406	FC_IRQ_EN	Frame Checker Interrupt Enable Register.	0x0001	R/W
0x9407	FC_TX_SEL	Frame Checker Transmit Select Register.	0x0000	R/W
0x9408	FC_MAX_FRM_SIZE	Frame Checker Max Frame Size Register.	0x05F2	R/W
0x940A	FC_FRM_CNT_H	Frame Checker Count High Register.	0x0000	R
0x940B	FC_FRM_CNT_L	Frame Checker Count Low Register.	0x0000	R
0x940C	FC_LEN_ERR_CNT	Frame Checker Length Error Count Register.	0x0000	R
0x940D	FC_ALGN_ERR_CNT	Frame Checker Alignment Error Count Register.	0x0000	R
0x940E	FC_SYMB_ERR_CNT	Frame Checker Symbol Error Counter Register.	0x0000	R
0x940F	FC_OSZ_CNT	Frame Checker Oversized Frame Count Register.	0x0000	R
0x9410	FC_USZ_CNT	Frame Checker Undersized Frame Count Register.	0x0000	R
0x9411	FC_ODD_CNT	Frame Checker Odd Nibble Frame Count Register.	0x0000	R
0x9412	FC_ODD_PRE_CNT	Frame Checker Odd Preamble Packet Count Register.	0x0000	R
0x9413	FC_DRIBBLE_BITS_CNT	Frame Checker Dribble Bits Frame Count Register.	0x0000	R
0x9414	FC_FALSE_CARRIER_CNT	Frame Checker False Carrier Count Register.	0x0000	R
0x9415	FG_EN	Frame Generator Enable Register.	0x0000	R/W
0x9416	FG_CNTRL_RSTRT	Frame Generator Control and Restart Register.	0x0001	R/W
0x9417	FG_CONT_MODE_EN	Frame Generator Continuous Mode Enable Register.	0x0000	R/W
0x9418	FG_IRQ_EN	Frame Generator Interrupt Enable Register.	0x0000	R/W
0x941A	FG_FRM_LEN	Frame Generator Frame Length Register.	0x006B	R/W
0x941C	FG_NFRM_H	Frame Generator Number of Frames High Register.	0x0000	R/W
0x941D	FG_NFRM_L	Frame Generator Number of Frames Low Register.	0x0100	R/W
0x941E	FG_DONE	Frame Generator Done Register.	0x0000	R
0x9427	FIFO_SYNC	FIFO Sync Register.	0x0000	R/W
0x9428	SOP_CTRL	Start of Packet Control Register.	0x0034	R/W
0x9429	SOP_RX_DEL	Start of Packet Receive Detection Delay Register.	0x0000	R/W
0x942A	SOP_TX_DEL	Start of Packet Transmit Detection Delay Register.	0x0000	R/W
0x9602	DPTH_MII_BYTE	Control of FIFO Depth for MII Modes Register.	0x0001	R/W
0xA000	LPI_WAKE_ERR_CNT	LPI Wake Error Count Register.	0x0000	R
0xA001	B_1000_RTRN_EN	Base 1000 Retrain Enable Register.	0x0000	R/W
0xB403	B_10E_En	Base 10e Enable Register.	0x0001	R/W
0xB412	B_10_TX_TST_MODE	10BASE-T Transmit Test Mode Register.	0x0000	R/W
0xB413	B_100_TX_TST_MODE	100BASE-TX Transmit Test Mode Register.	0x0000	R/W
0xBA1B	CDIAG_RUN	Run Automated Cable Diagnostics Register.	0x0000	R/W
0xBA1C	CDIAG_XPAIR_DIS	Cable Diagnostics Cross Pair Fault Checking Disable Register.	0x0000	R/W
0xBA1D	CDIAG_DTLD_RSLTS_0	Cable Diagnostics Results 0 Register.	0x0000	R
0xBA1E	CDIAG_DTLD_RSLTS_1	Cable Diagnostics Results 1 Register.	0x0000	R

Address	Name	Description	Reset	Access
0xBA1F	CDIAG_DTLD_RSLTS_2	Cable Diagnostics Results 2 Register.	0x0000	R
0xBA20	CDIAG_DTLD_RSLTS_3	Cable Diagnostics Results 3 Register.	0x0000	R
0xBA21	CDIAG_FLT_DIST_0	Cable Diagnostics Fault Distance Pair 0 Register.	0x00FF	R
0xBA22	CDIAG_FLT_DIST_1	Cable Diagnostics Fault Distance Pair 1 Register.	0x00FF	R
0xBA23	CDIAG_FLT_DIST_2	Cable Diagnostics Fault Distance Pair 2 Register.	0x00FF	R
0xBA24	CDIAG_FLT_DIST_3	Cable Diagnostics Fault Distance Pair 3 Register.	0x00FF	R
0xBA25	CDIAG_CBL_LEN_EST	Cable Diagnostics Cable Length Estimate Register.	0x00FF	R
0xBC00	LED_PUL_STR_DUR	LED Pulse Stretching Duration Register.	0x0011	R/W

PHY CORE REGISTER DETAILS

MII Control Register

Address: 0x0000, Reset: 0x1040, Name: MII_CONTROL

This address corresponds to the MII control register specified in Clause 22.2.4.1 of Standard 802.3. Note that the default reset value of this register is dependent on the hardware configuration pins settings.

Table 31. Bit Descriptions for MII_CONTROL

Bits	Bit Name	Description	Reset	Access
15	SFT_RST	Software Reset Bit. Note that this bit is self clearing. When the reset operation is complete, this bit returns to 1'b0. 1: PHY reset. 0: normal operation.	0x0	R/W
14	LOOPBACK	Enable/Disable Loopback Mode. 1: enable loopback mode. 0: disable loopback mode.	0x0	R/W
13	SPEED_SEL_LSB	The speed selection MSB and LSB register bits are used to configure the link speed. Note that the default value of this register bit is configurable via the hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 11: reserved. 10: 1 Gbps. 01: 100 Mbps. 00: 10 Mbps.	0x0	R/W
12	AUTONEG_EN	The autonegotiation enable bit is used to enable/disable autonegotiation. Note that the default value of this register bit is configurable via the hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 1: enable autonegotiation process. 0: disable autonegotiation process.	0x1	R/W
11	SFT_PD	Software Power-Down Bit. Note that the default value of this register bit is configurable via the hardware configuration pins. The PHY can be held in reset until initialized by the software. 1: software power-down. 0: normal operation.	0x0	R/W
10	ISOLATE	Isolate Bit. 1: electrically isolate PHY from MAC interface by setting MAC interface pins to tristate (even if active). 0: normal operation.	0x0	R/W
9	RESTART_ANEG	Restart Autonegotiation Bit. Note that this bit is self clearing. When the autonegotiation process is restarted, this bit returns to 1'b0. 1: restart the autonegotiation process. 0: normal operation.	0x0	R/W
8	DPLX_MODE	Duplex Mode Bit. 1: full duplex. 0: half duplex.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
7	COLTEST	Collision Test Bit. 1: enable collision signal test. 0: disable collision signal test.	0x0	R/W
6	SPEED_SEL_MSB	See SPEED_SEL_LSB Bit Description. 11: reserved. 10: 1 Gbps. 01: 100 Mbps. 00: 10 Mbps.	0x1	R/W
5	UNIDIR_EN	The unidirectional enable register bit is read only and always reads as 1'b0. Transmission from the media independent interface is only enabled when the PHY has determined that a valid link has been established.	0x0	R
[4:0]	RESERVED	Reserved.	0x0	R

MII Status Register

Address: 0x0001, Reset: 0x7949, Name: MII_STATUS

This address corresponds to the MII status register specified in Clause 22.2.4.2 of IEEE Standard 802.3.

Table 32. Bit Descriptions for MII_STATUS

Bits	Bit Name	Description	Reset	Access
15	T_4_SPRT	The 100BASE-T4 ability bit always reads as 1'b0 because the PHY does not support 100BASE-T4.	0x0	R
14	FD_100_SPRT	The 100BASE-TX full duplex ability bit always reads as 1'b1 because the PHY supports 100BASE-TX full duplex.	0x1	R
13	HD_100_SPRT	The 100BASE-TX half duplex ability bit always reads as 1'b1 because the PHY supports 100BASE-TX half duplex.	0x1	R
12	FD_10_SPRT	The 10BASE-T full duplex ability bit always reads as 1'b1 because the PHY supports 10BASE-T full duplex.	0x1	R
11	HD_10_SPRT	The 10BASE-T half duplex ability bit always reads as 1'b1 because the PHY supports 10BASE-T half duplex.	0x1	R
10	FD_T_2_SPRT	The 100BASE-T2 full duplex ability bit always reads as 1'b0 because the PHY does not support 100BASE-T2.	0x0	R
9	HD_T_2_SPRT	The 100BASE-T2 half duplex ability bit always reads as 1'b0 because the PHY does not support 100BASE-T2.	0x0	R
8	EXT_STAT_SPRT	The extended status support bit always reads as 1'b1, indicating that the PHY provides extended status information in Register 0x000F.	0x1	R
7	UNIDIR_ABLE	When zero, the unidirectional ability register bit indicates that the PHY can only transmit data from the media independent interface when it has determined that a valid link has been established. This bit always reads as 1'b0.	0x0	R
6	MF_PREAM_SUP_ABLE	Management Frame Preamble Suppression Ability Bit. This always reads as 1'b1 because the PHY accepts management frames with preamble suppressed.	0x1	R
5	AUTONEG_DONE	Autonegotiation Complete Bit. 1: autonegotiation process completed. 0: autonegotiation process not completed.	0x0	R
4	REM_FLT_LAT	Remote Fault Bit. When this bit goes high, it latches high until it is unlatched by reading. 1: remote fault condition detected. 0: no remote fault condition detected.	0x0	R
3	AUTONEG_ABLE	Autonegotiation Ability Bit. This bit always reads as 1'b1. 1: PHY is able to perform autonegotiation. 0: PHY is not able to perform autonegotiation.	0x1	R
2	LINK_STAT_LAT	Link Status Bit. If the link subsequently drops, this bit latches low until it is unlatched by reading. 1: link is up. 0: link is down.	0x0	R

Bits	Bit Name	Description	Reset	Access
1	JABBER_DET_LAT	Jabber Detect Bit. When this bit goes high, it latches high until it is unlatched by reading. 1: jabber condition detected. 0: no jabber condition detected.	0x0	R
0	EXT_CAPABLE	The extended capability bit always reads as 1'b1 because the PHY provides an extended set of capabilities.	0x1	R

PHY Identifier 1 Register

Address: 0x0002, Reset: 0x0283, Name: PHY_ID_1

This address corresponds to the MII status register specified in Clause 22.2.4.3.1 of IEEE Standard 802.3 and allows 16 bits of the organizationally unique identifier (OUI) to be observed.

Table 33. Bit Descriptions for PHY_ID_1

Bits	Bit Name	Description	Reset	Access
[15:0]	PHY_ID_1	Organizationally Unique Identifier Bits[3:18].	0x283	R

PHY Identifier 2 Register

Address: 0x0003, Reset: 0xBC30, Name: PHY_ID_2

This address corresponds to the MII status register specified in Clause 22.2.4.3.1 of IEEE Standard 802.3 and allows 6 bits of the OUI along with the model number and revision number to be observed.

Table 34. Bit Descriptions for PHY_ID_2

Bits	Bit Name	Description	Reset	Access
[15:10]	PHY_ID_2_OUI	Organizationally Unique Identifier Bits[19:24].	0x2F	R
[9:4]	MODEL_NUM	Manufacturer Model Number.	0x3	R
[3:0]	REV_NUM	Manufacturer Revision Number.	0x0	R

Autonegotiation Advertisement Register

Address: 0x0004, Reset: 0x01E1, Name: AUTONEG_ADV

This address corresponds to the autonegotiation advertisement register specified in Clause 28.2.4.1.3 of IEEE Standard 802.3. Note that the default reset value of this register is dependent on the hardware configuration pins settings.

Table 35. Bit Descriptions for AUTONEG_ADV

Bits	Bit Name	Description	Reset	Access
15	NEXT_PAGE_ADV	Next page exchange occurs after the base link codewords have been exchanged. Next page exchange consists of using the normal autonegotiation arbitration process to send next page messages. Next page transmission ends when both ends of a link segment set their next page bits to Logic 0, indicating that neither has anything additional to transmit.	0x0	R/W
14	RESERVED	Reserved.	0x0	R
13	REM_FLT_ADV	The remote fault bit provides a standard transport mechanism for the transmission of simple fault information.	0x0	R/W
12	EXT_NEXT_PAGE_ADV	The extended next page bit indicates that the local device supports transmission of extended next pages. The use of extended next page is orthogonal to the negotiated data rate, medium, or link technology.	0x0	R/W
11	APAUSE_ADV	The technology ability field is a 7-bit wide field (Bits[11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise asymmetric pause operation for full duplex links.	0x0	R/W
10	PAUSE_ADV	The technology ability field is a 7-bit wide field (Bits[11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise pause operation for full duplex links.	0x0	R/W
9	T_4_ADV	The technology ability field is a 7-bit wide field (Bits[11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise 100BASE-T4 and always reads as 1'b0 because this technology is not supported.	0x0	R

Bits	Bit Name	Description	Reset	Access
8	FD_100_ADV	The technology ability field is a 7-bit wide field (Bits[11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise 100BASE-TX full duplex. Note that the default value of this register bit is configurable via the hardware configuration pins, which allows the default operation of the PHY to be configured in unmanaged applications.	0x1	R/W
7	HD_100_ADV	The technology ability field is a 7-bit wide field (Bits[11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise 100BASE-TX half duplex. Note that the default value of this register bit is configurable via the hardware configuration pins, which allows the default operation of the PHY to be configured in unmanaged applications.	0x1	R/W
6	FD_10_ADV	The technology ability field is a 7-bit wide field (Bits[11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise 10BASE-T full duplex. Note that the default value of this register bit is configurable via the hardware configuration pins, which allows the default operation of the PHY to be configured in unmanaged applications.	0x1	R/W
5	HD_10_ADV	The technology ability field is a 7-bit wide field (Bits[11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise 10BASE-T half duplex. Note that the default value of this register bit is configurable via the hardware configuration pins, which allows the default operation of the PHY to be configured in unmanaged applications.	0x1	R/W
[4:0]	SELECTOR_ADV	Selector field is a 5-bit wide field, encoding 32 possible messages. This field always reads as 1'b1, indicating that the PHY only supports IEEE Standard 802.3.	0x1	R/W

Autonegotiation Link Partner Base Page Ability Register

Address: 0x0005, Reset: 0x0000, Name: LP_ABILITY

This address corresponds to the link partner ability register specified in Clause 28.2.4.1.4 of IEEE Standard 802.3.

Table 36. Bit Descriptions for LP_ABILITY

Bits	Bit Name	Description	Reset	Access
15	LP_NEXT_PAGE	Link Partner Next Page Bit. Next page exchange occurs after the base link code words have been exchanged. Next page exchange consists of using the normal autonegotiation arbitration process to send next page messages. Next page transmission ends when both ends of a link segment set their next page bits to Logic 0, indicating that neither has anything additional to transmit.	0x0	R
14	LP_ACK	This bit is used by the internal handshaking in autonegotiation and must be ignored. 1: link partner has successfully received its link code word. 0: link partner has not received its link code word.	0x0	R
13	LP_REM_FLT	The link partner remote fault bit provides a standard transport mechanism for the transmission of simple fault information.	0x0	R
12	LP_EXT_NEXT_PAGE_ABLE	The link partner extended next page bit indicates that the link partner supports transmission of extended next page. The use of extended next page is orthogonal to the negotiated data rate, medium, or link technology.	0x0	R
11	LP_APAUSE_ABLE	The technology ability field is a 7-bit wide field (Bits[11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertises asymmetric pause operation for full duplex links.	0x0	R
10	LP_PAUSE_ABLE	The technology ability field is a 7-bit wide field (Bits[11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertises pause operation for full duplex links.	0x0	R
9	LP_T_4_ABLE	The technology ability field is a 7-bit wide field (Bits[11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertises 100BASE-T4.	0x0	R
8	LP_FD_100_ABLE	The technology ability field is a 7-bit wide field (Bits[11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertises 100BASE-TX full duplex.	0x0	R
7	LP_HD_100_ABLE	The technology ability field is a 7-bit wide field (Bits[11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertises 100BASE-TX half duplex.	0x0	R

Bits	Bit Name	Description	Reset	Access
6	LP_FD_10_ABLE	The technology ability field is a 7-bit wide field (Bits[11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertises 10BASE-T full duplex.	0x0	R
5	LP_HD_10_ABLE	The technology ability field is a 7-bit wide field (Bits[11:5] within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertises 10BASE-T half duplex.	0x0	R
[4:0]	LP_SELECTOR	Link Partner Selector Field. This is a 5-bit wide field, encoding 32 possible messages. The value 0x1 indicates IEEE Standard 802.3.	0x0	R

Autonegotiation Expansion Register

Address: 0x0006, Reset: 0x0064, Name: AUTONEG_EXP

This address corresponds to the autonegotiation expansion register specified in Clause 28.2.4.1.5 of IEEE Standard 802.3.

Table 37. Bit Descriptions for AUTONEG_EXP

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	RX_NP_LOC_ABLE	The received next page location ability bit always reads as 1'b1 because received next pages are stored in Register 0x0008. 1: received next page storage location is specified by Bit 5 (RX_NP_LOC). 0: received next page storage location is not specified by Bit 5 (RX_NP_LOC).	0x1	R
5	RX_NP_LOC	The received next page location bit always reads as 1'b1. 1: link partner next pages are stored in Register 0x0008. 0: link partner next pages are stored in Register 0x0005.	0x1	R
4	PAR_DET_FLT	Parallel Detection Fault Bit. When this bit goes high, it latches high until it is unlatched by reading. 1: a fault has been detected via the parallel detection function. 0: a fault has not been detected via the parallel detection function.	0x0	R
3	LP_NP_ABLE	Link Partner Next Page Ability Bit. 1: link partner is next page capable. 0: link partner is not next page capable.	0x0	R
2	NP_ABLE	The next page ability bit always reads as 1'b1, indicating that the PHY supports next pages. 1: local device is next page capable. 0: local device is not next page capable.	0x1	R
1	PAGE_RX_LAT	Page Received Bit. When this bit goes high, it latches high until it is unlatched by reading. 1: a new page has been received. 0: a new page has not been received.	0x0	R
0	LP_AUTONEG_ABLE	Link Partner Autonegotiation Ability Bit. 1: link partner is autonegotiation capable. 0: link partner is not autonegotiation capable.	0x0	R

Autonegotiation Next Page Transmit Register

Address: 0x0007, Reset: 0x2001, Name: TX_NEXT_PAGE

This address corresponds to the autonegotiation next page transmit register specified in Clause 28.2.4.1.6 of IEEE Standard 802.3.

Table 38. Bit Descriptions for TX_NEXT_PAGE

Bits	Bit Name	Description	Reset	Access
15	NP_NEXT_PAGE	Next page (NP) is used by the next page function to indicate that additional next page(s) follow. Otherwise, this is the last next page to be transmitted.	0x0	R/W
14	RESERVED	Reserved.	0x0	R
13	NP_MSG_PAGE	Message page (MP) is used by the next page function to indicate that this is a message page. Otherwise, this is an unformatted page.	0x1	R/W
12	NP_ACK_2	Acknowledge 2 (Ack2) is used by the next page function to indicate that a device has the ability to comply with the message.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
11	NP_TOGGLE	Toggle (T) is used by the arbitration function to ensure synchronization with the link partner during next page exchange. This bit always takes the opposite value of the toggle bit in the previously exchanged link code word.	0x0	R
[10:0]	NP_CODE	Message code field is an 11-bit wide field, encoding 2048 possible messages. If the message page bit is set to Logic 0, the bit encoding of the link code word is interpreted as an unformatted page.	0x1	R/W

Autonegotiation Link Partner Received Next Page Register

Address: 0x0008, Reset: 0x0000, Name: LP_RX_NEXT_PAGE

This address corresponds to the autonegotiation link partner received next page register specified in Clause 28.2.4.1.7 of IEEE Standard 802.3.

Table 39. Bit Descriptions for LP_RX_NEXT_PAGE

Bits	Bit Name	Description	Reset	Access
15	LP_NP_NEXT_PAGE	Link partner next page (NP) is used by the next page function to indicate that the link partner sends additional next page(s). Otherwise, this is the last next page to be transmitted.	0x0	R
14	LP_NP_ACK	This bit is used by the internal handshaking in autonegotiation and must be ignored. 1: link partner has successfully received its link code word. 0: link partner has not received its link code word.	0x0	R
13	LP_NP_MSG_PAGE	Link partner message page (MP) is used by the next page function to indicate that this is a message page. Otherwise, this is an unformatted page.	0x0	R
12	LP_NP_ACK_2	Acknowledge 2 (Ack2) is used by the next page function to indicate that the link partner has the ability to comply with the message.	0x0	R
11	LP_NP_TOGGLE	Link partner toggle (T) is used by the arbitration function to ensure synchronization with the link partner during the next page exchange. This bit always takes the opposite value of the toggle bit in the previously exchanged link code word.	0x0	R
[10:0]	LP_NP_CODE	Link partner message code field is an 11-bit wide field, encoding 2048 possible messages. If the message page bit is set to Logic 0, the bit encoding of the link code word is interpreted as an unformatted page.	0x0	R

Master Slave Control Register

Address: 0x0009, Reset: 0x0200, Name: MSTR_SLV_CONTROL

This address corresponds to the master slave control register specified in Clause 40.5.1.1 of IEEE Standard 802.3. Note that the default reset value of this register is dependent on the hardware configuration pins settings.

Table 40. Bit Descriptions for MSTR_SLV_CONTROL

Bits	Bit Name	Description	Reset	Access
[15:13]	TST_MODE	Transmitter test mode operations are defined by the test mode bits as specified in Clause 40.6.1.1.2 of IEEE Standard 802.3. 111: reserved. 110: reserved. 101: reserved. 100: Test Mode 4—transmitter distortion test. 011: Test Mode 3—transmit jitter test in slave mode. 010: Test Mode 2—transmit jitter test in master mode. 001: Test Mode 1—transmit waveform test. 000: normal operation.	0x0	R/W
12	MAN_MSTR_SLV_EN_ADV	Manual Master/Slave Enable Advertisement Bit. 1: enable master slave manual configuration value. 0: disable master slave manual configuration value.	0x0	R/W
11	MAN_MSTR_ADV	Master/Slave Advertisement Bit. 1: configure PHY as master during master slave negotiation only when MAN_MSTR_SLV_EN_ADV is set to Logical 1. 0: configure PHY as slave during master slave negotiation only when MAN_MSTR_SLV_EN_ADV is set to Logical 1.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
10	PREF_MSTR_ADV	Prefer Master (or Port Type) Advertisement Bit. This bit is used to indicate the preference to operate as master (multiport device) or as slave (single port device) if the MAN_MSTR_SLV_EN_ADV bit (Bit 9), is not set. Usage of this bit is described in Clause 40.5.2 of IEEE Standard 802.3. Note that the default value of this register bit is configurable via the hardware configuration pins, which allows the default operation of the PHY to be configured in unmanaged applications. 1: multiport device. 0: single port device.	0x0	R/W
9	FD_1000_ADV	1000BASE-T Full Duplex Advertisement Bit. Note that the default value of this register bit is configurable via the hardware configuration pins, which allows the default operation of the PHY to be configured in unmanaged applications. 1: advertise PHY is 1000BASE-T full duplex capable. 0: advertise PHY is not 1000BASE-T full duplex capable.	0x1	R/W
8	HD_1000_ADV	1000BASE-T Half Duplex Advertisement Bit. Note that the default value of this register bit is configurable via the hardware configuration pins, which allows the default operation of the PHY to be configured in unmanaged applications. 1: advertise PHY is 1000BASE-T half duplex capable. 0: advertise PHY is not 1000BASE-T half duplex capable.	0x0	R/W
[7:0]	RESERVED	Reserved.	0x0	R

Master Slave Status Register

Address: 0x000A, Reset: 0x0000, Name: MSTR_SLV_STATUS

This address corresponds to the master slave status register specified in Clause 40.5.1.1 of IEEE Standard 802.3.

Table 41. Bit Descriptions for MSTR_SLV_STATUS

Bits	Bit Name	Description	Reset	Access
15	MSTR_SLV_FLT	Master/Slave Configuration Fault Bit. When this bit goes high, it latches high until it is unlatched by reading. This bit self clears on autonegotiation enable or autonegotiation complete. See Clause 40.5.1.1 of IEEE Standard 802.3 for more details. 1: master slave configuration fault detected. 0: no master slave configuration fault detected.	0x0	R
14	MSTR_RSLVD	Master/Slave Configuration Resolution Bit. 1: local PHY configuration resolved to master. 0: local PHY configuration resolved to slave.	0x0	R
13	LOC_RCVR_STATUS	Local Receiver Status Bit. Defined by the value of LOC_RCVR_STATUS, as described in Clause 40.4.5.1 of IEEE Standard 802.3. 1: local receiver okay (LOC_RCVR_STATUS = okay). 0: local receiver not okay (LOC_RCVR_STATUS = not okay).	0x0	R
12	REM_RCVR_STATUS	Remote Receiver Status Bit. Defined by the value of REM_RCVR_STATUS as, described in Clause 40.4.5.1 of IEEE Standard 802.3. 1: remote receiver okay (REM_RCVR_STATUS = okay). 0: remote receiver not okay (REM_RCVR_STATUS = not okay).	0x0	R
11	LP_FD_1000_ABLE	Link Partner 1000BASE-T Full Duplex Ability Bit. This bit is guaranteed to be valid only when the PAGE_RX_LAT bit (Register 0x0006, Bit 1) has been set to 1. 1: link partner is capable of 1000BASE-T full duplex. 0: link partner is not capable of 1000BASE-T full duplex.	0x0	R
10	LP_HD_1000_ABLE	Link Partner 1000BASE-T Half Duplex Ability Bit. This bit is guaranteed to be valid only when the PAGE_RX_LAT bit (6.1) has been set to 1. 1: link partner is capable of 1000BASE-T half duplex. 0: link partner is not capable of 1000BASE-T half duplex.	0x0	R
[9:8]	RESERVED	Reserved.	0x0	R
[7:0]	IDLE_ERR_CNT	These idle error count bits contain a cumulative count of the errors detected when the receiver is receiving idles. See Clause 40.5.1.1 of IEEE Standard 802.3 for more details.	0x0	R

Extended Status Register

Address: 0x000F, Reset: 0x3000, Name: EXT_STATUS

This address corresponds to the extended status register specified in Clause 22.2.4.4 of IEEE Standard 802.3.

Table 42. Bit Descriptions for EXT_STATUS

Bits	Bit Name	Description	Reset	Access
15	FD_1000_X_SPRT	This bit is always zero because the PHY does not support full duplex 1000BASE-X.	0x0	R
14	HD_1000_X_SPRT	This bit is always zero because the PHY does not support half duplex 1000BASE-X.	0x0	R
13	FD_1000_SPRT	This bit is always one because the PHY supports full duplex 1000BASE-T.	0x1	R
12	HD_1000_SPRT	This bit is always one because the PHY supports half duplex 1000BASE-T.	0x1	R
[11:0]	RESERVED	Reserved.	0x0	R

Extended Register Pointer Register

Address: 0x0010, Reset: 0x0000, Name: EXT_REG_PTR

The extended register pointer and extended register data registers provide a mechanism to access the indirect access address map via directly accessible registers for cases where the station management does not support Clause 45.

Table 43. Bit Descriptions for EXT_REG_PTR

Bits	Bit Name	Description	Reset	Access
[15:0]	EXT_REG_PTR	The extended register pointer and extended register data registers provide an indirect mechanism to access EMI registers using normal Clause 22 access for cases where the station management does not support Clause 45. Write the 16-bit register address into the EXT_REG_PTR register. The EMI register can be read or written by reading or writing the EXT_REG_DATA register. An EMI register can be directly accessed using Clause 45 access.	0x0	R/W

Extended Register Data Register

Address: 0x0011, Reset: 0x0000, Name: EXT_REG_DATA

The extended register pointer and extended register data registers provide a mechanism to access the indirect access address map via directly accessible registers for cases where the station management does not support Clause 45.

Table 44. Bit Descriptions for EXT_REG_DATA

Bits	Bit Name	Description	Reset	Access
[15:0]	EXT_REG_DATA	The extended register pointer and extended register data registers provide an indirect mechanism to access EMI registers using normal Clause 22 access for cases where the station management does not support Clause 45. See Table 43 for further details.	0x0	R/W

PHY Control 1 Register

Address: 0x0012, Reset: 0x0002, Name: PHY_CTRL_1

This register provides access to various PHY control register bits, in particular for diagnostic clocking control and MDI crossover.

Table 45. Bit Descriptions for PHY_CTRL_1

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	AUTO_MDI_EN	The automatic MDI/MDIX resolution enable register bit allows the automatic cable crossover feature of the PHY to be controlled. Note that the default value of this register bit is configurable via a hardware configuration pin, which allows the default operation of the PHY to be configured in unmanaged applications. 1: enable auto MDI/MDIX. Prefer MDI if MAN_MDIX is 1'b0 and prefer MDIX if MAN_MDIX is 1'b1. 0: disable auto MDI/MDIX.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
9	MAN_MDIX	When this bit is set and the AUTO_MDI_EN bit is clear, the PHY operates in the MDIX configuration. In this configuration, no crossover is implemented and the logical pairs of the PCS correspond to the physical pairs of the AFE. When this bit is clear and the AUTO_MDI_EN bit is clear, the PHY operates in the MDI configuration and crossovers the pairs. If the AUTO_MDI_EN bit is set, the MAN_MDIX bit determines the MDI or MDIX preference option. 1: operate in MDIX configuration. 0: operate in MDI configuration.	0x0	R/W
[8:3]	RESERVED	Reserved.	0x0	R
2	DIAG_CLK_EN	Enable PHY Diagnostics Clock. This clock is required for certain diagnostic functions within the PHY, for example, the frame generator/checker. 1: enable PHY diagnostics clock. 0: disable PHY diagnostics clock.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x2	R/W

PHY Control Status 1 Register

Address: 0x0013, Reset: 0x1041, Name: PHY_CTRL_STATUS_1

This register provides access to PHY loopback control bits.

Table 46. Bit Descriptions for PHY_CTRL_STATUS_1

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R/W
12	LB_ALL_DIG_SEL	Setting this bit selects all digital loopback. This loops the data within the PHY at the analog/digital boundary so that data received on the MAC interface TXD_x pins is looped back to the RXD_x pins. This requires the IEEE loopback bit (Register 0x0000, Bit 14) to be set.	0x1	R/W
11	RESERVED	Reserved.	0x0	R
10	LB_LD_SEL	Setting this bit selects line driver loopback. If this register bit is set, every time the loopback bit is set the PHY enters line driver loopback mode. In line driver loopback mode, leave the MDI pins open to create a large impedance mismatch. The PHY can then operate by receiving the reflection from its own transmission.	0x0	R/W
9	LB_REMOTE_EN	Setting this bit enables remote loopback. This requires a link up with a remote PHY and it loops the data received from the remote PHY back to the remote PHY using all of the digital and analog circuitry of the PHY.	0x0	R/W
8	ISOLATE_RX	Setting this bit suppresses data being sent to the MAC during loopback.	0x0	R/W
7	LB_EXT_EN	Setting this bit enables external cable loopback. This requires an external cable with Pair 0 and Pair 1 and Pair 2 and Pair 3 shorted together to provide an analog loopback at the end of the cable. All of the digital and analog circuitry of the PHY and the signal processing is adjusted so that the transmitted signal is not cancelled. The IEEE loopback bit (Register 0x0000, Bit 14) must not be set.	0x0	R/W
6	LB_TX_SUP	Setting this bit suppresses the transmit signal at the MDI pins in all digital loopback.	0x1	R/W
[5:1]	RESERVED	Reserved.	0x0	R
0	LB_MII_LS_OK	Setting this bit sets the link status signal to okay during MII loopback.	0x1	R/W

Receive Error Count Register

Address: 0x0014, Reset: 0x0000, Name: RX_ERR_CNT

The receive error counter register is used to access the receive error counter associated with the frame checker in the PHY.

Table 47. Bit Descriptions for RX_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	RX_ERR_CNT	This is the receive error counter associated with the frame checker in the PHY. Note that this bit is self clearing upon reading.	0x0	R

PHY Control Status 2 Register

Address: 0x0015, Reset: 0x0000, Name: PHY_CTRL_STATUS_2

This register provides access to various PHY control and status registers, in particular autonegotiation controls and energy detect power-down control and status bits.

Table 48. Bit Descriptions for PHY_CTRL_STATUS_2

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	NRG_PD_EN	Setting this bit enables energy detect power-down. If there is no signal energy detected for a number of seconds, the PHY enters energy detect power-down mode. Note that the default value of this register bit is configurable via the hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 1: enable energy detect power-down mode. 0: disable energy detect power-down mode.	0x0	R/W
2	NRG_PD_TX_EN	When this bit is set, the PHY periodically wakes up when in energy detect power-down and transmits a number of pulses. This is to avoid a lock up situation where the PHYs on both ends of the line are in energy detect power-down mode. Note that the default value of this register bit is configurable via the hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 1: enable periodic transmission of the pulse while in energy detect power-down mode. 0: disable periodic transmission of the pulse while in energy detect power-down mode.	0x0	R/W
1	PHY_IN_NRG_PD	This status bit indicates that the PHY is in energy detect power-down mode. 1: PHY is in energy detect power-down mode. 0: PHY is not in energy detect power-down mode.	0x0	R
0	RESERVED	Reserved.	0x0	R/W

PHY Control 2 Register

Address: 0x0016, Reset: 0x0308, Name: PHY_CTRL_2

This register provides access to various PHY control registers, for control of clocking, group MDIO access, and autonegotiation.

Table 49. Bit Descriptions for PHY_CTRL_2

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R/W
11	DN_SPEED_TO_100_EN	Setting this bit enables downspeed to 100BASE-TX. Note that autonegotiation must also be enabled. If the PHY is unable to bring a link up at 1000BASE-T, it automatically drops down to 100BASE-TX (assuming this speed has been advertised). Note that the default value of this register bit is configurable via the hardware configuration pins performing the PHY_CFG1 and PHY_CFG0 functions, which allows the default operation of the PHY to be configured in unmanaged applications. 1: enable downspeed to 100BASE-TX. 0: disable downspeed to 100BASE-TX.	0x0	R/W
10	DN_SPEED_TO_10_EN	Setting this bit enables downspeed to 10BASE-T. Note that autonegotiation must also be enabled. If the PHY is unable to bring a link up at a high speed, it automatically drops down to 10BASE-T (assuming this speed has been advertised) if necessary. 1: enable downspeed to 10BASE-T. 0: disable downspeed to 10BASE-T.	0x0	R/W
[9:7]	RESERVED	Reserved.	0x6	R/W
6	GROUP_MDIO_EN	The group MDIO enable register bit may be used to place the PHY in group MDIO mode. In this mode, the PHY responds to any write or address operation to PHY address 5'd31 as if it was an access to its own PHY address. It is recommended that this bit be set only when performing specific sequences and then be cleared again.	0x0	R/W
[5:0]	RESERVED	Reserved.	0x8	R/W

PHY Control 3 Register

Address: 0x0017, Reset: 0x3048, Name: PHY_CTRL_3

This register provides access to PHY control register bits for link enable and autonegotiation controls.

Table 50. Bit Descriptions for PHY_CTRL_3

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	LINK_EN	Setting this bit enables linking. If linking is disabled, the PHY enters the standby state and does not attempt to bring up links. The standby state can be used to run diagnostics, including cable diagnostics. 1: enable linking. 0: disable linking.	0x1	R/W
[12:10]	NUM_SPEED_RETRY	If downspeed is enabled, this register bit specifies the number of retries the PHY must attempt to bring up a link at the advertised speed before advertising a lower speed. By default, the PHY attempts to bring up a link 5 times (4 retries) before downspeeding.	0x4	R/W
[9:0]	RESERVED	Reserved.	0x48	R/W

Interrupt Mask Register

Address: 0x0018, Reset: 0x0000, Name: IRQ_MASK

The interrupt mask register allows interrupts to be masked or unmasked.

Table 51. Bit Descriptions for IRQ_MASK

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R/W
10	CBL_DIAG_IRQ_EN	Cable Diagnostics Interrupt Enable Bit. 1: enable cable diagnostics interrupt. 0: disable cable diagnostics interrupt.	0x0	R/W
9	MDIO_SYNC_IRQ_EN	MDIO Synchronization Lost Interrupt Enable Bit. 1: enable MDIO synchronization lost interrupt. 0: disable MDIO synchronization lost interrupt.	0x0	R/W
8	AN_STAT_CHNG_IRQ_EN	Autonegotiation Status Changed Interrupt Enable Bit. 1: enable autonegotiation status changed interrupt. 0: disable autonegotiation status changed interrupt.	0x0	R/W
7	RESERVED	Reserved.	0x0	R/W
6	PAGE_RX_IRQ_EN	Autonegotiation Page Received Interrupt Enable Bit. 1: enable autonegotiation page received interrupt. 0: disable autonegotiation page received interrupt.	0x0	R/W
5	IDLE_ERR_CNT_IRQ_EN	Idle Error Counter Saturated Interrupt Enable Bit. 1: enable idle error counter saturated interrupt. 0: disable idle error counter saturated interrupt.	0x0	R/W
4	FIFO_OU_IRQ_EN	MAC Interface FIFO Overflow/Underflow Interrupt Enable Bit. 1: enable MAC interface FIFO overflow/underflow interrupt. 0: disable MAC interface FIFO overflow/underflow interrupt.	0x0	R/W
3	RX_STAT_CHNG_IRQ_EN	Receive Status Changed Interrupt Enable Bit. 1: enable receive status changed interrupt. 0: disable receive status changed interrupt.	0x0	R/W
2	LNK_STAT_CHNG_IRQ_EN	Link Status Changed Interrupt Enable Bit. 1: enable link status changed interrupt. 0: disable link status changed interrupt.	0x0	R/W
1	SPEED_CHNG_IRQ_EN	Speed Changed Interrupt Enable Bit. 1: enable speed changed interrupt. 0: disable speed changed interrupt.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
0	HW_IRQ_EN	When set, this enables the hardware interrupt pin, INT_N, and INT_N is asserted when an interrupt is generated. 1: enable the hardware interrupt pin, INT_N. 0: disable the hardware interrupt pin, INT_N.	0x0	R/W

Interrupt Status Register

Address: 0x0019, Reset: 0x0000, Name: IRQ_STATUS

The interrupt status register is used to check which interrupts have triggered since the last time it was read. Each bit goes high when the associated interrupt triggers and then latches high until it is unlatched by reading (note that reading any of the bits in this register unlatches all of the bits in the register). The bits of IRQ_STATUS go high even when the associated interrupts are not enabled. However, only bits associated with enabled interrupts are considered when generating the IRQ_PENDING indication.

Table 52. Bit Descriptions for IRQ_STATUS

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	CBL_DIAG_IRQ_STAT	If the cable diagnostics interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R
9	MDIO_SYNC_IRQ_STAT	If the MDIO synchronization lost interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R
8	AN_STAT_CHNG_IRQ_STAT	If the autonegotiation status changed interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R
7	RESERVED	Reserved.	0x0	R
6	PAGE_RX_IRQ_STAT	If the autonegotiation page received interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R
5	IDLE_ERR_CNT_IRQ_STAT	If the idle error counter saturated interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R
4	FIFO_OU_IRQ_STAT	If the MAC interface RGMII transmit FIFO overflow/underflow interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R
3	RX_STAT_CHNG_IRQ_STAT	If the receive status changed interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R
2	LNK_STAT_CHNG_IRQ_STAT	If the link status changed interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R
1	SPEED_CHNG_IRQ_STAT	If the speed changed interrupt status bit is 1, this indicates that the associated interrupt triggered since last read. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R
0	IRQ_PENDING	If the interrupt pending status bit is 1, this indicates that an interrupt has occurred and is pending. Note that when this bit goes high, it latches high until it is unlatched by reading.	0x0	R

PHY Status 1 Register

Address: 0x001A, Reset: 0x0300, Name: PHY_STATUS_1

This register provides access to various PHY status registers.

Table 53. Bit Descriptions for PHY_STATUS_1

Bits	Bit Name	Description	Reset	Access
15	PHY_IN_STNDBY	A 1 indicates that the PHY is in standby state and does not attempt to bring up links. The standby state can be used to run diagnostics, including cable diagnostics.	0x0	R
14	MSTR_SLV_FLT_STAT	Master Slave Configuration Fault Status Bit. A 1 indicates that a fault has occurred in the resolution of master/slave. This bit is a copy of MSTR_SLV_FLT, (MSTR_SLAV_STATUS register, Address 0x000A). Reading the MSTR_SL_FLT_STAT bit does not clear MSTR_SLV_FLT.	0x0	R
13	PAR_DET_FLT_STAT	Parallel Detection Fault Status Bit. A 1 indicates that a fault has occurred in the parallel detection process. This bit is a copy of PAR_DET_FLT, (AUTONEG_EXP register, Address 0x0006). Reading the PAR_DET_FLT_STAT bit does not clear PAR_DET_FLT.	0x0	R
12	AUTONEG_STAT	Autonegotiation Status Bit. A 1 indicates that autonegotiation has completed. This bit is a copy of AUTONEG_DONE (MII_STATUS register, Address 0x0001). Reading the AUTONEG_STAT bit does not clear AUTONEG_DONE.	0x0	R
11	PAIR_01_SWAP	A 1 indicates that Pair 0 and Pair 1 have been swapped.	0x0	R
10	B_10_POL_INV	A 1 indicates that the polarity of the 10BASE-T signal has been inverted.	0x0	R
[9:7]	HCD_TECH	This field indicates the resolved technology after the link is established. 111: reserved. 110: reserved. 101: speed resolved to 1000BASE-T full duplex. 100: speed resolved to 1000BASE-T half duplex. 011: speed resolved to 100BASE-TX full duplex. 010: speed resolved to 100BASE-TX half duplex. 001: speed resolved to 10BASE-T full duplex. 000: speed resolved to 10BASE-T half duplex.	0x6	R
6	LINK_STAT	A 1 indicates that a link is up.	0x0	R
5	TX_EN_STAT	A 1 indicates that transmit enable (TX_EN) is asserted.	0x0	R
4	RX_DV_STAT	A 1 indicates that receive data valid (RX_DV) is asserted.	0x0	R
3	COL_STAT	A 1 indicates that collision is asserted.	0x0	R
2	AUTONEG_SUP	A 1 indicates that both the local and remote PHYs support autonegotiation.	0x0	R
1	LP_PAUSE_ADV	A 1 indicates that the link partner has advertised pause. The link partner pause advertisement bit indicates that the link partner advertised support for pause operation on full duplex links. This bit provides the same information as LP_PAUSE_ABLE.	0x0	R
0	LP_APAUSE_ADV	A 1 indicates that the link partner has advertised asymmetric pause. The link partner asymmetric pause advertisement bit indicates that the link partner advertised support for asymmetric pause operation on full duplex links. This bit provides the same information as LP_APAUSE_ABLE.	0x0	R

LED Control 1 Register

Address: 0x001B, Reset: 0x0001, Name: LED_CTRL_1

This register provides access to various PHY LED control register bits.

Table 54. Bit Descriptions for LED_CTRL_1

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R/W
10	LED_A_EXT_CFG_EN	Enable Extended Configuration Set for LED_0 Pin. Also see LED_CTRL_2 register, Address 0x001C, Bits[3:0]. 1: enable extended configuration set for LED_0 pin. 0: disable extended configuration set for LED_0 pin.	0x0	R/W
[9:8]	RESERVED	Reserved.	0x0	R

Bits	Bit Name	Description	Reset	Access
[7:4]	LED_PAT_PAUSE_DUR	Internal LED Pattern Pause Duration for LED_0. After the blink pattern is driven out to the LED_0 pin, the last bit is held for a duration specified by the LED pattern pause duration register field. This duration is the value of LED tick duration (for example, the time for each bit) multiplied by the value of the LED pattern pause duration register field. Also see the LED_PAT register field (LED_CTRL_3 register, Address 0x001D, Bits[7:0]) and the LED_PAT_TICK_DUR register field (LED_CTRL_3 register, Address 0x001D, Bits[13:8]). The default blink is a 0.5 sec on and 0.5 sec off pattern.	0x0	R/W
[3:2]	LED_PUL_STR_DUR_SEL	This bit field selects the duration of the pulse stretching. 11: user-programmable. In this case, the duration of the pulse stretching is programmable by the LED_PUL_STR_DUR register (Address 0xBC00, Bits[5:0]). 10: 102 ms. 01: 64 ms. 00: 32 ms.	0x0	R/W
1	LED_OE_N	LED Active Low Output Enable Register Bit. 1: disable LED outputs. 0: enable LED outputs.	0x0	R/W
0	LED_PUL_STR_EN	Setting this bit enables pulse stretching for transmit, receive, or collision LED events so that very short duration events are visible. The LED pulse stretching enable register indicates that the PHY must stretch any pulses indicating transmit, receive, or collision. Without stretching, these pulses may be too short to cause an LED to light.	0x1	R/W

LED Control 2 Register

Address: 0x001C, Reset: 0x210A, Name: LED_CTRL_2

This register provides access to various PHY LED control register bits.

Table 55. Bit Descriptions for LED_CTRL_2

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x210	R/W
[3:0]	LED_A_CFG	LED_0 configuration is made up of five bits. These four bits, Bits[3:0], are the LSBs and Bit 4 is from LED_A_EXT_CFG_EN (LED_CTRL_1 register, Address 0x001B). The combination of the five bits configures LED_0, selecting one of 32 possible configuration functions according to the following settings. The default setting is 01010 (on if link up and blink on activity). 11111: on if 10BASE-T link, blink if 100BASE-TX link. 11110: on if 10BASE-T link, blink if 1000BASE-T link. 11101: on if 100BASE-TX link, blink if 10BASE-T link. 11100: on if 100BASE-TX link, blink if 1000BASE-T link. 11011: on if 1000BASE-T link, blink if 10BASE-T link. 11010: blink if transmit. 11001: blink on activity. 11000: on if 10BASE-T or 1000BASE-T link, blink on activity. 10111: on if 10BASE-T or 1000BASE-T link. 10110: on if 100BASE-TX or 1000BASE-T link, blink on activity. 10101: on if 10BASE-T or 100BASE-TX link, blink on activity. 10100: on if 1000BASE-T link, blink on activity. 10011: on if 100BASE-TX link, blink on activity. 10010: on if 10BASE-T link, blink on activity. 10001: on if 100BASE-TX or 1000BASE-T link. 10000: on if 10BASE-T or 100BASE-TX link. 01111: off. 01110: on. 01101: blink. 01100: on if full duplex link, blink on collision. 01011: on if link, blink if receiving. 01010: on if link, blink on activity (default).	0xA	R/W

Bits	Bit Name	Description	Reset	Access
		01001: on if collision. 01000: on if full duplex link. 00111: on if activity (transmitting or receiving). 00110: on if receiving. 00101: on if transmitting. 00100: on if link up. 00011: on if 1000BASE-T link, blink if 100BASE-TX. 00010: on if 10BASE-T link. 00001: on if 100BASE-TX link. 00000: on if 1000BASE-T link.		

LED Control 3 Register

Address: 0x001D, Reset: 0x1855, Name: LED_CTRL_3

This register provides access to various PHY LED control register bits.

Table 56. Bit Descriptions for LED_CTRL_3

Bits	Bit Name	Description	Reset	Access
[15:14]	LED_PAT_SEL	The LED_PAT_SEL bit field is always 2'b00, allowing the user to program the LED_0 blink pattern via the LED_PAT, LED_PAT_TICK_DUR, and LED_PAT_PAUSE_DUR bit fields. 11: reserved. 10: reserved. 01: reserved. 00: read/write access to LED_0 blink pattern registers.	0x0	R/W
[13:8]	LED_PAT_TICK_DUR	Each bit in the blink pattern bit field (LED_PAT) is driven to the corresponding LED pin and held for the duration specified in this 6-bit LED pattern duration bit field. The duration is the value of this register plus 1 multiplied by 8, for example, 8 ms, 16 ms, … 504 ms. The value 63 has a special meaning of 1 ms tick duration. Also see the LED_PAT_PAUSE_DUR bit field (LED_CTRL_1 register, Address 0x001B). The default blink is a 0.5 sec on and 0.5 sec off pattern.	0x18	R/W
[7:0]	LED_PAT	The internal LED pattern for LED_0 can be read or written via this field. The LED_PAT_SEL field selects which set of internal blink pattern registers for LED_0 is accessed. The default value of the LED pattern is 0x55 and is, therefore, an alternating 0/1 pattern (LED_CTRL_1 register, Address 0x001B). The default blink is a 0.5 sec on and 0.5 sec off pattern.	0x55	R/W

PHY Status 2 Register

Address: 0x001F, Reset: 0x03FC, Name: PHY_STATUS_2

This register provides access to various PHY status register bits.

Table 57. Bit Descriptions for PHY_STATUS_2

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	PAIR_23_SWAP	A 1 indicates that Pair 2 and Pair 3 have been swapped.	0x0	R
13	PAIR_3_POL_INV	A 1 indicates that the polarity on Pair 3 has been inverted.	0x0	R
12	PAIR_2_POL_INV	A 1 indicates that the polarity on Pair 2 has been inverted.	0x0	R
11	PAIR_1_POL_INV	A 1 indicates that the polarity on Pair 1 has been inverted.	0x0	R
10	PAIR_0_POL_INV	A 1 indicates that the polarity on Pair 0 has been inverted.	0x0	R
[9:1]	RESERVED	Reserved.	0x1FE	R
0	B_1000_DSCR_ACQ_ERR	A 1 indicates an error has occurred during the acquisition of the scrambler during 1000BASE-T start-up. This error can occur because the pair skew is too large.	0x0	R

Energy Efficient Ethernet Capability Register

Address: 0x8000, Reset: 0x0006, Name: EEE_CAPABILITY

This address corresponds to the EEE capability register specified in Clause 45.2.3.9 of IEEE Standard 802.3, which, in the IEEE standard, is at MMD Register Address 3.20. This register is used to indicate the capability of the PCS to support EEE functions for each PHY type.

Table 58. Bit Descriptions for EEE_CAPABILITY

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	EEE_10_G_KR_SPRT	The 10GBASE-KR EEE capability bit always reads as 1'b0. 1: EEE is supported for 10GBASE-KR. 0: EEE is not supported for 10GBASE-KR.	0x0	R
5	EEE_10_G_KX_4_SPRT	The 10GBASE-KX4 EEE capability bit always reads as 1'b0. 1: EEE is supported for 10GBASE-KX4. 0: EEE is not supported for 10GBASE-KX4.	0x0	R
4	EEE_1000_KX_SPRT	The 1000BASE-KX EEE capability bit always reads as 1'b0. 1: EEE is supported for 1000BASE-KX. 0: EEE is not supported for 1000BASE-KX.	0x0	R
3	EEE_10_G_SPRT	The 10GBASE-T EEE capability bit always reads as 1'b0. 1: EEE is supported for 10GBASE-T. 0: EEE is not supported for 10GBASE-T.	0x0	R
2	EEE_1000_SPRT	The 1000BASE-T EEE capability bit always reads as 1'b1. 1: EEE is supported for 1000BASE-T. 0: EEE is not supported for 1000BASE-T.	0x1	R
1	EEE_100_SPRT	The 100BASE-TX EEE capability bit always reads as 1'b1. 1: EEE is supported for 100BASE-TX. 0: EEE is not supported for 100BASE-TX.	0x1	R
0	RESERVED	Reserved.	0x0	R

Energy Efficient Ethernet Advertisement Register

Address: 0x8001, Reset: 0x0000, Name: EEE_ADV

This address corresponds to the EEE advertisement register specified in Clause 45.2.7.13 of Standard 802.3, which, in the IEEE standard, is at MMD Register Address 7.60. This register is used to define the EEE advertisement during autonegotiation. The reset value of this register is 0x0000 except where the hardware configuration pins are set to enable EEE. In this case, the reset value is 0x0006.

Table 59. Bit Descriptions for EEE_ADV

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	EEE_10_G_KR_ADV	The 10GBASE-KR EEE advertisement bit always reads as 1'b0. 1: advertise that the 10GBASE-KR has EEE capability. 0: do not advertise that the 10GBASE-KR has EEE capability.	0x0	R
5	EEE_10_G_KX_4_ADV	The 10GBASE-KX4 EEE advertisement bit always reads as 1'b0. 1: advertise that the 10GBASE-KX4 has EEE capability. 0: do not advertise that the 10GBASE-KX4 has EEE capability.	0x0	R
4	EEE_1000_KX_ADV	The 1000BASE-KX EEE advertisement bit always reads as 1'b0. 1: advertise that the 1000BASE-KX has EEE capability. 0: do not advertise that the 1000BASE-KX has EEE capability.	0x0	R
3	EEE_10_G_ADV	The 10GBASE-T EEE advertisement bit always reads as 1'b0. 1: advertise that the 10GBASE-T has EEE capability. 0: do not advertise that the 10GBASE-T has EEE capability.	0x0	R

Bits	Bit Name	Description	Reset	Access
2	EEE_1000_ADV	The default value of the 1000BASE-T EEE advertisement register bit is dependent on the hardware configuration pins settings. When EEE is enabled by these pins, the default value is 1'b1 and when disabled, the default value is 1'b0. 1: advertise that the 1000BASE-T has EEE capability. 0: do not advertise that the 1000BASE-T has EEE capability.	0x0	R/W
1	EEE_100_ADV	The default value of the 100BASE-TX EEE advertisement register bit is dependent on the hardware configuration pins settings. When EEE is enabled by these pins, the default value is 1'b1 and when disabled, the default value is 1'b0. 1: advertise that the 100BASE-TX has EEE capability. 0: do not advertise that the 100BASE-TX has EEE capability.	0x0	R/W
0	RESERVED	Reserved.	0x0	R

Energy Efficient Ethernet Link Partner Ability Register

Address: 0x8002, Reset: 0x0000, Name: EEE_LP_ABILITY

This address corresponds to the EEE link partner ability register specified in Clause 45.2.7.14 of Standard 802.3, which, in the IEEE standard, is at MMD Register Address 7.61. This register reflects the EEE advertisement of the link partner during autonegotiation.

Table 60. Bit Descriptions for EEE_LP_ABILITY

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	LP_EEE_10_G_KR_ABLE	Link Partner 10GBASE-KR EEE Ability Bit. 1: link partner is advertising EEE capability for 10GBASE-KR. 0: link partner is not advertising EEE capability for 10GBASE-KR.	0x0	R
5	LP_EEE_10_G_KX_4_ABLE	Link Partner 10GBASE-KX4 EEE Ability Bit. 1: link partner is advertising EEE capability for 10GBASE-KX4. 0: link partner is not advertising EEE capability for 10GBASE-KX4.	0x0	R
4	LP_EEE_1000_KX_ABLE	Link Partner 1000BASE-KX EEE Ability Bit. 1: link partner is advertising EEE capability for 1000BASE-KX. 0: link partner is not advertising EEE capability for 1000BASE-KX.	0x0	R
3	LP_EEE_10_G_ABLE	Link Partner 10GBASE-T EEE Ability Bit. 1: link partner is advertising EEE capability for 10GBASE-T. 0: link partner is not advertising EEE capability for 10GBASE-T.	0x0	R
2	LP_EEE_1000_ABLE	Link Partner 1000BASE-T EEE Ability Bit. 1: link partner is advertising EEE capability for 1000BASE-T. 0: link partner is not advertising EEE capability for 1000BASE-T.	0x0	R
1	LP_EEE_100_ABLE	Link Partner 100BASE-TX EEE Ability Bit. 1: link partner is advertising EEE capability for 100BASE-TX. 0: link partner is not advertising EEE capability for 100BASE-TX.	0x0	R
0	RESERVED	Reserved.	0x0	R

Energy Efficient Ethernet Resolved Register

Address: 0x8008, Reset: 0x0000, Name: EEE_RSLVD

This register indicates whether or not the resolved technology after the link has been established is EEE capable.

Table 61. Bit Descriptions for EEE_RSLVD

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	EEE_RSLVD	This bit indicates that the resolved technology after the link has been established is EEE capable. This is a vendor specific register bit. 1: resolved technology is EEE capable. 0: resolved technology is not EEE capable.	0x0	R

Mean Square Error A Register

Address: 0x8402, Reset: 0x0000, Name: MSE_A

This register is an indication of signal quality and is a measure of the mean square error on Dimension A.

Table 62. Bit Descriptions for MSE_A

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	MSE_A	This register is an indication of signal quality when a 100BASE-TX or 1000BASE-T link is up and is a measure of the mean square error on Dimension A.	0x0	R

Mean Square Error B Register

Address: 0x8403, Reset: 0x0000, Name: MSE_B

This register is an indication of signal quality and is a measure of the mean square error on Dimension B.

Table 63. Bit Descriptions for MSE_B

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	MSE_B	This register is an indication of signal quality when a 1000BASE-T link is up and is a measure of the mean square error on Dimension B.	0x0	R

Mean Square Error C Register

Address: 0x8404, Reset: 0x0000, Name: MSE_C

This register is an indication of signal quality and is a measure of the mean square error on Dimension C.

Table 64. Bit Descriptions for MSE_C

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	MSE_C	This register is an indication of signal quality when a 1000BASE-T link is up and is a measure of the mean square error on Dimension C.	0x0	R

Mean Square Error D Register

Address: 0x8405, Reset: 0x0000, Name: MSE_D

This register is an indication of signal quality and is a measure of the mean square error on Dimension D.

Table 65. Bit Descriptions for MSE_D

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	MSE_D	This register is an indication of signal quality when a 1000BASE-T link is up and is a measure of the mean square error on Dimension D.	0x0	R

Enhanced Link Detection Enable Register

Address: 0x8E27, Reset: 0x003D, Name: FLD_EN

This register controls the enables for the enhanced link detection function. This is early detection and indication of link loss.

Table 66. Bit Descriptions for FLD_EN

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
7	FLD_PCS_ERR_B_100_EN	Enhanced link detection PCS receive error detection enable for 100BASE-TX.	0x0	R/W
6	FLD_PCS_ERR_B_1000_EN	Enhanced link detection PCS receive error detection enable for 1000BASE-T.	0x0	R/W
5	FLD_SLCR_OUT_STUCK_B_100_EN	Enhanced link detection PMA slicer output stuck at detection enable for 100BASE-TX.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
4	FLD_SLCR_OUT_STUCK_B_1000_EN	Enhanced link detection PMA slicer output stuck at detection enable for 1000BASE-T.	0x1	R/W
3	FLD_SLCR_IN_ZDET_B_100_EN	Enhanced link detection PMA slicer input zero detection enable for 100BASE-TX.	0x1	R/W
2	FLD_SLCR_IN_ZDET_B_1000_EN	Enhanced link detection PMA slicer input zero detection enable for 1000BASE-T.	0x1	R/W
1	FLD_SLCR_IN_INVLD_B_100_EN	Enhanced link detection PMA slicer input invalid level detection enable for 100BASE-TX. Enabled when set high.	0x0	R/W
0	FLD_SLCR_IN_INVLD_B_1000_EN	Enhanced link detection PMA slicer input invalid level detection enable for 1000BASE-T. Enabled when set high.	0x1	R/W

Enhanced Link Detection Latched Status Register

Address: 0x8E38, Reset: 0x0000, Name: FLD_STAT_LAT

This register is the latched status for the enhanced link detection function. This bit is latched until the start of the next link-up, when it is cleared.

Table 67. Bit Descriptions for FLD_STAT_LAT

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	FAST_LINK_DOWN_LAT	Main Enhanced Link Detection Latched Indication.	0x0	R
[12:0]	RESERVED	Reserved.	0x0	R

Receive MII Clock Stop Enable Register

Address: 0x9400, Reset: 0x0400, Name: RX_MII_CLK_STOP_EN

This register contains the clock stop enable bit specified in Clause 45.2.3.1.4 of IEEE Standard 802.3, which, in the IEEE standard, is at MMD Register Address 3.0, Bit 10.

Table 68. Bit Descriptions for RX_MII_CLK_STOP_EN

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	RX_MII_CLK_STOP_EN	If this bit is set, the PHY may stop the receive MII clock while it is signaling low power enable (LPI). Otherwise, it keeps the clock active. 1: the PHY may stop the clock during LPI. 0: clock not stoppable.	0x1	R/W
[9:0]	RESERVED	Reserved.	0x0	R

PCS Status 1 Register

Address: 0x9401, Reset: 0x0040, Name: PCS_STATUS_1

The bits contained in this register correspond to the bits in the PCS Status 1 register specified in Clause 45.2.3.2 of IEEE Standard 802.3, which, in the IEEE standard, is at MMD Register Address 3.1, Bits[11:8] and Bit 6.

Table 69. Bit Descriptions for PCS_STATUS_1

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
11	TX_LPI_RCVD	The transmit LPI received bit is a latched version of TX_LPI. When this bit goes high, it latches high until it is unlatched by reading. 1: transmit PCS has received LPI. 0: LPI not received.	0x0	R
10	RX_LPI_RCVD	The receive LPI received bit is a latched version of RX_LPI. When this bit goes high, it latches high until it is unlatched by reading. 1: receive PCS has received LPI. 0: LPI not received.	0x0	R

Bits	Bit Name	Description	Reset	Access
9	TX_LPI	Transmit LPI Bit. 1: transmit PCS is currently receiving LPI. 0: PCS is not currently receiving LPI.	0x0	R
8	RX_LPI	Receive LPI Bit. 1: receive PCS is currently receiving LPI. 0: PCS is not currently receiving LPI.	0x0	R
7	RESERVED	Reserved.	0x0	R
6	TX_MII_CLK_STOP_CPBL	The transmit MII clock stop capable bit always reads as 1'b1. 1: the MAC may stop the clock during LPI. 0: clock not stoppable.	0x1	R
[5:0]	RESERVED	Reserved.	0x0	R

Frame Checker Enable Register

Address: 0x9403, Reset: 0x0001, Name: FC_EN

This register is used to enable the frame checker. The frame checker analyzes the received frames from either the MAC interface or the PHY (see the FC_TX_SEL register, Address 0x9407, Bit 0) to report the number of frames received, CRC errors, and various other frame errors. The frame checker frame and error counter registers count these events.

Table 70. Bit Descriptions for FC_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FC_EN	When set, this bit enables the frame checker.	0x1	R/W

Frame Checker Interrupt Enable Register

Address: 0x9406, Reset: 0x0001, Name: FC_IRQ_EN

This register is used to enable the frame checker interrupt. An interrupt is generated when a receive error occurs. Enable the frame checker/generator interrupt in the interrupt mask register. Set the FC_FG_IRQ_EN bit (IRQ_MASK register, Address 0x0018). The interrupt status can be read via the FC_FG_IRQ_STAT bit (IRQ_STATUS register, Address 0x0019).

Table 71. Bit Descriptions for FC_IRQ_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FC_IRQ_EN	When set, this bit enables the frame checker interrupt.	0x1	R/W

Frame Checker Transmit Select Register

Address: 0x9407, Reset: 0x0000, Name: FC_TX_SEL

This register is used to select the transmit side or receive side for frames to be checked. If set, frames received on the MAC interface to be transmitted are checked. The frame checker can be used to verify that correct data is received over the MAC interface and is also useful if remote loopback is enabled (set the LB_REMOTE_EN bit the in PHY_CTRL_STATUS_1 register, Address 0x0013, Bit 9) because it can be used to check the received data after it is looped back at the MAC interface.

Table 72. Bit Descriptions for FC_TX_SEL

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FC_TX_SEL	When set, this bit indicates that the frame checker must check frames received to be transmitted by the PHY. 1: check frames from the MAC interface to be transmitted by the PHY. 0: check frames received by the PHY from the remote end.	0x0	R/W

Frame Checker Maximum Frame Size Register

Address: 0x9408, Reset: 0x05F2, Name: FC_MAX_FRM_SIZE

This register specifies the maximum frame size. Frames longer than this size are counted as oversized frames.

Table 73. Bit Descriptions for FC_MAX_FRM_SIZE

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_MAX_FRM_SIZE	This bit field specifies the max frame size. Received frames that are longer than this are counted as oversized frames. Note, this frame length excludes the preamble and start frame delimiter.	0x5F2	R/W

Frame Checker Count High Register

Address: 0x940A, Reset: 0x0000, Name: FC_FRM_CNT_H

This register is a latched copy of Bits[31:16] of the 32-bit receive frame counter register. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the receive frame counter register is latched. A copy of the receive frame counter register is latched when recant is read so that the error count and receive frame count are synchronized.

Table 74. Bit Descriptions for FC_FRM_CNT_H

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_FRM_CNT_H	Bits[31:16] of Latched Copy of the Number of Received Frames.	0x0	R

Frame Checker Count Low Register

Address: 0x940B, Reset: 0x0000, Name: FC_FRM_CNT_L

This register is a latched copy of Bits[15:0] of the 32-bit receive frame counter register. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the receive frame counter register is latched. A copy of the receive frame counter register is latched when RX_ERR_CNT is read so that the error count and receive frame count are synchronized.

Table 75. Bit Descriptions for FC_FRM_CNT_L

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_FRM_CNT_L	Bits[15:0] of Latched Copy of the Number of Received Frames.	0x0	R

Frame Checker Length Error Count Register

Address: 0x940C, Reset: 0x0000, Name: FC_LEN_ERR_CNT

This register is a latched copy of the frame length error counter register. This register is a count of received frames with a length error status. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the frame length error counter register is latched, which ensures that the frame length error count and receive frame count are synchronized.

Table 76. Bit Descriptions for FC_LEN_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_LEN_ERR_CNT	Latched Copy of the Frame Length Error Counter.	0x0	R

Frame Checker Alignment Error Count Register

Address: 0x940D, Reset: 0x0000, Name: FC_ALGN_ERR_CNT

This register is a latched copy of the frame alignment error counter register. This register is a count of received frames with an alignment error status. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the alignment error counter register is latched, which ensures that the frame alignment error count and receive frame count are synchronized.

Table 77. Bit Descriptions for FC_ALGN_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_ALGN_ERR_CNT	Latched Copy of the Frame Alignment Error Counter.	0x0	R

Frame Checker Symbol Error Counter Register

Address: 0x940E, Reset: 0x0000, Name: FC_SYMB_ERR_CNT

This register is a latched copy of the symbol error counter register. This register is a count of received frames with both RX_ER and RX_DV set. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the symbol error counter register is latched, which ensures that the symbol error count and receive frame count are synchronized.

Table 78. Bit Descriptions for FC_SYMB_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_SYMB_ERR_CNT	Latched Copy of the Symbol Error Counter.	0x0	R

Frame Checker Oversized Frame Count Register

Address: 0x940F, Reset: 0x0000, Name: FC_OSZ_CNT

This register is a latched copy of the oversized frame error counter register. This register is a count of received frames with a length greater than specified in frame checker maximum frame size (FC_MAX_FRM_SIZE register, Address 0x9407). When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the oversized frame error counter register is latched, which ensures that the oversized frame error count and receive frame count are synchronized.

Table 79. Bit Descriptions for FC_OSZ_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_OSZ_CNT	Latched Copy of the Oversized Frame Error Counter.	0x0	R

Frame Checker Undersized Frame Count Register

Address: 0x9410, Reset: 0x0000, Name: FC_USZ_CNT

This register is a latched copy of the undersized frame error counter register. This register is a count of received frames with a length less than 64 bytes. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the undersized frame error counter register is latched, which ensures that the undersized frame error count and receive frame count are synchronized.

Table 80. Bit Descriptions for FC_USZ_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_USZ_CNT	Latched Copy of the Undersized Frame Error Counter.	0x0	R

Frame Checker Odd Nibble Frame Count Register

Address: 0x9411, Reset: 0x0000, Name: FC_ODD_CNT

This register is a latched copy of the odd nibble frame counter register. This register is a count of received frames with an odd number of nibbles in the frame in 100BASE-TX or 10BASE-T mode. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the odd nibble frame counter register is latched, which ensures that the odd nibble frame count and receive frame count are synchronized.

Table 81. Bit Descriptions for FC_ODD_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_ODD_CNT	Latched Copy of the Odd Nibble Counter.	0x0	R

Frame Checker Odd Preamble Packet Count Register

Address: 0x9412, Reset: 0x0000, Name: FC_ODD_PRE_CNT

This register is a latched copy of the odd preamble packet counter register. This register is a count of received frames with an odd number of nibbles in the preamble in 100BASE-TX mode. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the odd preamble packet counter register is latched, which ensures that the odd preamble packet count and receive frame count are synchronized.

Table 82. Bit Descriptions for FC_ODD_PRE_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_ODD_PRE_CNT	Latched Copy of the Odd Preamble Packet Counter.	0x0	R

Frame Checker Dribble Bits Frame Count Register

Address: 0x9413, Reset: 0x0000, Name: FC_DRIBBLE_BITS_CNT

This register is a latched copy of the dribble bits frame counter register. This register is a count of received frames with a noninteger number of nibbles in 10BASE-T mode. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the dribble bits frame counter register is latched, which ensures that the dribble bits frame count and receive frame count are synchronized.

Table 83. Bit Descriptions for FC_DRIBBLE_BITS_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_DRIBBLE_BITS_CNT	Latched Copy of the Dribble Bits Frame Counter.	0x0	R

Frame Checker False Carrier Count Register

Address: 0x9414, Reset: 0x0000, Name: FC_FALSE_CARRIER_CNT

This register is a latched copy of the false carrier events counter register. This is a count of the number of times the BAD SSD state is entered. When the receive error counter (RX_ERR_CNT register, Address 0x0014) is read, the false carrier events counter register is latched, which ensures that the false carrier events count and receive frame count are synchronized.

Table 84. Bit Descriptions for FC_FALSE_CARRIER_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	FC_FALSE_CARRIER_CNT	Latched Copy of the False Carrier Events Counter.	0x0	R

Frame Generator Enable Register

Address: 0x9415, Reset: 0x0000, Name: FG_EN

This register is used to enable the frame generator. When the frame generator is enabled, the source of data for the PHY comes from the frame generator and not the MAC interface. To use the frame generator, the diagnostic clock must also be enabled. Set the DIAG_CLK_EN bit (PHY_CTRL_1 register, Address 0x0012, Bit 2).

Table 85. Bit Descriptions for FG_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_EN	When set, this bit enables the built-in frame generator.	0x0	R/W

Frame Generator Control and Restart Register

Address: 0x9416, Reset: 0x0001, Name: FG_CNTRL_RSTRT

This register provides frame generator control and restart functions.

Table 86. Bit Descriptions for FG_CNTRL_RSTRT

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	FG_RSTRT	When set, this bit restarts the frame generator. This bit is self clearing.	0x0	R/W
[2:0]	FG_CNTRL	This bit field controls the frame generator in accordance with the following encoding: 111: reserved. 110: reserved. 101: data field decrementing from 255 (decimal) to 0. 100: alternative 0x55 in the MAC client data frame field. 011: all ones in the MAC client data frame field. 010: all zeros in the MAC client data frame field. 001: random number in the MAC client data frame field. 000: no frames after completion of current frame.	0x1	R/W

Frame Generator Continuous Mode Enable Register

Address: 0x9417, Reset: 0x0000, Name: FG_CONT_MODE_EN

This register is used to put the frame generator into continuous mode. The default mode of operation is burst mode, where the number of frames generated is specified by the FG_NFRM_H register and FG_NFRM_L register (Address 0x941C and Address 0x941D).

Table 87. Bit Descriptions for FG_CONT_MODE_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_CONT_MODE_EN	This bit is used to put the frame generator into continuous mode or burst mode. 1: frame generator operates in continuous mode. In this mode, the frame generator keeps generating frames indefinitely. 0: frame generator operates in burst mode. In this mode, the frame generator generates a single burst of frames and then stops. The number of frames in the burst is determined by the FG_NFRM_H register and FG_NFRM_L register.	0x0	R/W

Frame Generator Interrupt Enable Register

Address: 0x9418, Reset: 0x0000, Name: FG_IRQ_EN

This register is used to enable the frame generator interrupt. An interrupt is generated when the requested number of frames has been generated. Enable the frame checker/generator interrupt in the IRQ_MASK register. Set the FC_FG_IRQ_EN bit (Address 0x0018, Bit 7). The interrupt status can be read via the IRQ_STATUS register, FC_FG_IRQ_STAT bit (Address 0x0019, Bit 7).

Table 88. Bit Descriptions for FG_IRQ_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_IRQ_EN	When set, this bit indicates that the frame generator must generate an interrupt when it has transmitted the programmed number of frames. 1: enable the frame generator interrupt. 0: disable the frame generator interrupt.	0x0	R/W

Frame Generator Frame Length Register

Address: 0x941A, Reset: 0x006B, Name: FG_FRM_LEN

This register specifies the MAC client data field frame length in bytes. In addition to the data field, 6 bytes are added for the source address, 6 bytes for the destination address, 2 bytes for the length field, and 4 bytes for the frame check sequence (FCS). The total frame length is the data field length plus 18.

Table 89. Bit Descriptions for FG_FRM_LEN

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_FRM_LEN	The Data Field Frame Length in Bytes.	0x6B	R/W

Frame Generator Number of Frames High Register

Address: 0x941C, Reset: 0x0000, Name: FG_NFRM_H

This register is Bits[31:16] of a 32-bit register that specifics the number of frames to be generated each time the frame generator is enabled or restarted.

Table 90. Bit Descriptions for FG_NFRM_H

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_NFRM_H	Bits[31:16] of the Number of Frames to be Generated.	0x0	R/W

Frame Generator Number of Frames Low Register

Address: 0x941D, Reset: 0x0100, Name: FG_NFRM_L

This register is Bits[15:0] of a 32-bit register that specifics the number of frames to be generated each time the frame generator is enabled or restarted.

Table 91. Bit Descriptions for FG_NFRM_L

Bits	Bit Name	Description	Reset	Access
[15:0]	FG_NFRM_L	Bits[15:0] of the Number of Frames to be Generated.	0x100	R/W

Frame Generator Done Register

Address: 0x941E, Reset: 0x0000, Name: FG_DONE

This register is used to indicate that the frame generator has completed the generation of the number of frames requested in the FG_NFRM_H register and FG_NFRM_L register (Address 0x941C and Address 0x941D, respectively).

Table 92. Bit Descriptions for FG_DONE

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FG_DONE	This bit reads as 1'b1 to indicate that the generation of frames has completed. When set, this bit goes high and it latches high until it is unlatched by reading.	0x0	R

FIFO_SYNC Register

Address: 0x9427, Reset: 0x0000, Name: FIFO_SYNC

When set, the transmit FIFO is configured for synchronous operation (except in 1000BASE-T slave mode) to minimize latency.

Table 93. Bit Descriptions for FIFO_SYNC

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FIFO_SYNC	FIFO_SYNC. When set, the transmit FIFO is configured for synchronous operation (except in 1000BASE-T slave mode) to minimize latency.	0x0	R/W

Start of Packet Control Register

Address: 0x9428, Reset: 0x0034, Name: SOP_CTRL

This register controls the start of packet (SOP) detection for IEEE 1588 time stamp controls.

Table 94. Bit Descriptions for SOP_CTRL

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
[6:4]	SOP_N_8_CYCM_1	When the SOP_NCYC_EN bit is set, the SOP_N_8_CYCM_1 bit field specifies the number of cycles of the MII RX_CLK clock that the transmit and receive SOP indications remain asserted. Add 1 to the value specified and then multiply by 8 to get the number of cycles. Note that the SOP indications are always deasserted at the end of the frame.	0x3	R/W
3	SOP_NCYC_EN	When this bit is set, the duration of the transmit and receive SOP indications are defined by the SOP_N_8_CYCM_1 bit field. Otherwise, the SOP indications are set for the duration of the frame.	0x0	R/W
2	SOP_SFD_EN	When this bit is set, SFD detection is enabled, so that the SOP signals are asserted when the SFD in the frame is detected. If this register bit is cleared, the SOP signals are asserted on the first byte or nibble of the frame. Note that if this signal is changed while packets are being transmitted or received, the SOP signals may be wrongly asserted. Therefore, only change the signal while the link is down or when SOP_TX_EN and SOP_RX_EN are cleared.	0x1	R/W
1	SOP_RX_EN	When set, this bit enables the generation of SOP detection for received frames.	0x0	R/W
0	SOP_TX_EN	When set, this bit enables the generation of SOP detection for transmitted frames. To minimize the SOP indication variation, the detection is done after the transmit FIFO for modes in which the transmit FIFO is used.	0x0	R/W

Start of Packet Receive Detection Delay Register

Address: 0x9429, Reset: 0x0000, Name: SOP_RX_DEL

This register controls the receive side SOP detection delay.

Table 95. Bit Descriptions for SOP_RX_DEL

Bits	Bit Name	Description	Reset	Access
[15:11]	SOP_RX_10_DEL_NCYC	This bit field specifies the number of cycles of the MII RX_CLK clock to delay the received frames SOP indication for 10BASE-T links.	0x0	R/W
[10:6]	SOP_RX_100_DEL_NCYC	This bit field specifies the number of cycles of the MII RX_CLK clock to delay the received frames SOP indication for 100BASE-TX links.	0x0	R/W
[5:0]	SOP_RX_1000_DEL_NCYC	This register field specifies the number of cycles of the receive clock (for example, 8 ns cycles) to delay the received frames SOP indication for 1000BASE-T links. It is mainly intended to support MAC interfaces with long latency in Gigabit mode (like SGMII) so that the received frame SOP indication is not asserted before the MAC receives the frame.	0x0	R/W

Start of Packet Transmit Detection Delay Register

Address: 0x942A, Reset: 0x0000, Name: SOP_TX_DEL

This register controls the transmit side SOP detection delay.

Table 96. Bit Descriptions for SOP_TX_DEL

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
[12:8]	SOP_TX_10_DEL_N_8_NS	This bit field specifies the number of 8 ns periods to delay the transmitted frames SOP indication for 10BASE-T links. To align the transmit SOP indication assertion close to the reference point set on the MDI pins, set this register to 5'd20.	0x0	R/W
[7:4]	SOP_TX_100_DEL_N_8_NS	This bit field specifies the number of 8 ns periods to delay the transmitted frames SOP indication for 100BASE-TX links. To align the transmit SOP indication assertion close to the reference point set on the MDI pins, set this register to 4'd0.	0x0	R/W
[3:0]	SOP_TX_1000_DEL_N_8_NS	This bit field specifies the number of 8 ns periods to delay the transmitted frames SOP indication for 1000BASE-T links. To align the transmit SOP indication assertion close to the reference point set on the MDI pins (so that the timestamping point does not have to be adjusted at the MAC/switch side), set this register to 4'd6.	0x0	R/W

Control of FIFO Depth for MII Modes Register

Address: 0x9602, Reset: 0x0001, Name: DPTH_MII_BYTE

FIFO depth in bytes in MII modes.

Table 97. Bit Descriptions for DPTH_MII_BYTE

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	DPTH_MII_BYTE	Applies to MII modes for 10 Mbps and 100 Mbps. When set, the FIFO depth is in bytes. When zero, the FIFO depth is in nibbles. The default value of this bit is 1. Therefore, the FIFO prefill is set in bytes. In MII mode, because the interface is nibble based, the internal prefill in the transmit FIFO is larger and, therefore, the latency is longer.	0x1	R/W

LPI Wake Error Count Register

Address: 0xA000, Reset: 0x0000, Name: LPI_WAKE_ERR_CNT

This address corresponds to the EEE wake error counter register specified in Clause 45.2.3.10 of IEEE Standard 802.3, which in the IEEE standard is at MMD Register Address 3.22.

Table 98. Bit Descriptions for LPI_WAKE_ERR_CNT

Bits	Bit Name	Description	Reset	Access
[15:0]	LPI_WAKE_ERR_CNT	This bit field counts wake time faults where the PHY fails to complete its normal wake sequence within the time required. This field self clears upon reading.	0x0	R

Base 1000 Retrain Enable Register

Address: 0xA001, Reset: 0x0000, Name: B_1000_RTRN_EN

This register allows 1000BASE-T retrain to be enabled. When 1000BASE-T retrain is enabled and the receiver status becomes not okay, the PHY retrains. During this time, the link remains up but it is not possible to transmit or receive data. When 1000BASE-T retrain is disabled and the receiver status becomes not okay, the PHY drops the link.

Table 99. Bit Descriptions for B_1000_RTRN_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	B_1000_RTRN_EN	When set, this bit enables 1000BASE-T retrain. Clause 40.4.6.1 of Standard 802.3 requires a PHY that is operating in 1000BASE-T mode to retrain if it detects that its receiver status is not okay. Such a retrain prevents data from being transmitted or received for a long period, but does not cause the LINK_STAT_LAT bit in the direct address map to latch low. When B_1000_RTRN_EN is clear, 1000BASE-T retrain is disabled. In this case, when the receiver status becomes not okay, it always results in the link dropping. 1: 1000BASE-T retrain is enabled. 0: 1000BASE-T retrain is disabled.	0x0	R/W

Base 10e Enable Register

Address: 0xB403, Reset: 0x0001, Name: B_10_E_EN

When set, this register enables 10BASE-Te operation. 10BASE-Te is a variant of 10BASE-T that transmits at a lower voltage level.

Table 100. Bit Descriptions for B_10_E_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	B_10_E_EN	10BASE-Te. When set, this bit enables 10BASE-Te operation, this is the default operation of the device. 10BASE-Te is a variant of 10BASE-T that transmits at a lower voltage level.	0x1	R/W

10BASE-T Transmit Test Mode Register

Address: 0xB412, Reset: 0x0000, Name: B_10_TX_TST_MODE

This register provides the ability to transmit a 10BASE-T test signal.

Table 101. Bit Descriptions for B_10_TX_TST_MODE

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
[2:0]	B_10_TX_TST_MODE	The PHY provides the ability to transmit a 10BASE-T test signal consisting of either a 5 MHz or a 10 MHz square wave. 111: reserved. 110: reserved. 101: reserved. 100: transmit 5 MHz square wave on Dimension 1.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		011: transmit 5 MHz square wave on Dimension 0. 010: transmit 10 MHz square wave on Dimension 1. 001: transmit 10 MHz square wave on Dimension 0. 000: 10BASE-T test mode disabled.		

100BASE-TX Transmit Test Mode Register

Address: 0xB413, Reset: 0x0000, Name: B_100_TX_TST_MODE

This register provides the ability to transmit a 100BASE-TX test signal.

Table 102. Bit Descriptions for B_100_TX_TST_MODE

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
[2:0]	B_100_TX_TST_MODE	The PHY provides the ability to transmit a 100BASE-TX test signal that cycles continuously through the valid MLT3 signal levels: zero, positive, zero, and negative. Each transmit level can be held for either 16 ns (short dwell time) or 112 ns (long dwell time). The MLT3 transmit test waveform with a 16 ns dwell time measures duty cycle distortion, as specified in Clause 9.1.8 of ANSI Standard X3.263. The MLT3 transmit test waveform with a 112 ns dwell time measures waveform overshoot, amplitude symmetry, and rise/fall times, as specified in Clauses 9.1.3, 9.1.4, and 9.1.6 of ANSI Standard X3.263. 111: reserved. 110: reserved. 101: reserved. 100: transmit MLT3 test waveform, 112 ns dwell time on Dimension 1. 011: transmit MLT3 test waveform, 112 ns dwell time on Dimension 0. 010: transmit MLT3 test waveform, 16 ns dwell time on Dimension 1. 001: transmit MLT3 test waveform, 16 ns dwell time on Dimension 0. 000: 100BASE-TX test mode disabled.	0x0	R/W

Run Automated Cable Diagnostics Register

Address: 0xBA1B, Reset: 0x0000, Name: CDIAG_RUN

This register is used to start the automated running of cable diagnostics and to return results in the cable diagnostic results registers.

Table 103. Bit Descriptions for CDIAG_RUN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CDIAG_RUN	When set, this bit starts an automatic cable diagnostics run. Run this bit with the PHY in standby. Clear the LINK_EN bit (PHY_CTRL_3 register, Address 0x0017, Bit 13). This bit self clears when the cable diagnostics are completed.	0x0	R/W

Cable Diagnostics Cross Pair Fault Checking Disable Register

Address: 0xBA1C, Reset: 0x0000, Name: CDIAG_XPAIR_DIS

This register allows the checking of cross pair faults in the cable diagnostics to be disabled.

Table 104. Bit Descriptions for CDIAG_XPAIR_DIS

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CDIAG_XPAIR_DIS	When set, this bit disables cross pair fault checking. 1: disable cross pair fault checking. 0: enable cross pair fault checking.	0x0	R/W

Cable Diagnostics Results 0 Register

Address: 0xBA1D, Reset: 0x0000, Name: CDIAG_DTLD_RSLTS_0

This register provides cable diagnostics results for Pair 0.

Table 105. Bit Descriptions for CDIAG_DTLD_RSLTS_0

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	CDIAG_RSLT_0_BSY	When set, this bit indicates that Pair 0 is busy. This bit indicates that there was unknown activity on Pair 0 during cable diagnostics.	0x0	R
9	CDIAG_RSLT_0_XSIM_3	When set, this bit indicates that there is a significant impedance cross pair short between Pair 0 and Pair 3.	0x0	R
8	CDIAG_RSLT_0_XSIM_2	When set, this bit indicates that there is a significant impedance cross pair short between Pair 0 and Pair 2.	0x0	R
7	CDIAG_RSLT_0_XSIM_1	When set, this bit indicates that there is a significant impedance cross pair short between Pair 0 and Pair 1.	0x0	R
6	CDIAG_RSLT_0_SIM	When set, this bit indicates that there is a significant impedance mismatch on Pair 0.	0x0	R
5	CDIAG_RSLT_0_XSHRT_3	When set, this bit indicates that there is a cross pair short between Pair 0 and Pair 3.	0x0	R
4	CDIAG_RSLT_0_XSHRT_2	When set, this bit indicates that there is a cross pair short between Pair 0 and Pair 2.	0x0	R
3	CDIAG_RSLT_0_XSHRT_1	When set, this bit indicates that there is a cross pair short between Pair 0 and Pair 1.	0x0	R
2	CDIAG_RSLT_0_SHRT	When set, this bit indicates that there is a short on Pair 0.	0x0	R
1	CDIAG_RSLT_0_OPN	When set, this bit indicates that there is an open on Pair 0.	0x0	R
0	CDIAG_RSLT_0_GD	When set, this bit indicates that Pair 0 is well terminated.	0x0	R

Cable Diagnostics Results 1 Register

Address: 0xBA1E, Reset: 0x0000, Name: CDIAG_DTLD_RSLTS_1

This register provides cable diagnostics results for Pair 1.

Table 106. Bit Descriptions for CDIAG_DTLD_RSLTS_1

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	CDIAG_RSLT_1_BSY	When set, this bit indicates Pair 1 is busy. This bit indicates that there was unknown activity on Pair 1 during cable diagnostics.	0x0	R
9	CDIAG_RSLT_1_XSIM_3	When set, this bit indicates that there is a significant impedance cross pair short between Pair 1 and Pair 3.	0x0	R
8	CDIAG_RSLT_1_XSIM_2	When set, this bit indicates that there is a significant impedance cross pair short between Pair 1 and Pair 2.	0x0	R
7	CDIAG_RSLT_1_XSIM_0	When set, this bit indicates that there is a significant impedance cross pair short between Pair 1 and Pair 0.	0x0	R
6	CDIAG_RSLT_1_SIM	When set, this bit indicates that there is a significant impedance mismatch on Pair 1.	0x0	R
5	CDIAG_RSLT_1_XSHRT_3	When set, this bit indicates that there is a cross pair short between Pair 1 and Pair 3.	0x0	R
4	CDIAG_RSLT_1_XSHRT_2	When set, this bit indicates that there is a cross pair short between Pair 1 and Pair 2.	0x0	R
3	CDIAG_RSLT_1_XSHRT_0	When set, this bit indicates that there is a cross pair short between Pair 1 and Pair 0.	0x0	R
2	CDIAG_RSLT_1_SHRT	When set, this bit indicates that there is a short on Pair 1.	0x0	R
1	CDIAG_RSLT_1_OPN	When set, this bit indicates that there is an open on Pair 1.	0x0	R
0	CDIAG_RSLT_1_GD	When set, this bit indicates that Pair 1 is well terminated.	0x0	R

Cable Diagnostics Results 2 Register

Address: 0xBA1F, Reset: 0x0000, Name: CDIAG_DTLD_RSLTS_2

This register provides cable diagnostics results for Pair 2.

Table 107. Bit Descriptions for CDIAG_DTLD_RSLTS_2

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	CDIAG_RSLT_2_BSY	When set, this bit indicates that Pair 2 is busy. This bit indicates that there was unknown activity on Pair 2 during cable diagnostics.	0x0	R
9	CDIAG_RSLT_2_XSIM_3	When set, this bit indicates that there is a significant impedance cross pair short between Pair 2 and Pair 3.	0x0	R
8	CDIAG_RSLT_2_XSIM_1	When set, this bit indicates that there is a significant impedance cross pair short between Pair 2 and Pair 1.	0x0	R
7	CDIAG_RSLT_2_XSIM_0	When set, this bit indicates that there is a significant impedance cross pair short between Pair 2 and Pair 0.	0x0	R
6	CDIAG_RSLT_2_SIM	When set, this bit indicates that there is a significant impedance mismatch on Pair 2.	0x0	R
5	CDIAG_RSLT_2_XSHRT_3	When set, this bit indicates that there is a cross pair short between Pair 2 and Pair 3.	0x0	R
4	CDIAG_RSLT_2_XSHRT_1	When set, this bit indicates that there is a cross pair short between Pair 2 and Pair 1.	0x0	R
3	CDIAG_RSLT_2_XSHRT_0	When set, this bit indicates that there is a cross pair short between Pair 2 and Pair 0.	0x0	R
2	CDIAG_RSLT_2_SHRT	When set, this bit indicates that there is a short on Pair 2.	0x0	R
1	CDIAG_RSLT_2_OPN	When set, this bit indicates that there is an open on Pair 2.	0x0	R
0	CDIAG_RSLT_2_GD	When set, this bit indicates that Pair 2 is well terminated.	0x0	R

Cable Diagnostics Results 3 Register

Address: 0xBA20, Reset: 0x0000, Name: CDIAG_DTLD_RSLTS_3

This register provides cable diagnostics results for Pair 3.

Table 108. Bit Descriptions for CDIAG_DTLD_RSLTS_3

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	CDIAG_RSLT_3_BSY	When set, this bit indicates that Pair 3 is busy. This bit indicates that there was unknown activity on Pair 3 during cable diagnostics.	0x0	R
9	CDIAG_RSLT_3_XSIM_2	When set, this bit indicates that there is a significant impedance cross pair short between Pair 3 and Pair 2.	0x0	R
8	CDIAG_RSLT_3_XSIM_1	When set, this bit indicates that there is a significant impedance cross pair short between Pair 3 and Pair 1.	0x0	R
7	CDIAG_RSLT_3_XSIM_0	When set, this bit indicates that there is a significant impedance cross pair short between Pair 3 and Pair 0.	0x0	R
6	CDIAG_RSLT_3_SIM	When set, this bit indicates that there is a significant impedance mismatch on Pair 3.	0x0	R
5	CDIAG_RSLT_3_XSHRT_2	When set, this bit indicates that there is a cross pair short between Pair 3 and Pair 2.	0x0	R
4	CDIAG_RSLT_3_XSHRT_1	When set, this bit indicates that there is a cross pair short between Pair 3 and Pair 1.	0x0	R
3	CDIAG_RSLT_3_XSHRT_0	When set, this bit indicates that there is a cross pair short between Pair 3 and Pair 0.	0x0	R
2	CDIAG_RSLT_3_SHRT	When set, this bit indicates that there is a short on Pair 3.	0x0	R
1	CDIAG_RSLT_3_OPN	When set, this bit indicates that there is an open on Pair 3.	0x0	R
0	CDIAG_RSLT_3_GD	When set, this bit indicates that Pair 3 is well terminated.	0x0	R

Cable Diagnostics Fault Distance Pair 0 Register

Address: 0xBA21, Reset: 0x00FF, Name: CDIAG_FLT_DIST_0

This register provides the distance to the first fault on Pair 0.

Table 109. Bit Descriptions for CDIAG_FLT_DIST_0

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	CDIAG_FLT_DIST_0	This bit field provides the distance to the first fault on Pair 0 in meters. A value of 0xFF indicates an unknown result.	0xFF	R

Cable Diagnostics Fault Distance Pair 1 Register

Address: 0xBA22, Reset: 0x00FF, Name: CDIAG_FLT_DIST_1

This register provides the distance to the first fault on Pair 1.

Table 110. Bit Descriptions for CDIAG_FLT_DIST_1

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	CDIAG_FLT_DIST_1	This bit field provides the distance to the first fault on Pair 1 in meters. A value of 0xFF indicates an unknown result.	0xFF	R

Cable Diagnostics Fault Distance Pair 2 Register

Address: 0xBA23, Reset: 0x00FF, Name: CDIAG_FLT_DIST_2

This register provides the distance to the first fault on Pair 2.

Table 111. Bit Descriptions for CDIAG_FLT_DIST_2

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	CDIAG_FLT_DIST_2	This bit field provides the distance to the first fault on Pair 2 in meters. A value of 0xFF indicates an unknown result.	0xFF	R

Cable Diagnostics Fault Distance Pair 3 Register

Address: 0xBA24, Reset: 0x00FF, Name: CDIAG_FLT_DIST_3

This register provides the distance to the first fault on Pair 3.

Table 112. Bit Descriptions for CDIAG_FLT_DIST_3

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	CDIAG_FLT_DIST_3	This bit field provides the distance to the first fault on Pair 3 in meters. A value of 0xFF indicates an unknown result.	0xFF	R

Cable Diagnostics Cable Length Estimate Register

Address: 0xBA25, Reset: 0x00FF, Name: CDIAG_CBL_LEN_EST

This register provides an estimate of the cable length in meters based on the signal processing and is estimated during link establishment for 100BASE-TX and 1000BASE-T.

Table 113. Bit Descriptions for CDIAG_CBL_LEN_EST

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	CDIAG_CBL_LEN_EST	This bit field provides a cable length estimate in meters. A value of 0xFF indicates an unknown result.	0xFF	R

LED Pulse Stretching Duration Register

Address: 0xBC00, Reset: 0x0011, Name: LED_PUL_STR_DUR

When the LED_PUL_STR_DUR_SEL bit field in the LED_CTRL_1 register (Address 0x001B, Bits[3:2]) is set to 2'b11, the LED_PUL_STR_DUR register determines the LED pulse stretching duration.

Table 114. Bit Descriptions for LED_PUL_STR_DUR

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
[5:0]	LED_PUL_STR_DUR	When the LED_PUL_STR_DUR_SEL bit field in the LED_CTRL_1 register (Address 0x001B, Bits[3:2]) is set to 2'b11, the LED_PUL_STR_DUR bit field determines the LED pulse stretching duration. Multiply the value specified by 8 to determine the duration in milliseconds.	0x11	R/W

SUBSYSTEM REGISTER SUMMARY

The subsystem registers are accessible at Device Address 0x1E using Clause 45 access. For systems that do not support the interface specified under Clause 45, these registers can be accessed using Clause 22 access via Register 0x0010 and Register 0x0011.

The default value of some of the registers are determined by the value of the hardware configuration pins, which are read just after the RESET_N pin is deasserted (see the Hardware Configuration Pins section) so that the default operation of the ADIN1300 can be configured in unmanaged applications. The default values in the registers listed in Table 115 assume that the ADIN1300 is configured with autonegotiation enabled, all speeds advertised, and the ADIN1300 is not configured to enter software power-down after reset.

Table 115. Subsystem Register Summary

Address	Name	Description	Reset	Access
0xFF0C	GE_SFT_RST	Subsystem Software Reset Register.	0x0000	R/W
0xFF0D	GE_SFT_RST_CFG_EN	Subsystem Software Reset Configuration Enable Register.	0x0000	R/W
0xFF1F	GE_CLK_CFG	Subsystem Clock Configuration Register.	0x0000	R/W
0xFF23	GE_RGMII_CFG	Subsystem RGMII Configuration Register.	0x0E07	R/W
0xFF24	GE_RMII_CFG	Subsystem RMII Configuration Register.	0x0116	R/W
0xFF26	GE_PHY_BASE_CFG	Subsystem PHY Base Configuration Register.	0x0C86	R/W
0xFF3C	GE_LNK_STAT_INV_EN	Subsystem Link Status Invert Enable Register.	0x0000	R/W
0xFF3D	GE_IO_GP_CLK_OR_CNTRL	Subsystem GP_CLK Pin Override Control Register.	0x0000	R/W
0xFF3E	GE_IO_GP_OUT_OR_CNTRL	Subsystem LINK_ST Pin Override Control Register.	0x0000	R/W
0xFF3F	GE_IO_INT_N_OR_CNTRL	Subsystem INT_N Pin Override Control Register.	0x0000	R/W
0xFF41	GE_IO_LED_A_OR_CNTRL	Subsystem LED_0 Pin Override Control Register.	0x0000	R/W

SUBSYSTEM REGISTER DETAILS

Subsystem Software Reset Register

Address: 0xFF0C, Reset: 0x0000, Name: GE_SFT_RST

The soft reset register is used to reset the subsystem.

Table 116. Bit Descriptions for GE_SFT_RST

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	GE_SFT_RST	The subsystem can be reset by setting GE_SFT_RST to 1. The subsystem behavior depends on the setting of the GE_SFT_RST_CFG_EN register. When the GE_SFT_RST_CFG_EN bit is set, the subsystem requests a new set of hardware configuration pin settings from the chip during the software reset sequence. When GE_SFT_RST_CFG_EN is clear, the previously stored hardware configuration pin settings are reloaded into the corresponding management registers.	0x0	R/W

Subsystem Software Reset Configuration Enable Register

Address: 0xFF0D, Reset: 0x0000, Name: GE_SFT_RST_CFG_EN

In the event of a software reset using the GE_SFT_RST bit, the subsystem behavior depends on the setting of this register bit.

Table 117. Bit Descriptions for GE_SFT_RST_CFG_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	GE_SFT_RST_CFG_EN	In the event of a subsystem software reset using the GE_SFT_RST bit, the subsystem behavior depends on the setting of the GE_SFT_RST_CFG_EN bit. 1: when the GE_SFT_RST_CFG_EN bit is set, the subsystem requests a new set of hardware configuration pin settings from the chip during the software reset sequence. 0: when GE_SFT_RST_CFG_EN is clear, the previously stored hardware configuration pin settings are reloaded into the corresponding management registers.	0x0	R/W

Subsystem Clock Configuration Register

Address: 0xFF1F, Reset: 0x0000, Name: GE_CLK_CFG

This register allows the subsystem output clock configuration to be controlled.

Table 118. Bit Descriptions for GE_CLK_CFG

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
5	GE_CLK_RCVR_125_EN	When this bit is set, the125 MHz PHY recovered clock (or PLL clock) is driven at the GP_CLK pin.	0x0	R/W
4	GE_CLK_FREE_125_EN	When this bit is set, the 125 MHz PHY free running clock is driven at the GP_CLK pin.	0x0	R/W
3	GE_REF_CLK_EN	When this bit is set, the 25 MHz reference clock from the crystal oscillator is driven at the CLK25_REF pin. Note that when an external 50 MHz clock is driven at XTAL_I (for RMII), it is divided by 2, and the divided 25 MHz reference clock is driven at the CLK25_REF pin.	0x0	R/W
2	GE_CLK_HRT_RCVR_EN	The PHY provides a digital recovered heartbeat clock. This clock is sourced from either the 25 MHz reference clock or the 125 MHz recovered clock depending on the mode that the PHY is in and on the settings of certain registers. Setting GE_CLK_HRT_RCVR_EN causes the subsystem to request the chip to drive the digital recovered heartbeat clock at the GP_CLK pin.	0x0	R/W
1	GE_CLK_HRT_FREE_EN	The PHY provides a digital free running heartbeat clock. This clock is sourced either from the 25 MHz reference clock or the 125 MHz free running clock depending on the mode that the PHY is in and on the settings of certain registers. Setting GE_CLK_HRT_FREE_EN causes the subsystem to request the chip to drive the digital free running heartbeat clock at the GP_CLK pin.	0x0	R/W
0	GE_CLK_25_EN	When this bit is set, the 25 MHz reference clock from the crystal oscillator is driven at the GP_CLK pin (having been processed through the digital block, and is not as clean as the equivalent clock available at the CLK25_REF pin).	0x0	R/W

Subsystem RGMII Configuration Register

Address: 0xFF23, Reset: 0x0E07, Name: GE_RGMII_CFG

This register allows the MAC interface RGMII configuration to be controlled.

Table 119. Bit Descriptions for GE_RGMII_CFG

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x1	R
10	GE_RGMII_100_LOW_LTNCY_EN	Enable/Disable Low RGMII Latency for 100BASE-TX. 1: enable low RGMII latency for 100BASE-TX. 0: disable low RGMII latency for 100BASE-TX.	0x1	R/W
9	GE_RGMII_10_LOW_LTNCY_EN	Enable/Disable Low RGMII Latency for 10BASE-T. 1: enable low RGMII latency for 10BASE-T. 0: disable low RGMII latency for 10BASE-T.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
[8:6]	GE_RGMII_RX_SEL	This field allows the RGMII receive clock delay to be specified in terms of the data link layer (DLL) unit delay (t_U = 200 ps). 111: 10 × t_U + 400 ps. 110: 9 × t_U + 400 ps. 101: reserved. 100: reserved. 011: reserved. 010: 7 × t_U + 400 ps. 001: 6 × t_U + 400 ps. 000: 8 × t_U + 400 ps.	0x0	R/W
[5:3]	GE_RGMII_GTX_SEL	This field allows the RGMII transmit clock delay to be specified in terms of the DLL unit delay (t_U = 200 ps). 111: 10 × t_U + 400 ps. 110: 9 × t_U + 400 ps. 101: reserved. 100: reserved. 011: reserved. 010: 7 × t_U + 400 ps. 001: 6 × t_U + 400 ps. 000: 8 × t_U + 400 ps.	0x0	R/W
2	GE_RGMII_RX_ID_EN	Enable/disable receive clock internal 2 ns delay in RGMII mode. Note that the default value of this bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 1: enable receive clock internal 2 ns delay in RGMII mode. 0: disable receive clock internal 2 ns delay in RGMII mode.	0x1	R/W
1	GE_RGMII_TX_ID_EN	Enable/disable transmit clock internal 2 ns delay in RGMII mode. Note that the default value of this bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 1: enable transmit clock internal 2 ns delay in RGMII mode. 0: disable transmit clock internal 2 ns delay in RGMII mode.	0x1	R/W
0	GE_RGMII_EN	This bit selects the RGMII MAC interface mode. Note that the default value of this bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications.	0x1	R/W

Subsystem RMII Configuration Register

Address: 0xFF24, Reset: 0x0116, Name: GE_RMII_CFG

This register allows the MAC interface RMII configuration to be controlled.

Table 120. Bit Descriptions for GE_RMII_CFG

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x1	R
7	GE_RMII_FIFO_RST	This bit allows the RMII FIFO to be reset.	0x0	R/W
[6:4]	GE_RMII_FIFO_DPTH	This field allows the RMII receive FIFO depth to be selected. 111: reserved. 110: reserved. 101: ± 24 bits. 100: ± 20 bits. 011: ± 16 bits. 010: ± 12 bits. 001: ± 8 bits. 000: ± 4 bits.	0x1	R/W

Bits	Bit Name	Description	Reset	Access
3	GE_RMII_TXD_CHK_EN	This bit determines whether or not the TXD_0 pin and TXD_1 pin are monitored to detect the start of a frame. This bit allows connecting the RMII receive CRS_DV to the RMII TX_EN signal. This allows a receive to transmit RMII pin loopback for media converter applications. This is something that it is not supported in the RMII specification.	0x0	R/W
2	GE_RMII_CRS_EN	This bit determines whether or not CRS is encoded in the CRS_DV output signal. This allows a receive to transmit RMII pin loopback for media converter applications. This is something that it is not supported in the RMII specification.	0x1	R/W
1	GE_RMII_BAD_SSD_RX_ER_EN	This bit determines whether or not the RX_ER output signal is asserted when a false carrier (bad SSD) is detected. When cleared, RX_ER is only asserted in case of a symbol error during a frame.	0x1	R/W
0	GE_RMII_EN	This bit selects the RMII MAC interface mode. Note that the default value of this register bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. As RMII mode requires a 50 MHz reference clock, the RMII interface must be configured from the hardware configuration pins and not from software.	0x0	R/W

Subsystem PHY Base Configuration Register

Address: 0xFF26, Reset: 0x0C86, Name: GE_PHY_BASE_CFG

This subsystem register allows the enhanced link detection function of the PHY to be configured for 100BASE-TX and for 1000BASE-T, and allows 1000BASE-T retrain to be configured. Each time a PHY core software reset is issued, the PHY resets its registers, including the 1000BASE-T retrain enable register bit (B_1000_RTRN_EN bit, Address 0x1E.0xA001, Bit 0) and the enhanced link detection 1000BASE-T and 100BASE-TX enable register bits (within the FLD_EN register, Address 0x1E.0x8E27). The default value of the B_1000_RTRN_EN bit is set via the 1000BASE-T retrain enable configuration bit (GE_RTRN_EN_CFG, within this register). The default value of the enhanced link detection 1000BASE-T enable register bits (within the FLD_EN register) are set via the GE_FLD_1000_EN_CFG bit and GE_FLD_100_EN_CFG bit within this register. If the value of any of these enable configuration bits are changed, the corresponding 1000BASE-T retrain enable register bit and the enhanced link detection 1000BASE-T and 100BASE-TX enable register bits in the PHY only change after a PHY software reset.

Table 121. Bit Descriptions for GE_PHY_BASE_CFG

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
12	GE_RTRN_EN_CFG	When this bit is set, the IEEE Standard 802.3 1000BASE-T retrain functionality is enabled in the PHY.	0x0	R/W
11	GE_FLD_1000_EN_CFG	When this bit is set, the enhanced link detection functionality is enabled when the PHY establishes a 1000BASE-T link.	0x1	R/W
10	GE_FLD_100_EN_CFG	When this bit is set, the enhanced link detection functionality is enabled when the PHY establishes a 100BASE-TX link.	0x1	R/W
[9:4]	RESERVED	Reserved.	0x8	R/W
3	GE_PHY_SFT_PD_CFG	When this bit is set, the PHY enters software power-down on exit from reset.	0x0	R/W
[2:0]	RESERVED	Reserved.	0x6	R/W

Subsystem Link Status Invert Enable Register

Address: 0xFF3C, Reset: 0x0000, Name: GE_LNK_STAT_INV_EN

This register allows the link status output signal on the LINK_ST pin to be inverted, meaning that link up is indicated by setting LINK_ST low.

Table 122. Bit Descriptions for GE_LNK_STAT_INV_EN

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	GE_LNK_STAT_INV_EN	When set to 1, this bit enables the link status output signal on the LINK_ST pin to be inverted, meaning that link up is indicated by setting LINK_ST low.	0x0	R/W

Subsystem GP_CLK Pin Override Control Register

Address: 0xFF3D, Reset: 0x0000, Name: GE_IO_GP_CLK_OR_CNTRL

This register allows the default function of the GP_CLK pin to be overridden.

Table 123. Bit Descriptions for GE_IO_GP_CLK_OR_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
[2:0]	GE_IO_GP_CLK_OR_CNTRL	This bit field allows the default function of the GP_CLK pin to be overridden. 111: PHY clock selected by the registers in the GE_CLK_CFG register. 110: RX_ER. 101: COL. 100: CRS. 011: receive start of packet indication. 010: transmit start of packet indication. 001: link status. 000: default function. The default function is RX_ER when the PHY is configured for MII or RMII MAC interface. In all other cases, the default function is GP_CLK.	0x0	R/W

Subsystem LINK_ST Pin Override Control Register

Address: 0xFF3E, Reset: 0x0000, Name: GE_IO_GP_OUT_OR_CNTRL

This register allows the default function of the LINK_ST pin to be overridden.

Table 124. Bit Descriptions for GE_IO_GP_OUT_OR_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
[2:0]	GE_IO_GP_OUT_OR_CNTRL	This bit field allows the default function of the LINK_ST pin to be overridden. 111: link status. 110: reserved. 101: COL. 100: CRS. 011: receive start of packet indication. 010: transmit start of packet indication. 001: link status. 000: default function, link status.	0x0	R/W

Subsystem INT_N Pin Override Control Register

Address: 0xFF3F, Reset: 0x0000, Name: GE_IO_INT_N_OR_CNTRL

This register allows the default function of the INT_N pin to be overridden.

Table 125. Bit Descriptions for GE_IO_INT_N_OR_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
[2:0]	GE_IO_INT_N_OR_CNTRL	This bit field allows the default function of the INT_N pin to be overridden. 111: INT_N. 110: TX_ER. 101: COL. 100: CRS. 011: receive start of packet indication. 010: transmit start of packet indication. 001: link status. 000: default function, INT_N. The default function when configured for MII MAC interface with EEE advertisement disabled from hardware pin configuration is CRS. In all other cases, the pin function is INT_N.	0x0	R/W

Subsystem LED_0 Pin Override Control Register

Address: 0xFF41, Reset: 0x0000, Name: GE_IO_LED_A_OR_CNTRL

This register allows the default function of the LED_0 pin to be overridden.

Table 126. Bit Descriptions for GE_IO_LED_A_OR_CNTRL

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:0]	GE_IO_LED_A_OR_CNTRL	This bit field allows the default function of the LED_0 pin to be overridden. 1111: LED_0. 1110: LED_0. 1101: LED_0. 1100: LED_0. 1011: LED_0. 1010: LED_0. 1001: reserved. 1000: reserved. 0111: LED_0. 0110: TX_ER. 0101: COL. 0100: CRS. 0011: receive start of packet indication. 0010: transmit start of packet indication. 0001: link status. 0000: default function, LED_0. When configured for MII MAC interface with EEE advertisement disabled from the hardware configuration pins, the default function is COL. When configured for MII MAC interface with EEE advertisement enabled from the hardware pin configuration, the default function is TX_ER. In all other cases, the default is LED_0.	0x0	R/W

PCB LAYOUT RECOMMENDATIONS

This is an overview of the key areas of interest during placement and layout of the PHY and corresponding support components. Take care when routing high speed interface signals to maximize signal performance and ensure optimum EMC performance, with a view to ensure critical signal traces are kept as short as possible to minimize noise coupling.

PHY PACKAGE LAYOUT

The LFCSP has an exposed pad underneath the package that must be soldered to the PCB ground for mechanical and thermal reasons. For thermal impedance performance and to maximize heat removal, use of a 4 × 4 array of thermal vias beneath the exposed ground pad is recommended.

There are also two keep out areas on the top and bottom of the exposed pad. The PCB land pattern must incorporate the exposed ground paddle with vias and these two keep out areas in the footprint. No PCB traces or vias can be used in either of the keep out areas. The EVAL-ADIN1300FMCZ uses an array of 4 × 4 vias on a 0.75 mm grid arrangement, as shown in Figure 39. The via pad diameter dimension is 0.02 in. (0.5015 mm) and the finished drill hole diameter is 0.01 in. (0.2489 mm).

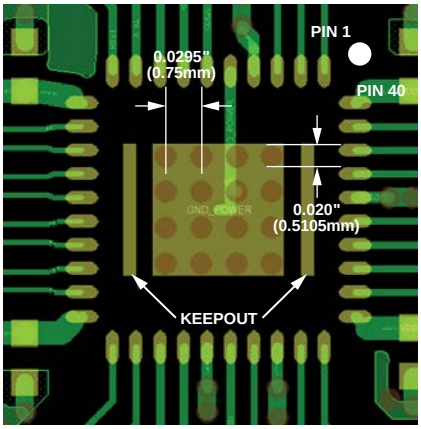


Figure 39. Exposed Paddle Via Array on EVAL-ADIN1300FMCZ

COMPONENT PLACEMENT

Prioritization of the critical traces and components helps simplify the routing exercise. Place and orient the critical traces and components first to ensure an effective layout with minimal turns, vias, and crossing traces. For an Ethernet PHY layout, the important components are the crystal and load capacitors, the transformer on the MDI lines, and all bypass capacitors local to the device. Prioritize these components and the routing to them. Keep the PHY chip at least 1 in. away from the edge of the board. The following sections provide more detail for each of the areas.

Crystal Placement and Routing

To ensure minimum current consumption and to minimize stray capacitances, make connections between the crystal, capacitors, and ground as close to the ADIN1300 as possible.

Magnetics Placement

Orient the magnetics and RJ45 in line with the MDI_x_x pins from the PHY chip.

MDI, DIFFERENTIAL PAIR ROUTING

The MDI interface runs from the ADIN1300 PHY to the transformer, and from there to the RJ45 connector. Traces running from the MDI_x_x pins of the ADIN1300 to the magnetics must be on the same side of the board, kept as short as possible (ideally less than 1 in. in length), and individual trace impedance of these tracks kept below 50 Ω, with differential impedance of 100 Ω for each pair. The same recommendations apply for traces running from the magnetics to the RJ45 connector. Keep impedances constant throughout because any discontinuities may affect signal integrity.

Each pair must be routed together, trace widths kept the same throughout, trace lengths kept equal where possible, and avoid any right angles on these traces (use curves in traces or 45° angles). Avoid stubs on all signal traces. Where possible, route traces on the same layer.

Route traces over a continuous reference plane with no interruptions to reduce inductance.

Where possible, ensure a solid return path underneath all signal traces. Avoid routing signal traces across plane splits.

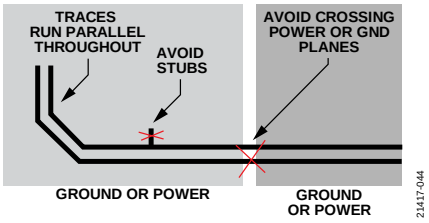


Figure 40. Things to Avoid when Routing Differential Pairs

MAC INTERFACE PINS

Keep trace lengths as short as possible. Route traces with an impedance of 50 Ω to ground.

POWER AND GROUND PLANES

From a PCB layout point of view, it is important to place the decoupling capacitors as close as possible to the power and GND pins to minimize the inductance.

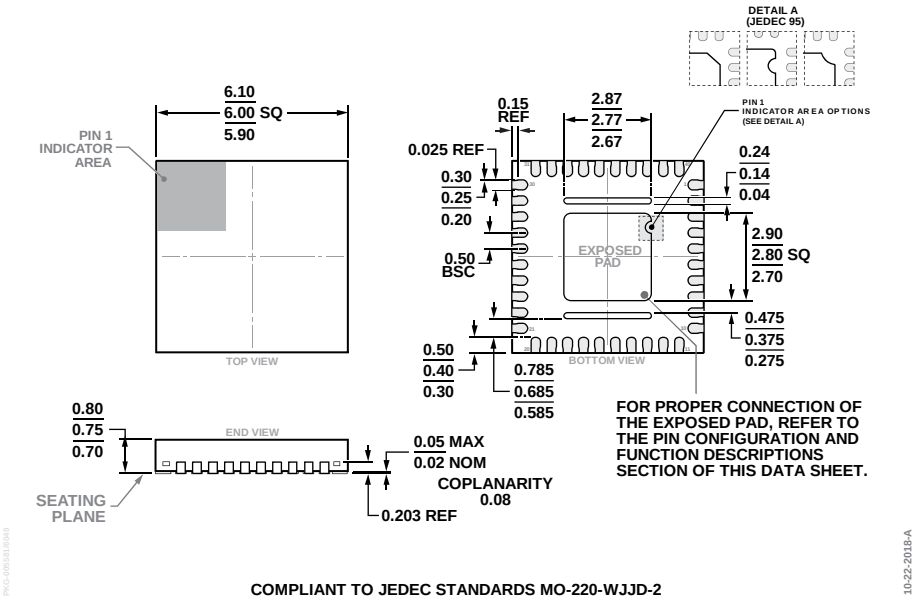
Magnetics Module Grounding

A split ground plane under the transformer minimizes noise coupling across the transformer and between adjacent coils within. Ensure a physical separation of the ground planes underneath the transformer. Make the width of this separation at least 100 mil.

RJ45 Module Grounding

For optimal EMC performance, it is recommended to use a metal shielded RJ45 connector with the shield connected to chassis ground. There must be an isolation gap between the chassis ground and the PHY IC ground with consistent isolation across all layers.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD-2

Figure 41. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.75 mm Package Height
(CP-40-26)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADIN1300CCPZ	−40°C to +105°C	40-Lead LFCSP	CP-40-26
ADIN1300CCPZ-R7	−40°C to +105°C	40-Lead LFCSP	CP-40-26
ADIN1300BCPZ	−40°C to +85°C	40-Lead LFCSP	CP-40-26
ADIN1300BCPZ-R7	−40°C to +85°C	40-Lead LFCSP	CP-40-26
EVAL-ADIN1300FMCZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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