

## FEATURES

- Digitally controlled VGA
- 2 dB to 32 dB gain range
- 1 dB gain step size
- 100  $\Omega$  differential input resistance
- 10  $\Omega$  differential output resistance
- Noise figure: 5.1 dB at 300 MHz, 5 V supply, and maximum gain
- OIP3 at maximum gain
  - 39.4 dBm at 300 MHz at 5 V supply
  - 38.1 dBm at 700 MHz at 5 V supply
- Gain step accuracy:  $\pm 0.2$  dB
- 3 dB bandwidth at 32 dB: 1.0 GHz typical at 5 V supply
- Multiple control interface options
  - Parallel 5-bit control interface with latch
  - 3- and 4-wire SPI with fast attack
  - Gain step-up and step-down interface
- Wide input dynamic range
- Power-down control
- Single 3.3 V or 5 V supply operation
- 112 mA quiescent current at 5 V supply
- 20-lead, 4 mm  $\times$  4 mm LFCSP

## APPLICATIONS

- Differential ADC drivers
- High intermediate frequency (IF) sampling receivers
- High output power IF amplification
- DOCSIS Fdx upstream amplifier
- Instrumentation

## GENERAL DESCRIPTION

The ADL5206 is a wide bandwidth, variable gain amplifier (VGA) with digital control (also known as a digital gain amplifier (DGA)) that provides precise gain control, high output third-order intercept (OIP3), and low noise figure over the entire gain range. The excellent OIP3 performance of 39.4 dBm (at 300 MHz, 5 V supply, and maximum gain) makes the ADL5206 an excellent gain control device for a variety of receiver applications.

For wide input dynamic range applications, the ADL5206 provides a broad 2 dB to 32 dB gain range with a 1 dB step size. The gain is adjustable through multiple gain control and interface options: parallel, serial peripheral interface (SPI), or gain step-up and step-down controls.

The ADL5206 can be powered up independently by applying the appropriate logic level to the PWUP pin. The quiescent

## FUNCTIONAL BLOCK DIAGRAM

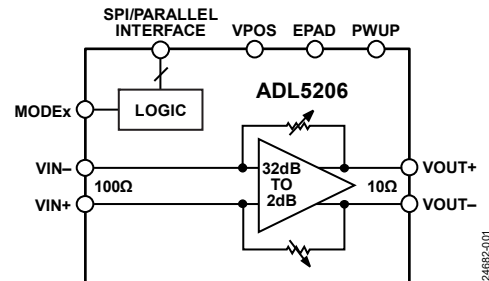


Figure 1.

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current of the ADL5206 is typically 112 mA with a 5 V supply. When disabled, the ADL5206 consumes only 8 mA and offers excellent input to output isolation. The gain setting is preserved when the device is disabled.

Fabricated on the Analog Devices, Inc., high speed, silicon germanium (SiGe), bipolar complementary metal-oxide semiconductor (BiCMOS) process, the ADL5206 provides precise gain adjustment capabilities with good distortion performance. The ADL5206 amplifier comes in a compact, thermally enhanced, 4 mm  $\times$  4 mm, 20-lead LFCSP and operates over the temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

Note that throughout this data sheet, multifunction pins, such as CS/GS1/D3, are referred to by the entire pin name or by a single function of the pin.

Rev. 0

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## REVISION HISTORY

9/2020—Revision 0: Initial Version

## SPECIFICATIONS

$T_A = 25^\circ\text{C}$ , load impedance ( $Z_{\text{LOAD}}$ ) = 100  $\Omega$ , maximum gain (gain code = 00000), frequency = 300 MHz, and 2 V p-p differential output, unless otherwise noted.

Table 1.

Parameter <sup>2</sup>	Test Conditions/Comments	3.3 V Supply <sup>1</sup>			5 V Supply <sup>1</sup>			Unit
		Min	Typ	Max	Min	Typ	Max	
<b>DYNAMIC PERFORMANCE</b>								
–3 dB Bandwidth	At 20 dB		1.7		1.6			GHz
	At 25 dB		1.4		1.3			GHz
	At 32 dB		1.2		1.0			GHz
Slew Rate			4.3		4.3			V/ns
<b>INPUT STAGE</b>								
Maximum Input Swing <sup>3</sup>	VIN+ and VIN– pins Gain code = 11111		4		6.2			V p-p
Differential Input Resistance			100		100			$\Omega$
Input Common-Mode Voltage			1.65		2.5			V
Common-Mode Rejection Ratio (CMRR)			56		56			dB
<b>GAIN</b>								
Voltage Gain Range			30		30			dB
Maximum Gain	Gain code = 00000		32		32			dB
Minimum Gain	Gain code = 11110 to 11111		2		2			dB
Gain Step Size			1		1			dB
Gain Step Accuracy			$\pm 0.2$		$\pm 0.2$			dB
Gain Flatness	From 30 MHz to 700 MHz		0.2		0.2			dB p-p
Gain Temperature Sensitivity	Gain code = 00000 and at 700 MHz		3		4			mdB/ $^\circ\text{C}$
Fast Attack Step Response Delay	For input voltage ( $V_{\text{IN}}$ ) = 0.1 V, FA changing from 0 to 1 with 16 dB step		5		5			ns
<b>COMMON-MODE INPUTS</b>								
VCM Pin Input Resistance			2.6		2.6			k $\Omega$
<b>OUTPUT STAGE</b>								
Output Voltage Swing	VOUT+ and VOUT– pins At 1 dB compression point (P1dB), gain code = 00000		4.1		6.25			V p-p
Common-Mode Voltage Reference	VCM pin	1.2	1.65	1.8	1.4	2.5	2.7	V
Output Common-Mode Offset	$((V_{\text{OUT}+}) + (V_{\text{OUT}-}))/2 - V_{\text{CM}}/2$	–10		+10	–10		+10	mV
Differential Output Resistance			10		10			$\Omega$
Short-Circuit Current			20		25			mA
<b>NOISE AND HARMONIC PERFORMANCE</b>								
10 MHz								
Noise Figure			6.2		6.3			dB
Second Harmonic Distortion (HD2)	$V_{\text{OUT}} = 2 \text{ V p-p}$		–85		–89.2			dBc
Third Harmonic Distortion (HD3)	$V_{\text{OUT}} = 2 \text{ V p-p}$		–76.5		–85.6			dBc
Output Second-Order Intercept (OIP2)	$V_{\text{OUT}} = 2 \text{ V p-p composite}$		84.3		87.1			dBm
Third Intermodulation Distortion (IMD3)	$V_{\text{OUT}} = 2 \text{ V p-p composite}$		–78.9		–85.8			dBc
Output Third-Order Intercept (OIP3)	$V_{\text{OUT}} = 2 \text{ V p-p composite}$		39.4		42.9			dBm

Parameter <sup>2</sup>	Test Conditions/Comments	3.3 V Supply <sup>1</sup>			5 V Supply <sup>1</sup>			Unit
		Min	Typ	Max	Min	Typ	Max	
100 MHz								
Noise Figure			5.8			5.9		dB
HD2	$V_{OUT} = 2\text{ V p-p}$		-75.8			-78.4		dBc
HD3	$V_{OUT} = 2\text{ V p-p}$		-72.2			-81		dBc
OIP2	$V_{OUT} = 2\text{ V p-p composite}$		74.7			76.8		dBm
IMD3	$V_{OUT} = 2\text{ V p-p composite}$		-77			-84.8		dBc
OIP3	$V_{OUT} = 2\text{ V p-p composite}$		38.5			42.4		dBm
300 MHz								
Noise Figure			4.6			5.1		dB
HD2	$V_{OUT} = 2\text{ V p-p}$		-67.8			-77.6		dBc
HD3	$V_{OUT} = 2\text{ V p-p}$		-56.2			-67.9		dBc
OIP2	$V_{OUT} = 2\text{ V p-p composite}$		70.5			79.5		dBm
IMD3	$V_{OUT} = 2\text{ V p-p composite}$		-75			-78.8		dBc
OIP3	$V_{OUT} = 2\text{ V p-p composite}$		37.5			39.4		dBm
500 MHz								
Noise Figure			4.5			5		dB
HD2	$V_{OUT} = 2\text{ V p-p}$		-58.7			-65.6		dBc
HD3	$V_{OUT} = 2\text{ V p-p}$		-52.6			-66.2		dBc
OIP2	$V_{OUT} = 2\text{ V p-p composite}$		58.3			65.7		dBm
IMD3	$V_{OUT} = 2\text{ V p-p composite}$		-68.3			-76.6		dBc
OIP3	$V_{OUT} = 2\text{ V p-p composite}$		34			38.3		dBm
OP1dB			14.3			18		dBm
700 MHz								
Noise Figure			6.7			7		dB
HD2	$V_{OUT} = 2\text{ V p-p}$		-62.7			-69		dBc
HD3	$V_{OUT} = 2\text{ V p-p}$		-55.4			-77.7		dBc
OIP2	$V_{OUT} = 2\text{ V p-p composite}$		64.2			67.2		dBm
IMD3	$V_{OUT} = 2\text{ V p-p composite}$		-61.2			-76.3		dBc
OIP3	$V_{OUT} = 2\text{ V p-p composite}$		30.6			38.1		dBm
1000 MHz								
Noise Figure			7.5			7.9		dB
HD2	$V_{OUT} = 2\text{ V p-p}$		-60.3			-62.5		dBc
HD3	$V_{OUT} = 2\text{ V p-p}$		-49			-61		dBc
OIP2	$V_{OUT} = 2\text{ V p-p composite}$		61.6			63.3		dBm
IMD3	$V_{OUT} = 2\text{ V p-p composite}$		-56.5			-69.1		dBc
OIP3	$V_{OUT} = 2\text{ V p-p composite}$		28.2			34.5		dBm
1200 MHz								
Noise Figure			6.6			7		dB
HD2	$V_{OUT} = 2\text{ V p-p}$		-53.4			-57.2		dBc
HD3	$V_{OUT} = 2\text{ V p-p}$		-44			-52		dBc
OIP2	$V_{OUT} = 2\text{ V p-p composite}$		53.6			57.5		dBm
IMD3	$V_{OUT} = 2\text{ V p-p composite}$		-54.4			-66.9		dBc
OIP3	$V_{OUT} = 2\text{ V p-p composite}$		27.2			33.4		dBm

Parameter <sup>2</sup>	Test Conditions/Comments	3.3 V Supply <sup>1</sup>			5 V Supply <sup>1</sup>			Unit
		Min	Typ	Max	Min	Typ	Max	
DIGITAL INTERFACE								
Input Voltage	MODE1, MODE0, PWUP, LATCH, and SDIO pins							
Logic High ( $V_{IH}$ )		2		VPOS	2		3.3	V
Logic Low ( $V_{IL}$ )		0		1.0	0		1.0	V
Input Leakage Current	Digital $V_{IN} = 0\text{ V to }3.3\text{ V}$		$\pm 3$			$\pm 3$		$\mu\text{A}$
Output Voltage	SDIO pin							
Logic High ( $V_{OH}$ )	Output high current ( $I_{OH}$ ) = -2 mA	2.4			2.4			2.4
Logic Low ( $V_{OL}$ )	Output low current ( $I_{OL}$ ) = 2 mA			0.5			0.5	
POWER INTERFACE								
Supply Voltage ( $V_{POS}$ )	VPOS pin	3.15	3.3	3.45	4.75	5	5.25	V
Quiescent Current			87			112		mA
Power-Down Current	PWUP pin = low		8			8		mA

<sup>1</sup> The 3.3 V supply is low power mode, and the 5 V supply is high performance mode.

<sup>2</sup> When referring to a single function of a multifunction pin in the specifications table, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

<sup>3</sup> The maximum input swing of 6.2 V p-p is for the lowest gain setting of 2 dB. As the gain setting increases, the maximum input swing must be reduced correspondingly to maintain the same maximum output swing. The maximum output swing is based on P1dB.

TIMING SPECIFICATIONS

Table 2. SPI Timing Parameters

Parameter	Description	Min	Typ	Max	Unit
$f_{SCLK}$	Maximum serial clock rate, $1/t_{SCLK}$ ( $t_{SCLK}$ is the SCLK time)		25		MHz
$t_{PWH}$	Minimum period that SCLK is in a logic high state		10		ns
$t_{PWL}$	Minimum period that SCLK is in a logic low state		10		ns
$t_{DS}$	Setup time between the data and the rising edge of SCLK		5		ns
$t_{DH}$	Hold time between the data and the rising edge of SCLK		5		ns
$t_{DCS}$	Setup time between the falling edge of $\overline{CS}$ and the rising edge of SCLK		10		ns
$t_H$	Hold time between the rising edge of $\overline{CS}$ and the last falling edge of SCLK		10		ns
$t_{DV}$	Maximum time delay between the falling edge of SCLK and the output data valid for a read operation		5	14	ns
$t_z$	Maximum time delay between $\overline{CS}$ deactivation and the SDIO bus return to high impedance			12	ns

Timing Diagrams

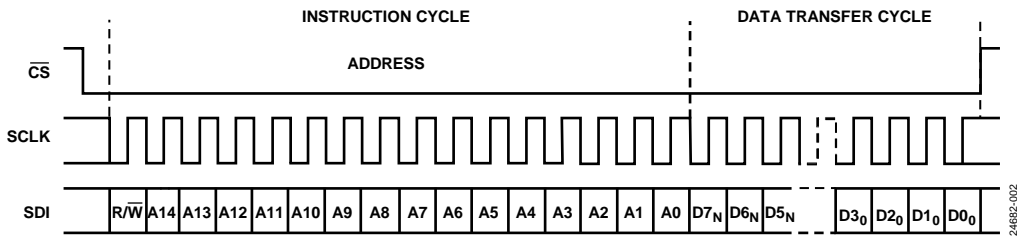


Figure 2. SPI Register Timing, MSB First

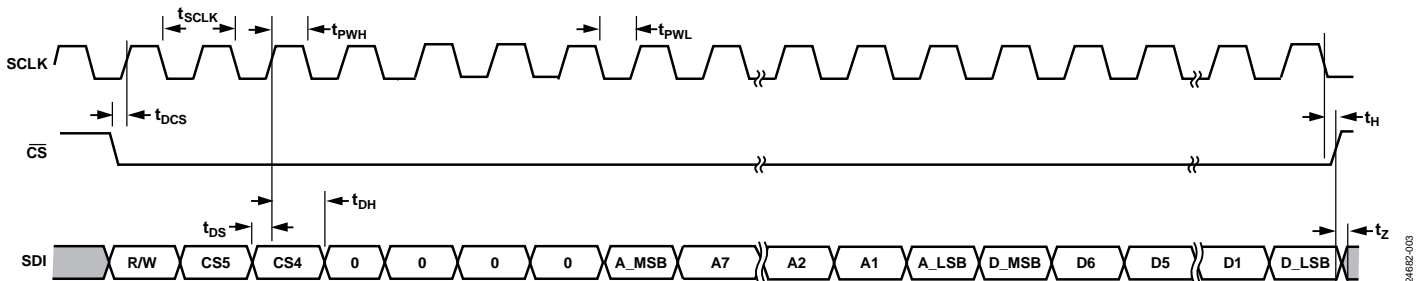


Figure 3. Timing Diagram for the SPI Register Write

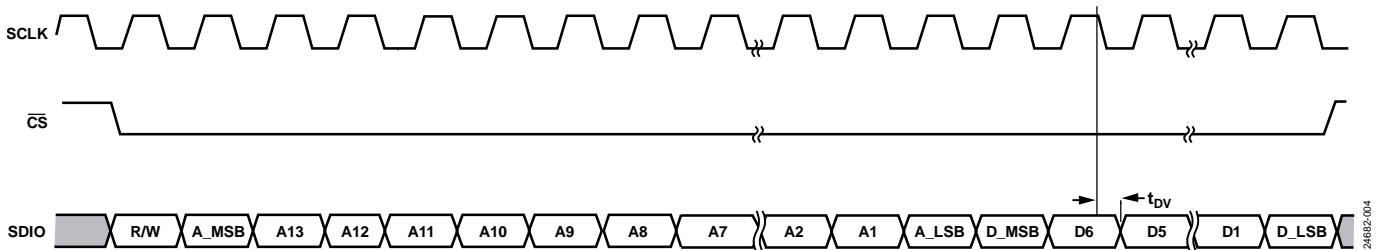


Figure 4. Timing Diagram for SPI Register Read

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter <sup>1</sup>	Rating
Differential Output Voltage Swing × Bandwidth Product	
5 V Supply Voltage	4 V-GHz
3.3 V Supply Voltage	3 V-GHz
Supply Voltage, $V_{POS}$	5.4 V
PWUP, D0 to D4, MODE0, MODE1, LATCH	–0.5 V to +3.6 V
Input Voltage (VIN+ and VIN–)	–0.5 V to +3.1 V
Differential Input Voltage <sup>2</sup> ((VIN+) – (VIN–))	±1 V
Internal Power Dissipation ( $P_{DISS}$ )	500 mW
Temperature	
Maximum Junction	135°C
Operating Range	–40°C to +85°C
Storage Range	–65°C to +150°C

<sup>1</sup> When referring to a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

<sup>2</sup> The differential input voltage limit is significantly lower than the maximum input swing of 6.2 V p-p with a 5 V supply. The maximum input swing is for the lowest gain setting of 2 dB. As the gain setting increases, the maximum input swing must be reduced correspondingly to maintain the same maximum output swing. The maximum output swing is based on P1dB.

Stresses at or above those listed under absolute maximum ratings can cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 4 shows the thermal resistance from the die to ambient ( $\theta_{JA}$ ), die to board ( $\theta_{JB}$ ), and die to lead ( $\theta_{JC}$ ).

Table 4. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JB}$	$\theta_{JC}$	Unit
CP-20-16	55.42	16.01	9.08	°C/W

### JUNCTION TO BOARD THERMAL IMPEDANCE

The junction thermal, die to board, impedance ( $\theta_{JB}$ ) is the thermal impedance from the die to the leads of the ADL5206. The value given in Table 4 is based on the standard PCB described in the JESD51-7 standard for thermal testing of surface-mount components. PCB size and complexity (number of layers) affect  $\theta_{JB}$ , and more layers tend to reduce thermal impedance slightly.

If the PCB temperature ( $T_B$ ) is known, use the junction to board thermal impedance to calculate the die temperature (also known as the junction temperature,  $T_J$ ) to ensure that the die temperature does not exceed the specified limit of 135°C. For example, if the PCB temperature is 85°C, the die temperature is given by

$$T_J = T_B + (P_{DISS} \times \theta_{JB})$$

The worst case  $P_{DISS}$  for the ADL5206 is 500 mW (5.0 V × 110 mA, see Table 3). Therefore,  $T_J$  is

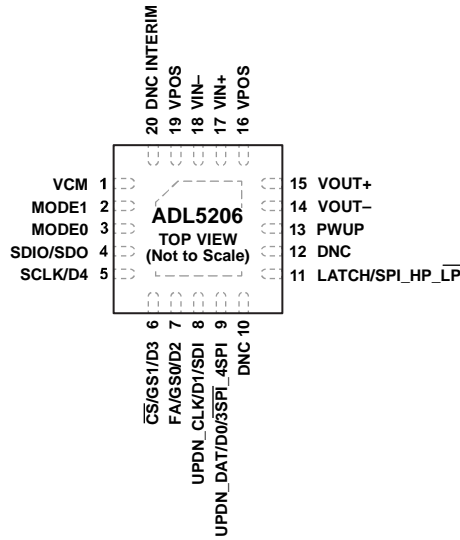
$$T_J = 85^\circ\text{C} + (0.499 \text{ W} \times 24.4^\circ\text{C/W}) = 97.2^\circ\text{C}$$

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THESE PINS.
  2. EXPOSED PAD GROUND. THE EXPOSED PAD MUST BE CONNECTED TO A LOW IMPEDANCE GROUND PLANE.

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Figure 5. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCM	Common-Mode Output.
2	MODE1	The MSB for Mode Control. Use both the MODE0 and MODE1 pins to select high performance or to select low power parallel, SPI, or up and down interface mode.
3	MODE0	The LSB for Mode Control. Use both the MODE1 and MODE0 pins to select parallel, SPI, or UPDN mode.
4	SDIO/SDO	Serial Data Input and Output in 3-Wire SPI Mode (SDIO). Serial data output in 4-wire SPI mode (SDO).
5	SCLK/D4	Serial Clock Input/Digital Bit 4. Depending on the selection of the MODE0 and MODE1 pins, this pin has two functions. In serial or SPI mode, this pin functions as SCLK. In parallel mode, this pin represents D4 when in the parallel gain control interface.
6	$\overline{CS}/GS1/D3$	Chip Select (Active Low)/Gain Step 1/Digital Bit 3. Depending on the selection of the MODE0 and MODE1 pins, this pin has three functions. In serial or SPI mode, this pin becomes $\overline{CS}$ . When in UPDN mode, the GS1 function is enabled for this pin, which controls the MSB gain step size. In parallel mode, this pin represents D3 when in the parallel gain control interface.
7	FA/GS0/D2	Fast Attack/Gain Step 0/Digital Bit 2. Depending on the selection of the MODE0 and MODE1 pins, this pin has three functions. In serial or SPI mode, the FA function of this pin is enabled. The FA function allows the user to define a larger attenuation jump in the digital gain control settings. The FA pin attenuates according to an FA SPI word definition of FA0 and FA1 (the attenuation step size bits), which is defined by the user. When in UPDN mode, the GS0 function is enabled for this pin which controls the LSB gain step size. In parallel mode, this pin represents D2 when in the parallel gain control interface.
8	UPDN_CLK/D1/SDI	Clock Interface for Up and Down Interface (UPDN_CLK). Depending on MODE0 and MODE1 selection, this pin has three functions. In the up and down interface mode, this pin becomes UPDN_CLK. In parallel mode, this pin represents Digital Bit 1 (D1) when using a parallel gain control interface. In 4-wire SPI mode, this pin is the serial data input (SDI).
9	UPDN_DAT/D0/ $\overline{3SPI\_4SPI}$	Data Interface for Up and Down Interface (UPDN_DAT). Depending on MODE0 and MODE1 selection, this pin has three functions. In up and down interface mode, this pin becomes UPDN_DAT. In parallel mode, this pin represents Digital Bit 0 (D0) when using a parallel gain control interface. In SPI mode, logic low selects 3-wire SPI and logic high selects 4-wire SPI ( $\overline{3SPI\_4SPI}$ ).
10, 12	DNC	Do Not Connect. Do not connect to these pins.



Pin No.	Mnemonic	Description
11	LATCH/SPI_HP_LP	The latch when the MODE0 and MODE1 pins are in parallel mode (LATCH). A logic low on this pin allows the gain to change, and a logic high on this pin prevents the gain change. In SPI mode, logic high selects high performance mode, and logic low selects low power mode (SPI_HP_LP).
13	PWUP	Power-Up. PWUP remains the power-up pin function with any selection of the MODE0 and MODE1 pins. A logic high on this pin powers up, and a logic low on this pin powers down.
14	VOUT-	Negative Analog Output.
15	VOUT+	Positive Analog Output.
16, 19	VPOS	Positive Power Supply, 5 V.
17	VIN+	Positive Analog Input.
18	VIN-	Negative Analog Input.
20	DNC INTERIM	Do Not Connect. Tie DNC INTERIM to a resistor divider that is 25 kΩ to 5 V and 50 kΩ to ground or to a pull-up that is 50 kΩ to 3.3 V.
	EP	Exposed Pad Ground. The exposed pad must be connected to a low impedance ground plane. This plane is the ground (0 V) reference for all voltages in Table 1.

Table 6. Pin Function Overview for Various Modes

Mode	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 11	Pin 13
Parallel										
High Performance	0	0	Unused	D4	D3	D2	D1	D0	LATCH	1
Low Power	1	1	Unused	D4	D3	D2	D1	D0	LATCH	1
SPI, 3-Wire										
High Performance	0	1	SDIO	SCLK	$\overline{\text{CS}}$	FA	Unused	0	0	1
Low Power	0	1	SDIO	SCLK	$\overline{\text{CS}}$	FA	Unused	0	1	1
SPI, 4-Wire										
High Performance	0	1	SDO	SCLK	$\overline{\text{CS}}$	FA	SDI	1	0	1
Low Power	0	1	SDO	SCLK	$\overline{\text{CS}}$	FA	SDI	1	1	1
Up or Down										
High Performance	1	0	Unused	Unused	GS1	GS0	UPDN_CLK	UPDN_DAT	0	1
Low Power	1	0	Unused	Unused	GS1	GS0	UPDN_CLK	UPDN_DAT	1	1

## TYPICAL PERFORMANCE CHARACTERISTICS

Nominal  $V_{POS} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $Z_{LOAD} = 100\ \Omega$ , maximum gain (gain code = 00000), 2 V p-p composite differential output for IMD3 and OIP3, 2 V p-p differential output for HD2 and HD3, and  $V_{CM} = V_{POS}/2$ , unless otherwise noted.

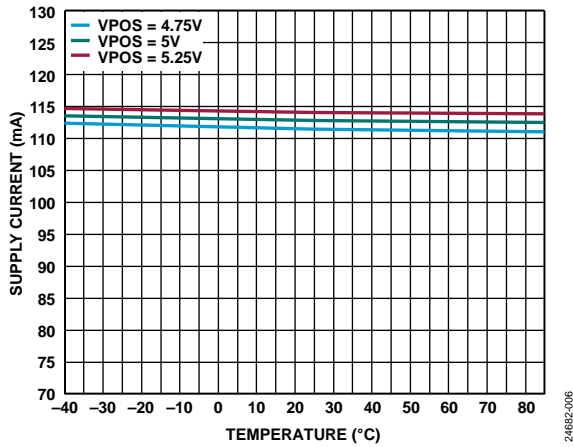


Figure 6. Supply Current vs. Temperature, High Performance Mode

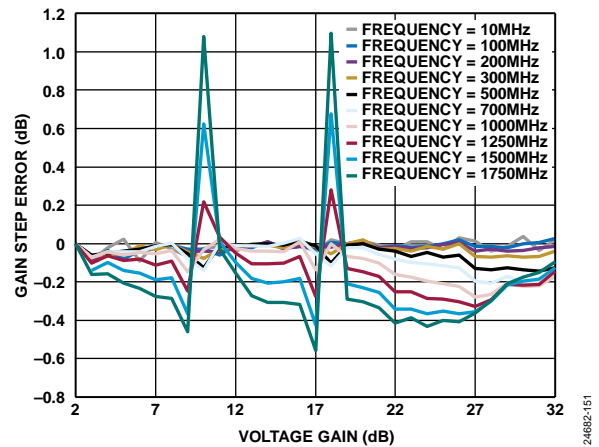


Figure 9. Gain Step Error vs. Voltage Gain, 5 V High Performance Mode

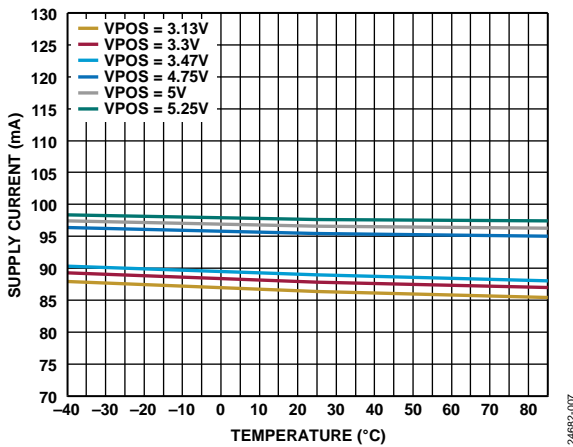


Figure 7. Supply Current vs. Temperature, Low Power Mode

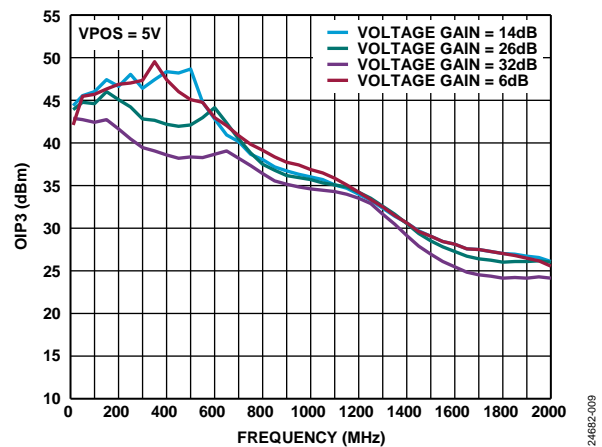


Figure 10. OIP3 vs. Frequency over  $V_{POS} = 5\text{ V}$  at Four Voltage Gains, High Performance Mode

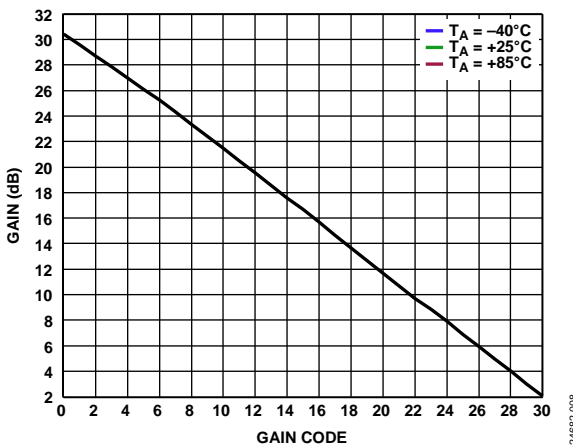


Figure 8. Gain vs. Gain Code over Temperature at 500 MHz

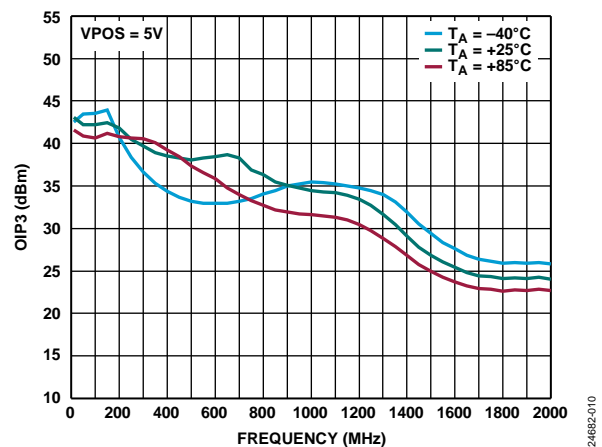


Figure 11. OIP3 vs. Frequency over  $V_{POS} = 5\text{ V}$  for Three Temperatures at Maximum Gain, High Performance Mode

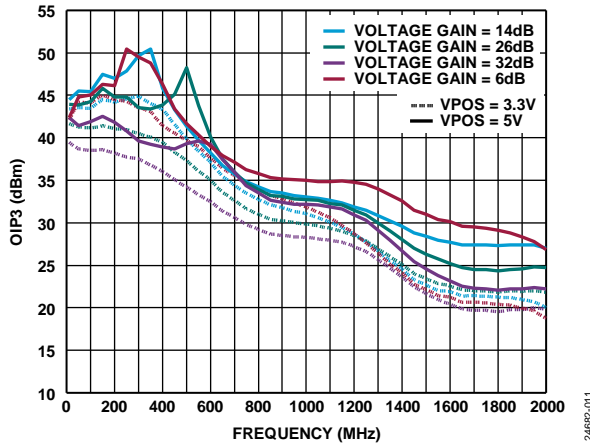


Figure 12. OIP3 vs. Frequency over VPOS = 3.3 V and VPOS = 5 V at Four Voltage Gains, Low Power Mode

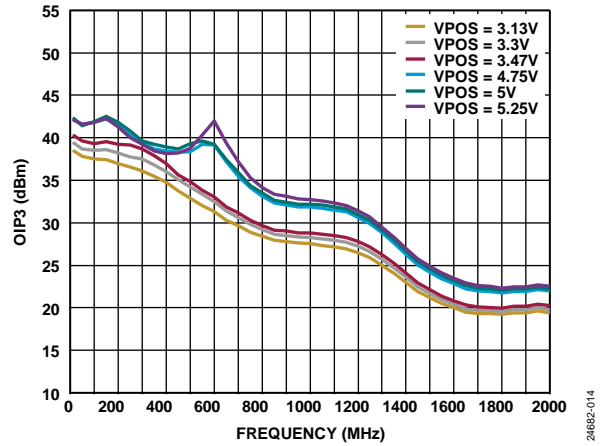


Figure 15. OIP3 vs. Frequency and VPOS Variance (5%) at Maximum Gain, Low Power Mode

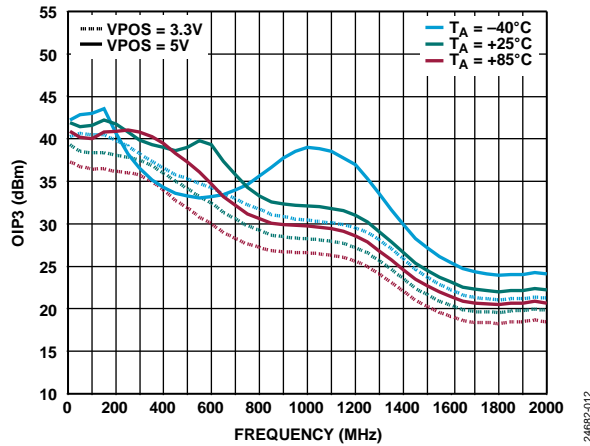


Figure 13. OIP3 vs. Frequency over VPOS = 3.3 V and VPOS = 5 V for Three Temperatures at Maximum Gain, Low Power Mode

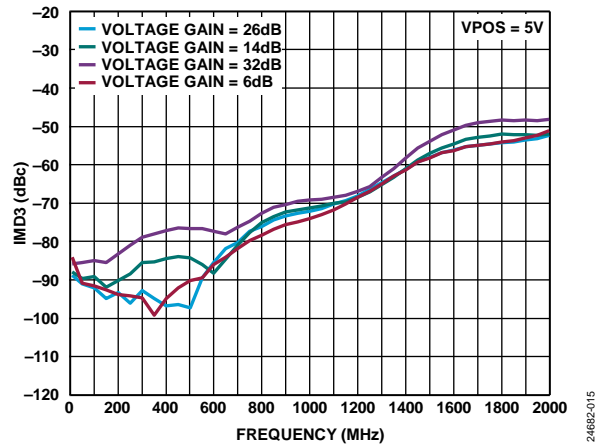


Figure 16. IMD3 vs. Frequency over VPOS = 5 V for Four Voltage Gains, High Performance Mode

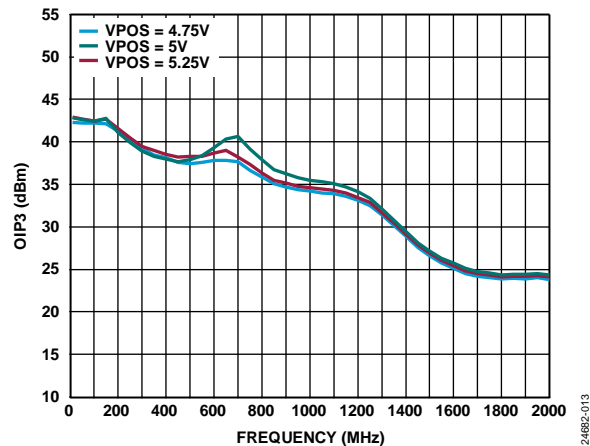


Figure 14. OIP3 vs. Frequency and VPOS Variance (5%) at Maximum Gain, High Performance Mode

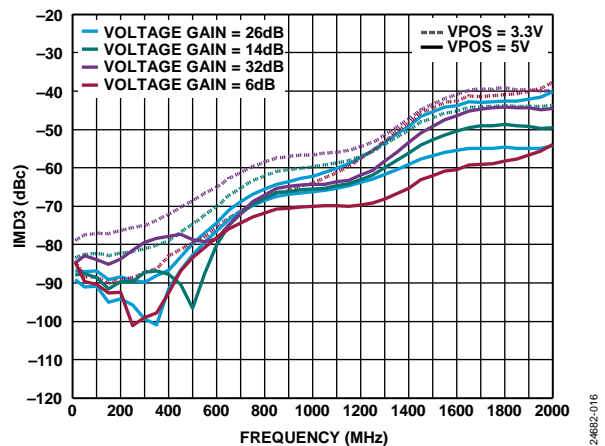


Figure 17. IMD3 vs. Frequency over VPOS = 3.3 V and VPOS = 5 V for Four Voltage Gains, Low Power Mode

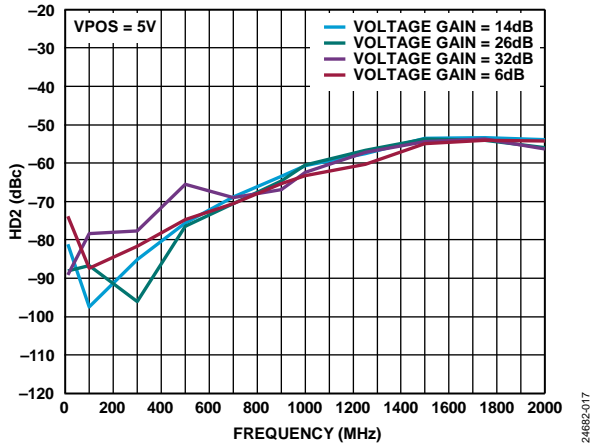


Figure 18. HD2 vs. Frequency over VPOS = 5 V for Four Voltage Gains, High Performance Mode

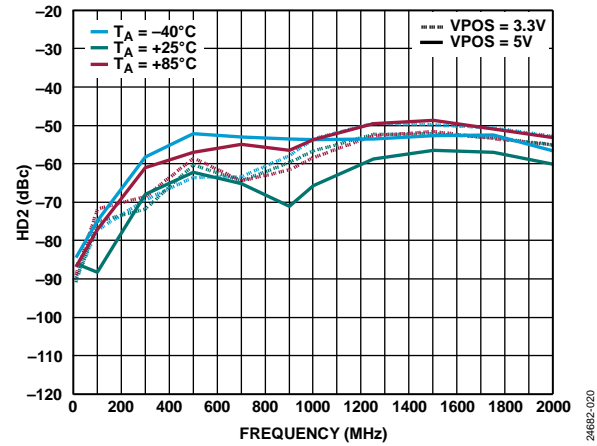


Figure 21. HD2 vs. Frequency over VPOS = 3.3 V and VPOS = 5 V for Three Temperatures at Maximum Gain, 2 V p-p, Low Power Mode

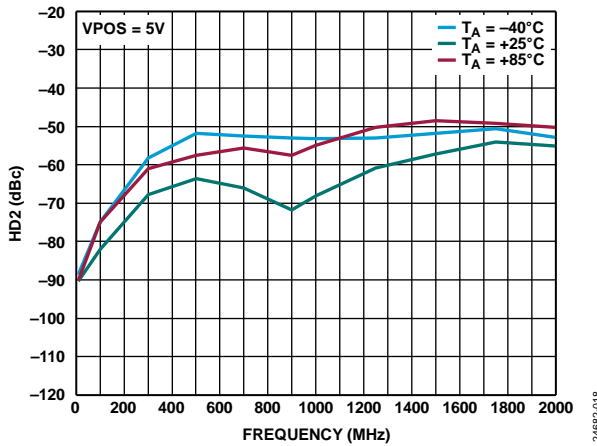


Figure 19. HD2 vs. Frequency over VPOS = 5 V for Three Temperatures at Maximum Gain, 2 V p-p, High Performance Mode

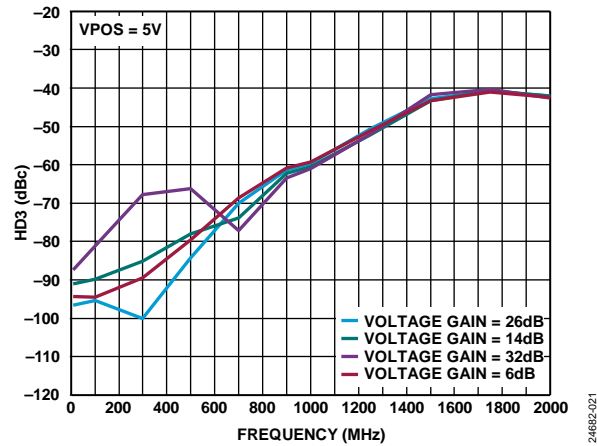


Figure 22. HD3 vs. Frequency over VPOS = 5 V for Four Voltage Gains at 2 V p-p, High Performance Mode

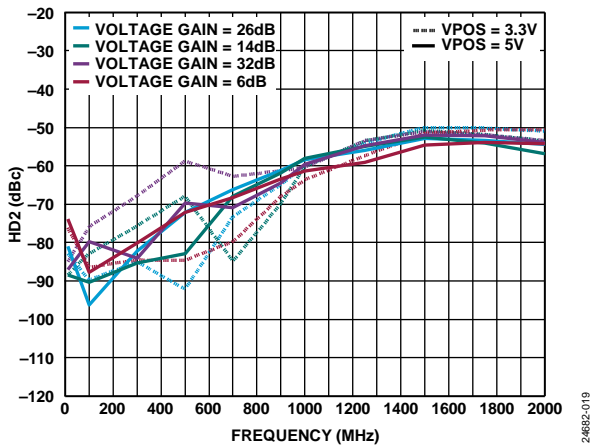


Figure 20. HD2 vs. Frequency over VPOS = 3.3 V and VPOS = 5 V for Four Voltage Gains at 2 V p-p, Low Power Mode

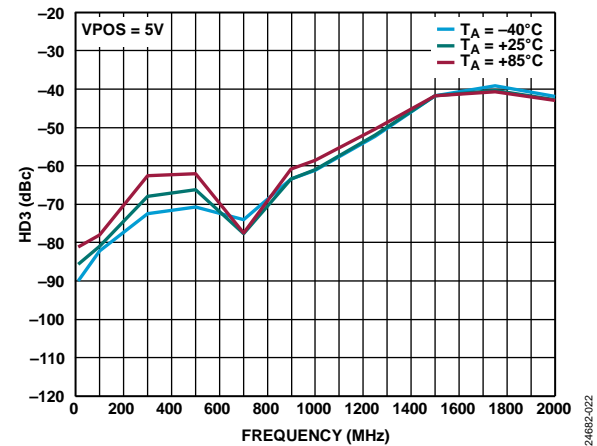


Figure 23. HD3 vs. Frequency over VPOS = 5 V for Three Temperatures at Maximum Gain, 2 V p-p, High Performance Mode

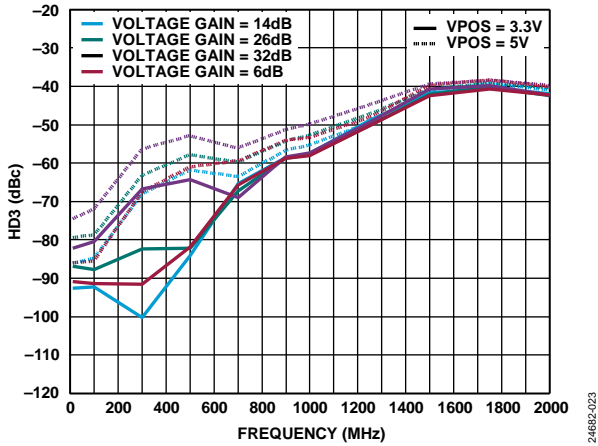


Figure 24. HD3 vs. Frequency over VPOS = 3.3 V and VPOS = 5 V for Four Voltage Gains at 2 V p-p, Low Power Mode

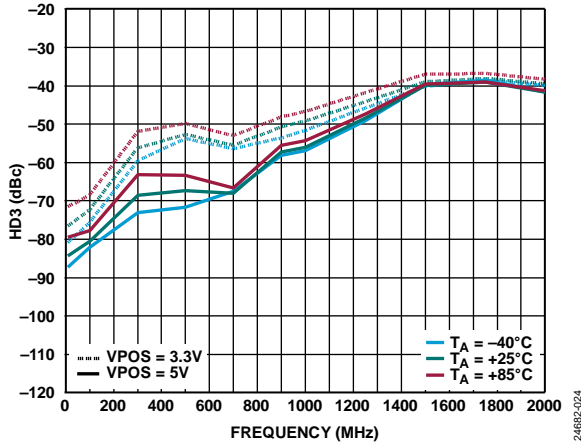


Figure 25. HD3 vs. Frequency over VPOS = 3.3 V and VPOS = 5 V for Three Temperatures at Maximum Gain, 2 V p-p, Low Power Mode

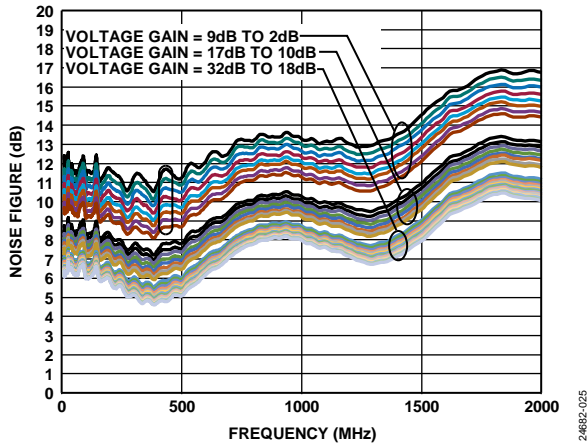


Figure 26. Noise Figure vs. Frequency over Voltage Gain Ranges, 5 V High Performance Mode

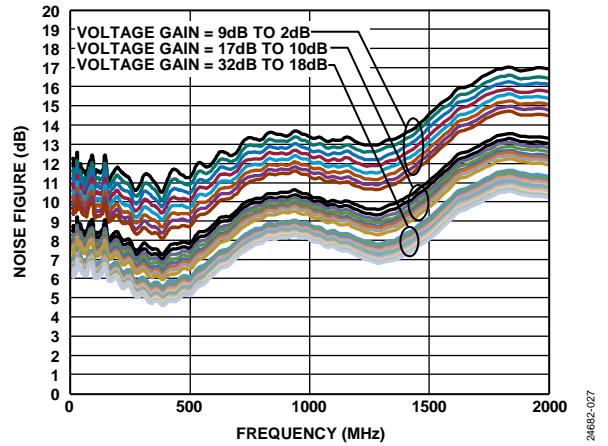


Figure 27. Noise Figure vs. Frequency over Voltage Gain Ranges, 5 V Low Power Mode

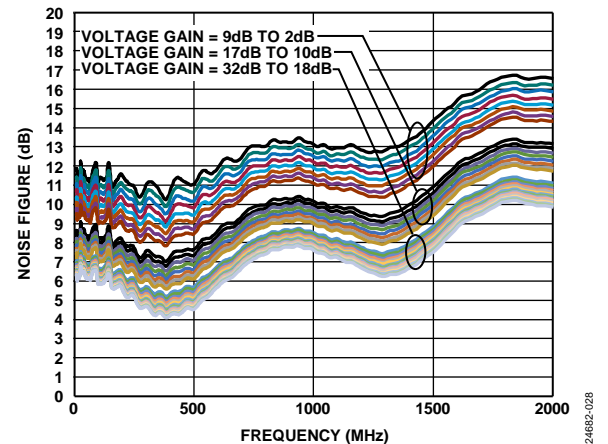


Figure 28. Noise Figure vs. Frequency over Voltage Gain Ranges, 3.3 V Low Power Mode

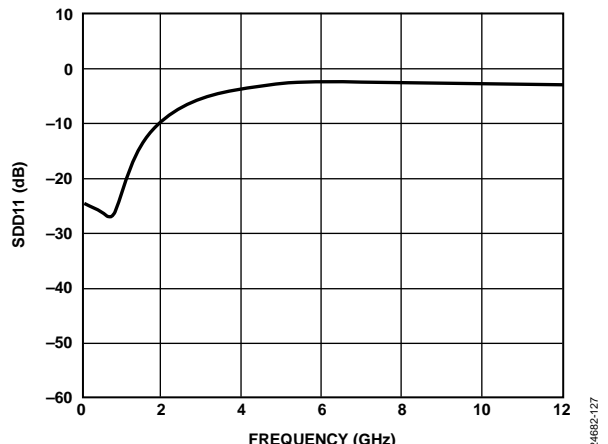


Figure 29. SDD11 vs. Frequency at Gain = 2 dB, 5 V High Performance Mode

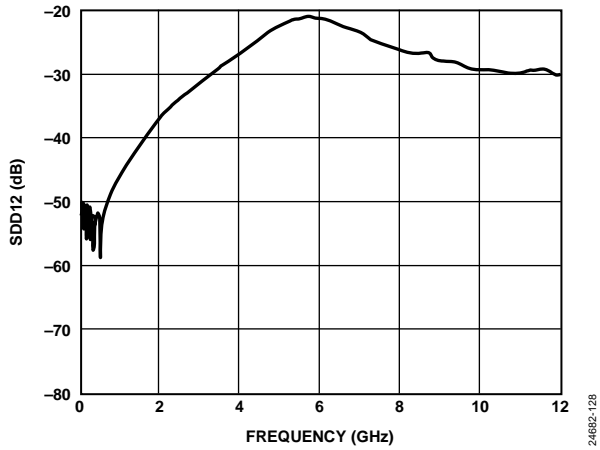


Figure 30. SDD12 vs. Frequency at Gain = 2 dB, 5 V High Performance Mode

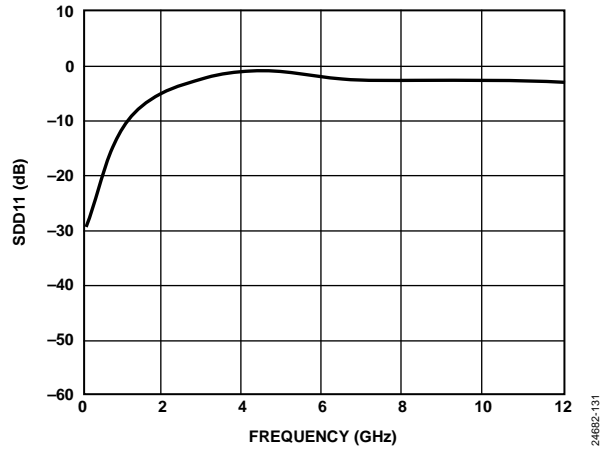


Figure 33. SDD11 vs. Frequency at Gain = 32 dB, 5 V High Performance Mode

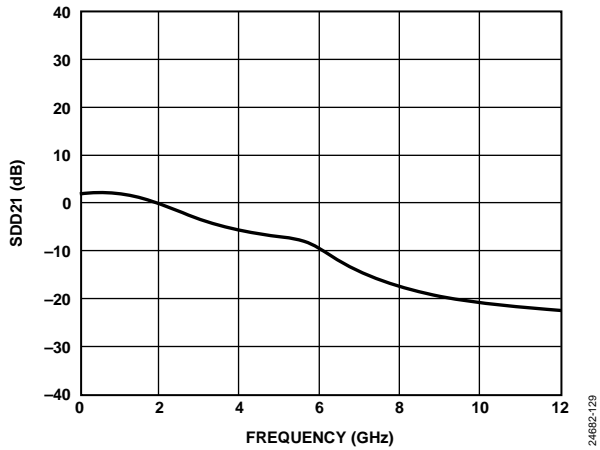


Figure 31. SDD21 vs. Frequency at Gain = 2 dB, 5 V High Performance Mode

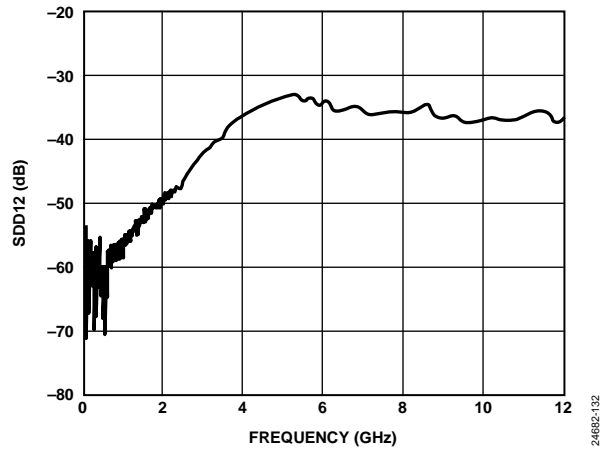


Figure 34. SDD12 vs. Frequency at Gain = 32 dB, 5 V High Performance Mode

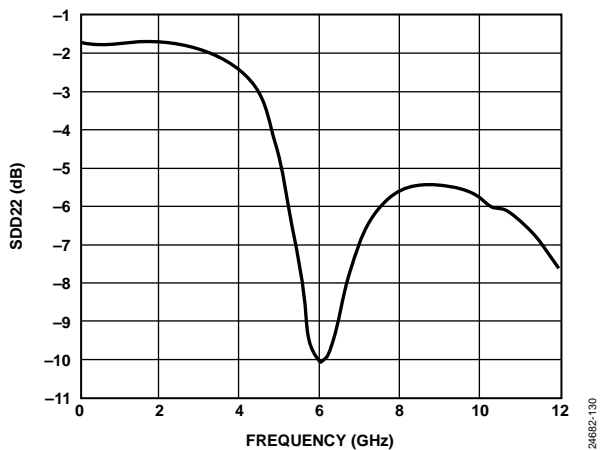


Figure 32. SDD22 vs. Frequency at Gain = 2 dB, 5 V High Performance Mode

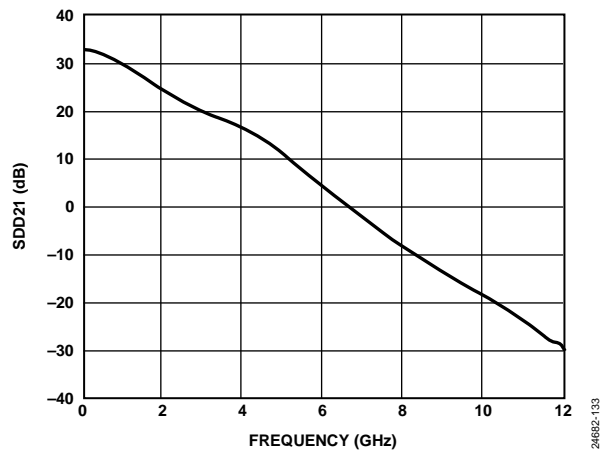


Figure 35. SDD21 vs. Frequency at Gain = 32 dB, 5 V High Performance Mode

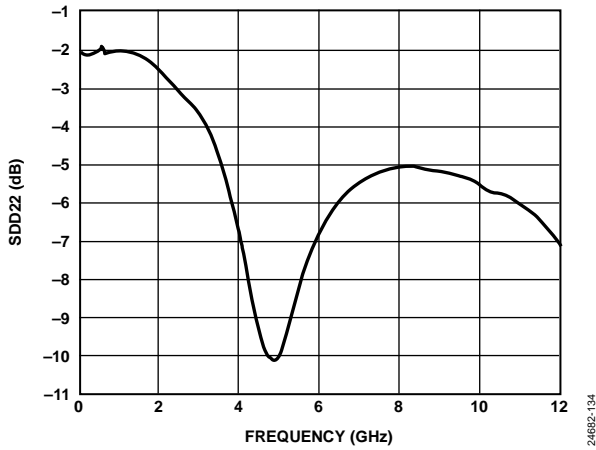


Figure 36. SDD22 vs. Frequency at Gain = 32 dB, 5 V High Performance Mode

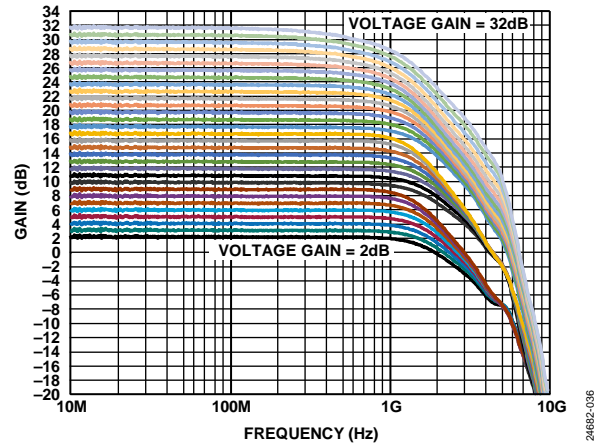


Figure 39. Gain vs. Frequency over Voltage Gains, 3.3 V Low Power Mode

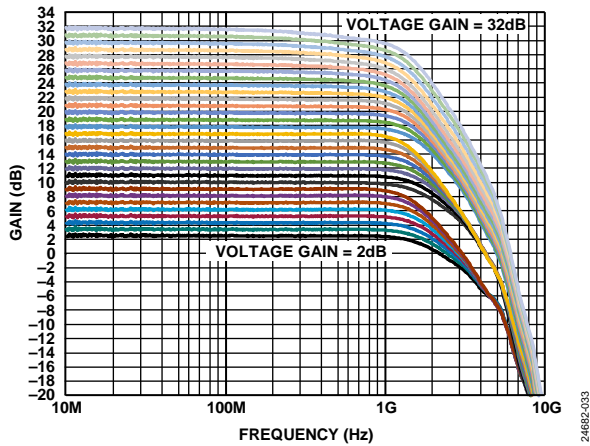


Figure 37. Gain vs. Frequency over Voltage Gains, 5 V High Performance Mode

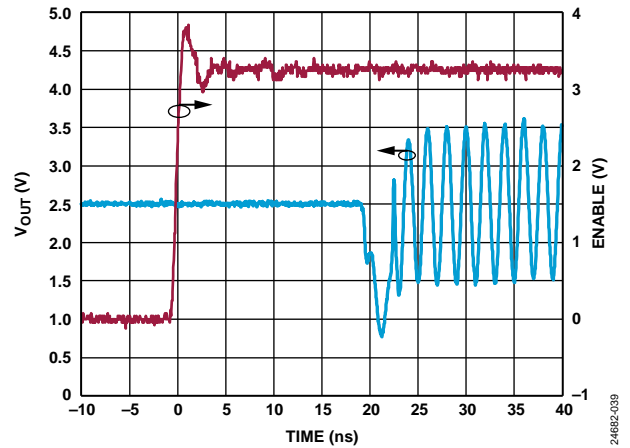


Figure 40. Enable Time Domain Response, 5 V High Performance Mode

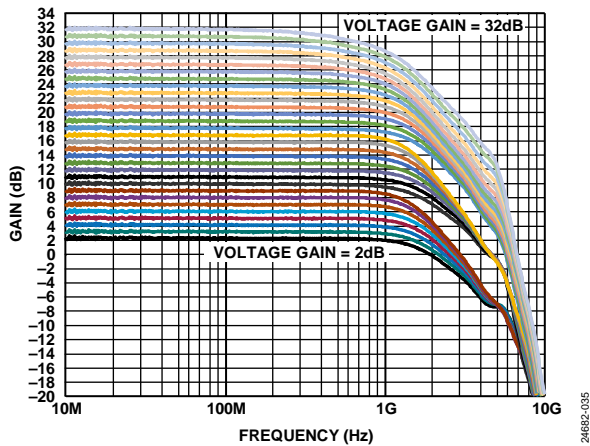


Figure 38. Gain vs. Frequency over Voltage Gains, 5 V Low Power Mode

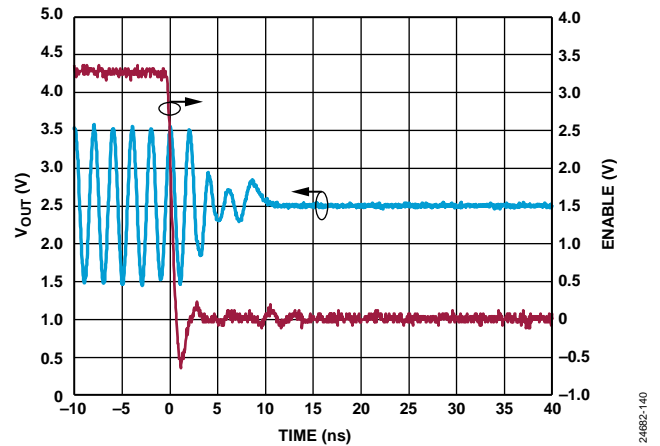


Figure 41. Disable Time Domain Response, 5 V High Performance Mode

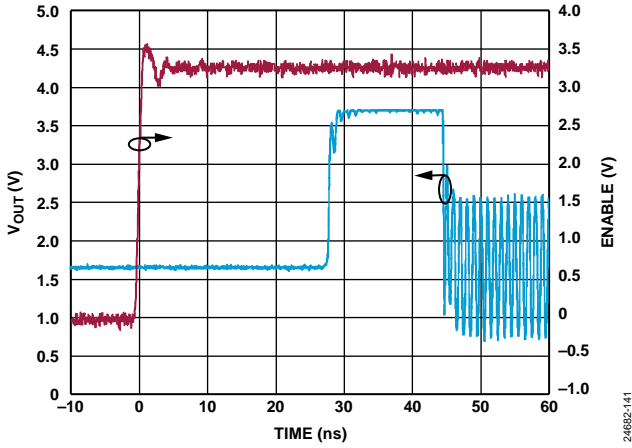


Figure 42. Enable Time Domain Response, 3.3 V Low Power Mode

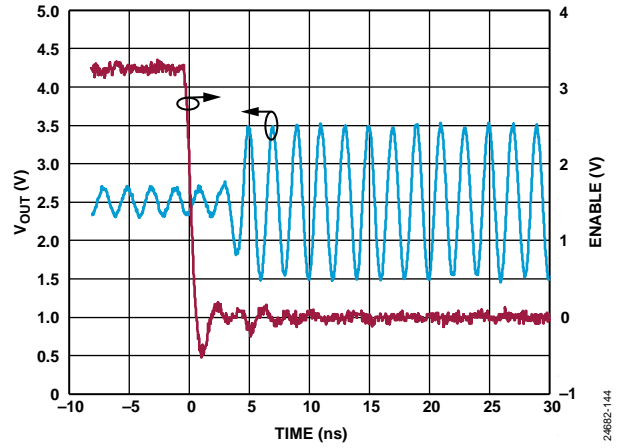


Figure 45. Fast Attack Disable Time Domain Response, 5 V High Performance Mode

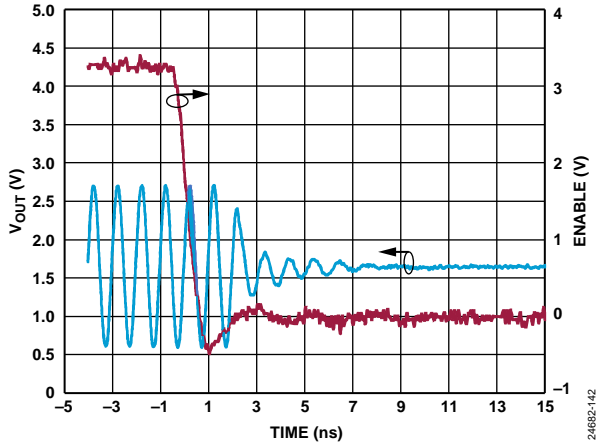


Figure 43. Disable Time Domain Response, 3.3 V Low Power Mode

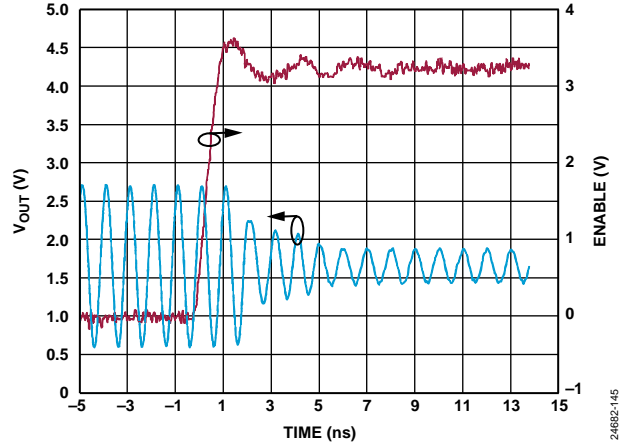


Figure 46. Fast Attack Enable Time Domain Response, 3.3 V Low Power Mode

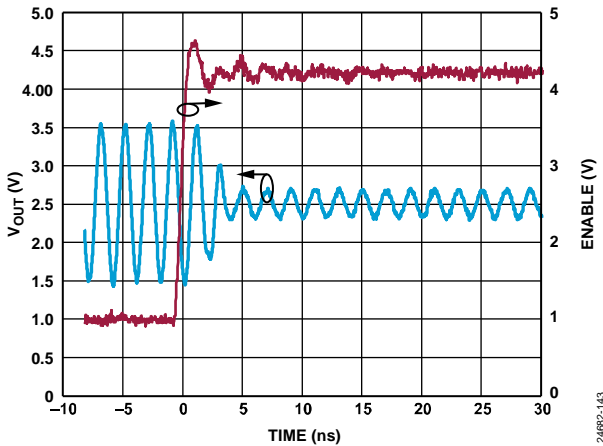


Figure 44. Fast Attack Enable Time Domain Response, 5 V High Performance Mode

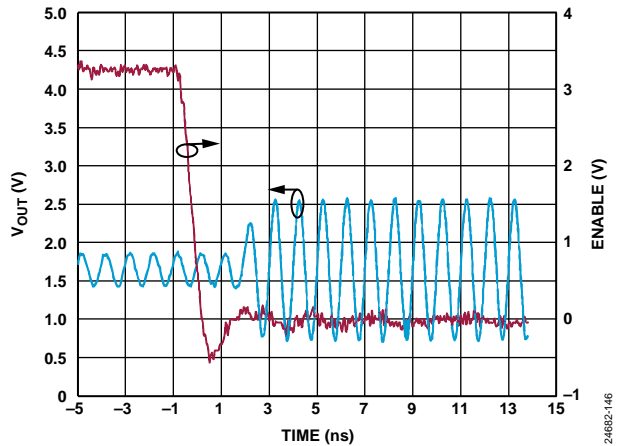


Figure 47. Fast Attack Disable Time Domain Response, 3.3 V Low Power Mode



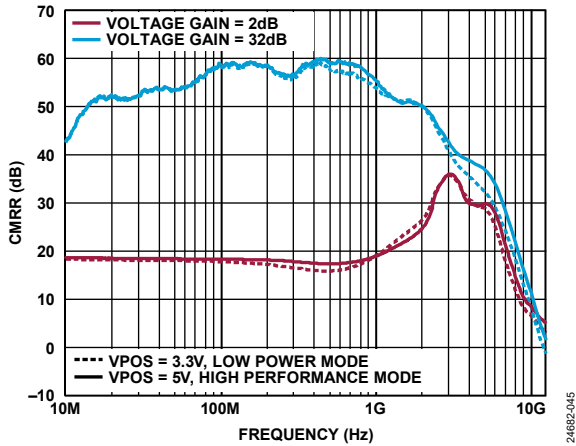


Figure 48. CMRR vs. Frequency at Voltage Gain = 2 dB and Voltage Gain = 32 dB, 5 V High Performance Mode and 3.3 V Low Power Mode

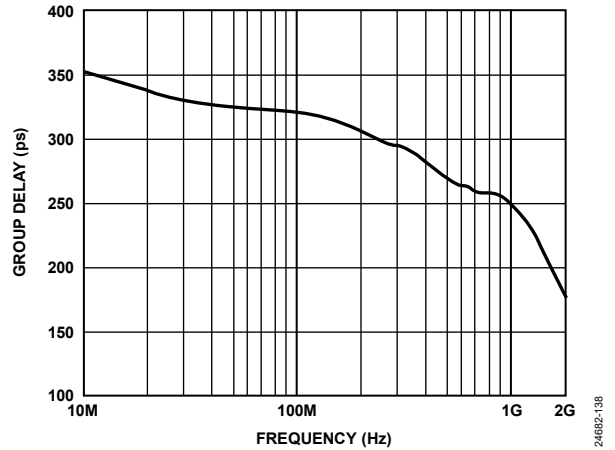


Figure 51. Group Delay vs. Frequency at Maximum Gain, 5 V High Performance Mode

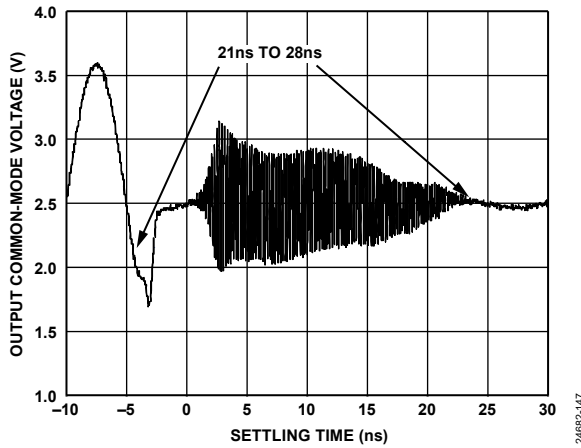


Figure 49. Output Common-Mode Voltage vs. Settling Time, 5 V High Performance Mode, Maximum Gain Transition

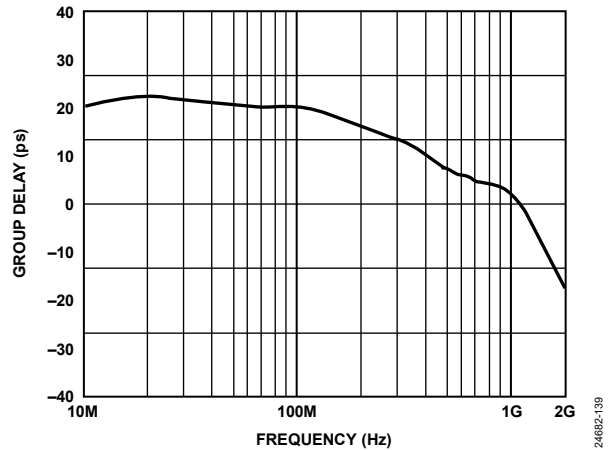


Figure 52. Group Delay vs. Frequency at Maximum Gain, 5 V Low Power Mode

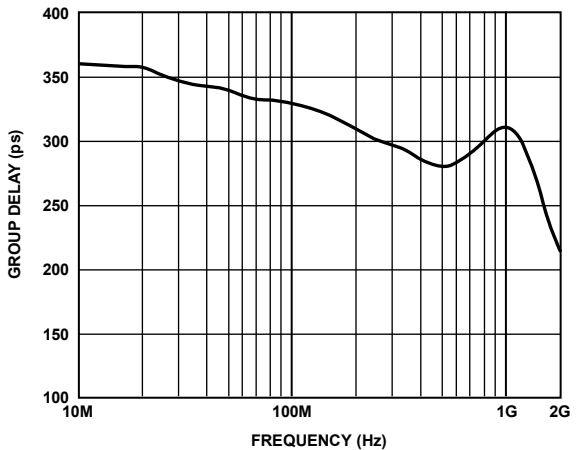


Figure 50. Group Delay vs. Frequency at Maximum Gain, 3.3 V Low Power Mode

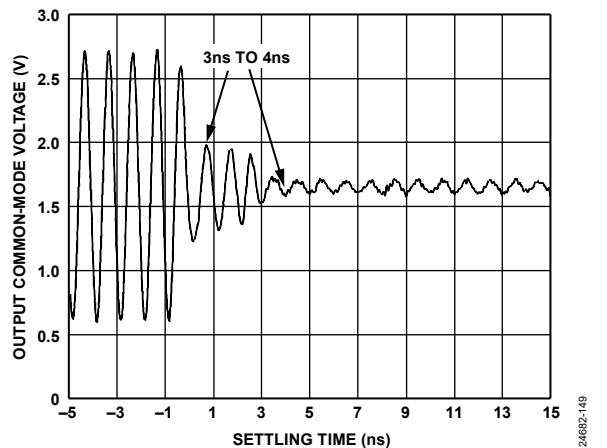
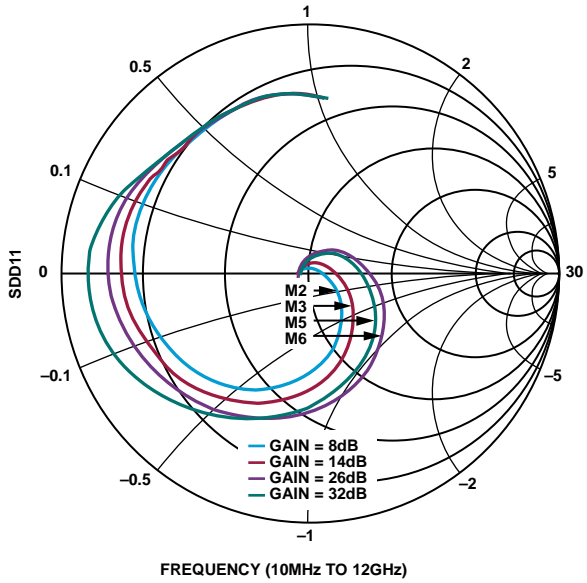
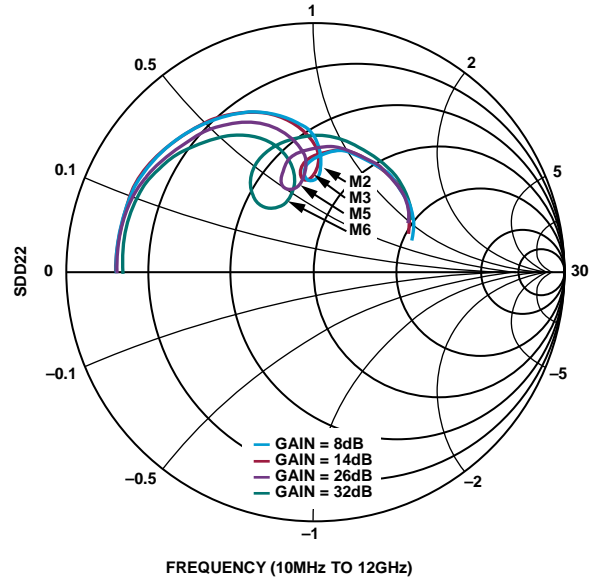


Figure 53. Output Common-Mode Voltage vs. Settling Time, 3.3 V Low Power Mode, Maximum Gain Transition



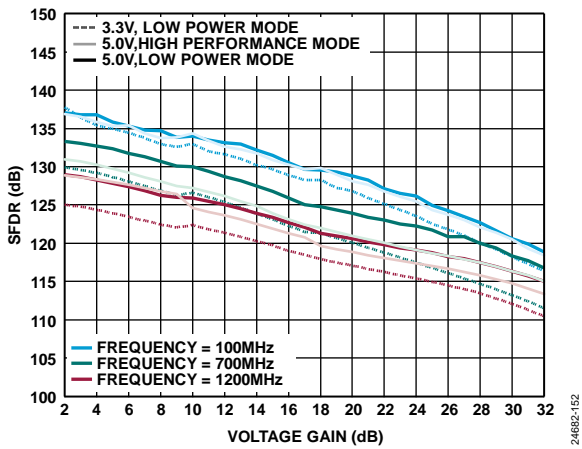
24682-135

Figure 54. Differential Input Reflection (SDD11) Magnitude and Phase vs. Frequency over Four Gain



24682-136

Figure 56. Differential Output Reflection (SDD22) Magnitude and Phase vs. Frequency over Four Gains



24682-152

Figure 55. Spurious-Free Dynamic Range (SFDR) vs. Voltage Gain Across Power Modes and Various Frequencies

## THEORY OF OPERATION

### BASIC STRUCTURE

The ADL5206 is a differential, digitally controlled VGA, which is also known as a DGA. The DGA consists of a  $100\ \Omega$  differential input, digitally controlled passive attenuator, followed by a digitally controlled gain amplifier. On-chip logic circuitry maps the gain codes such that all gain changes, from the maximum gain to minimum gain, are accomplished by only using the digitally controlled resistors in the feedback of the amplifier.

This technique does not require a digital step attenuator (DSA) on the input of the amplifier, thus providing SFDR increases as gain reduces. This topology also allows all 30 dB of gain reduction in the feedback with a total noise figure degradation of 7 dB only over the total 30 dB gain range at 700 MHz. The differential output impedance of the amplifier is  $10\ \Omega$ .

### CONTROL AND LOGIC CIRCUITRY

The ADL5206 features three different gain control interfaces: serial, parallel, or up and down control, which is determined by the combination of the MODE1 and MODE0 pins. For details on controlling the gain in each of these modes, see the Digital Interface Overview section. Typically, the gain step size is 1 dB. Larger step sizes can be programmed, as described in the Digital Interface Overview section. The amplifier has a maximum gain of 32 dB (Gain Code 00000) to a minimum gain of 2 dB (Gain Code 11110 to Gain Code 11111).

### COMMON-MODE VOLTAGE

The ADL5206 is flexible in terms of input and output coupling. The ADL5206 can be ac-coupled or dc-coupled at the inputs and/or outputs within the specified output common-mode voltage reference range of 1.2 V to 1.8 V for the 3.3 V supply and 1.4 V to 2.7 V for the 5 V supply, depending on the supply voltage. If no external output common-mode voltage is applied, the input and output common-mode voltages are set internally to half of the supply voltage.

The output common-mode voltages of the ADL5206 are controlled by the voltages on the VCM pin. The VCM pin is connected internally through  $5\ \text{k}\Omega$  resistors to the VPOS pin as well as to the exposed pad. As a result, the common-mode output voltage is preset internally to half of the supply voltage at VPOS. Alternatively, the VCM pin can be connected to the common-mode voltage reference output from an ADC, and thus the common-mode levels between the amplifier and the ADC can be matched without requiring any external components.

## REGISTER SUMMARY AND DETAILS

Table 7. Register Summary

Register Address	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x0	CTL	[7:0]	RESERVED	FAST_ATTACK_CTL		GAIN_CTL				0x18	R/W	

Register Address: 0x0, Reset: 0x18, Name: CTL

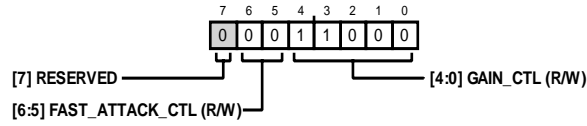


Table 8. Bit Descriptions for CTL

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved	0x0	R
[6:5]	FAST_ATTACK_CTL	Fast Attack Step Size	0x0	R/W
[4:0]	GAIN_CTL	Gain Control	0x18	R/W

# APPLICATIONS INFORMATION

## BASIC CONNECTIONS

Figure 57 shows the basic connections for operating the ADL5206.

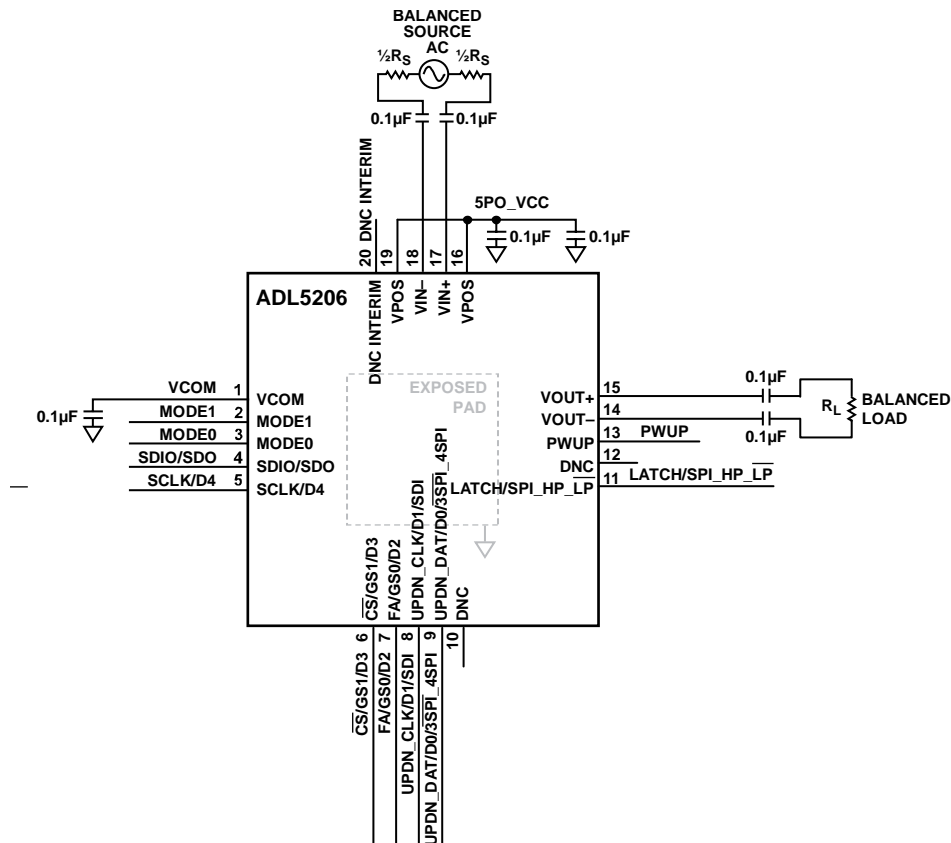
Apply a 3.3 V or 5 V voltage to the VPOS pins. Decouple the supply pins with at least one low inductance, surface-mount, 0.1  $\mu$ F ceramic capacitor and place the capacitor as close to the device as possible.

The differential outputs (VOUT+ and VOUT-) have a dc common-mode voltage that is approximately half of the supply. Therefore, decouple these outputs using 0.1  $\mu$ F capacitors to balance the load. The balanced differential inputs have the same dc common-mode voltage as the outputs. Note that the inputs

are decoupled using 0.1  $\mu$ F capacitors as well. The digital pins (that is the mode control pins, the associated SPI and parallel gain control pins, the power mode, and the PWUP pin) operate at a 3.3 V voltage.

To enable the ADL5206, pull the PWUP pin high ( $2.0\text{ V} \leq \text{PWUP} \leq 3.3\text{ V}$ ).

A logic low on the PWUP pin sets the ADL5206 to sleep mode, reducing the current consumption to approximately 7 mA. The VCOM pin is the output common-mode voltage, and the VCOM pin must be decoupled with a 0.1  $\mu$ F capacitor for filtering noise.



- NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THESE PINS.
  2. EXPOSED PAD GROUND. THE EXPOSED PAD MUST BE CONNECTED TO A LOW IMPEDANCE GROUND PLANE.

Figure 57. Basic Connections

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**DIGITAL INTERFACE OVERVIEW**

The three digital control interface options for the ADL5206 DGA include the following:

- Parallel control interface
- Serial peripheral interface
- Gain step-up and step-down interface

The digital control interface selection is made via two digital pins, MODE1 and MODE0, as shown in Table 9.

The same physical pins are shared between three interfaces, resulting in as many as three different functions per digital pin (see Table 5).

**Table 9. Digital Control Interface Selection Truth Table**

MODE1	MODE0	Interface
0	0	Parallel, high performance
0	1	Serial
1	0	Up and down
1	1	Parallel, low power

**Parallel Digital Interface**

The parallel digital interface uses five gain control bits and a latch pin. The LATCH pin controls whether the input data latch is transparent (logic low) or latched (logic high). In transparent mode, the gain changes as the input gain control bits change. In latched mode, the gain is determined by the latched gain setting and is not changed by changing the input gain control bits.

**SPI**

The SPI uses three pins (SDIO, SCLK, and  $\overline{CS}$ ) in 3-wire SPI mode and four pins (SDI, SDO, SCLK, and  $\overline{CS}$ ) in 4-wire SPI mode. The SPI data register consists of eight bits: five gain control bits (D0 to D4), two attenuation step size address bits (FA0 and FA1), and one read/write bit (R/W), as shown in Figure 58.

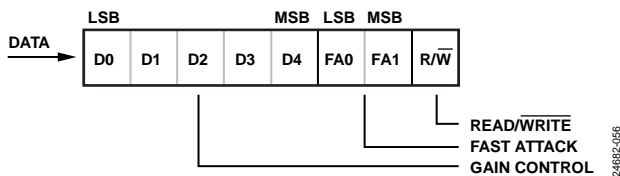


Figure 58. 8-Bit SPI Register

The SPI uses a bidirectional pin (SDIO) for writing to the SPI register and for reading from the SPI register in 3-wire SPI mode. Whereas in 4-wire SPI mode, SDI is dedicated to writing to the SPI register of the device, and SDO is dedicated to reading from the SPI register of the device. To write to the SPI register, pull the CS pin low and apply 8 clock pulses to shift the 8 bits into the corresponding SPI register, MSB first.

The SPI register read back operation is described in the SPI Read section.

SPI fast attack mode is controlled by the FA pin. A logic high on the FA pin results in an attenuation selected by the FA1 and the FA0 bits in the SPI register.

**Table 10. SPI 2-Bit Attenuation Step Size Truth Table**

FA1	FA0	Step Size (dB)
0	0	2
0	1	4
1	0	8
1	1	16

**Up and Down Interface**

The up and down interface uses two digital pins to control the gain. When the UPDN\_DAT pin is low, the gain is increased by a clock pulse on the UPDN\_CLK pin (rising and falling edges). When the UPDN\_DAT pin is high, the corresponding gain is decreased by a clock pulse on the UPDN\_CLK pin. Reset is detected when the rising edge of UPDN\_CLK latches one polarity on UPDN\_DAT, and the falling edge latches the opposite polarity. Reset results in a minimum gain code of 11110.

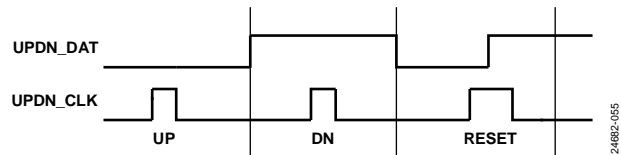


Figure 59. Up and Down Gain Control Timing

The step size is selectable by the GS1 and GS0 pins. The default step size is 1 dB. The gain code count rails at the top and bottom of the control range.

**Table 11. Step Size Control Truth Table**

GS1	GS0	Step Size (dB)
0	0	1
0	1	2
1	0	4
1	1	8

Table 12. Gain Code vs. Voltage Gain

5-Bit Binary Gain Code, D4 to D0	Voltage Gain (dB)
00000	32
00001	31
00010	30
00011	29
00100	28
00101	27
00110	26
00111	25
01000	24
01001	23
01010	22
01011	21
01100	20
01101	19
01110	18
01111	17
10000	16
10001	15
10010	14
10011	13
10100	12
10101	11
10110	10
10111	9
11000	8
11001	7
11010	6
11011	5
11100	4
11101	3
11110	2

**SPI READ**

The ADL5206 can be read back only in serial mode during a read cycle (from  $\overline{CS}$  low to  $\overline{CS}$  high) after the R/W bit is set high in the previous cycle. During the read cycle, data changes at each rising edge of SCLK and can be latched using the falling edge of SCLK. There is no continual read operation. A logic high (1) must be written into the R/W bit to enable the subsequent read cycle, and once the R/W bit is set, the rest of the bits are ignored in that write cycle.

The sequence for writing and then reading back is shown in Figure 60 to Figure 62, showing the operation of the input and output functions of the SDIO pin.

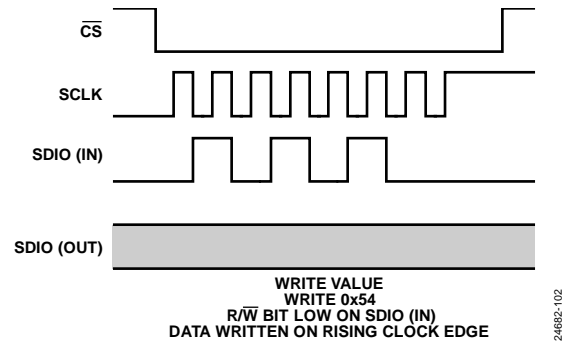


Figure 60. Write Gain Control Word

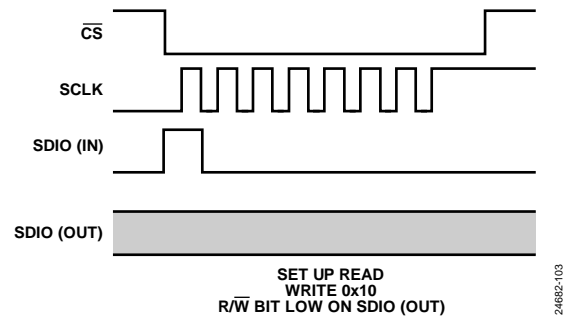


Figure 61. Write Logic 1 into R/W Bit

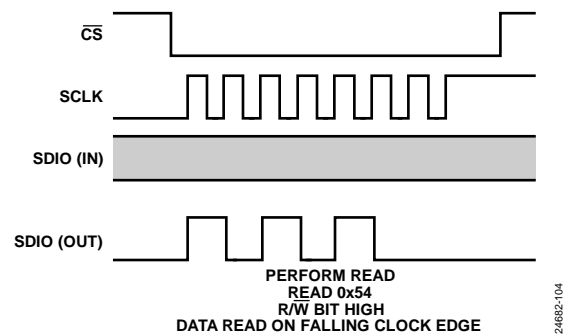


Figure 62. Perform Read

**ADC INTERFACING**

A typical data acquisition system using the ADL5206 together with an antialiasing filter and an ADC is shown in Figure 63. The main role of the filter after the amplifier is for attenuating the broadband noise and out of band harmonics generated by the amplifier. Component values for a 500 MHz acquisition bandwidth are listed in Table 13. Without this filter, the out of band noise and distortion components alias back into the Nyquist band, resulting in a reduction of signal-to-noise ratio. The design of the filter preceding the ADL5206 amplifier is more specific to the system rejection requirements for the acquisition system.

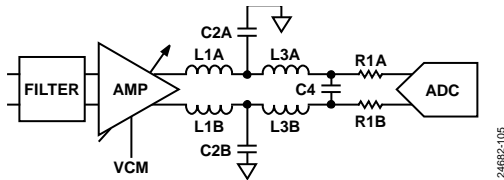


Figure 63. ADC Interface (One of Two Channels Shown)

**Table 13. Component Values for a 500 MHz Acquisition System**

Component	Value	Description/Comments
Amplifier	½ ADL5206	One channel
L1A, L1B	22 nH	Q ≥ 50 at 500 MHz
C2A, C2B	6.8 pF	Final value depends on PCB parasitics
L3A, L3B	22 nH	Q ≥ 50 at 500 MHz
C4	1.5 pF	Final value depends on PCB parasitics
R1A, R1B	10 Ω	Not applicable
ADC	½ AD9680	One channel, input impedance set to 100 Ω

**NOISE FIGURE vs. GAIN SETTING**

Because of the architecture of the ADL5206, the noise figure does not degrade significantly for the first 10 dB of gain reduction from the maximum gain setting. The noise figure increases by 0.5 dB only during the first 10 dB of gain reduction. The noise figure changes by 7 dB over the 30 dB gain range.

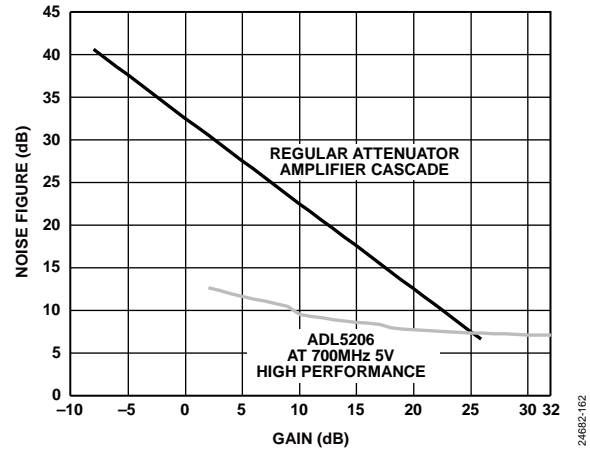
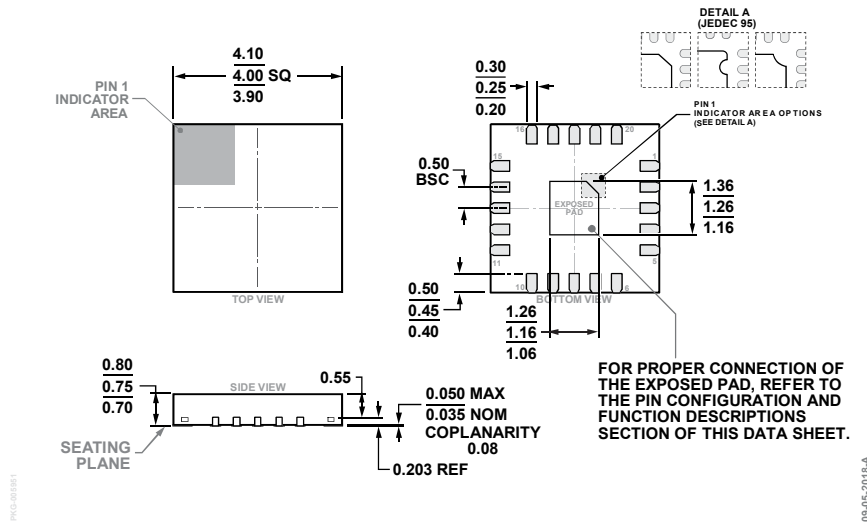


Figure 64. Noise Figure vs. Gain



# OUTLINE DIMENSIONS



## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADL5206ACPZ-R7	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-16
ADL5206ACPZ	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-16
ADL5206-EVALZ		Evaluation Board	

<sup>1</sup> Z = RoHS-Compliant Part.

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