160 dB Range, 100 pA to 10 mA Logarithmic Converter

Data Sheet

ADL5303

FEATURES

Optimized for fiber optic photodiode interfacing
8 full decades of range
Law conformance: 0.1 dB from 1 nA to 1 mA
Single-supply operation: 3.0 V to 5.5 V
Complete and temperature stable
Accurate laser trimmed scaling
Logarithmic slope of 10 mV/dB (at the VLOG pin)
Basic logarithmic intercept at 100 pA
Easy adjustment of slope and intercept
Output bandwidth of 10 MHz, 15 V/µs slew rate
Miniature 16-lead package (LFCSP)
Low power: ~4.5 mA quiescent current (enabled)

APPLICATIONS

High accuracy optical power measurement
Wide range baseband log compression
Versatile detector for APC loops

SIMPLIFIED BLOCK DIAGRAM

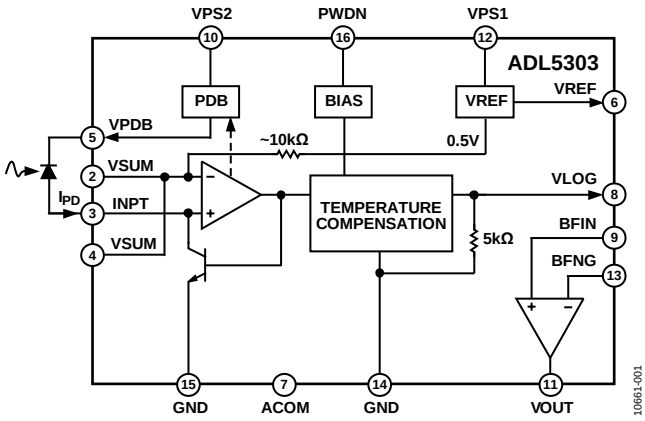

Figure 1.

GENERAL DESCRIPTION

The ADL5303 is a monolithic logarithmic detector optimized for the measurement of low frequency signal power in fiber optic systems and offers a large dynamic range in a versatile and easily used form. Wide measurement range and accuracy are achieved using proprietary design and precise laser trimming. The ADL5303 requires only a single positive supply, V_{PS}, of 5 V. When using low supply voltages, the log slope can be altered to fit the available span. Low quiescent current and chip disable facilitate use in battery-operated applications.

The input current, I_{PD}, flows in the collector of an optimally scaled NPN transistor, connected in a feedback path around a low offset JFET amplifier. The current summing input node operates at a constant voltage, independent of current, with a default value of 0.5 V; this may be adjusted over a wide range. An adaptive biasing scheme is provided for reducing photodiode dark current at very low light input levels. The VPDB pin applies approximately 0.1 V reverse bias across the photodiode for I_{PD} = 100 pA, rising linearly to 2.0 V of reverse bias at I_{PD} = 10 mA to improve response time at higher power levels. The input pin INPT is flanked by the VSUM guard pins that track the voltage at the summing node. Connecting the exposed pad of the device to the VSUM pins provides a continuous guard to minimize leakage into the INPT pin.

The default value of the logarithmic slope at the VLOG output is set by an internal 5 kΩ resistor. Logarithmic slope can be lowered with an external shunt resistor or increased using the buffer and a pair of external feedback resistors. The addition of a capacitor at the VLOG pin provides a simple low-pass filter. The intermediate voltage, V_{LOG}, is buffered in an output stage that can swing to within about 100 mV of ground and the positive supply, V_{PS}, and provides a peak current drive capacity of ±20 mA. An on-board 2 V reference is provided to facilitate the repositioning of the intercept. The incremental bandwidth of a translinear logarithmic amplifier inherently diminishes for small input currents. At I_{PD} =1 nA, the bandwidth of the ADL5303 is approximately 2 kHz increasing in proportion to I_{PD} up to a maximum value of 10 MHz.

Rev. D Document Feedback

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1/2014—Rev. 0 to Rev. A

Changes to Slope and Intercept Adjustments Section ... 14

1/2013—Revision 0: Initial Version

SPECIFICATIONS

V_{PS} = 5 V, GND, ACOM = 0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min[1]	Typ	Max[1]	Unit
INPUT INTERFACE	Pin 3, INPT; Pin 2 and Pin 4, VSUM				
Specified Current Range	Flows toward Pin 3	100			pA
				10	mA
Input Node Voltage	Internally preset; may be altered	0.46	0.5	0.54	V
Temperature Drift	−40°C < T_A < +85°C		0.04		mV/°C
Input Guard Offset Voltage	$V_{OFS} = V_{IN} - V_{SUM}$	−20		+20	mV
PHOTODIODE BIAS[2]	Established between VPDB and INPT				
Minimum Value	I_{PD} = 100 pA	70	100		mV
Transresistance			200		mV/mA
LOGARITHMIC OUTPUT	Pin 8, VLOG				
Slope	Laser trimmed at 25°C	195	200	205	mV/dec
	0°C < T_A < 70°C	193		207	mV/dec
Intercept	Laser trimmed at 25°C	60	100	140	pA
	0°C < T_A < 70°C	35		175	pA
Law Conformance Error	10 nA < I_{PD} < 1 mA, peak error		0.05	0.25	dB
	1 nA < I_{PD} < 1 mA, peak error		0.1	0.7	dB
Maximum Output Voltage			1.6		V
Minimum Output Voltage			0.1		V
Output Resistance	Laser trimmed at 25°C	4.95	5	5.05	kΩ
REFERENCE OUTPUT	Pin 6, VREF				
Voltage WRT Ground	Laser trimmed at 25°C	1.98	2	2.02	V
	−40°C < T_A < +85°C	1.92		2.08	V
Output Resistance			2		Ω
OUTPUT BUFFER	Pin 9, BFIN; Pin 13, BFNG; Pin 11, VOUT				
Input Offset Voltage		−20		+20	mV
Input Bias Current	Flowing out of Pin 9 or Pin 13		0.4		µA
Incremental Input Resistance			35		MΩ
Output Range	R_L = 1 kΩ to ground		V_{PS} − 0.1		V
Output Resistance			0.5		Ω
Wideband Noise[3]	I_{PD} > 1 µA (see the Typical Performance Characteristics section)		1		µV/√Hz
Small Signal Bandwidth[3]	I_{PD} > 1 µA (see the Typical Performance Characteristics section)		10		MHz
Slew Rate	0.2 V to 4.8 V output swing		15		V/µs
POWER-DOWN INPUT	Pin 16, PWDN				
Logic Level, High State	−40°C < T_A < +85°C, 2.7 V < V_{PS} < 5.5 V	2			V
Logic Level, Low State	−40°C < T_A < +85°C, 2.7 V < V_{PS} < 5.5 V			1	V
POWER SUPPLY	Pin 10 and Pin 12, VPS2 and VPS1; Pin 14 and 15, GND				
Supply Voltage		3.0	5	5.5	V
Quiescent Current			4.5	5.6	mA
In Disabled State			60		µA

[1] Minimum and maximum specified limits on parameters are guaranteed but not tested and are six sigma values.
[2] This bias is internally arranged to track the input voltage at INPT; it is not specified relative to ground.
[3] Output noise and incremental bandwidth are functions of input current; see the Typical Performance Characteristics section.

ABSOLUTE MAXIMUM RATINGS

Table 2.

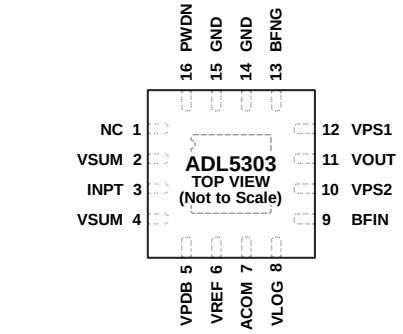
Parameter	Rating
V_{PS}	6 V
Input Current to INPT	20 mA
Thermal Data, 2-Layer JEDEC Board, No Air Flow (Exposed Pad Soldered to PCB)	
θ_{JA}	61.6°C/W
θ_{JC}	1.2°C/W
Maximum Power Dissipation (Exposed Pad Soldered to PCB)	0.6 W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT.
2. EXPOSED PAD. CONNECT THE EXPOSED PAD TO THE VSUM PINS TO PROVIDE LOW LEAKAGE GUARD.

10661-002

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	Pins labeled NC can be allowed to float, but it is better to connect these pins to ground. Avoid routing high speed signals through these pins because noise coupling may result.
2, 4	VSUM	Guard Pins. VSUM is used to shield the INPT current line.
3	INPT	Photodiode Current Input. Connect this pin to the photodiode anode (the photo current flows toward INPT).
5	VPDB	Photodiode Biaser Output. Connect this pin to the photodiode cathode when using adaptive bias control; otherwise, leave this pin floating.
6	VREF	Voltage Reference Output of 2 V.
7	ACOM	Analog Reference Ground.
8	VLOG	Output of the Logarithmic Front-End Processor. R_{OUT} = 5 kΩ to ground.
9	BFIN	Buffer Amplifier Noninverting Input (High Impedance).
10	VPS2	Positive Supply, V_{PS} (3.0 V to 5.5 V).
11	VOUT	Buffer Output; Low Impedance.
12	VPS1	Positive Supply, V_{PS} (3.0 V to 5.5 V).
13	BFNG	Buffer Amplifier Inverting Input.
14, 15	GND	Power Supply Ground Connection.
16	PWDN	Power-Down Control Input. Device is active when PWDN is taken low.
	EPAD	Exposed Pad. Connect the exposed pad to the VSUM pins to provide low leakage guard.

TYPICAL PERFORMANCE CHARACTERISTICS

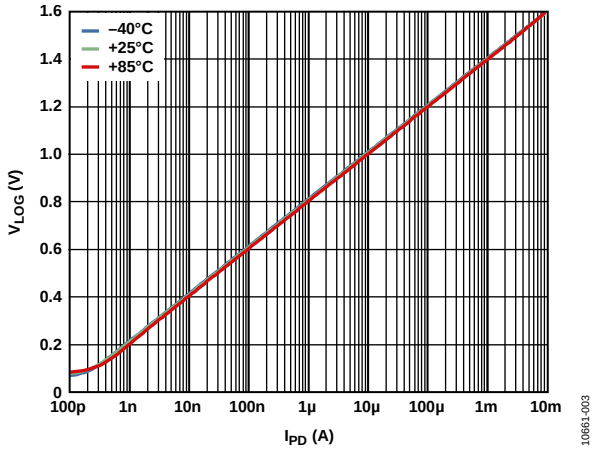


Figure 3. V_{LOG} vs. I_{PD}

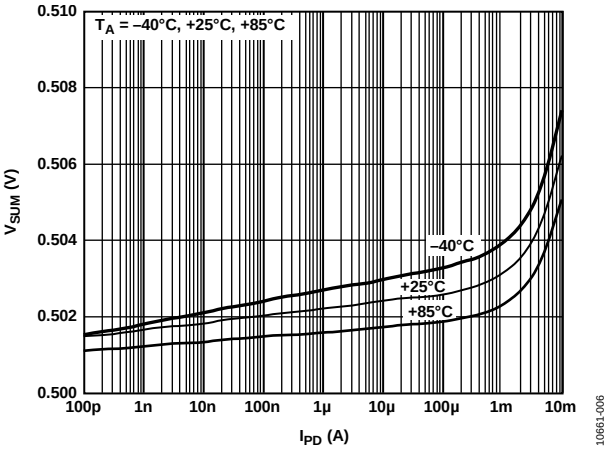


Figure 6. V_{SUM} vs. I_{PD}

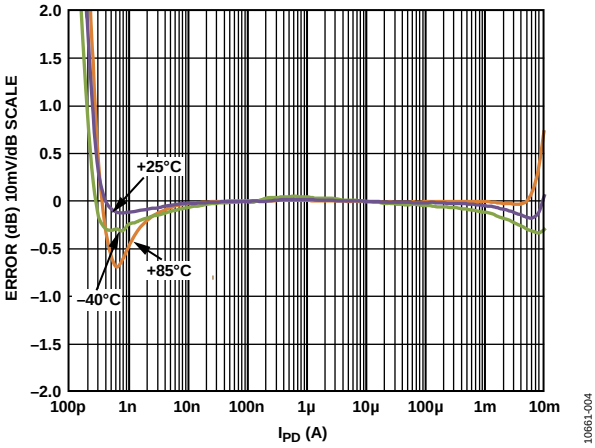


Figure 4. Logarithmic Conformance (Linearity) for V_{LOG}

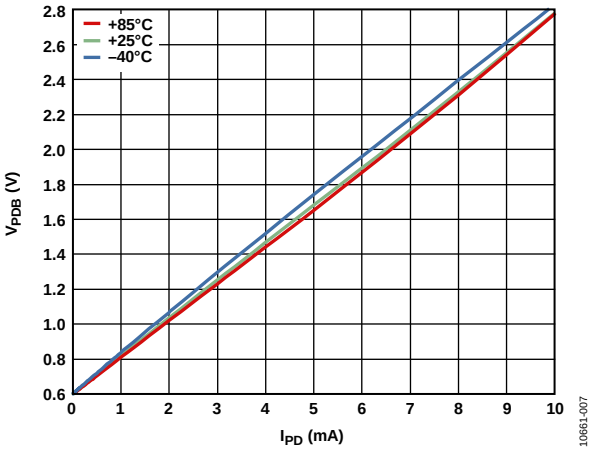


Figure 7. V_{PDB} vs. I_{PD}

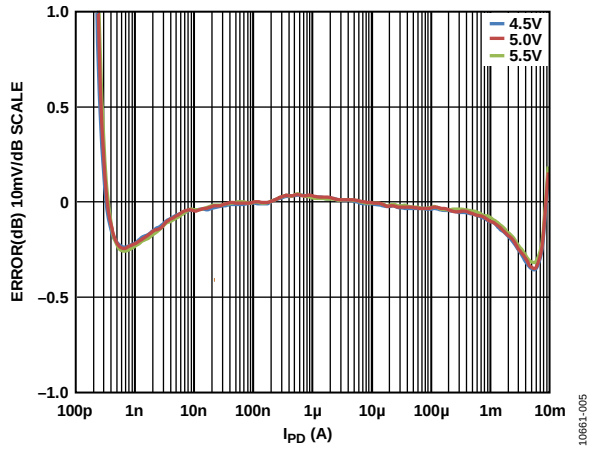


Figure 5. Absolute Deviation from Nominal Specified Value of V_{LOG} for Several Supply Voltages at 25°C

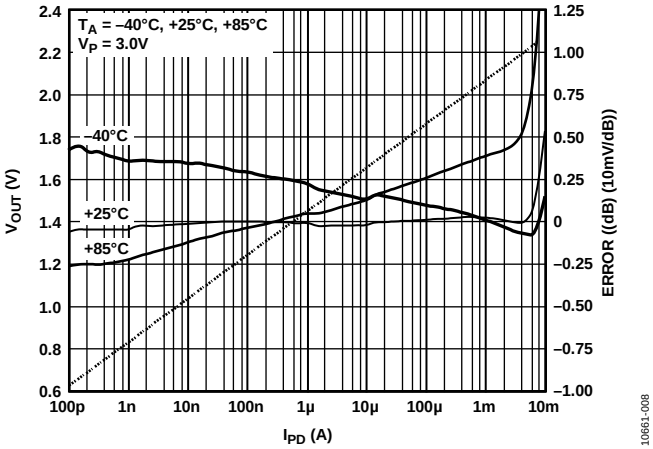


Figure 8. Logarithmic Conformance (Linearity) for a 3 V Single Supply

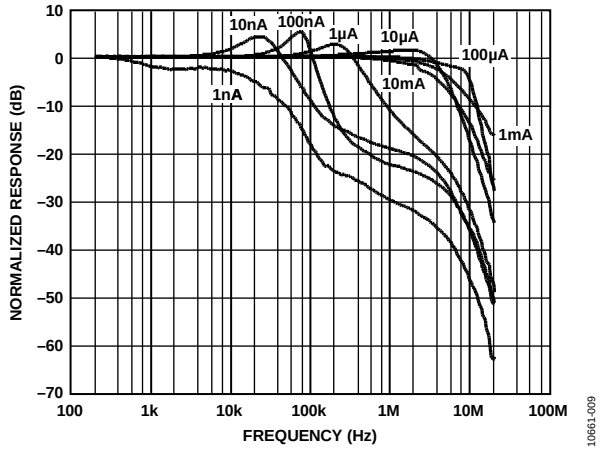


Figure 9. Small Signal AC Response, I_{PD} to V_{LOG} (5% Sine Modulation of I_{PD} at Frequency)

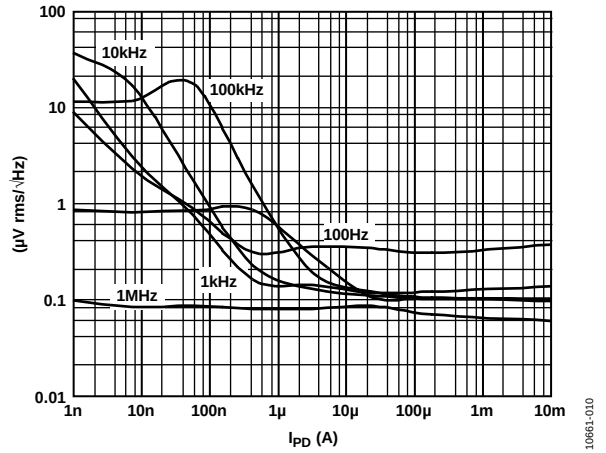


Figure 10. Spot Noise Spectral Density at V_{LOG} vs. I_{PD}

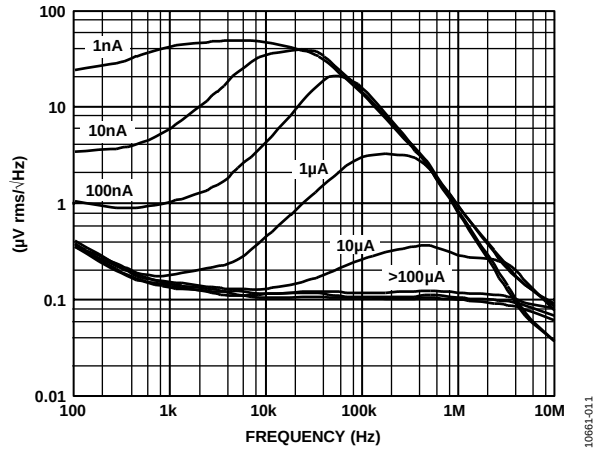


Figure 11. Spot Noise Spectral Density at V_{LOG} vs. Frequency

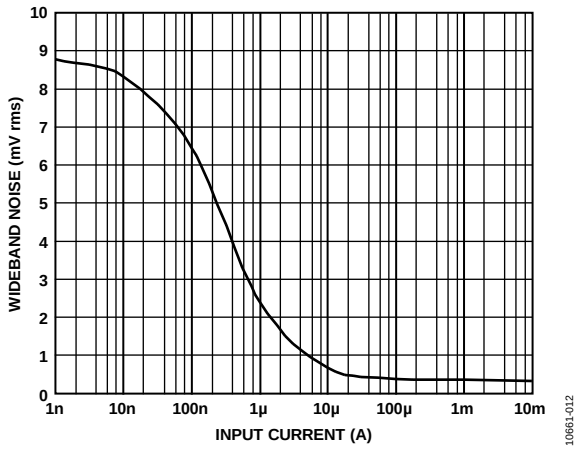


Figure 12. Total Wideband Noise Voltage at V_{LOG} vs. I_{PD}

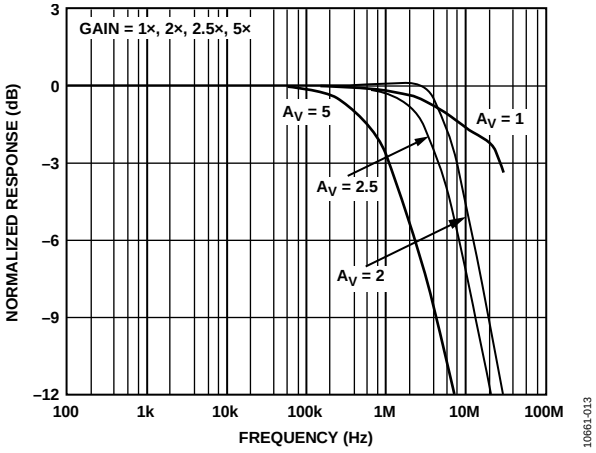


Figure 13. Small Signal Response of Buffer

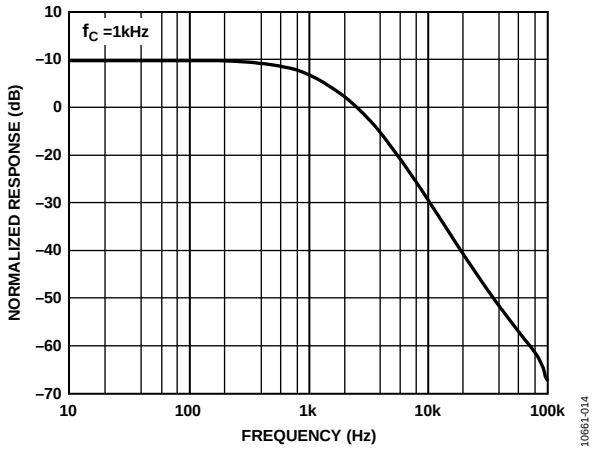


Figure 14. Small Signal Response of Buffer Operating as Two-Pole Filter

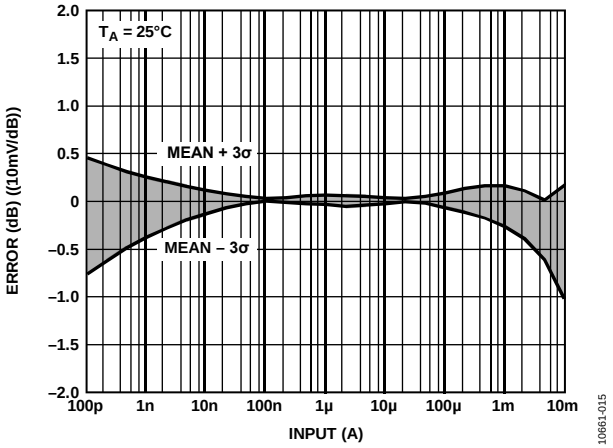


Figure 15. Logarithmic Conformance Error Distribution (3 σ to Either Side of Mean)

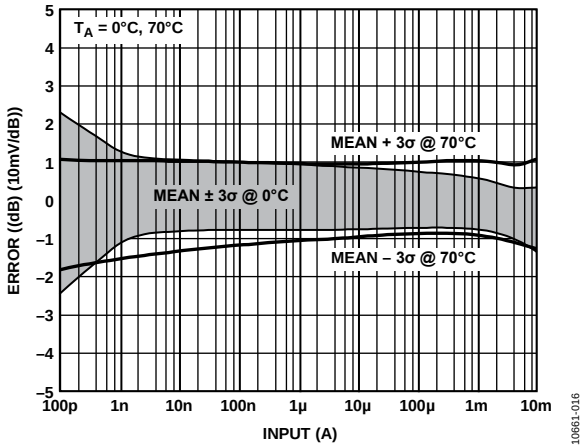


Figure 16. Logarithmic Conformance Error Distribution (3 σ to Either Side of Mean)

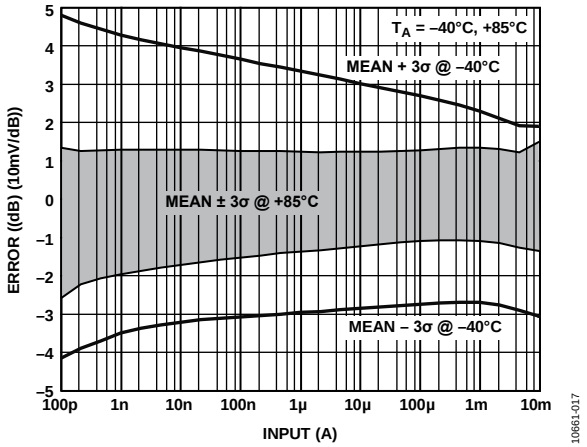


Figure 17. Logarithmic Conformance Error Distribution (3 σ to Either Side of Mean)

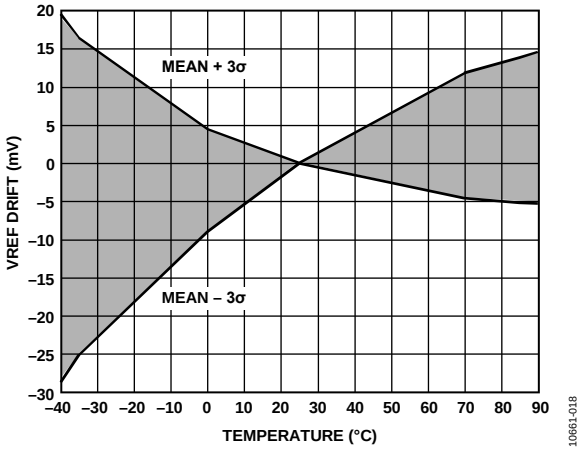


Figure 18. VREF Drift vs. Temperature (3 σ to Either Side of Mean)

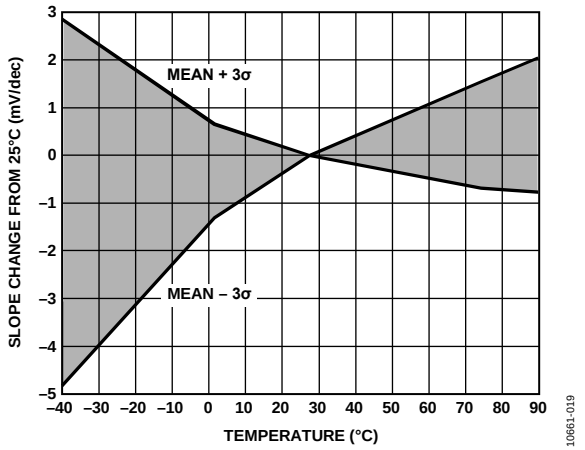


Figure 19. Slope Drift vs. Temperature (3 σ to Either Side of Mean)

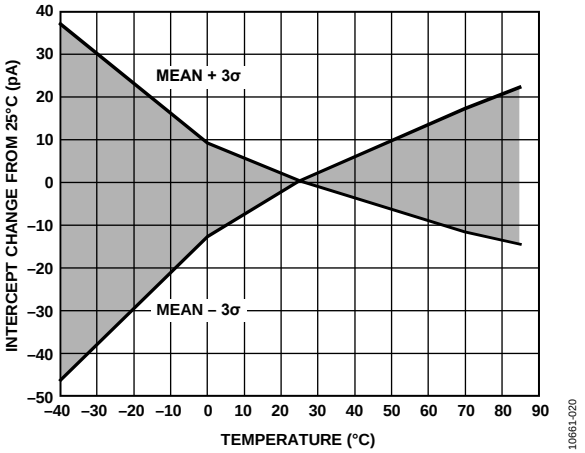


Figure 20. Intercept Drift vs. Temperature (3 σ to Either Side of Mean)

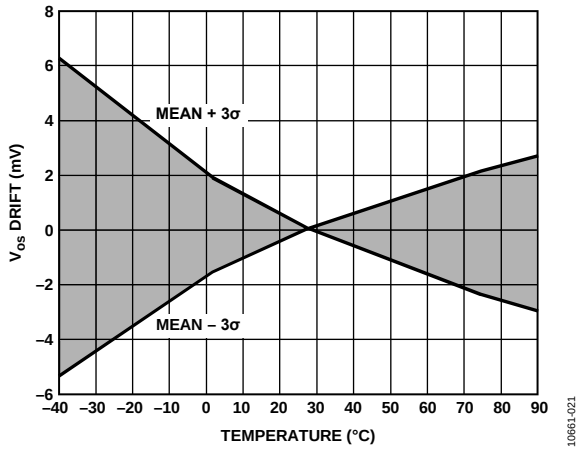


Figure 21. Output Buffer Offset vs. Temperature (3 σ to Either Side of Mean)

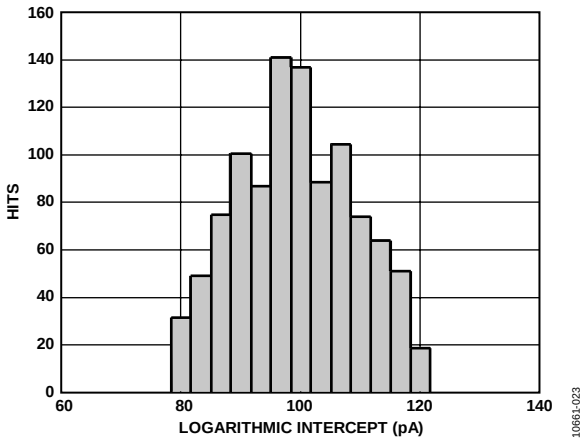


Figure 23. Distribution of Logarithmic Intercept

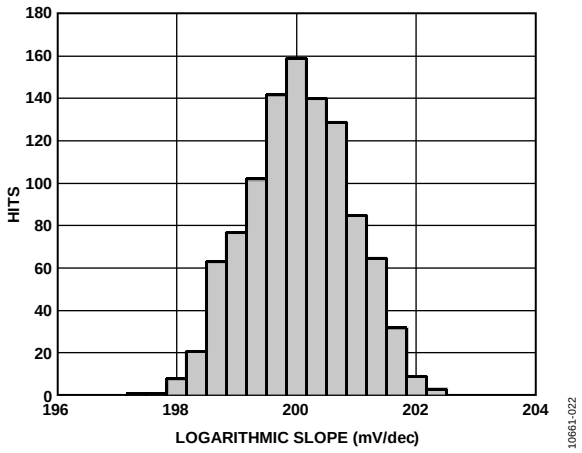


Figure 22. Distribution of Logarithmic Slope

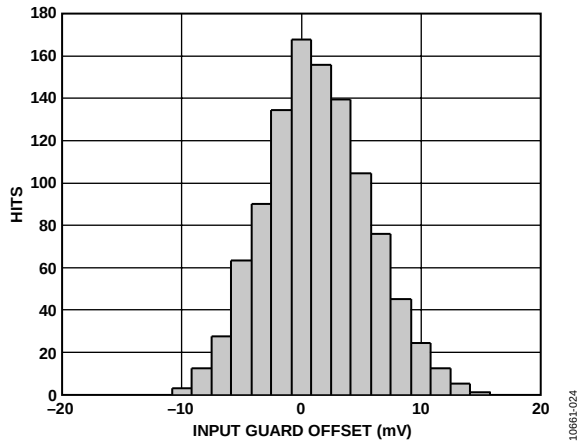


Figure 24. Distribution of Input Guard Offset Voltage V_{OFS} (V_{INPT} – V_{SUM})

THEORY OF OPERATION

BASIC CONCEPTS

The ADL5303 uses an advanced circuit implementation that exploits the logarithmic relationship between the base-to-emitter voltage, V_{BE}, and collector current, I_C, in a bipolar transistor.

Using these principles, the relationship between the input current, I_{PD}, applied to the INPT pin, and the voltage appearing at the intermediate output VLOG pin is:

$$V_{LOG} = V_Y \log_{10}(I_{PD}/I_Z) \quad (1)$$

where:
V_Y is the voltage slope (in the case of base-10 logarithms, it is also referred to as volts per decade).

I_Z is the fixed current in the logarithmic equation called the intercept.

In the following example, the scaling is chosen so that V_Y is trimmed to 200 mV/decade (10 mV/dB). The intercept is positioned at 100 pA; the output voltage, V_{LOG}, crosses zero when I_{PD} is of this value. However, the actual V_{LOG} must always be slightly above ground. Using Equation 2, calculate the output for any value of I_{PD}. Thus, for an input current of 25 nA,

$$V_{LOG} = 0.2\ V \log_{10}(25\ \text{nA}/100\ \text{pA}) = 0.4796\ \text{V} \quad (2)$$

In practice, both the slope and intercept can be altered, to either higher or lower values, without any significant loss of calibration accuracy, by using one or two external resistors, often in conjunction with the trimmed 2 V voltage reference at the VREF pin.

OPTICAL MEASUREMENTS

When interpreting the I_{PD} current in terms of optical power incident on a photodetector, it is necessary to be clear about the conversion (optical power to current) properties of a reverse biased photodiode. The units of this conversion are expressed in amps per watt and referred to as photodiode responsivity, ρ. For the typical InGaAs PIN photodiode, the responsivity is approximately 0.9 A/W.

It is important to note that in purely electrical circuits, current and power are not related in this proportional manner. A current applied to a resistive load results in a power proportional to the square of the current, $P = I^2R$. The difference in scaling for a photodiode is because I_{PD} flow in a reverse-biased diode is largely dependent on the fixed built-in voltage of the PN junction and is relatively insensitive to the external bias voltage. In the detector diode, power dissipated is proportional to the I_{PD} current and the relationship of I_{PD} to the optical power, P_{OPT}, is preserved.

$$I_{PD} = \rho P_{OPT} \quad (3)$$

The same relationship exists between the intercept current, I_Z, and an equivalent intercept power, P_Z, thus,

$$I_{PZ} = \rho P_Z \quad (4)$$

Therefore, Equation 1 can be written as

$$V_{LOG} = V_Y \log_{10}(P_{OPT}/P_Z) \quad (5)$$

For the ADL5303 operating in its default configuration, an I_Z of 100 pA corresponds to a P_Z of 110 pW, for a diode having a responsivity of 0.9 A/W. Thus, an optical power of 3 mW generates

$$V_{LOG} = 0.2\ \text{V} \log_{10}(3\ \text{mW}/110\ \text{pW}) = 1.487\ \text{V} \quad (6)$$

Note that when using the ADL5303 in optical applications the V_{LOG} output is referred to in terms of the equivalent optical power, the logarithmic slope remains 10 mV/dB at this output. This can be confusing because a decibel change on the optical side has a different meaning than on the electrical side. In either case, the logarithmic slope can always be expressed in units of millivolts per decade to help eliminate confusion.

DECIBEL SCALING

When power levels are expressed as decibels above a reference level (in dBm, for a reference of 1 mW), the logarithmic conversion has already been performed, and the log ratio in the previous expressions becomes a simple difference. Be careful in assigning variable names here, because P is often used to denote actual power as well as this same power expressed in decibels; however, these are numerically different quantities.

BANDWIDTH AND NOISE CONSIDERATIONS

Response time and wideband noise of translinear log amplifiers are a function of the signal current, I_{PD}. Bandwidth becomes progressively lower as I_{PD} is reduced, largely due to the effects of junction capacitances in the translinear device.

Figure 9 shows ac response curves for the ADL5303 at eight representative currents of 1 nA to 10 mA, using R1 = 750 Ω and C1 = 1000 pF. The values for R1 and C1 ensure stability over the full 160 dB dynamic range. More optimal values may be used for smaller subranges. A certain amount of experimental trial and error may be necessary to select the optimum input network component values for a given application.

The relationship between I_{PD} and the voltage noise spectral density, S_{NSD}, associated with the V_{BE} of Q1, calculates to the following:

$$S_{NSD} = \frac{14.7}{\sqrt{I_{PD}}} \quad (7)$$

where:
S_{NSD} is nV/Hz.
I_{PD} is expressed in microamps.
T_A = 25°C.

For an input of 1 nA, S_{NSD} evaluates to almost 0.5 μV/√Hz; assuming a 20 kHz bandwidth at this current, the integrated noise voltage is 70 μV rms. However, this calculation is not complete. The basic scaling of the V_{BE} is approximately 3 mV/dB; translated to 10 mV/dB, the noise predicted by Equation 7 must be multiplied by approximately 3.33. The additive noise effects associated with the reference transistor, Q2, and the temperature compensation circuitry must also be included. The final voltage noise spectral density presented at the VLOG pin varies inversely with I_{PD}, but is not a simple square root relationship. Figure 10 shows the measured noise spectral density vs. frequency at the VLOG output, for the same nine-decade spaced values of I_{PD}.

CHIP ENABLE

Power down the ADL5303 by taking the PWDN pin to a high logic level. The residual supply current in the disabled mode is typically 60 μA.

USING THE ADL5303

The default configuration (see Figure 25) includes a 2.5:1 attenuator in the feedback path around the buffer. This increases the slope of 10 mV/dB at the VLOG pin to 25 mV/dB at VOUT. For the full dynamic range of 160 dB (80 dB optical), the output swing is 4.0 V, which can be accommodated by the rail-to-rail output stage when using the recommended 5 V supply.

The capacitor from VLOG to ground forms an optional single-pole low-pass filter. Because the resistance at this pin is trimmed to 5 kΩ, an accurate time constant can be realized. For example, with C_{FLT} = 10 nF, the −3 dB corner frequency is 3.2 kHz. Such filtering is useful in minimizing the output noise, particularly when I_{PD} is small. Multipole filters are even more effective in reducing noise. A capacitor between VSUM and ground is essential for minimizing the noise on this node. When the bias voltage at either VPDB or VREF is not needed, these pins should be left unconnected.

SLOPE AND INTERCEPT ADJUSTMENTS

The choice of slope and intercept depends on the application. The versatility of the ADL5303 permits optimal choices to be made in two common situations. First, it allows an input current range of less than the full 160 dB to use the available voltage span at the output. Second, it allows this output voltage range to be optimally positioned to fit the input capacity of a subsequent ADC. In special applications, very high slopes, such as 1 V/decade, allow small subranges of I_{PD} to be covered at high sensitivity.

The slope can be lowered without limit by the addition of a shunt resistor, R_S, from VLOG to ground. Because the resistance at this pin is trimmed to 5 kΩ, the accuracy of the modified slope depends on the external resistor. It is calculated by,

$$V_{Y\_MODIFIED} = \frac{V_Y R_S}{R_S + 5\ \text{k}\Omega} \quad (8)$$

For example, using R_S = 3 kΩ, the slope is lowered to 75 mV per decade or 3.75 mV/dB. Table 4 provides a selection of suitable values for R_S and the resulting slopes.

Table 4. Examples of Lowering the Slope

R_S (kΩ)	Modified V_Y (mV/decade)
3	75
5	100
15	150
Open	200

In addition to uses in filter and comparator functions, the buffer amplifier provides the means to adjust both the slope and intercept, which require a minimal number of external components. The high input impedance at BFIN, low input offset voltage, large output swing, and wide bandwidth of this amplifier permit numerous transformations of the basic V_{LOG} signal, using standard op amp circuit practices. For example, it has been noted that to raise the gain of the buffer, and therefore the slope, a feedback attenuator, R_A and R_B in Figure 25, should be inserted between VLOG and the inverting input BFNG pin.

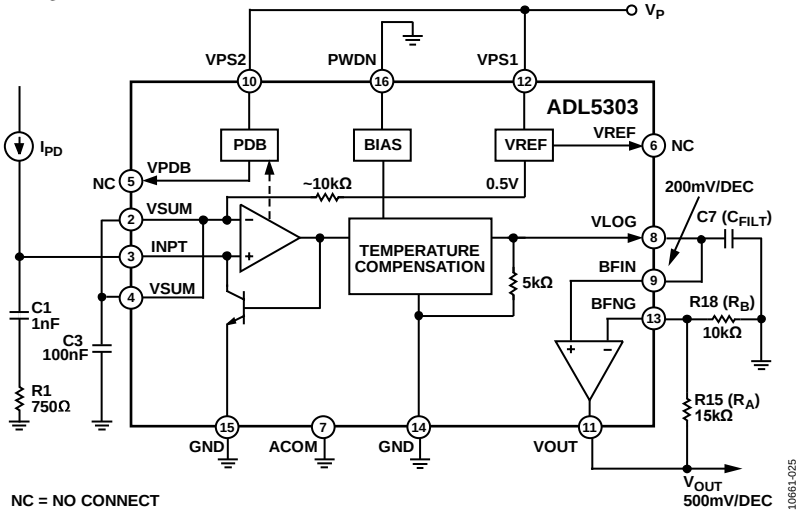


Figure 25. Basic Connections (R15, R18, C7 are Optional; R1 and C1 are the Default Values)

A wide range of gains may be used and the resistor magnitudes are not critical; their parallel sum should be about equal to the net source resistance at the noninverting input. When high gains are used, the output dynamic range is reduced; for a maximum swing of 4.8 V, it amounts to 4.8 V/V_Y decades. Thus, using a ratio of 3×, to set up a slope 30 mV/dB (600 mV/decade), eight decades can be handled, whereas with a ratio of 5×, which sets up a slope of 50 mV/dB (1 V/decade), the dynamic range is 4.8 decades, or 96 dB. When using a lower supply voltage, the calculation proceeds in the same way, remembering to first subtract 0.2 V to allow for 0.1 V upper and lower headroom in the output swing.

Alteration of the logarithmic intercept is only slightly more tricky. First, note that it is rarely necessary to lower the intercept below a value of 100 pA, because this merely raises all output voltages further above ground. However, where this is required, the first step is to raise the voltage, V_{LOG}, by connecting a resistor, R_Z, from VLOG to VREF (2 V) as shown in Figure 26.

This has the effect of elevating, V_{LOG}, for small inputs while lowering the slope to some extent because of the shunt effect of R_Z on the 5 kΩ output resistance. If necessary, the slope may be increased as before, using a feedback attenuator around the buffer. Table 5 lists some examples of lowering the intercept combined with several slope variations.

Table 5. Examples of Lowering the Intercept

V_Y (mV/decade)	I_Z (pA)	R_A (kΩ)	R_B (kΩ)	R_Z (kΩ)
200	1	20.0	100	25
200	10	10.0	100	50
200	50	3.01	100	165
300	1	10.0	12.4	25
300	10	8.06	12.4	50
300	50	6.65	12.4	165
400	1	11.5	8.2	25
400	10	9.76	8.2	50
400	50	8.66	8.2	165
500	1	16.5	8.2	25
500	10	14.3	8.2	50
500	50	13.0	8.2	165

Use the following equation with Table 5:

$$V_{OUT} = G\left[V_Y \times \frac{R_Z}{R_Z + R_{LOG}} \times \log_{10}\left(\frac{I_{PD}}{I_Z}\right) + V_{REF} \times \frac{R_{LOG}}{R_{LOG} + R_Z}\right] \quad (9)$$

where $G = 1 + R_A/R_B$ and $R_{LOG} = 5$ kΩ.

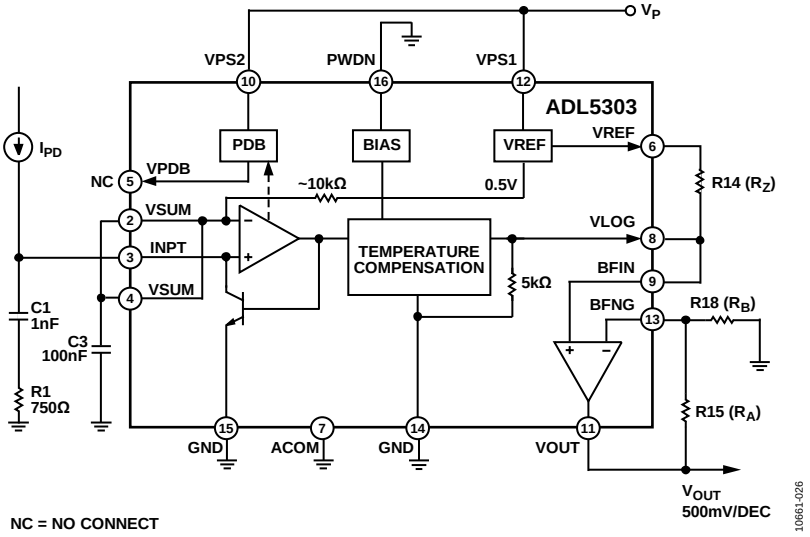


Figure 26. Method for Lowering the Intercept

Generally, it is useful to raise the intercept. Keep in mind that this moves the V_{LOG} line in Figure 26 to the right, lowering all output values. Figure 27 shows how raising the intercept is achieved. The feedback resistors, R_A and R_B, around the buffer are now augmented with a third resistor, R_Z, placed between the BFNG and VREF pins. Adding a third resistor raises the zero-signal voltage on BFNG, which has the effect of pushing V_{OUT} lower. Note that the addition of the R_Z resistor also alters the feedback ratio. However, this change in feedback ratio is readily compensated in the design of the network. Table 6 lists the resistor values for representative intercepts.

Table 6. Examples of Raising the Intercept

V_Y (mV/decade)	I_Z (nA)	R_A (kΩ)	R_B (kΩ)	R_C (kΩ)
300	10	7.5	37.4	24.9
300	100	8.25	130	18.2
400	10	10	16.5	25.5
400	100	9.76	25.5	16.2
400	500	9.76	36.5	13.3
500	10	12.4	12.4	24.9
500	100	12.4	16.5	16.5
500	500	11.5	20.0	12.4

Use the following equation with Table 6:

$$V_{OUT} = G\left[V_Y \times \log_{10}\left(\frac{I_{PD}}{I_Z} \right) - V_{REF} \times \frac{R_A \| R_B}{R_A \| R_B + R_C} \right] \quad (10)$$

where $G = 1 + \frac{R_A}{R_B \| R_C}$ and $R_A \| R_B = \frac{R_A \times R_B}{R_A + R_B}$.

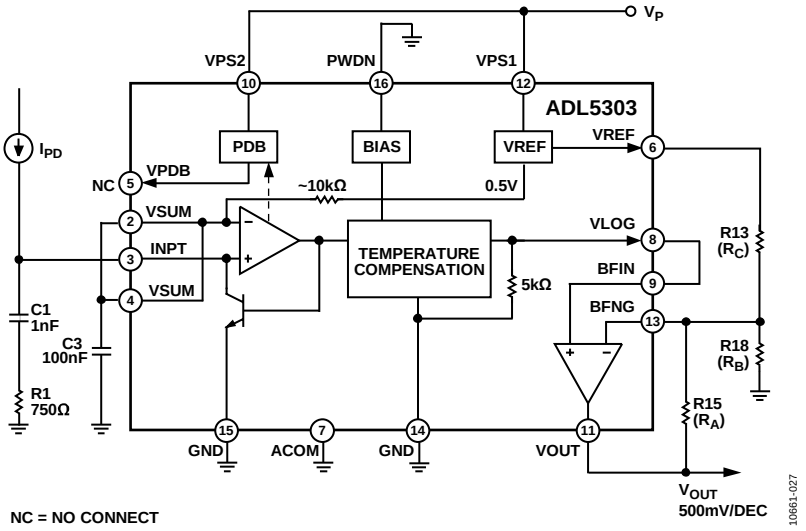


Figure 27. Method for Raising the Intercept

LOW SUPPLY SLOPE AND INTERCEPT ADJUSTMENT

When using the device with a supply of less than 4 V, it is necessary to reduce the slope and intercept at the VLOG pin to preserve good log conformance over the entire 160 dB operating range. The voltage at the VLOG pin is generated by an internal current source with an output current of 40 μA/decade feeding the internal laser trimmed output resistance of 5 kΩ. When the voltage at the VLOG pin exceeds V_P − 2.3 V, the current source ceases to respond linearly to logarithmic increases in current. Avoid headroom issues by reducing the logarithmic slope and intercept at the VLOG pin and by connecting an external resistor, R_S, from the VLOG pin to ground in combination with an intercept lowering resistor, R_Z. The values shown in Figure 28 illustrate a good solution for a 3.0 V positive supply. The resulting logarithmic slope measured at VLOG is 62.5 mV/decade with a new intercept of 57 fA. The original logarithmic slope of 200 mV/decade can be recovered using voltage gain on the internal buffer amplifier.

CHANGING THE VOLTAGE AT THE SUMMING NODE

The default value of VSUM is determined by using a quarter of VREF (2 V). This can be altered by applying an independent voltage source to VSUM, or by adding an external resistive divider from VREF to VSUM. This network operates in parallel with the internal divider (40 kΩ and 13.3 kΩ), and the choice of external resistors should take this into account. In practice, the total resistance of the added string may be as low as 10 kΩ (consuming 400 μA from VREF). Low values of VSUM and thus V_{CE} are not advised when large values of I_{PD} are expected.

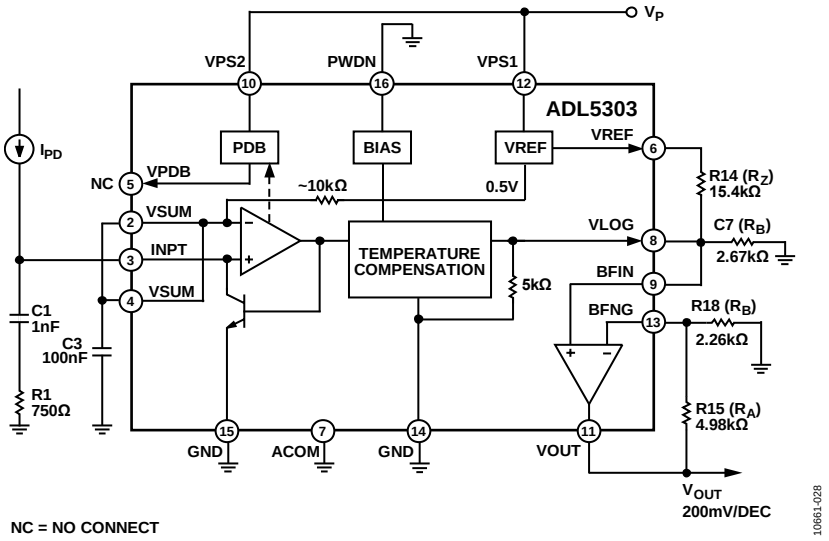


Figure 28. Recommended Low Supply Application Circuit

USING THE ADAPTIVE BIAS

For most photodiode applications, the placement of the anode somewhat above ground is acceptable, as long as the positive bias on the cathode is adequate to support the peak current for a particular diode, limited mainly by its series resistance. To address this matter, the ADL5303 provides for a diode bias that increases linearly with the current. This bias voltage appears at the VPDB pin, and varies from 0.6 V (reverse-biasing the diode by 0.1 V) for I_{PD} = 100 pA and rises to 2.6 V (for a diode bias of 2 V) at I_{PD} = 10 mA. This results in a constant internal junction bias of 0.1 V when the series resistance of the photodiode is 200 Ω. For optical power measurements over a wide dynamic range, the adaptive biasing function is valuable in minimizing dark current while preventing the loss of photodiode bias at high currents. Use of the adaptive bias feature is shown in Figure 29.

Capacitor CPB, between the photodiode cathode at the VPDB pin and ground, is included to lower the impedance at this node and thereby improve the high frequency accuracy at current levels where the ADL5303 bandwidth is high. CPB also ensures a high frequency path for any high frequency modulation on the optical signal, which might not otherwise be accurately averaged. CPB is not necessary in all cases, and experimentation may be required to find an optimum value.

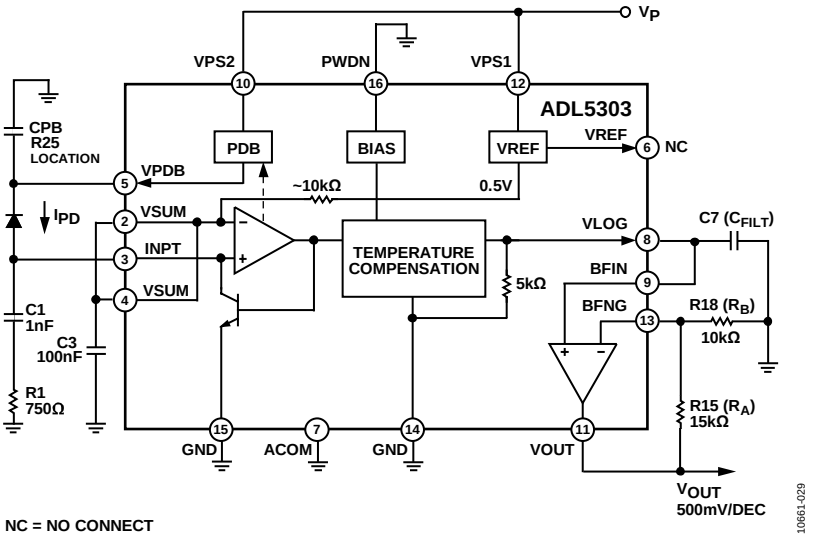


Figure 29. Using the Adaptive Biasing

APPLICATIONS INFORMATION

Smaller input voltages can be measured accurately when aided by a small offset nulling voltage applied to VSUM. The minimum voltage that can be accurately measured is limited only by the drift in the input offset of the ADL5303. The specifications show the maximum spread over the full temperature and supply range. Over a limited temperature range and with a regulated supply, the offset drift is lower; in this situation, processing of inputs down to 5 mV is practicable.

RESCALING

The use of a much larger value for the intercept may be useful in certain situations. In this example, it has been moved up four decades, from the default value of 100 pA to the center of the full eight-decade range at 1 mA. Using a voltage input as previously described, this corresponds to an altered voltage mode intercept, V_Z, which is 1 V for R_{IN} = 1 MΩ. To take full advantage of the larger output swing, the gain of the buffer has been increased to 4.53, resulting in a scaling of 900 mV/decade and a full-scale output of ±3.6 V.

INVERTING THE SLOPE

The buffer is essentially an uncommitted op amp that can be used to support the operation of the ADL5303 in a variety of ways. It can be completely disconnected from the signal chain when not needed. Figure 30 shows its use as an inverting amplifier; this changes the polarity of the slope. The output can be repositioned to a positive value by applying a fraction of V_{REF} to the BFIN pin. The full design for a practical application is left undefined in this brief illustration, but a few cases are discussed, as follows.

For example, if slope of −30 mV/dB is needed; a gain of 3 is required. Because VLOG exhibits a source resistance of 5 kΩ, R_A must be 15 kΩ. A positive offset, V_{OS}, is applied to the BFIN pin, as indicated in Figure 30. The resulting output voltage can be expressed as

$$V_{OUT} = -\left(\frac{R_A}{5\,\text{k}\Omega}\right) V_Y \times \log_{10}\left(\frac{I_{PD}}{I_Z}\right) + V_{OS} \quad (11)$$

When the gain is set to 13 (R_A = 5 kΩ), the 2 V V_{REF} can be tied directly to BFIN, in which case the starting point for the output response is at 4 V. However, because the slope in this case is only −0.2 V/decade, the full current range takes the output down by only 1.6 V. Clearly, a higher slope (or gain) is desirable; in which case, set V_{OS} to a smaller voltage to avoid railing the output at low currents. If V_{OS} = 1.2 V and G = 33, VOUT now starts at 4.8 V and falls through this same voltage toward ground with a slope of −0.6 V per decade, spanning the full range of I_{PD}.

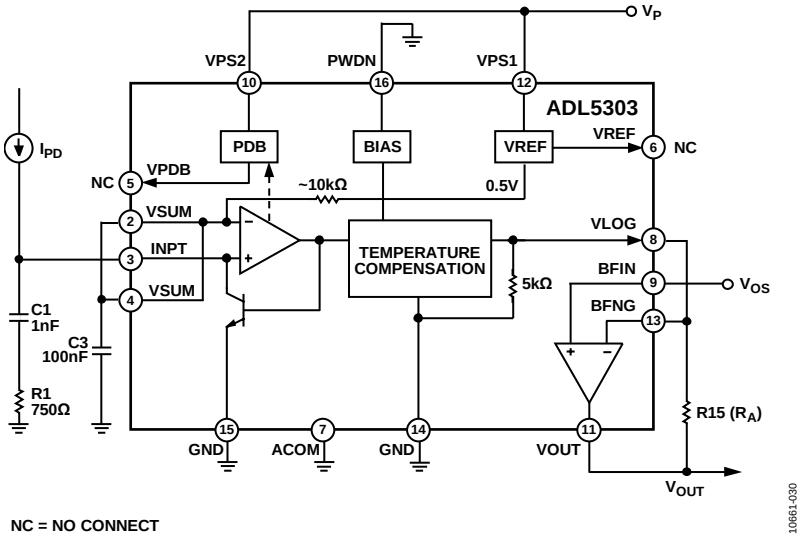


Figure 30. Using the Buffer to Invert the Polarity of the Slope

EVALUATION BOARD

An evaluation board is available for the ADL5303, the schematic for which is shown in Figure 31, and the board layout is shown in Figure 32 and Figure 33. It can be configured for a wide variety of experiments. The board is factory set for photoconductive mode with a buffer gain of 2.5, providing a V_{LOG} slope of 10 mV/dB and an intercept of 100 pA. By substituting resistor and capacitor values, all of the application circuits presented in this data sheet can be evaluated.

The system is completed by the final buffer amplifier, which is an uncommitted op amp with a rail-to-rail output capability, a 10 MHz bandwidth, and good load driving capabilities. The buffer can be used to implement multipole low-pass filters for noise reduction. The buffer also facilitates modification of the output scaling and the intercept point using simple resistor divider networks and the 2 V output provided by the VREF pin.

SHIELDS AND GUARDS

Reducing errors from external sources in a current sensing circuit requires a different approach then the voltage sensing input of the typical high impedance op amp circuit. Leakage can be a significant source of error for highly sensitive log amps, especially at the low end of their range. For example, a 1 GΩ leakage path to ground from the INPT input with a V_{SUM} set to the default 0.5 V generates a 0.5 nA offset. The ADL5303 evaluation board makes extensive use of guards to reduce the effects of leakage at low input levels. It is important to carefully handle and clean the ADL5303 evaluation board to prevent contaminants from handling or improper washing of the PCB causing leakage currents. Circuit board designs for the ADL5303 must connect the EPAD to the VSUM pins to provide a continuous guard around the sensitive INPT pin to reduce the influence of surface contaminants.

A common mistake for those unfamiliar with low level current sensing is to attach a high impedance scope probe or meter to measure the input for debug. This can cause significant error, as the typical 1M ~ 100 MΩ impedance of these probes sources/sinks current from the input, depending on their bias.

In instrumentation applications where measurements <1 nA are required, the use of triaxial cables and connectors is common to reduce leakage through the insulating dielectric by carrying a continuous guard from current source to sensing circuit on the intermediate conductor. This type of guarding circuit is different from a conventional electrostatic shield used in voltage sensing applications. An electrostatic shield relies on low impedance and the ability to flow current freely to minimize voltage induced on the shield that can capacitively couple into a high impedance input. A guard is actively driven to the same voltage as the current carrying center conductor eliminating leakage through the dielectric between the center conductor and the guard. The guard does not flow current other than the leakage from the guard to the outer shield. The guard is usually connected to a single end of the cable only because any significant current flow through the guard can couple inductively to the center conductor. Using the ADL5303 evaluation board, the guard can be driven either from the guard of an external current source or from the internal VSUM bias of the ADL5303.

The ADL5303 evaluation board can bias the shield of a coaxial cable connected to the INPT input to the nominal V_{SUM} voltage with Switch S1 but this requires careful consideration of the environment on the other side of the cable. For example if the ADL5303 evaluation board is configured for V_{SUM} = 0.5 V connecting the other end of the INPT coaxial cable to an instrument with a ground referenced shield pulls V_{SUM} to ground and collapses the input stage of the ADL5303. Floating the current source end of the shield provides a low leakage guard but a separate return path for the signal current must then be provided. If cable dielectric leakage is not a concern, the INPT can be connected directly to a coaxial cable with the shield providing a signal ground.

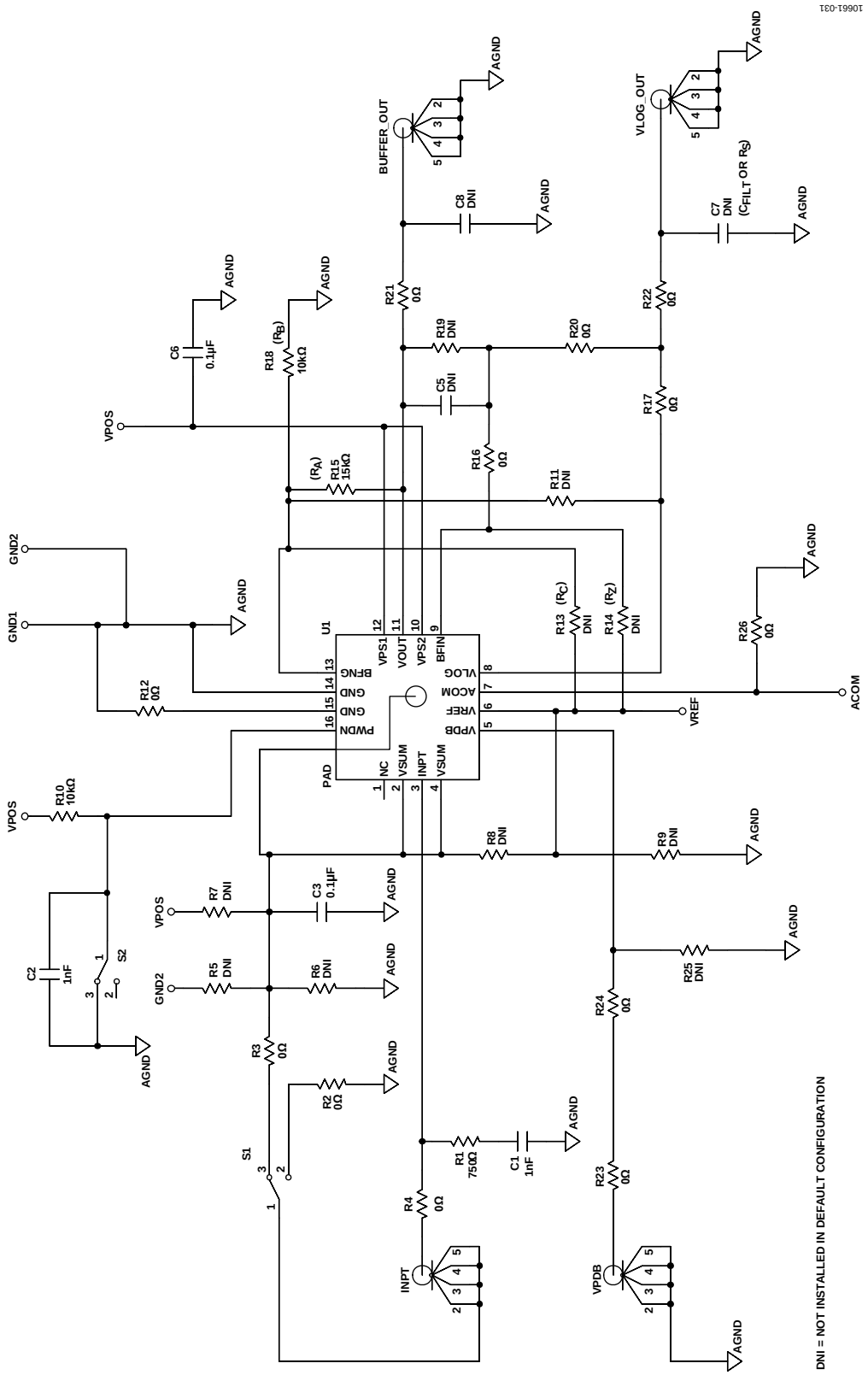


Figure 31. Schematic

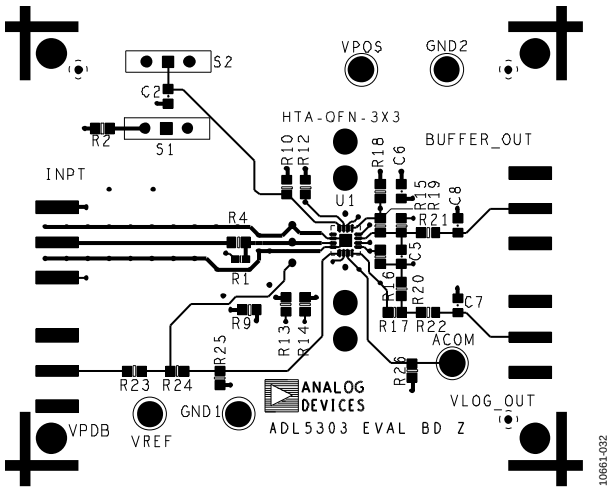


Figure 32. Component Side Layout

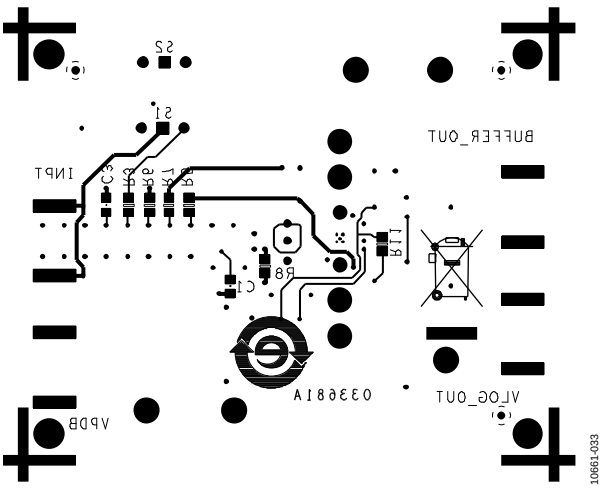


Figure 33. Component Side Silkscreen

Table 7. Evaluation Board Configuration Options

Component	Function	Default Condition
VPOS, AGND	Positive supply and ground pins.	
S1	Device enable. When S1 is in the 0 position, the PWDN pin is connected to ground and the ADL5303 is in its normal operating mode.	S1 = installed
S2	Guard/shield options. The shells of the SMA connectors used for the input and the photodiode bias can be set to the voltage on the VSUM pin or connected to ground. When S2 is in the 0 position, the SMA shell is connected to VSUM.	S2 = installed
R13 (R_C), R14 (R_Z)	Intercept adjustment. A dc offset can be applied to the input terminals of the buffer amplifier to adjust the effective logarithmic intercept.	R13 = open (Size 0603) R14 = open (Size 0603)
R5, R6, R7, R8, R9	Bias adjustment. The voltage on the VSUM and INPT pins can be altered using appropriate resistor values.	R5, R6, R7 = open (Size 0603) R8, R9 = open (Size 0603)
R15 (R_A), R18 (R_B)	Slope adjustment.	R15 = 15 kΩ (Size 0603) R18 = 10 kΩ (Size 0603)
C3	VSUM decoupling capacitor.	C3 = 0.1 µF (Size 0603)
C6	Supply decoupling capacitor.	C6 = 0.1 µF (Size 0603)
R25 (CPB)	Photodiode bias decoupling. Provides high frequency decoupling.	R25 = open (Size 0603)
C5, C7 (C_{FILT} or R_S), C8, R11, R16, R17, R19, R20	Output filtering. Allows implementation of a variety of filter configurations, from simple RC low-pass filters to three-pole Sallen-Key filters.	R11, R19, C5 = Open (Size 0603) R16, R17, R20 = 0 Ω (Size 0603) C7, C8 = Open (Size 0603)
R1, C1	Input filtering. Provides essential HF compensation at the input pin, INPT.	R1 = 750 Ω (Size 0402) C1 = 1 nF (Size 0603)
R2, R3, R4, R23, R24, R21, R22, R12, R26	Isolation jumpers.	All = 0 Ω (Size 0603)

OUTLINE DIMENSIONS

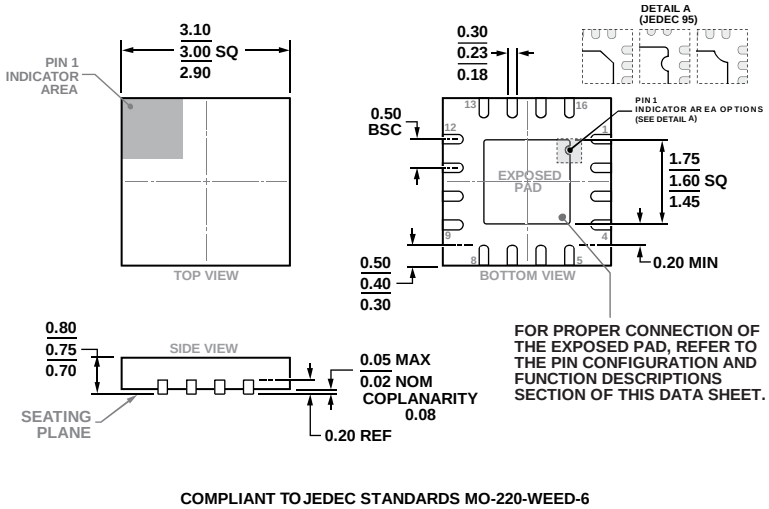


Figure 34. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Marking Code	Ordering Quantity
ADL5303ACPZ-R2	−40°C to +85°C	16-Lead LFCSP	CP-16-22	H38	250
ADL5303ACPZ-R7	−40°C to +85°C	16-Lead LFCSP, 7″ Tape and Reel	CP-16-22	H38	1500
ADL5303ACPZ-RL	−40°C to +85°C	16-Lead LFCSP, 13″ Tape and Reel	CP-16-22	H38	5000
ADL5303-EVALZ		Evaluation Board			

[1] Z = RoHS Compliant Part.

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