20 MHz to 500 MHz IF Gain Block

Data Sheet **ADL5531**

FEATURES

- **Fixed gain of 20 dB**
- **Operation up to 500 MHz**
- **Input/output internally matched to 50 Ω**
- **Integrated bias control circuit**
- **Output IP3**
  - **41 dBm at 70 MHz**
  - **39 dBm at 190 MHz**
- **Output 1 dB compression: 20.6 dB at 190 MHz**
- **Noise figure: 2.5 dB at 190 MHz**
- **Single 5 V power supply**
- **Small footprint 8-lead LFCSP**
- **ADL5534 20 dB gain dual-channel version**
- **±2 kV ESD (Class 2)**

FUNCTIONAL BLOCK DIAGRAM

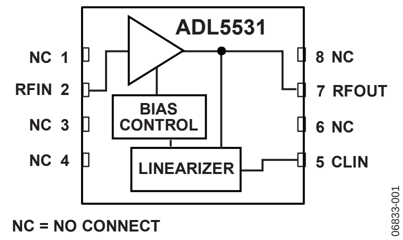

Figure 1.

GENERAL DESCRIPTION

The ADL5531 is a broadband, fixed-gain, linear amplifier that operates at frequencies up to 500 MHz. The device can be used in a wide variety of equipment, including cellular, satellite, broadband, and instrumentation equipment.

The ADL5531 provides a gain of 20 dB, which is stable over frequency, temperature, power supply, and from device to device. This amplifier is single ended and internally matched to 50 Ω. Only input/output ac coupling capacitors, power supply decoupling capacitors, and external inductors are required for operation.

The ADL5531 is fabricated on a GaAs HBT process and has an ESD rating of ±2 kV (Class 2). The device is packaged in an 8-lead 3 mm × 3 mm LFCSP that uses an exposed paddle for excellent thermal impedance.

The ADL5531 consumes 100 mA on a single 5 V supply and is fully specified for operation from −40°C to +85°C.

The dual-channel 20 dB gain version, ADL5534, is also available from Analog Devices, Inc.

Rev. C **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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REVISION HISTORY

8/2017—Rev. B to Rev. C

Changed CP-8-2 to CP-8-13 .... Throughout
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11/2013—Rev. A to Rev. B

Changes to Figure 2 6
Added Figure 14, Renumbered Sequentially 8

8/2008—Rev. 0 to Rev. A

Changes to Features Section and General Description Section 1
Added Exposed Pad Notation to Outline Dimensions 11

8/2007—Revision 0: Initial Version

SPECIFICATIONS

VPOS = 5 V and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		20		500	MHz
Gain (S21)	190 MHz		20.3		dB
Input Return Loss (S11)	190 MHz		−19.5		dB
Output Return Loss (S22)	190 MHz		−26.5		dB
Reverse Isolation (S12)	190 MHz		−23.0		dB
FREQUENCY = 70 MHz					
Gain			20.9		dB
vs. Frequency	± 5 MHz		±0.03		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.22		dB
vs. Supply	4.75 V to 5.25 V		±0.19		dB
Output 1 dB Compression Point			20.4		dBm
Output Third-Order Intercept	Δf = 1 MHz, output power (P_{OUT}) = 0 dBm per tone		41.0		dBm
Noise Figure			2.5		dB
FREQUENCY = 190 MHz					
Gain		19.7	20.3	21.0	dB
vs. Frequency	± 50 MHz		±0.12		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.22		dB
vs. Supply	4.75 V to 5.25 V		±0.17		dB
Output 1 dB Compression Point			20.6		dBm
Output Third-Order Intercept	Δf = 1 MHz, output power (P_{OUT}) = 0 dBm per tone		39.0		dBm
Noise Figure			2.5		dB
FREQUENCY = 380 MHz					
Gain		19.2	19.7	20.5	dB
vs. Frequency	± 50 MHz		±0.15		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.24		dB
vs. Supply	4.75 V to 5.25 V		±0.15		dB
Output 1 dB Compression Point			20.4		dBm
Output Third-Order Intercept	Δf = 1 MHz, output power (P_{OUT}) = 0 dBm per tone		36.0		dBm
Noise Figure			3.0		dB
POWER INTERFACE	Pin RFOUT				
Supply Voltage		4.75	5	5.25	V
Supply Current			100	110	mA
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±15		mA
Power Dissipation	VPOS = 5 V		0.5		W

TYPICAL SCATTERING PARAMETERS

VPOS = 5 V and T_A = 25°C. The effects of the test fixture have been de-embedded up to the pins of the device.

Table 2.

Frequency (MHz)	S11		S21		S12		S22	
	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)
20	−19.9933	−132.614	21.99753	173.7349	−24.2574	4.854191	−19.1444	−46.7161
50	−19.6622	−151.093	21.20511	170.3258	−23.4894	5.603544	−21.4752	−89.9497
100	−17.9244	−166.031	20.83152	167.5595	−23.22	6.119636	−23.0386	−115.741
150	−18.4041	−177.116	20.67117	164.1871	−23.0914	6.631844	−23.335	−119.722
200	−18.6386	+179.6269	20.56097	160.4721	−22.9921	7.784913	−22.8555	−115.855
250	−19.2303	+175.3384	20.45422	156.5272	−22.9219	8.763143	−21.6619	−111.307
300	−19.4456	+175.0622	20.34563	152.4398	−22.8475	9.908631	−20.2707	−106.681
350	−20.1783	+173.422	20.21365	148.3008	−22.7662	11.21706	−18.7007	−104.369
400	−20.2409	+174.1593	20.07116	144.2311	−22.665	12.36953	−17.1242	−103.565
450	−20.7266	+175.6233	19.90932	140.0789	−22.5569	13.57857	−15.726	−103.863
500	−20.6064	+175.853	19.72779	135.9952	−22.4519	14.73385	−14.41	−105.079

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage on RFOUT	5.5 V
Input Power on RFIN	10 dBm
Internal Power Dissipation (Paddle Soldered)	600 mW
θ_{JA} (Junction to Air)	103°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
ESD Rating—Human Body Model	±2 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

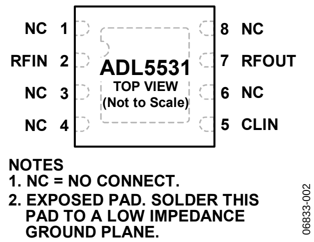

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 4, 6, 8	NC	No Connect.
2	RFIN	RF Input. Requires a 10 nF dc blocking capacitor.
5	CLIN	A 1 nF capacitor connected between Pin 5 and ground provides decoupling for the on-board linearizer.
7	RFOUT	RF Output and Bias. DC bias is provided to this pin through a 470 nH inductor (Coilcraft 1008CS-471XJLC or equivalent). The RF path requires a 10 nF dc blocking capacitor.
EP	Exposed Pad	GND. Solder this pad to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

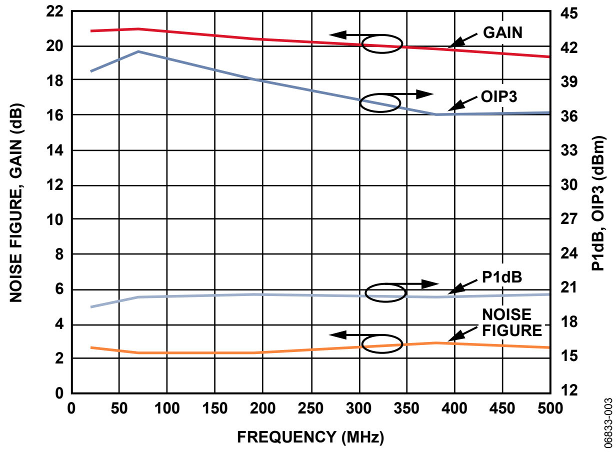

Figure 3. Noise Figure, Gain, P1dB, and OIP3 vs. Frequency

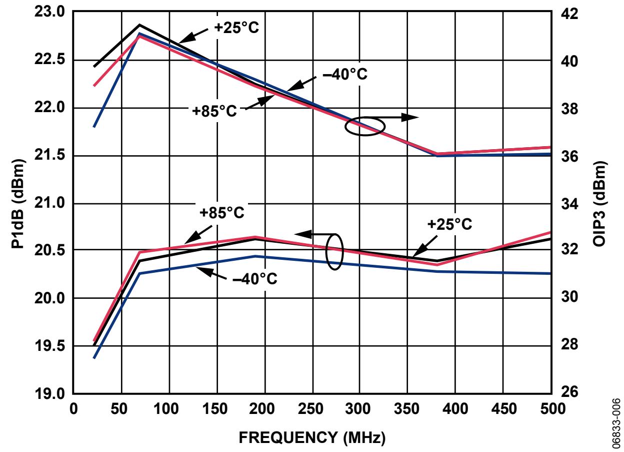

Figure 6. P1dB and OIP3 vs. Frequency and Temperature

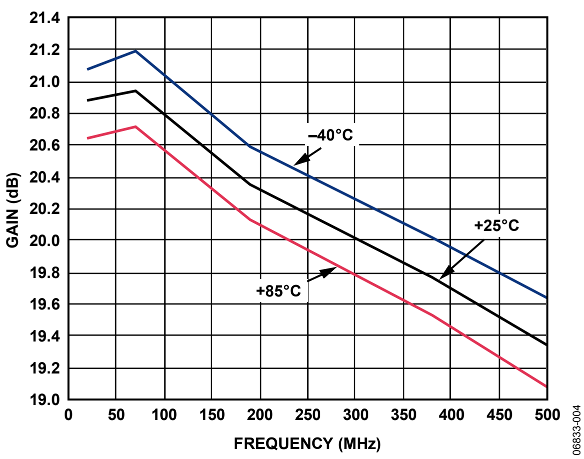

Figure 4. Gain vs. Frequency and Temperature

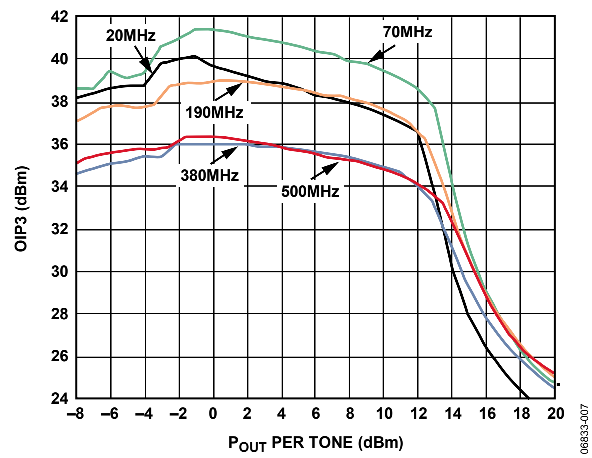

Figure 7. OIP3 vs. Output Power (P_{OUT}) and Frequency

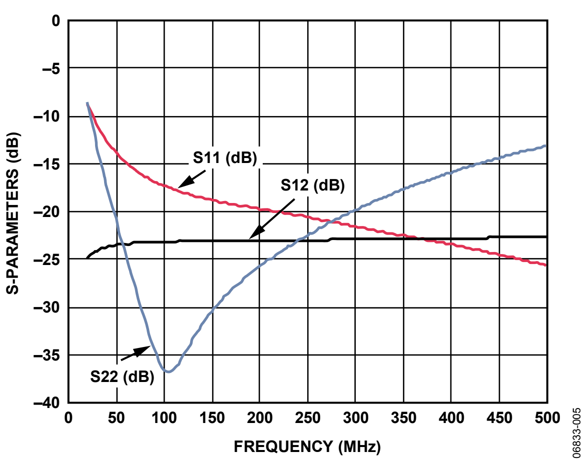

Figure 5. Input Return Loss (S11), Reverse Isolation (S12), and Output Return Loss (S22) vs. Frequency

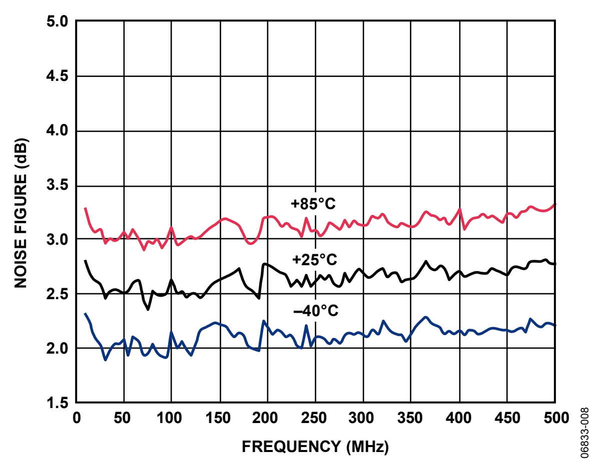

Figure 8. Noise Figure vs. Frequency and Temperature

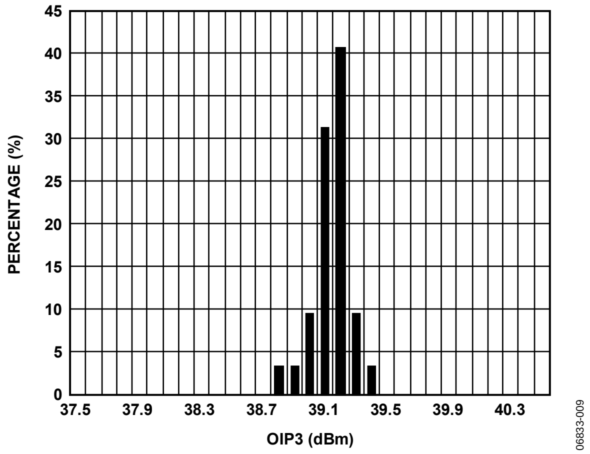

Figure 9. OIP3 Distribution at 190 MHz

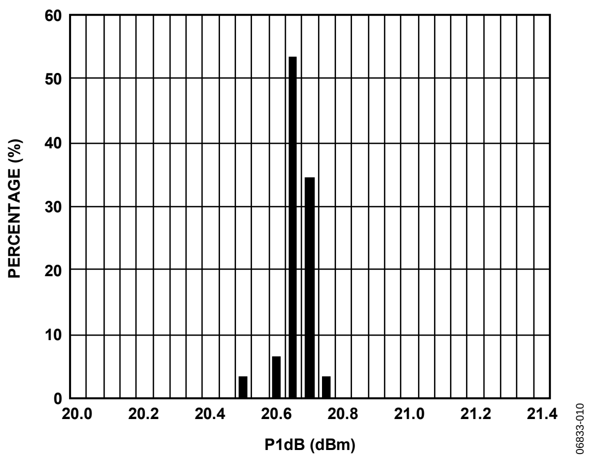

Figure 10. P1dB Distribution at 190 MHz

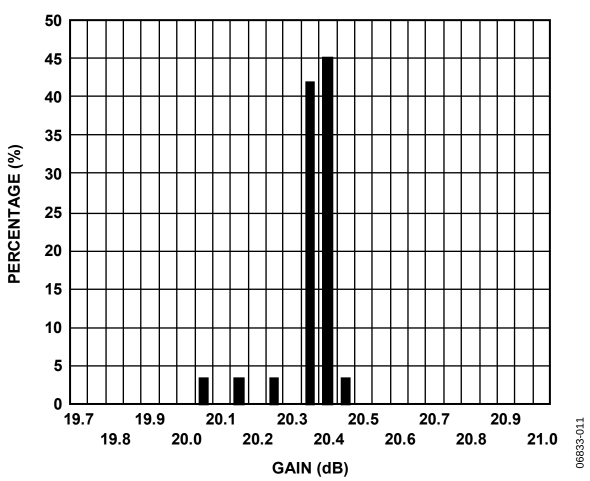

Figure 11. Gain Distribution at 190 MHz

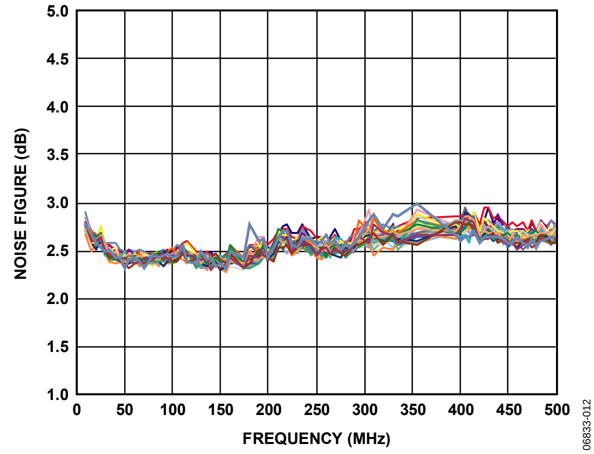

Figure 12. Noise Figure vs. Frequency at 25°C, Multiple Devices Shown

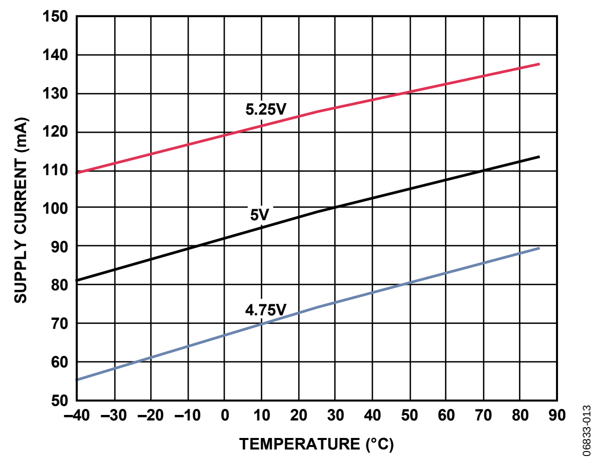

Figure 13. Supply Current vs. Supply Voltage and Temperature

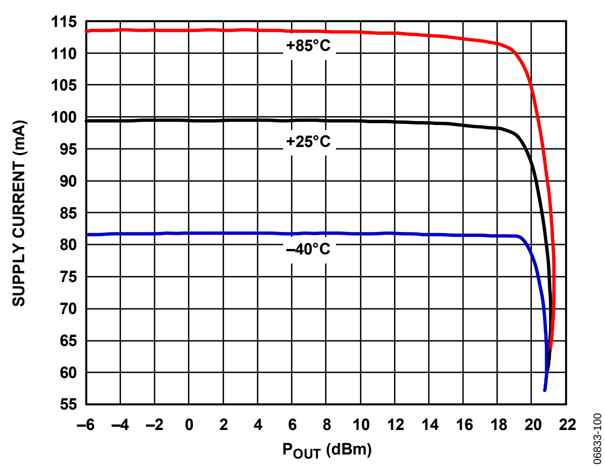

Figure 14. Supply Current vs. P_{OUT} and Temperature

BASIC CONNECTIONS

The basic connections for operating the ADL5531 are shown in Figure 16. The input and output are ac-coupled with 10 nF (0402) capacitors. DC bias is provided to the amplifier via an inductor (Coilcraft 1008CS-471XJLC or equivalent) connected to the RFOUT pin. The bias voltage should be decoupled using 10 nF and 1 µF capacitors.

SOLDERING INFORMATION AND RECOMMENDED PCB LAND PATTERN

Figure 15 shows the recommended land pattern for ADL5531. To minimize thermal impedance, the exposed pad on the package underside is soldered down to a ground plane. If multiple ground layers exist, they are stitched together using vias (a minimum of five vias is recommended). Pin 1, Pin 3, Pin 4, Pin 6, and Pin 8 can be left unconnected or can be connected to ground. Connecting these pins to ground slightly enhances thermal impedance. For more information on land pattern design and layout, refer to AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

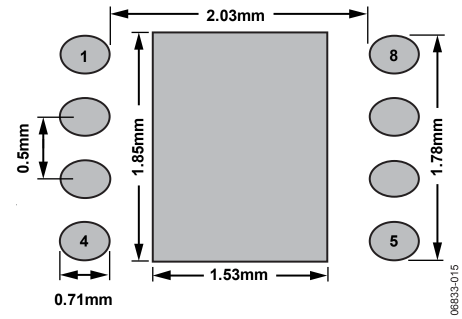

Figure 15. Recommended Land Pattern

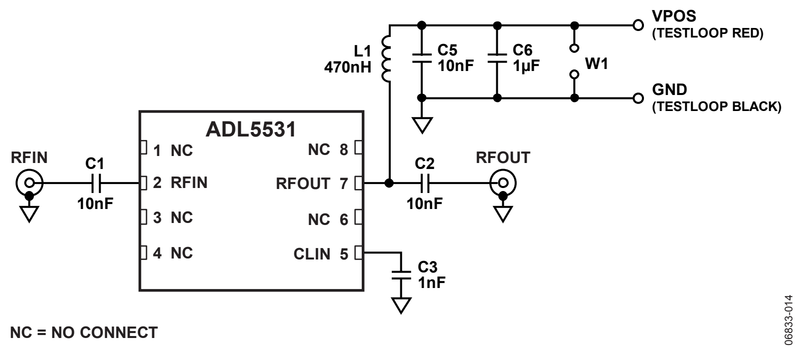

Figure 16. Basic Connections

EVALUATION BOARD

Figure 19 shows the schematic for the ADL5531 evaluation board. The board is powered by a single 5 V supply.

The components used on the board are listed in Table 5. Power can be applied to the board through clip-on leads or through Jumper W1. Note that C4, C7, C8, L3, L4, L5, R1, and R2 have no function.

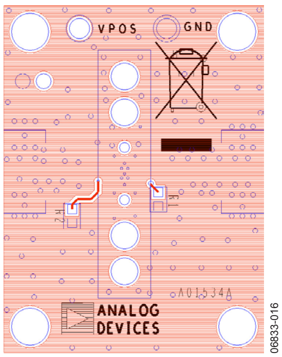

Figure 17. Evaluation Board Layout (Bottom)

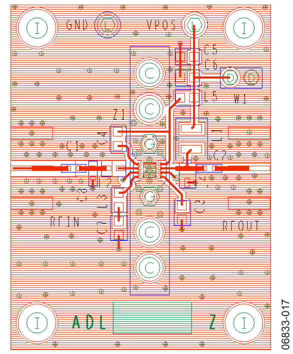

Figure 18. Evaluation Board Layout (Top)

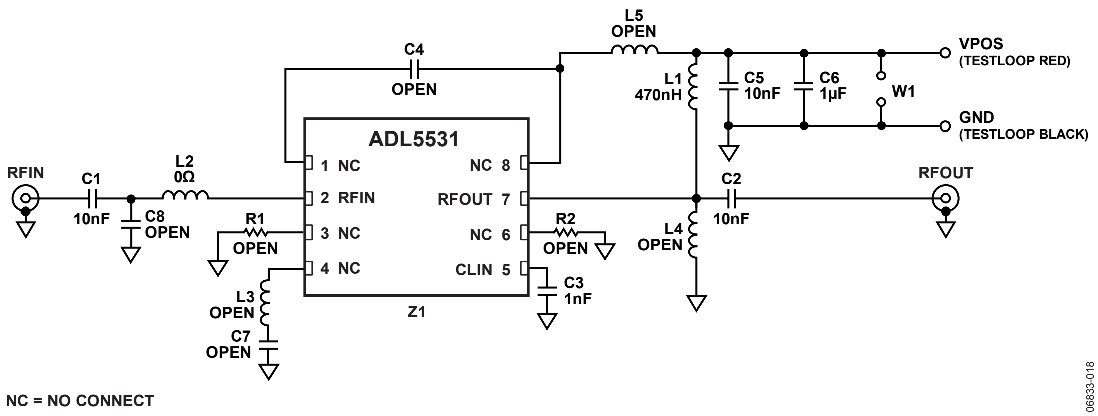

Figure 19. Evaluation Board Schematic

Table 5. Evaluation Board Configuration Options

Component	Function	Default Value
Z1	DUT	ADL5531
C1, C2	AC coupling capacitors	10 nF, 0402
C3	Linearizer capacitor	1 nF, 0603
C5	Power supply decoupling capacitor	10 nF, 0603
C6	Power supply decoupling capacitor	1 µF, 0603
C4, C7, C8		Open
R1, R2		Open
L1	DC bias inductor	470 nH, 1008 (Coilcraft 1008CS-471XJLC or equivalent)
L2		0 Ω, 0402
L3, L4, L5		Open
VPOS, GND	Clip-on terminals for power supply	VPOS, GND
W1	2-pin jumper for connection of ground and supply via cable	W1
RFIN, RFOUT	50 Ω SMA female connectors	RFIN, RFOUT

OUTLINE DIMENSIONS

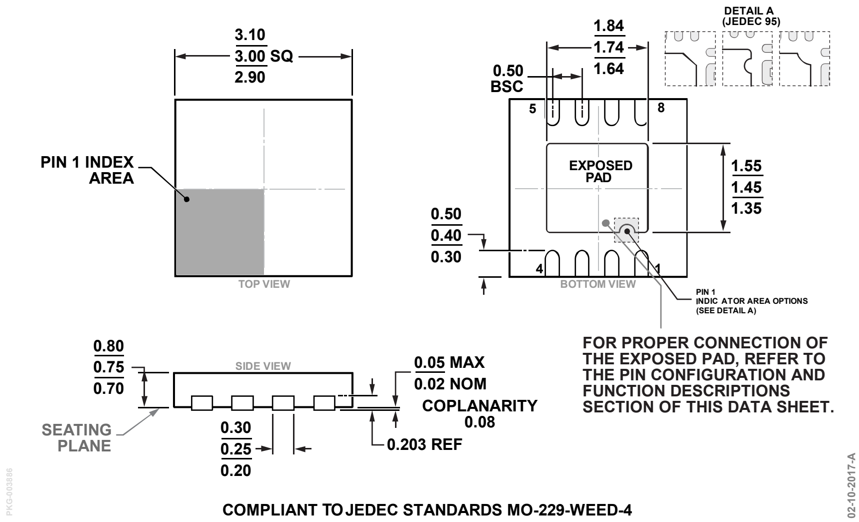

Figure 20. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
CP-8-13
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADL5531ACPZ-R7	−40°C to +85°C	8-Lead LFCSP, 7" Tape and Reel	CP-8-13	Q16
ADL5531-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES