3.0 V to 5.5 V, ±12 kV IEC ESD Protected, 50 Mbps RS-485 Transceivers

Enhanced Product

ADM3065E-EP/ADM3066E-EP/ADM3067E-EP

FEATURES

- TIA/EIA RS-485 compliant over full supply range
- 3.0 V to 5.5 V operating voltage range on V_{CC}
- 1.62 V to 5.5 V V_{IO} logic supply option available
- ESD protection on the bus pins
  - IEC 61000-4-2 ±12 kV contact discharge
  - IEC 61000-4-2 ±15 kV air discharge
  - DO-160 Section 25 ±15 kV air discharge
  - HBM ≥ ±30 kV
- Full hot swap support (glitch free power-up/power-down)
- High speed 50 Mbps data rate
- Full receiver short-circuit, open circuit, and bus idle fail-safe
- PROFIBUS compliant at V_{CC} ≥ 4.5 V
- Half duplex and full duplex models available
- Allows connection of up to 128 transceivers onto the bus
- Space-saving package options
  - 8-lead and 10-lead MSOP
  - 8-lead and 14-lead, narrow-body SOIC

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Extended industrial temperature range: −55°C to +125°C
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Product change notification
- Qualification data available on request

APPLICATIONS

- Industrial fieldbuses
- Process control
- Building automation
- PROFIBUS networks
- Motor control servo drives and encoders

FUNCTIONAL BLOCK DIAGRAMS

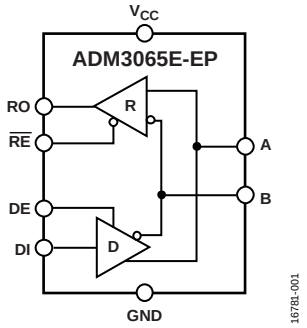


Figure 1. ADM3065E-EP Functional Block Diagram

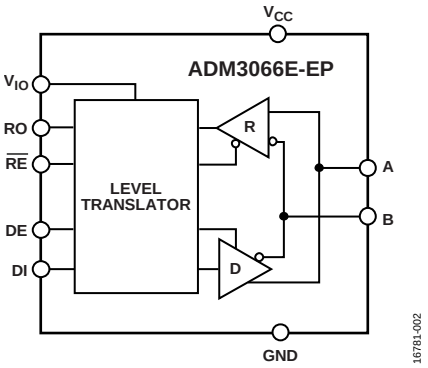


Figure 2. ADM3066E-EP Functional Block Diagram

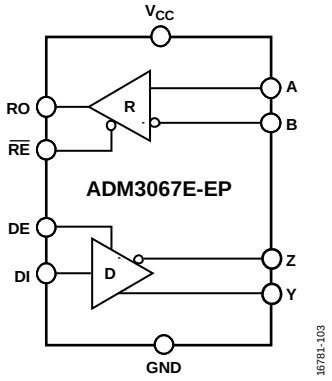


Figure 3. ADM3067E-EP Functional Block Diagram

Rev. 0

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support
www.analog.com

TABLE OF CONTENTS

Features 1
Enhanced Product Features 1
Applications 1
Functional Block Diagrams 1
Revision History 2
General Description 3
Specifications 4
Timing Specifications 5
Absolute Maximum Ratings 8
Thermal Resistance 8
ESD Caution 8
Pin Configurations and Function Descriptions 9
Typical Performance Characteristics 12
Test Circuits 15
Theory of Operation 16
High Speed IEC ESD Protected RS-485 16
DO-160 Section 25 ESD Protection 16
Outline Dimensions 17
Ordering Guide 18

REVISION HISTORY

4/2019—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADM3065E-EP/ADM3066E-EP/ADM3067E-EP are 3.0 V to 5.5 V, IEC electrostatic discharge (ESD) protected RS-485 transceivers, allowing the devices to withstand ±12 kV contact discharges on the transceiver bus pins without latch-up or damage. The ADM3066E-EP features a V_{IO} logic supply pin allowing a flexible digital interface capable of operating as low as 1.62 V.

The ADM3065E-EP/ADM3066E-EP/ADM3067E-EP are suitable for high speed, 50 Mbps, bidirectional data communication on multipoint bus transmission lines. The ADM3065E-EP/ADM3066E-EP/ADM3067E-EP feature a one-fourth unit load input impedance, which allows up to 128 transceivers on a bus.

The ADM3065E-EP/ADM3066E-EP are half-duplex RS-485 transceivers, fully compliant to the PROFIBUS® standard with increased 2.1 V bus differential voltage at $V_{CC} \geq 4.5$ V. The ADM3067E-EP is a full duplex RS-485 transceiver option.

The RS-485 transceivers are available in a number of space-saving packages, such as the 8-lead or 10-lead, 3 mm × 3 mm MSOP; and the 8-lead or 14-lead, narrow-body SOIC packages.

Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. If, during fault conditions, a significant temperature increase is detected in the internal driver circuitry, this feature forces the driver output into a high impedance state.

The ADM3065E-EP/ADM3066E-EP/ADM3067E-EP guarantee a logic high receiver output when the receiver inputs are shorted, open, or connected to a terminated transmission line with all drivers disabled.

Table 1 presents an overview of the ADM3065E-EP/ADM3066E-EP/ADM3067E-EP data rate capability across temperature, power supply, and package options. Refer to the Ordering Guide for model numbering.

Additional application and technical information can be found in the ADM3065E/ADM3066E/ADM3067E data sheet.

Table 1. Summary of the ADM3065E-EP/ADM3066E-EP/ADM3067E-EP Operating Conditions—Data Rate Capability Across Temperature, Power Supply, and Package

Maximum Data Rate[1]	Maximum V_{CC} (V)	Maximum Temperature	Package Description
50 Mbps	5.5	−55°C to +105°C	8-lead SOIC_N, 8-lead MSOP, 10-lead MSOP, and 14-lead SOIC_N
50 Mbps	3.6	−55°C to +125°C	8-lead SOIC_N, 8 lead MSOP, 10 lead MSOP, and 14-lead SOIC_N

[1] The ADM3065E-EP/ADM3066E-EP/ADM3067E-EP data input (DI) is transmitting 50 Mbps clock data, and the ADM3065E-EP/ADM3066E-EP/ADM3067E-EP driver enable (DE) is enabled for 50% of the DI transmit time.

SPECIFICATIONS

V_{CC} = 3.0 V to 5.5 V, V_{IO} = 1.62 V to V_{CC} (ADM3066E-EP), V_{IO} = V_{CC} for the ADM3065E-EP and ADM3067E-EP, T_A = T_{MIN} (−55°C) to T_{MAX} (+125°C), unless otherwise noted. All typical specifications are at T_A = 25°C, V_{IO} = V_{CC} = 3.3 V, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY						
No Load Supply Current	I_{CC}		2	7.5	mA	DE = V_{IO}, $\overline{RE}$ = 0 V
				7.5	mA	DE = V_{IO}, $\overline{RE}$ = V_{IO}
				4.5	mA	DE = 0 V, $\overline{RE}$ = 0 V
Supply Current, Data Rate = 50 Mbps			107	172	mA	V_{CC} > 4.5 V, load resistance (R_L) = 54 Ω, DE = V_{IO}, $\overline{RE}$ = 0 V
			67	75	mA	R_L = 54 Ω, DE = V_{IO}, $\overline{RE}$ = 0 V (V_{CC} = 3.0 V)
Supply Current in Shutdown Mode	I_{SHDN}		210	450	µA	DE = 0 V, $\overline{RE}$ = V_{IO}
ADM3066E-EP V_{IO} Shutdown Current	I_{IOSHDN}		1	50	µA	DE = 0 V, $\overline{RE}$ = V_{IO}
DRIVER						
Differential Outputs						
Output Voltage, Loaded	$\lvert V_{OD2}\rvert$	2.0		V_{CC}	V	V_{CC} ≥ 3.0 V, R_L = 50 Ω, see Figure 29
	$\lvert V_{OD2}\rvert$	1.5		V_{CC}	V	V_{CC} ≥ 3.0 V, R_L = 27 Ω (RS-485), see Figure 29
	$\lvert V_{OD2}\rvert$	2.1		V_{CC}	V	V_{CC} ≥ 4.5 V, R_L = 50 Ω, see Figure 29
	$\lvert V_{OD2}\rvert$	2.1		V_{CC}	V	V_{CC} ≥ 4.5 V, R_L = 27 Ω (RS-485), see Figure 29
	$\lvert V_{OD3}\rvert$	1.5		V_{CC}	V	V_{CC} ≥ 3.0 V, −7 V ≤ common-mode voltage (V_{CM}) ≤ +12 V, see Figure 30
	$\lvert V_{OD3}\rvert$	2.1		V_{CC}	V	V_{CC} ≥ 4.5 V, −7 V ≤ V_{CM} ≤ +12 V, see Figure 30
Change in Differential Input Voltage for Complementary Output States	$\Delta\lvert V_{OD}\rvert$			0.2	V	R_L = 27 Ω or 50 Ω, see Figure 29
Common-Mode Output Voltage	V_{OC}			3.0	V	R_L = 27 Ω or 50 Ω, see Figure 29
Change in Common-Mode Voltage for Complementary Output States	$\Delta\lvert V_{OC}\rvert$			0.2	V	R_L = 27 Ω or 50 Ω, see Figure 29
Output Short-Circuit Current	I_{OS}	−250		+250	mA	−7 V < output voltage (V_{OUT}) < +12 V
ADM3067E-EP Output Leakage (Y, Z) Current	I_O			+100	µA	DE = 0 V, $\overline{RE}$ = 0 V, V_{CC} = 0 V or 3.6 V, input voltage (V_{IN}) = 12 V
		−100			µA	DE = 0 V, $\overline{RE}$ = 0 V, V_{CC} = 0 V or 3.6 V, V_{IN} = −7 V
Logic Inputs (DE, $\overline{RE}$, DI)						
Input Voltage						
Low	V_{IL}			0.33 × V_{IO}	V	DE, $\overline{RE}$, DI, 1.62 V ≤ V_{IO} ≤ 5.5 V
High	V_{IH}	0.67 × V_{IO}			V	DE, $\overline{RE}$, DI, 1.62 V ≤ V_{IO} ≤ 5.5 V
Input Current	I_I	−2		+2	µA	DE, $\overline{RE}$, DI, 1.62 V ≤ V_{IO} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{IO}
RECEIVER						
Differential Inputs						
Differential Input Threshold Voltage	V_{TH}	−200	−125	−30	mV	−7 V < V_{CM} < +12 V
Input Voltage Hysteresis	V_{HYS}		30		mV	−7 V < V_{CM} < +12 V
Input Current (A, B)	I_I			0.25	mA	DE = 0 V, V_{CC} = powered/unpowered, V_{IN} = 12 V
		−0.20			mA	DE = 0 V, V_{CC} = powered/unpowered, V_{IN} = −7 V
Line Input Resistance	R_{IN}	48			kΩ	−7 V ≤ V_{CM} ≤ +12 V
Logic Outputs						
Output Voltage						
Low	V_{OL}			0.4	V	V_{IO} = 3.6 V, output current (I_{OUT}) = 2 mA, V_{ID}[1] ≤ −0.2 V
				0.4	V	V_{IO} = 2.7 V, I_{OUT} = 1 mA, V_{ID}[1] ≤ −0.2 V, ADM3066E-EP only
				0.2	V	V_{IO} = 1.95 V, I_{OUT} = 500 µA, V_{ID}[1] ≤ −0.2 V, ADM3066E-EP only

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
High	V_{OH}	2.4			V	V_{IO} = 3.0 V, I_{OUT} = −2 mA, V_{ID}[1] ≥ −0.03 V
		2.0			V	V_{IO} = 2.3 V, I_{OUT} = −1 mA, V_{ID}[1] ≥ −0.03 V, ADM3066E-EP only
		V_{IO} − 0.2			V	V_{IO} = 1.65 V, I_{OUT} = −500 µA, V_{ID}[1] ≥ −0.03 V, ADM3066E-EP only
Short-Circuit Current				85	mA	V_{OUT} = GND or V_{IO}
Three-State Output Leakage	I_{OZR}			±2	µA	RO = 0 V or V_{IO}

[1] V_{ID} is the receiver input differential voltage.

TIMING SPECIFICATIONS

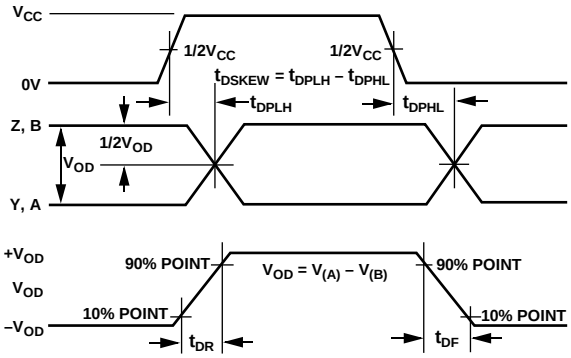
V_{CC} = 3.0 V to 5.5 V, V_{IO} = 1.62 V to V_{CC} (ADM3066E-EP), T_A = T_{MIN} (−55°C) to T_{MAX} (+125°C), unless otherwise noted. All typical specifications are at T_A = 25°C, V_{IO} = V_{CC} = 3.3 V, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate[1]		50			Mbps	
Propagation Delay	t_{DPLH}, t_{DPHL}		9	15	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 4 and Figure 31
Skew	t_{DSKEW}		1	2	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 4 and Figure 31
Rise/Fall Times	t_{DR}, t_{DF}		4	6.7	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 4 and Figure 31
Enable to Output High	t_{DZH}		10	30	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 5 and Figure 32
Enable to Output Low	t_{DZL}		10	30	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 5 and Figure 32
Disable Time from Low	t_{DLZ}		10	30	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 5 and Figure 32
Disable Time from High	t_{DHZ}		10	30	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 5 and Figure 32
Enable Time from Shutdown to High	$t_{DZH(SHDN)}$[2]			2000	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 5 and Figure 32
Enable Time from Shutdown to Low	$t_{DZL(SHDN)}$[2]			2000	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 5 and Figure 32
RECEIVER						
Maximum Data Rate		50			Mbps	
Propagation Delay	t_{RPLH}, t_{RPHL}			35	ns	C_L = 15 pF, $\|V_{ID}\|$ ≥ 1.5 V, V_{CM} = 1.5 V, see Figure 6 and Figure 33
Skew/Pulse Width Distortion	t_{RSKEW}			3.5	ns	C_L = 15 pF, $\|V_{ID}\|$ ≥ 1.5 V, V_{CM} = 1.5 V, see Figure 6 and Figure 33
Enable to Output High	t_{RZH}		10	35	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\|$ ≥ 1.5 V, DE high, see Figure 7 and Figure 35
Enable to Output Low	t_{RZL}		10	35	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\|$ ≥ 1.5 V, DE high, see Figure 7 and Figure 35
Disable Time from Low	t_{RLZ}		10	35	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\|$ ≥ 1.5 V, see Figure 7 and Figure 35
Disable Time from High	t_{RHZ}		10	35	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\|$ ≥ 1.5 V, see Figure 7 and Figure 35
Enable from Shutdown to High	$t_{RZH(SHDN)}$[3]			2000	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\|$ ≥ 1.5 V, see Figure 7 and Figure 34
Enable from Shutdown to Low	$t_{RZL(SHDN)}$[3]			2000	ns	R_L = 1 kΩ, C_L = 15 pF, $\|V_{ID}\|$ ≥ 1.5 V, see Figure 7 and Figure 34
TIME TO SHUTDOWN	t_{SHDN}[4]	40			ns	

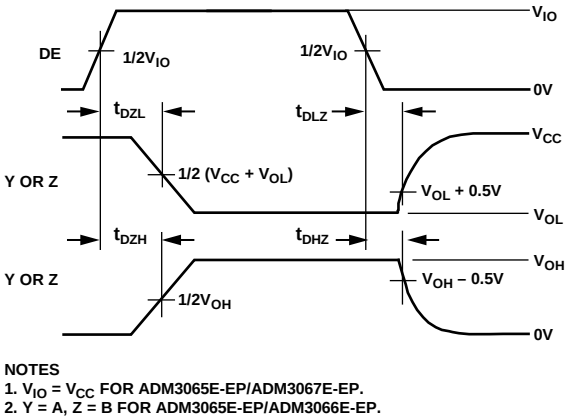
[1] Maximum data rate assumes a ratio of t_{DR}:t_{BIT}:t_{DF} equal to 1:1:1.
[2] $t_{DZH(SHDN)}$ and $t_{DZL(SHDN)}$ refer to the time for the device to enable when DE changes from 0 V to V_{CC}. $\overline{RE}$ = V_{CC} for this condition.
[3] $t_{RZH(SHDN)}$ and $t_{RZL(SHDN)}$ refer to the time for the device to enable when $\overline{RE}$ changes from V_{CC} to 0 V. DE = 0 V for this condition.
[4] Minimum time required to put the device into shutdown: DE and $\overline{RE}$ must be disabled for more than 40 ns for the device to go into shutdown.

Timing Diagrams



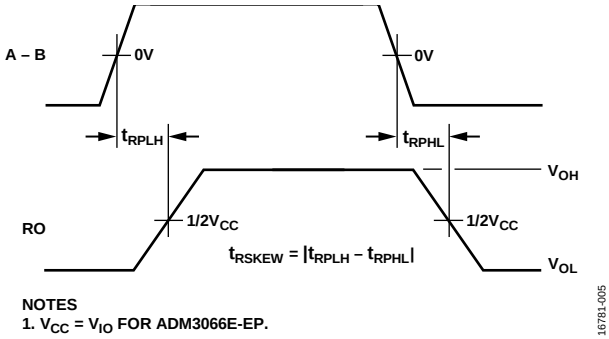
NOTES
1. V_{OD} IS THE DIFFERENCE BETWEEN A AND B, WITH $+V_{OD}$ BEING THE MAXIMUM POINT OF V_{OD}, AND $-V_{OD}$ BEING THE MINIMUM POINT OF V_{OD}.
2. $V_{CC} = V_{IO}$ FOR ADM3066E-EP.

Figure 4. Driver Propagation Delay Rise and Fall Timing Diagram



NOTES
1. $V_{IO} = V_{CC}$ FOR ADM3065E-EP/ADM3067E-EP.
2. Y = A, Z = B FOR ADM3065E-EP/ADM3066E-EP.

Figure 5. Driver Enable and Disable Timing Diagram



NOTES
1. $V_{CC} = V_{IO}$ FOR ADM3066E-EP.

Figure 6. Receiver Propagation Delay Timing Diagram

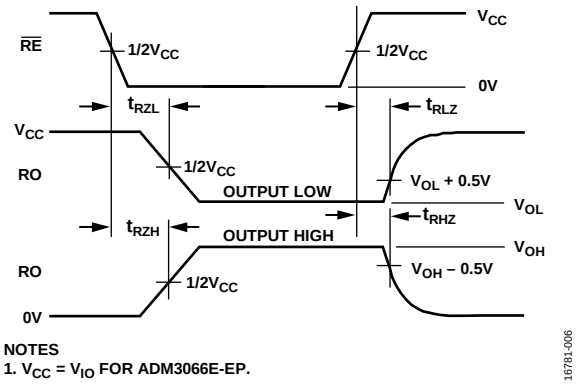


Figure 7. Receiver Enable and Disable Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{CC} to GND	6 V
V_{IO} to GND	−0.3 V to +6 V
Digital Input and Output Voltage (DE, $\overline{RE}$, DI, and RO)	−0.3 V to V_{CC} + 0.3 V
Driver Output and Receiver Input Voltage	−9 V to +14 V
Operating Temperature Ranges	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Continuous Total Power Dissipation	
8-Lead SOIC_N	0.225 W
8-Lead MSOP	0.151 W
10-Lead MSOP	0.151 W
14-Lead SOIC_N	0.239 W
Maximum Junction Temperature	150°C
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD on the Bus Pins (A, B, Y, Z)	
IEC 61000-4-2 Contact Discharge	±12 kV
IEC 61000-4-2 Air Discharge	±15 kV
DO-160 Section 25 Air Discharge	±15 kV
ESD Human Body Model (HBM)	
On the Bus Pins (A, B, Y, Z)	≥±30 kV
All Other Pins	±8 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[1]	Unit
R-8	110.88	58.63	°C/W
RM-8	165.69	49.61	°C/W
RM-10	165.69	49.61	°C/W
R-14	104.5	42.90	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no bias. See JEDEC JESD-51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

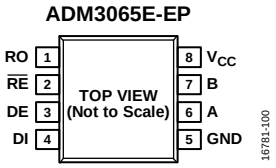


Figure 8. ADM3065E-EP 8-Lead Narrow Body SOIC_N Pin Configuration

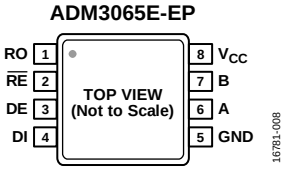


Figure 9. ADM3065E-EP 8-Lead MSOP Pin Configuration

Table 6. ADM3065E-EP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RO	Receiver Output Data. This output is high when (A − B) ≥ −30 mV and low when (A − B) ≤ −200 mV. This output is tristated when the receiver is disabled; that is, when $\overline{RE}$ is driven high.
2	$\overline{RE}$	Receiver Enable Input. This is an active low input. Driving this input low enables the receiver, and driving it high disables the receiver.
3	DE	Driver Enable. A high level on this pin enables the driver differential outputs, A and B. A low level places the driver output into a high impedance state.
4	DI	Transmit Data Input. Data to be transmitted by the driver is applied to this input.
5	GND	Ground.
6	A	Noninverting Driver Output and Receiver Input. When the driver is disabled, or when V_{CC} is powered down, Pin A is put into a high impedance state to avoid overloading the bus.
7	B	Inverting Driver Output and Receiver Input. When the driver is disabled, or when V_{CC} is powered down, Pin B is put into a high impedance state to avoid overloading the bus.
8	V_{CC}	3.0 V to 5.5 V Power Supply. Adding a 0.1 µF decoupling capacitor between the V_{CC} pin and the GND pin is recommended.

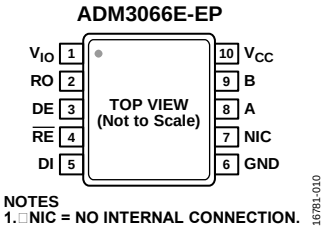


Figure 10. ADM3066E-EP 10-Lead MSOP Pin Configuration

Table 7. ADM3066E-EP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{IO}	1.62 V to 5.5 V Logic Supply. Adding a 0.1 µF decoupling capacitor between the V_{IO} pin and the GND pin is recommended.
2	RO	Receiver Output Data. This output is high when (A − B) ≥ −30 mV and low when (A − B) ≤ −200 mV. This output is tristated when the receiver is disabled; that is, when $\overline{RE}$ is driven high.
3	DE	Driver Enable. A high level on this pin enables the driver differential outputs, A and B. A low level places the driver output into a high impedance state.
4	$\overline{RE}$	Receiver Enable Input. This is an active low input. Driving this input low enables the receiver, and driving it high disables the receiver.
5	DI	Transmit Data Input. Data to be transmitted by the driver is applied to this input.
6	GND	Ground.
7	NIC	No Internal Connection. This pin is not internally connected.
8	A	Noninverting Driver Output and Receiver Input. When the driver is disabled, or when V_{CC} is powered down, Pin A is put into a high impedance state to avoid overloading the bus.
9	B	Inverting Driver Output and Receiver Input. When the driver is disabled, or when V_{CC} is powered down, Pin B is put into a high impedance state to avoid overloading the bus.
10	V_{CC}	3.0 V to 5.5 V Power Supply. Adding a 0.1 µF decoupling capacitor between the V_{CC} pin and the GND pin is recommended.

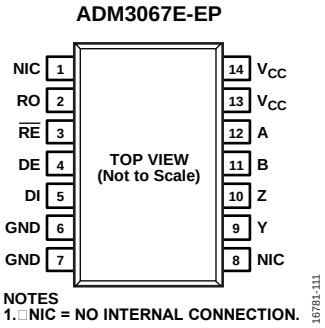


Figure 11. ADM3067E-EP 14-Lead SOIC Pin Configuration

Table 8. ADM3067E-EP Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8	NIC	No Internal Connection. This pin is not internally connected.
2	RO	Receiver Output Data. This output is high when (A − B) ≥ −30 mV and low when (A − B) ≤ −200 mV. This output is tristated when the receiver is disabled; that is, when $\overline{RE}$ is driven high.
3	$\overline{RE}$	Receiver Enable Input. This is an active low input. Driving this input low enables the receiver, and driving it high disables the receiver.
4	DE	Driver Enable. A high level on this pin enables the driver differential outputs, Y and Z. A low level places the driver output into a high impedance state.
5	DI	Transmit Data Input. Data to be transmitted by the driver is applied to this input.
6, 7	GND	Ground.
9	Y	Driver Noninverting Output. When the driver is disabled, or when V_{CC} is powered down, Pin Y is put into a high impedance state to avoid overloading the bus.
10	Z	Driver Inverting Output. When the driver is disabled, or when V_{CC} is powered down, Pin Z is put into a high impedance state to avoid overloading the bus.
11	B	Inverting Receiver Input.
12	A	Noninverting Receiver Input.
13, 14	V_{CC}	3.0 V to 5.5 V Power Supply. Adding a 0.1 µF decoupling capacitor between the V_{CC} pin and the GND pin is recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

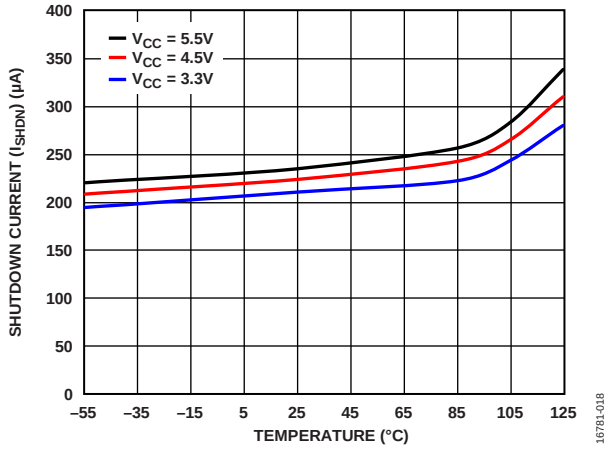


Figure 12. Shutdown Current (I_{SHDN}) vs. Temperature

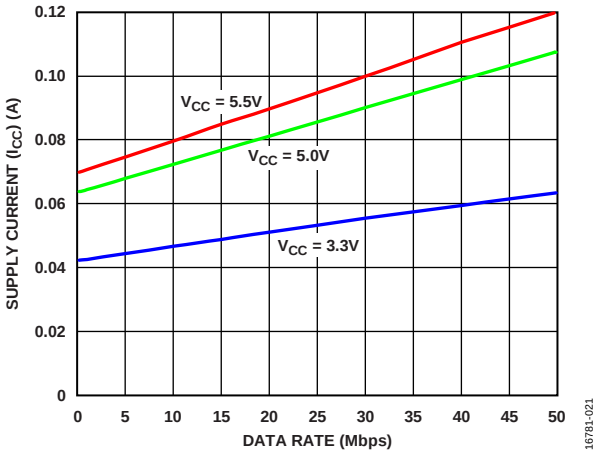


Figure 15. Supply Current (I_{CC}) vs. Data Rate with 54 Ω Load Resistance

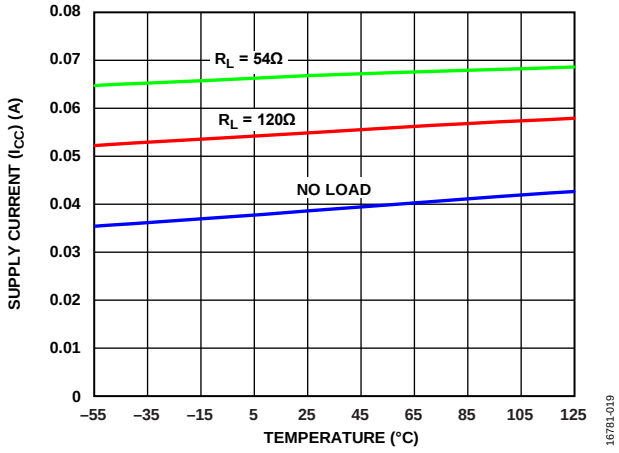


Figure 13. Supply Current (I_{CC}) vs. Temperature, Data Rate = 50 Mbps, V_{CC} = 3.3 V

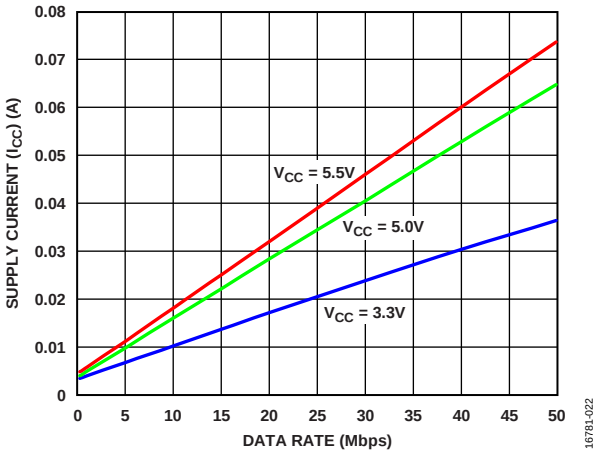


Figure 16. Supply Current (I_{CC}) vs. Data Rate with No Load Resistance

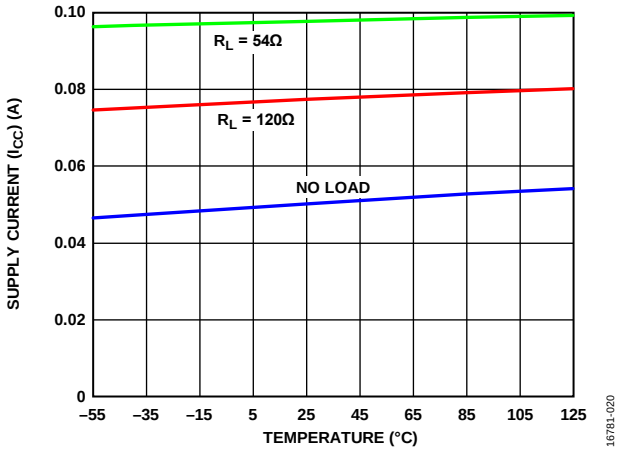


Figure 14. Supply Current (I_{CC}) vs. Temperature, Data Rate = 50 Mbps, V_{CC} = 5.0 V

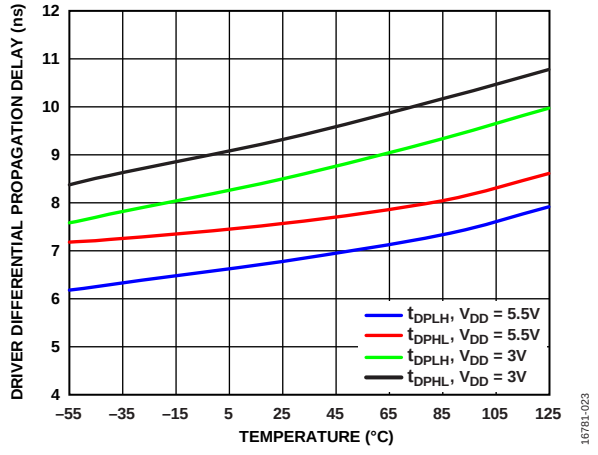


Figure 17. Driver Differential Propagation Delay vs. Temperature, 50 Mbps

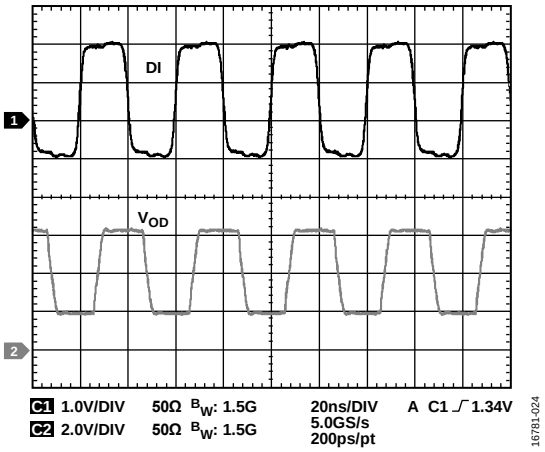


Figure 18. Driver Propagation Delay at 50 Mbps

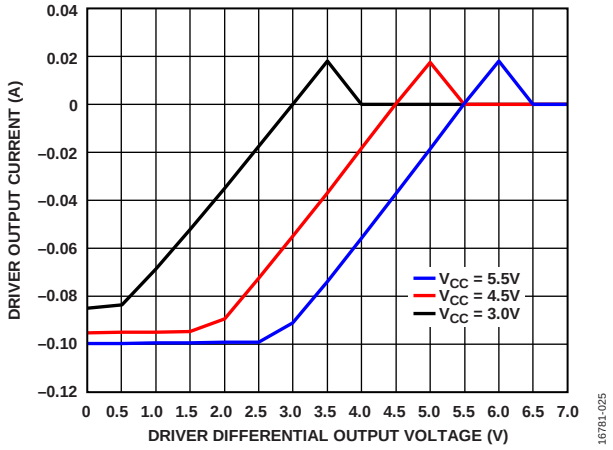


Figure 19. Driver Output Current vs. Driver Differential Output Voltage

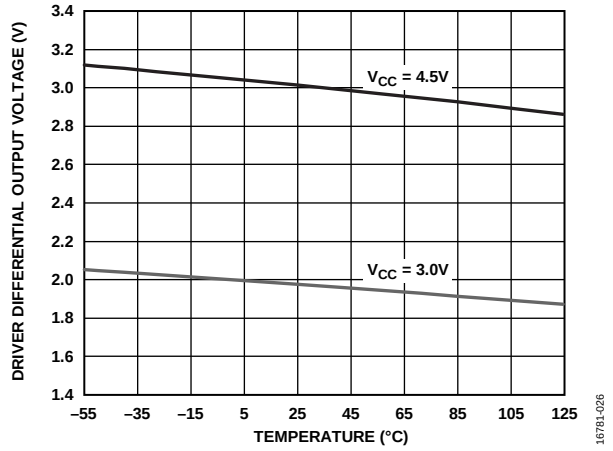


Figure 20. Driver Differential Output Voltage vs. Temperature

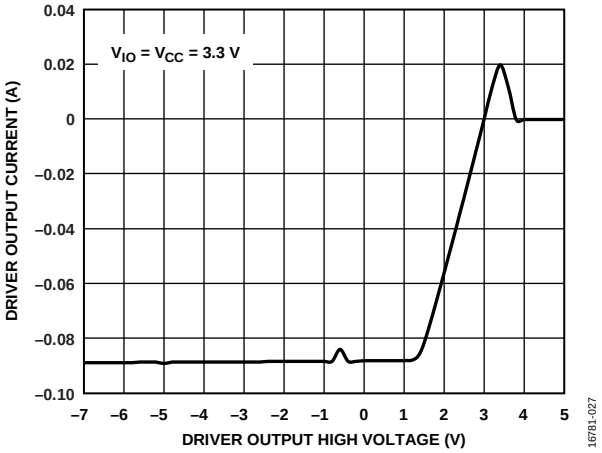


Figure 21. Driver Output Current vs. Driver Output High Voltage

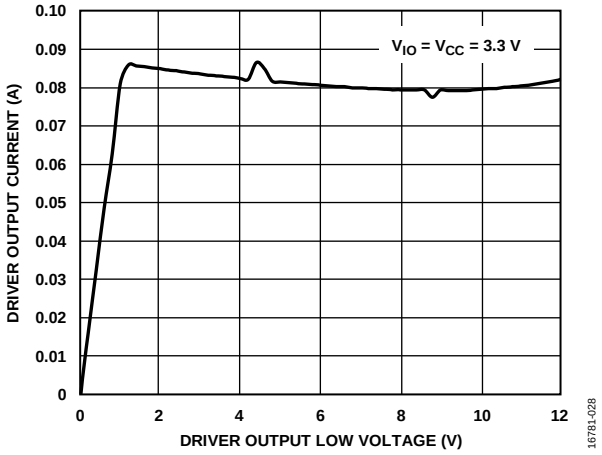


Figure 22. Driver Output Current vs. Driver Output Low Voltage

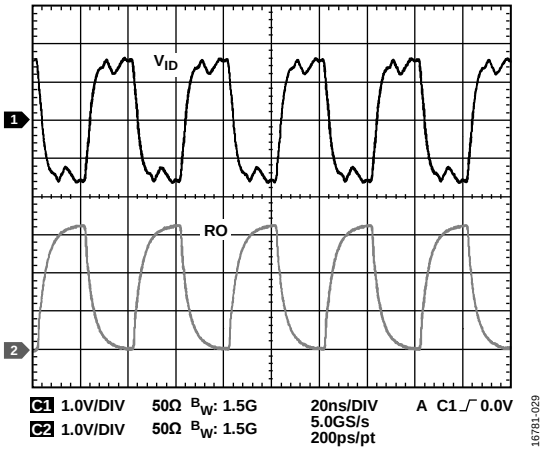


Figure 23. Receiver Propagation Delay at 50 Mbps, $|V_{ID}| \geq 1.5$ V

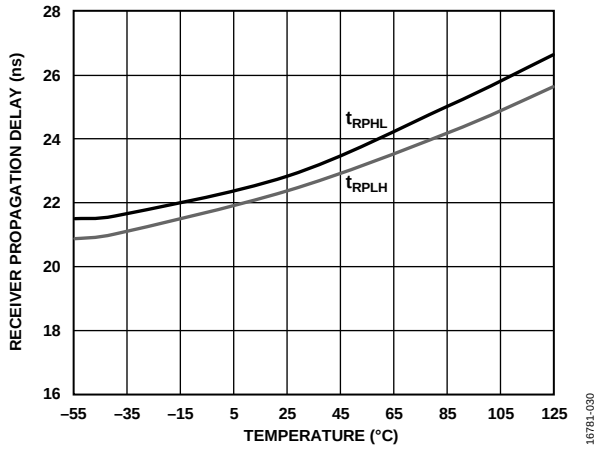


Figure 24. Receiver Propagation Delay vs. Temperature, 50 Mbps

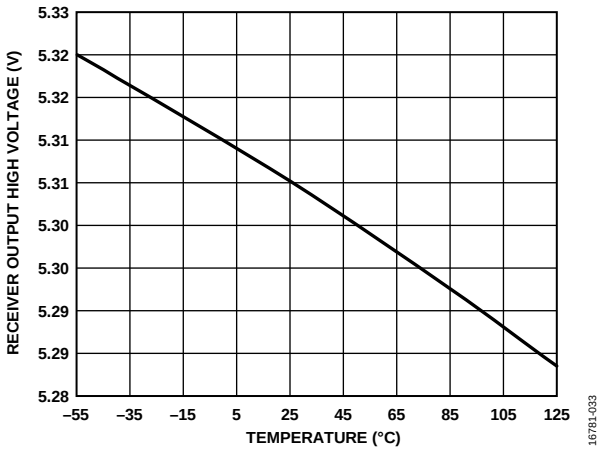


Figure 27. Receiver Output High Voltage vs. Temperature

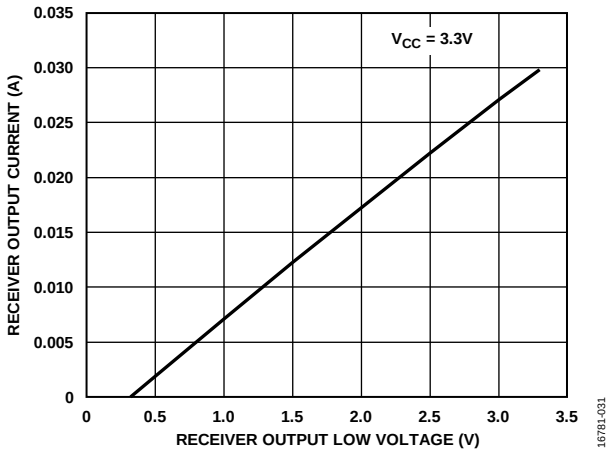


Figure 25. Receiver Output Current vs. Receiver Output Low Voltage (V_{CC} = 3.3 V)

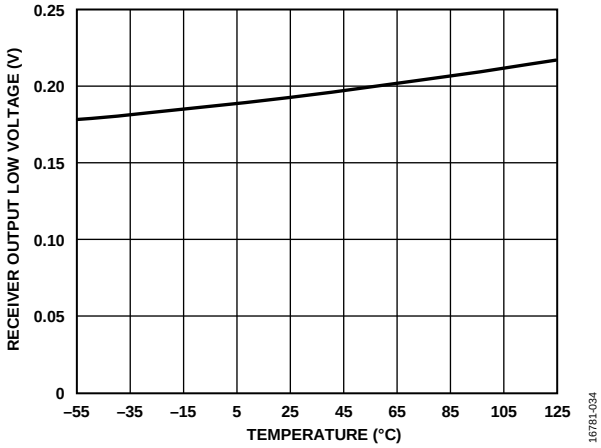


Figure 28. Receiver Output Low Voltage vs. Temperature

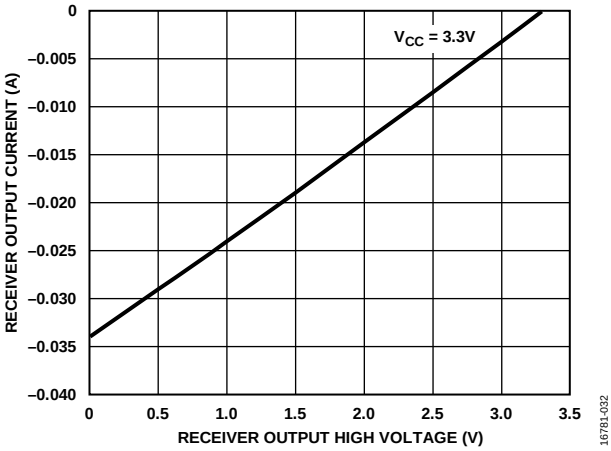


Figure 26. Receiver Output Current vs. Receiver Output High Voltage (V_{CC} = 3.3 V)

TEST CIRCUITS

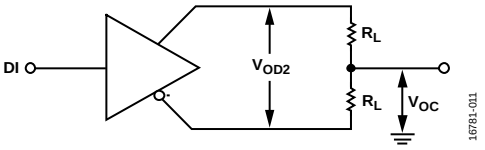


Figure 29. Driver Voltage Measurements

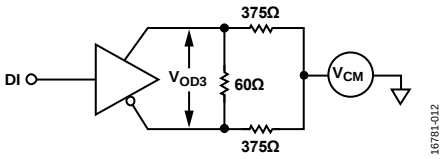


Figure 30. Driver Voltage Measurements over Common-Mode Range

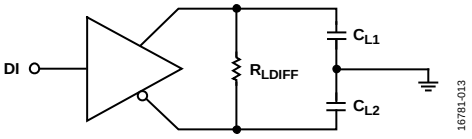


Figure 31. Driver Propagation Delay

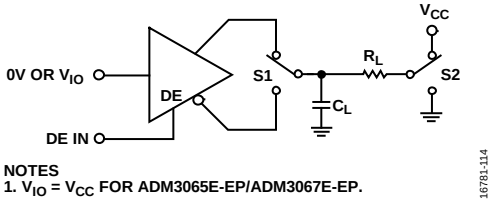


Figure 32. Driver Enable/Disable

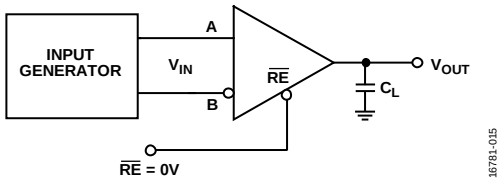


Figure 33. Receiver Propagation Delay/Skew

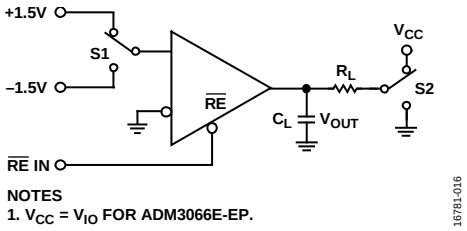


Figure 34. Receiver Enable/Disable from Shutdown

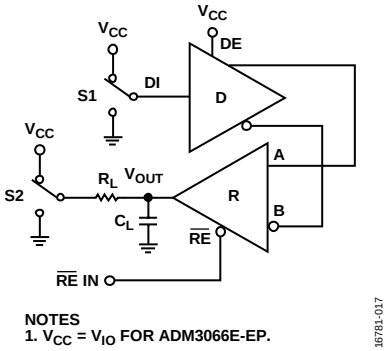


Figure 35. Receiver Enable/Disable

THEORY OF OPERATION

HIGH SPEED IEC ESD PROTECTED RS-485

The ADM3065E-EP/ADM3066E-EP/ADM3067E-EP are 3.0 V to 5.5 V, 50 Mbps RS-485 transceivers with DO-160 Section 25 ESD protection on the bus pins. The ADM3065E-EP/ADM3066E-EP/ADM3067E-EP can withstand up to ±12 kV contact discharge on transceiver bus pins (A, B, Y, and Z) without latch-up or damage.

DO-160 SECTION 25 ESD PROTECTION

ESD is the sudden transfer of electrostatic charge between bodies at different potentials caused by near contact or induced by an electric field. It has the characteristics of high current in a short time period. The primary purpose of the DO-160 Section 25 ESD test is to determine the immunity of systems to external ESD events outside the system during operation.

During testing, the data port is subjected to at least 10 positive and 10 negative single discharges. Selection of the test voltage is dependent on the system end environment.

Figure 36 shows the 8 kV contact discharge current waveform as described in the DO-160 Section 25 ESD specification. Some of the key waveform parameters are rise times of less than 1 ns and pulse widths of approximately 60 ns. The DO-160 Section 25 standard uses the same resistor/capacitor (RC) network and an equivalent test procedure as the IEC61000-4-2 standard.

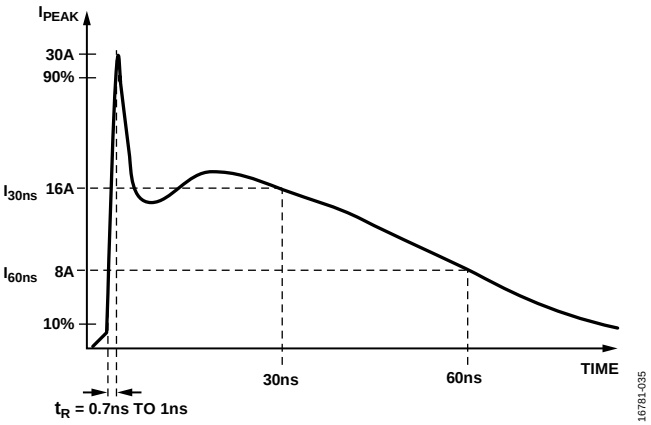


Figure 36. DO-160 Section 25 ESD Waveform (8 kV)

Figure 37 shows the 8 kV contact discharge current waveform from the DO-160 Section 25 ESD standard compared to the HBM ESD 8 kV waveform. Figure 37 shows that the two standards specify a different waveform shape and peak current. The peak current associated with a DO-160 Section 25 ESD 8 kV pulse is 30 A, whereas the corresponding peak current for HBM ESD is more than five times less, at 5.33 A. The other difference is the rise time of the initial voltage spike, with the DO-160 Section 25 ESD waveform having a much faster rise time of 1 ns, compared to the 10 ns associated with the HBM ESD waveform. The amount of power associated with a DO-160 Section 25 waveform is much greater than that of an HBM ESD waveform. The HBM ESD standard requires the equipment under test to be subjected to three positive and three negative discharges, whereas the DO-160 standard requires 10 positive and 10 negative discharge tests.

The ADM3065E-EP/ADM3066E-EP/ADM3067E-EP with DO-160 Section 25 and IEC61000-4-2 ESD ratings is better suited for operation in harsh environments compared to other RS-485 transceivers that state varying levels of HBM ESD protection.

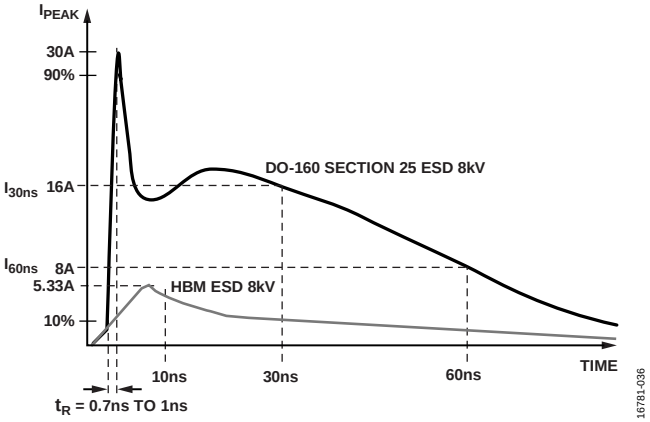
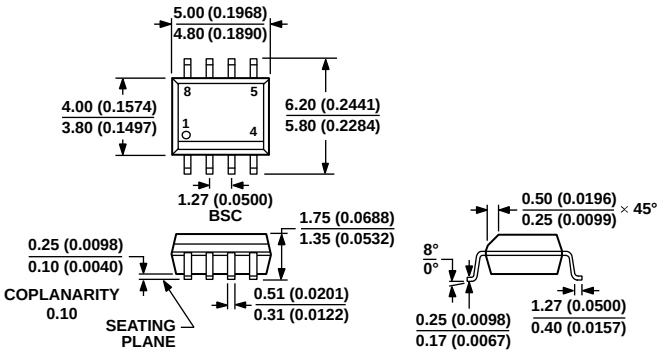


Figure 37. DO-160 Section 25 ESD Waveform 8 kV Compared to HBM ESD Waveform 8 kV

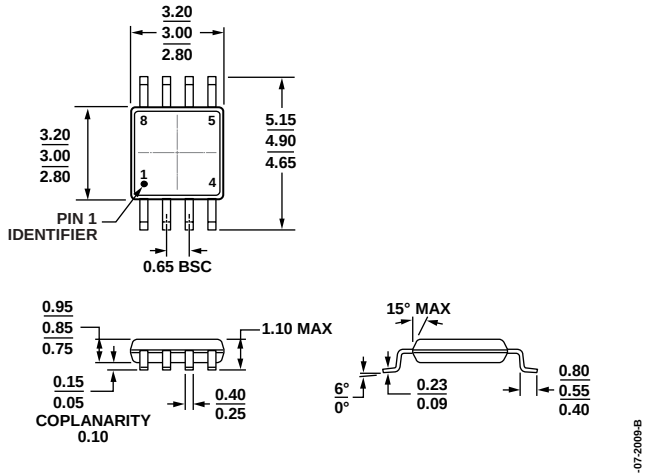
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 38. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

10-07-2009-B

Figure 39. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

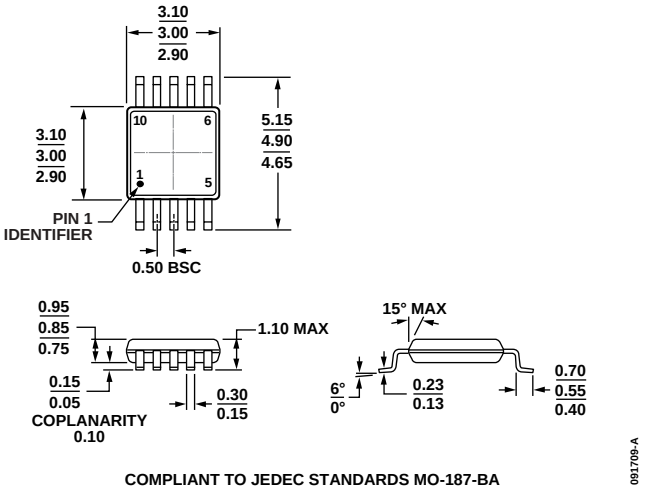


Figure 40. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

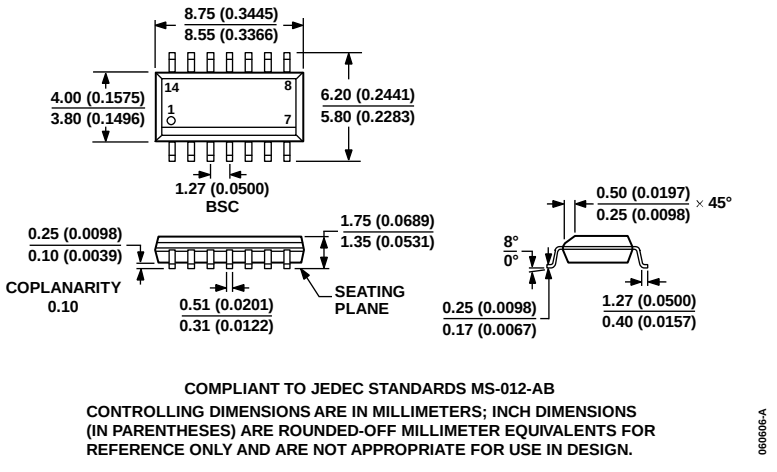


Figure 41. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADM3065ETRZ-EP	−55°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM3065ETRZ-EP-R7	−55°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADM3065ETRMZ-EP	−55°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8
ADM3065ETRMZ-EP-R7	−55°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8
ADM3066ETRMZ-EP	−55°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10
ADM3066ETRMZ-EP-R7	−55°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10
ADM3067ETRZ-EP	−55°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
ADM3067ETRZ-EP-R7	−55°C to +125°C	14-Lead Standard Small Outline Package [SOIC_N]	R-14
EVAL-ADM3065EEBZ		8-Lead SOIC Evaluation Board	
EVAL-ADM3065EEB1Z		8-Lead MSOP Evaluation Board	
EVAL-ADM3066EEBZ		10-Lead MSOP Evaluation Board	
EVAL-ADM3067EEBZ		14-Lead SOIC Evaluation Board	

[1] Z = RoHS Compliant Part.

D16781-0-4/19(0)

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for RS-485 Interface IC ***category:***

Click to view products by Analog Devices ***manufacturer:***

Other Similar products are found below :

LTC1483CN8 LTC1482CN8 SN75976A1MDGGREP SN65HVD24DR SN65HVD70DR SN65HVD1477DGKR SN65HVD1477DGK LTC1685CS8#PBF MAX14770EESA+T LTC486CN#PBF THVD1500DR LTC488CSW#PBF LTC2876HMS8E#PBF LTC485CS8#PBF THVD1550DR LTC1487CN8#PBF LTC489CSW#PBF LTC1485CN8#PBF LTC2861IDE#PBF LTC1686IS8#PBF LTC488CN#PBF LTC1480IN8#PBF ADM3066EARMZ ADM3095EBRZ LTC487IN#PBF LTC1482CMS8#PBF LTC488IN#PBF LTC486IN#PBF LTC1481IN8#PBF ADM3063EARZ ADM3064EARZ-R7 ADM3064EARZ ADM3065ETRMZ-EP ADM3066EBRMZ-R7 ADM3066ETRMZ-EP ADM3095EARZ LTC1687IS#PBF LTC1483IS8#PBF LTC1686CS8#PBF LTC1481CS8#PBF LTC1482CS8#TRPBF LTC2877HDD#PBF LTC485CN8#PBF SP488CS MAX3443ECPA+ LTC1484CN8#PBF LTC1482CN8#PBF LTC1483IN8#PBF LTC1483CS8 LTC1483IS8