6.5 V, 1 A, Ultralow Noise, High PSRR, Fast Transient Response CMOS LDO

Data Sheet **ADM7171**

FEATURES

- **Input voltage range: 2.3 V to 6.5 V**
- **Maximum load current: 1 A**
- **Low noise: 5 µV rms independent of output voltage at 100 Hz to 100 kHz**
- **Fast transient response: 1.5 µs for 1 mA to 500 mA load step**
- **60 dB PSRR at 100 kHz**
- **Low dropout voltage: 42 mV at 500 mA load, V_{OUT} = 3 V**
- **Initial accuracy: −0.5% (minimum), +1% (maximum)**
- **Accuracy over line, load, and temperature: ±1.5%**
- **Quiescent current, I_{GND} = 0.7 mA with no load**
- **Low shutdown current: 0.25 µA at V_{IN} = 5 V**
- **Stable with small 4.7 µF ceramic output capacitor**
- **Adjustable and fixed output voltage options: 1.2 V to 5.0 V**
- **Adjustable output from 1.2 V to V_{IN} − V_{DO}**
- **Precision enable**
- **Adjustable soft start**
- **8-lead, 3 mm × 3 mm LFCSP package**
- **Supported by ADIsimPower tool**

APPLICATIONS

- **Regulation to noise sensitive applications: ADC and DAC circuits, precision amplifiers, PLLs/VCOs, and clocking ICs**
- **Communications and infrastructure**
- **Medical and healthcare**
- **Industrial and instrumentation**

GENERAL DESCRIPTION

The ADM7171 is a CMOS, low dropout linear regulator (LDO) that operates from 2.3 V to 6.5 V and provides up to 1 A of output current. This high output current LDO is ideal for regulation of high performance analog and mixed signal circuits operating from 6 V down to 1.2 V rails. Using an advanced proprietary architecture, the device provides high power supply rejection and low noise, and achieves excellent line and load transient response with just a small 4.7 µF ceramic output capacitor. Load transient response is typically 1.5 µs for a 1 mA to 500 mA load step.

The ADM7171 is available in 17 fixed output voltage options. The following voltages are available from stock: 1.3 V, 1.8 V, 2.5 V, 3.0 V, 3.3 V, 4.2 V, and 5.0 V. Additional voltages that are available by special order are: 1.5 V, 1.85 V, 2.0 V, 2.2 V, 2.7 V, 2.75 V, 2.8 V, 2.85 V, 3.8 V, and 4.6 V. An adjustable version is also available that allows output voltages that range from 1.2 V to V_{IN} − V_{DO} with an external feedback divider.

Inrush current can be controlled by adjusting the start-up time via the soft start pin. The typical start-up time with a 1 nF soft start capacitor is 1.0 ms.

Rev. E **Document Feedback**

TYPICAL APPLICATION CIRCUIT

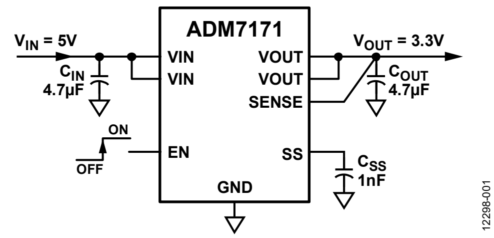

Figure 1. ADM7171 with Fixed Output Voltage, 3.3 V

The ADM7171 regulator output noise is 5 µV rms independent of the output voltage. The ADM7171 is available in an 8-lead, 3 mm × 3 mm LFCSP, making it not only a very compact solution, but also providing excellent thermal performance for applications requiring up to 1 A of output current in a small, low profile footprint.

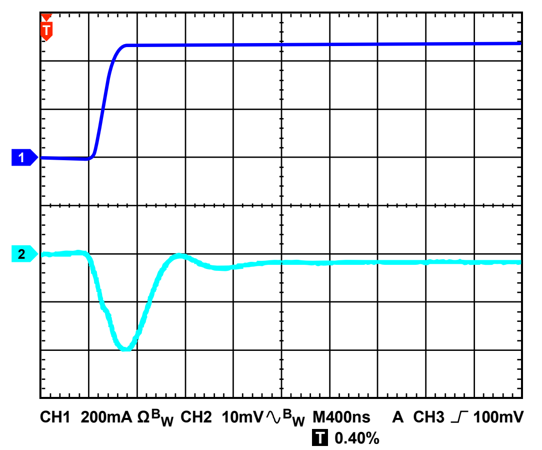

Figure 2. Transient Response (Trace 2), 1 mA to 500 mA Load Step in 400 ns (Trace 1)

Table 1. Related Devices

Device	Input Voltage	Output Current	Package
ADM7170	2.3 V to 6.5 V	500 mA	8-lead LFCSP
ADM7172	2.3 V to 6.5 V	2 A	8-lead LFCSP

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7/2014—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = (V_{OUT} + 0.5 V) or 2.3 V (whichever is greater), EN = V_{IN}, I_{LOAD} = 10 mA, C_{IN} = C_{OUT} = 4.7 µF, T_A = 25°C for typical specifications, T_J = −40°C to +125°C for minimum/maximum specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}		2.3		6.5	V
LOAD CURRENT	I_{LOAD}				1	A
OPERATING SUPPLY CURRENT	I_{GND}	I_{LOAD} = 0 µA		0.7	2.0	mA
		I_{LOAD} = 1 A		4.0	6.3	mA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND, V_{IN} = 5 V		0.25	3.8	µA
OUTPUT VOLTAGE ACCURACY						
Fixed Output Voltage Accuracy	V_{OUT}	I_{LOAD} = 10 mA, T_J = 25°C	−0.5		+1	%
		100 µA< I_{LOAD} < 1A V_{IN} = (V_{OUT} + 0.5V) to 6.5 V	−1.5		+1.5	%
Adjustable Output Voltage Accuracy	V_{SENSE}	I_{LOAD} = 10 mA	1.194	1.200	1.212	V
		10 mA < I_{LOAD} < 2 A, V_{IN} = (V_{OUT} + 0.5 V) to 6.5 V	1.182		1.218	V
REGULATION						
Line	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.5 V) to 6.5 V	−0.1		+0.1	%/V
Load	$\Delta V_{OUT}/\Delta I_{LOAD}$	I_{LOAD} = 100 µA to 1 A		0.1	0.4	%/A
SENSE INPUT BIAS CURRENT	$SENSE_{I-BIAS}$	100 µA< I_{LOAD} < 1 A, V_{IN} = (V_{OUT} + 0.5 V) to 6.5 V		1		nA
DROPOUT VOLTAGE[1]	$V_{DROPOUT}$	I_{LOAD} = 500 mA, V_{OUT} = 3 V		42	70	mV
		I_{LOAD} = 1 A, V_{OUT} = 3 V		84	135	mV
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, all fixed output voltages		6		µV rms
		100 Hz to 100 kHz, all fixed output voltages		5		µV rms
Noise Spectral Density		100 Hz, all fixed output voltages		110		nV/√Hz
		1 kHz, all fixed output voltages		40		nV/√Hz
		10 kHz, all fixed output voltages		20		nV/√Hz
		100 kHz, all fixed output voltages		12		nV/√Hz
POWER SUPPLY REJECTION RATIO	PSRR	100 kHz, V_{IN} = 4.0 V, V_{OUT} = 3 V, I_{LOAD} = 1 A, C_{SS} = 0 nF		60		dB
		100 kHz, V_{IN} = 3.5 V, V_{OUT} = 3 V, I_{LOAD} = 1 A, C_{SS} = 0 nF		53		dB
		100 kHz, V_{IN} = 3.3 V, V_{OUT} = 3 V, I_{LOAD} = 1 A, C_{SS} = 0 nF		42		dB
		1 MHz, V_{IN} = 4.0 V, V_{OUT} = 3 V, I_{LOAD} = 1 A, C_{SS} = 0 nF		31		dB
		1 MHz, V_{IN} = 3.5 V, V_{OUT} = 3 V, I_{LOAD} = 1 A, C_{SS} = 0 nF		30		dB
		1 MHz, V_{IN} = 3.3 V, V_{OUT} = 3 V, I_{LOAD} = 1 A, C_{SS} = 0 nF		20		dB
TRANSIENT LOAD RESPONSE	t_{TR-REC}	Time for output voltage to settle within ±V_{SETTLE} from V_{DEV} for a 1 mA to 500 mA load step, load step rise time = 400 ns		1.5		µs
	V_{DEV}	Output voltage deviation due to 1 mA to 500 mA load step		35		mV
	V_{SETTLE}	Output voltage deviation after transient load response time (t_{TR-REC}) has passed, V_{OUT} = 5 V, C_{OUT} = 4.7 µF		0.1		%
START-UP TIME[2]	$t_{START-UP}$	V_{OUT} = 5 V, C_{SS} = 0 nF		380		µs
		V_{OUT} = 5 V, C_{SS} = 1 nF		1.0		ms
SOFT START CURRENT	I_{SS}	V_{IN} = 5 V	0.5	1	1.5	µA
CURRENT-LIMIT THRESHOLD[3]	I_{LIMIT}		1.3	2.1	2.7	A
V_{OUT} PULL-DOWN RESISTANCE	$V_{OUT-PULL}$	EN = 0 V, V_{OUT} = 1 V		11		kΩ
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
UNDERVOLTAGE THRESHOLDS						
Input Voltage Rising	$UVLO_{RISE}$				2.28	V
Input Voltage Falling	$UVLO_{FALL}$		1.94			V
Hysteresis	$UVLO_{HYS}$			200		mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
EN INPUT STANDBY		$2.3\ V \le V_{IN} \le 6.5\ V$				
EN Input Logic High	$EN_{STBY-HIGH}$		1.1			V
EN Input Logic Low	$EN_{STBY-LOW}$				0.4	V
EN Input Logic Hysteresis	$EN_{STBY-HYS}$			80		mV
EN INPUT PRECISION		$2.3\ V \le V_{IN} \le 6.5\ V$				
EN Input Logic High	EN_{HIGH}		1.11	1.2	1.27	V
EN Input Logic Low	EN_{LOW}		1.01	1.1	1.16	V
EN Input Logic Hysteresis	EN_{HYS}			100		mV
EN Input Leakage Current	I_{EN-LKG}	EN = V_{IN} or GND		0.1	1.0	µA
EN Input Delay Time	TI_{EN-DLY}	From EN rising from 0 V to V_{IN} to 0.1 V × V_{OUT}		130		µs

[1] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. Dropout applies only for output voltages greater than 2.3 V.
[2] Start-up time is defined as the time between the rising edge of EN to VOUT being at 90% of its nominal value.
[3] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 5.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 5.0 V, or 4.5 V.

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
MINIMUM INPUT AND OUTPUT CAPACITANCE[1]	C_{MIN}	T_A = −40°C to +125°C	3.3			µF
CAPACITOR ESR	R_{ESR}	T_A = −40°C to +125°C	0.001		0.05	Ω

[1] Ensure that the minimum input and output capacitance is greater than 3.3 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VIN to GND	−0.3 V to +7 V
VOUT to GND	−0.3 V to V_{IN}
EN to GND	−0.3 V to +7 V
SS to GND	−0.3 V to V_{IN}
SENSE to GND	−0.3 V to +7 V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADM7171 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may need to be derated.

In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit provided that the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 in. × 3 in. circuit board. See JESD51-7 and JESD51-9 for detailed information on the board construction. For additional information, see the AN-617 Application Note, *Wafer Level Chip Scale Package*, available at www.analog.com.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

See JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA}, θ_{JC}, and Ψ_{JB} are specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Ψ_{JB}	Unit
8-Lead LFCSP	36.4	23.5	13.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

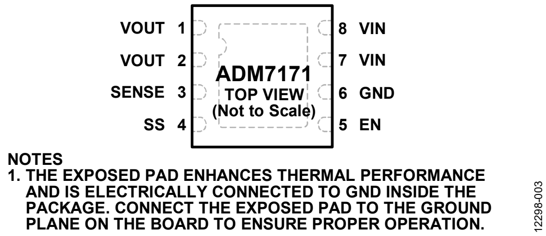

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VOUT	Regulated Output Voltage. Bypass this pin to GND with a 4.7 µF or greater capacitor.
2	VOUT	Regulated Output Voltage. This pin is internally connected to Pin 1.
3	SENSE	Sense Input. Connect this pin as close as possible to the load for best load regulation. Use an external resistor divider to set the output voltage higher than the fixed output voltage.
4	SS	Soft Start. A 1 nF external capacitor connected to SS results in a 1.0 ms start-up time.
5	EN	Regulator Enable. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN (Pin 7 or Pin 8).
6	GND	Ground.
7	VIN	Regulator Input Supply. Bypass this pin to GND with a 4.7 µF or greater capacitor.
8	VIN	Regulator Input Supply. This pin is internally connected to Pin 7.
	EP	Exposed Pad. The exposed pad is on the bottom of the package. The exposed pad enhances thermal performance and is electrically connected to GND inside the package. Connect the exposed pad to the ground plane on the board to ensure proper operation.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5.5 V, V_{OUT} = 5 V, I_{LOAD} = 10 mA, C_{IN} = C_{OUT} = 4.7 µF, T_A = 25°C, unless otherwise noted.

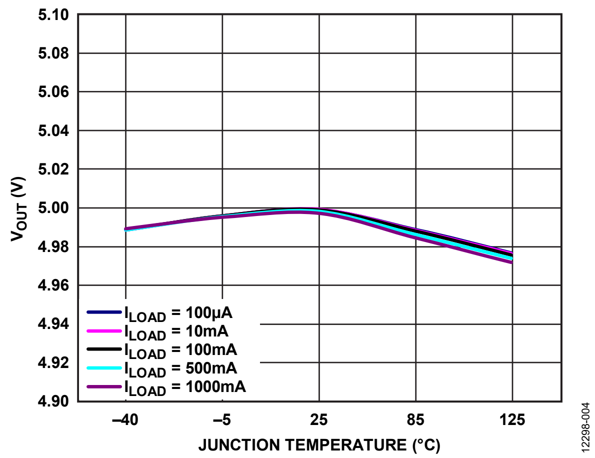

Figure 4. Output Voltage (V_{OUT}) vs. Junction Temperature

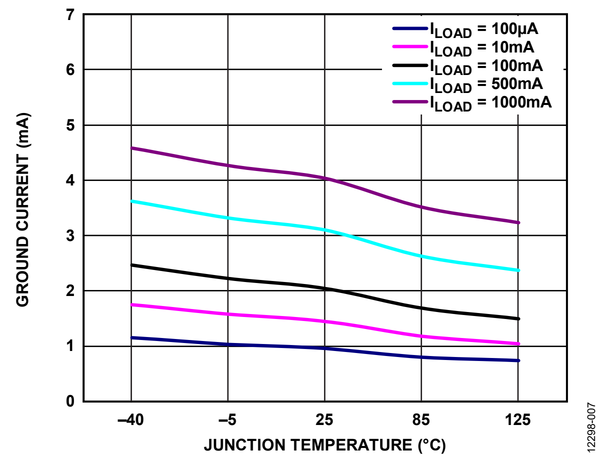

Figure 7. Ground Current vs. Junction Temperature

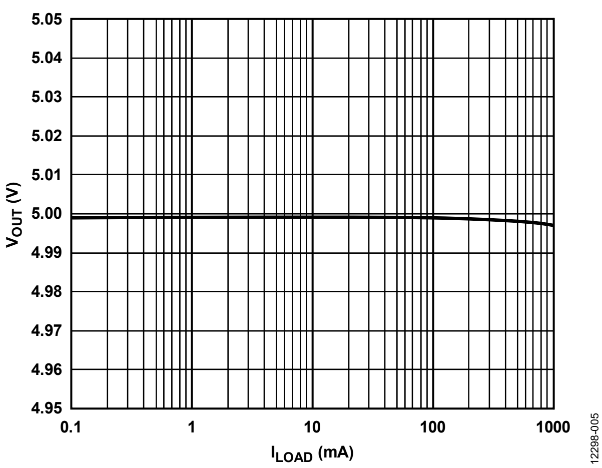

Figure 5. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD})

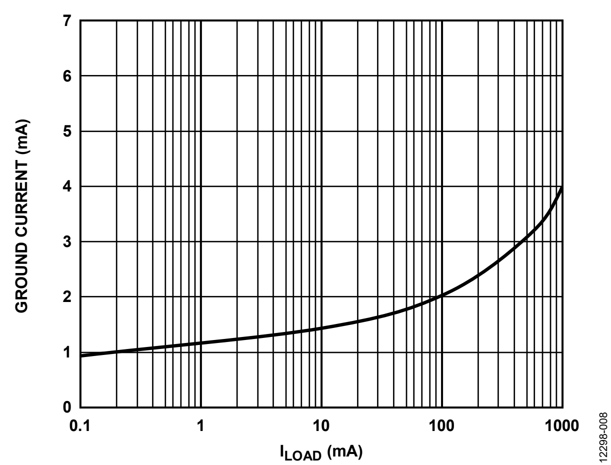

Figure 8. Ground Current vs. Load Current (I_{LOAD})

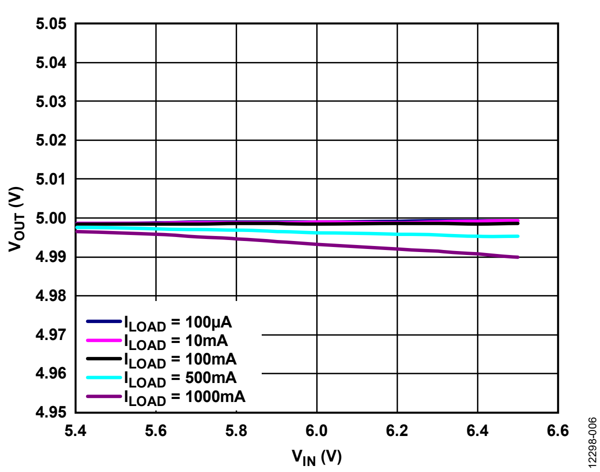

Figure 6. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN})

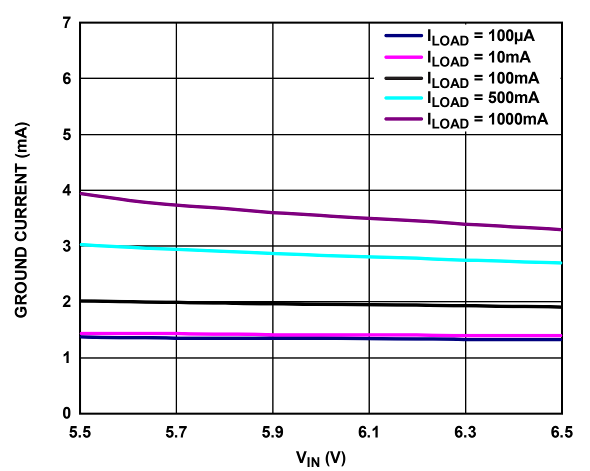

Figure 9. Ground Current vs. Input Voltage (V_{IN})

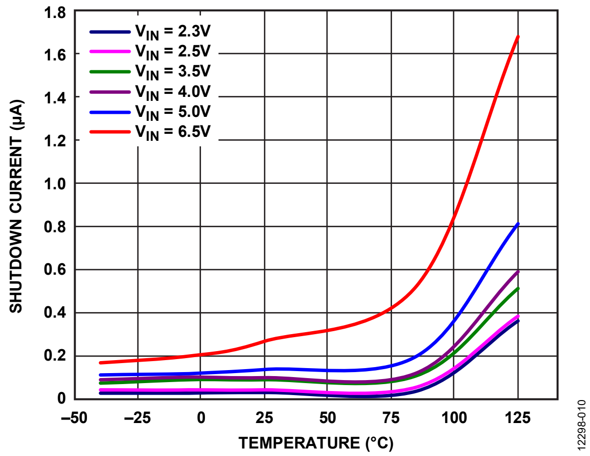

Figure 10. Shutdown Current vs. Temperature at Various Input Voltages

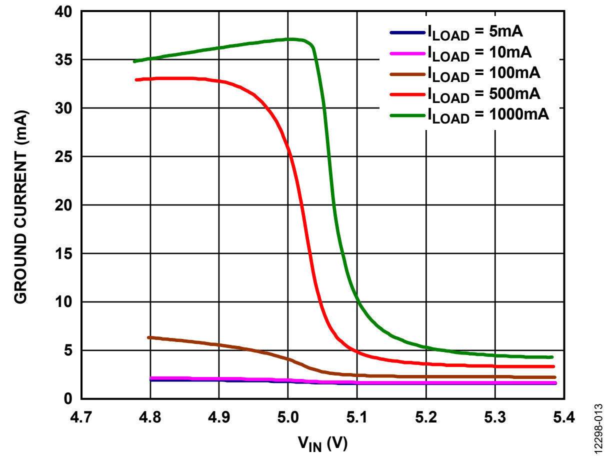

Figure 13. Ground Current vs. Input Voltage (V_{IN}) in Dropout, V_{OUT} = 5 V

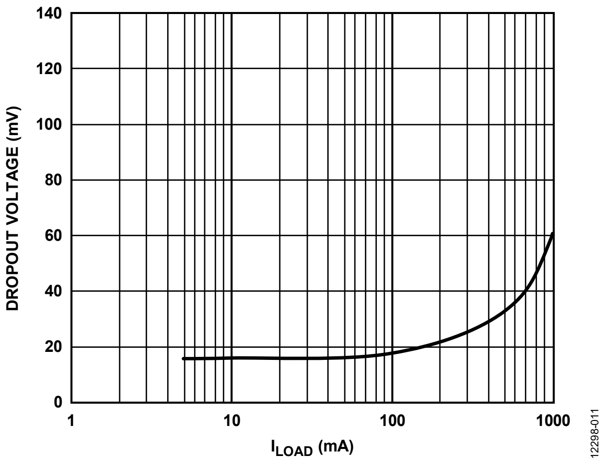

Figure 11. Dropout Voltage vs. Load Current (I_{LOAD}), V_{OUT} = 5 V

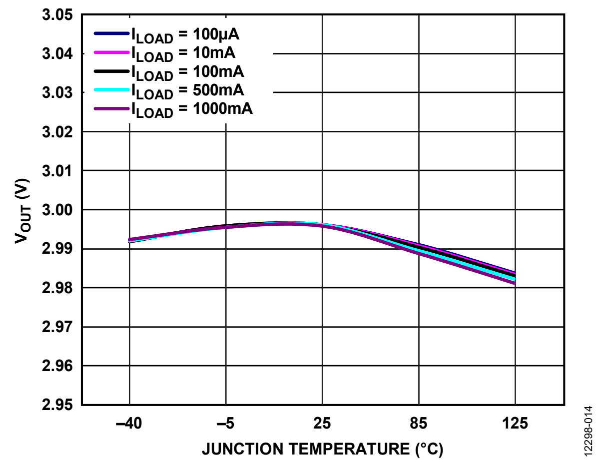

Figure 14. Output Voltage (V_{OUT}) vs. Junction Temperature, V_{OUT} = 3 V

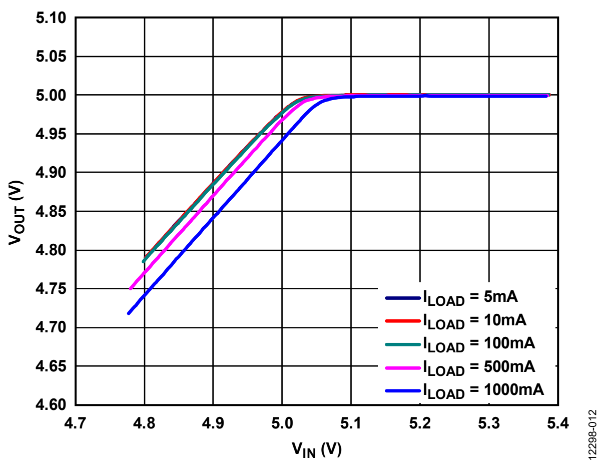

Figure 12. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout, V_{OUT} = 5 V

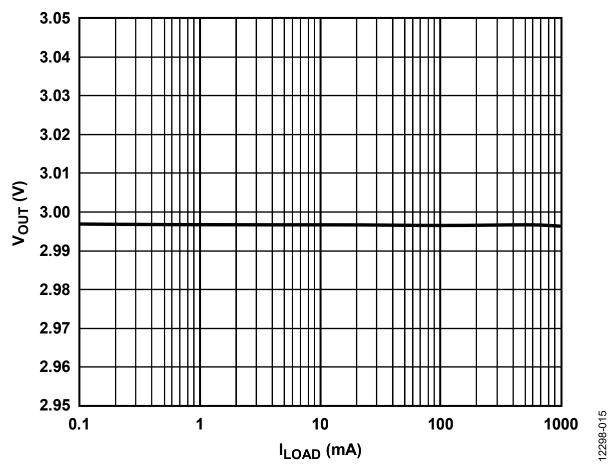

Figure 15. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = 3 V

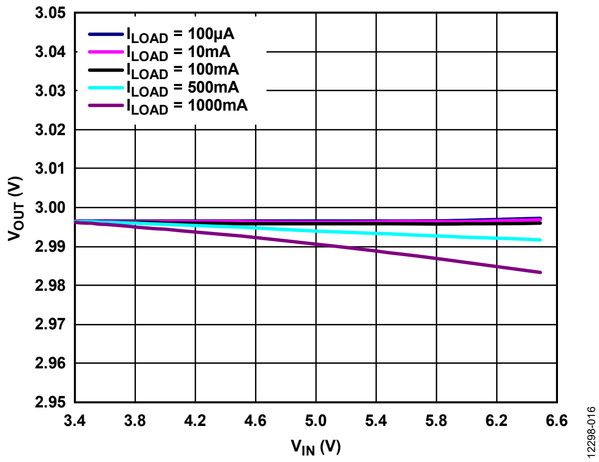

Figure 16. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), V_{OUT} = 3 V

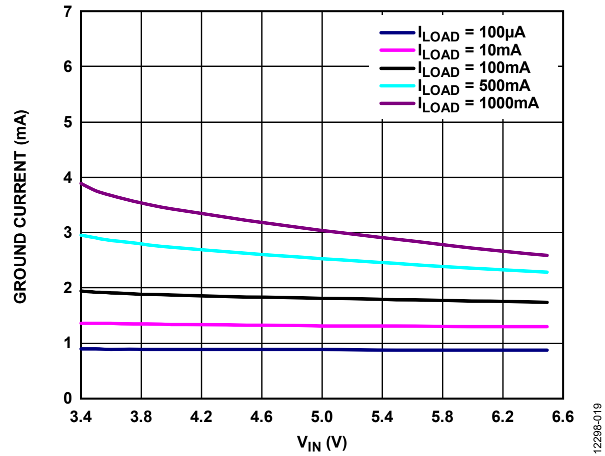

Figure 19. Ground Current vs. Input Voltage (V_{IN}), V_{OUT} = 3 V

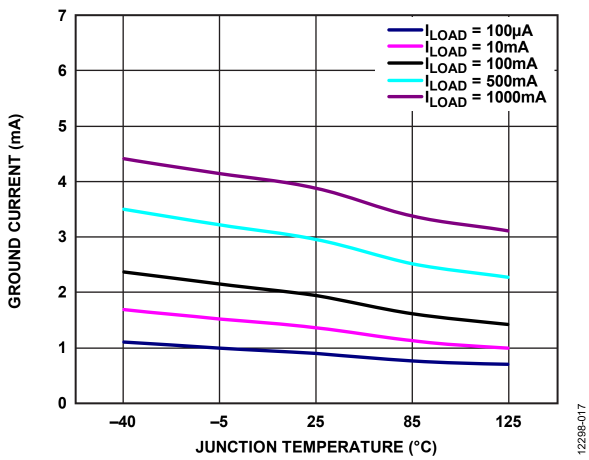

Figure 17. Ground Current vs. Junction Temperature, V_{OUT} = 3 V

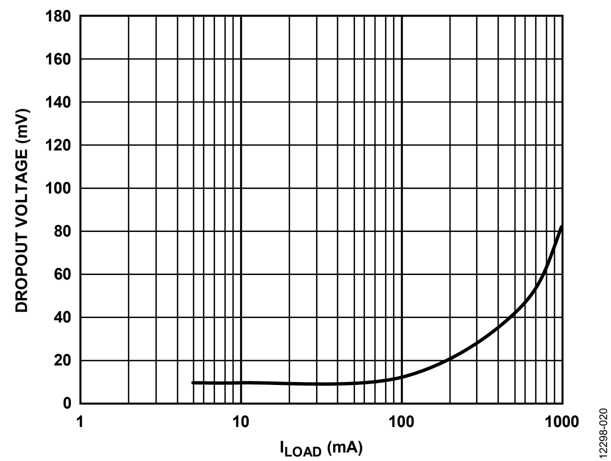

Figure 20. Dropout Voltage vs. Load Current (I_{LOAD}), V_{OUT} = 3 V

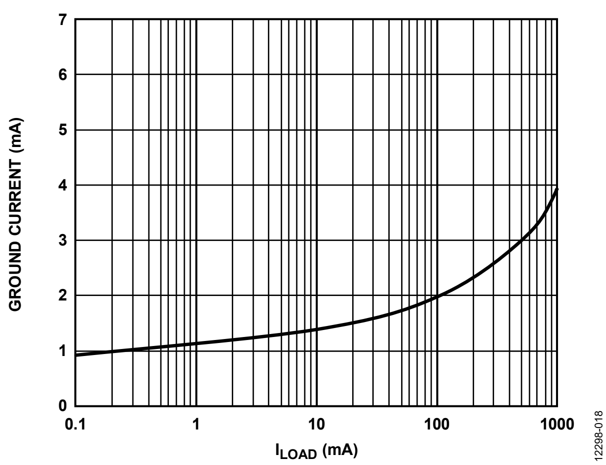

Figure 18. Ground Current vs. Load Current (I_{LOAD}), V_{OUT} = 3 V

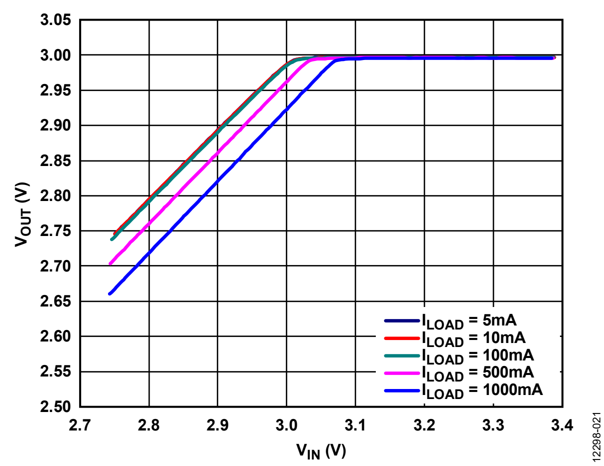

Figure 21. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout, V_{OUT} = 3 V

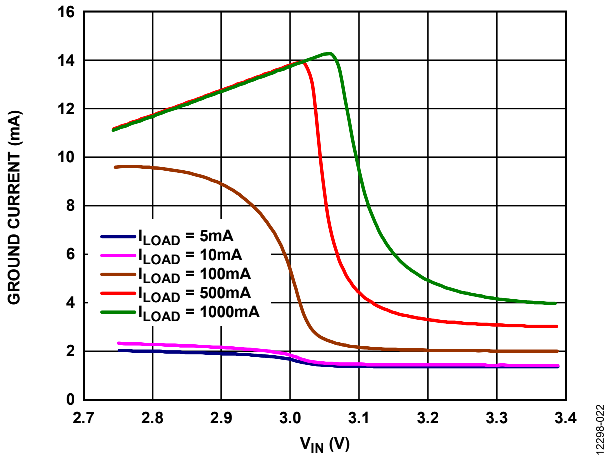

Figure 22. Ground Current vs. Input Voltage (V_{IN}) in Dropout, V_{OUT} = 3 V

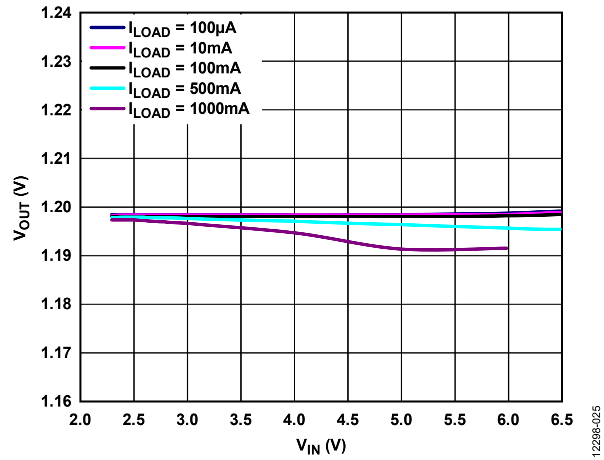

Figure 25. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), Adjustable Version, V_{OUT} = 1.2 V

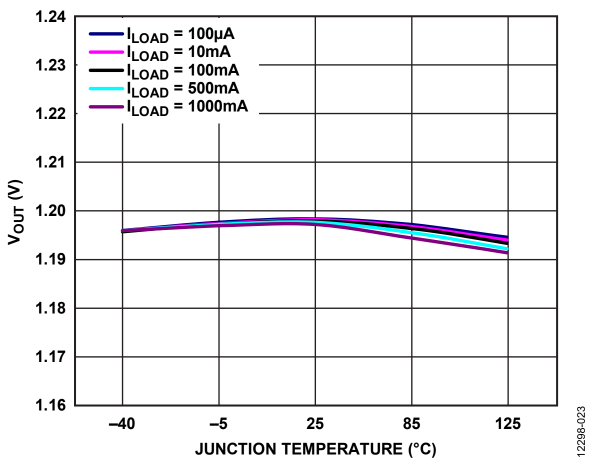

Figure 23. Output Voltage (V_{OUT}) vs. Junction Temperature, Adjustable Version, V_{OUT} = 1.2 V

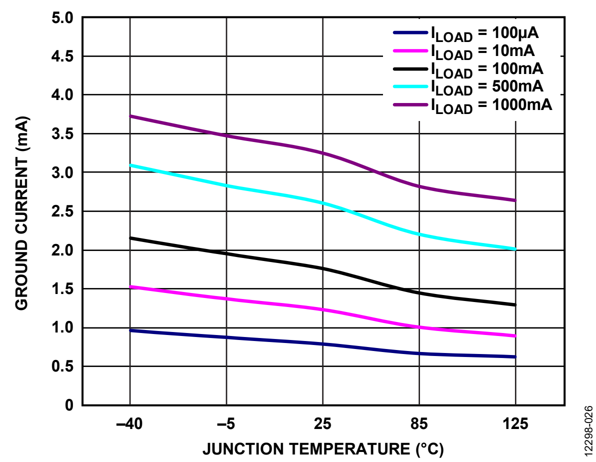

Figure 26. Ground Current vs. Junction Temperature, Adjustable Version, V_{OUT} = 1.2 V

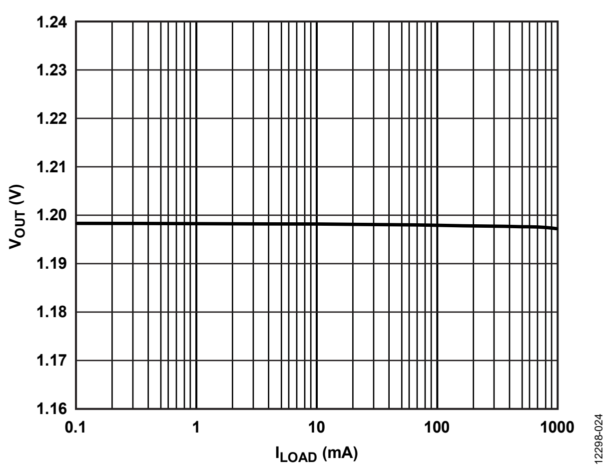

Figure 24. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), Adjustable Version, V_{OUT} = 1.2 V

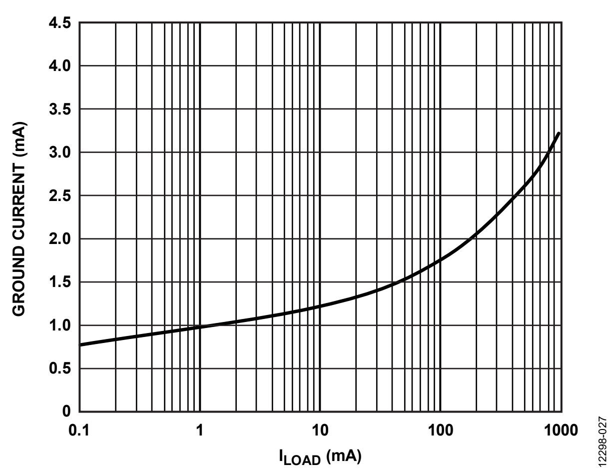

Figure 27. Ground Current vs. Load Current (I_{LOAD}), Adjustable Version, V_{OUT} = 1.2 V

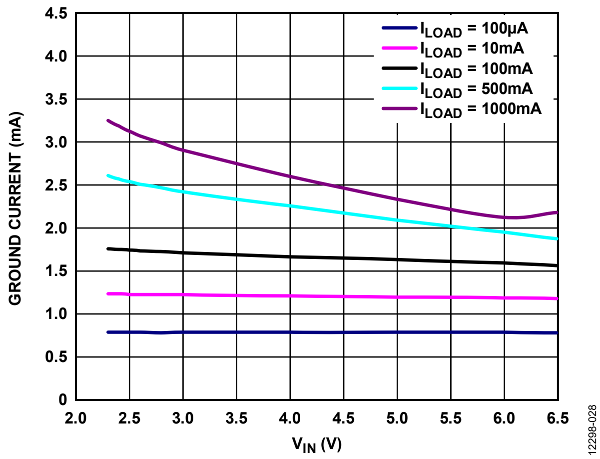

Figure 28. Ground Current vs. Input Voltage (V_{IN}), Adjustable Version, V_{OUT} = 1.2 V

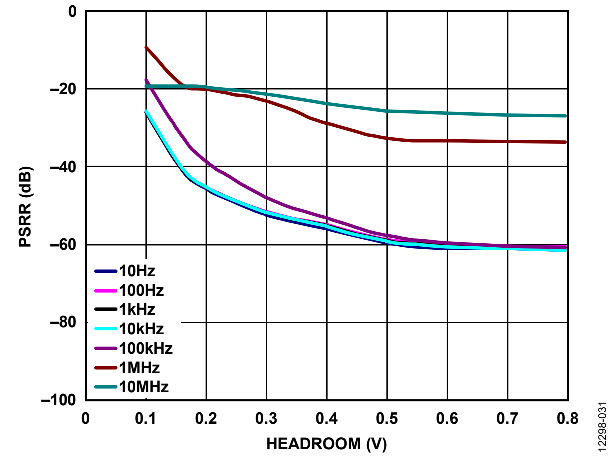

Figure 31. Power Supply Rejection Ratio (PSRR) vs. Headroom, V_{OUT} = 3 V, 1 A Load Current, Different Frequencies

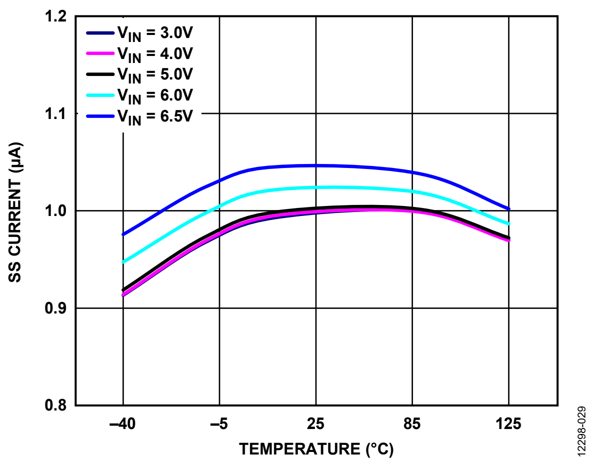

Figure 29. Soft Start Current vs. Temperature, Different Input Voltages, V_{OUT} = 5 V

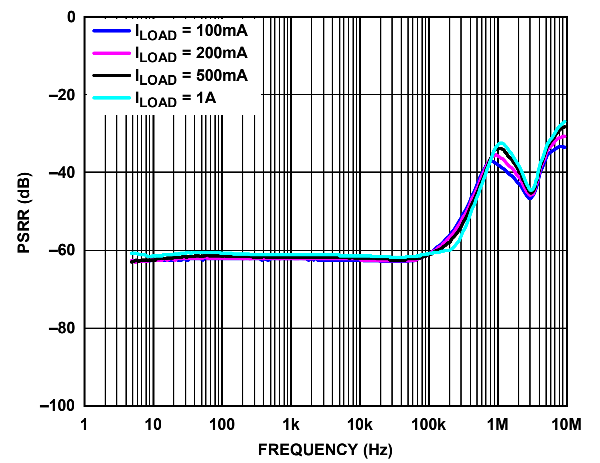

Figure 32. Power Supply Rejection Ratio (PSRR) vs. Frequency, 800 mV Headroom, V_{OUT} = 3 V

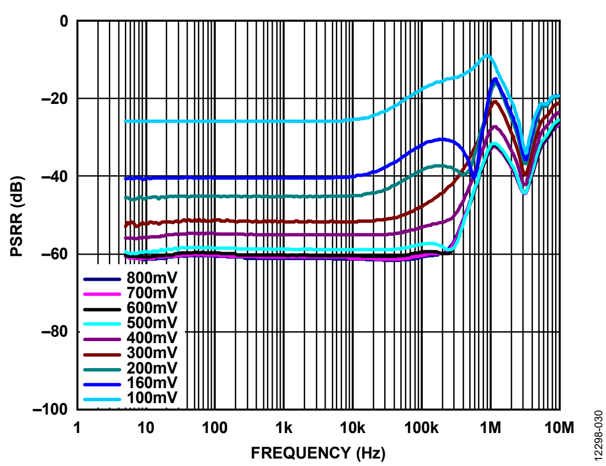

Figure 30. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = 3 V, 1 A Load Current, Various Headroom Voltages

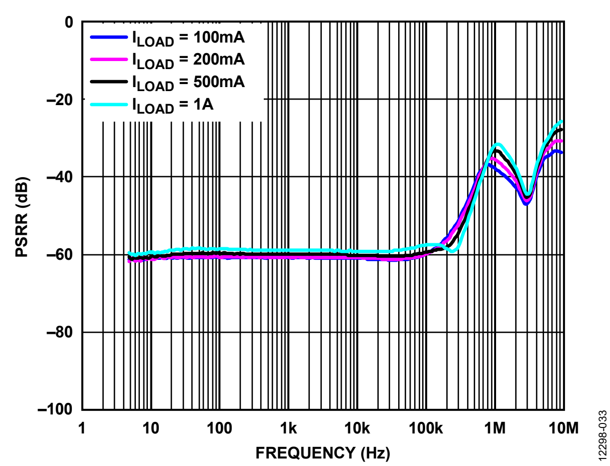

Figure 33. Power Supply Rejection Ratio (PSRR) vs. Frequency, 500 mV Headroom, V_{OUT} = 3 V

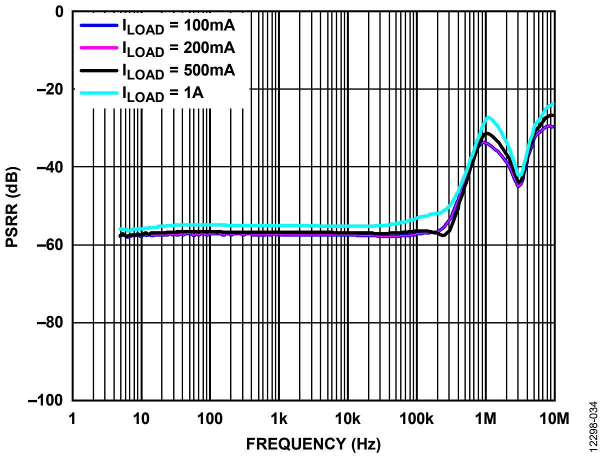

Figure 34. Power Supply Rejection Ratio (PSRR) vs. Frequency, 400 mV Headroom, V_{OUT} = 3 V

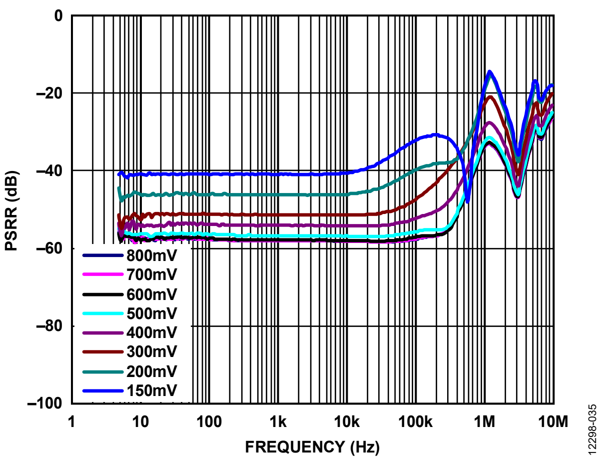

Figure 35. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = 5 V, 1 A Load Current, Various Headroom Voltages

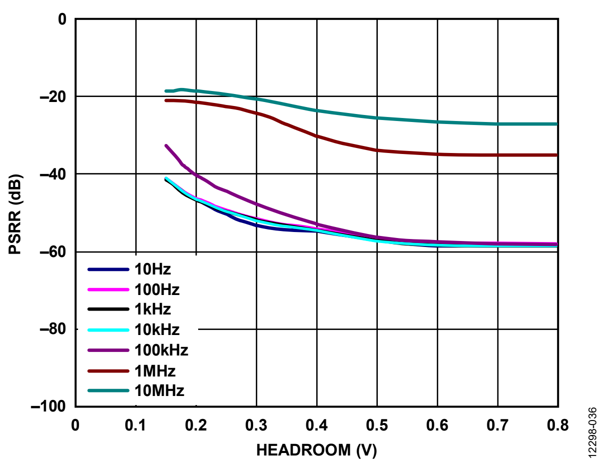

Figure 36. Power Supply Rejection Ratio (PSRR) vs. Headroom, V_{OUT} = 5 V, 1 A Load Current, Different Frequencies

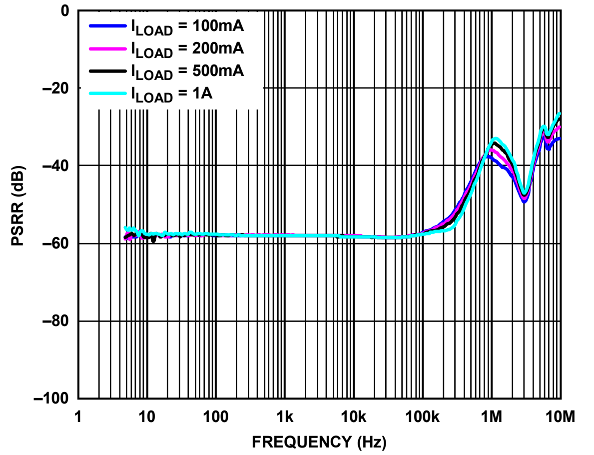

Figure 37. Power Supply Rejection Ratio (PSRR) vs. Frequency, 800 mV Headroom, V_{OUT} = 5 V

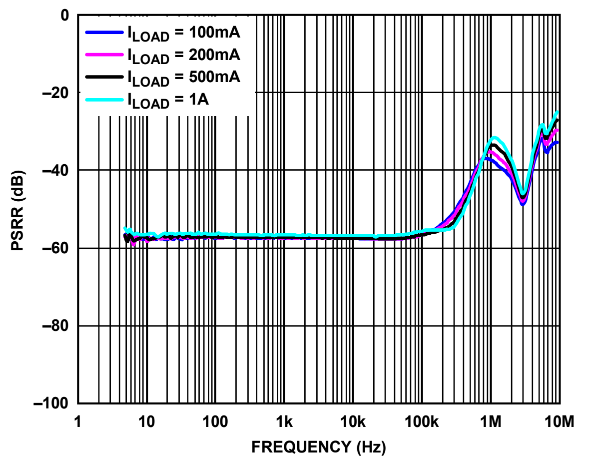

Figure 38. Power Supply Rejection Ratio (PSRR) vs. Frequency, 500 mV Headroom, V_{OUT} = 5 V

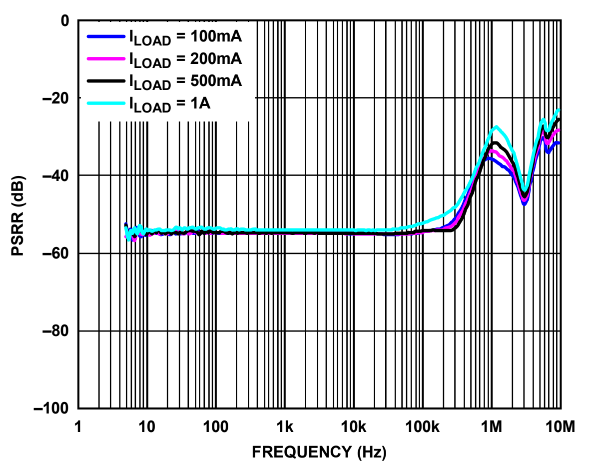

Figure 39. Power Supply Rejection Ratio (PSRR) vs. Frequency, 400 mV Headroom, V_{OUT} = 5 V

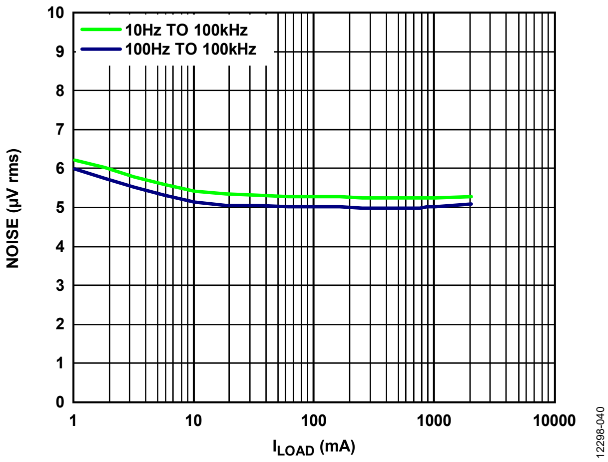

Figure 40. RMS Output Noise vs. Load Current (I_{LOAD}), Adjustable Version, V_{OUT} = 1.2 V

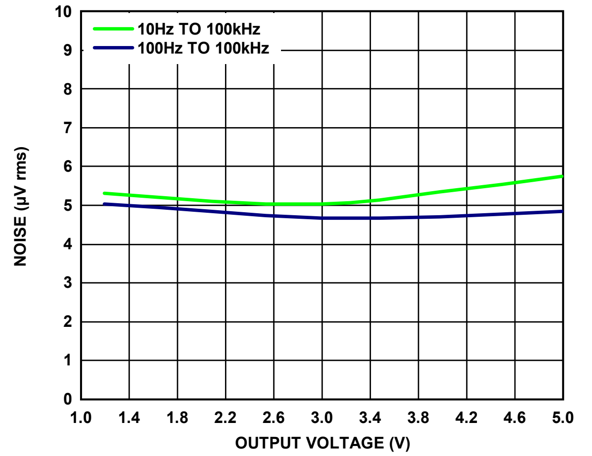

Figure 43. RMS Output Noise vs. Output Voltage, Load Current = 100 mA

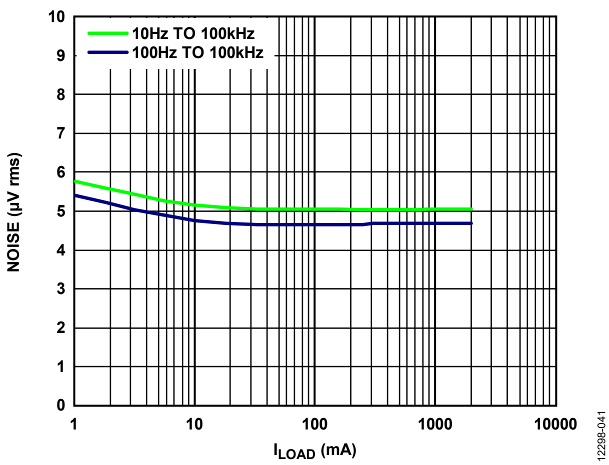

Figure 41. RMS Output Noise vs. Load Current (I_{LOAD}), V_{OUT} = 3 V

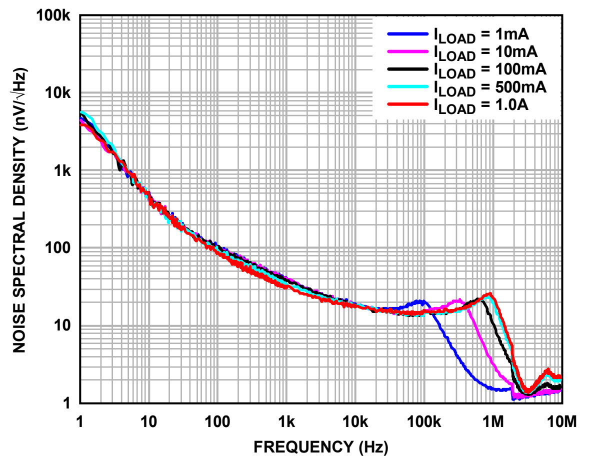

Figure 44. Output Noise Spectral Density, Adjustable Version, V_{OUT} = 1.2 V

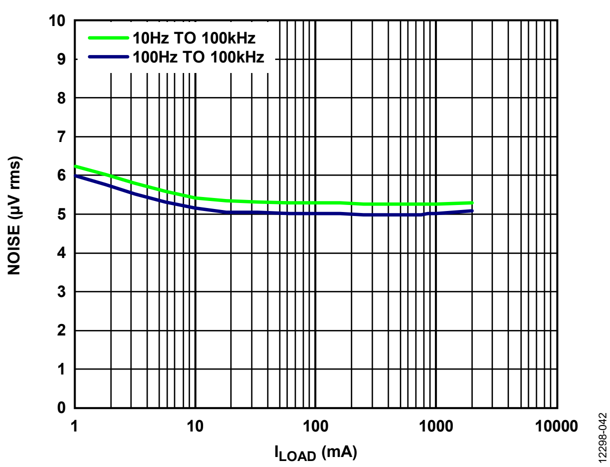

Figure 42. RMS Output Noise vs. Load Current (I_{LOAD}), V_{OUT} = 5 V

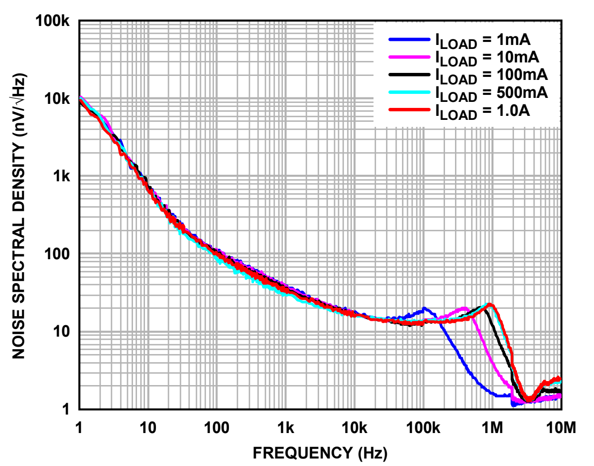

Figure 45. Output Noise Spectral Density, V_{OUT} = 3 V

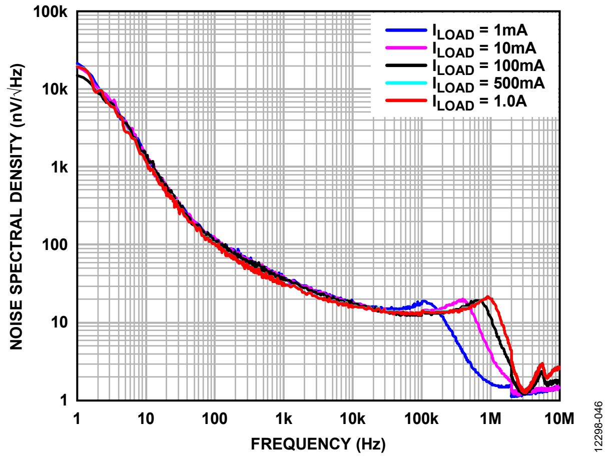

Figure 46. Output Noise Spectral Density, V_{OUT} = 5 V

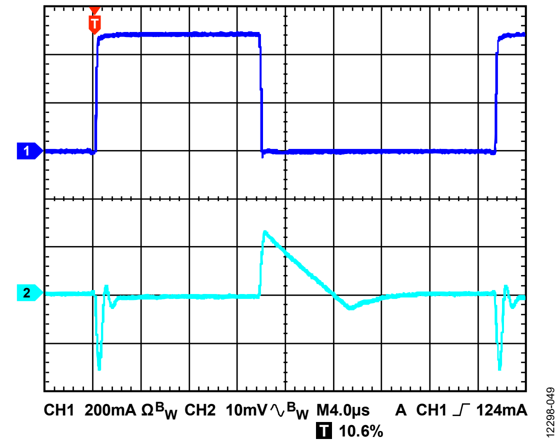

Figure 49. Load Transient Response, I_{LOAD} = 10 mA to 500 mA, V_{OUT} = 5 V, V_{IN} = 5.5 V, CH1= I_{LOAD}, CH2 = V_{OUT}

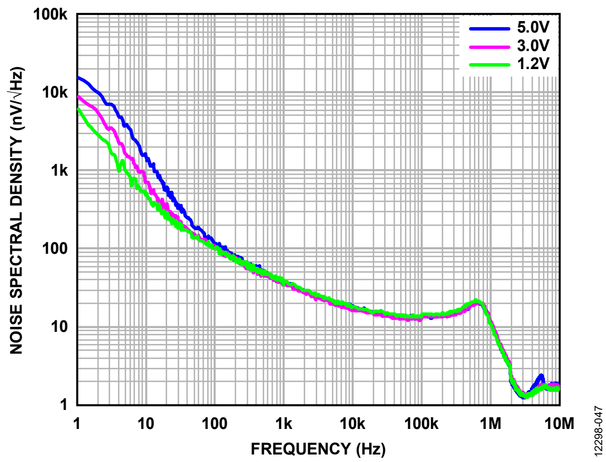

Figure 47. Output Noise Spectral Density, Different Output Voltages, Load Current = 100 mA

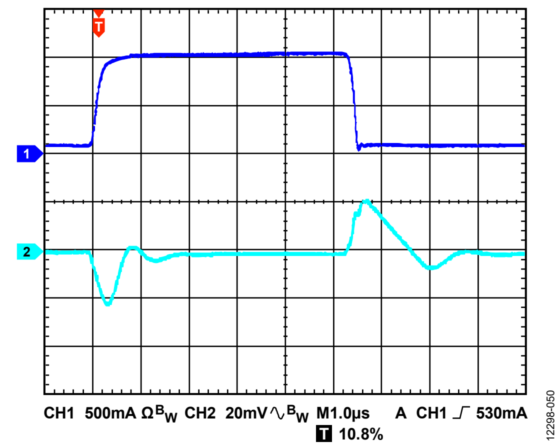

Figure 50. Load Transient Response, I_{LOAD} = 10 mA to 1 A, Adjustable Version, V_{OUT} = 1.2 V, V_{IN} = 2.5 V, CH1 = I_{LOAD}, CH2 = V_{OUT}

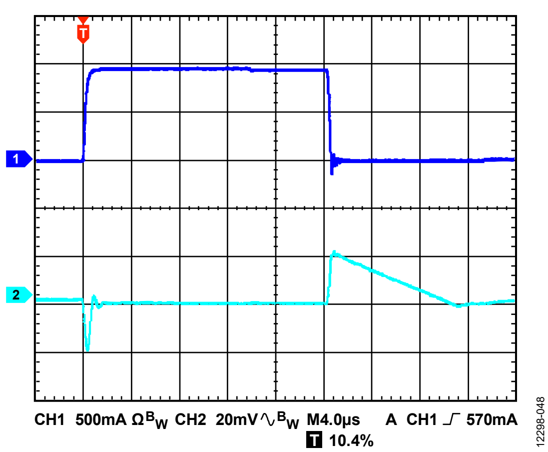

Figure 48. Load Transient Response, I_{LOAD} = 10 mA to 1 A, V_{OUT} = 5 V, V_{IN} = 5.5 V, CH1 = I_{LOAD}, CH2 = V_{OUT}

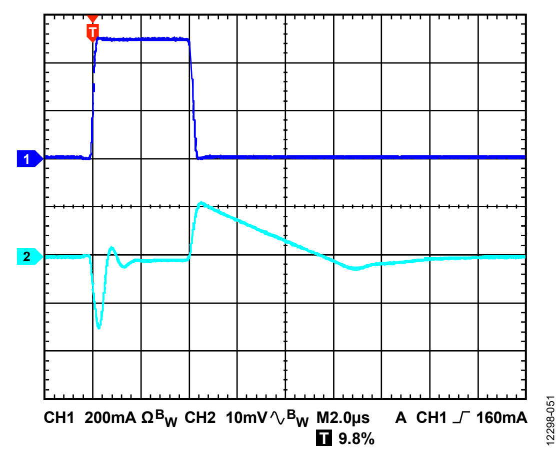

Figure 51. Load Transient Response, I_{LOAD} = 10 mA to 500 mA, Adjustable Version, V_{OUT} = 1.2 V, V_{IN} = 2.5 V, CH1 = I_{LOAD}, CH2 = V_{OUT}

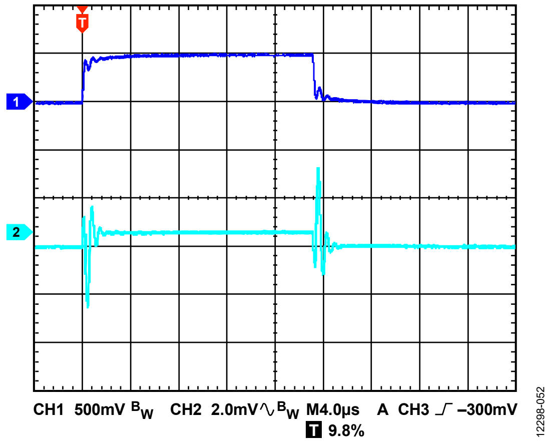

Figure 52. Line Transient Response, 6 V to 6.5 V, I_{LOAD} = 1 A, V_{OUT} = 5 V, CH1 = V_{IN}, CH2 = V_{OUT}

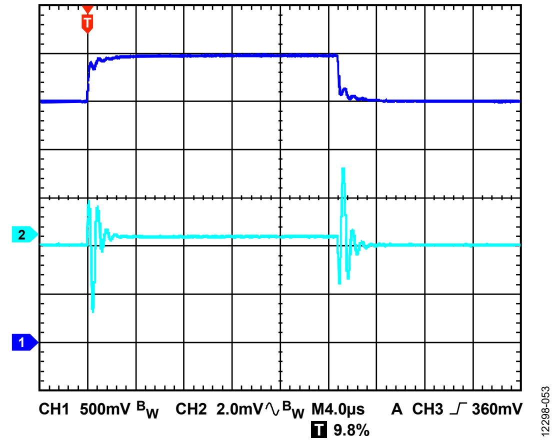

Figure 53. Line Transient Response, 2.5 V to 3 V, I_{LOAD} = 1 A, Adjustable Version, V_{OUT} = 1.2 V, CH1 = V_{IN}, CH2 = V_{OUT}

THEORY OF OPERATION

The ADM7171 is a low quiescent current, low dropout linear regulator that operates from 2.3 V to 6.5 V and provides up to 1 A of load current. Drawing a low 4.0 mA of quiescent current (typical) at full load makes the ADM7171 ideal for portable equipment. Typical shutdown current consumption is 0.25 µA at room temperature.

Optimized for use with small 4.7 µF ceramic capacitors, the ADM7171 provides excellent transient performance.

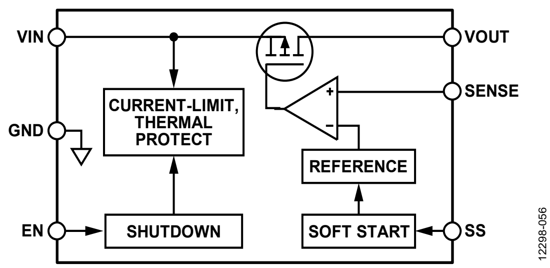

Figure 54. Internal Block Diagram

Internally, the ADM7171 consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. When the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. When the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The ADM7171 is available in 17 fixed output voltage options, ranging from 1.2 V to 5 V. The ADM7171 architecture allows any fixed output voltage to be set to a higher voltage with an external voltage divider. For example, a fixed 5 V output ADM7171 can be set to a 6 V output according to the following equation:

$$V_{OUT} = 5\text{ V}(1 + R1/R2)$$

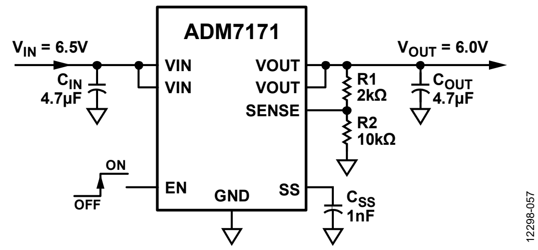

Figure 55. Typical Adjustable Output Voltage Application Schematic

Use a value of less than 200 kΩ for R2 to minimize errors in the output voltage caused by the SENSE pin input current. For example, when R1 and R2 each equal 200 kΩ and the default output voltage is 1.2 V, the adjusted output voltage is 2.4 V. The output voltage error introduced by the SENSE pin input current is 0.1 mV or 0.004%, assuming a typical SENSE pin input bias current of 1 nA at 25°C.

The ADM7171 uses the EN pin to enable and disable the VOUT pins under normal operating conditions. When EN is high, V_{OUT} turns on, when EN is low, V_{OUT} turns off. For automatic startup, tie EN to VIN (Pin 7 or Pin 8).

APPLICATIONS INFORMATION

ADIsimPOWER DESIGN TOOL

The ADM7171 is supported by the ADIsimPower™ design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count, taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about, and to obtain ADIsimPower design tools, visit www.analog.com/ADIsimPower.

CAPACITOR SELECTION

Multilayer ceramic capacitors (MLCC) combine small size, low effective series resistance (ESR), low ESL, and wide operating temperature range, making them an ideal choice for bypass capacitors. They are not without limitations, however. Depending on the dielectric material, the capacitance can vary dramatically with temperature, dc bias, and ac signal level. Therefore, selecting the proper capacitor results in the best circuit performance.

Output Capacitor

The ADM7171 is designed for operation with small, space-saving ceramic capacitors but functions with most commonly used capacitors as long as care is taken with regard to the ESR value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 4.7 µF capacitance with an ESR of 0.05 Ω or less is recommended to ensure the stability of the ADM7171. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADM7171 to large changes in load current. Figure 56 shows the transient responses for an output capacitance value of 4.7 µF.

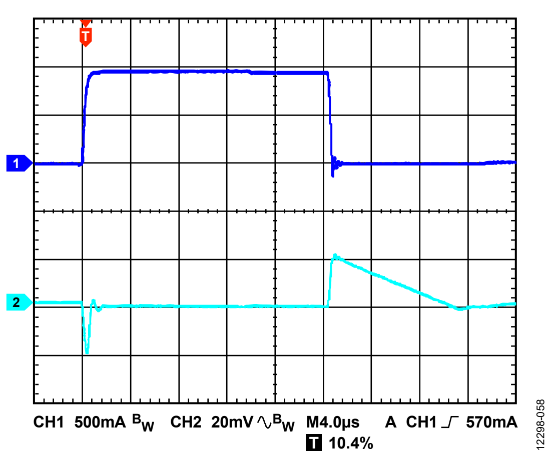

Figure 56. Output Transient Response, V_{OUT} = 5 V, C_{OUT} = 4.7 µF

Input Bypass Capacitor

Connecting a 4.7 µF capacitor from VIN to GND reduces the circuit sensitivity to PCB layout, especially when long input traces or a high source impedance is encountered. If greater than 4.7 µF of output capacitance is required, increase the input capacitor to match it.

Input and Output Capacitor Properties

Any good quality ceramic capacitors can be used with the ADM7171 if they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors require a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V to 100 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

Figure 57 depicts the capacitance vs. dc bias voltage of a 0805, 4.7 µF, 16 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is ~±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

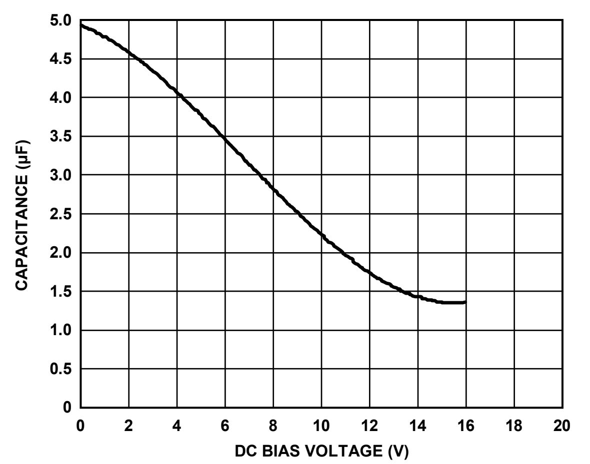

Figure 57. Capacitance vs. DC Bias Voltage

Use Equation 1 to determine the worst case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:
C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst case capacitor temperature coefficient.
TOL is the worst case component tolerance.

In this example, the worst case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{BIAS} is 4.35 µF at 3.0 V, as shown in Figure 57.

Substituting these values in Equation 1 yields

$$C_{EFF} = 4.35\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 3.33\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage of 3.0 V.

To guarantee the performance of the ADM7171, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

PROGRAMMABLE PRECISION ENABLE

The ADM7171 uses the EN pin to enable and disable the VOUT pins under normal operating conditions. As shown in Figure 58, when a rising voltage on EN crosses the upper threshold, typically 1.2 V, V_{OUT} turns on. When a falling voltage on EN crosses the lower threshold, typically 1.1 V, V_{OUT} turns off. The hysteresis of the EN threshold is approximately 100 mV.

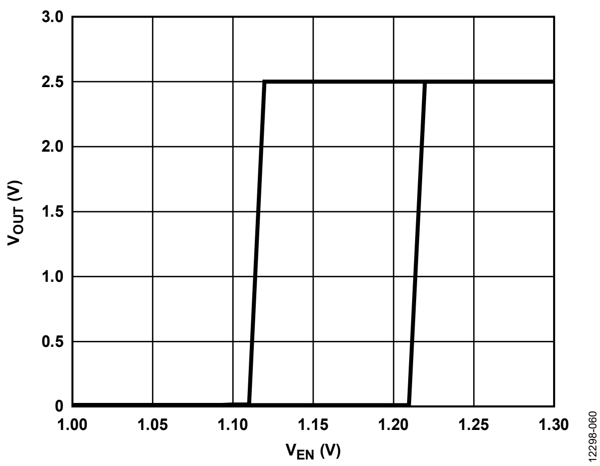

Figure 58. Typical V_{OUT} Response to EN Pin Operation

The upper and lower thresholds are user programmable and can be set higher than the nominal 1.2 V threshold by using two resistors. The resistance values, R_{EN1} and R_{EN2}, can be determined from

$$R_{EN1} = R_{EN2} \times (V_{IN} - 1.2\ V)/1.2\ V$$

where:
R_{EN2} is nominally 10 kΩ to 100 kΩ.
V_{IN} is the desired turn-on voltage.

The hysteresis voltage increases by the factor

$$(R_{EN1} + R_{EN2})/R_{EN1}$$

For the example shown in Figure 59, the enable threshold is 3.6 V with a hysteresis of 300 mV.

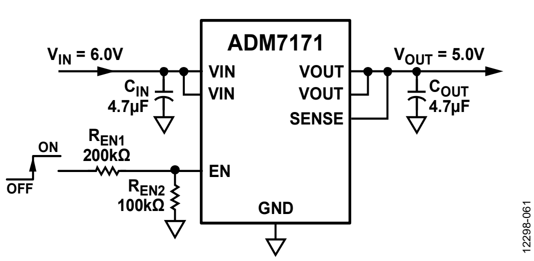

Figure 59. Typical EN Pin Voltage Divider

Figure 58 shows the typical hysteresis of the EN pin. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

UNDERVOLTAGE LOCKOUT

The ADM7171 also incorporates an internal undervoltage lockout circuit to disable the output voltage when the input voltage is less than the minimum input voltage rating of the regulator. The upper and lower thresholds are internally fixed with about 200 mV of hysteresis. This hysteresis prevents on/off oscillations that can occur when caused by noise on the input voltage as it passes through the threshold points.

SOFT START

The ADM7171 uses an internal soft start (SS pin open) to limit the inrush current when the output is enabled. The start-up time for the 5.0 V option is approximately 380 µs from the time the EN active threshold is crossed to when the output reaches 90% of its final value. As shown in Figure 60, the start-up time is nearly independent of the output voltage setting.

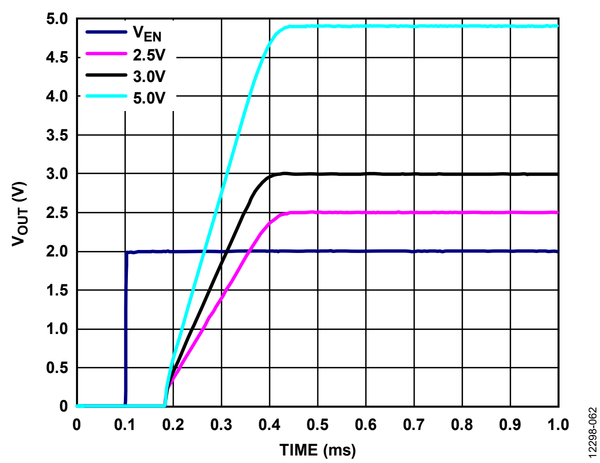

Figure 60. Typical Start-Up Behavior

An external capacitor connected to the SS pin determines the soft start time. The SS pin can be left open for a typical 380 µs start-up time. Do not ground this pin. When an external soft start capacitor is used, the soft start time is determined by the following equation:

$$SS_{TIME}\ (\text{sec}) = t_{START\text{-}UP\ at\ 0\ nF} + (0.6 \times C_{SS})/I_{SS}$$

where:

$t_{START\text{-}UP\ at\ 0\ nF}$ is the start-up time at C_{SS} = 0 nF (typically 380 µs).
C_{SS} is the soft start capacitor (F).
I_{SS} is the soft start current (typically 1 µA).

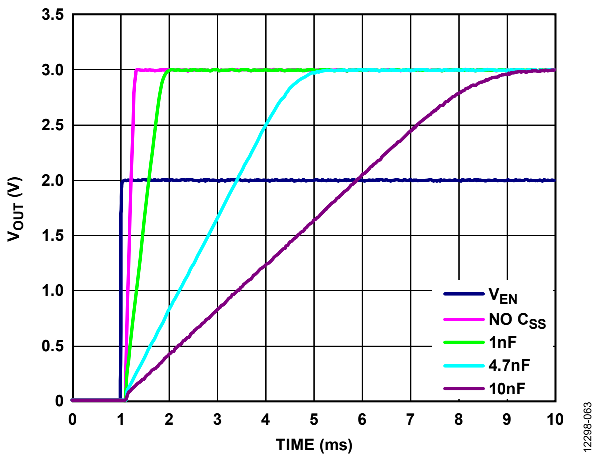

Figure 61. Typical Soft Start Behavior, Different C_{SS} Values

NOISE REDUCTION OF THE ADM7171 IN ADJUSTABLE MODE

The ultralow output noise of the ADM7171 is achieved by keeping the LDO error amplifier in unity gain and setting the reference voltage equal to the output voltage. This architecture does not work for an adjustable output voltage LDO in the conventional sense. However, the ADM7171 architecture allows any fixed output voltage to be set to a higher voltage with an external voltage divider. For example, the adjustable (1.2 V in unity gain) output ADM7171 can be set to a 6 V output according to the following equation:

$$V_{OUT} = 1.2\ \text{V}(1 + R1/R2)$$

The disadvantage of using the ADM7171 in this manner is that the output voltage noise is proportional to the output voltage. Therefore, it is best to choose a fixed output voltage that is close to the target voltage to minimize the increase in output noise.

The adjustable LDO circuit can be modified to reduce the output voltage noise to levels close to that of the fixed output ADM7171. The circuit shown in Figure 62 adds two additional components to the output voltage setting resistor divider. C_{NR} and R_{NR} are added in parallel with R_{FB1} to reduce the ac gain of the error amplifier. R_{NR} is chosen to be small with respect to R_{FB2}. If R_{NR} is 1% to 10% of the value of R_{FB2}, the minimum ac gain of the error amplifier is approximately 0.1 dB to 0.8 dB. The actual gain is determined by the parallel combination of R_{NR} and R_{FB1}. This ensures that the error amplifier always operates at slightly greater than unity gain.

C_{NR} is chosen by setting the reactance of C_{NR} equal to R_{FB1} − R_{NR} at a frequency between 0.5 Hz and 10 Hz. This sets the frequency where the ac gain of the error amplifier is 3 dB less than its dc gain.

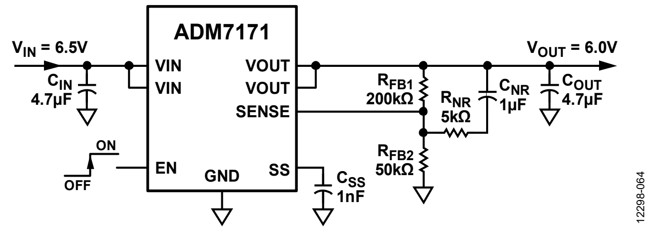

Figure 62. Noise Reduction Modification

Assuming the noise of a fixed output LDO is approximately 5 µV, identify the noise of the adjustable LDO by using the following formula:

$$Noise = 5\ \mu\text{V} \times (R_{PAR} + R_{FB2})/R_{FB2}$$

where R_{PAR} is the parallel combination of R_{FB1} and R_{NR}.

Based on the component values shown in Figure 62, the ADM7171 has the following characteristics:

- DC gain of 5 (14 dB)
- 3 dB roll-off frequency of 0.8 Hz
- High frequency ac gain of 1.09 (0.75 dB)
- Noise reduction factor of 4.42 (12.91 dB)
- RMS noise of the adjustable LDO without noise reduction of 25 µV rms
- RMS noise of the adjustable LDO with noise reduction (assuming 5 µV rms for fixed voltage option) of 5.5 µV rms

EFFECT OF NOISE REDUCTION ON START-UP TIME

The start-up time of the ADM7171 is affected by the noise reduction network and must be considered in applications wherein power supply sequencing is critical.

The noise reduction circuit adds a pole in the feedback loop that slows down the start-up time. The start-up time for an adjustable model with a noise reduction network can be approximated using the following equation:

$$SSNR_{TIME}\ (\text{sec}) = 5.5 \times C_{NR} \times (R_{NR} + R_{FB1})$$

For a C_{NR}, R_{NR}, and R_{FB1} combination of 1 µF, 5 kΩ, and 200 kΩ, respectively, as shown in Figure 62, the start-up time is approximately 1.1 seconds. When $SSNR_{TIME}$ is greater than SS_{TIME}, it dictates the length of the start-up time instead of the soft start capacitor.

CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The ADM7171 is protected against damage due to excessive power dissipation by current-limit and thermal overload protection circuits. The ADM7171 is designed to current limit when the output load reaches 3 A (typical). When the output load exceeds 3 A, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and/or high power dissipation) when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 135°C, the output is turned on again, and the output current is restored to its operating value.

Consider the case where a hard short from VOUT to ground occurs. At first, the ADM7171 current limits, so that only 3 A is conducted into the short. If self heating of the junction is great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 3 A into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 3 A and 0 mA that continues for as long as the short remains at the output.

Current-limit and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that the junction temperature does not exceed 125°C.

THERMAL CONSIDERATIONS

In applications with low input-to-output voltage differential, the ADM7171 does not dissipate much heat. However, in applications with high ambient temperature and/or high input voltage, the heat dissipated in the package may become large enough that it causes the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 150°C, the converter enters thermal shutdown. It recovers only after the junction temperature has decreased below 135°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is very important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the ADM7171 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds that are used and the amount of copper used to solder the package GND pin to the PCB.

Table 7 shows typical θ_{JA} values of the 8-lead LFCSP package for various PCB copper sizes. The typical value of Ψ_{JB} is 15.1°C/W for the 8-lead LFCSP package.

Table 7. Typical θ_{JA} Values

Copper Size (mm^2)	θ_{JA} (°C/W) of LFCSP
25[1]	165.1
100	125.8
500	68.1
1000	56.4
6400	42.1

[1] Device soldered to minimum size pin traces.

The junction temperature of the ADM7171 is calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (3)$$

where:
I_{LOAD} is the load current.
I_{GND} is the ground current.
V_{IN} and V_{OUT} are the input and output voltages, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + (((V_{IN} - V_{OUT}) \times I_{LOAD}) \times \theta_{JA}) \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input-to-output voltage differential, and continuous load current, a minimum copper size requirement exists for the PCB to ensure that the junction temperature does not rise above 125°C. Figure 63 to Figure 65 show junction temperature calculations for different ambient temperatures, power dissipation, and areas of PCB copper.

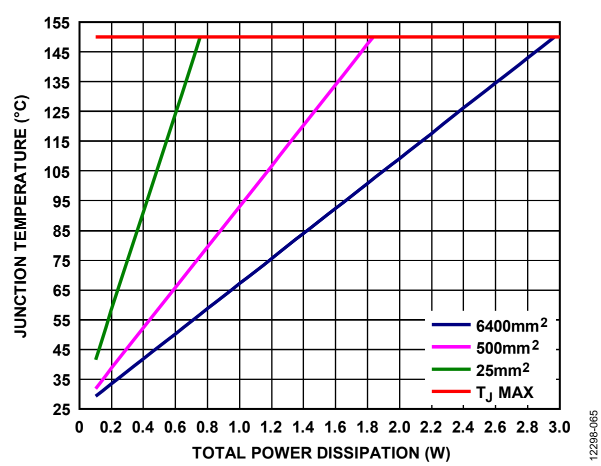

Figure 63. LFCSP, T_A = 25°C

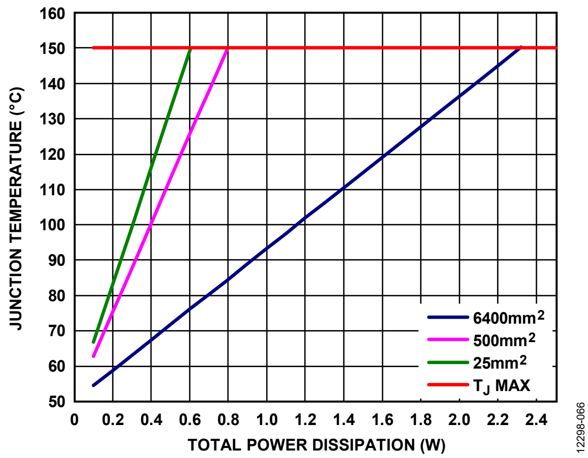

Figure 64. LFCSP, $T_A = 50°C$

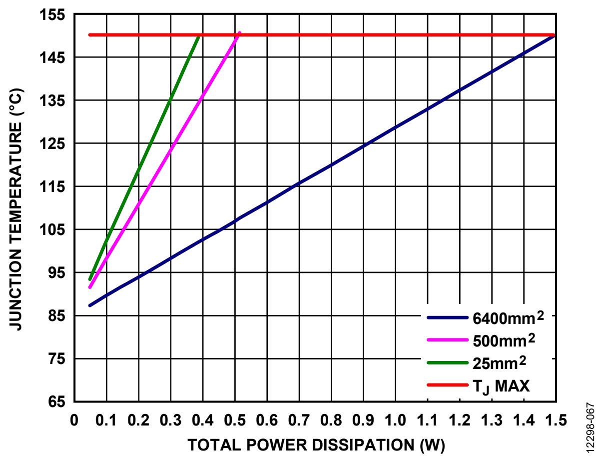

Figure 65. LFCSP, $T_A = 85°C$

In the case where the board temperature is known, use the thermal characterization parameter, Ψ_{JB}, to estimate the junction temperature rise. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (5)$$

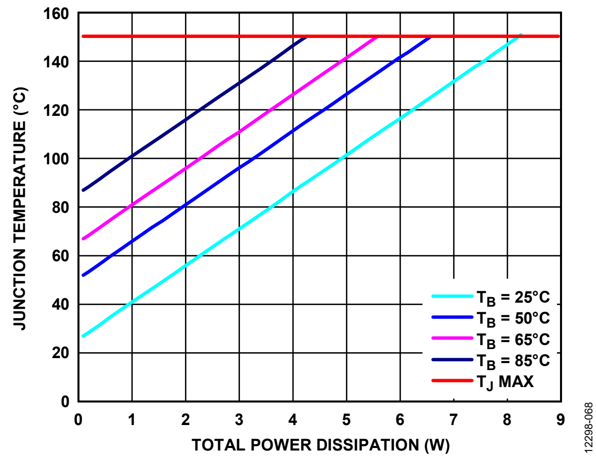

Figure 66. LFCSP Power Dissipation for Various Board Temperatures

TYPICAL APPLICATIONS CIRCUITS

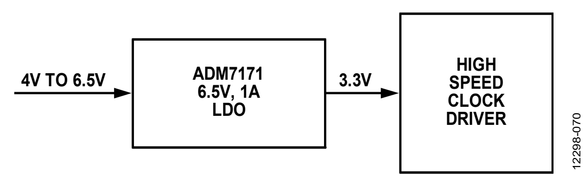

Figure 67. Clock Driver Power

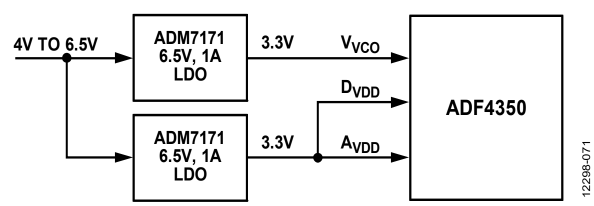

Figure 68. RF PLL/VCO Power

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADM7171. However, as listed in Table 7, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUT and GND pins. Use of 0805 or 1206 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

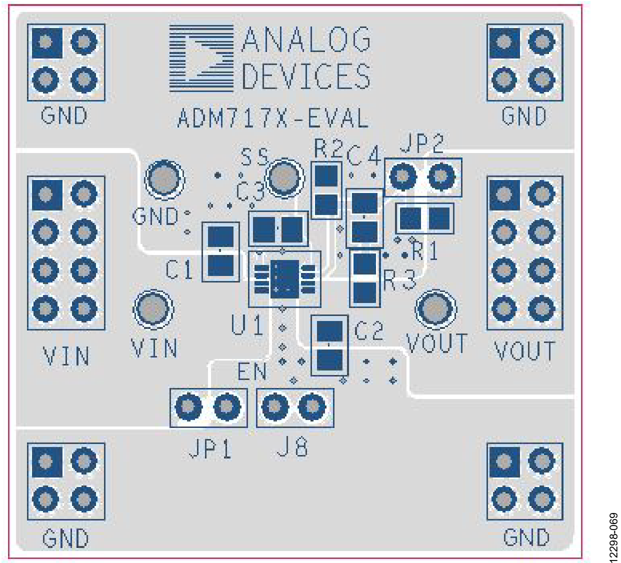

Figure 69. Example LFCSP PCB Layout

OUTLINE DIMENSIONS

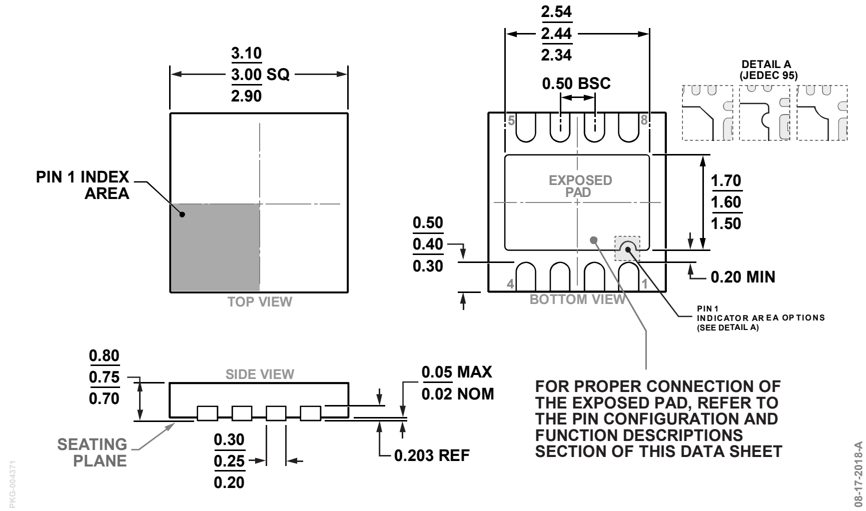

Figure 70. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-21)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage (V)[2, 3]	Package Description	Package Option	Marking Code
ADM7171ACPZ-1.3-R7	−40°C to +125°C	1.3	8-Lead LFCSP	CP-8-21	LPX
ADM7171ACPZ-1.8-R7	−40°C to +125°C	1.8	8-Lead LFCSP	CP-8-21	LPY
ADM7171ACPZ-2.5-R7	−40°C to +125°C	2.5	8-Lead LFCSP	CP-8-21	LR3
ADM7171ACPZ-3.0-R7	−40°C to +125°C	3.0	8-Lead LFCSP	CP-8-21	LPZ
ADM7171ACPZ-3.3-R7	−40°C to +125°C	3.3	8-Lead LFCSP	CP-8-21	LQ0
ADM7171ACPZ-4.2-R7	−40°C to +125°C	4.2	8-Lead LFCSP	CP-8-21	LQX
ADM7171ACPZ-5.0-R7	−40°C to +125°C	5.0	8-Lead LFCSP	CP-8-21	LQ1
ADM7171ACPZ-R7	−40°C to +125°C	Adjustable (1.2 V)	8-Lead LFCSP	CP-8-21	LQ2
ADM7171ACPZ-R2	−40°C to +125°C	Adjustable (1.2 V)	8-Lead LFCSP	CP-8-21	LQ2
ADM7171CP-EVALZ		Evaluation Board			

[1] Z = RoHS Compliant Part.
[2] For additional voltage options, contact a local Analog Devices, Inc., sales or distribution representative.
[3] The evaluation board is preconfigured with an adjustable voltage (1.2 V) preset to a 3.0 V ADM7171.

D12298-0-9/19(E)