6.5 V, 2 A, Ultralow Noise, High PSRR, Fast Transient Response CMOS LDO

Known Good Die

ADM7172-KGD

FEATURES

- Input voltage range: 2.3 V to 6.5 V
- Maximum load current: 2 A
- Low noise: 5 µV rms independent of output voltage at 100 Hz to 100 kHz
- Fast transient response: 1.5 µs for 1 mA to 1.5 A load step
- 60 dB PSRR at 100 kHz
- Low dropout voltage: 172 mV at 2 A load, V_{OUT} = 3 V
- Initial accuracy: −0.5% (minimum), +1% (maximum)
- Accuracy over line, load, and temperature: ±1.5%
- Quiescent current, I_{GND} = 0.7 mA with no load
- Low shutdown current: 0.25 µA at V_{IN} = 5 V
- Stable with small 4.7 µF ceramic output capacitor
- Adjustable and fixed output voltage options: 1.2 V to 5.0 V
- Adjustable output from 1.2 V to V_{IN} − V_{DO}
- Precision enable
- Adjustable soft start

APPLICATIONS

- Regulation to noise sensitive applications: analog-to-digital converter (ADC) and digital-to-analog converter (DAC) circuits, precision amplifiers, phase-locked loops (PLLs)/ voltage controlled oscillators (VCOs), and clocking ICs
- Communications and infrastructure
- Medical and healthcare
- Industrial and instrumentation

GENERAL DESCRIPTION

The ADM7172-KGD is a CMOS, low dropout linear regulator (LDO) that operates from 2.3 V to 6.5 V and provides up to 2 A of output current. This high output current LDO is ideal for regulation of high performance analog and mixed-signal circuits operating from 6 V down to 1.2 V rails. Using an advanced proprietary architecture, the device provides high power supply rejection and low noise and achieves excellent line and load transient response with just a small 4.7 µF ceramic output capacitor. Load transient response is typically 1.5 µs for a 1 mA to 1.5 A load step.

The ADM7172-KGD is available in a 4.2 V fixed output voltage option. Additional voltages that are available by special order are 1.3 V, 1.5 V, 1.8 V, 1.85 V, 2.0 V, 2.2 V, 2.5 V, 2.7 V, 2.75 V, 2.8 V, 2.85 V, 3.0 V, 3.8 V, 3.3 V, 4.2 V, 4.6 V, 5.0 V, and an adjustable output option.

Inrush current can be controlled by adjusting the start-up time via the soft start pin. The typical start-up time with a 1 nF soft start capacitor is 1.0 ms.

The ADM7172-KGD regulator output noise is 5 µV rms, independent of the output voltage.

Additional application and technical information can be found in the ADM7172 data sheet.

Rev. A Document Feedback

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REVISION HISTORY

3/16—Rev. A to Rev. B

Changes to General Description Section ... 1

9/15—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = (V_{OUT} + 0.5 V) or 2.3 V (whichever is greater), EN = V_{IN}, I_{LOAD} = 10 mA, C_{IN} = C_{OUT} = 4.7 μF, T_A = 25°C for typical specifications, T_J = −40°C to +125°C for minimum/maximum specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}		2.3		6.5	V
LOAD CURRENT	I_{LOAD}				2	A
OPERATING SUPPLY CURRENT	I_{GND}	I_{LOAD} = 0 μA		0.7	2.0	mA
		I_{LOAD} = 2 A		4.8	8.7	mA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND, V_{IN} = 5 V		0.25	3.8	μA
OUTPUT VOLTAGE ACCURACY						
Fixed Output Voltage Accuracy	V_{OUT}	I_{LOAD} = 10 mA, T_J = 25°C	−0.5		+1	%
		100 μA < I_{LOAD} < 2 A, V_{IN} = (V_{OUT} + 0.5 V) to 6.5 V	−1.5		+1.5	%
Adjustable Output Voltage Accuracy	V_{SENSE}	I_{LOAD} = 10 mA	1.194	1.200	1.212	V
		10 mA < I_{LOAD} < 2 A, V_{IN} = (V_{OUT} + 0.5 V) to 6.5 V	1.182		1.218	V
REGULATION						
Line	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.5 V) to 6.5 V	−0.1		+0.1	%/V
Load	$\Delta V_{OUT}/\Delta I_{LOAD}$	I_{LOAD} = 100 μA to 2 A		0.1	0.3	%/A
SENSE INPUT BIAS CURRENT	$SENSE_{I-BIAS}$	100 μA < I_{LOAD} < 2 A, V_{IN} = (V_{OUT} + 0.5 V) to 6.5 V		1		nA
DROPOUT VOLTAGE[1]	$V_{DROPOUT}$	I_{LOAD} = 500 mA, V_{OUT} = 3 V		42	70	mV
		I_{LOAD} = 1 A, V_{OUT} = 3 V		84	135	mV
		I_{LOAD} = 2 A, V_{OUT} = 3 V		172	270	mV
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, all fixed output voltages		6		μV rms
		100 Hz to 100 kHz, all fixed output voltages		5		μV rms
Noise Spectral Density		100 Hz, all fixed output voltages		110		nV/√Hz
		1 kHz, all fixed output voltages		40		nV/√Hz
		10 kHz, all fixed output voltages		20		nV/√Hz
		100 kHz, all fixed output voltages		12		nV/√Hz
POWER SUPPLY REJECTION RATIO	PSRR	100 kHz, V_{IN} = 4.0 V, V_{OUT} = 3 V, I_{LOAD} = 1.5 A, C_{SS} = 0 nF		60		dB
		100 kHz, V_{IN} = 3.5 V, V_{OUT} = 3 V, I_{LOAD} = 1.5 A, C_{SS} = 0 nF		53		dB
		100 kHz, V_{IN} = 3.3 V, V_{OUT} = 3 V, I_{LOAD} = 1.5 A, C_{SS} = 0 nF		42		dB
		1 MHz, V_{IN} = 4.0 V, V_{OUT} = 3 V, I_{LOAD} = 1.5 A, C_{SS} = 0 nF		31		dB
		1 MHz, V_{IN} = 3.5 V, V_{OUT} = 3 V, I_{LOAD} = 1.5 A, C_{SS} = 0 nF		30		dB
		1 MHz, V_{IN} = 3.3 V, V_{OUT} = 3 V, I_{LOAD} = 1.5 A, C_{SS} = 0 nF		20		dB
TRANSIENT LOAD RESPONSE	t_{TR-REC}	Time for output voltage to settle within ±V_{SETTLE} from V_{DEV} for a 1 mA to 1.5 A load step, load step rise time = 400 ns		1.5		μs
	V_{DEV}	Output voltage deviation due to 1 mA to 1.5 A load step		35		mV
	V_{SETTLE}	Output voltage deviation after transient load response time (t_{TR-REC}) has passed, V_{OUT} = 5 V, C_{OUT} = 4.7 μF		0.1		%
START-UP TIME[2]	$t_{START-UP}$	V_{OUT} = 5 V, C_{SS} = 0 nF		380		μs
		V_{OUT} = 5 V, C_{SS} = 1 nF		1.0		ms
SOFT START CURRENT	I_{SS}	V_{IN} = 5 V	0.5	1	1.5	μA
CURRENT-LIMIT THRESHOLD[3]	I_{LIMIT}		2.4	3.3	3.9	A
V_{OUT} PULL-DOWN RESISTANCE	$V_{OUT-PULL}$	EN = 0 V, V_{OUT} = 1 V		11		kΩ
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
UNDERVOLTAGE THRESHOLDS						
Input Voltage Rising	$UVLO_{RISE}$				2.28	V
Input Voltage Falling	$UVLO_{FALL}$		1.94			V
Hysteresis	$UVLO_{HYS}$			200		mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
EN INPUT STANDBY		$2.3\ V \leq V_{IN} \leq 6.5\ V$				
EN Input Logic High	$EN_{STBY\text{-}HIGH}$		1.1			V
EN Input Logic Low	$EN_{STBY\text{-}LOW}$				0.4	V
EN Input Logic Hysteresis	$EN_{STBY\text{-}HYS}$			80		mV
EN INPUT PRECISION		$2.3\ V \leq V_{IN} \leq 6.5\ V$				
EN Input Logic High	EN_{HIGH}		1.11	1.2	1.27	V
EN Input Logic Low	EN_{LOW}		1.01	1.1	1.16	V
EN Input Logic Hysteresis	EN_{HYS}			100		mV
EN Input Leakage Current	$I_{EN\text{-}LKG}$	EN = V_{IN} or GND		0.1	1.0	µA
EN Input Delay Time	$TI_{EN\text{-}DLY}$	From EN rising from 0 V to V_{IN} to 0.1 V × V_{OUT}		130		µs

[1] Dropout voltage is defined as the input to output voltage differential when the input voltage is set to the nominal output voltage. Dropout applies only for output voltages greater than 2.3 V.
[2] Start-up time is defined as the time between the rising edge of EN to VOUT being at 90% of the nominal value.
[3] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 5.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 5.0 V, or 4.5 V.

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
MINIMUM INPUT AND OUTPUT CAPACITANCE[1]	C_{MIN}	T_A = −40°C to +125°C	3.3			µF
CAPACITOR ESR	R_{ESR}	T_A = −40°C to +125°C	0.001		0.05	Ω

[1] Ensure that the minimum input and output capacitance is greater than 3.3 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to GND	−0.3 V to +7 V
VOUT to GND	−0.3 V to V_{IN}
EN to GND	−0.3 V to +7 V
SS to GND	−0.3 V to V_{IN}
SENSE to GND	−0.3 V to +7 V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

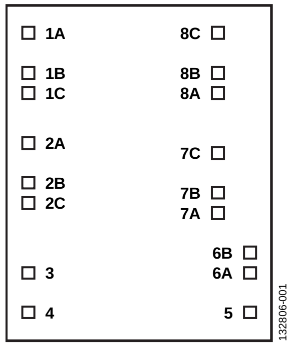

Figure 1. Pad Configuration

Table 4. Pad Function Descriptions

Pad	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Pad Type	Description
1A	−392.275	+799.55	VOUT1A	Triple	Regulated Output Voltage, Triple Bond Pad.
1B	−392.275	+607.9	VOUT1B	Triple	Regulated Output Voltage, Triple Bond Pad.
1C	−392.275	+483.05	VOUT1C	Triple	Regulated Output Voltage, Triple Bond Pad.
2A	−392.275	+306.2	VOUT2A	Triple	Regulated Output Voltage, Triple Bond Pad.
2B	−392.275	+120.8	VOUT2B	Triple	Regulated Output Voltage, Triple Bond Pad.
2C	−392.275	−8.35	VOUT2C	Triple	Regulated Output Voltage, Triple Bond Pad.
3	−392.25	−424.55	SENSE	Single	Sense Input.
4	−392.25	−660.925	SS	Single	Soft Start.
5	+400	−501.6	EN	Single	Regulator Enable.
6A	+399.8	−366.225	GNDA	Double	Ground, Double Bond Pad.
6B	+399.8	−271.225	GNDB	Double	Ground, Double Bond Pad.
7A	+246.6	−70.8	VIN1A	Triple	Regulator Input Supply, Triple Bond Pad.
7B	+246.6	+33.7	VIN1B	Triple	Regulator Input Supply, Triple Bond Pad.
7C	+246.6	+268.9	VIN1C	Triple	Regulator Input Supply, Triple Bond Pad.
8A	+246.6	+462.75	VIN2A	Triple	Regulator Input Supply, Triple Bond Pad.
8B	+246.6	+588.7	VIN2B	Triple	Regulator Input Supply, Triple Bond Pad.
8C	+246.6	+818.1	VIN2C	Triple	Regulator Input Supply, Triple Bond Pad.

OUTLINE DIMENSIONS

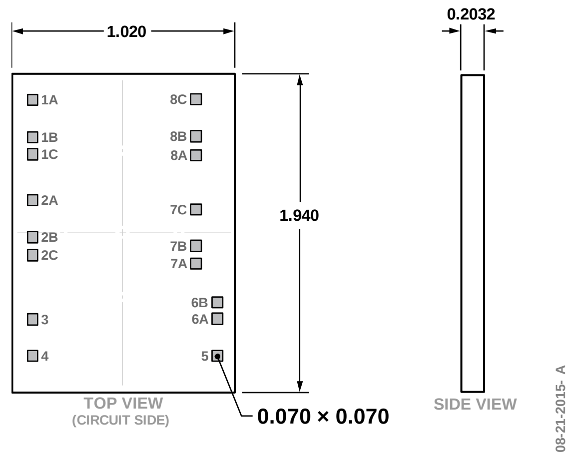

Figure 2. 8-Pad Bare Die [CHIP]
(C-8-5)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 5. Die Specifications

Parameter	Value	Unit
Die Size (Maximum)	1020 × 1940	µm
Bond Pad (Minimum)	70 × 70	µm
Thickness	203.2	µm
Scribe Line Width	80	µm
Bond Pad Composition	AlCu (0.5%)	%
Passivation Type	Nitride	Not applicable
Backside Bias	GND	Not applicable

Table 6. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Ablestik 8290
Bonding Method	1.2 mil gold

ORDERING GUIDE

Model	Output Voltage (V)	Temperature Range	Package Description	Package Option
ADM7172-4.2-KGD-WP	4.2	−40°C to +125°C	8-Pad Bare Die [CHIP]	C-8-5

ANALOG DEVICES

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