12.6 GHz to 15.4 GHz, GaAs, MMIC, I/Q Downconverter

Data Sheet **ADMV1010**

FEATURES

- **RF input frequency range: 12.6 GHz to 15.4 GHz**
- **IF output frequency range: 2.7 GHz to 3.5 GHz**
- **LO input frequency range: 9 GHz to 12.6 GHz**
- **Power conversion gain: 15 dB typical**
- **Image rejection: 25 dB typical**
- **SSB noise figure: 2 dB typical**
- **Input IP3: 1 dBm typical**
- **Input P1dB: −7 dBm typical**
- **Single-ended, 50 Ω RF and LO input ports**
- **4.9 mm × 4.9 mm, 32-terminal LCC with exposed pad**

APPLICATIONS

- **Point to point microwave radios**
- **Radars and electronic warfare systems**
- **Instrumentation and automatic test equipment**
- **Satellite communications**

FUNCTIONAL BLOCK DIAGRAM

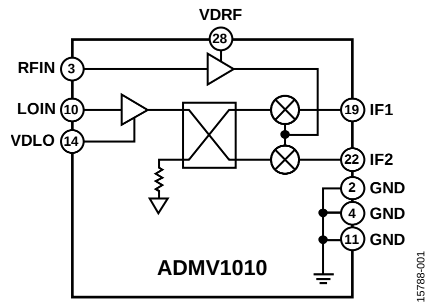

Figure 1.

GENERAL DESCRIPTION

The ADMV1010 is a compact, gallium arsenide (GaAs) design, monolithic microwave integrated circuit (MMIC), I/Q downconverter in a RoHS compliant package optimized for point to point microwave radio designs that operates in the 12.6 GHz to 15.4 GHz frequency range. The ADMV1010 is optimized to work as a low noise, upper sideband (low-side local oscillator (LO)), image reject downconverter.

The ADMV1010 provides 15 dB of conversion gain with 25 dB of image rejection. The ADMV1010 uses a radio frequency (RF), low noise amplifier (LNA) followed by an in-phase/quadrature (I/Q) double balanced mixer, where a driver amplifier drives the LO. IF1 and IF2 mixer outputs are provided, and an external 90° hybrid is needed to select the required sideband. The I/Q mixer topology reduces the need for filtering the unwanted sideband. The ADMV1010 is a much smaller alternative to hybrid style SSB downconverter assemblies, and it eliminates the need for wire bonding by allowing the use of surface-mount manufacturing assemblies.

The ADMV1010 downconverter comes in a compact, thermally enhanced, 4.9 mm × 4.9 mm, 32-terminal LCC package. The ADMV1010 operates over the −40°C to +85°C temperature range.

Rev. B Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support **www.analog.com**

TABLE OF CONTENTS

REVISION HISTORY

4/2018—Rev. A to Rev. B

Changes to Thermal Resistance Section ... 4
Changes to Figure 2 and Table 4 ... 5

1/2018—Rev. 0 to Rev. A

Changes to General Description and Figure 1 ... 1
Changes to Table 1 ... 3
Changes to Table 2 ... 4
Added Thermal Resistance Section and Table 3; Renumbered Sequentially ... 4
Changes to Figure 2 and Table 4 ... 5
Changes to Figure 4 ... 6
Changes to Figure 11 and Figure 12 ... 7
Changes to Figure 16 through Figure 18 ... 8
Changes to Figure 21 and Figure 22 ... 9
Changes to Figure 26 through Figure 28 ... 10
Changes to Figure 31 and Figure 32 ... 11
Changes to Figure 35 and Figure 36 ... 12
Changes to Figure 37 through Figure 40 ... 13
Changes to Figure 44 through Figure 46 ... 14
Changes to M × N Spurious Performance Section and Table 5 ... 15
Changes to Applications Information Section and Figure 47 ... 17
Changes to Ordering Guide ... 21

10/2017—Revision 0: Initial Version

SPECIFICATIONS

Data taken at VDRF = 4 V, VDLO = 4 V, LO = −4 dBm ≤ LO ≤ +4 dBm, −40°C ≤ T_A ≤ +85°C; data taken using Mini-Circuits QCN-45+ power splitter as upper sideband (low-side LO), unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT FREQUENCY RANGE			12.6		15.4	GHz
LO						
Input Frequency Range			9		12.6	GHz
Amplitude			−4	0	+4	dBm
IF OUTPUT FREQUENCY RANGE			2.7		3.5	GHz
RF PERFORMANCE		With hybrid				
Conversion Gain			11	15	17	dB
SSB Noise Figure	SSB NF			2	2.6	dB
Input Third-Order Intercept	IP3	At −23 dBm/tone	−0.5	+1		dBm
Input 1 dB Compression Point	P1dB		−10	−8		dBm
Image Rejection			20	35		dB
Leakage						
LO to RF				−35	−25	dBm
LO to IF				−20	−15	dBm
IM3 at Input						
−20 dBm Input Power			46	49		dBc
−25 dBm Input Power			52	55		dBc
−30 dBm Input Power			56	59		dBc
Return Loss						
RF Input				−12	−10	dB
IF Output				−15	−10	dB
LO Input				−15	−10	dB
POWER INTERFACE						
Voltage						
RF	VDRF			4		V
LO	VDLO			4		V
Current						
RF	IDRF			78	100	mA
LO	IDLO			83	100	mA
Total Power				0.7	0.8	W

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	
VDRF	5.5 V
VDLO	5.5 V
RF Input Power	15 dBm
LO Input Power	15 dBm
Maximum Junction Temperature (T_J)	175°C
Maximum Power Dissipation	1.7 W
Lifetime at Maximum Junction Temperature	>1 million hours
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	260°C
Moisture Sensitivity Level (MSL) Rating	MSL3
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	250 V
Field Induced Charged Device Model (FICDM)	500 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is thermal resistance, junction to ambient (°C/W), and θ_{JC} is thermal resistance, junction to case (°C/W).

Table 3.

Package Type	θ_{JA}[1]	θ_{JC}[1]	Unit
E-32-1	33.4	51	°C/W

[1] See JEDEC standard JESD51-2 for additional information on optimizing the thermal impedance (PCB with 3 × 3 vias).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

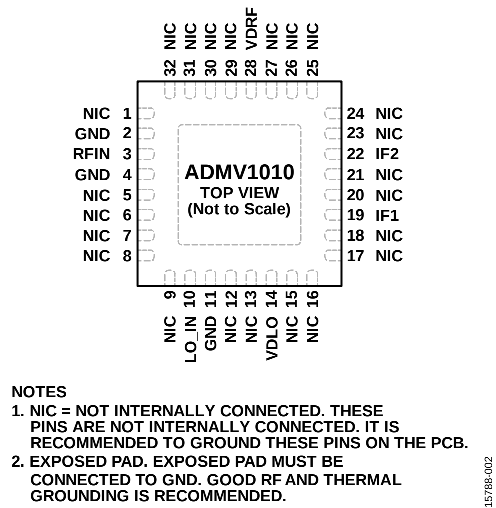

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5 to 9, 12, 13, 15 to 18, 20, 21, 23 to 27, 29 to 32	NIC	Not Internally Connected. These pins are not internally connected. It is recommended to ground these pins on the PCB.
2, 4, 11	GND	Ground.
3	RFIN	RF Input. This pin is ac-coupled internally and matched to 50 Ω, single-ended.
10	LO_IN	LO Input. This pin is ac-coupled internally and matched to 50 Ω single-ended.
14	VDLO	Power Supply Voltage for the LO Amplifier. Refer to the Applications Information section for the required external components and biasing.
19	IF1	Quadrature IF Output 1. Matched to 50 Ω and ac coupled. No external dc block required.
22	IF2	Quadrature IF Output 2. Matched to 50 Ω and ac coupled. No external dc block required.
28	VDRF	Power Supply Voltage for the RF Amplifier. Refer to the Applications Information section for the required external components and biasing.
	EPAD	Exposed Pad. The exposed pad must be connected to GND. Good RF and thermal grounding is recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

IF FREQUENCY = 2.7 GHz

Data taken at VDRF = 4 V, VDLO = 4 V, LO = −4 dBm ≤ LO ≤ +4 dBm, −40°C ≤ T_A ≤ +85°C, data taken with Mini-Circuits QCN-45+ power splitter as upper sideband (low-side LO), unless otherwise noted.

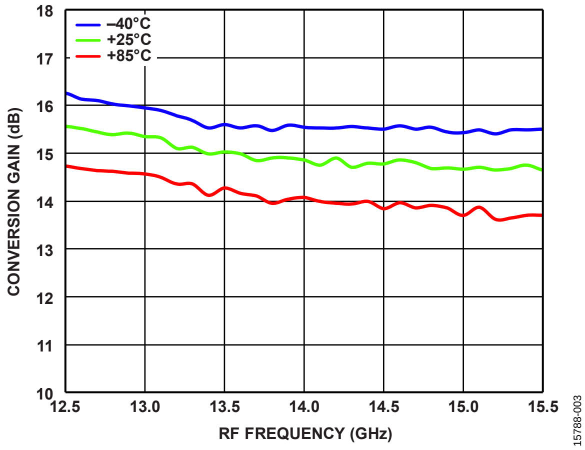

Figure 3. Conversion Gain vs. RF Frequency at Various Temperatures

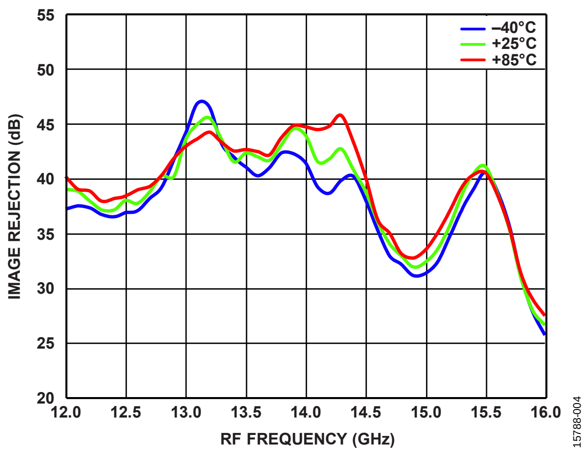

Figure 4. Image Rejection vs. RF Frequency at Various Temperatures

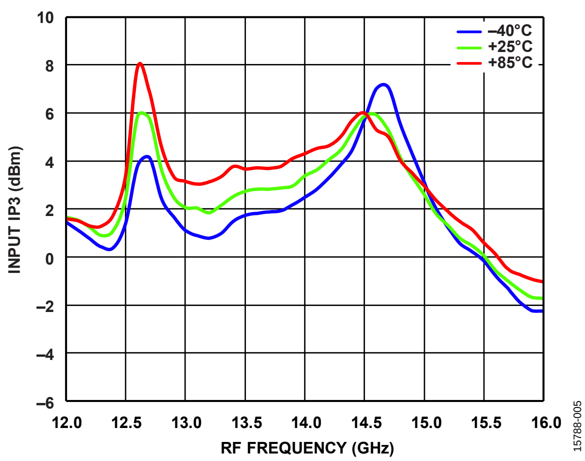

Figure 5. Input IP3 vs. RF Frequency at Various Temperatures

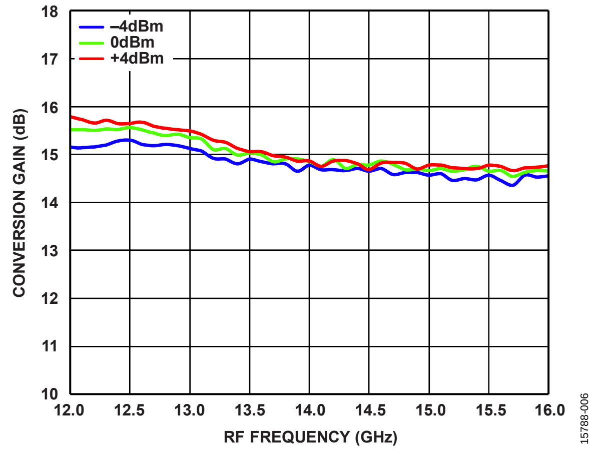

Figure 6. Conversion Gain vs. RF Frequency at Various LO Powers

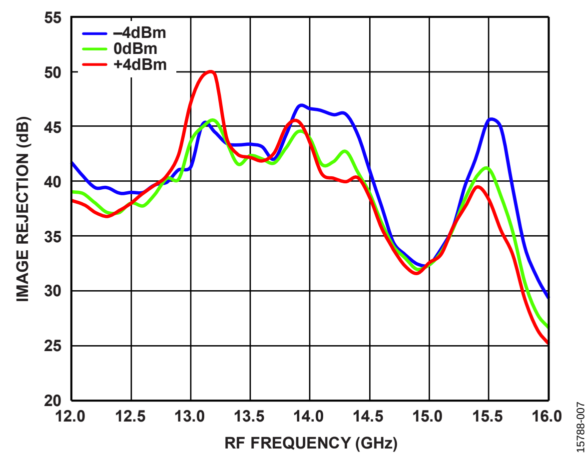

Figure 7. Image Rejection vs. RF Frequency at Various LO Powers

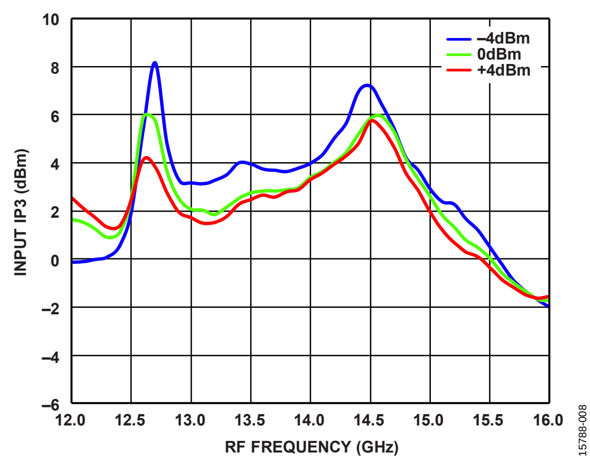

Figure 8. Input IP3 vs. RF Frequency at Various LO Powers

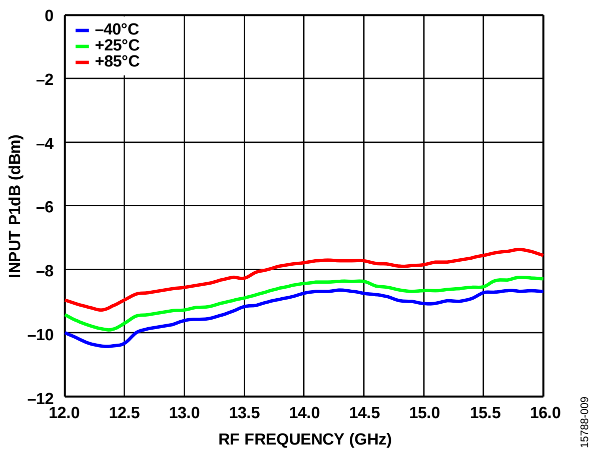

Figure 9. Input P1dB vs. RF Frequency at Various Temperatures

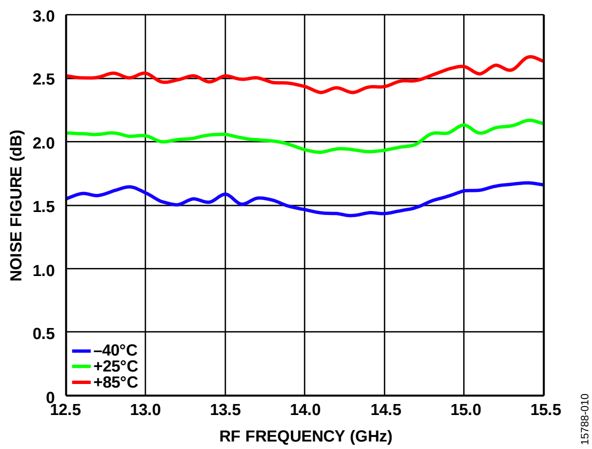

Figure 10. Noise Figure vs. RF Frequency at Various Temperatures

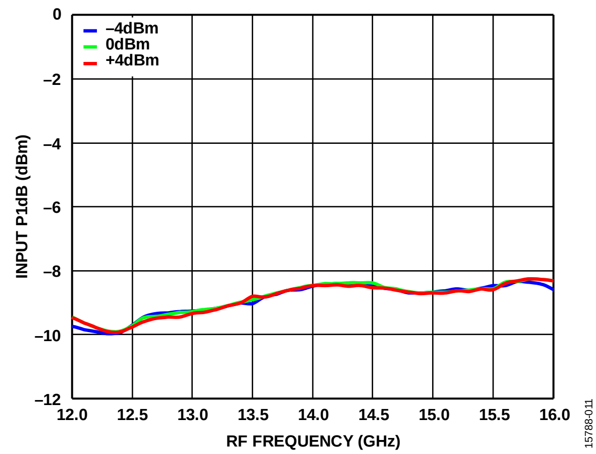

Figure 11. Input P1dB vs. RF Frequency at Various LO Powers

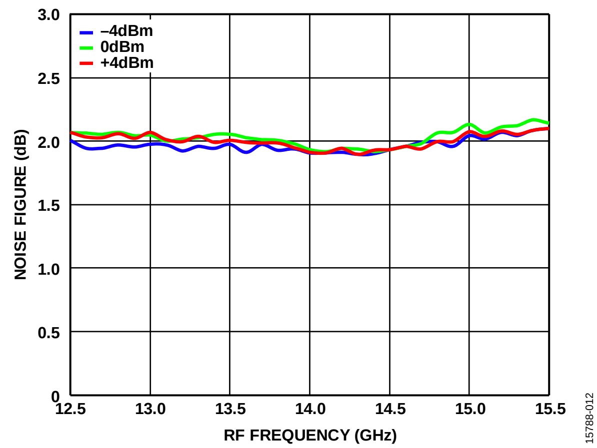

Figure 12. Noise Figure vs. RF Frequency at Various LO Powers

IF FREQUENCY = 3.1 GHz

Data taken at VDRF = 4 V, VDLO = 4 V, LO = −4 dBm ≤ LO ≤ +4 dBm, −40°C ≤ T_A ≤ +85°C, data taken with Mini-Circuits QCN-45+ power splitter as upper sideband (low-side LO), unless otherwise noted.

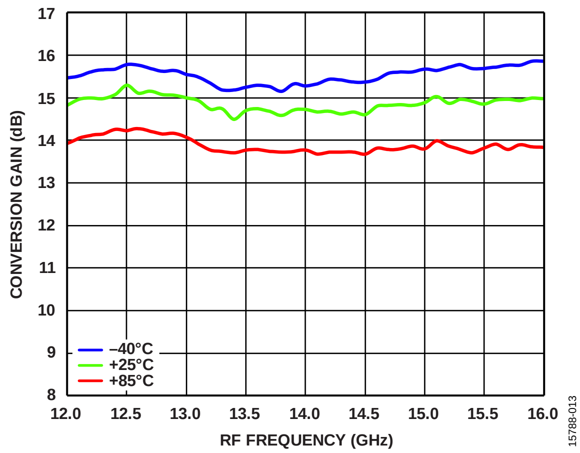

Figure 13. Conversion Gain vs. RF Frequency at Various Temperatures

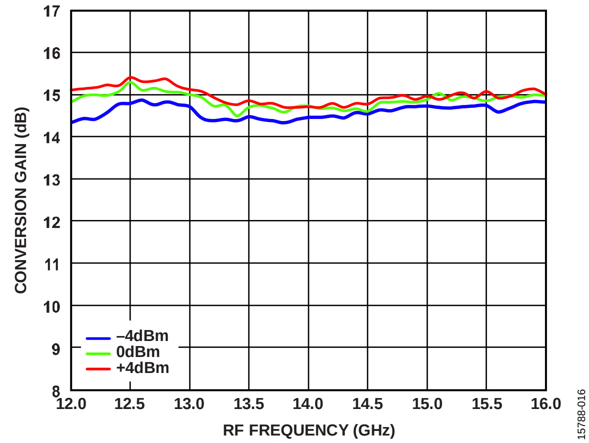

Figure 16. Conversion Gain vs. RF Frequency at Various LO Powers

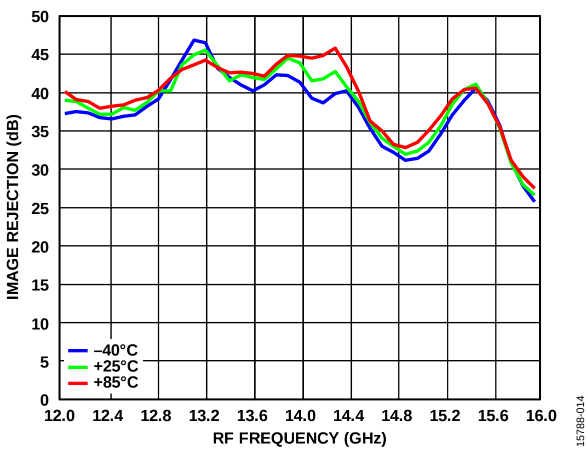

Figure 14. Image Rejection vs. RF Frequency at Various Temperatures

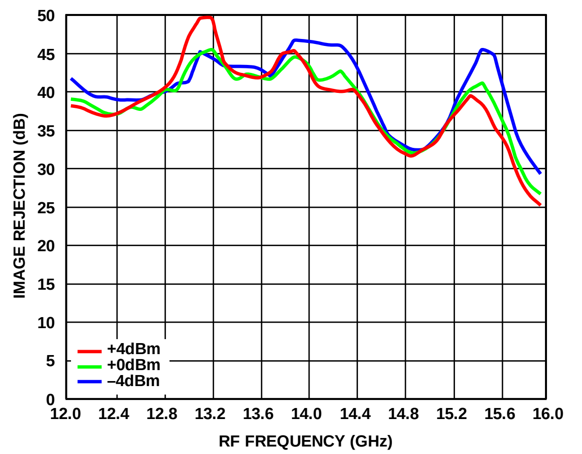

Figure 17. Image Rejection vs. RF Frequency at Various LO Powers

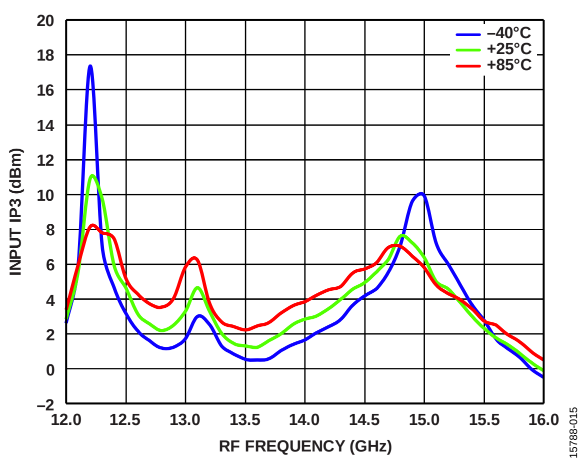

Figure 15. Input IP3 vs. RF Frequency at Various Temperatures

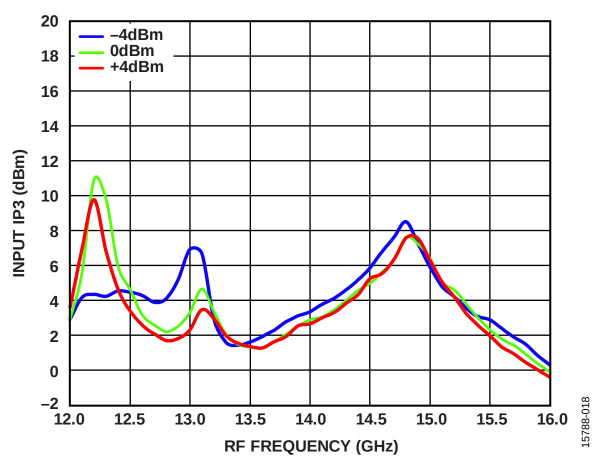

Figure 18. Input IP3 vs. RF Frequency at Various LO Powers

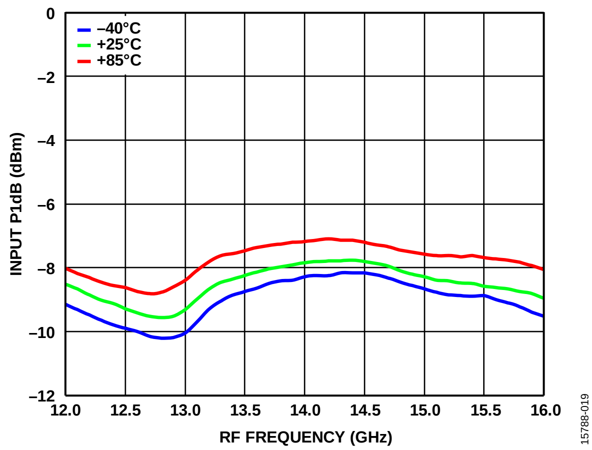

Figure 19. Input P1dB vs. RF Frequency at Various Temperatures

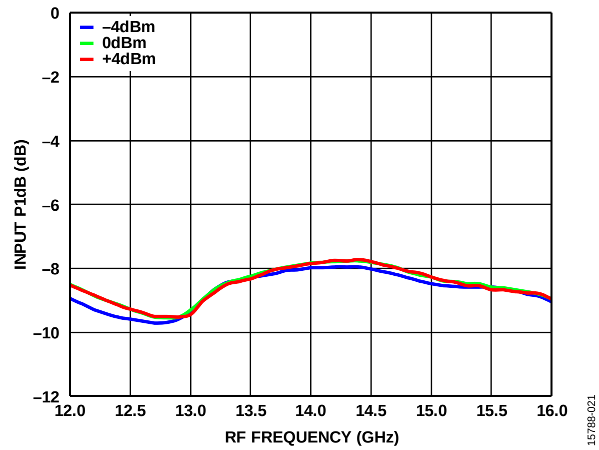

Figure 21. Input P1dB vs. RF Frequency at Various LO Powers

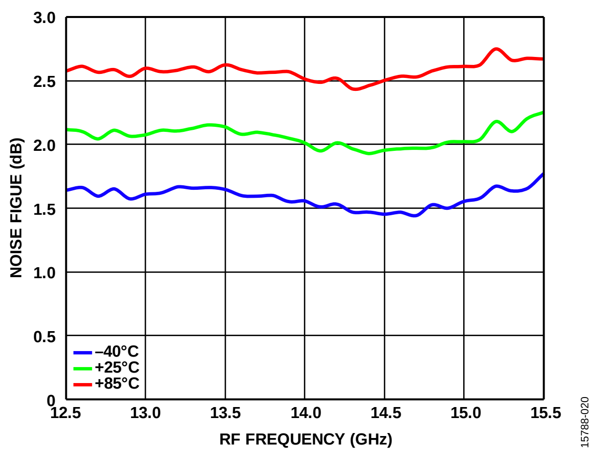

Figure 20. Noise Figure vs. RF Frequency at Various Temperatures

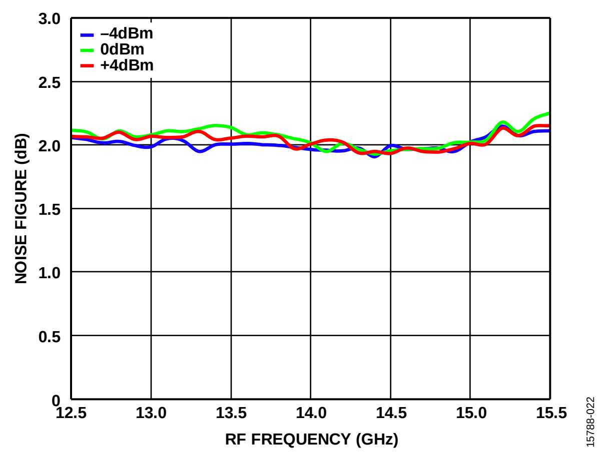

Figure 22. Noise Figure vs. RF Frequency at Various LO Powers

IF FREQUENCY = 3.5 GHz

Data taken at VDRF = 4 V, VDLO = 4 V, LO = −4 dBm ≤ LO ≤ +4 dBm, −40°C ≤ T_A ≤ +85°C, data taken with Mini-Circuits QCN-45+ power splitter as upper sideband (low-side LO), unless otherwise noted.

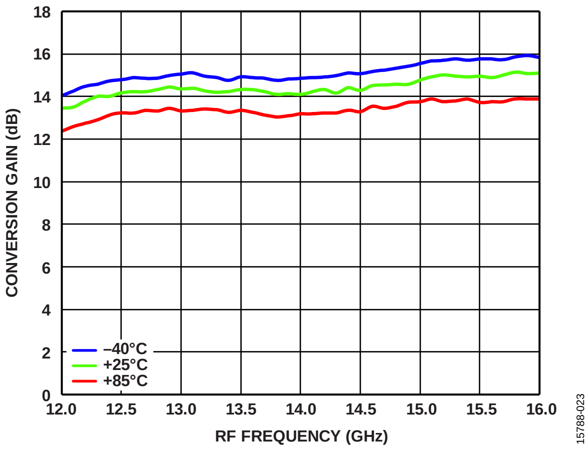

Figure 23. Conversion Gain vs. RF Frequency at Various Temperatures

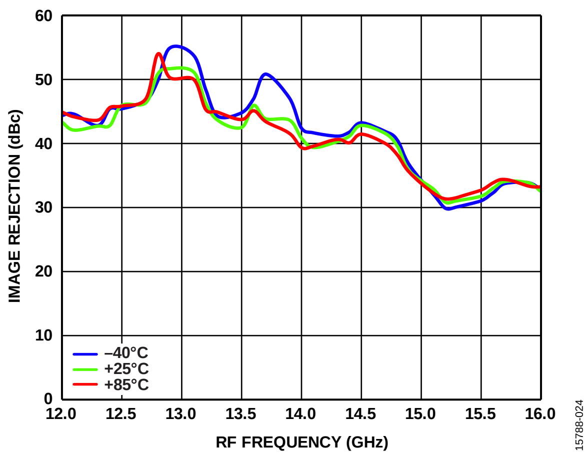

Figure 24. Image Rejection vs. RF Frequency at Various Temperatures

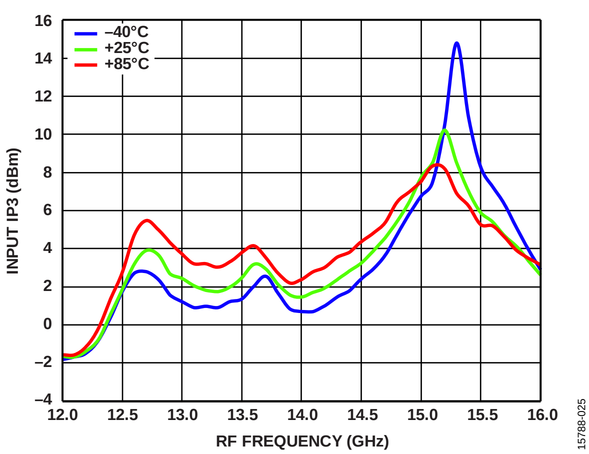

Figure 25. Input IP3 vs. RF Frequency at Various Temperatures

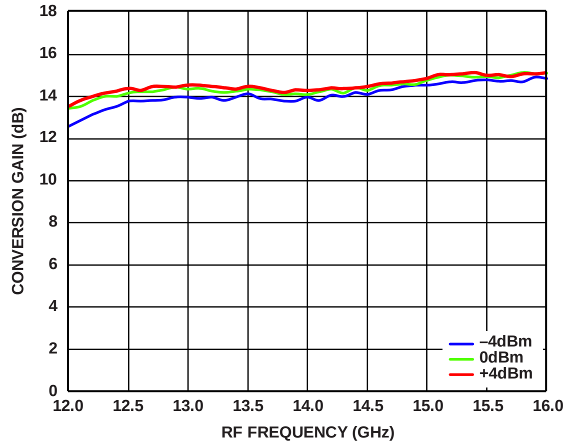

Figure 26. Conversion Gain vs. RF Frequency at Various LO Powers

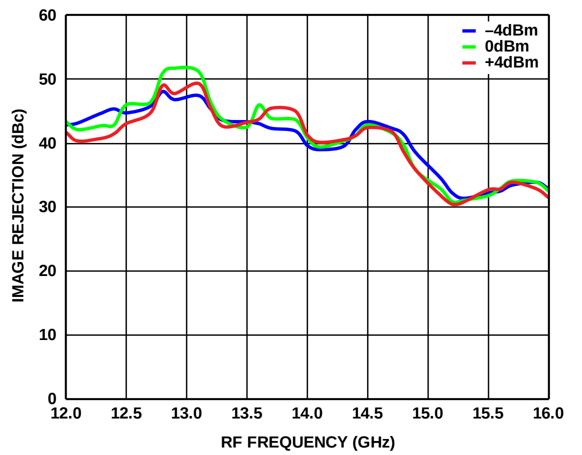

Figure 27. Image Rejection vs. RF Frequency at Various LO Powers

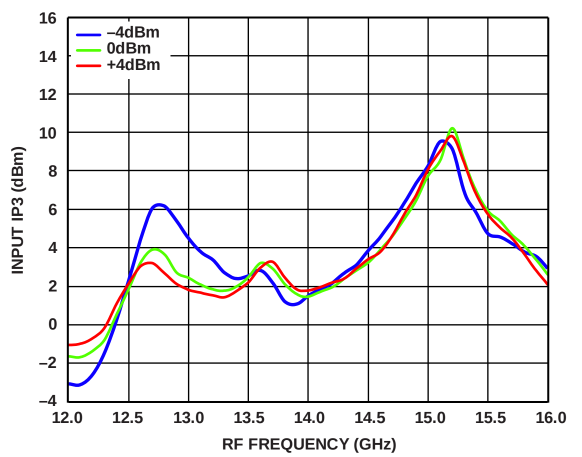

Figure 28. Input IP3 vs. RF Frequency at Various LO Powers

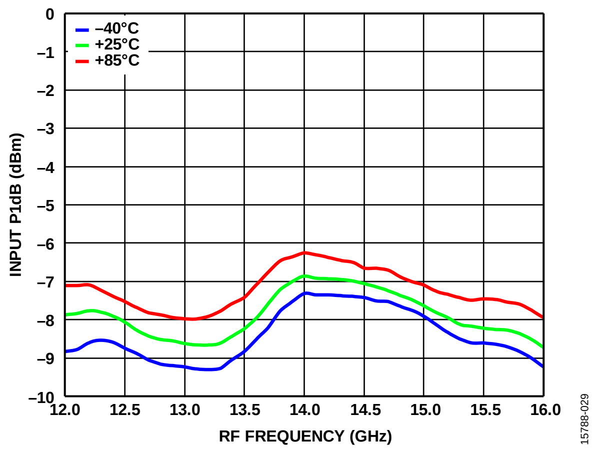

Figure 29. Input P1dB vs. RF Frequency at Various Temperatures

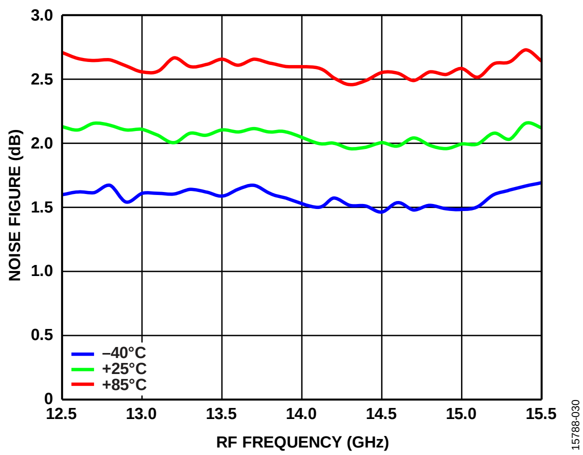

Figure 30. Noise Figure vs. RF Frequency at Various Temperatures

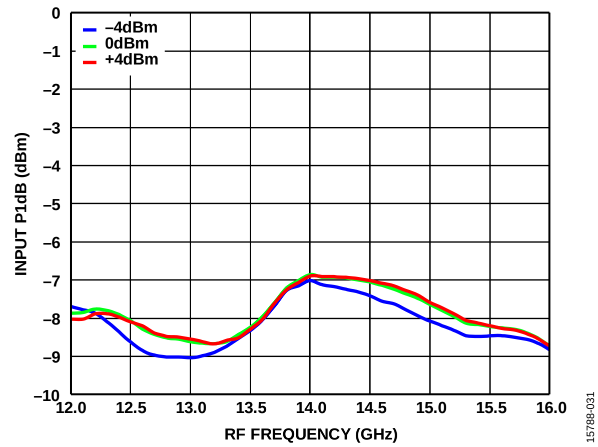

Figure 31. Input P1dB vs. RF Frequency at Various LO Powers

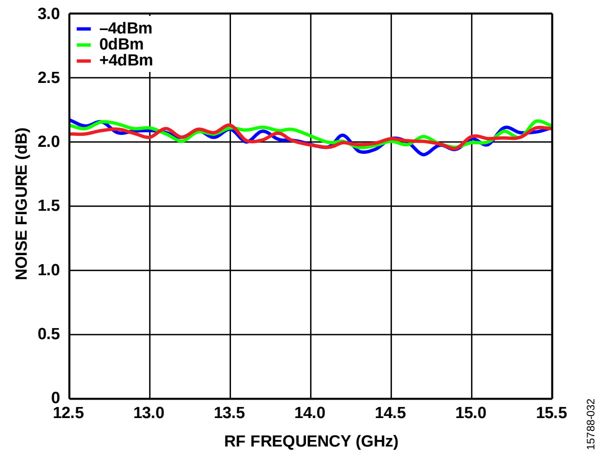

Figure 32. Noise Figure vs. RF Frequency at Various LO Powers

IF BANDWIDTH

Data taken at VDRF = 4 V, VDLO = 4 V, LO = −4 dBm ≤ LO ≤ +4 dBm at 9 GHz, −40°C ≤ T_A ≤ +85°C, data taken with Mini-Circuits QCN-45+ power splitter as upper sideband (low-side LO), unless otherwise noted.

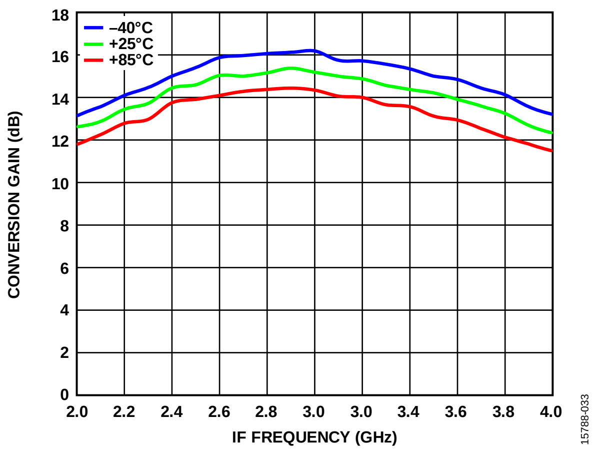

Figure 33. Conversion Gain vs. IF Frequency at Various Temperatures

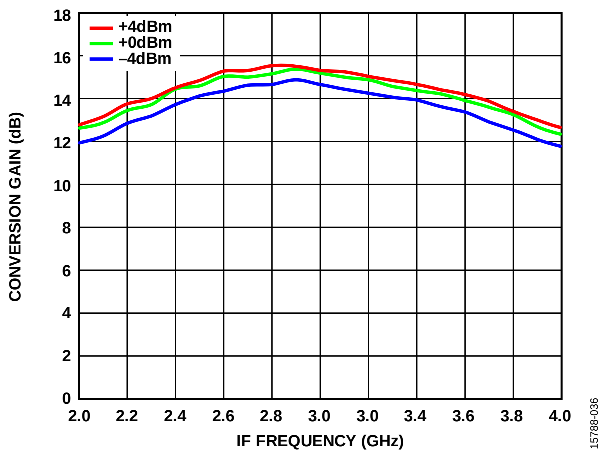

Figure 35. Conversion Gain vs. IF Frequency at Various LO Powers

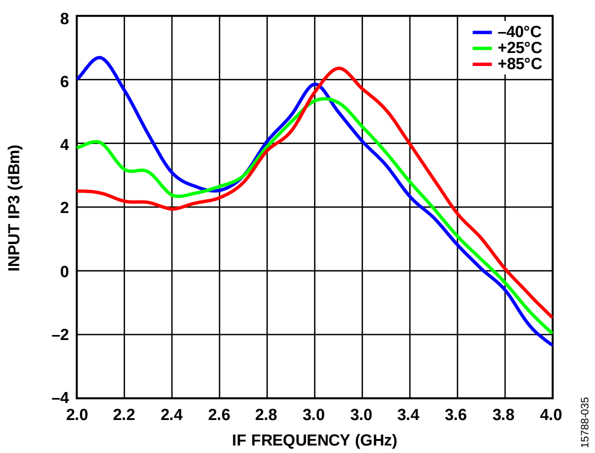

Figure 34. Input IP3 vs. IF Frequency at Various Temperatures

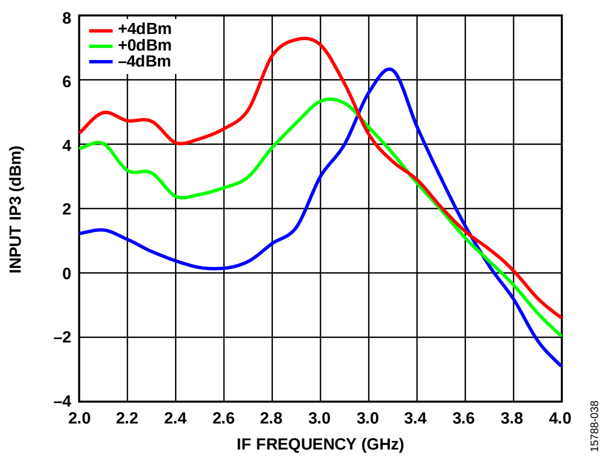

Figure 36. Input IP3 vs. IF Frequency at Various LO Powers

LEAKAGE PERFORMANCE

Data taken at VDRF = 4 V, VDLO = 4 V, LO = −4 dBm ≤ LO ≤ +4 dBm, −40°C ≤ T_A ≤ +85°C, data taken with Mini-Circuits QCN-45+ power splitter as upper sideband (low-side LO), unless otherwise noted.

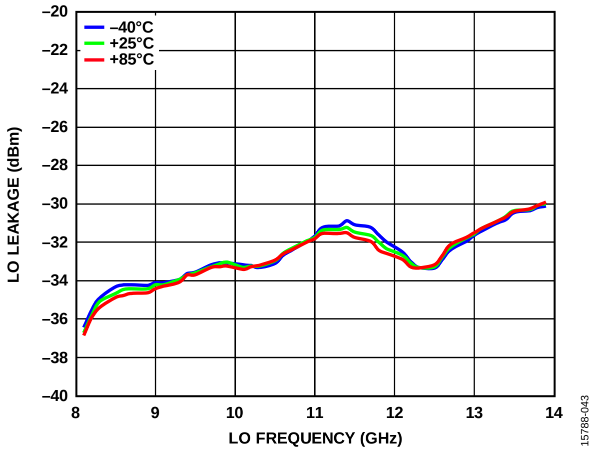

Figure 37. LO Leakage at RFIN vs. LO Frequency at Various Temperatures

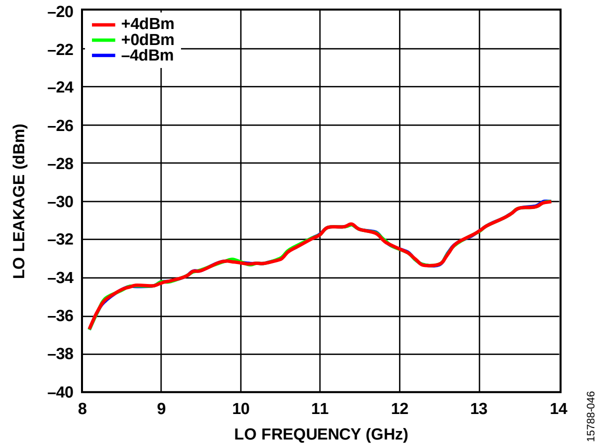

Figure 39. LO Leakage at RFIN vs. LO Frequency at Various LO Powers

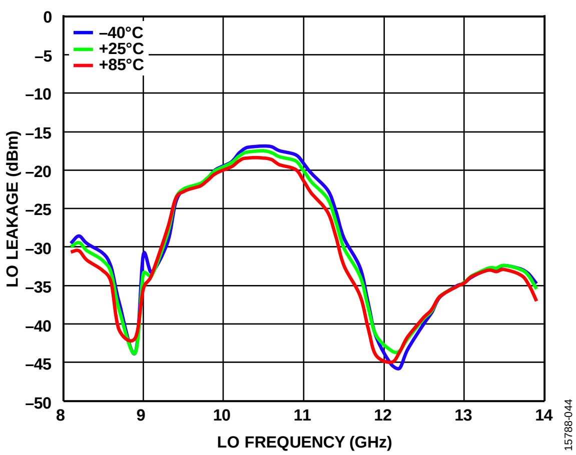

Figure 38. LO Leakage at IF Output vs. LO Frequency at Various Temperatures

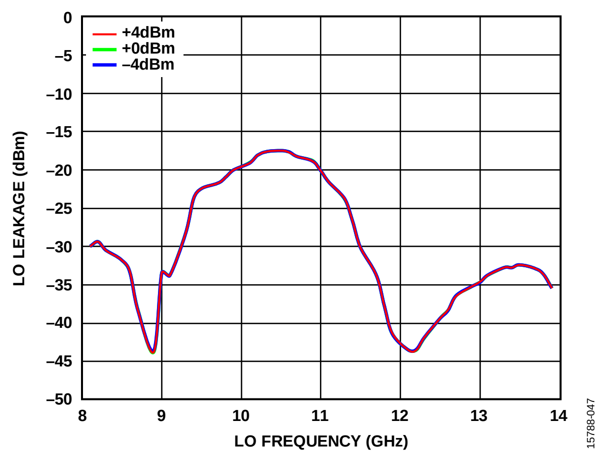

Figure 40. LO Leakage at IF Output vs. LO Frequency at Various LO Powers

RETURN LOSS PERFORMANCE

Data taken at VDRF = 4 V, VDLO = 4 V, LO = −4 dBm ≤ LO ≤ +4 dBm, −40°C ≤ T_A ≤ +85°C, data taken with Mini-Circuits QCN-45+ power splitter as upper sideband (low-side LO), unless otherwise noted. Measurement includes trace loss and RF connector loss.

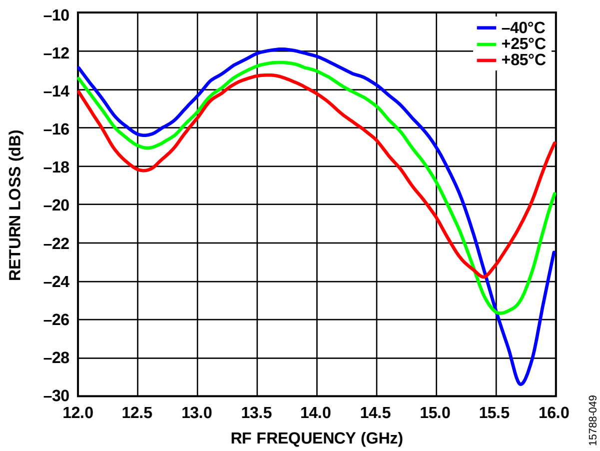

Figure 41. RF Input Return Loss vs. RF Frequency at Various Temperatures

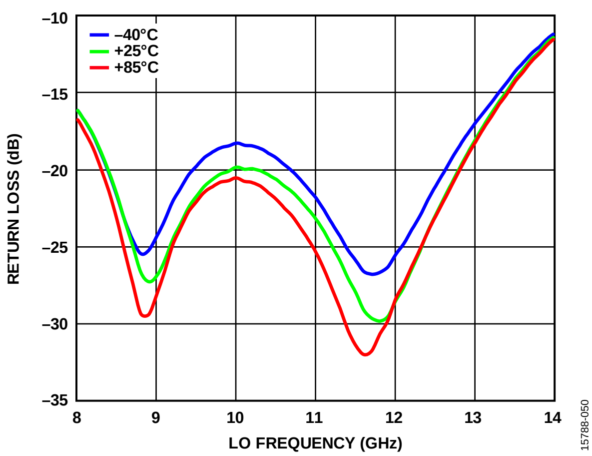

Figure 42. LO Input Return Loss vs. LO Frequency at Various Temperatures

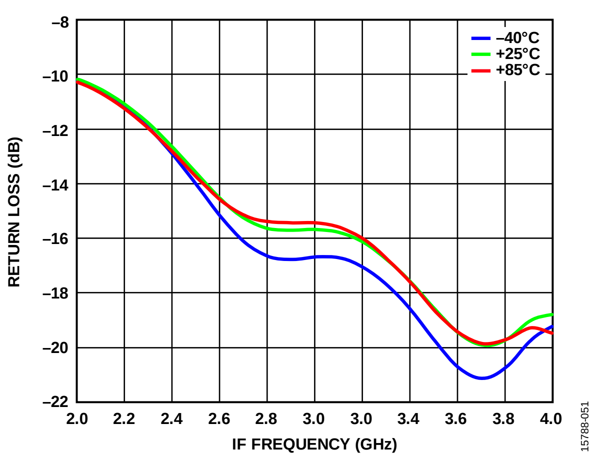

Figure 43. IF Output Return Loss vs. IF Frequency at Various Temperatures

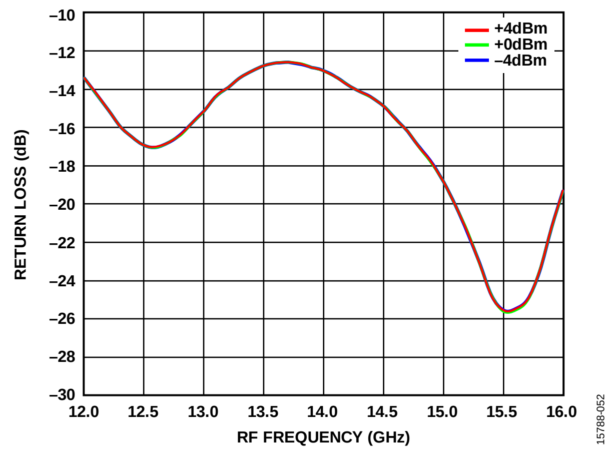

Figure 44. RF Input Return Loss vs. RF Frequency at Various LO Powers

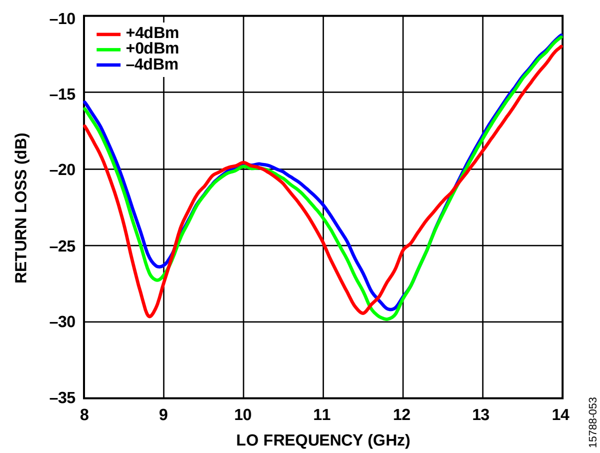

Figure 45. LO Input Return Loss vs. LO Frequency at Various LO Powers

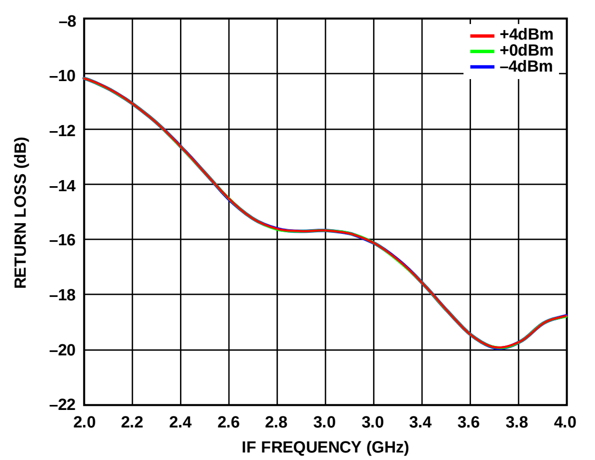

Figure 46. IF Output Return Loss vs. IF Frequency at Various LO Powers

SPURIOUS PERFORMANCE

Data taken at VDRF = 4 V, VDLO = 4 V, LO = 0 dBm, −40°C ≤ T_A ≤ +85°C; data taken with Mini-Circuits QCN-45+ power splitter as upper sideband (low-side LO), unless otherwise noted.

Table 5. LO Harmonic Leakage (dBm) at IF Output

	Harmonics			
LO Frequency (MHz)[1]	1.0	2.0	3.0	4.0
9000	−36	−48	−47	−49
9500	−22	−47	−45	−50
10,000	−20	−47	−43	−60
10,500	−18	−48	−42	−53
11,000	−19	−46	−41	−50
11,500	−28	−41	−38	−65
12,000	−42	−47	−35	−60
12,600	−43	−46	−32	−61

[1] LO Input Power = 0 dBm.

M × N SPURIOUS PERFORMANCE

LO = 4 dBm, Upper Sideband

IF = 2700 MHz, RF = 13.3 GHz at −20 dBm; all values in dBc below the IF power level. N/A means not applicable.

		N × LO				
		−2	−1	0	+1	+2
M × RF	−1	N/A	N/A	N/A	N/A	28
	0	N/A	N/A	N/A	13	39
	+1	N/A	0	24	51	43
	+2	52	86	61	65	71

IF = 3100 MHz, RF = 13.3 GHz at −20 dBm; all values in dBc below the IF power level. N/A means not applicable.

		N × LO				
		−2	−1	0	+1	+2
M × RF	−1	N/A	N/A	N/A	N/A	25
	0	N/A	N/A	N/A	13	40
	+1	N/A	0	24	50	40
	+2	55	78	61	63	72

IF = 3500 MHz, RF = 13.3 GHz at −20 dBm; all values in dBc below the IF power level. N/A means not applicable.

		N × LO				
		−2	−1	0	+1	+2
M × RF	−1	N/A	N/A	N/A	N/A	24
	0	N/A	N/A	N/A	14	38
	+1	N/A	0	24	49	44
	+2	54	66	60	61	70

THEORY OF OPERATION

The ADMV1010 is a compact GaAs, MMIC, single sideband (SSB) downconverter in a RoHS compliant package optimized for upper sideband point to point microwave radio applications operating in the 12.6 GHz to 15.4 GHz input frequency range. The ADMV1010 supports LO input frequencies of 9 GHz to 12.6 GHz and IF output frequencies of 2.7 GHz to 3.5 GHz.

The ADMV1010 uses a RF LNA amplifier followed by an I/Q double balanced mixer, where a driver amplifier drives the LO (see Figure 1). The combination of design, process, and packaging technology allows the functions of these subsystems to be integrated into a single die, using mature packaging and interconnection technologies to provide a high performance, low cost design with excellent electrical, mechanical, and thermal properties. In addition, the need for external components is minimized, optimizing cost and size.

LO DRIVER AMPLIFIER

The LO driver amplifier takes a single LO input and amplifies it to the desired LO signal level for the mixer to operate optimally. The LO driver amplifier is self biased, and it only requires a single dc bias voltage (VDLO) to operate. The bias current for the LO amplifier is 100 mA at 4 V typically. The LO drive range of −4 dBm to +4 dBm makes it compatible with Analog Devices, Inc., wideband synthesizer portfolio without the need for an external LO driver amplifier.

MIXER

The mixer is an I/Q double balanced mixer, and this mixer topology reduces the need for filtering the unwanted sideband. An external 90° hybrid is required to select the upper sideband of operation. The ADMV1010 has been optimized to work with the Mini-Circuits QCN-45+ RF 90° hybrid.

LNA

The LNA is self biased, and it requires only a single dc bias voltage (VDRF) to operate. The bias current for the LNA is 60 mA at 4 V typically.

The application circuit (see Figure 47) provided shows the necessary external components on the bias lines to eliminate any undesired stability problems for the RF amplifier and the LO amplifier.

The ADMV1010 is a much smaller alternative to hybrid style image reject converter assemblies, and it eliminates the need for wire bonding by allowing the use of surface-mount manufacturing assemblies.

The ADMV1010 downconverter comes in a compact, thermally enhanced, 4.9 mm × 4.9 mm, 32-terminal ceramic leadless chip carrier (LCC) package. The ADMV1010 operates over the −40°C to +85°C temperature range.

APPLICATIONS INFORMATION

The evaluation board and typical application circuit are optimized for low-side LO (upper sideband) performance with the Mini-Circuit QCN-45+ RF 90° hybrid. Because the I/Q mixers are double balanced, the ADMV1010 can support IF frequencies from 3.5 GHz to low frequency.

TYPICAL APPLICATION CIRCUIT

The typical applications circuit is shown in Figure 47. The application circuit shown here has been replicated for the evaluation board circuit.

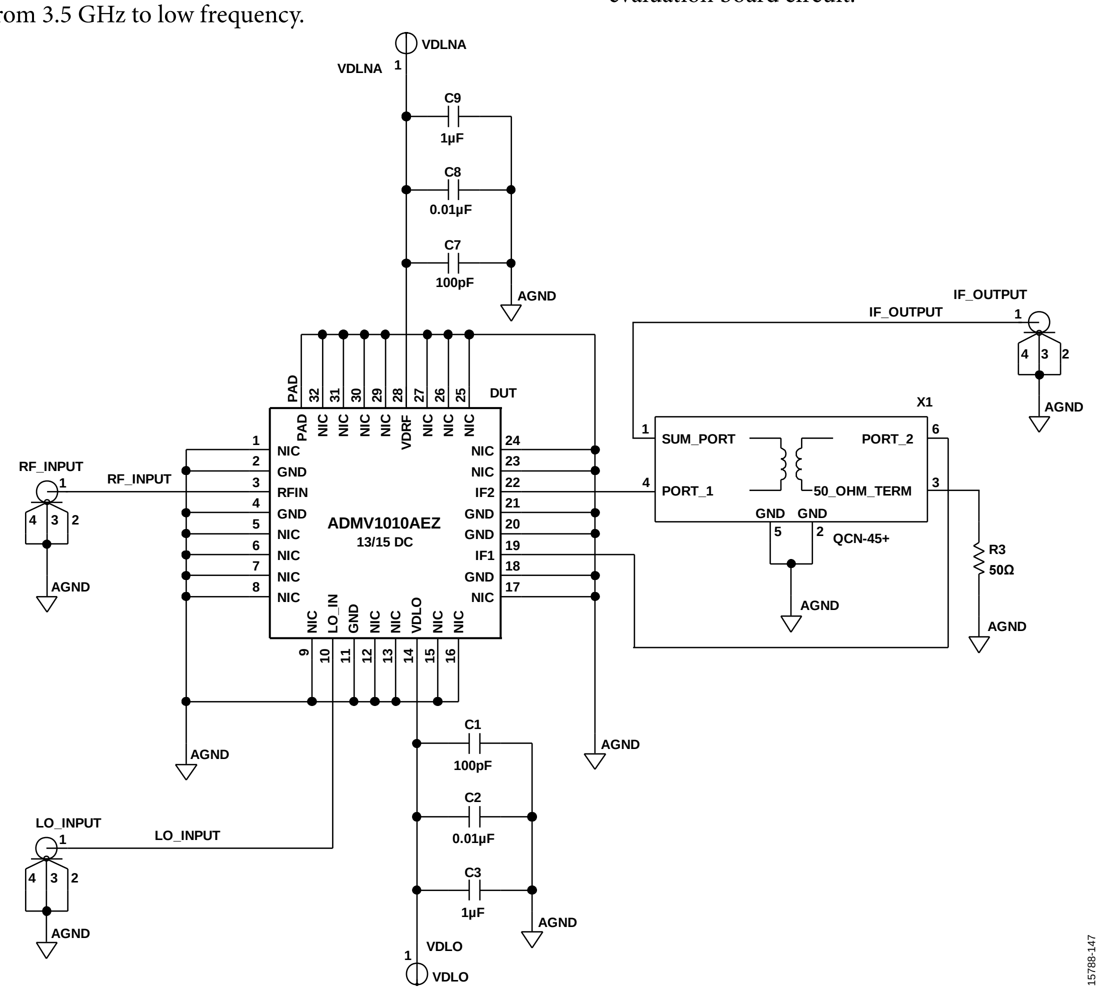

Figure 47. Typical Application Circuit

EVALUATION BOARD

The circuit board used in the application must use RF circuit design techniques. Signal lines must have 50 Ω impedance, and the package ground leads and exposed pad must be connected directly to the ground plane similarly to that shown in Figure 48 and Figure 49. Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation circuit board shown in Figure 50 is available from Analog Devices upon request.

Layout

Solder the exposed pad on the underside of the ADMV1010 to a low thermal and electrical impedance ground plane. This pad is typically soldered to an exposed opening in the solder mask on the evaluation board. Connect these ground vias to all other ground layers on the evaluation board to maximize heat dissipation from the device package. Figure 48 shows the printed circuit board (PCB) land pattern footprint for the ADMV1010-EVALZ, and Figure 49 shows the solder paste stencil for the ADMV1010-EVALZ.

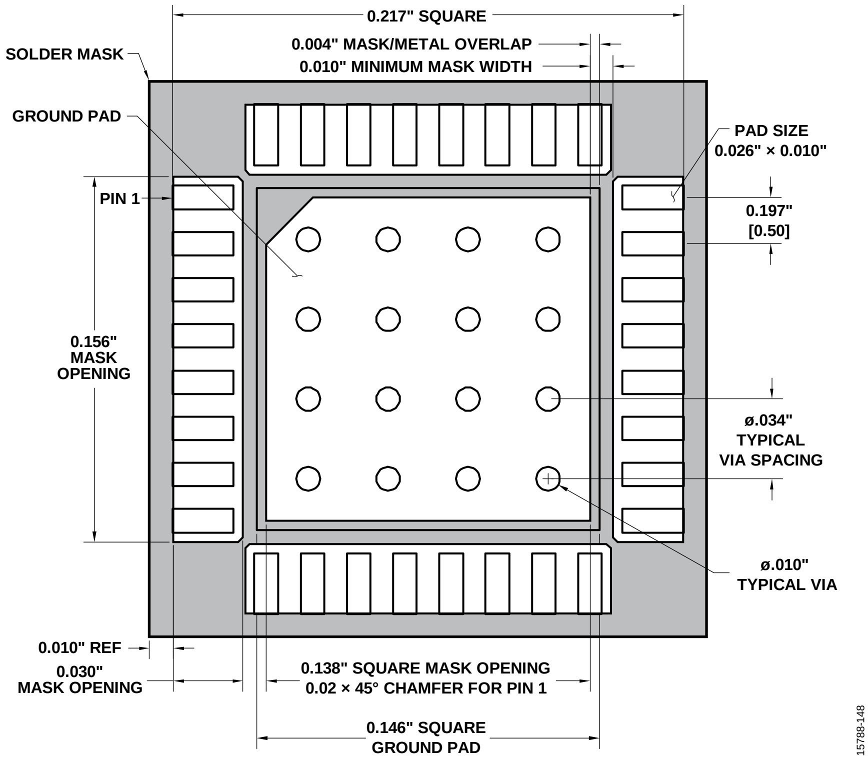

Figure 48. PCB Land Pattern Footprint of the ADMV1010-EVALZ

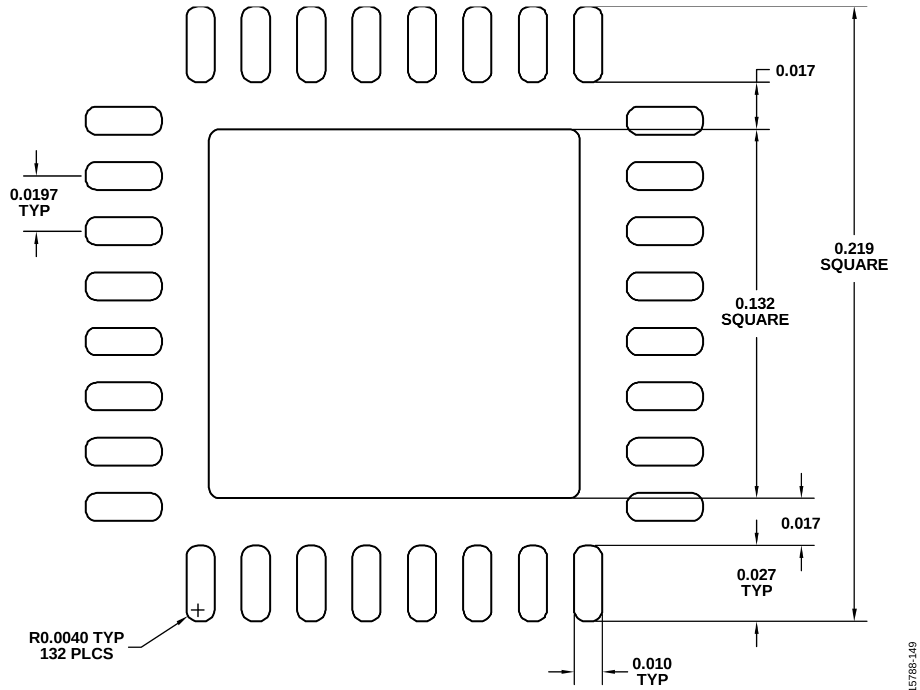

Figure 49. Solder Paste Stencil of the ADMV1010-EVALZ

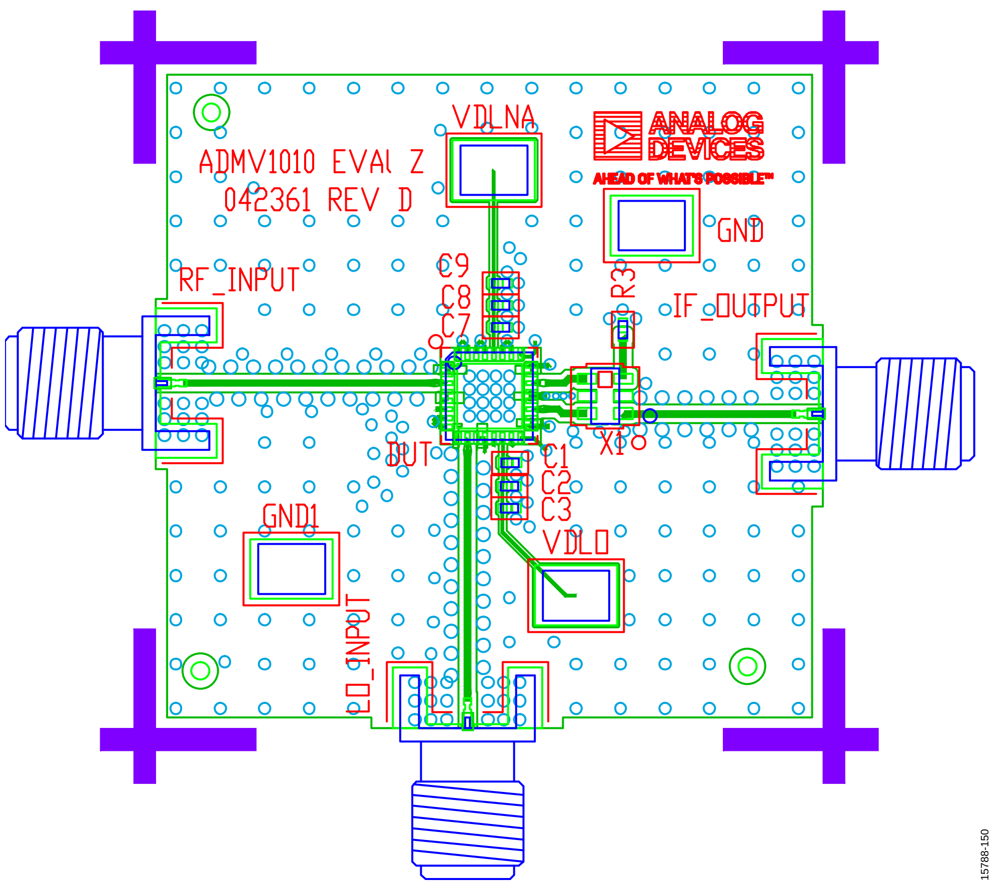

Figure 50. ADMV1010-EVALZ Evaluation Board, Top Layer

BILL OF MATERIALS

Table 6.

Qty.	Reference Designator	Description	Manufacturer/Part No.
1	Not applicable	PCB	Analog Devices/042361
2	C1, C7	100 pF multilayer ceramic capacitors, high temperature, 0402	Murata/GRM1555C1H101JA01D
2	C2, C8	0.01 µF ceramic capacitors, X7R, 0402	Murata/GRM155R71E103KA01D
2	C3, C9	1 µF monolithic ceramic capacitors, SMD, X5R, 0402	Taiyo Yuden/UMK107AB7105KA-T
4	GND, GND1, VDLO, VDLNA	Connection PCB SMT test points, CNKEY5016TP	Keystone Electronics Corporation/5016
3	LO_INPUT, RF_INPUT, IF_OUTPUT	Connection PCB SMA, K_SRI-NS, CNSMAL460W295H156	SRI Connector Gage Co./25-146-1000-92
1	R3	50 Ω, high frequency chip resistor, 0402	Vishay Precision Group/FC0402E50R0FST1
1	X1	XFMR power splitter/combiner, 2500 MHz to 4500 MHz, TSML126W63H42	Mini-Circuits/QCN-45+
1	Device Under Test (DUT)	GaAs, MMIC, I/Q downconverter	Analog Devices/ADMV1010AEZ
1	Heatsink	Heatsink	Analog Devices/111332

OUTLINE DIMENSIONS

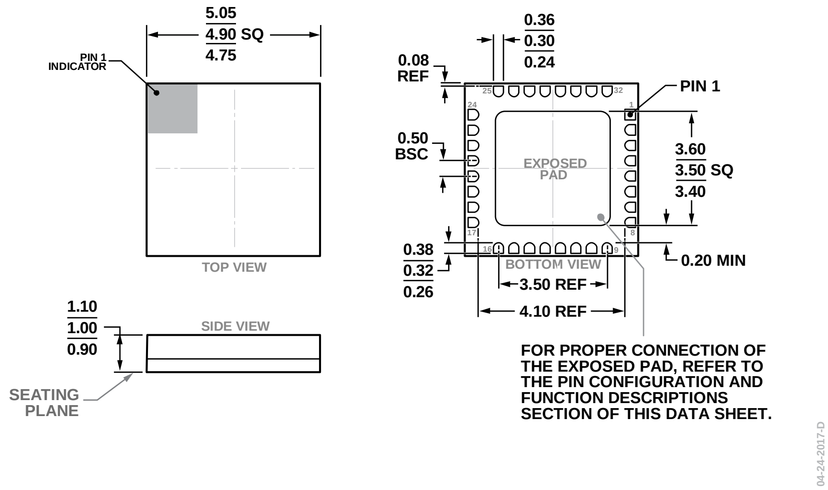

Figure 51. 32-Terminal Ceramic Leadless Chip Carrier [LCC] (E-32-1) Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Body Material	Lead Finish	Package Description	Package Option
ADMV1010AEZ	−40°C to +85°C	Alumina Ceramic	Gold Over Nickel	32-Terminal Ceramic LCC	E-32-1
ADMV1010AEZ-R7	−40°C to +85°C	Alumina Ceramic	Gold Over Nickel	32-Terminal Ceramic LCC	E-32-1
ADMV1010-EVALZ				Evaluation Board	

[1] Z = RoHS Compliant Part.

D15788-0-4/18(B)