Tiny, I²C Programmable, Linear Battery Charger with Power Path and USB Mode Compatibility

Data Sheet

ADP5061

FEATURES

- 2.6 mm × 2 mm WLCSP package
- Fully programmable via I²C
- Flexible digital control inputs
- Up to 2.1 A current from an ac charger in LDO mode
- Operating input voltage from 4.0 V to 6.7 V
- Tolerant input voltage from −0.5 V to +20 V (USB VBUS)
- Fully compatible with USB 3.0 and USB Battery Charging Specification 1.2
- Built-in current sensing and limiting
- As low as 30 mΩ battery isolation FET between battery and charger output
- Thermal regulation prevents over heating
- Compliant with JEITA 1 and JEITA 2 Li-Ion battery charging temperature specifications
- SYS_EN flag permits the system to be disabled until battery is at minimum required level for guaranteed system start-up

APPLICATIONS

- Digital still cameras
- Digital video cameras
- Single cell Li-Ion portable equipment
- PDAs, audio, and GPS devices
- Portable medical devices
- Mobile phones

TYPICAL APPLICATION CIRCUIT

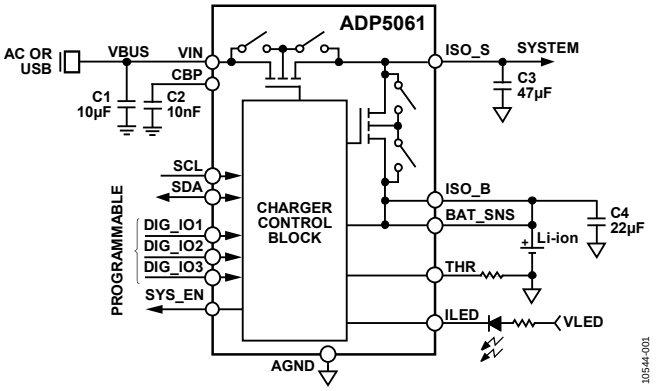

Figure 1.

GENERAL DESCRIPTION

The ADP5061 charger is fully compliant with USB 3.0 and the USB Battery Charging Specification 1.2 and enables charging via the mini USB VBUS pin from a wall charger, car charger, or USB host port.

The ADP5061 operates from a 4 V to 6.7 V input voltage range but is tolerant of voltages up to 20 V. The 20 V voltage tolerance alleviates the concerns about the USB bus spiking during disconnect or connect scenarios.

The ADP5061 features an internal FET between the linear charger output and the battery. This permits battery isolation and, hence, system powering under a dead battery or no battery scenario, which allows for immediate system function on connection to a USB power supply.

Based on the type of USB source, which is detected by an external USB detection chip, the ADP5061 can be set to apply the correct current limit for optimal charging and USB compliance.

The ADP5061 has three factory programmable digital input/output pins that provide maximum flexibility for different systems. These digital input/output pins permit combinations of features such as, input current limits, charging enable and disable, charging current limits, and a dedicated interrupt output pin.

Rev. D
Document Feedback

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SPECIFICATIONS

$-40°C < T_J < +125°C$, $V_{VIN} = 5.0$ V, $V_{HOT} < V_{THR} < V_{COLD}$, $V_{BAT\_SNS} = 3.6$ V, $V_{ISO\_B} = V_{BAT\_SNS}$, $C_{VIN} = 10$ µF, $C_{ISO\_S} = 22$ µF, $C_{ISO\_B} = 22$ µF, $C_{CBP} = 10$ nF, all registers at default values, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
GENERAL PARAMETERS						
Undervoltage Lockout	V_{UVLO}	2.25	2.35	2.5	V	Falling threshold, higher of V_{VIN} and V_{BAT_SNS}[1]
Hysteresis		50	100	150	mV	Hysteresis, higher of V_{VIN} and V_{BAT_SNS} rising[1]
Total Input Current	I_{LIM}	74	92	100	mA	Nominal USB initialized current level[2]
		114		150	mA	USB super speed
				300	mA	USB enumerated current level (specification for China)
		425	470	500	mA	USB enumerated current level
				900	mA	Dedicated charger input
				1500	mA	Dedicated wall charger
VINx Current Consumption	I_{QVIN}		2		mA	Charging or LDO mode
	I_{QVIN_DIS}		280	450	µA	DIS_IC1 = high, $V_{ISO\_B} <$ VINx < 5.5 V
Battery Current Consumption	I_{QBATT}		20		µA	LDO mode, $V_{ISO\_S} > V_{BAT\_SNS}$
				5	µA	Standby, includes ISO_Sx pin leakage, $V_{VIN} = 0$ V, $T_J = -40°C$ to $+85°C$
			0.5	0.9	mA	Standby, battery monitor active
CHARGER						
Fast Charge Current CC Mode	I_{CHG}	715	750	775	mA	$V_{ISO\_B} = 3.9$ V; fast charge current accuracy is guaranteed at temperatures from $T_J = -40°C$ to isothermal regulation limit (typically $T_J = +115°C$)[2, 3]
Fast Charge Current Accuracy		−40		+30	mA	I_{CHG} = 50 mA to 550 mA
		−50		+30	mA	I_{CHG} = 600 mA to 950 mA
		−65		+35	mA	I_{CHG} = 1000 mA to 1300 mA
Trickle Charge Current[2]	I_{TRK_DEAD}	16	20	25	mA	
Weak Charge Current[2, 3]	I_{CHG_WEAK}		$I_{TRK\_DEAD} + I_{CHG}$		mA	
Trickle to Weak Charge Threshold						
Dead Battery	V_{TRK_DEAD}	2.4	2.5	2.6	V	$V_{TRK\_DEAD} < V_{BAT\_SNS} < V_{WEAK}$[2, 4]
Hysteresis	ΔV_{TRK_DEAD}		100		mV	On BAT_SNS[2]
Weak Battery Threshold						
Weak to Fast Charge Threshold	V_{WEAK}	2.89	3.0	3.11	V	On BAT_SNS[2, 4]
	ΔV_{WEAK}		100		mV	
Battery Termination Voltage	V_{TRM}		4.200		V	
Termination Voltage Accuracy		−0.25		+0.25	%	On BAT_SNS, $T_J = 25°C$, $I_{END} = 52.5$ mA[2]
		−0.96		+0.89	%	$T_J = 0°C$ to $115°C$[2]
		−1.15		+1.20	%	$T_J = -40°C$ to $+125°C$
Battery Overvoltage Threshold	V_{BATOV}		$V_{IN} - 0.075$		V	Relative to VINx voltage, BAT_SNS rising
Charge Complete Current	I_{END}	15	52.5	98	mA	$V_{BAT\_SNS} = V_{TRM}$
Charging Complete Current Threshold Accuracy		17		83	mA	$I_{END} = 52.5$ mA, $T_J = 0°C$ to $115°C$[2]
		59		123		$I_{END} = 92.5$ mA, $T_J = 0°C$ to $115°C$
Recharge Voltage Differential	V_{RCH}	160	260	390	mV	Relative to V_{TRM}, BAT_SNS falling[2]
Battery Node Short Threshold Voltage[2]	V_{BAT_SHR}	2.2	2.4	2.5	V	
Battery Short Detection Current	I_{TRK_SHORT}		20		mA	$I_{TRK\_SHORT} = I_{TRK\_DEAD}$[2]
Charging Start Voltage Limit	V_{CHG_VLIM}	3.6	3.7	3.8	V	Voltage limit is not active by default
Charging Soft Start Current	I_{CHG_START}	185	260	365	mA	$V_{BAT\_SNS} > V_{TRK\_DEAD}$
Charging Soft Start Timer	t_{CHG_START}		3		ms	
BATTERY ISOLATION FET						
Bump to Bump Resistance Between ISO_Sx and ISO_Bx	$R_{DSONISO}$		30	49	mΩ	On battery supplement mode, VINx = 0 V, $V_{ISO\_B} = 4.2$ V, $I_{ISO\_B} = 500$ mA
Regulated System Voltage: V_{BAT} Low	V_{ISO_SFC}	3.6	3.8	4.0	V	VTRM[5:0] programming ≥ 4.00 V
		3.3	3.5	3.7		VTRM[5:0] programming < 4.00 V
Battery Supplementary Threshold	V_{THISO}	0	5	12	mV	$V_{ISO\_S} < V_{ISO\_B}$, V_{SYS} rising

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LDO AND HIGH VOLTAGE BLOCKING						
Regulated System Voltage	V_{ISO_STRK}	4.214	4.3	4.386	V	VSYSTEM[2:0] = 000 (binary) = 4.3 V, I_{ISO_S} = 100 mA, LDO mode[2]
Load Regulation			−0.28		%/A	I_{ISO_S} = 0 m A to 1500 mA
High Voltage Blocking FET (LDO FET) On Resistance	$R_{DS(ON)HV}$		330	485	mΩ	I_{VIN} = 500 mA
Maximum Output Current			2.1		A	V_{ISO_S} = 4.3 V, LDO mode
VINx Input Voltage, Good Threshold Rising	$V_{VIN\_OK\_RISE}$	3.75	3.9	4.0	V	
VINx Falling	$V_{VIN\_OK\_FALL}$		3.6	3.7	V	
VINx Input Overvoltage Threshold	V_{VIN_OV}	6.7	6.9	7.2	V	
Hysteresis	ΔV_{VIN_OV}		0.1		V	
VINx Transition Timing	T_{VIN_RISE}	10			µs	Minimum rise time for VINx from 5 V to 20 V
	T_{VIN_FALL}	10			µs	Minimum fall time for VINx from 4 V to 0 V
THERMAL CONTROL						
Isothermal Charging Temperature	T_{LIM}		115		°C	
Thermal Early Warning Temperature	T_{SDL}		130		°C	
Thermal Shutdown Temperature	T_{SD}		140		°C	T_J rising
			110		°C	T_J falling
THERMISTOR CONTROL						
Thermistor Current						
10,000 NTC	I_{NTC_10k}			400	µA	
100,000 NTC	I_{NTC_100k}			40	µA	
Thermistor Capacitance	C_{NTC}			100	pF	
Cold Temperature Threshold	T_{NTC_COLD}		0		°C	No battery charging occurs
Resistance Thresholds						
Cool to Cold Resistance	R_{COLD_FALL}	20,500	25,600	30,720	Ω	
Cold to Cool Resistance	R_{COLD_RISE}		24,400		Ω	
Hot Temperature Threshold	T_{NTC_HOT}		60		°C	No battery charging occurs
Resistance Thresholds						
Hot to Typical Resistance	R_{HOT_FALL}		3700		Ω	
Typical to Hot Resistance	R_{HOT_RISE}	2750	3350	3950	Ω	
JEITA1 Li-ION BATTERY CHARGING SPECIFICATION DEFAULTS[5]						
JEITA Cold Temperature	T_{JEITA_COLD}		0		°C	No battery charging occurs
Resistance Thresholds						
Cool to Cold Resistance	R_{COLD_FALL}	20,500	25,600	30,720	Ω	
Cold to Cool Resistance	R_{COLD_RISE}		24,400		Ω	
JEITA Cool Temperature	T_{JEITA_COOL}		10		°C	Battery charging occurs at 50% of programmed level
Resistance Thresholds						
Typical to Cool Resistance	R_{TYP_FALL}	13,200	16,500	19,800	Ω	
Cool to Typical Resistance	R_{TYP_RISE}		15,900		Ω	
JEITA Typical Temperature	T_{JEITA_TYP}				°C	Normal battery charging occurs at default/programmed levels
Resistance Thresholds						
Warm to Typical Resistance	R_{WARM_FALL}		5800		Ω	
Typical to Warm Resistance	R_{WARM_RISE}	4260	5200	6140	Ω	
JEITA Warm Temperature	T_{JEITA_WARM}		45		°C	Battery termination voltage (V_{TRM}) is reduced by 100 mV
Resistance Thresholds						
Hot to Warm Resistance	R_{HOT_FALL}		3700		Ω	
Warm to Hot Resistance	R_{HOT_RISE}	2750	3350	3950	Ω	
JEITA Hot Temperature	T_{JEITA_HOT}		60		°C	No battery charging occurs

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
JEITA2 Li-ION BATTERY CHARGING SPECIFICATION DEFAULTS[5]						
JEITA Cold Temperature	T_{JEITA_COLD}		0		°C	No battery charging occurs
Resistance Thresholds						
Cool to Cold Resistance	R_{COLD_FALL}	20,500	25,600	30,720	Ω	
Cold to Cool Resistance	R_{COLD_RISE}		24,400		Ω	
JEITA Cool Temperature	T_{JEITA_COOL}		10		°C	Battery termination voltage (V_{TRM}) is reduced by 100 mV
Resistance Thresholds						
Typical to Cool Resistance	R_{TYP_FALL}	13,200	16,500	19,800	Ω	
Cool to Typical Resistance	R_{TYP_RISE}		15,900		Ω	
JEITA Typical Temperature	T_{JEITA_TYP}				°C	Normal battery charging occurs at default/programmed levels
Resistance Thresholds						
Warm to Typical Resistance	R_{WARM_FALL}		5800		Ω	
Typical to Warm Resistance	R_{WARM_RISE}	4260	5200	6140	Ω	
JEITA Warm Temperature	T_{JEITA_WARM}		45		°C	Battery termination voltage (V_{TRM}) is reduced by 100 mV
Resistance Thresholds						
Hot to Warm Resistance	R_{HOT_FALL}		3700		Ω	
Warm to Hot Resistance	R_{HOT_RISE}	2750	3350	3950	Ω	
JEITA Hot Temperature	T_{JEITA_HOT}		60		°C	No battery charging occurs
BATTERY DETECTION						
Battery Detection						
Sink Current	I_{SINK}	13	20	34	mA	
Source Current	I_{SOURCE}	7	10	13	mA	
Battery Threshold						
Low	V_{BATL}	1.8	1.9	2.0	V	
High	V_{BATH}		3.4		V	
Battery Detection Timer	t_{BATOK}		333		ms	
TIMERS						
Clock Oscillator Frequency	f_{CLK}	2.7	3	3.3	MHz	
Start Charging Delay	t_{START}		1		sec	
Trickle Charge	t_{TRK}		60		min	
Fast Charge	t_{CHG}		600		min	
Charge Complete	t_{END}		7.5		min	$V_{BAT\_SNS} = V_{TRM}$, $I_{CHG} < I_{END}$
Deglitch	t_{DG}		31		ms	Applies to V_{TRK}, V_{RCH}, I_{END}, V_{DEAD}, V_{VIN_OK}
Watchdog[2]	t_{WD}		32		sec	
Safety	t_{SAFE}	36	40	44	min	
Battery Short[2]	t_{BAT_SHR}		30		sec	
ILED OUTPUT PINS						
Voltage Drop over ILED	V_{ILED}		200		mV	I_{ILED} = 20 mA
Maximum Operating Voltage over ILED	$V_{MAXILED}$			5.5	V	
SYS_EN OUTPUT PIN						
SYS_EN FET On Resistance	$R_{ON\_SYS\_EN}$		10		Ω	I_{SYS_EN} = 20 mA
LOGIC INPUT PIN						
Maximum Voltage on Digital Inputs[6]	V_{DIN_MAX}			5.5	V	Applies to SCL, SDA, DIG_IO1, DIG_IO2, DIG_IO3
Maximum Logic Low Input Voltage	V_{IL}			0.5	V	Applies to SCL, SDA, DIG_IO1, DIG_IO2, DIG_IO3
Minimum Logic High Input Voltage	V_{IH}	1.2			V	Applies to SCL, SDA, DIG_IO1, DIG_IO2, DIG_IO3
Pull-Down Resistance		215	350	610	kΩ	Applies to DIG_IO1, DIG_IO2, DIG_IO3

[1] Undervoltage lockout generated normally from ISO_Sx or ISO_Bx; in certain transition cases, it can be generated from VINx.
[2] These values are programmable via I²C. Values are given with default register values.
[3] The output current during charging may be limited by the input current limit or by the isothermal charging mode.
[4] During weak charging mode, the charger provides at least 20 mA of charging current via the trickle charge branch to the battery unless trickle charging is disabled. Any residual current, which is not required by the system, is also used to charge the battery.
[5] Either JEITA1 (default) or JEITA2 can be selected in I²C, or both JEITA functions can enabled or disabled in I²C.
[6] Do not tie DIG_IOx pins directly to VINx. In cases where the DIG_IOx pins are required to be tied high, do so with a resistor divider from VINx so that the voltage on these pins never exceeds the voltage on ISO_Sx at any time.

RECOMMENDED INPUT AND OUTPUT CAPACITANCES

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CAPACITANCES						
VINx	C_{VIN}	4		10	µF	Effective capacitance
CBP	C_{BP}	6	10	14	nF	Effective capacitance
ISO_Sx	C_{ISO_S}	20	47	100	µF	Effective capacitance
ISO_Bx	C_{ISO_B}	10	22		µF	Effective capacitance

I²C COMPATIBLE INTERFACE TIMING SPECIFICATIONS

Table 3.

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
I²C-COMPATIBLE INTERFACE[2]						
Capacitive Load for Each Bus Line	C_S			400	pF	
SCL Clock Frequency	f_{SCL}			400	kHz	
SCL High Time	t_{HIGH}	0.6			µs	
SCL Low Time	t_{LOW}	1.3			µs	
Data Setup Time	$t_{SU, DAT}$	100			ns	
Data Hold Time	$t_{HD, DAT}$	0		0.9	µs	
Setup Time for Repeated Start	$t_{SU, STA}$	0.6			µs	
Hold Time for Start/Repeated Start	$t_{HD, STA}$	0.6			µs	
Bus Free Time Between a Stop and a Start Condition	t_{BUF}	1.3			µs	
Setup Time for Stop Condition	$t_{SU, STO}$	0.6			µs	
Rise Time of SCL/SDA	t_R	20		300	ns	
Fall Time of SCL/SDA	t_F	20		300	ns	
Pulse Width of Suppressed Spike	t_{SP}	0		50	ns	

[1] Guaranteed by design.
[2] A master device must provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL (see Figure 2).

Timing Diagram

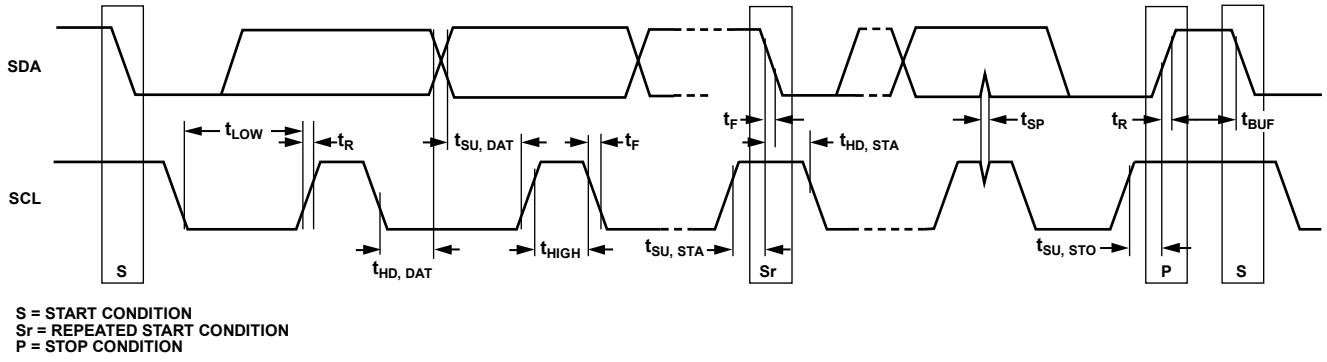

Figure 2. I²C Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
VIN1, VIN2, VIN3 to AGND	−0.5 V to +20 V
All Other Pins to AGND	−0.3 V to +6 V
Continuous Drain Current, Battery Supplementary Mode, from ISO_Bx to ISO_Sx	2.1 A
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	θ_{JB}	Unit
20-Lead WLCSP[1]	46.8	0.7	9.2	°C/W

[1] 5 × 4 array, 0.5 mm pitch (2.6 mm × 2.0 mm); based on a JEDEC 2S2P, 4-layer board with 0 m/sec airflow.

Maximum Power Dissipation

The maximum safe power dissipation in the ADP5061 package is limited by the associated rise in junction temperature (T_J) on the die. At a die temperature of approximately 150°C (the glass transition temperature), the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, thereby permanently shifting the parametric performance of the ADP5061. Exceeding a junction temperature of 175°C for an extended period can result in changes in the silicon devices, potentially causing failure.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

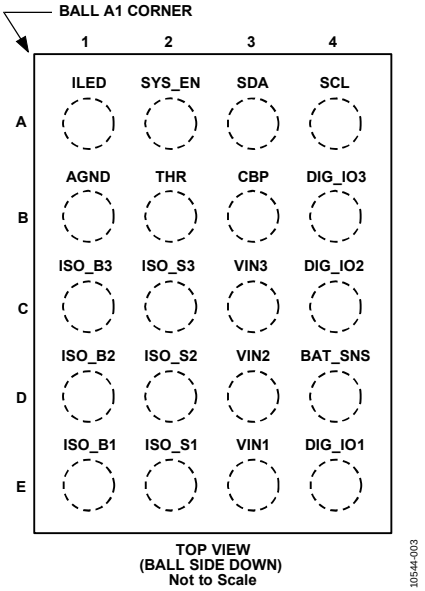

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
E2, D2, C2	ISO_S1, ISO_S2, ISO_S3	I/O	Linear Charger Supply Side Input to the Internal Isolation FET/Battery Current Regulation FET. High current input/output.
E3, D3, C3	VIN1, VIN2, VIN3	I/O	Power Connections to USB VBUS. These pins are high current inputs when in charging mode.
B1	AGND	G	Analog Ground.
E1, D1, C1	ISO_B1, ISO_B2, ISO_B3	I/O	Battery Supply Side Input to Internal Isolation FET/Battery Current Regulation FET.
A4	SCL	I	I²C-Compatible Interface Serial Clock.
A3	SDA	I/O	I²C-Compatible Interface Serial Data.
E4	DIG_IO1	GPIO	Set Input Current Limit. This pin sets the input current limit directly. When DIG_IO1 = low or high Z, the input limit is 100 mA. When DIG_IO1 = high, the input limit is 500 mA.[2, 3]
C4	DIG_IO2	GPIO	Models ADP5061ACBZ-2-R7 and ADP5061ACBZ-4-R7: Disable IC1. This pin sets the charger to the low current mode. When DIG_IO2 = low or high-Z, the charger operates in normal mode. When DIG_IO2 = high, the LDO and the charger are disabled and VINx current consumption is 280 µA (typical). 20 V VINx input protection is disabled and VINx voltage level must be equal to or lower than 5.5 V.[2, 3] Model ADP5061ACBZ-5-R7: Enable Charging. When DIG_IO3 = low or high-Z, charging is disabled. When DIG_IO3 = high, charging is enabled. [2, 3]
B4	DIG_IO3	GPIO	Models ADP5061ACBZ-2-R7 and ADP5061ACBZ-4-R7: Enable Charging. When DIG_IO3 = low or high-Z, charging is disabled. When DIG_IO3 = high, charging is enabled.[2, 3] Model ADP5061ACBZ-5-R7: Interrupt Output. This is the interrupt flag/open-drain pull-down FET pin to indicate when any of interrupts, which can be enabled using I²C register address 0x09, has occurred.
B2	THR	I	Battery Pack Thermistor Connection. If this pin is not used, connect a dummy 10 kΩ resistor from THR to GND.
D4	BAT_SNS	I	Battery Voltage Sense Pin.
A1	ILED	O	Open-Drain Output to Indicator LED.
A2	SYS_EN	O	System Enable. This is the battery OK flag/open-drain pull-down FET pin to enable the system when the battery level reaches the V_{WEAK} level.
B3	CBP	I/O	Bypass Capacitor Input.

[1] I is input, O is output, I/O is input/output, G is ground, and GPIO is factory programmable general-purpose input/output.
[2] See the Digital Input and Output Options section for details.
[3] DIG_IOx setting defines the initial state of the ADP5061. When the parameter or the mode that is related to each DIG_IOx pin setting is changed (by programming the equivalent I²C register bit or bits), the I²C register setting dominates over the DIG_IOx pin setting. VINx connection or disconnection resets control to the DIG_IOx pin.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{VIN} = 5.0 V, C_{VIN} = 10 µF, C_{ISO_S} = 44 µF, C_{ISO_B} = 22 µF, C_{BP} = 10 nF, all registers at default values, unless otherwise noted.

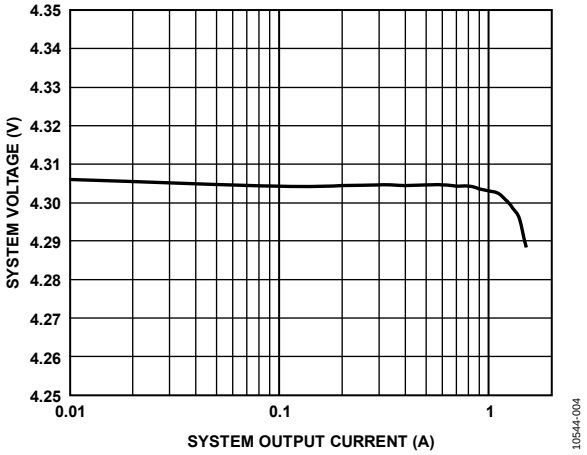

Figure 4. System Voltage vs. System Output Current, LDO Mode, VSYSTEM[2:0] = 000 (Binary) = 4.3 V

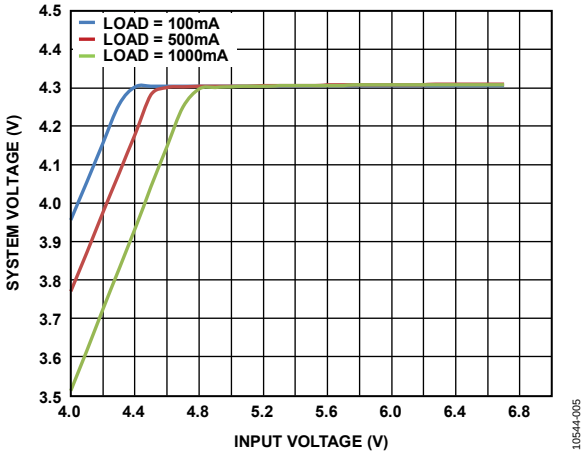

Figure 5. Output Voltage vs. Input Voltage (In Dropout), LDO Mode, VSYSTEM[2:0] = 000 (Binary) = 4.3 V

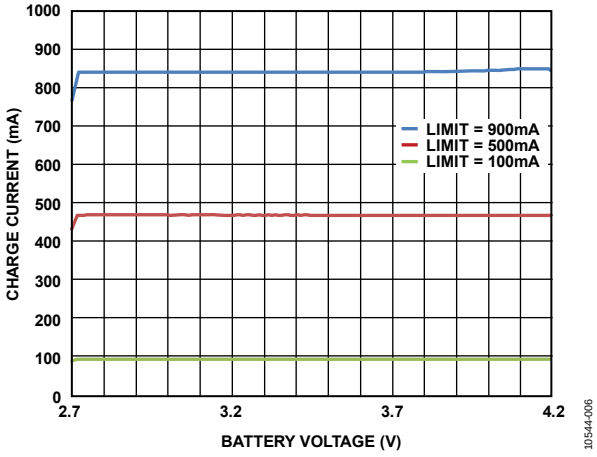

Figure 6. Input Current-Limited Charge Current vs. Battery Voltage

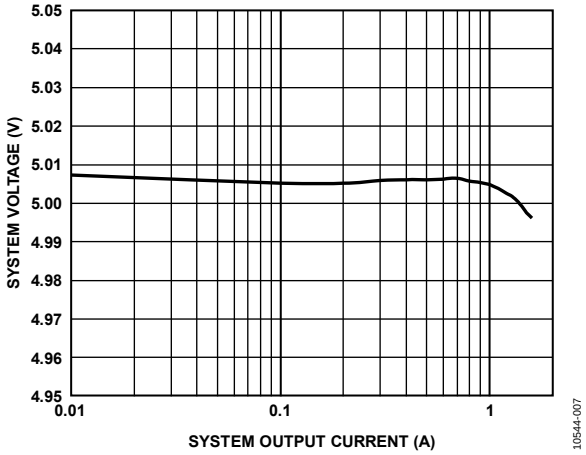

Figure 7. System Voltage vs. System Output Current, LDO Mode, V_{VIN} = 6.0 V, VSYSTEM[2:0] = 111 (Binary) = 5.0 V

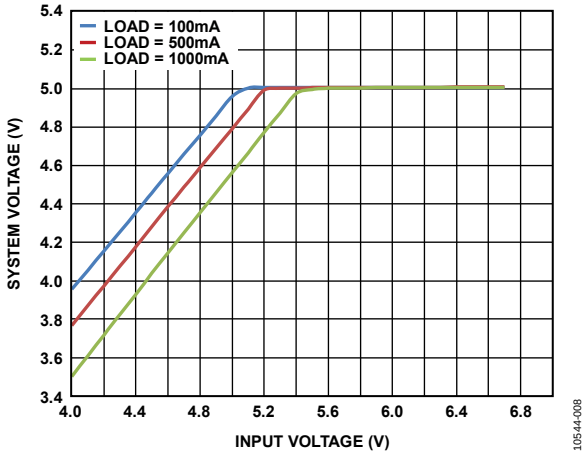

Figure 8. Output Voltage vs. Input Voltage (In Dropout), LDO Mode, VSYSTEM[2:0] = 111 (Binary) = 5.0 V

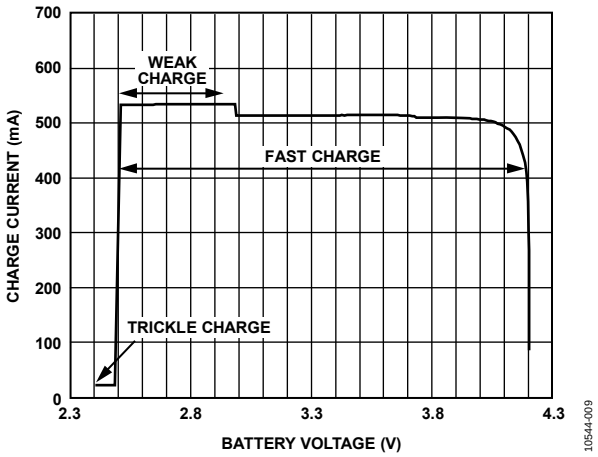

Figure 9. Battery Charge Current vs. Battery Voltage, ICHG[4:0] = 01001 (Binary) = 500 mA, ILIM[3:0] = 1111 (Binary) = 2100 mA

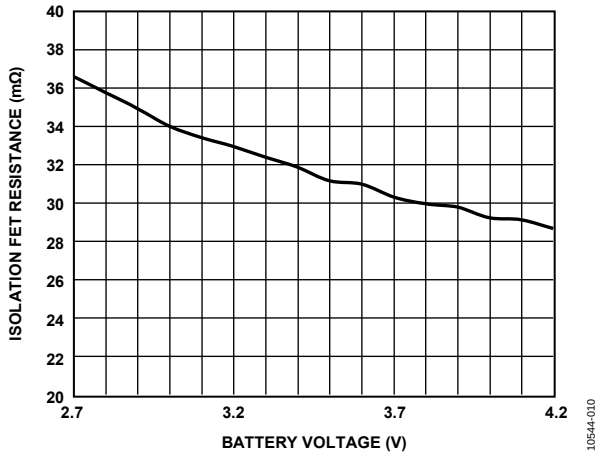

Figure 10. Ideal Diode R_{ON} vs. Battery Voltage, I_{ISO_S} = 500 mA, VINx Open

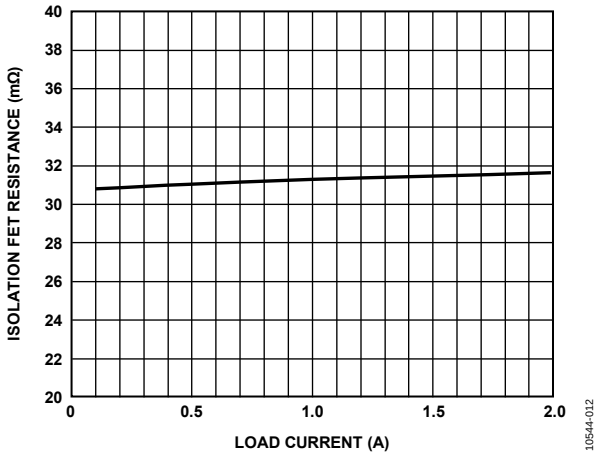

Figure 12. Ideal Diode R_{ON} vs. Load Current, V_{ISO_B} = 3.6 V

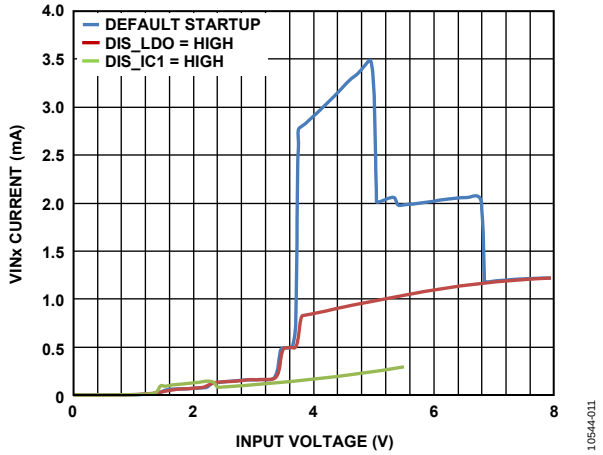

Figure 11. VINx Current vs. VINx Voltage

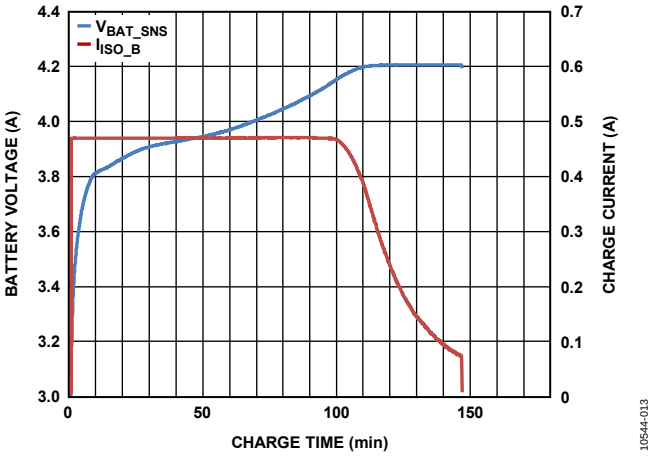

Figure 13. Charge Profile, ILIM[3:0] = 0110 (Binary) = 500 mA, Battery Capacity = 925 mAh

TEMPERATURE CHARACTERISTICS

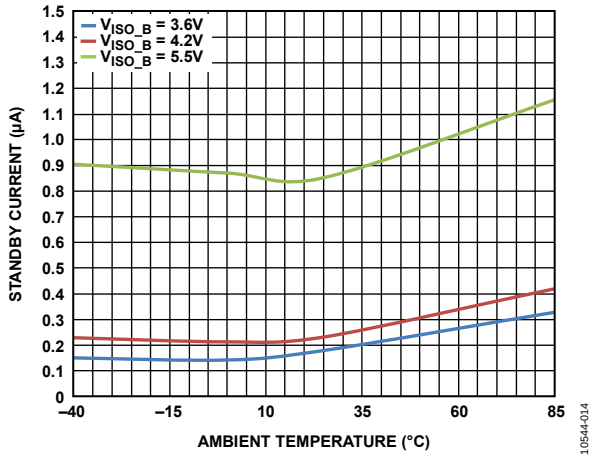

Figure 14. Battery Leakage Current vs. Ambient Temperature

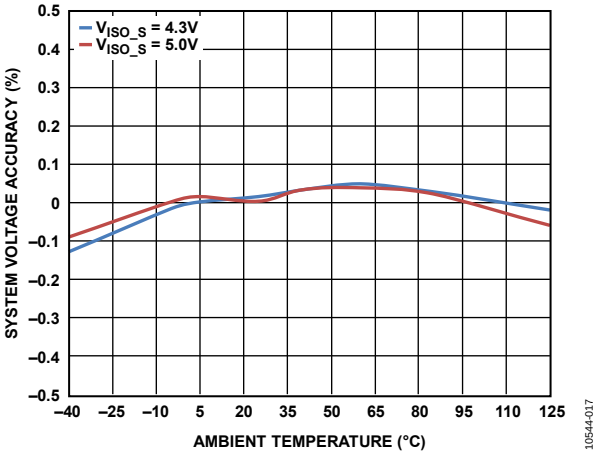

Figure 17. System Voltage vs. Temperature, Trickle Charge Mode, V_{ISO_S} = 4.3 V and VINx = 5.0 V, or V_{ISO_S} = 5.0 V and VINx = 6.0 V

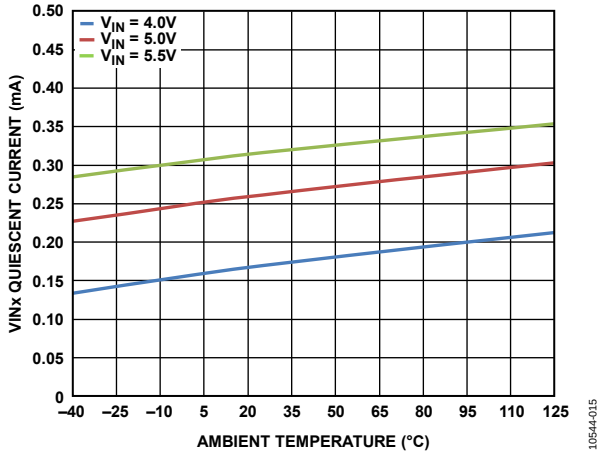

Figure 15. VINx Quiescent Current vs. Ambient Temperature, DIS_IC1 = High

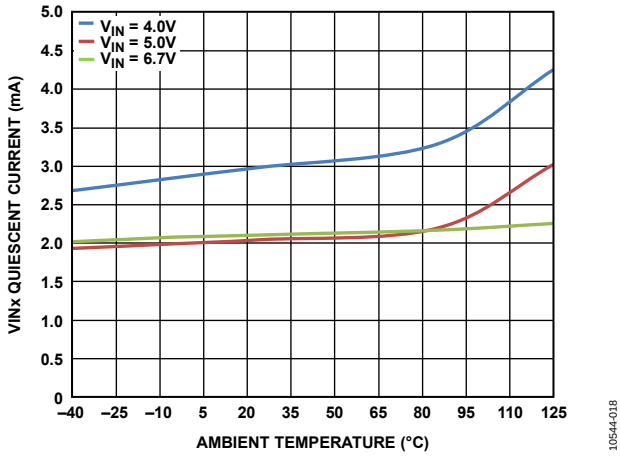

Figure 18. VINx Quiescent Current vs. Ambient Temperature, LDO Mode

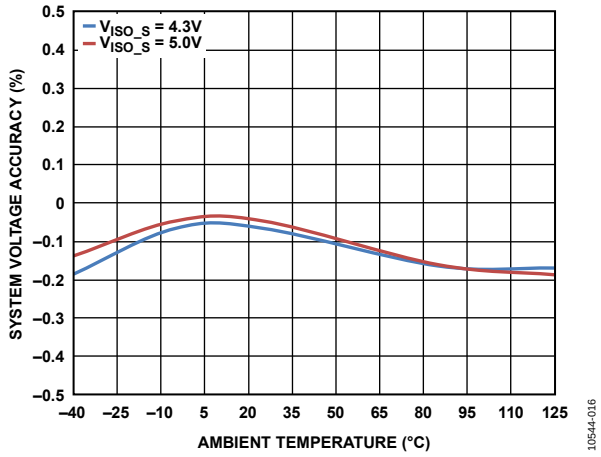

Figure 16. LDO Mode Voltage vs. Ambient Temperature, Load = 100 mA, V_{VIN} = 5.5 V

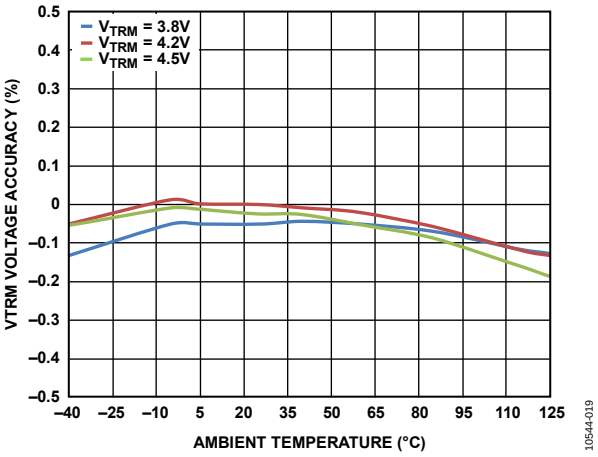

Figure 19. Termination Voltage vs. Ambient Temperature

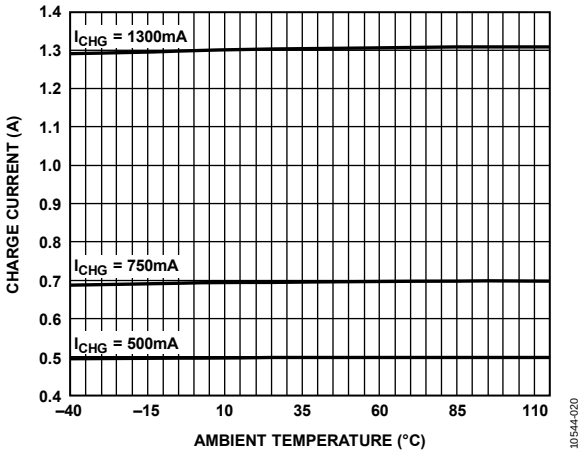

Figure 20. Fast Charge CC Mode Current vs. Ambient Temperature

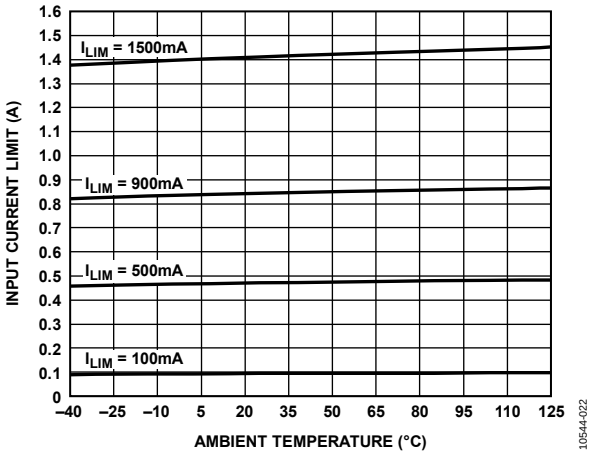

Figure 22. Input Current Limit vs. Ambient Temperature

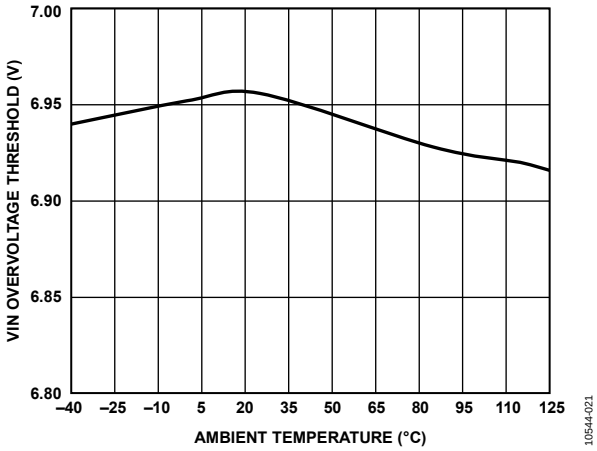

Figure 21. VINx Overvoltage Threshold vs. Ambient Temperature

TYPICAL WAVEFORMS

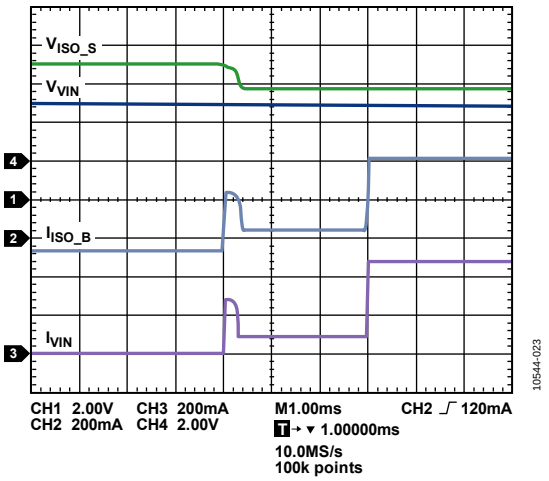

Figure 23. Charging Startup, V_{VIN} = 5.0 V, ILIM[3:0] = 0110 (Binary) = 500 mA, ICHG[4:0] = 01110 (Binary) = 750 mA

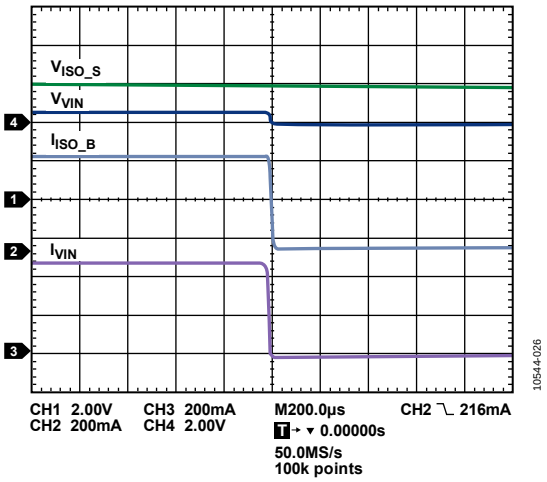

Figure 26. VBUS Disconnect

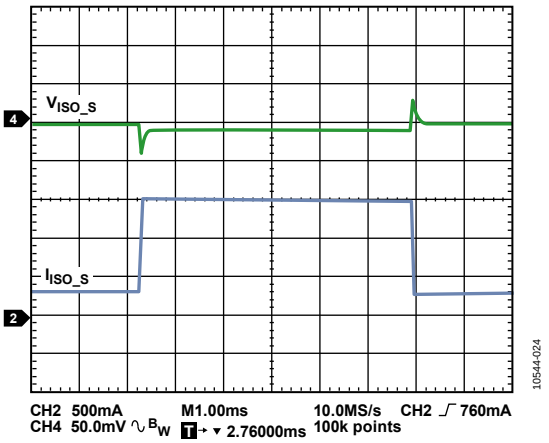

Figure 24. Load Transient, I_{ISO_Sx} Load = 300 mA to 1500 mA to 300 mA

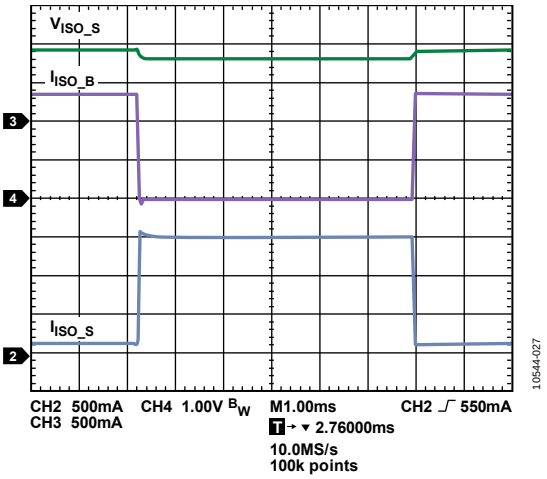

Figure 27. Load Transient. I_{ISO_Sx} Load = 300 mA to 1500 mA to 300 mA, EN_CHG = High, ILIM[3:0] = 0110 (Binary) = 500 mA

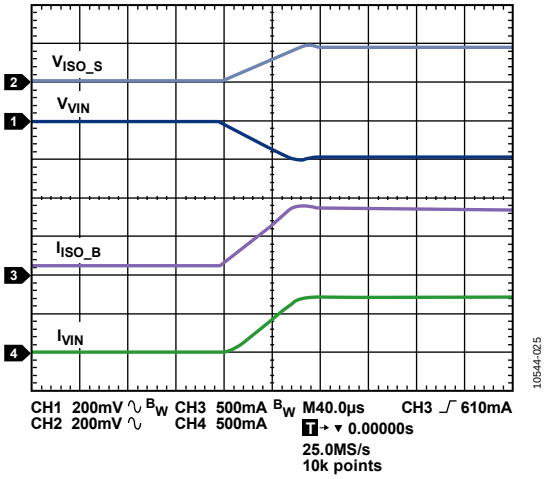

Figure 25. Input Current-Limit Transition from 100 mA to 900 mA, ISO_Sx Load = 66 Ω, Charging = 750 mA

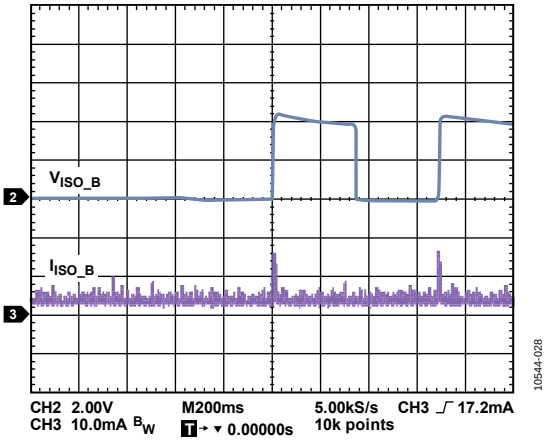

Figure 28. Battery Detection Waveform, VSYSTEM[2:0] = 000 (Binary) = 4.3 V, No Battery

THEORY OF OPERATION

SUMMARY OF OPERATION MODES

Table 7. Summary of the ADP5061 Operation Modes

Mode Name	VINx Condition	Battery Condition	Trickle Charge	LDO FET State	Battery Isolation FET	System Voltage ISO_Sx	Additional Conditions[1]
IC Off, Standby	0 V	Any battery condition	Off	Off	On/Off	Battery voltage or 0 V	Disable IC1
IC Off, Suspend	5 V	Any battery condition	Off	Off	On	Battery voltage	Disable IC1
LDO Mode Off, Isolation FET On	5 V	Any battery condition	Off	Off	On	Battery voltage	Disable LDO and enable isolation FET
LDO Mode Off, Isolation FET Off (System Off)	5 V	Any battery condition	Off	Off	Off	0 V	Enable battery charging
LDO Mode, Charger Off	5 V	Any battery condition	Off	LDO	Off	5.0 V	Enable battery charging
Trickle Charge Mode	5 V	Battery < V_{TRK_DEAD}	On	LDO	Off	5.0 V	Enable battery charging
Weak Charge Mode	5 V	V_{TRK_DEAD} ≤ battery < V_{WEAK}	On	CHG	CHG	3.8 V	Enable battery charging
Fast Charge Mode	5 V	Battery ≥ V_{WEAK}	Off	CHG	CHG	3.8 V (min)	Enable battery charging
Charge Mode, No Battery	5 V	Open	Off	LDO	Off	5.0 V	Enable battery charging
Charge Mode, Battery (ISO_Bx) Short	5 V	Short	On	LDO	Off	5.0 V	Enable battery charging

[1] See Table 8 for details.

Table 8. Operation Mode Controls

Pin Configuration	Equivalent I²C Address, Data	Description			
Enable Battery Charging	0x07, D0	Low = all charging modes disabled (fast, weak, trickle). High = all charging modes enabled (fast, weak, trickle).			
Disable IC1	0x07, D6	**Disable IC1**	**VINx[1] Supply Connected**	**LDO_FET**	**ISO_FET**
		Low	No	Off	On
			Yes	CHG	CHG
		High	No[2]	Off	On
			Yes	Off	On
Disable LDO and Enable Isolation FET	0x07, D3, D0	Low = LDO enabled. High = LDO disabled. In addition, when EN_CHG = low, the battery isolation FET is on; when EN_CHG = high, the battery isolation FET is off.			

[1] When disable IC1 mode is active and the VINx supply is connected, the supply voltage level must fulfill the following condition: $V_{ISO\_Bx} < V_{VINx} < 5.5$ V.

[2] When disable IC1 mode is active, the back gate of the LDO FET is not controlled. If the VINx pins are not connected, the voltage at VINx is $V_{ISO\_Bx} - V_f$ (V_f = forward voltage of the LDO FET body diode).

INTRODUCTION

The ADP5061 is a fully programmable I²C charger for single cell lithium-ion or lithium-polymer batteries suitable for a wide range of portable applications.

The linear charger architecture enables up to 2.1 A output current at 4.3 V to 5.0 V (I²C programmable) on the system power supply, and up to 1.3 A charge current into the battery from a dedicated charger.

The ADP5061 operates from an input voltage of 4 V up to 6.7 V but is tolerant of voltages of up to 20 V. The 20 V voltage tolerance alleviates the concerns of the USB bus spiking during disconnection or connection scenarios.

The ADP5061 features an internal FET between the linear charger output and the battery. This feature permits battery isolation and, hence, system powering under a dead battery or no battery scenario, which allows for immediate system function upon connection to a USB power supply.

The ADP5061 is fully compliant with USB 3.0 and the USB Battery Charging Specification 1.2. The ADP5061 is chargeable via the mini USB VBUS pin from a wall charger, car charger, or USB host port. Based on the type of USB source, which is detected by an external USB detection device, the ADP5061 can be set to apply the correct current limit for optimal charging and USB compliance. The USB charger permits correct operation under all USB-compliant sources such as wall chargers, host chargers, hub chargers, and standard host and hubs.

A processor can control the USB charger using the I²C to program the charging current and numerous other parameters, including

- Trickle charge current level
- Trickle charge voltage threshold
- Weak charge (constant current) current level
- Fast charge (constant current) current level
- Fast charge (constant voltage) voltage level at 1% accuracy
- Fast charge safety timer period
- Watchdog safety timer parameters
- Weak battery threshold detection
- Charge complete threshold
- Recharge threshold
- Charge enable/disable
- Battery pack temperature detection and automatic charger shutdown

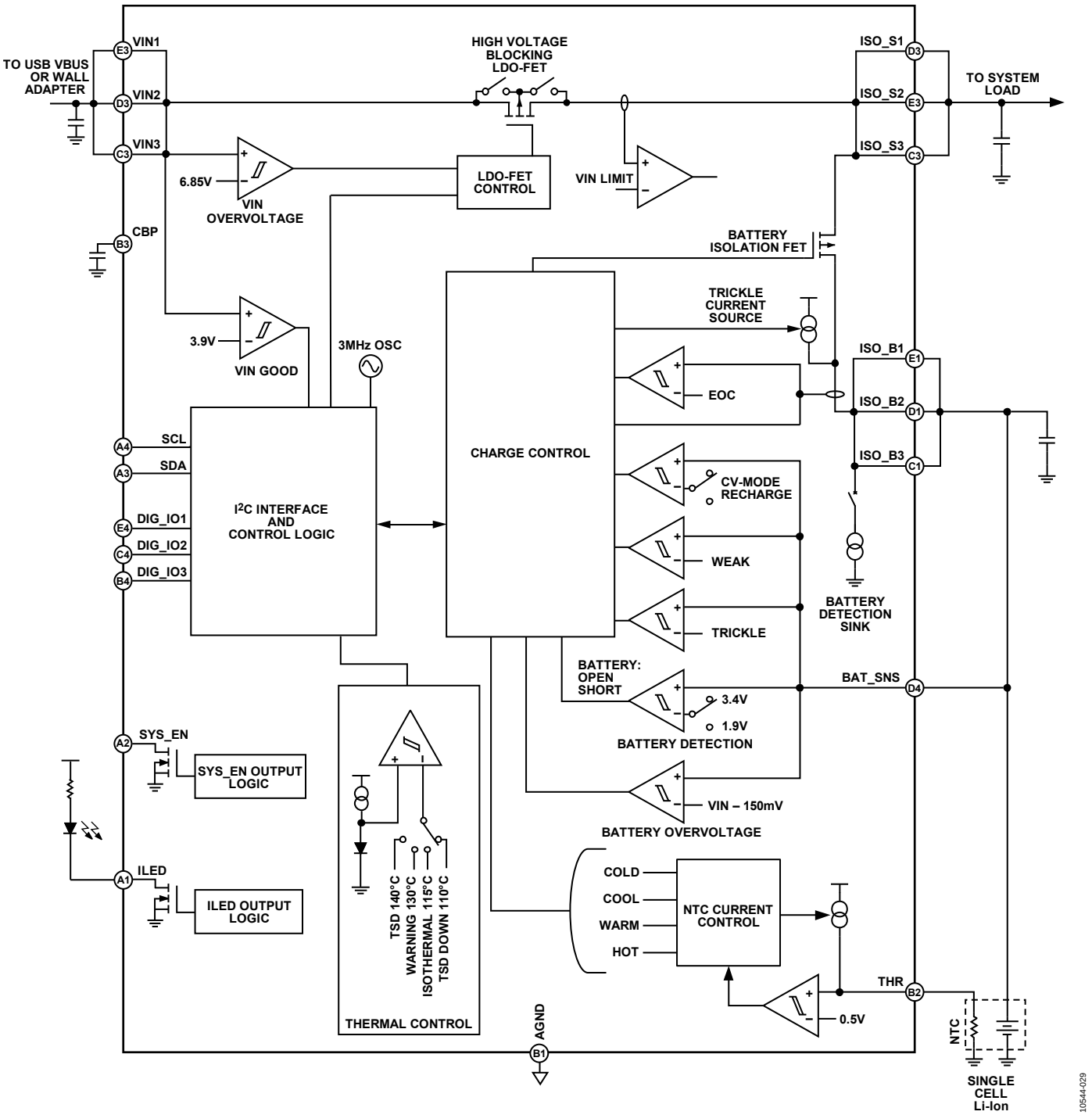

Figure 29. Block Diagram

The ADP5061 includes a number of significant features to optimize charging and functionality including

- Thermal regulation for maximum performance.
- USB host current-limit accuracy: ±5%.
- Termination voltage accuracy: ±1%.
- Battery thermistor input with automatic charger shutdown in the event that the battery temperature exceeds limits (compliant with the JEITA Li-Ion battery charging temperature specification).
- Three external pins (DIG_IO1, DIG_IO2, and DIG_IO3) that directly control a number of parameters. These pins are factory programmable for maximum flexibility. They can be factory programmed for functions such as
  - Enable/disable charging.
  - Control of 100 mA or 500 mA input current limit.
  - Control of 1500 mA input current limit.
  - Control of the battery charge current.
  - Interrupt output pin.

See the Digital Input and Output Options section for details.

CHARGER MODES

Input Current Limit

The VINx input current limit is controlled via the internal I²C ILIM bits. The input current limit can also be controlled via the DIG_IO1 pin (if factory programmed to do so) as outlined in Table 9. Any change in the I²C default from 100 mA dominates over the pin setting.

Table 9. DIG_IO1 Operation

DIG_IO1	Function
0	100 mA input current limit or I²C programmed value
1	500 mA input current limit or I²C programmed value (or reprogrammed I²C value from 100 mA default)

USB Compatibility

The ADP5061 features an I²C programmable input current limit to ensure compatibility with the requirements listed in Table 10. The current limit defaults to 100 mA to allow compatibility with a USB host or hub that is not configured.

The I²C register default is 100 mA. An I²C write command to the ILIM bits override the DIG_IOx pins, and the I²C register default value can be reprogrammed for alternative requirements.

When the input current-limit feature is used, the available input current may be too low for the charger to meet the programmed charging current, I_{CHG}, thereby reducing the rate of charge and setting the VIN_ILIM flag.

When connecting voltage to VINx without the proper voltage level on the battery side, the high voltage blocking mechanism is in a state wherein it draws only the current of <1 mA until V_{IN} reaches the VIN_OK level.

The ADP5061 charger provides support for the following connections through the single connector VINx pin (see Table 10).

Table 10. Input Current Compatibility with Standard USB Limits

Mode	Standard USB Limit	ADP5061 Function
USB (China Only)	100 mA limit for standard USB host or hub	100 mA input current limit or I²C programmed value
	300 mA limit for Chinese USB specification	300 mA input current limit or I²C programmed value
USB 2.0	100 mA limit for standard USB host or hub	100 mA input current limit or I²C programmed value
	500 mA limit for standard USB host or hub	500 mA input current limit or I²C programmed value
USB 3.0	150 mA limit for superspeed USB 3.0 host or hub	150 mA input current limit or I²C programmed value
	900 mA limit for superspeed, high speed USB host or hub charger	900 mA input current limit or I²C programmed value
Dedicated Charger	1500 mA limit for dedicated charger or low/full speed USB host or hub charger	1500 mA input current limit or I²C programmed value

Trickle Charge Mode

A deeply discharged Li-Ion cell can exhibit a very low cell voltage, making it unsafe to charge the cell at high current rates. The ADP5061 charger uses a trickle charge mode to reset the battery pack protection circuit and lift the cell voltage to a safe level for fast charging. A cell with a voltage below V_{TRK_DEAD} is charged with the trickle mode current, I_{TRK_DEAD}. During trickle charging mode, the CHARGER_STATUS bits are set.

During trickle charging, the ISO_Sx node is regulated to V_{ISO_STRK} by the LDO and the battery isolation FET is off, which means that the battery is isolated from the system power supply.

Trickle Charge Mode Timer

The duration of trickle charge mode is monitored to ensure that the battery is revived from its deeply discharged state. If trickle charge mode runs for longer than 60 minutes without the cell voltage reaching V_{TRK_DEAD}, a fault condition is assumed and charging stops. The fault condition is asserted on the CHARGER_STATUS bits, allowing the user to initiate the fault recovery procedure specified in the Fault Recovery section.

Weak Charge Mode (Constant Current)

When the battery voltage exceeds V_{TRK_DEAD} but is less than V_{WEAK}, the charger switches to intermediate charge mode.

During the weak charge mode, the battery voltage is too low to allow the full system to power-up. Because of the low battery level, the USB transceiver cannot be powered and, therefore, cannot enumerate for more current from a USB host. Consequently, the USB limit remains at 100 mA.

The system microcontroller may or may not be powered by the charger output voltage (V_{ISO_SFC}), depending upon the amount of current required by the microcontroller and/or the system architecture. When the ISO_Sx pins power the microcontroller, the battery charge current (I_{CHG_WEAK}) cannot be increased above 20 mA to ensure the microcontroller operation (if doing so), nor can I_{CHG_WEAK} be increased above the 100 mA USB limit. Thus, set the battery charging current as follows:

- Set the default 20 mA via the linear trickle charger branch (to ensure that the microprocessor remains alive if powered by the main charger output, ISO_Sx). Any residual current on the main charger output, ISO_Sx, is used to charge the battery.
- During weak current mode, other features may prevent the weak charging current from reaching its full programmed value. Isothermal charging mode or input current limiting for USB compatibility can affect the programmed weak charging current value under certain operating conditions. During weak charging, the ISO_Sx node is regulated to V_{ISO_SFC} by the battery isolation FET.

Fast Charge Mode (Constant Current)

When the battery voltage exceeds V_{TRK_DEAD} and V_{WEAK}, the charger switches to fast charge mode, charging the battery with the constant current, I_{CHG}. During fast charge mode (constant current), the CHARGER_STATUS bits are set to 010.

During constant current mode, other features may prevent the current, I_{CHG}, from reaching its full programmed value. Isothermal charging mode or input current limiting for USB compatibility can affect the value of I_{CHG} under certain operating conditions. The voltage on ISO_Sx is regulated to stay at V_{ISO_SFC} by the battery isolation FET when $V_{ISO\_B} < V_{ISO\_SFC}$.

Fast Charge Mode (Constant Voltage)

As the battery charges, its voltage rises and approaches the termination voltage, V_{TRM}. The ADP5061 charger monitors the voltage on the BAT_SNS pin to determine when charging should end. However, the internal ESR of the battery pack, combined with the printed circuit board (PCB) and other parasitic series resistances creates a voltage drop between the sense point at the BAT_SNS pin and the cell terminal. To compensate for this and ensure a fully charged cell, the ADP5061 enters a constant voltage charging mode when the termination voltage is detected on the BAT_SNS pin. The ADP5061 reduces charge current gradually as the cell continues to charge, maintaining a voltage of V_{TRM} on the BAT_SNS pin. During fast charge mode (constant voltage), the CHARGER_ STATUS register is set.

Fast Charge Mode Timer

The duration of fast charge mode is monitored to ensure that the battery is charging correctly. If the fast charge mode runs for longer than t_{CHG} without the voltage at the BAT_SNS pin reaching V_{TRM}, a fault condition is assumed and charging stops. The fault condition is asserted on the CHARGER_STATUS bits allowing the user to initiate the fault recovery procedure as specified in the Fault Recovery section.

If the fast charge mode runs for longer than t_{CHG}, and V_{TRM} has been reached on the BAT_SNS pin but the charge current has not yet fallen below I_{END}, charging stops. No fault condition is asserted in this circumstance and charging resumes as normal if the recharge threshold is breached.

Watchdog Timer

The ADP5061 charger features a programmable watchdog timer function to ensure charging is under the control of the processor. The watchdog timer starts running when the ADP5061 charger determines that the processor should be operational, that is, when the processor sets the RESET_WD bit for the first time or when the battery voltage is greater than the weak battery threshold, V_{WEAK}. When the watchdog timer has been triggered, it must be reset regularly within the watchdog timer period, t_{WD}.

While in charger mode, if the watchdog timer expires without being reset, the ADP5061 charger assumes that there is a software problem and triggers the safety timer, t_{SAFE}. For more information, see the Safety Timer section.

Safety Timer

While in charger mode, if the watchdog timer expires, the ADP5061 charger initiates the safety timer, t_{SAFE} (see the Watchdog Timer section). If the processor has programmed charging parameters by the time the charger initiates the safety timer, the I_{LIM} is set to the default value. Charging continues for a period of t_{SAFE}, and then the charger switches off and sets the CHARGER_STATUS bits.

Charge Complete

The ADP5061 charger monitors the charging current while in constant voltage fast charge mode. If the current falls below I_{END} and remains below I_{END} for t_{END}, charging stops and the CHDONE flag is set. If the charging current falls below I_{END} for less than t_{END} and then rises above I_{END} again, the t_{END} timer resets.

Recharge

After the detection of charge complete, and the cessation of charging, the ADP5061 charger monitors the BAT_SNS pin as the battery discharges through normal use. If the BAT_SNS pin voltage falls to V_{RCH}, the charger reactivates charging. Under most circumstances, triggering the recharge threshold results in the charger starting directly into fast charge constant voltage mode.

The recharge function can be disabled in I²C, but a status bit (Register 0x0C, Bit D3) informs the system that a recharge cycle is required.

IC Enable/Disable

The ADP5061 IC can be disabled by the DIG_IO2 digital input pin (if factory programmed to do so) or by the I²C registers. All internal control circuits are disabled when the IC is disabled. Disabling the IC1 option can also control the states of the LDO FET and the battery isolation FET.

It is critical to note that during the disable IC1 mode, a high voltage at VINx passes to the internal supply voltage because all of the internal control circuits are disabled. The VINx supply voltage must fulfill the following condition:

$$V_{ISO\_B} < VINx < 5.5\ V$$

Battery Charging Enable/Disable

The ADP5061 charging function can be disabled by setting the I²C EN_CHG bit to low. The LDO to the system still operates under this circumstance and can be set in I²C to the default or I²C programmed system voltage from 4.3 V to 5.0 V (see the relevant I²C register description for full details).

The ADP5061 charging function can also be controlled via one of the external DIG_IOx pins (if factory programmed to do so). Any change in the I²C EN_CHG bit takes precedence over the pin setting.

Battery Voltage Limit to Prevent Charging

The battery monitor of the ADP5061 charger can be configured to monitor battery voltage and prevent charging when the battery voltage is higher than V_{CHG_VLIM} (typically 3.7 V) during charging start-up (enabled by EN_CHG or DIG_IO3). This function can prevent unnecessary charging of a half discharged battery and, as such, can extend the lifetime of the Li-Ion battery cell. Charging starts automatically when the battery voltage drops below V_{CHG_VLIM} and continues through full charge cycle until the battery voltage reaches V_{TRM} (typically 4.2 V).

By default, the charging voltage limit is disabled and it can be enabled from I²C Register 0x08, Bit EN_CHG_VLIM.

SYS_EN Output

The ADP5061 features a SYS_EN open-drain FET to enable the system until the battery is at the minimum required level for guaranteed system start-up. When there are minimum battery voltage and/or minimum battery charge level requirements, the operation of SYS_EN can be set by I²C programming. The SYS_EN operation can be factory programmed to four different operating conditions as described in Table 11.

Table 11. SYS_EN Mode Descriptions

SYS_EN Mode Selection	Description
00	SYS_EN is activated when LDO is active and system voltage is available.
01	SYS_EN is activated by the ISO_Bx voltage, battery charging mode.
10	SYS_EN is activated and the isolation FET is disabled when the battery drops below V_{WEAK}. This option is active, when VINx = 0 V and the battery monitor is activated from Register 0x07, Bit D5 (EN_BMON).
11	SYS_EN is active in LDO mode when the charger is disabled. SYS_EN is active in charging mode when ISO_Bx ≥ V_{WEAK}.

Indicator LED Output (ILED)

The ILED is an open-drain output for indicator LED connection. Optionally, the ILED output can be used as a status output for a microcontroller. Indicator LED modes are shown in Table 12.

Table 12. Indicator LED Operation Modes

ADP5061 Mode	ILED Mode	On/Off Time
IC Off	Off	
LDO Mode Off	Off	
LDO Mode On	Off	
Charge Mode	Continuously on	
Timer Error (t_{TRK}, t_{CHG}, t_{SAFE})	Blinking	167 ms/833 ms
Overtemperature (T_{SD})	Blinking	1 sec/1 sec

THERMAL MANAGEMENT

Isothermal Charging

The ADP5061 includes a thermal feedback loop that limits the charge current when the die temperature exceeds T_{LIM} (typically 115°C). As the on-chip power dissipation and die temperature increase, the charge current is automatically reduced to maintain the die temperature within the recommended range. As the die temperature decreases due to lower on-chip power dissipation or ambient temperature, the charge current returns to the programmed level. During isothermal charging, the THERM_LIM I^2C flag is set to high.

This thermal feedback control loop allows the user to set the programmed charge current based on typical rather than worst case conditions.

The ADP5061 does not include a thermal feedback loop to limit ISO_Sx load current in LDO mode. If the power dissipated on the chip during LDO mode causes the die temperature to exceed 130°C, an interrupt is generated. If the die temperature continues to rise beyond 140°C, the device enters into thermal shutdown.

Thermal Shutdown and Thermal Early Warning

The ADP5061 charger features a thermal shutdown threshold detector. If the die temperature exceeds T_{SD}, the ADP5061 charger is disabled, and the TSD 140°C bit is set. The ADP5061 charger can be reenabled when the die temperature drops below the T_{SD} falling limit and the TSD 140°C bit is reset. To reset the TSD 140°C bit, write to the I^2C Fault Register 0x0D or cycle the power.

Before die temperature reaches T_{SD}, the early warning bit is set if T_{SDL} is exceeded. This allows the system to accommodate power consumption before thermal shutdown occurs.

Fault Recovery

Before performing the following operation, it is important to ensure that the cause of the fault has been rectified.

To recover from a charger fault (when the CHARGER_STATUS = 110), cycle power on VINx or write high to reset the I^2C fault bits in the fault register.

BATTERY ISOLATION FET

The ADP5061 charger features an integrated battery isolation FET for power path control. The battery isolation FET isolates a deeply discharged Li-Ion cell from the system power supply in both trickle and fast charge modes, thereby allowing the system to be powered at all times.

When VINx is below V_{VIN_OK}, the battery isolation FET is in full conducting mode.

The battery isolation FET is off during trickle charge mode. When the battery voltage exceeds V_{TRK}, the battery isolation FET switches to the system voltage regulation mode. During system voltage regulation mode, the battery isolation FET maintains the V_{ISO_SFC} voltage on the ISO_Sx pins. When the battery voltage exceeds V_{ISO_SFC}, the battery isolation FET is in full conducting mode.

The battery isolation FET supplements the battery to support high current functions on the system power supply. When voltage on ISO_Sx drops below ISO_Bx, the battery isolation FET enters into full conducting mode. When voltage on ISO_Sx rises above ISO_Bx, the isolation FET enters regulating mode or full conduction mode, depending on the Li-Ion cell voltage and the linear charger mode.

BATTERY DETECTION

Battery Voltage Level Detection

The ADP5061 charger features a battery detection mechanism to detect an absent battery. The charger actively sinks and sources current into the ISO_Bx/BAT_SNS node, and voltage vs. time is detected. The sink phase is used to detect a charged battery, whereas the source phase is used to detect a discharged battery.

The sink phase (see Figure 30) sinks I_{SINK} current from the ISO_Bx/ BAT_SNS pins for a time period, t_{BATOK}. If the BAT_SNS pin is below V_{BATL} when the t_{BATOK} timer expires, the charger assumes no battery is present, and starts the source phase. If the BAT_SNS exceeds the V_{BATL} voltage when the t_{BATOK} timer expires, the charger assumes the battery is present and begins a new charge cycle.

The source phase sources I_{SOURCE} current to ISO_Bx and the BAT_SNS pin for a time period, t_{BATOK}. If BAT_SNS pin exceeds V_{BATH} before the t_{BATOK} timer expires, the charger assumes that no battery is present. If the BAT_SNS does not exceed the V_{BATH} voltage when the t_{BATOK} timer expires, the charger assumes that a battery is present and begins a new charge cycle.

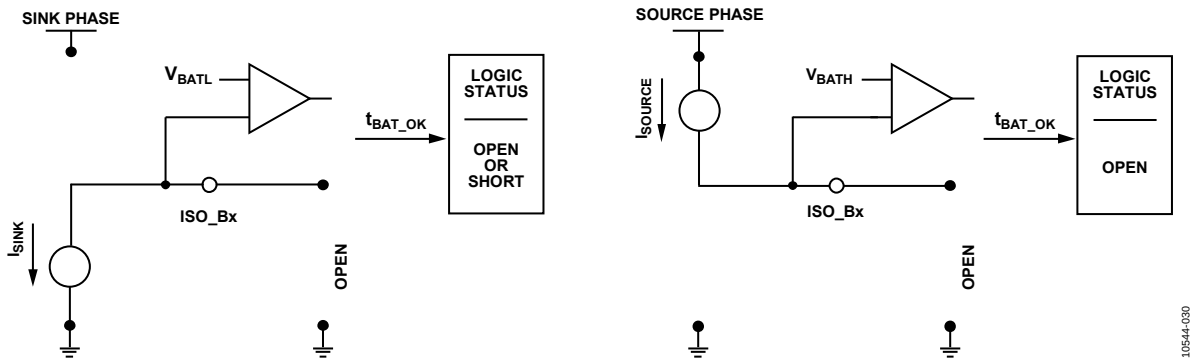

Figure 30. Sink Phase

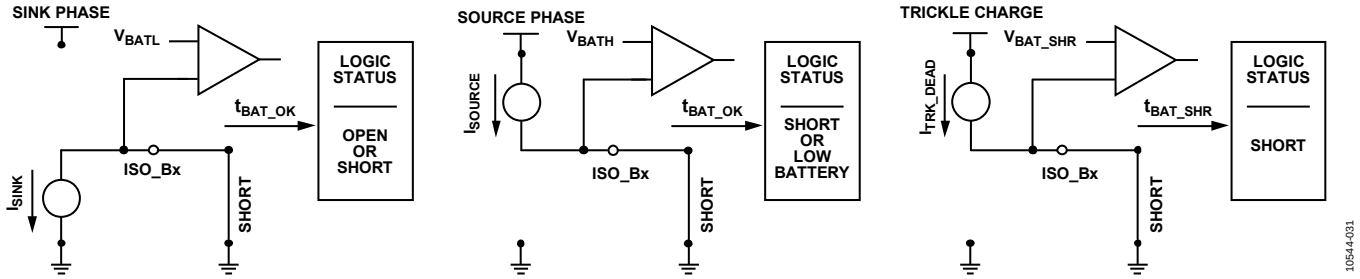

Figure 31. Trickle Charge

Battery (ISO_Bx) Short Detection

A battery short occurs under a damaged battery condition or when the battery protection circuitry is enabled.

On commencing trickle charging, the ADP5061 charger monitors the battery voltage. If this battery voltage does not exceed V_{BAT_SHR} within the specified timeout period, t_{BAT_SHR}, a fault is declared and the charger is stopped by turning the battery isolation FET off, but the system voltage is maintained at V_{ISO_STRK} by the linear regulator.

After source phase, if the ISO_Bx or BAT_SNS level remains below V_{BATH}, either the battery voltage is low or the battery node can be shorted. Because the battery voltage is low, trickle charging mode is initiated (see Figure 31). If the BAT_SNS level remains below V_{BAT_SHR} after t_{BAT_SHR} has elapsed, the ADP5061 assumes that the battery node is shorted.

The trickle charge branch is active during the battery short scenario, and trickle charge current to the battery is maintained until the 60-minute trickle charge mode timer expires.

BATTERY PACK TEMPERATURE SENSING

Battery Thermistor Input

The ADP5061 charger features battery pack temperature sensing that precludes charging when the battery pack temperature is outside the specified range. The THR pin provides an on and off switching current source that should be connected directly to the battery pack thermistor terminal. The activation interval of the THR current source is 167 ms.

The battery pack temperature sensing can be controlled by I²C, using the conditions shown in Table 13. Note that the I²C register default setting for EN_THR (Register 0x07) is 0 = temperature sensing off.

Table 13. THR Input Function

Conditions		
VINx	**V_{ISO_B}**	**THR Function**
Open or V_{IN} = 0 V to 4.0 V	<2.5 V	Off
Open or V_{IN} = 0 V to 4.0 V	>2.5 V	Off, controlled by I²C
4.0 V to 6.7 V	Don't care	Always on

If the battery pack thermistor is not connected directly to the THR pin, a 10 kΩ (tolerance ±20%) dummy resistor must be connected between the THR input and GND. Leaving the THR pin open results in a false detection of the battery temperature being <0°C and charging is disabled.

The ADP5061 charger monitors the voltage in the THR pin and suspends charging if the current is outside the range of less than 0°C or greater than 60°C.

The ADP5061 charger is designed for use with an NTC thermistor in the battery pack with a nominal room temperature value of either 10 kΩ at 25°C or 100 kΩ at 25°C, which is selected by factory programming.

The ADP5061 charger is designed for use with an NTC thermistor in the battery pack with a temperature coefficient curve (beta). Factory programming supports eight beta values covering a range from 3150 to 4400 (see Table 44).

JEITA Li-Ion Battery Temperature Charging Specification

The ADP5061 is compliant with the JEITA1 and JEITA2 Li-Ion battery charging temperature specifications as outlined in Table 14 and in Table 16, respectively.

JEITA function can be enabled via the I²C interface and, optionally, the JEITA1 or JEITA2 function can be selected in I²C. Alternatively, the JEITA1 or JEITA2 can be set as enabled to default by factory programming.

When the ADP5061 identifies a hot or cold battery condition, the ADP5061 takes the following actions:

- Stops charging the battery.
- Connects or enables the battery isolation FET such that the ADP5061 continues in LDO mode.

Table 14. JEITA1 Specifications

Parameter	Symbol	Conditions	Min	Max	Unit
JEITA1 Cold Temperature Limits	I_{JEITA_COLD}	No battery charging occurs		0	°C
JEITA1 Cool Temperature Limits	I_{JEITA_COOL}	Battery charging occurs at approximately 50% of programmed level—see Table 15 for specific charging current reduction levels	0	10	°C
JEITA1 Typical Temperature Limits	I_{JEITA_TYP}	Normal battery charging occurs at default/programmed levels	10	45	°C
JEITA1 Warm Temperature Limits	I_{JEITA_WARM}	Battery termination voltage (V_{TRM}) is reduced by 100 mV from programmed value	45	60	°C
JEITA1 Hot Temperature Limits	I_{JEITA_HOT}	No battery charging occurs	60		°C

Table 15. JEITA1 Reduced Charge Current Levels, Battery Cool Temperature

ICHG[4:0] (Default)	ICHG JEITA1	ICHG[4:0] (Default)	ICHG JEITA1
00000 = 50 mA	50 mA	01100 = 650 mA	300 mA
00001 = 100 mA	50 mA	01101 = 700 mA	350 mA
00010 = 150 mA	50 mA	01110 = 750 mA	350 mA
00011 = 200 mA	100 mA	01111 = 800 mA	400 mA
00100 = 250 mA	100 mA	10000 = 850 mA	400 mA
00101 = 300 mA	150 mA	10001 = 900 mA	450 mA
00110 = 350 mA	150 mA	10010 = 950 mA	450 mA
00111 = 400 mA	200 mA	10011 = 1000 mA	500 mA
01000 = 450 mA	200 mA	10100 = 1050 mA	500 mA
01001 = 500 mA	250 mA	10101 = 1100 mA	550 mA
01010 = 550 mA	250 mA	10110 = 1200 mA	600 mA
01011 = 600 mA	300 mA	10111 = 1300 mA	650 mA

Table 16. JEITA2 Specifications

Parameter	Symbol	Conditions	Min	Max	Unit
JEITA2 Cold Temperature Limits	I_{JEITA_COLD}	No battery charging occurs		0	°C
JEITA2 Cool Temperature Limits	I_{JEITA_COOL}	Battery termination voltage (V_{TRM}) is reduced by 100 mV from programmed value	0	10	°C
JEITA2 Typical Temperature Limits	I_{JEITA_TYP}	Normal battery charging occurs at default/programmed levels	10	45	°C
JEITA2 Warm Temperature Limits	I_{JEITA_WARM}	Battery termination voltage (V_{TRM}) is reduced by 100 mV from programmed value	45	60	°C
JEITA2 Hot Temperature Limits	I_{JEITA_HOT}	No battery charging occurs	60		°C

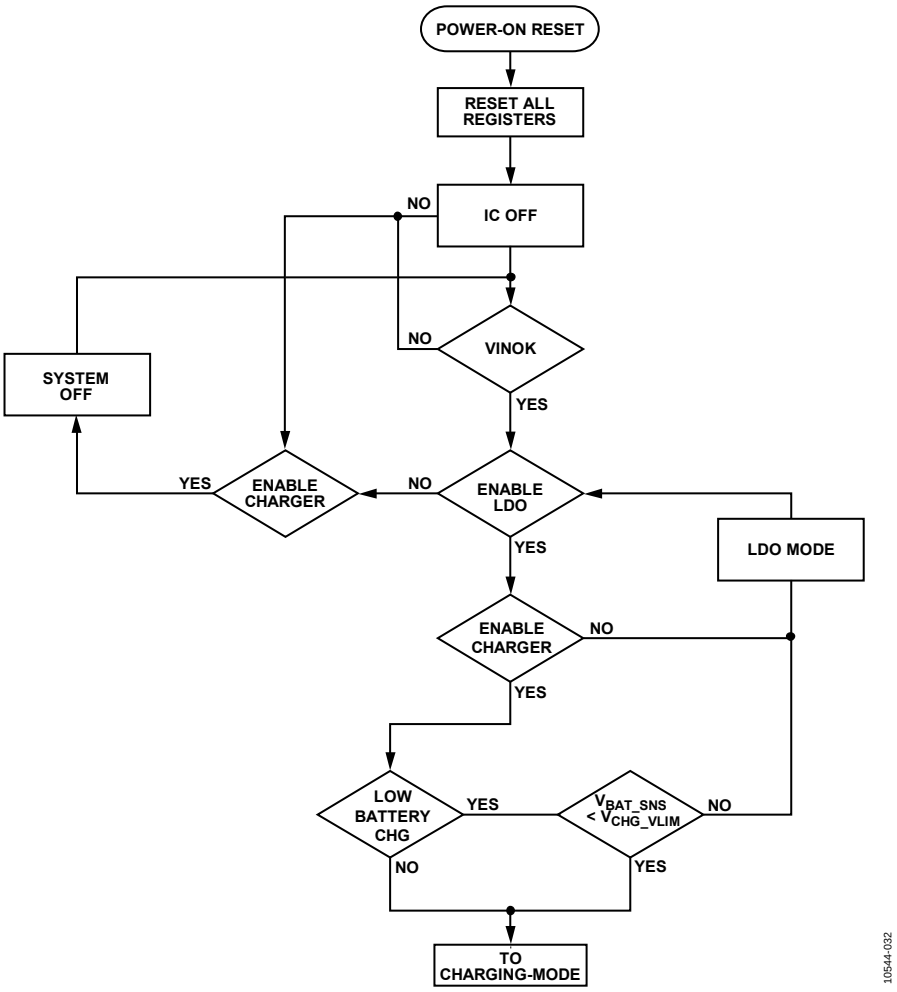

Figure 32. Simplified Battery and VIN Connect Flowchart

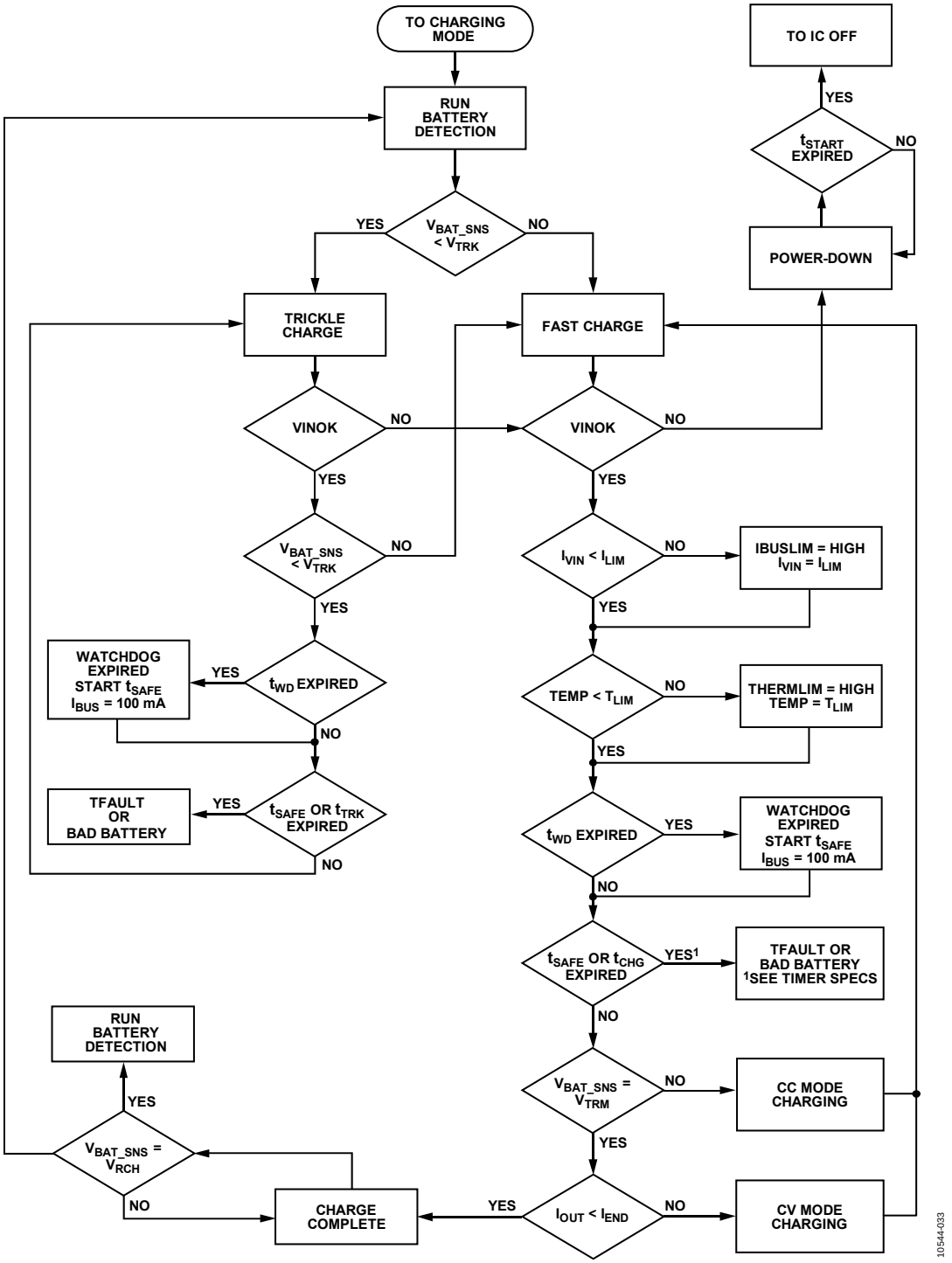

Figure 33. Simplified Charging Mode Flowchart

I²C INTERFACE

The ADP5061 includes an I²C-compatible serial interface for control of the charging and LDO functions, as well as for a readback of system status registers. The I²C chip address is 0x28 in write mode and 0x29 in read mode.

Registers values are reset to the default values when the VINx supply falls below the V_{VIN_OK} falling voltage threshold. The I²C registers also reset when the battery is disconnected and V_{IN} is 0 V.

The subaddress content selects which of the ADP5061 registers is written to first. The ADP5061 sends an acknowledgement to the master after the 8-bit data byte has been written (see Figure 34 for an example of the I²C write sequence to a single register). The ADP5061 increments the subaddress automatically and starts receiving a data byte at the next register until the master sends an I²C stop as shown in Figure 35.

Figure 36 shows the I²C read sequence of a single register. ADP5061 sends the data from the register denoted by the subaddress and increments the subaddress automatically, sending data from the next register until the master sends an I²C stop condition as shown in Figure 37.

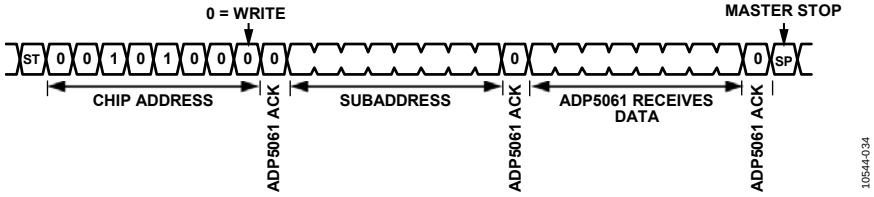

Figure 34. I²C Single Register Write Sequence

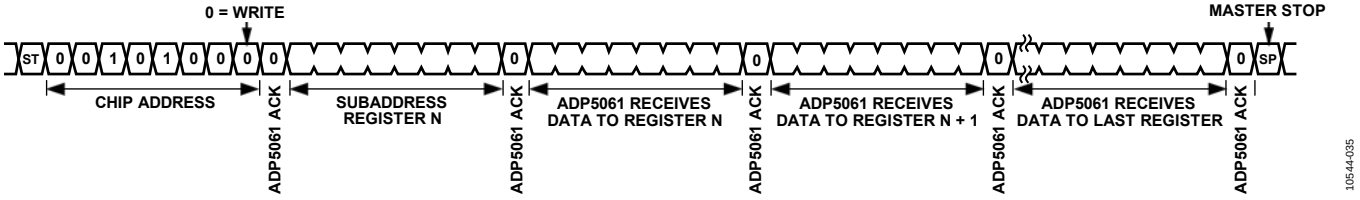

Figure 35. I²C Multiple Register Write Sequence

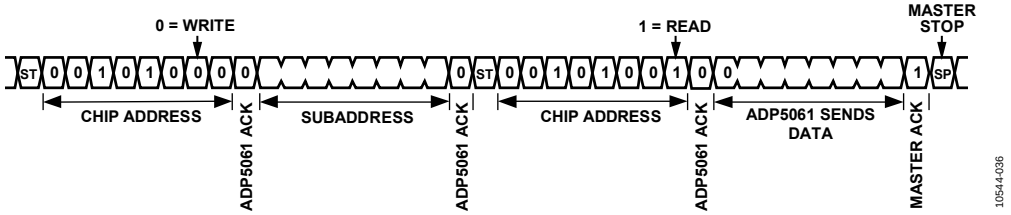

Figure 36. I²C Single Register Read Sequence

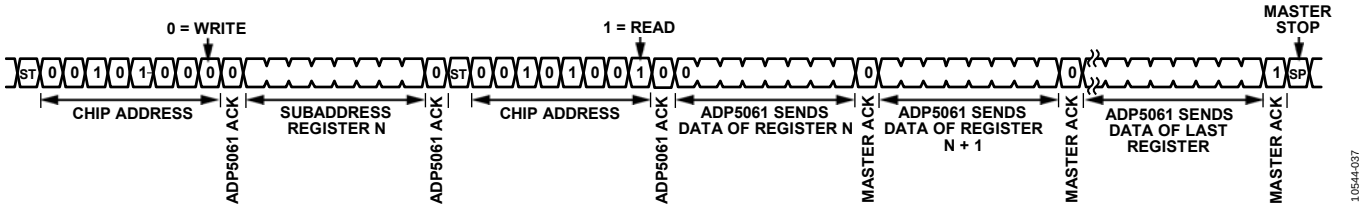

Figure 37. I²C Multiple Register Read Sequence

I²C REGISTER MAP

See the Factory Programmable Options section for programming option details. Note that a blank cell indicates a bit that is not used.

Table 17. I²C Register Map

Register									
Addr.	**Name**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x00	Manufacturer and model ID	MANUF				Model			
0x01	Silicon revision					REV			
0x02	VINx pins settings					ILIM[1]			
0x03	Termination settings	VTRM[1, 2]						CHG_VLIM[1:0] [1, 2]	
0x04	Charging current		ICHG[1, 2]					ITRK_DEAD[1]	
0x05	Voltage thresholds	DIS_RCH[1, 3]	VRCH[1]		VTRK_DEAD[1, 3]		VWEAK[1]		
0x06	Timer settings			EN_TEND[1]	EN_CHG_TIMER[1]	CHG_TMR_PERIOD[1]	EN_WD[1, 3]	WD_PERIOD[1]	RESET_WD
0x07	Functional Settings 1		DIS_IC1[1]	EN_BMON[1]	EN_THR[1]	DIS_LDO[1]	EN_EOC[1]		EN_CHG[1]
0x08	Functional Settings 2	EN_JEITA[1, 3]	JEITA_SELECT[1, 3]	EN_CHG_VLIM[1, 3]	IDEAL_DIODE[1:0][1, 3]		VSYSTEM[2:0][1, 3]		
0x09	Interrupt enable		EN_THERM_LIM_INT	EN_WD_INT	EN_TSD_INT	EN_THR_INT	EN_BAT_INT	EN_CHG_INT	EN_VIN_INT
0x0A	Interrupt active		THERM_LIM_INT	WD_INT	TSD_INT	THR_INT	BAT_INT	CHG_INT	VIN_INT
0x0B	Charger Status 1	VIN_OV	VIN_OK	VIN_ILIM	THERM_LIM	CHDONE	CHARGER_STATUS		
0x0C	Charger Status 2	THR_STATUS				RCH_LIM_INFO	BATTERY_STATUS		
0x0D	Fault register					BAT_SHR[1]		TSD 130°C[1]	TSD 140°C[1]
0x10	Battery short	TBAT_SHR[1]					VBAT_SHR[1]		
0x11	IEND	IEND[1, 3]			C/20 EOC[1]	C/10 EOC[1]	C/5 EOC[1]	SYS_EN_SET[1, 3]	

[1] These bits reset to default I²C values when VINx is connected or disconnected.
[2] The default I²C values of these bits are partially factory programmable.
[3] The default I²C values of these bits are fully factory programmable.

REGISTER BIT DESCRIPTIONS

In Table 18 through Table 33, the following abbreviations are used: R is read only, W is write only, R/W is read/write, and N/A means not applicable.

Table 18. Manufacturer and Model ID, Register Address 0x00

Bit No.	Bit Name	Access	Default	Description
[7:4]	MANUF[3:0]	R	0001	The 4-bit manufacturer identification bus
[3:0]	MODEL[3:0]	R	1001	The 4-bit model identification bus

Table 19. Silicon Revision Register, Register Address 0x01

Bit No.	Bit Name	Access	Default	Description
[7:4]	Not used	R		
[3:0]	REV[3:0]	R	0100	The 4-bit silicon revision identification bus

Table 20. VINx Settings Register, Register Address 0x02

Bit No.	Bit Name	Access	Default	Description
[7:5]	Not used	R		
4	RFU	R/W	0	Reserved for future use.
[3:0]	ILIM[3:0]	R/W	0000 = 100 mA	VINx input current-limit programming bus. The current into VINx can be limited to the following programmed values: 0000 = 100 mA. 0001 = 150 mA. 0010 = 200 mA. 0011 = 250 mA. 0100 = 300 mA. 0101 = 400 mA. 0110 = 500 mA. 0111 = 600 mA. 1000 = 700 mA. 1001 = 800 mA. 1010 = 900 mA. 1011 = 1000 mA. 1100 = 1200 mA. 1101 = 1500 mA. 1110 = 1800 mA. 1111 = 2100 mA.

Table 21. Termination Settings, Register Address 0x03

Bit No.	Bit Name	Access	Default	Description
[7:2]	VTRM[5:0]	R/W	100011 = 4.20 V	Termination voltage programming bus. The values of the float voltage can be programmed to the following values: 001111 = 3.80 V. 010000 = 3.82 V. 010001 = 3.84 V. 010010 = 3.86 V. 010011 = 3.88 V. 010100 = 3.90 V. 010101 = 3.92 V. 010110 = 3.94 V. 010111 = 3.96 V. 011000 = 3.98 V. 011001 = 4.00 V. 011010 = 4.02 V. 011011 = 4.04 V. 011100 = 4.06 V. 011101 = 4.08 V. 011110 = 4.10 V. 011111 = 4.12 V. 100000 = 4.14 V. 100001 = 4.16 V. 100010 = 4.18 V. 100011 = 4.20 V. 100100 = 4.22 V. 100101 = 4.24 V. 100110 = 4.26 V. 100111 = 4.28 V. 101000 = 4.30 V. 101001 = 4.32 V. 101010 = 4.34 V. 101011 = 4.36 V. 101100 = 4.38 V. 101101 = 4.40 V. 101110 = 4.42 V. 101111 = 4.44 V. 110000 = 4.44 V. 110001 = 4.46 V. 110010 = 4.48 V. 110011 to 111111 = 4.50 V.
[1:0]	CHG_VLIM[1:0]	R/W	00 = 3.2 V	Charging voltage limit programming bus. The values of the charging voltage limit can be programmed to the following values: 00 = 3.2 V. 01 = 3.4 V. 10 = 3.7 V. 11 = 3.8 V.

Table 22. Charging Current Settings, Register Address 0x04

Bit No.	Bit Name	Access	Default	Description
7	Not used	R		
[6:2]	ICHG[4:0]	R/W	See Table 39 for the model-specific default values.	Fast charge current programming bus. The values of the constant current charge can be programmed to the following values: 00000 = 50 mA. 00001 = 100 mA. 00010 = 150 mA. 00011 = 200 mA. 00100 = 250 mA. 00101 = 300 mA. 00110 = 350 mA. 00111 = 400 mA. 01000 = 450 mA. 01001 = 500 mA. 01010 = 550 mA. 01011 = 600 mA. 01100 = 650 mA. 01101 = 700 mA. 01110 = 750 mA. 01111 = 800 mA. 10000 = 850 mA. 10001 = 900 mA. 10010 = 950 mA. 10011 = 1000 mA. 10100 = 1050 mA. 10101 = 1100 mA. 10110 = 1200 mA. 10111 to 11111 = 1300 mA.
[1:0]	ITRK_DEAD[1:0]	R/W	10 = 20 mA	Trickle and weak charge current programming bus. The values of the trickle and weak charge currents can be programmed to the following values: 00 = 5 mA. 01 = 10 mA. 10 = 20 mA. 11 = 80 mA.

Table 23. Voltage Thresholds, Register Address 0x05

Bit No.	Bit Name	Access	Default	Description
7	DIS_RCH	R/W	0 = recharge enabled	0 = recharge enabled. 1 = recharge disabled.
[6:5]	VRCH[1:0]	R/W	11 = 260 mV	Recharge voltage programming bus. The values of the recharge threshold can be programmed to the following values (note that the recharge cycle can be disabled in I^2C by the DIS_RCH bit): 00 = 80 mV. 01 = 140 mV. 10 = 200 mV. 11 = 260 mV.

Bit No.	Bit Name	Access	Default	Description
[4:3]	VTRK_DEAD[1:0]	R/W	01 = 2.5 V	Trickle to fast charge dead battery voltage programming bus. The values of the trickle to fast charge threshold can be programmed to the following values: 00 = 2.0 V. 01 = 2.5 V. 10 = 2.6 V. 11 = 2.9 V.
[2:0]	VWEAK[2:0]	R/W	011 = 3.0 V	Weak battery voltage rising threshold. 000 = 2.7 V. 001 = 2.8 V. 010 = 2.9 V. 011 = 3.0 V. 100 = 3.1 V. 101 = 3.2 V. 110 = 3.3 V. 111 = 3.4 V.

Table 24. Timer Settings, Register Address 0x06

Bit No.	Bit Name	Access	Default	Description
[7:6]	Not used			
5	EN_TEND	R/W	1	0 = charge complete timer, t_{END}, disabled. A 31 ms deglitch timer remains on. 1 = charge complete timer enabled.
4	EN_CHG_TIMER	R/W	1	0 = trickle/fast charge timer disabled. 1 = trickle/fast charge timer enabled.
3	CHG_TMR_PERIOD	R/W	1	Trickle and fast charge timer period. 0 = 30 sec trickle charge timer and 300 minute fast charge timer. 1 = 60 sec trickle charge timer and 600 minute fast charge timer.
2	EN_WD	R/W	0	0 = watchdog timer is disabled even when BAT_SNS exceeds V_{DEAD}. 1 = watchdog timer safety timer is enabled.
1	WD_PERIOD	R/W	0	Watchdog safety timer period. 0 = 32 sec watchdog timer and 40 minute safety timer. 1 = 64 sec watchdog timer and 40 minute safety timer.
0	RESET_WD	W	0	When RESET_WD is set to logic high by I^2C, the watchdog safety timer is reset.

Table 25. Functional Settings 1, Register Address 0x07

Bit No.	Bit Name	Access	Default	Description
7	Not used			
6	DIS_IC1	R/W	0	0 = normal operation. 1 = the ADP5061 is disabled, V_{VIN} must be $V_{ISO\_B} < V_{VIN} < 5.5$ V.
5	EN_BMON	R/W	0	0 = when $V_{VIN} < V_{VIN\_OK}$, the battery monitor is disabled. When V_{VIN} = 4.0 to 6.7 V, the battery monitor is enabled regardless of the EN_BMON state. 1 = the battery monitor is enabled even when the voltage at the VINx pins is below V_{VIN_OK}.
4	EN_THR	R/W	0	0 = when $V_{VIN} < V_{VIN\_OK}$, the THR current source is disabled. When V_{VIN} = 4.0 V to 6.7 V, the THR current source is enabled regardless of the EN_THR state. 1 = THR current source is enabled even when the voltage at the VINx pins is below V_{VIN_OK}.
3	DIS_LDO	R/W	0	0 = LDO is enabled. 1 = LDO is off. In addition, If EN_CHG = low, the battery isolation FET is on. If EN_CHG = high, the battery isolation FET is off.

Bit No.	Bit Name	Access	Default	Description
2	EN_EOC	R/W	1	0 = end of charge not allowed. 1 = end of charge allowed.
1	Not used			
0	EN_CHG	R/W	0	0 = battery charging is disabled. 1 = battery charging is enabled.

Table 26. Functional Settings 2, Register Address 0x08

Bit No.	Bit Name	Access	Default	Description
7	EN_JEITA	R/W	0 = JEITA disabled	0 = JEITA compliance of the Li-Ion temperature battery charging specifications is disabled. 1 = JEITA compliance enabled.
6	JEITA_SELECT	R/W	0 = JEITA1	0 = JEITA1 is selected. 1 = JEITA2 is selected.
5	EN_CHG_VLIM	R/W	0	0 = charging voltage limit disabled. 1 = voltage limit activated. The charger prevents charging until the battery voltage drops below the V_{CHG_VLIM} threshold.
[4:3]	IDEAL_DIODE[1:0]	R/W	00	00 = ideal diode operates always when $V_{ISO\_S} < V_{ISO\_B}$. 01 = ideal diode operates when $V_{ISO\_S} < V_{ISO\_B}$ and $V_{BAT\_SNS} > V_{WEAK}$. 10 = ideal diode is disabled. 11 = ideal diode is disabled.
[2:0]	VSYSTEM[2:0]	R/W	See Table 42 for the model-specific default values	System voltage programming bus. The values of the system voltage can be programmed to the following values: 000 = 4.3 V. 001 = 4.4 V. 010 = 4.5 V. 011 = 4.6 V. 100 = 4.7 V. 101 = 4.8 V. 110 = 4.9 V. 111 = 5.0 V.

Table 27. Interrupt Enable Register, Register Address 0x09

Bit No.	Mnemonic	Access	Default	Description
7	Not used			
6	EN_THERM_LIM_INT	R/W	0	0 = isothermal charging interrupt is disabled. 1 = isothermal charging interrupt is enabled.
5	EN_WD_INT	R/W	0	0 = watchdog alarm interrupt is disabled. 1 = watchdog alarm interrupt is enabled.
4	EN_TSD_INT	R/W	0	0 = overtemperature interrupt is disabled. 1 = overtemperature interrupt is enabled.
3	EN_THR_INT	R/W	0	0 = THR temperature thresholds interrupt is disabled. 1 = THR temperature thresholds interrupt is enabled.
2	EN_BAT_INT	R/W	0	0 = battery voltage thresholds interrupt is disabled. 1 = battery voltage thresholds interrupt is enabled.
1	EN_CHG_INT	R/W	0	0 = charger mode change interrupt is disabled. 1 = charger mode change interrupt is enabled.
0	EN_VIN_INT	R/W	0	0 = VINx pin voltage thresholds interrupt is disabled. 1 = VINx pin voltage thresholds interrupt is enabled.

Table 28. Interrupt Active Register, Register Address 0x0A

Bit No.	Mnemonic	Access	Default	Description
7	Not used			
6	THERM_LIM_INT	R	0	1 = indicates an interrupt caused by isothermal charging.
5	WD_INT	R	0	1 = indicates an interrupt caused by the watchdog alarm. The watchdog timer expires within 2 sec or 4 sec, depending on the watch dog period setting of 32 sec or 64 sec, respectively.
4	TSD_INT	R	0	1 = indicates an interrupt caused by an overtemperature fault.
3	THR_INT	R	0	1 = indicates an interrupt caused by THR temperature thresholds.
2	BAT_INT	R	0	1 = indicates an interrupt caused by battery voltage thresholds.
1	CHG_INT	R	0	1 = indicates an interrupt caused by a charger mode change.
0	VIN_INT	R	0	1 = indicates an interrupt caused by V_{IN} voltage thresholds.

Table 29. Charger Status Register 1, Register Address 0x0B

Bit No.	Mnemonic	Access	Default	Description
7	VIN_OV	R	N/A	1 = indicates that the voltage at the VINx pins exceeds V_{VIN_OV}.
6	VIN_OK	R	N/A	1 = indicates that the voltage at the VINx pins exceeds V_{VIN_OK}.
5	VIN_ILIM	R	N/A	1 = indicates that the current into a VINx pin is limited by the high voltage blocking FET and the charger is not running at the full programmed I_{CHG}.
4	THERM_LIM	R	N/A	1 = indicates that the charger is not running at the full programmed I_{CHG} but is limited by the die temperature.
3	CHDONE	R	N/A	1 = indicates the end of charge cycle has been reached. This bit latches on, in that it does not reset to low when the V_{RCH} threshold is breached.
[2:0]	CHARGER_STATUS[2:0]	R	N/A	Charger status bus. 000 = off. 001 = trickle charge. 010 = fast charge (CC mode). 011 = fast charge (CV mode). 100 = charge complete. 101 = LDO mode. 110 = trickle or fast charge timer expired. 111 = battery detection.

Table 30. Charger Status Register 2, Register Address 0x0C

Bit No.	Mnemonic	Access	Default	Description
[7:5]	THR_STATUS[2:0]	R	N/A	THR pin status. 000 = off. 001 = battery cold. 010 = battery cool. 011 = battery warm. 100 = battery hot. 111 = thermistor OK.
4	Not used	R	N/A	
3	RCH_LIM_INFO	R	N/A	The recharge limit information function is activated when DIS_RCH is logic high and the CHARGER_STATUS[2:0] = 100 (binary). The status bit informs the system that a recharge cycle is required. 0 = $V_{BAT\_SNS} > V_{RCH}$. 1 = $V_{BAT\_SNS} < V_{RCH}$.
2:0	BATTERY_STATUS[2:0]	R		Battery status bus. 000 = battery monitor off. 001 = no battery. 010 = $V_{BAT\_SNS} < V_{TRK}$. 011 = $V_{TRK} \leq V_{BAT\_SNS} < V_{WEAK}$. 100 = $V_{BAT\_SNS} \geq V_{WEAK}$.

Table 31. Fault Register[1], Register Address 0x0D

Bit No.	Mnemonic	Access	Default	Description
[7:4]	Not used			
3	BAT_SHR	R/W	0	1 = indicates detection of a battery short.
2	Not used	R/W		
1	TSD 130°C	R/W	0	1 = indicates an overtemperature (lower) fault.
0	TSD 140°C	R/W	0	1 = indicates an overtemperature fault.

[1] To reset the fault bits in the fault register, cycle power on VINx or write high to the corresponding I^2C bit.

Table 32. Battery Short, Register Address 0x10

Bit No.	Mnemonic	Access	Default	Description
[7:5]	TBAT_SHR[2:0]	R/W	100 = 30 sec	Battery short timeout timer. 000 = 1 sec. 001 = 2 sec. 010 = 4 sec. 011 = 10 sec. 100 = 30 sec. 101 = 60 sec. 110 = 120 sec. 111 = 180 sec.
[4:3]	Not used	R/W		
[2:0]	VBAT_SHR[2:0]	R/W	100 = 2.4 V	Battery short voltage threshold level. 000 = 2.0 V. 001 = 2.1 V. 010 = 2.2 V. 011 = 2.3 V. 100 = 2.4 V. 101 = 2.5 V. 110 = 2.6 V. 111 = 2.7 V.

Table 33. IEND Register, Register Address 0x11

Bit No.	Mnemonic	Access	Default	Description
[7:5]	IEND[2:0]	R/W	See Table 40 for the model-specific default values.	Termination current programming bus. The values of the termination current can be programmed to the following values: 000 = 12.5 mA. 001 = 32.5 mA. 010 = 52.5 mA. 011 = 72.5 mA. 100 = 92.5 mA. 101 = 117.5 mA. 110 = 142.5 mA. 111 = 170.0 mA.
4	C/20 EOC	R/W	0	The C/20 EOC bit has priority over the other settings (C/10 EOC, C/5 EOC, and IEND). 1 = the termination current is ICHG/20 with the following limitations: Minimum value = 12.5 mA. Maximum value = 170 mA.
3	C/10 EOC	R/W	0	The C/10 EOC bit has priority over the other termination current settings (IEND), but does not have priority over the C/20 EOC setting. 1 = the termination current is ICHG/10 unless C/20 EOC is high. The termination current is limited to the following values: Minimum value = 12.5 mA. Maximum value = 170 mA.
2	C/5 EOC	R/W	0	The C/5 bit has priority over the other termination current settings (IEND), but does not have priority over the C/20 EOC setting or the C/10 EOC setting. 1 = the termination current is ICHG / 5 unless the C/20 or the C/10 EOC is high. The termination current is limited to the following values: Minimum value = 12.5 mA. Maximum value = 170 mA.
1:0	SYS_EN_SET[1:0]	R/W	00	Selects the operation of the system enable pin (SYS_EN). 00 = SYS_EN is activated when LDO is active and the system voltage is available. 01 = SYS_EN activated by ISO_Bx voltage, the battery charging mode. 10 = SYS_EN is activated and the isolation FET is disabled when the battery drops below V_{WEAK}.[1] 11 = SYS_EN is active in LDO mode when the charger is disabled. SYS_EN is active in the charging mode when $V_{ISO\_B} \geq V_{WEAK}$.

[1] This option is active when VINx = 0 V and the battery monitor is activated from Register 0x07, Bit D5 (EN_BMON).

APPLICATIONS INFORMATION

EXTERNAL COMPONENTS

ISO_Sx (V_{OUT}) Capacitor Selection

To obtain stable operation of the ADP5061 in a safe way, the combined effective capacitance of the ISO_Sx capacitor and the system capacitance must not be less than 20 µF and must not exceed 100 µF at any point during operation.

When choosing the capacitor value, it is also important to account for the loss of capacitance due to the output voltage dc bias. Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric that is adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or higher are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

The worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage is calculated using the following equation:

$$C_{EFF} = C_{OUT} \times (1 - TEMPCO) \times (1 - TOL)$$

where:
C_{EFF} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over the −40°C to +85°C temperature range is assumed to be 15% for an X7R dielectric. The tolerance of the capacitor (TOL) is assumed to be 20%, and C_{OUT} is 30.4 µF at 5.0 V, as shown in Figure 38.

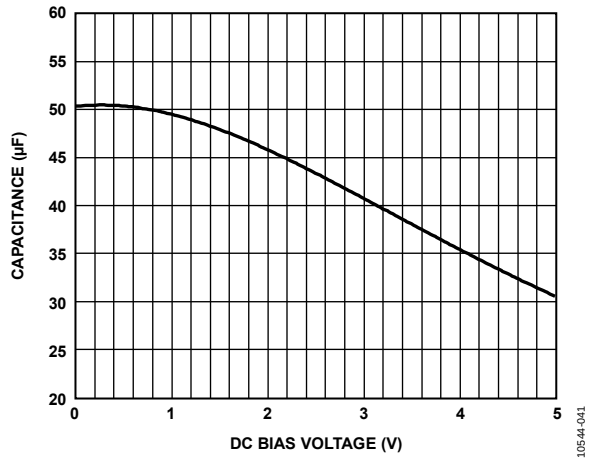

Figure 38. Murata GRM32ER61A476ME20C Capacitance vs. Bias Voltage

Substituting these values in the equation yields

$$C_{EFF} = 34.3\ \mu F \times (1 - 0.15) \times (1 - 0.2) \approx 20.7\ \mu F$$

To guarantee the performance of the charger in various operation modes including trickle charge, constant current charge, and constant voltage charge, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

Splitting ISO_Sx Capacitance

In many applications, the total ISO_Sx capacitance consists of a number of capacitors. The system voltage node (ISO_Sx) usually supplies a single regulator or a number of ICs and regulators, each of which requires a capacitor close to its power supply input (see Figure 39).

The capacitance close to the ADP5061 ISO_Sx output should be at least 10 µF, as long as the total effective capacitance is at least 20 µF at any point during operation.

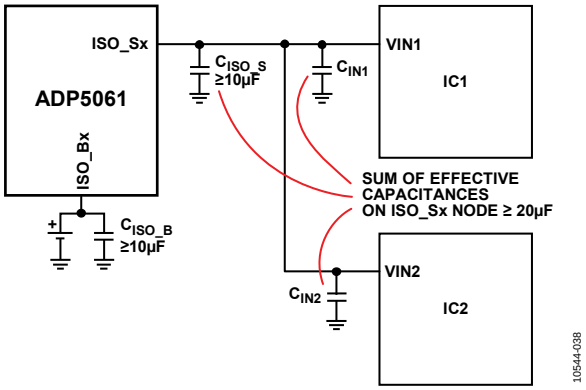

Figure 39. Splitting ISO_Sx Capacitance

ISO_Bx Capacitor Selection

The ISO_Bx effective capacitance (including temperature and dc bias effects) must not be less than 10 µF at any point during operation. Typically, a nominal capacitance of 22 µF is required to fulfill the condition at all points of operation. Suggestions for an ISO_Bx capacitor are listed in Table 35.

CBP Capacitor Selection

The internal supply voltage of the ADP5061 is equipped with a noise suppressing capacitor at the CBP terminal. Do not allow CBP capacitance to exceed 14 nF at any point during operation. Do not connect any external voltage source, any resistive load, or any other current load to the CBP terminal. Suggestions for a CBP capacitor are listed in Table 36.

VINx Capacitor Selection

According to the USB 2.0 specification, USB peripherals have a detectable change in capacitance on VBUS when they are attached to a USB port. The peripheral device VBUS bypass capacitance must be at least 1 µF but not larger than 10 µF.

The VINx input of the ADP5061 is tolerant of voltages as high as 20 V; however, if an application requires exposing the VINx input to voltages of up to 20 V, the voltage range of the capacitor must also be above 20 V. Suggestions for a VINx capacitor are given in Table 37.

When using ceramic capacitors, a higher voltage range is usually achieved by selecting a component with larger physical dimensions. In applications where lower than 20 V at VINx input voltages can be guaranteed, smaller output capacitors can be used accordingly.

Table 34. ISO_Sx Capacitor Suggestions

Vendor	Part Number	Value	Voltage	Size
Murata	GRM32ER61A476ME20	47 µF	10 V	1210
TDK	C3225X5R1A476M	47 µF	10 V	1210

Table 35. ISO_Bx Capacitor Suggestions

Vendor	Part Number	Value	Voltage	Size
Murata	GRM31CR61A226KE19	22 µF	10 V	1206
Murata	GRM31CR60J226ME19	22 µF	6.3 V	1206
TDK	C3216X5R0J226M	22 µF	6.3 V	1206
Taiyo-Yuden	JMK316ABJ226KL	22 µF	6.3 V	1206

Table 36. CBP Capacitor Suggestions

Vendor	Part Number	Value	Voltage	Size
Murata	GRM15XR71C103KA86	10 nF	16 V	0402
TDK	C1005X7R1C103K	10 nF	16 V	0402

Table 37. VINx Capacitor Suggestions

Vendor	Part Number	Value	Voltage	Size
Murata	GRM21BR61E106MA73	10 µF	25 V	0805
TDK	C2012X5R1E106K	10 µF	25 V	0805

PCB LAYOUT GUIDELINES

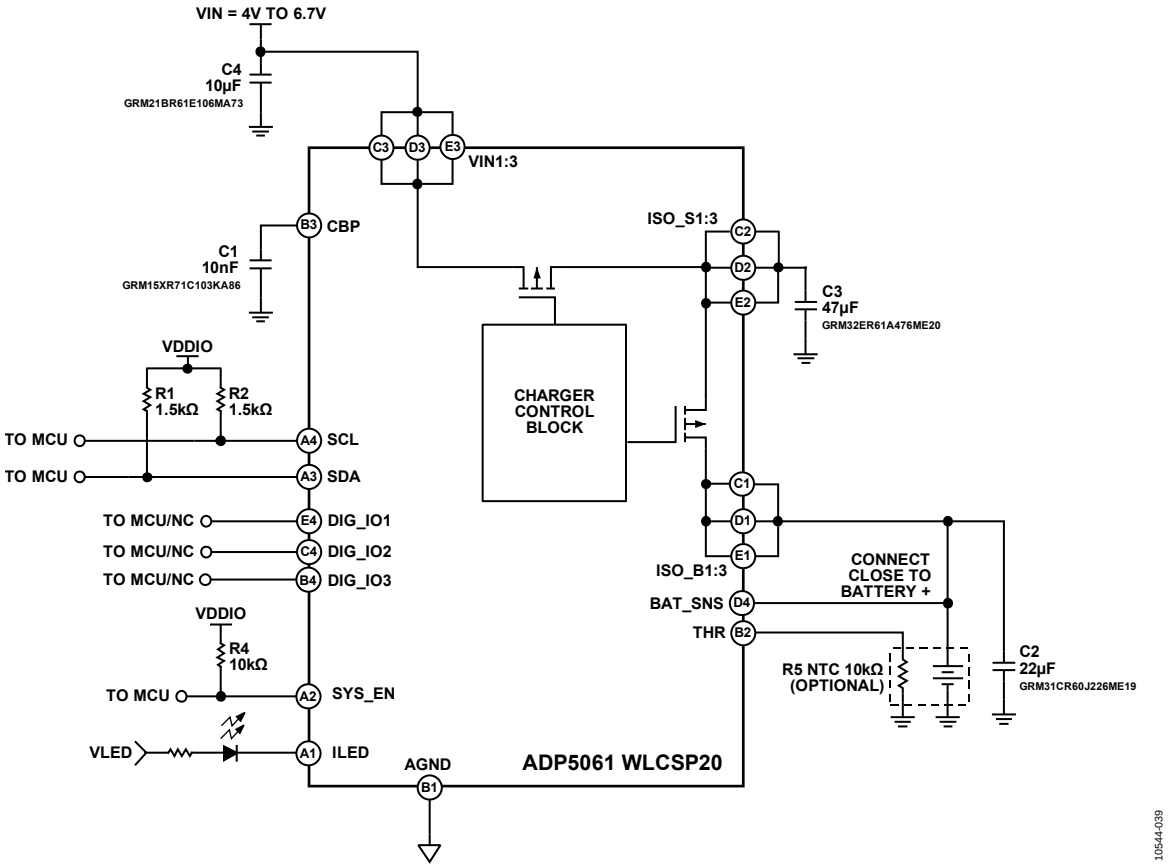

Figure 40. Reference Circuit Diagram

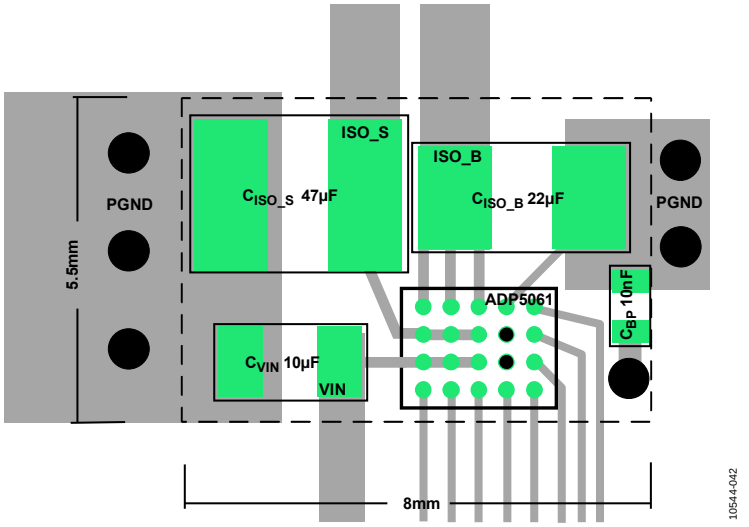

Figure 41. Reference PCB Floor Plan

POWER DISSIPATION AND THERMAL CONSIDERATIONS

CHARGER POWER DISSIPATION

When the ADP5061 charger operates at high ambient temperatures and at maximum current charging and loading conditions, the junction temperature can reach the maximum allowable operating limit of 125°C.

When the junction temperature exceeds 140°C, the ADP5061 turns off, allowing the device to cool down. When the die temperature falls below 110°C and the TSD 140°C fault bit in Register 0x0D is cleared by an I^2C write, the ADP5061 resumes normal operation.

This section provides guidelines to calculate the power dissipated in the device to ensure that the ADP5061 operates below the maximum allowable junction temperature.

To determine the available output current in different operating modes under various operating conditions, the user can reference the following equations:

$$P_D = P_{LDOFET} + P_{ISOFET} \quad (1)$$

where:
P_{LDOFET} is the power dissipated in the input LDO FET.
P_{ISOFET} is the power dissipated in the battery isolation FET.
Calculate the power dissipation in the LDO FET and the battery isolation FET using Equation 2 and Equation 3.

$$P_{LDOFET} = (V_{IN} - V_{ISO\_S}) \times (I_{CHG} + I_{LOAD}) \quad (2)$$

$$P_{ISOFET} = (V_{ISO\_S} - V_{ISO\_B}) \times I_{CHG} \quad (3)$$

where:
V_{IN} is the input voltage at the VINx pins.
V_{ISO_S} is the system voltage at the ISO_Sx pins.
V_{ISO_B} is the battery voltage at the ISO_Bx pins.
I_{CHG} is the battery charge current.
I_{LOAD} is the system load current from the ISO_Sx pins.

LDO Mode

The system regulation voltage is user programmable from 4.3 V to 5.0 V. In LDO mode (charging disabled, EN_CHG = low), calculation of the total power dissipation is simplified, assuming that all current is drawn from the VINx pins and the battery is not shared with ISO_Sx.

$$P_D = (V_{IN} - V_{ISO\_S}) \times I_{LOAD}$$

Charging Mode

In charging mode, the voltage at the ISO_Sx pins depends on the battery level. When the battery voltage is lower than V_{ISO_SFC} (typically 3.8 V), the voltage drop over the battery isolation FET is higher and the power dissipation must be calculated using Equation 3. When the battery voltage level reaches V_{ISO_SFC}, the power dissipation can be calculated using Equation 4.

$$P_{ISOFET} = R_{DSON\_ISO} \times I_{CHG} \quad (4)$$

where:
R_{DSON_ISO} is the on resistance of the battery isolation FET (typically 110 mΩ during charging).

The thermal control loop of the ADP5061 automatically limits the charge current to maintain a die temperature below T_{LIM} (typically 115°C).

The most intuitive and practical way to calculate the power dissipation in the ADP5061 device is to measure the power dissipated at the input and all of the outputs. Perform the measurements at the worst-case conditions (voltages, currents, and temperature). The difference between input and output power is the power that is dissipated in the device.

JUNCTION TEMPERATURE

In cases where the board temperature, T_A, is known, the thermal resistance parameter, θ_{JA}, can be used to estimate the junction temperature rise. T_J is calculated from T_A and P_D using the formula

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (5)$$

The typical θ_{JA} value for the 20-bump WLCSP is 46.8°C/W (see Table 5). A very important factor to consider is that θ_{JA} is based on a 4-layer, 4 in × 3 in, 2.5 oz. copper board as per JEDEC standard, and real applications may use different sizes and layers. It is important to maximize the copper to remove the heat from the device. Copper exposed to air dissipates heat better than copper used in the inner layers.

If the case temperature can be measured, the junction temperature is calculated by

$$T_J = T_C + (P_D \times \theta_{JC}) \quad (6)$$

where T_C is the case temperature and θ_{JC} is the junction-to-case thermal resistance provided in Table 5.

For a WLCSP device, where possible, remove heat from every current carrying bump (VINx, ISO_Sx, and ISO_Bx). For example, thermal vias to the board power planes can be placed close to these pins, where available.

The reliable operation of the charger can be achieved only if the estimated die junction temperature of the ADP5061 (Equation 5) is less than 125°C. Reliability and mean time between failures (MTBF) are greatly affected by increasing the junction temperature. Additional information about product reliability can be found in the *ADI Reliability Handbook* located at the following URL: www.analog.com/reliability_handbook.

FACTORY PROGRAMMABLE OPTIONS

CHARGER OPTIONS

Table 38 to Table 50 list the factory programmable options of the ADP5061. In each of these tables, the selection column represents the default setting of the ADP5061ACBZ-2-R7, ADP5061ACBZ-4-R7, and ADP5061ACBZ-5-R7 models. The difference between these two models are shown in Table 39, Table 40, Table 42, and Table 50. All other default settings are the same for each model.

Table 38. Default Termination Voltage

Option	Selection
000 = 4.20 V	000 = 4.20 V
010 = 3.70 V	
011 = 3.80 V	
100 = 3.90 V	
101 = 4.00 V	
110 = 4.10 V	
111 = 4.40 V	

Table 39. Default Fast Charge Current

Option	Selection/Model
000 = 500 mA	
001 = 300 mA	001 = 300 mA/ADP5061ACBZ-5-R7
010 = 550 mA	
011 = 600 mA	
100 = 750 mA	100 = 750 mA/ ADP5061ACBZ-2-R7, ADP5061ACBZ-4-R7
101 = 900 mA	
110 = 1300 mA	
111 = 1300 mA	

Table 40. Default End of Charge Current

Option	Selection/Model
000 = 52.5 mA	000 = 52.5 mA/ ADP5061ACBZ-2-R7, ADP5061ACBZ-4-R77
001 = 72.5 mA	
010 = 12.5 mA	010 = 12.5 mA/ADP5061ACBZ-5-R7
011 = 32.5 mA	
100 = 142.5 mA	
101 = 167.5 mA	
110 = 92.5 mA	
111 = 117.5 mA	

Table 41. Default Trickle to Fast Charge Threshold

Option	Selection
00 = 2.5 V	00 = 2.5 V
01 = 2.0 V	
10 = 2.9 V	
11 = 2.6 V	

Table 42. Default System Voltage

Option	Selection/Model
000 = 4.3 V	000 = 4.3 V/ADP5061ACBZ-4-R7
001 = 4.4 V	
010 = 4.5 V	010 = 4.5 V/ADP5061ACBZ-5-R7
011 = 4.6 V	
100 = 4.7 V	
101 = 4.8 V	
110 = 4.9 V	
111 = 5.0 V	111 = 5.0 V/ADP5061ACBZ-2-R7

Table 43. Thermistor Resistance

Option	Selection
0 = 10 kΩ	0 = 10 kΩ
1 = 100 kΩ	

Table 44. Thermistor Beta Value

Option	Selection
0100 = 3150	0100 = 3150
0101 = 3350	
0110 = 3500	
0111 = 3650	
1000 = 3850	
1001 = 4000	
1010 = 4200	
1011 = 4400	

Table 45. DIS_IC1 Mode Select

Option	Selection
0 = DIC_IC1 mode select, VINx current = 280 µA, ISO_B can float, no leak to ISO_Bx	0
1 = DIC_IC1 mode select, VINx current = 110 µA, supply switch leaks from VINx to ISO_Bx	

Table 46. Trickle or Fast Charge Timer Fault Operation

Option	Selection
0 = after timeout LDO off, charging off	
1 = after timeout LDO mode active, charging off	1 = LDO mode active

I²C REGISTER DEFAULTS

Table 47. I²C Register Default Settings

Bit Name	I²C Register Address, Bit Location	Option	Selection
CHG_VLIM	Address 0x03, Bits[D1:D0]	0 = limit 3.2 V, 1 = limit 3.7 V	0 = limit 3.2 V
DIS_RCH	Address 0x05, Bit D7	0 = recharge enabled, 1 = recharge disabled	0 = recharge enabled
EN_WD	Address 0x06, Bit D2	0 = watchdog disabled, 1 = watchdog enabled	0 = disabled
DIS_IC1	Address 0x07, Bit D6	0 = not activated, 1 = activated	0 = not activated
EN_CHG	Address 0x07, Bit D0	0 = charging disabled, 1 = charging enabled	0 = charging disabled
EN_JEITA	Address 0x08, Bit D7	0 = JEITA disabled, 1 = JEITA enabled	0 = JEITA disabled
JEITA_SELECT	Address 0x08, Bit D6	0 = JEITA1 charging, 1= JEITA2 charging	0 = JEITA1 charging
EN_CHG_VLIM	Address 0x08, Bit D5	0 = limit disabled, 1 = limit enabled	0 = limit disabled
IDEAL_DIODE[1:0]	Address 0x08, Bits[D4:D3]	00 = ideal diode operates when $V_{ISO\_S} < V_{ISO\_B}$ 01 = ideal diode operates when $V_{ISO\_S} < V_{ISO\_B}$ and $V_{BAT\_SNS} > V_{WEAK}$ 10 = ideal diode is disabled 11 = ideal diode is disabled	00

DIGITAL INPUT AND OUTPUT OPTIONS

Table 48. I²C Address 0x11, Bits[D1:D0] SYS_EN Output Default

Option	Selection
00 = SYS_EN is activated when LDO is active and system voltage is available	00
01 = SYS_EN is activated by ISO_Bx voltage; battery charging mode	
10 = SYS_EN is activated and isolation FET is disabled when battery drops below VWEAK[1]	
11 = SYS_EN is active in LDO mode when charger is disabled. SYS_EN is active in charging mode when VISO_B ≥ VWEAK	

[1] This option is active when VINx = 0 V and battery monitor is activated from Register 0x07, Bit D5 (EN_BMON).

DIG_IO1, DIG_IO2, and DIG_IO3 Options

Table 49. DIG_IO1 Polarity

Option	Selection
0 = DIG_IO1 polarity, high active operation 1 = DIG_IO1 polarity, low active operation	0 = high active

Table 50. DIG_IOx Options

Option	DIG_IO1 Function	DIG_IO2 Function	DIG_IO3 Function	Selection / Model
0000	I_{VINx} limit Low = 100 mA High = 500 mA	Disable IC1 Low = not activated High = activated	Charging disable/enable Low = charging disable High = charging enabled	0000 ADP5061ACBZ-2-R7 ADP5061ACBZ-4-R7
0010	I_{VINx} limit Low = 100 mA High= 500 mA	I_{VINx} limit Not applicable High = I_{VINx} limit 1500 mA	Disable IC1 Low = not activated High = activated	
0011	I_{VINx} limit Low = 100 mA High= 500 mA	I_{VINx} limit Not applicable High = I_{VINx} limit 1500 mA	Fast charge current Low = ICHG[4:0] High = ICHG[4:0] ÷ 2	
0100	I_{VINx} limit Low = 100 mA High= 500 mA	I_{VINx} limit Not applicable High = I_{VIN} limit 1500 mA	LDO Low = LDO active High = LDO disabled	
0101	I_{VINx} limit Low = 100 mA High= 500 mA	I_{VINx} limit Not applicable High = I_{VINx} limit 1500 mA	Charging Low = charging disabled High = charging enabled	
0110	I_{VINx} limit Low = 100 mA High= 500 mA	Recharge Not applicable High = disable recharge	Charging Low = charging disabled High = charging enabled	
0111	Charging Low = charging disabled High = charging enabled	Disable IC1 Low = not activated High = activated	Recharge Not applicable High = disable recharge	
1000	I_{VINx} limit Low = 100 mA High= 500 mA	I_{VINx} limit Not applicable High = I_{VINx} limit 1500 mA	Interrupt output Not applicable Not applicable	
1001	I_{VINx} limit Low = 100 mA High= 500 mA	Charging Low = charging disabled High = charging enabled	Interrupt output Not applicable Not applicable	1001 ADP5061ACBZ-5-R7
1010	I_{VINx} limit Low = 100 mA High= 500 mA	Disable IC1 Low = not activated High = activated	Interrupt output Not applicable Not applicable	
1011	I_{VINx} limit Low = 100 mA High= 500 mA	Recharge Not applicable High = disable recharge	Interrupt output Not applicable Not applicable	
1100	I_{VINx} limit Low = 100 mA High= 500 mA	Fast charge current Low = ICHG High = ICHG[4:0] ÷ 2	Interrupt output Not applicable Not applicable	
1101	I_{VINx} limit Low = 100 mA High= 500 mA	LDO Low = LDO active High = LDO disabled	Interrupt output Not applicable Not applicable	
1110	I_{VINx} limit Not applicable High = I_{VINx} limit 1500 mA	Charging Low = charging disabled High = charging enabled	Interrupt output Not applicable Not applicable	
1111	Disable IC1 Low = not activated High = activated	Charging Low = charging disabled High = charging enabled	Interrupt output Not applicable Not applicable	

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

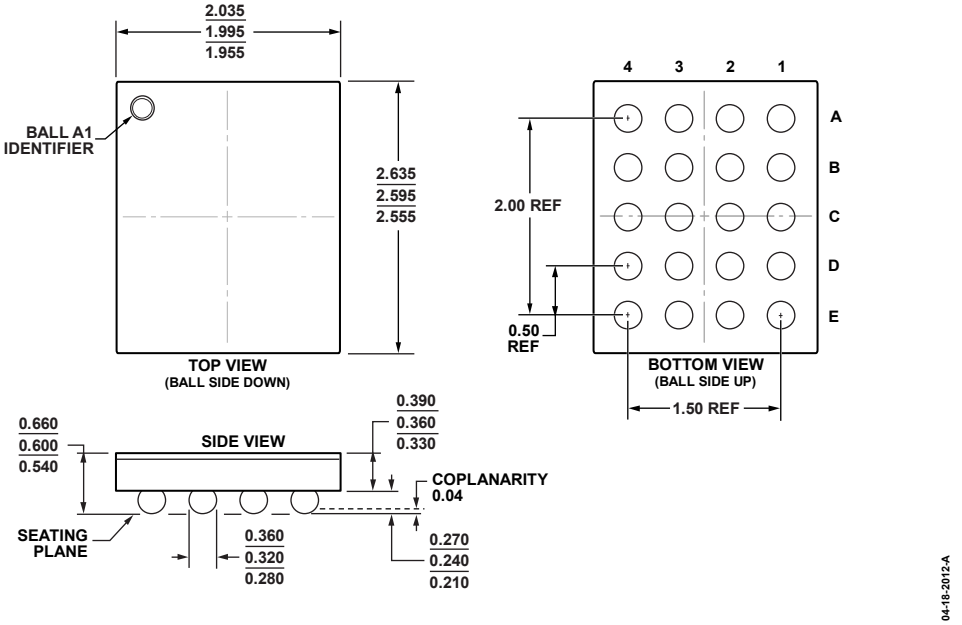

Figure 42. 20-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-20-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADP5061ACBZ-2-R7	–40°C to +125°C	20-Ball WLCSP	CB-20-9
ADP5061ACBZ-4-R7	–40°C to +125°C	20-Ball WLCSP	CB-20-9
ADP5061ACBZ-5-R7	–40°C to +125°C	20-Ball WLCSP	CB-20-9
ADP5061CB-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] For additional factory programmable options, contact a local Analog Devices, Inc., sales or distribution representative.

NOTES

NOTES

D10544-0-10/19(D)

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