Advanced Battery Management PMIC with Ultra Low Power Buck and Buck Boost

Data Sheet **ADP5360**

FEATURES

- **Linear battery charger**
  - **High accuracy and programmable charge terminal voltage and charge current up to 320 mA**
  - **Compliant with JEITA charge temperature specification**
- **Li-Ion and Li-Poly battery monitor and protection**
  - **Voltage-based fuel gauge with adaptive filter limitation**
  - **Independent battery protection of overcharge and overdischarge**
  - **Temperature sensor with external NTC**
- **Ultralow quiescent current buck converter**
  - **Quick output discharge option**
- **Ultralow quiescent current buck boost converter**
  - **Quick output discharge option**
- **Supervisory with manual reset ($\overline{MR}$) and watchdog timer**
- **Shipment mode extends battery life**
- **Full I²C programmability with dedicated interrupt pin**

APPLICATIONS

Rechargeable Li-Ion/Li-Poly battery-powered devices
Portable consumer devices
Portable medical devices
Wearable devices

GENERAL DESCRIPTION

The ADP5360 combines one high performance linear charger for a single lithium-ion (Li-Ion)/lithium-polymer (Li-Poly) battery with a programmable, ultralow quiescent current fuel gauge and battery protection circuit, one ultralow quiescent buck, one buck boost switching regulator, and a supervisory circuit that can monitor output voltage.

The ADP5360 charger operates at up to 6.8 V to prevent USB bus spiking during disconnect or connect scenarios.

The ADP5360 features an internal isolation field effect transistor (FET) between the linear charger output and the battery node. The full battery protection features are activated when the device is in the battery overcharge and overdischarge fault conditions.

The ADP5360 fuel gauge uses a voltage-based algorithm with an adaptive filter limitation solution. The fuel gauge reports real-time battery state of charge (SOC) for the rechargeable Li-Ion battery with ultralow quiescent current.

The ADP5360 buck regulator operates at 1.0 MHz switching frequency in forced pulse-width modulation (FPWM) mode. In hysteresis mode, the regulator achieves excellent efficiency at a low output power.

The ADP5360 buck boost regulator only operates in hysteresis mode and outputs a voltage less than or greater than the battery voltage.

The ADP5360 supervisory circuits monitor the regulator output voltage and provide a power-on reset signal to the system. A watchdog timer and an external pushbutton can reset the microprocessor.

The I²C-compatible interface enables the programmability of all battery charging parameters, the protection threshold, the buck output voltage, and the status bit readback.

The ADP5360 operates over the −40°C to +85°C junction temperature range and is available in a 32-ball, 2.56 mm × 2.56 mm wafer level chip scale package (WLCSP).

Rev. 0 Document Feedback

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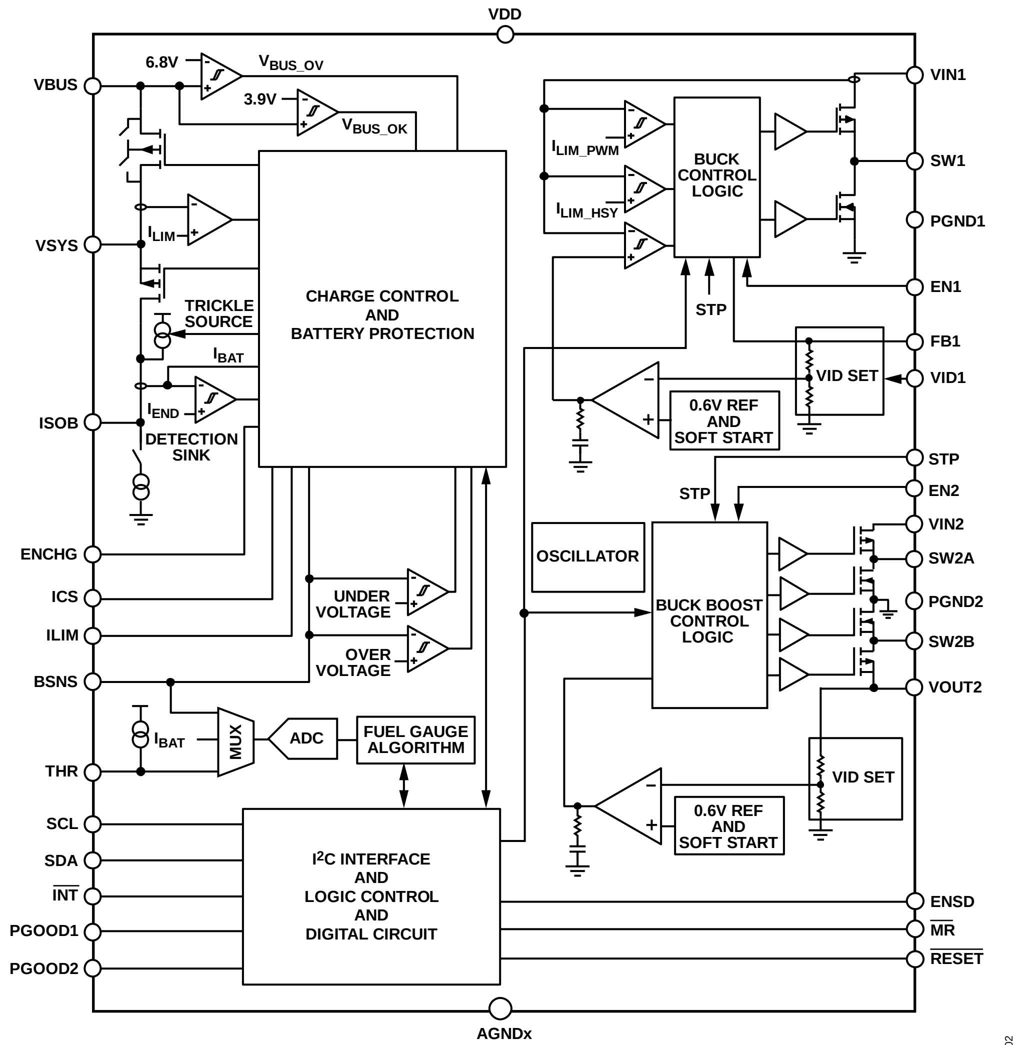
REVISION HISTORY

11/2019—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. I_{BAT} IS THE BATTERY SENSE CURRENT.

Figure 1.

SPECIFICATIONS

BATTERY CHARGER SPECIFICATIONS

T_J = −40°C to +85°C, voltage of the VBUS pin (V_{VBUS}) = 5.0 V, voltage of the ISOB pin (V_{ISOB}) = 3.8 V, C1 = 2.2 µF, C2 = 1 µF, C3 = C4 = 10 µF (see Figure 60), and all registers are at default values, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
GENERAL PARAMETERS						
Undervoltage Lockout (UVLO)	V_{UVLO}	Rising threshold, voltage of the ISOB pin, V_{VBUS} = 0 V		2.1	2.15	V
		Falling threshold, voltage of the ISOB pin, V_{VBUS} = 0 V	1.8	1.88		V
Input Current Limit	I_{LIM}	I_{LIM} = 100 mA		95	100	mA
Operation Current						
VBUS Consumption	I_{Q_BUS}	Charger, fuel gauge, buck, and buck boost enabled, no charge current		1.5	2	mA
Battery Consumption	I_{Q_PRO}	Enable battery protection only, V_{VBUS} = 0 V		0.25	1.8	µA
	$I_{Q\_FG\_ACT}$	Fuel gauge, active mode, V_{VBUS} = 0 V		3.5	5	µA
	$I_{Q\_FG\_SLEEP}$	Fuel gauge, sleep mode, V_{VBUS} = 0 V		0.2	0.85	µA
	I_{Q_REG}	Enable buck and buck boost, V_{VBUS} = 0 V		0.34	1	µA
	I_{Q_DISALL}	All disabled, V_{VBUS} = 0 V		150	450	nA
	I_{Q_SHIP}	Shipment mode, T_J = 25°C		10	50	nA
		Shipment mode, T_J = −40°C to +85°C			310	nA
CHARGING PARAMETERS						
Fast Charge Constant Current						
Mode	I_{CHG}	I_{CHG} = 100 mA	94	100	106	mA
Accuracy[1]		I_{CHG} = 10 mA to 320 mA, T_J = 0°C to 85°C	−15		+15	%
Charge Current						
Trickle[1]	I_{TRK_DEAD}	I_{TRK_DEAD} = 5 mA, T_J = 0°C to 85°C	4	5	6	mA
Weak	I_{CHG_WEAK}			I_{TRK_DEAD} + I_{CHG}		mA
Trickle to Weak Charge Threshold[1]	V_{TRK_DEAD}	V_{TRK_DEAD} = 2.5 V	2.41	2.5	2.57	V
Hysteresis	ΔV_{TRK_DEAD}			100		mV
Weak to Fast Charge Threshold[1]	V_{WEAK}	V_{WEAK} = 3.0 V	2.88	3.0	3.08	V
Hysteresis	ΔV_{WEAK}			100		mV
Battery Termination Voltage	V_{TRM}					
Termination Voltage Accuracy[1]		V_{TRM} = 4.2 V on the BSNS pin, T_J = 25°C	4.18	4.200	4.22	V
		V_{TRM} = 4.2 V, on the BSNS pin, T_J = 0°C to 85°C	−1		+1	%
Charge Complete Current[1]	I_{END}	I_{END} = 5 mA, T_J = 0°C to 85°C	2	5	8	mA
Recharge Voltage Differential[1]	V_{RCH}			120		mV
BATTERY ISOLATION FET	ISOFET					
Resistance Between ISOB and VSYS	R_{DSON_ISO}	V_{VBUS} = 0 V, current of the ISOB pin (I_{ISOB}) = 100 mA		145	220	mΩ
LOW DROPOUT (LDO) AND HIGH VOLTAGE BLOCKING FET						
Regulated System Voltage[1]	V_{SYS_REG}	V_{TRM} = 4.2 V, V_{SYSTEM} = V_{TRM} + 200 mV		4.4		V
High Voltage Blocking FET On Resistance	R_{DSON_HV}	I_{VBUS} = 100 mA		550	820	mΩ
Input Operating Voltage Range		V_{VBUS}	4.1		6.8	V
Good Threshold	V_{VBUS_OK}					
Rising	$V_{VBUS\_OK\_RISE}$			3.9	4.0	V
Falling	$V_{VBUS\_OK\_FALL}$		3.5	3.6		V
Overvoltage Threshold	V_{VBUS_OV}					
Rising	$V_{VBUS\_OV\_RISE}$			6.8	7.0	V
Falling	$V_{VBUS\_OV\_FALL}$		6.4	6.6		V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
THERMAL PROTECTION						
Thermal Shutdown Temperature[2]	T_{SD}	$T_{J\ RISING}$		110		°C
		$T_{J\ FALLING}$		100		°C
THERMISTOR CONTROL						
Thermistor Current						
Negative Temperature Coefficient (NTC) Resistor (R_{NTC}) = 10 kΩ	I_{NTC_10k}		57.5	60	62	µA
R_{NTC} = 47 kΩ	I_{NTC_47k}		11.5	12	12.5	µA
R_{NTC} = 100 kΩ	I_{NTC_100k}		5.65	6	6.35	µA
BATTERY DETECTION						
Sink Current	I_{SINK}		4.1	6	7	mA
Source Current	I_{SOURCE}		2	2.5	3	mA
Battery Threshold						
Low	V_{BATL}		1.92	2	2.06	V
High	V_{BATH}		3.27	3.4	3.48	V
Timer	t_{BATOK}			333		ms
Threshold After Charging Completed	V_{NOBAT}			2		V
TIMERS						
Start Charging Delay Timer	t_{START}			300		ms
Trickle Charge Timer[1]	t_{TRK}	CHG_TMR_PERIOD = 60 minutes and 600 minutes		60		min
Fast Charge Timer[1]	t_{CHG}	CHG_TMR_PERIOD = 60 minutes and 600 minutes		600		min
Charge Complete Timer	t_{END}	Voltage of the BSNS pin (V_{BSNS}) = V_{TRM}, EN_TEND = 1 bit, register set		7.5		min
Deglitch Timer	t_{DG}	Applies to V_{TRM}, V_{RCH}, I_{END}, V_{WEAK}, V_{TRK_DEAD}, and V_{VBUS_OK}		31		ms
Safety Timer	t_{SAFE}		36	40	44	min
Reset Timeout Period	t_{RP}			200		ms
$\overline{\text{MR}}$ for Shipment Mode	t_{SH}			200		ms
Watchdog Timer[1]	t_{WD}			12.5		sec
I^2C (SCL AND SDA)						
Maximum Voltage on Digital Inputs	V_{DIN_MAX}				5.5	V
Input Voltage						
Low Level	V_{IL}	Applies to SCL, SDA			0.4	V
High Level	V_{IH}	Applies to SCL, SDA	1.2			V
Low Level Output Voltage	V_{OL}	Applies to SDA, SDA current sink (I_{SDA_SINK}) = 2 mA			0.4	V
$\overline{\text{INT}}$, $\overline{\text{RESET}}$, PGOOD1, AND PGOOD2						
Input and Output Leakage Current	I_{IO_LEAK}	Input and output voltage (V_{IO}) = 5 V		10	150	nA
Input and Output Low Voltage	V_{IO_LOW}	Input and output current (I_{IO}) = 1 mA		90	200	mV
ENCHG, EN1, EN2, STP, $\overline{\text{MR}}$, ENSD						
Input Voltage Threshold						
High	V_{IH}		1.2			V
Low	V_{IL}				0.4	V
Input Leakage Current	$I_{EN\_LEAKAGE}$				150	nA

[1] These values are programmable via I^2C. Values are given with default register values.
[2] Specification is not production tested but is supported by characterization data at initial product release.

BATTERY MONITOR SPECIFICATIONS

T_J = −40°C to +85°C, V_{ISOB} = 3.8 V, C1 = 2.2 µF, C2 = 1 µF, C3 = C4 = 10 µF, and all registers are at default values, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
BATTERY VOLTAGE SENSING						
Analog-to-Digital Converter (ADC) Reading Voltage						
Range			0		4.8	V
Resolution		Based on 12-bit ADC		1.17		mV
Accuracy		T_J = 25°C	−12.5		+12.5	mV
			−1		+1	%
Fuel Gauge UVLO Threshold		V_{BSNS}				
Rising	$V_{UVLO\_FG\_RISE}$			2.7	2.8	V
Falling	$V_{UVLO\_FG\_FALL}$		2.48	2.58		V
BATTERY OVERDISCHARGE MONITORING						
Undervoltage Threshold						
Rising	V_{BPUV_FALL}		−1.5		+1.5	%
Falling Hysteresis	$V_{BPUV\_FALL\_HYS}$	HYS_UV_DISCH = 2%		2		%
Undervoltage Deglitch Timer	t_{BPUV_DIS}	DGT_UV_DISCH = 30 ms		30		ms
Overdischarge Current						
Threshold	I_{BPOC_DIS}	OC_DISCH = 600 mA	480	600	700	mA
Deglitch Timer	t_{BPOC_DIS}	DGT_OC_DISCH = 5 ms		5		ms
Hiccup Off Time	t_{DIS_HCP}			200		ms
BATTERY OVERCHARGE MONITORING		V_{VBUS} = 5 V				
Overvoltage Threshold						
Rising	V_{BPOV_RISE}		−1.5		+1.5	%
Falling Hysteresis	$V_{BPOV\_RISE\_HYS}$	HYS_OV_CHG = 2%		2		%
Overvoltage Deglitch Timer	t_{BPOV_CHG}	DGT_OV_CHG = 0.5 sec		0.5		sec
Overcurrent Threshold	I_{BPOC}	OC_CHG = 150 mA	130	150	170	mA
Overcurrent Deglitch Timer	t_{BPOC_CHG}	DGT_OC_CHG = 10 ms		10		ms
Hiccup Off Time	t_{CHG_HCP}			200		ms

BUCK REGULATOR SPECIFICATIONS

T_J = −40°C to +85°C, voltage of the VIN1 pin (V_{VIN1}) = voltage of the VSYS pin (V_{VSYS}) = 3.8 V, buck output voltage (V_{OUT1}) = 1.2 V, C5 = C6 = 10 µF, L1 = 4.7 µH (see Figure 60), and all registers are at default values, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
UVLO THRESHOLD		V_{VIN1}				
Rising	V_{UVLO1_RISE}			2.3	2.35	V
Falling	V_{UVLO1_FALL}		2.15	2.2		V
OSCILLATOR CIRCUIT						
Switching Frequency in Pulse Width Modulation (PWM) Mode	f_{SW1}		0.85	1.0	1.15	MHz
Feedback Threshold of Frequency Fold	$V_{OSC\_FOLD\_RISE}$	V_{OUT1} = 2.5 V		1.25		V
FB1 PIN						
Output Voltage Option Range	V_{OUT1}	Factory trim or I²C, six bits	0.6		3.75	V
PWM Mode						
Fixed Voltage Identification (VID) Code Voltage Accuracy	$V_{FB1\_PWM\_FIX}$		−2		+2	%

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Hysteresis Mode						
Fixed VID Code Voltage Threshold Accuracy	$V_{FB1\_HYS\_FIX}$		−2		+2	%
Hysteresis of Voltage Threshold	$V_{FB1\_HYS\ (HYS)}$			1		%
Feedback Bias Current	I_{FB1}	V_{OUT1} = 0.6 V		50		nA
SW1 PIN						
Power FET On Resistance						
High-Side	$R_{DS\ (ON)\ H}$	Pin to pin measurement		280	380	mΩ
Low-Side	$R_{DS\ (ON)\ L}$	Pin to pin measurement		260	380	mΩ
Current Limit in PWM Mode	I_{LIM_PWM}	PWM mode	850	1000	1150	mA
Peak Current in Hysteresis Mode	I_{LIM_HYS}	Hysteresis mode, BUCK_ILIM = 200 mA	160	200	240	mA
Minimum On Time[1]	t_{MIN_ON}			60		ns
SOFT START						
Default Soft Start Time	t_{SS1}	BUCK_SS[1:0] = 1 ms		1		ms
OUTPUT DISCHARGE SWITCH ON RESISTANCE	R_{DIS1}			255		Ω

[1] Guaranteed by design.

BUCK BOOST REGULATOR SPECIFICATIONS

T_J = −40°C to +85°C, voltage of the VIN2 pin (V_{VIN2}) = V_{VSYS} = 3.8 V, voltage of the VOUT2 pin (V_{VOUT2}) = 5 V, C_7 = C_8 = 10 µF, L2 = 4.7 µH (see Figure 60), and all registers are at default values, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
UVLO THRESHOLD		V_{VIN2}				
Rising	V_{UVLO2_RISING}			2.3	2.36	V
Falling	$V_{UVLO2\_FALLING}$		2.11	2.16		V
OUTPUT VOLTAGE RANGE		Factory trim or I²C, six bits	1.8		5.5	V
Output Voltage Accuracy	V_{VOUT2}		−2		+2	%
Hysteresis of Voltage Threshold Accuracy	V_{VOUT2_HYS}			1		%
SW2A AND SW2B PINS						
SWA2 Pin FET Resistance						
High-Side	$R_{DS(ON)1\_2A\text{-}H}$			354	470	mΩ
Low-Side	$R_{DS(ON)1\_2A\text{-}L}$			250	360	mΩ
SW2B Pin FET Resistance						
High-Side	$R_{DS(ON)1\_2B\text{-}H}$			290	400	mΩ
Low-Side	$R_{DS(ON)1\_2B\text{-}L}$			230	330	mΩ
Peak Current-Limit Threshold	$I_{TH(ILIM1\_2)}$	BUCKBST_ILIM = 200 mA	160	200	240	mA
SOFT START TIME						
Soft Start Time	t_{SS2}	BUCKBST_SS[0:1] = 1 ms		1		ms
Programmable Soft Start Range			1		512	ms
OUTPUT DISCHARGE SWITCH ON RESISTANCE	R_{DIS2}			255		Ω

I²C-COMPATIBLE INTERFACE TIMING SPECIFICATIONS

T_A = 25°C and V_{ISOB} = 3.8 V, unless otherwise noted.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit
I²C-COMPATIBLE INTERFACE					
Capacitive Load, Each Bus Line	C_S			400	pF
SCL Clock Frequency	f_{SCL}			400	kHz
SCL High Time	t_{HIGH}	0.6			µs
SCL Low Time	t_{LOW}	1.3			µs
Data Setup Time	t_{SUDAT}	100			ns
Data Hold Time[1]	t_{HDDAT}	0		0.9	µs
Setup Time for Repeated Start	t_{SUSTA}	0.6			µs
Hold Time for Start and Repeated Start	t_{HDSTA}	0.6			µs
Bus Free Time Between a Stop Condition and a Start Condition	t_{BUF}	1.3			µs
Setup Time for Stop Condition	t_{SUSTO}	0.6			µs
Rise Time of SCL and SDA	t_R	20		300	ns
Fall Time of SCL and SDA	t_F	20		300	ns
Pulse Width of Suppressed Spike	t_{SP}	0		50	ns

[1] A master device must provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL. See Figure 2 for more information.

Timing Diagram

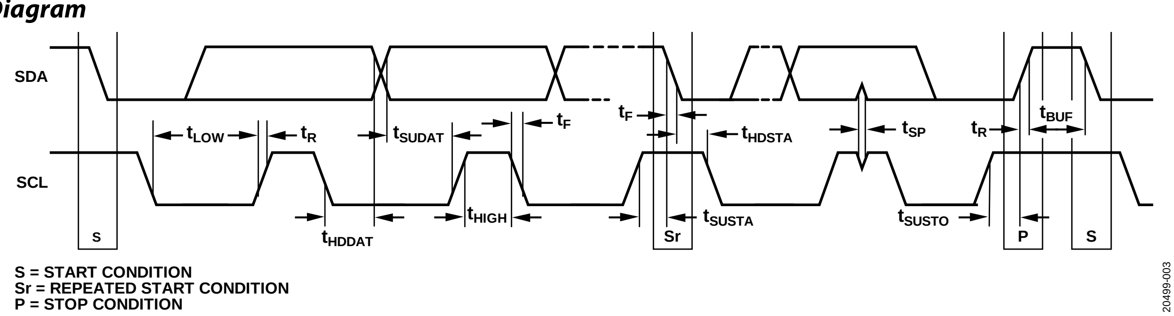


Figure 2. I²C Timing Diagram

RECOMMENDED INPUT AND OUTPUT CAPACITANCE AND INDUCTANCE

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CAPACITANCE	Effective capacitance				
VBUS Capacitance		1.0	2.2		µF
VDD Pin Capacitance		0.47	1.0	10	µF
Total Capacitance					
VSYS Pin		4.7	10		µF
ISOB Pin		4.7	10		µF
VIN1 Pin		2.2	10		µF
VIN2 Pin		2.2	10		µF
VOUT1 Node		1	10		µF
VOUT2 Pin		1	10		µF
INDUCTANCE					
Buck		2.2	4.7	6.8	µH
Buck Boost		2.2	4.7	6.8	µH

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
VBUS to PGND1	−0.5 V to +20 V
PGND1, PGND2 to AGNDx	−0.3 V to +0.3 V
All Other Pins to AGNDx	−0.3 V to +6 V
Continuous Drain Current, Battery Supplementary Mode from ISOB to VSYS, T_J = 85°C	1.1 A
Temperature Range	
Storage	−65°C to +150°C
Operating Junction	−40°C to +85°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient, thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CB-32-2	50	0.35	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADP5360 package is limited by the associated rise in T_J on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADP5360.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

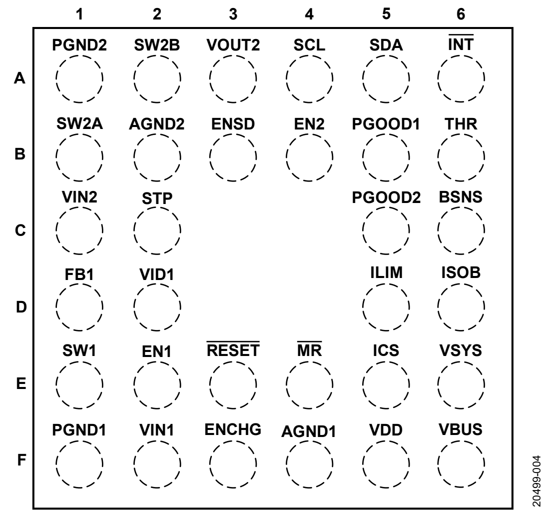


Figure 3. Ball Configuration (Top View)

Table 9. Ball Function Descriptions

Ball No.	Mnemonic	Description
A1	PGND2	Power Ground for the Buck Boost Regulator.
A2	SW2B	Switching Node for the Buck Boost Regulator.
A3	VOUT2	Buck Boost Regulator Output Pin.
A4	SCL	I^2C Serial Clock. This pin requires an external pull-up resistor.
A5	SDA	I^2C Serial Data. This pin requires an external pull-up resistor.
A6	$\overline{\text{INT}}$	Processor Interrupt (Active Low). This pin requires an external pull-up resistor. If this pin is not used, this pin can be left floating.
B1	SW2A	Switching Node for the Buck Boost Regulator.
B2	AGND2	Analog Ground.
B3	ENSD	Shutdown Mode Select. When this pin is low, the shutdown mode disables. When this pin is high, the shutdown mode enables.
B4	EN2	Enable Pin for Buck Boost Regulator.
B5	PGOOD1	Power-Good Signal Output. This open-drain output is the power-good signal for the selected VBUSOK, BATOK, CHG_CMPLT, VOUT2OK, or VOUT1OK bits (see Table 65).
B6	THR	Battery Pack Thermistor Connection.
C1	VIN2	Input Power for the Buck Regulator.
C2	STP	Stop Switching for the Selected Channel.
C5	PGOOD2	Power-Good Signal Output. This open-drain output is the power-good signal for the selected VBUSOK, BATOK, CHG_CMPLT, VOUT2OK, or VOUT1OK bits (see Table 65).
C6	BSNS	Battery Voltage Sense.
D1	FB1	Feedback Sensing Input for the Buck Regulator.
D2	VID1	Configure Buck Regulator Output Voltage. Connect a resistor from VID1 to AGND1 and AGND2 to program the buck regulator default output voltage. Float the pin to disable the pin select feature and use the register default set.
D5	ILIM	Input Current-Limit Select. Connect a resistor to AGND1 and AGND2 to set the default input current-limit level. Float the pin to disable the pin select feature and use the register default set.
D6	ISOB	Battery Supply-Side Input to Internal Isolation FET.

Ball No.	Mnemonic	Description
E1	SW1	Switching Node for Buck Regulator.
E2	EN1	Hardware Enable for Buck Regulators.
E3	$\overline{\text{RESET}}$	Reset Output.
E4	$\overline{\text{MR}}$	Manual Reset Input.
E5	ICS	Set Charge Current. Connect one resistor to ground to set the default charge current. Float the pin to disable the pin select feature and use the register default set.
E6	VSYS	Linear Charger, Supply Side Input to the Internal Isolation FET.
F1	PGND1	Power Ground for the Buck Regulator.
F2	VIN1	Input Power for the Buck Regulator.
F3	ENCHG	Logic Input for the Enable Charger Function.
F4	AGND1	Analog Ground.
F5	VDD	Internal Circuit Power Supply.
F6	VBUS	Power Connection to USB VBUS.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{VBUS} = 5.0 V, V_{ISOB} = 3.6 V, C1 = 2.2 µF, C2 = 1 µF, C3 = C4 = 10 µF, C5 = C6 = 10 µF, C7 = C8 = 10 µF, L1 = L2 = 4.7 µH, and all registers are at default values, unless otherwise noted.

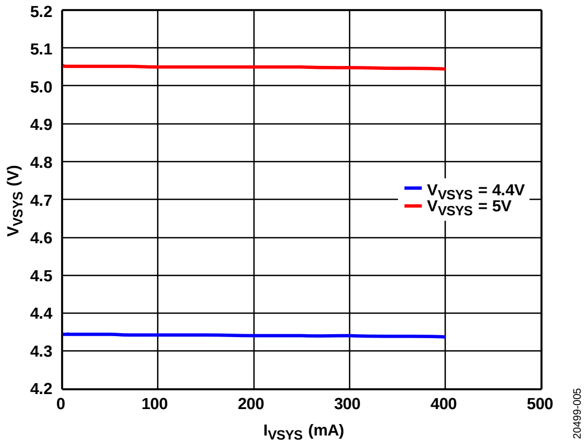


Figure 4. VSYS Load Regulation, V_{VSYS} = 4.4 V and 5 V, V_{VBUS} = 5.5 V, I_{VSYS} from 1 mA to 400 mA, No Charging

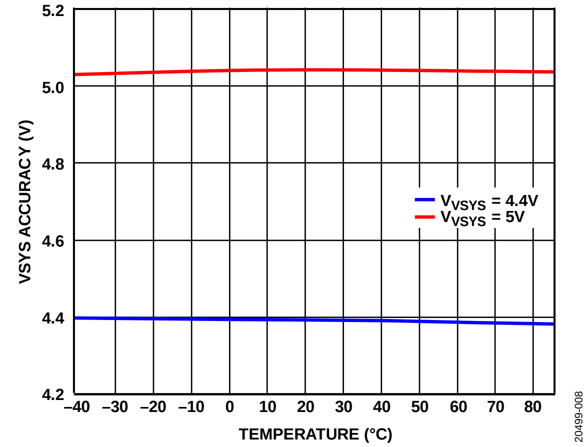


Figure 7. VSYS Accuracy vs. Temperature, V_{VBUS} = 5.5 V

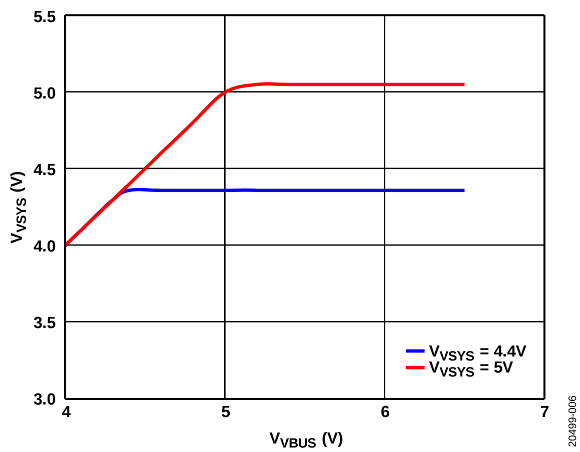


Figure 5. VSYS Line Regulation, V_{VSYS} = 4.4 V and 5 V, No Charging

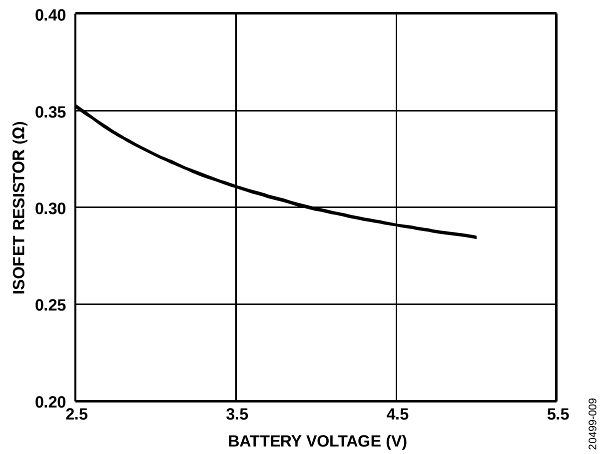


Figure 8. ISOFET Resistor vs. Battery Voltage

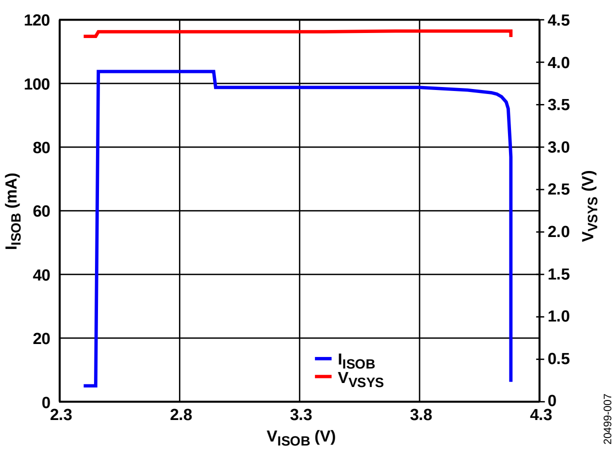


Figure 6. Charge Profile, V_{TRM} = 4.2 V, I_{CHG} = 100 mA

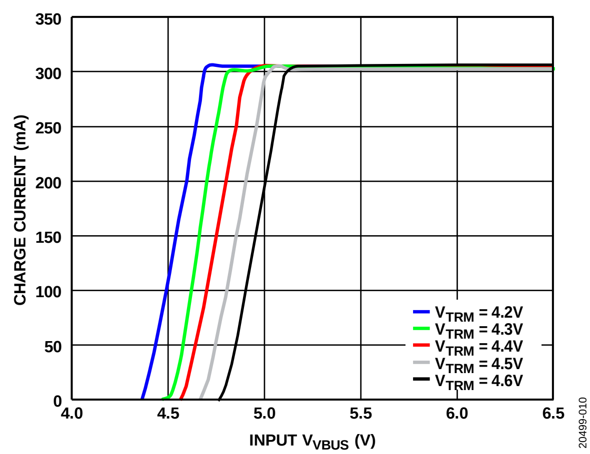


Figure 9. Charge Current vs. Input V_{VBUS}, I_{CHG} = 300 mA

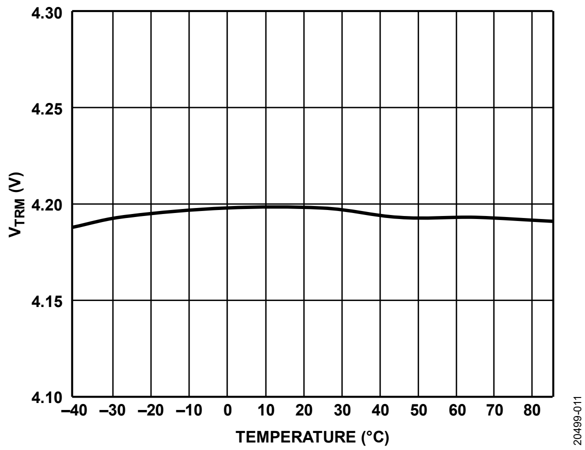


Figure 10. V_{TRM} vs. Temperature, V_{TRM} = 4.2 V

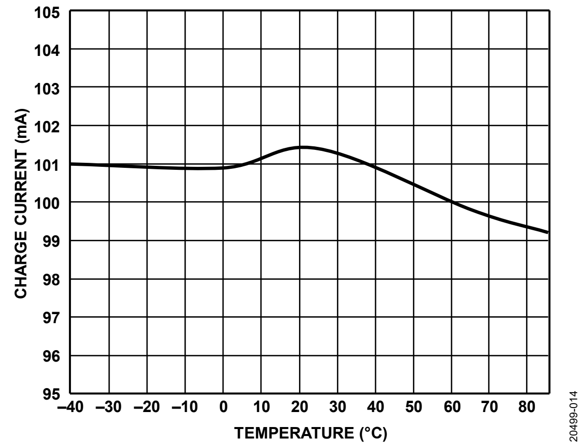


Figure 13. Charge Current vs. Temperature, I_{CHG} = 100 mA

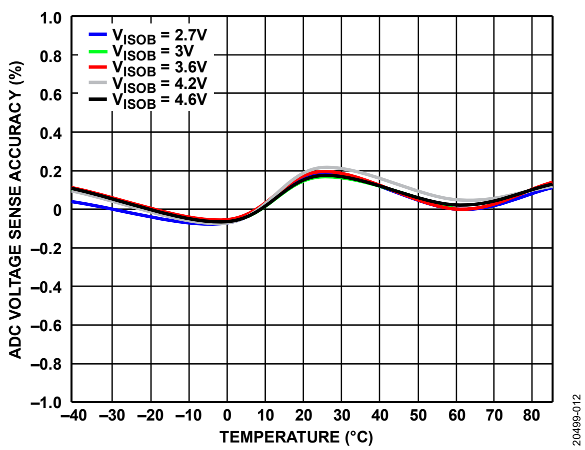


Figure 11. ADC Voltage Sense Accuracy vs. Temperature, V_{VBUS} = 0 V

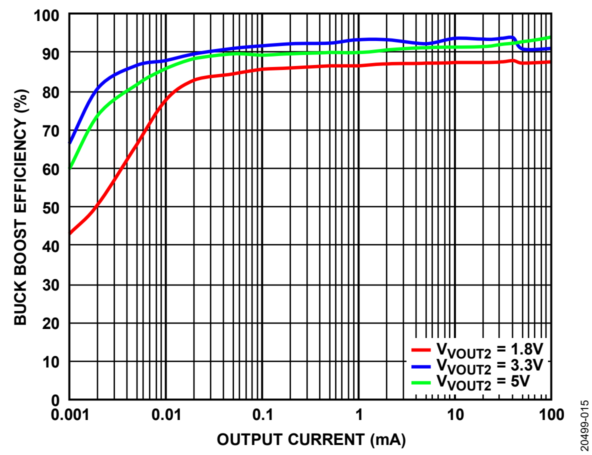


Figure 14. Buck Boost Efficiency vs. Output Current, V_{VIN2} = 3.6 V

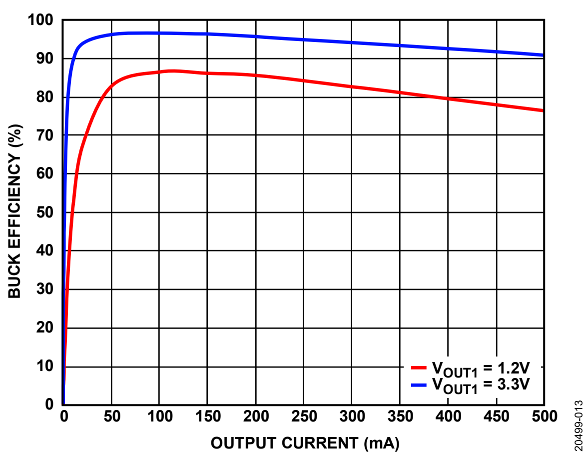


Figure 12. Buck Efficiency vs. Output Current, V_{VIN1} = 3.6 V, PWM Mode

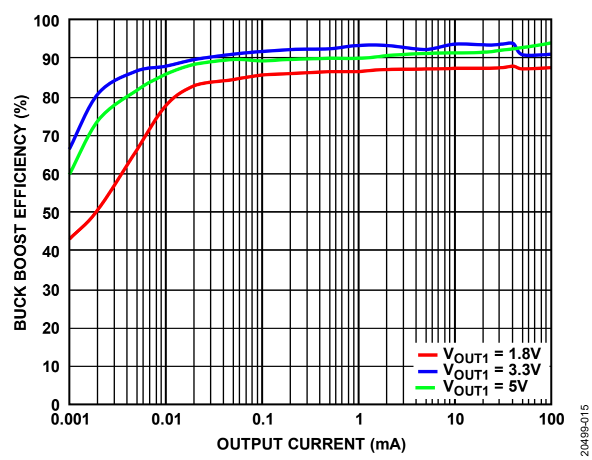


Figure 15. Buck Efficiency vs. Output Current, V_{VIN1} = 3.8 V, Hysteresis Mode

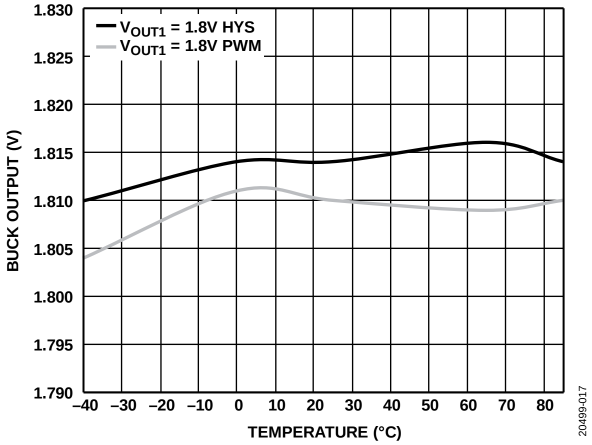


Figure 16. Buck Output vs. Temperature, VFB1_PWM_FIX and VFB1_HYS_FIX Accuracy

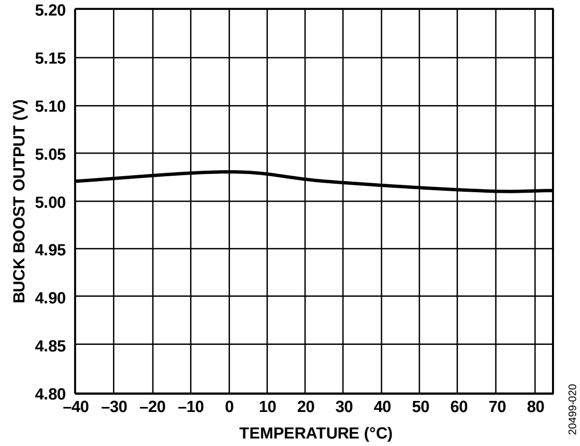


Figure 19. Buck Boost Output vs. Temperature, VOUT2 Accuracy

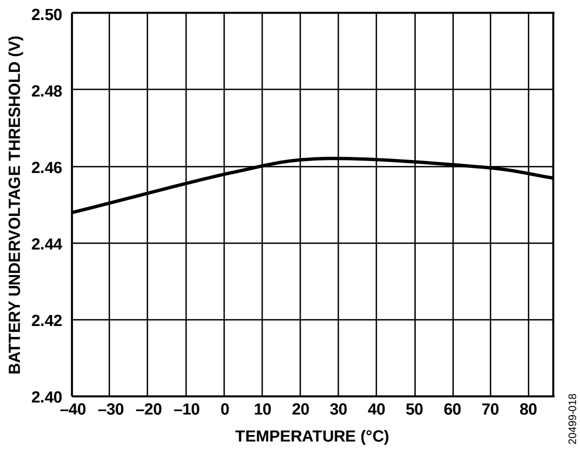


Figure 17. Battery Undervoltage Threshold vs. Temperature, BAT_UV = 2.5 V

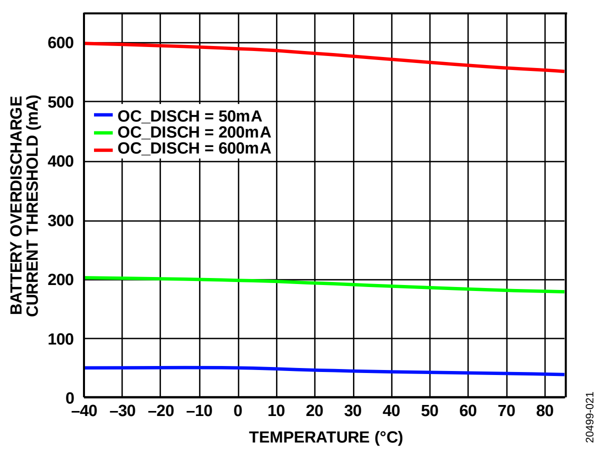


Figure 20. Battery Overdischarge Current Threshold vs. Temperature, V_{ISOB} = 3.8 V

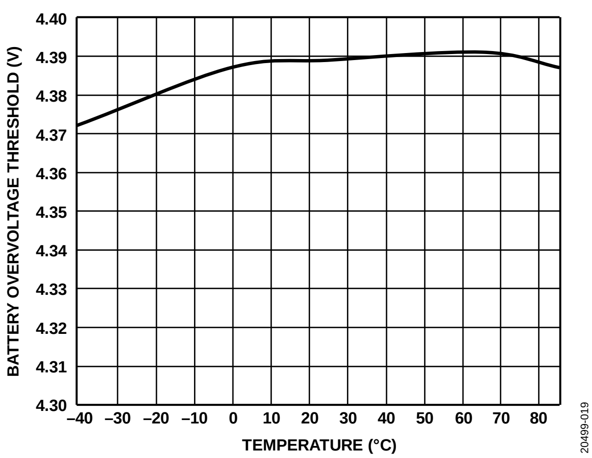


Figure 18. Battery Overvoltage Threshold vs. Temperature, V_{BPOV_RISE} = 4.3 V

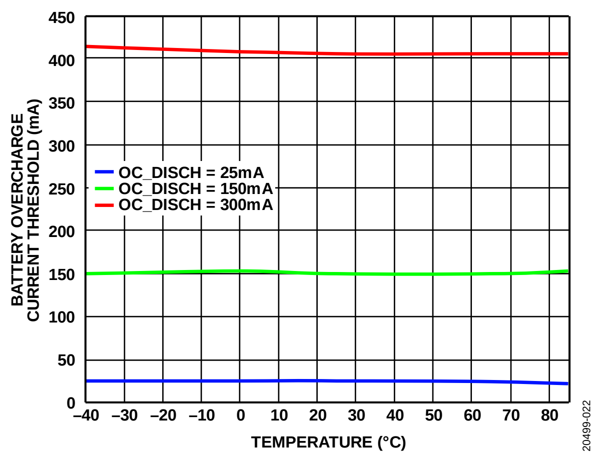


Figure 21. Battery Overcharge Current Threshold vs. Temperature, V_{ISOB} = 3.8 V

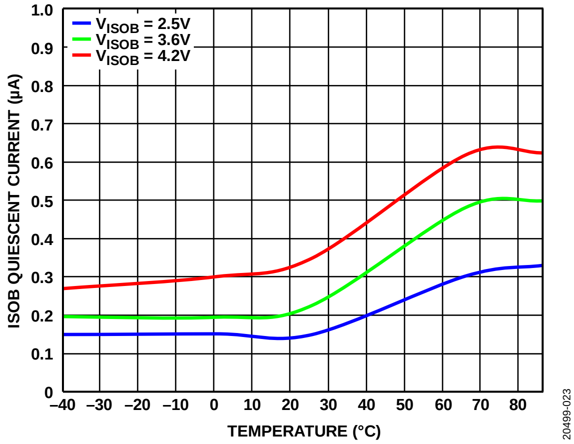


Figure 22. ISOB Quiescent Current vs. Temperature, All Disabled

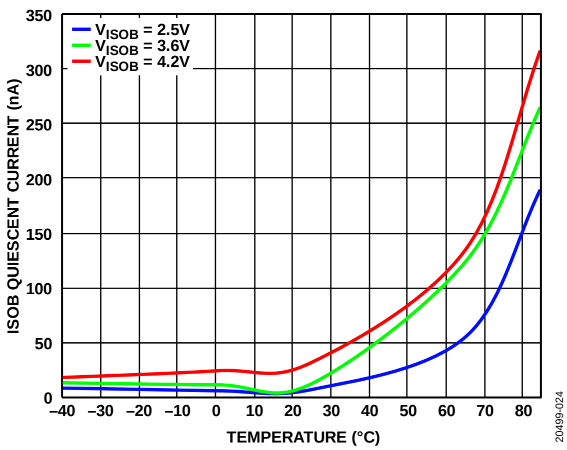


Figure 23. ISOB Quiescent Current vs. Temperature in Shipment Mode

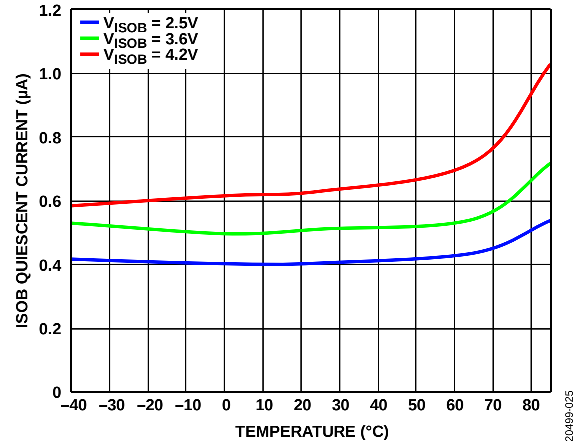


Figure 24. ISOB Quiescent Current vs. Temperature, Fuel Gauge Sleep Mode Enabled, Battery Protection Enabled, Buck Enabled, Buck Boost Enabled

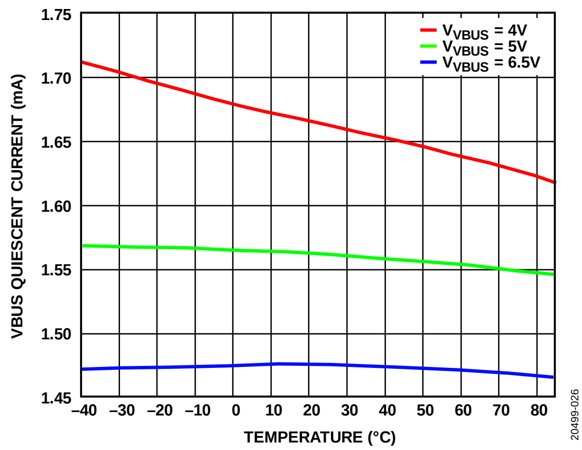


Figure 25. VBUS Quiescent Current vs. Temperature

TYPICAL WAVEFORMS

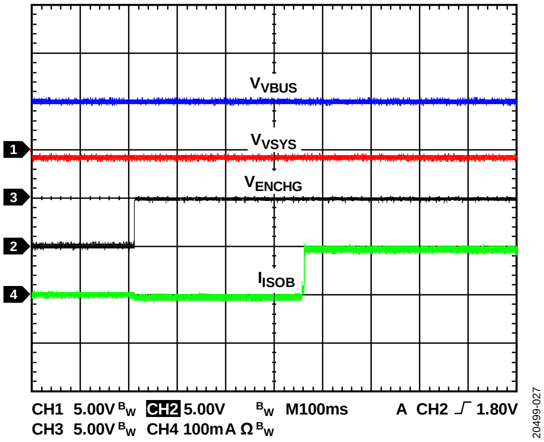


Figure 26. Charge Startup, V_{VBUS} = 5 V, V_{ISOB} = 3.8 V, I_{ILIM} = 200 mA, I_{CHG} = 100 mA

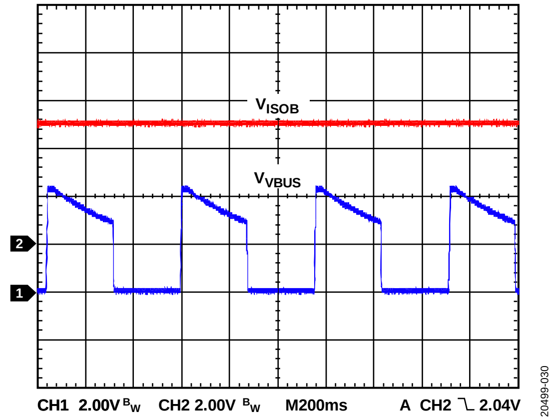


Figure 29. Battery Detection Waveform

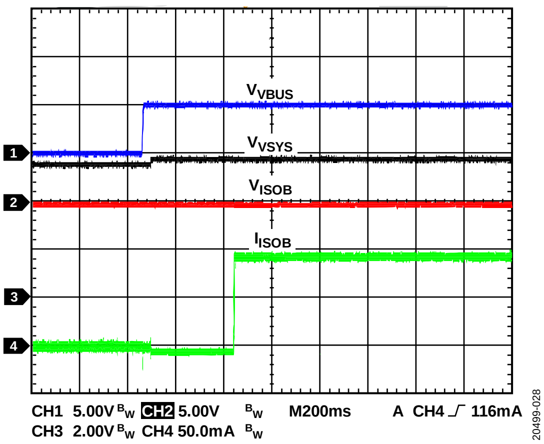


Figure 27. USB Connect and Start Charge, V_{VBUS} = 5 V, V_{ISOB} = 3.8 V, I_{CHG} = 100 mA

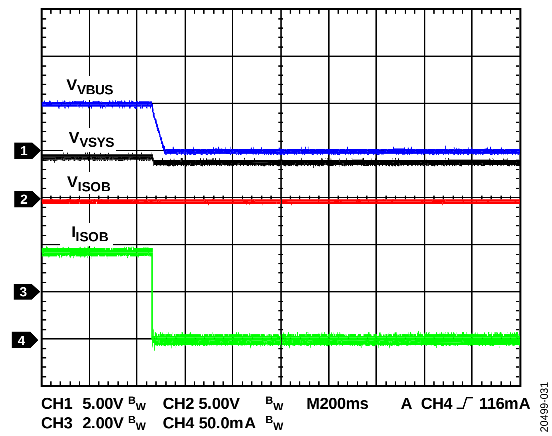


Figure 30. USB Disconnect and End Charge, V_{VBUS} = 5 V, V_{ISOB} = 3.8 V, I_{CHG} = 100 mA

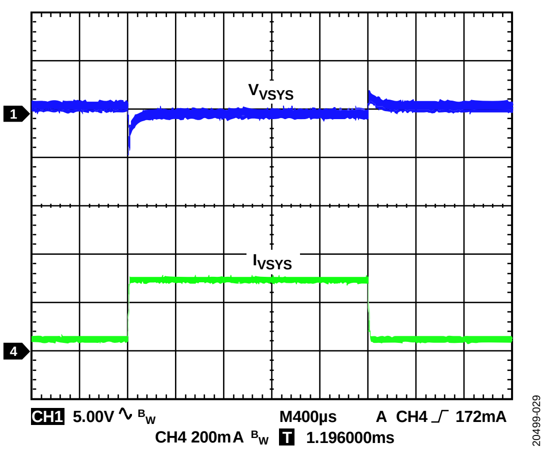


Figure 28. VSYS Load Transient, I_{VSYS} = 50 mA to 300 mA

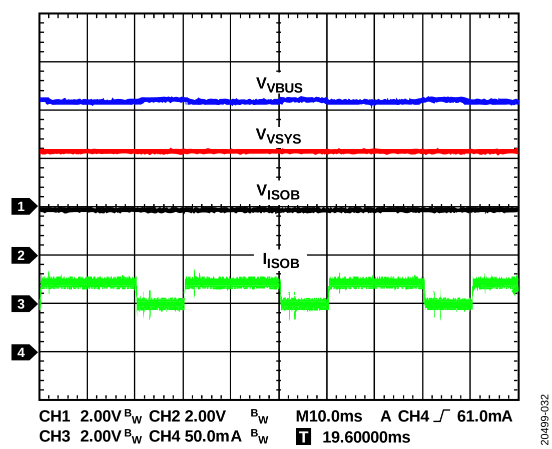


Figure 31. Adaptive Charge Current, VADPICHG[2:0] = 4.6 V, V_{VBUS} = 5 V with 10 Ω Impedance, I_{CHG} = 100 mA

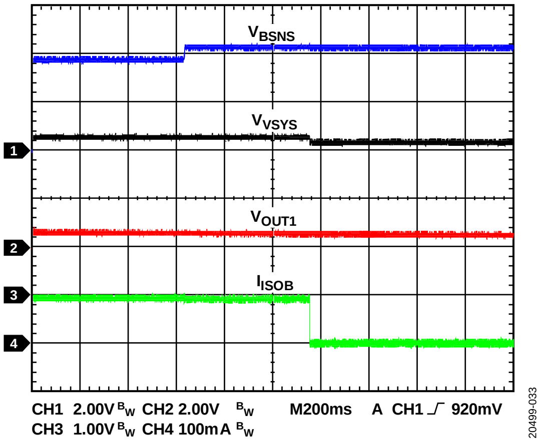


Figure 32. Battery Overvoltage Protection Waveform, V_{VBUS} = 5 V, OV_CHG = 4.3 V, DGT_OV_CHG = 0.5 sec

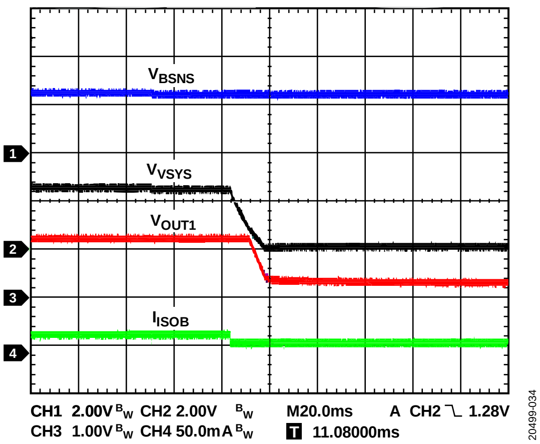


Figure 33. Battery Undervoltage Protection Waveform, V_{VBUS} = 0 V, UV_DISCH = 2.5 V, DGT_UV_DISCH = 30 ms

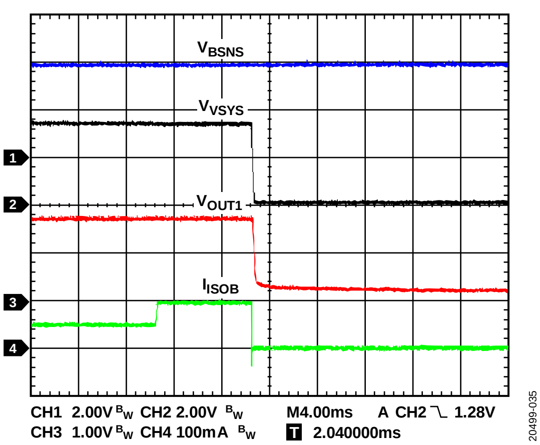


Figure 34. Battery Discharge Overcurrent Waveform, V_{VBUS} = 0 V, V_{ISOB} = 3.8 V, OC_DISCH = 100 mA, DGT_OC_DISCH = 10 ms

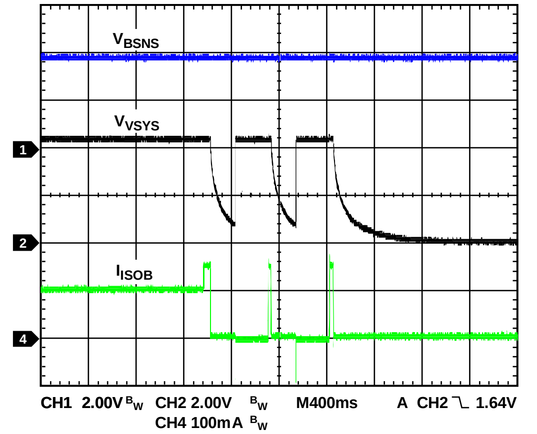


Figure 35. Battery Charge Overcurrent Waveform, V_{VBUS} = 5 V, V_{ISOB} = 3.8 V, OC_CHG = 150 mA, DGT_OC_CHG = 10 ms

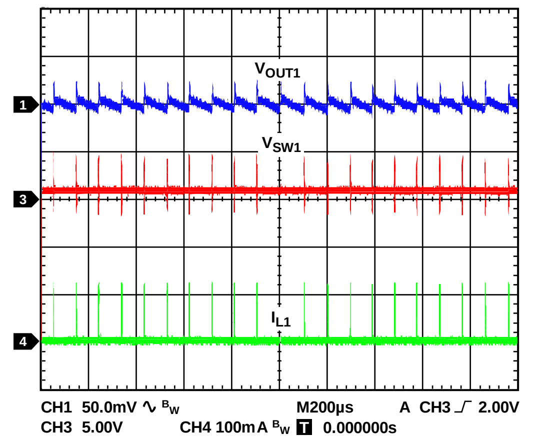


Figure 36. Buck Steady Hysteresis Waveform, Hysteresis Mode, V_{VIN2} = 3.8 V, V_{OUT1} = 1.2 V, Buck Output Current (I_{OUT1}) = 1 mA

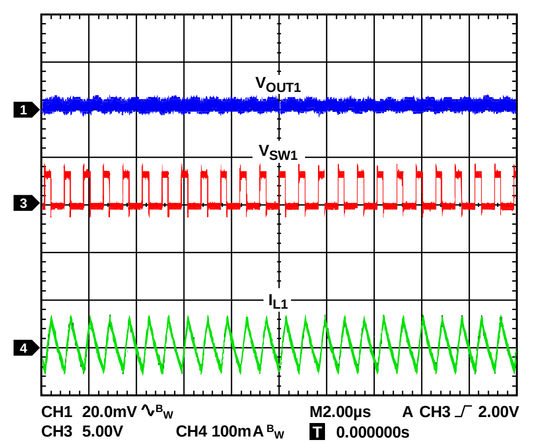


Figure 37. Buck Steady PWM Waveform, PWM Mode, V_{VIN1} = 3.8 V, V_{OUT1} = 1.2 V, I_{OUT1} = 1 mA

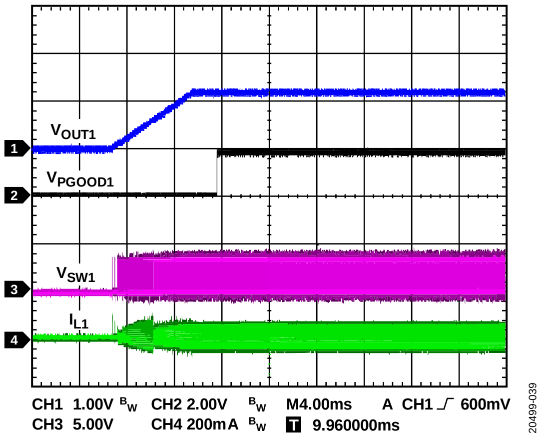


Figure 38. Buck Output Soft Start, Set EN_BUCK High, PWM Mode, V_{VIN1} = 3.8 V, V_{OUT1} = 1.2 V, PGOOD1 Mask to Buck Output (VOUT1), I_{OUT1} = 1 mA, t_{SS1} = 8 ms

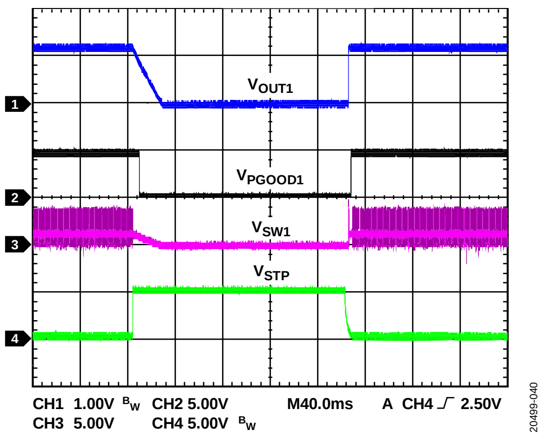


Figure 39. Buck Stop Function Waveform, V_{VIN1} = 3.8 V, V_{OUT1} = 1.2 V, Hysteresis Mode, PGOOD1 Mask to VOUT1, STP_BUCK = 1 Bit

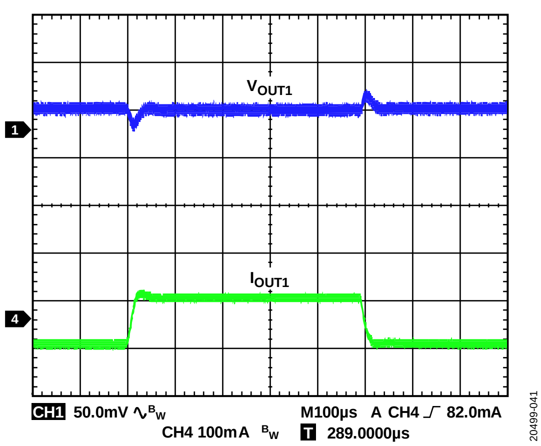


Figure 40. Buck Output Transient Waveform, V_{VIN1} = 3.8 V, V_{OUT1} = 1.2 V, I_{OUT1} = 1 mA to 100 mA, PWM Mode

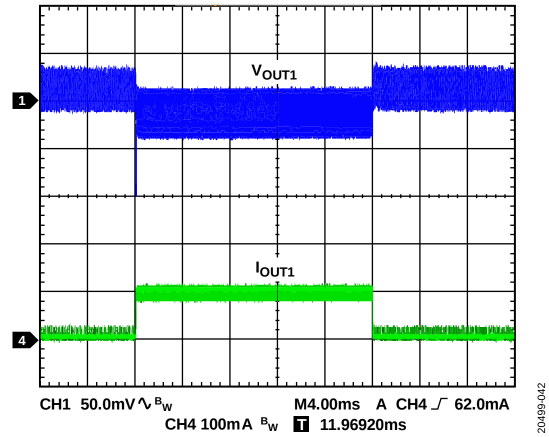


Figure 41. Buck Output Transient Waveform, V_{VIN1} = 3.8 V, V_{OUT1} = 1.2 V, I_{OUT1} = 1 mA to 100 mA, Hysteresis Mode

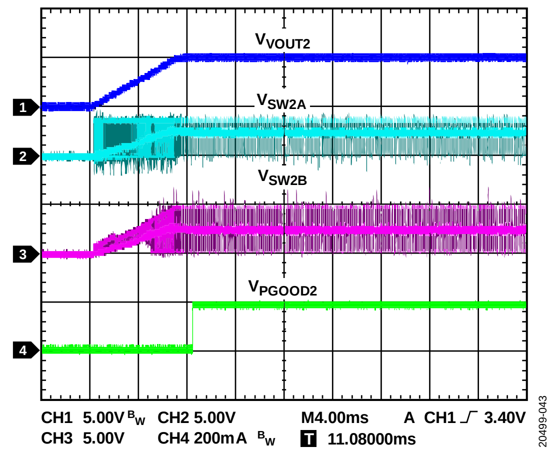


Figure 42. Buck Boost Output Soft Start Waveform, V_{VIN2} = 3.8 V, V_{OUT2} = 5 V, BUCKBST_SS[0:1] = 8 ms, Buck Boost Output Current (I_{OUT2}) = 1 mA, PGOOD2 Mask to VOUT2

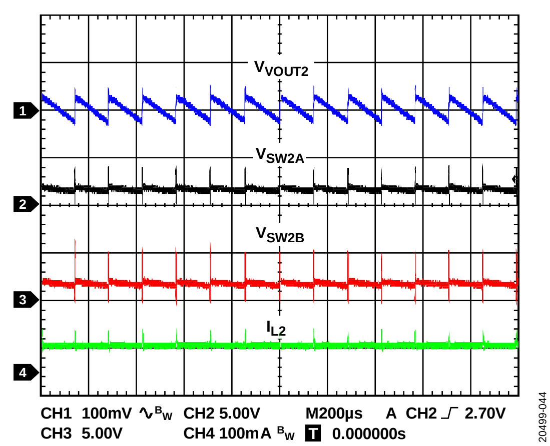


Figure 43. Buck Boost Steady Waveform, V_{VIN2} = 3.8 V, V_{OUT2} = 5 V, I_{OUT2} = 1 mA

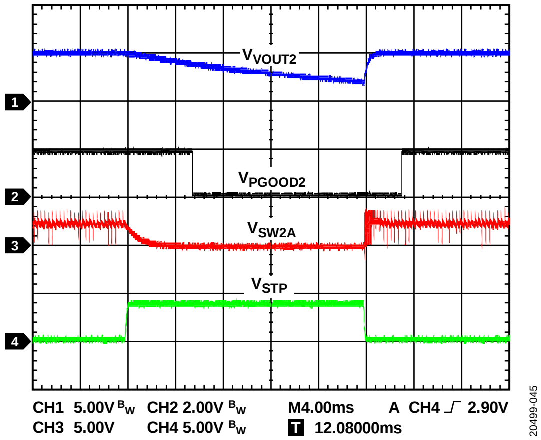


Figure 44. Buck Boost Stop Function Waveform, V_{VIN2} = 3.8 V, V_{VOUT2} = 5 V, PGOOD2 Mask to VOUT2, STP_BUCKBST = 1 Bit

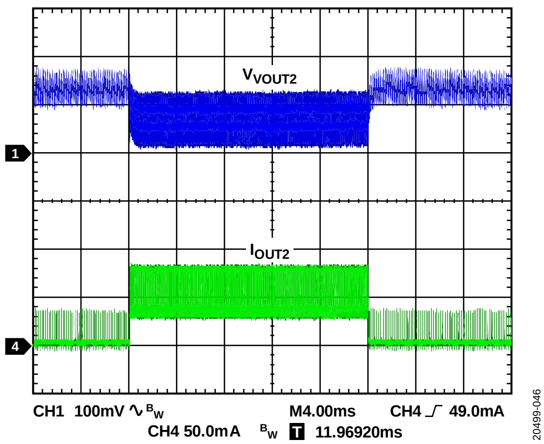


Figure 45. Buck Boost Output Transient Waveform, V_{VIN2} = 3.8 V, V_{VOUT2} = 3.3 V, I_{OUT2} = 1 mA to 50 mA

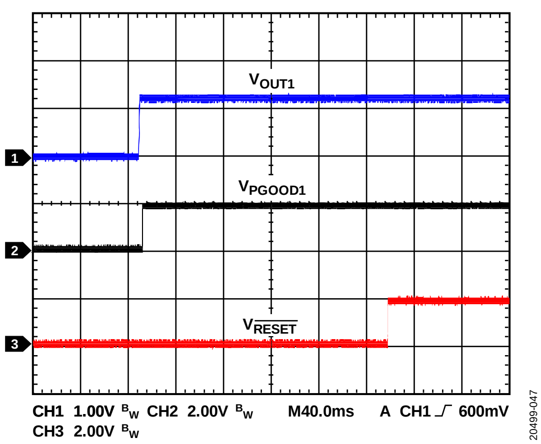


Figure 46. $\overline{\text{RESET}}$ Output and VOUT1, V_{ISOB} = 3.8 V, V_{OUT1} = 1.2 V, RESET_TIME = 200 ms, PGOOD1 Mask to VOUT1

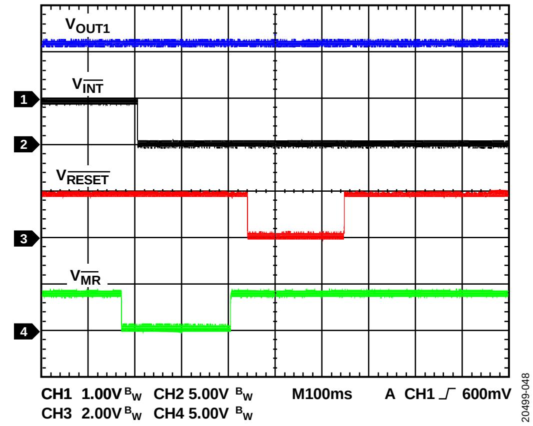


Figure 47. $\overline{\text{MR}}$ Press to Trigger Interrupt and $\overline{\text{RESET}}$, EN_WD_INT = 1 Bit, RESET_TIME = 200 ms

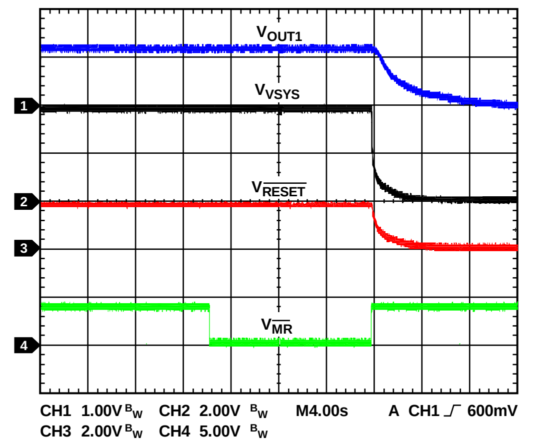


Figure 48. Press $\overline{\text{MR}}$ for Greater than 12 sec to Enter Shipment Mode, EN_MR_SD = 1 Bit, ENSD Pin High

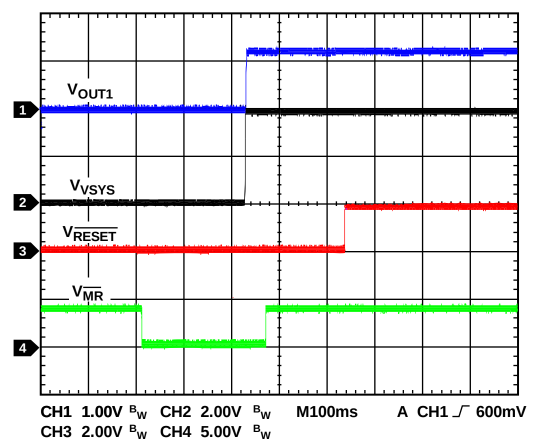


Figure 49. Press $\overline{\text{MR}}$ to Exit Shipment Mode, ENSD Pin High

THEORY OF OPERATION

BATTERY CHARGER

Charger Introduction

The ADP5360 integrates a fully I²C-programmable charger for single-cell Li-Ion/Li-Poly batteries suitable for a wide range of portable applications.

The linear charger architecture enables up to 500 mA of output current on the system power supply and up to 320 mA of charge current into the battery from a dedicated charger.

The charger of the ADP5360 operates from an input voltage of up to 6.8 V but is tolerant of voltages up to 20 V to alleviate the concern of USB bus spiking during disconnection or connection scenarios.

The ADP5360 features an internal FET between the linear charger output and the battery node to permit battery isolation and system power in a dead battery or no battery scenario, allowing instanteneous system function when connected to a USB power supply.

The charger of the ADP5360 enables charging via the mini VBUS pin (F6 pin) from a wall charger, car charger, or USB host port. Based on the type of USB source, which is detected by an external USB detection device, the ADP5360 can apply the proper current limit for optimal charging and USB compliance. The USB charger permits correct operation under all USB compliant sources including wall chargers, host chargers, hub chargers, and standard hosts and hubs.

A processor controls the USB charger using the I²C to program the charging current and numerous other parameters, including the following:

- Trickle charge current level and voltage threshold
- Fast charge (constant current) current level
- Fast charge (constant voltage) termination voltage level
- Fast charge safety timer period
- Weak battery threshold detection
- End of charge current level for charge completion
- Recharge voltage threshold
- VBUS input current limit

Input Current Limit and USB Compatibility

The VBUS input current limit is programmed via an internal I²C ILIM register (R_{ILIM}) from 50 mA to 500 mA, ensuring compatibility with different requirements. An external resistor from the ILIM pin to ground can also set the input current limit as the default. Floating the ILIM pin activates the register default value when powering up.

Table 10. VBUS Input Current-Limit Default Set with ILIM Pin

R_{ILIM} Value (kΩ)	ILIM Value (mA)
100	50
68	100
47	150
36	200
27	250
20	300
15	400
10	500

The current-limit defaults to 100 mA to allow compatibility with a USB host or hub that is not configured. This input current limit resets to a default value of 100 mA during every VBUS power-on cycle, thereby protecting the USB port.

When the input current-limit feature is used, it is possible for the available input current to be too low for the charger to meet the programmed charging current (I_{CHG}), and the rate of charge reduces. In this case, the VBUS_ILIM bit flag sets.

When V_{VBUS} is between 3.9 V and 6.8 V, the VBUSOK bit is set.

Trickle Charge Mode

A deeply discharged Li-Ion cell can exhibit a low cell voltage, making it unsafe to charge the cell at high current rates. The ADP5360 charger uses its trickle charge mode to raise the cell voltage to a safe level for fast charging. A cell with a voltage lower than V_{TRK_DEAD} charges with I_{TRK_DEAD}. During trickle charge mode, the CHARGER_STATUS[2:0] bits of the CHARGER_STATUS1 register are set.

During trickle charging, the VSYS node is regulated to V_{SYS_REG} by the linear regulator. The battery isolation FET is off, therefore the battery is isolated from the system power supply. Refer to Table 11 for the V_{SYS_REG} output voltages.

Table 11. V_{SYS_REG} Output Voltages

	V_{SYS_REG} (V)	
V_{TRM} Setting	$V_{SYSTEM} = V_{TRM} + 200$ mV	$V_{SYSTEM} = 5$ V
$V_{TRM} \leq 4.26$ V	4.4	5
4.26 V < $V_{TRM} \leq 4.36$ V	4.5	5
4.36 V < $V_{TRM} \leq 4.46$ V	4.6	5
4.46 V < $V_{TRM} \leq 4.56$ V	4.7	5
4.56 V < $V_{TRM} \leq 4.66$ V	4.8	5

When V_{VBUS} is lower than the set value of V_{SYS_REG}, V_{VSYS} cannot be regulated, which impacts the charged current (see Figure 9).

Trickle Charge Mode Timer

The duration of trickle charge mode is monitored to ensure that the battery revives from the deeply discharged state. If trickle charge mode runs for longer than t_{TRK} without the cell voltage reaching V_{TRK_DEAD}, a fault condition is assumed and charging stops. The battery isolation FET turns off, and VSYS is regulated to V_{SYS_REG} by the linear regulator. The fault condition asserts on when the CHARGER_STATUS[2:0] bits are set to 0b110, allowing the user to initiate the fault recovery procedure specified in the Fault Recovery section.

Weak Charge Mode (Constant Current)

When the battery voltage exceeds V_{TRK_DEAD} but is less than V_{WEAK}, the charger switches to the weak charge mode, and VSYS is regulated to V_{SYS_REG} by the battery isolation FET. Note that, V_{SYSTEM} = 5 V is not active on the output of V_{SYS_REG} during charge mode.

During weak charge mode, the battery is charged with programmed I_{CHG} from VSYS through the isolation FET and I_{TRK_DEAD}. Due to the VBUS input current limit, the real charge current (I_{CHG}) from VSYS may be less than the programmed value. System load can share the current from VSYS. However, I_{TRK_DEAD} always charges the battery during weak charge mode.

Fast Charge Mode (Constant Current)

When the battery voltage exceeds V_{WEAK}, the charger switches to fast charge mode, charging the battery with I_{CHG}. Address 0x04, ICHG[4:0] programs I_{CHG} via the I²C interface. During fast charge mode (constant current), the CHARGER_STATUS[2:0] bits are set to 0b010. The default I_{CHG} value can be set by the external resistor from the ICS pin (R_{ICS}) to ground. Floating the ICS pin activates the register default value when powering up.

Table 12. Charge Current Default Set Using the ICS Pin

R_{ICS} Value (kΩ)	I_{CHG} Value (mA)
100	10
68	50
47	80
36	100
27	150
20	200
15	250
10	300

During constant current mode, other features can prevent I_{CHG} from reaching the full programmed value. Input current limiting for USB compatibility can affect the I_{CHG} value under certain operating conditions. The battery isolation FET regulates V_{VSYS} to stay at V_{SYS_REG}. Note that, V_{SYSTEM} = 5 V is not active on the output of V_{SYS_REG} during charge mode.

The ADP5360 features a dynamic charge current that is adaptive when V_{VBUS} drops too much due to possible high internal impedance. The dynamic charge current monitors V_{VBUS} and reduces the charge current level when V_{VBUS} falls lower than the threshold, which can be programed by the I²C interface. When the charge current adapts due to the V_{VBUS} level, the ADPICHG status bit is set high. By default, this feature is disabled and can be enabled by the I²C setting.

Fast Charge Mode (Constant Voltage)

As the battery charges, the voltage rises and approaches V_{TRM}. The ADP5360 charger monitors V_{BSNS} to determine when charging ends. However, the internal impedance of the battery pack combined with the PCB and other parasitic series resistances creates a voltage drop between the sense point at the BSNS pin and the cell terminal. To compensate for this voltage drop and ensure a fully charged cell, the ADP5360 enters a constant voltage charge mode when V_{BSNS} reaches the termination voltage. The ADP5360 reduces charge current gradually as the cell continues to charge, maintaining a voltage of V_{TRM} on the BSNS pin. During constant voltage fast charge mode, the CHARGER_STATUS[2:0] bits are set to 0b011.

Fast Charge Mode Timer

The duration of fast charge mode is monitored to ensure that the battery is charging correctly. If the fast charge mode runs for longer than t_{CHG} without V_{BSNS} reaching V_{TRM}, a fault condition is assumed, charging stops, the battery isolation FET turns off, and VSYS regulates to V_{SYS_REG} by the linear regulator. A fault condition asserts on when the CHARGER_STATUS[2:0] bits are set to 0b110, allowing the user to initiate the fault recovery procedure specified in the Fault Recovery section.

If the fast charge mode runs for longer than t_{CHG} and the BSNS pin reaches V_{TRM} but the charge current has not yet fallen lower than I_{END}, charging stops by turning off the battery isolation FET. Note that the linear regulator still works, and VSYS regulates to V_{SYS_REG}. No fault condition is asserted in this circumstance, and the ADP5360 attains charge complete status.

Safety Timer

If the watchdog timer (see the Watchdog Timer section for more information) expires while in charger mode, the ADP5360 charger initiates t_{SAFE}. Charging continues for a period of t_{SAFE}, then stops by turning off the battery isolation FET and setting the CHARGER_STATUS[2:0] bits to 0b110.

Charge Complete

The ADP5360 charger monitors the charging current while in constant voltage fast charge mode. When EN_TEND is low, the current falls lower than I_{END} for t_{DG}, and the charger is stopped by turning the battery isolation FET off. The system voltage is maintained at V_{SYS_REG} by the linear regulator and sets the CHG_CMPLT flag. When EN_TEND is set to high, the charging current falls lower than I_{END} for another t_{END}, stopping the charger and setting the CHG_CMPLT flag.

Recharge

After the detection of charge is complete, and the battery isolation FET turns off, the ADP5360 charger still monitors the BSNS pin. If the BSNS pin voltage falls by V_{RCH}, the charger reactivates. Under most circumstances, triggering the recharge threshold results in the charger starting in fast charge mode.

Battery Charging Enable or Disable

To enable the ADP5360 charging function, set the EN_CHG bit high or pull the ENCHG pin high. The hardware ENCHG pin is logically OR'ed with the EN_CHG bit, Address 0x07. If the charger is disabled, the linear regulator remains turned on and regulates V_{VSYS} to V_{SYS_REG}. The battery isolation FET turns off, and the linear regulator provides the power for the system.

BATTERY ISOLATION FET

The ADP5360 charger features an integrated battery isolation FET for power path control and battery protection. The battery isolation FET isolates a deeply discharged Li-Ion cell from the system power supply in both trickle and fast charge modes, therefore allowing the system to be powered at all times. The battery isolation FET maintains V_{SYS_REG} on the VSYS pin.

When VBUS is lower than V_{VBUS_OK}, the battery isolation FET is in full conducting status.

The battery isolation FET supplements the battery to support high current functions on the system power supply when VBUS current is limited.

When the voltage on VSYS drops lower than ISOB, the battery isolation FET enters full conducting mode.

BATTERY DETECTION

Battery Level Detection

The ADP5360 charger features a battery detection mechanism to detect an absent battery. When the charger starts charging, it actively sinks and sources current into ISOB and voltage vs. time is detected. The sink phase detects a charged battery, while source phase detects a discharged battery.

The sink phase sinks current (I_{SINK}) from the ISOB pin and the BSNS pin for typically 330 ms (see Figure 50). If the BSNS pin is lower than V_{BATL} when the 330 ms timer expires, the charger starts the source phase. If the BSNS pin exceeds the V_{BATL} voltage when the 330 ms timer expires, the charger begins a new charge cycle.

The source phase sources current (I_{SOURCE}) to the ISOB pin or the BSNS pin for typically 330 ms. If the BSNS pin exceeds V_{BATH} before the 330 ms timer expires, it is assumed that no battery is present. If the BSNS pin does not exceed V_{BATH} when the 330 ms timer expires, it is assumed that a battery is present, and the charger begins a new charge cycle.

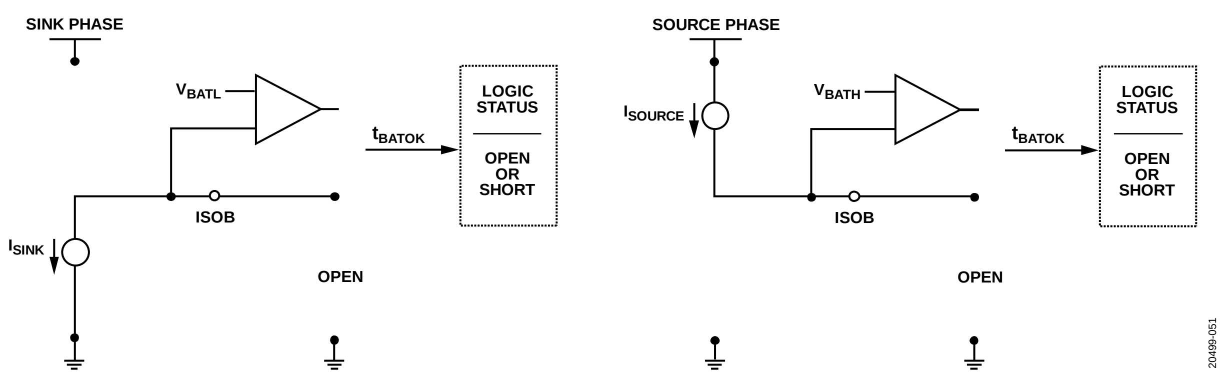


Figure 50. Battery Detection Sequence

BATTERY TEMPERATURE

Battery Pack Thermistor Input

The ADP5360 charger features battery pack temperature sensing that precludes charging when the battery pack temperature is outside of the specified range. The THR pin provides three programmable current sources: 60 µA, 12 µA, and 6 µA. Accordingly, the THR pin supports 10 kΩ, 47 kΩ, and 100 kΩ NTC resistors at 25°C. The THR pin is connected directly to the battery pack thermistor terminal.

When the THR function is enabled, the THR node voltage is sensed by the ADC and can be read in the 12-bit registers, THR_V_HIGH and THR_V_LOW. Calculate the external thermistor value (R_{NTC}) by using the following equation:

$$R_{NTC} = (THR\_V/60\ \mu A)$$

where:
THR_V is the ADC readback from the THR_V_HIGH and THR_V_LOW registers.
60 µA is selected by the THR pin source current.

To achieve the battery temperature, the R_{NTC} value must be known.

When V_{VBUS} is higher than $V_{VBUS\_OK\_RISE}$, the THR function is forced to enable for the charger control requirement. The update rate is 1 second. When V_{VBUS} is lower than $V_{VBUS\_OK\_RISE}$, set the EN_THR bit (Address 0x0A) high to enable the THR function. To save quiescent current the THR node voltage update rate slows to 30 seconds.

If the battery pack thermistor is not connected directly to the THR pin, a 100 kΩ (tolerance ±20%) dummy resistor must be connected between the THR pin and the AGND1 and AGND2 pins. Leaving the THR pin open results in a false detection of a <0°C battery temperature, and charging disables.

The ADP5360 charger monitors the voltage on the THR pin and suspends charging if the voltage is less than 0°C or higher than 60°C. For temperatures greater than 0°C and lower than 60°C, the THR_STATUS[2:0] bits, Address 0x09, are set accordingly.

JEITA Li-Ion Battery Temperature Charging Specification

The charge of the ADP5360 is compliant with the JEITA Li-Ion battery charging temperature specifications as shown in Table 13.

The JEITA function can be enabled via the I^2C interface. When the ADP5360 detects a JEITA cool condition, the charging current reduces, as shown in Table 14.

When the ADP5360 identifies a hot or cold battery condition, the battery isolation FET turns off. The VSYS pin is linear regulated at V_{SYS_REG} and provides power for the system.

Table 13. JEITA Li-Ion Battery Charging Specification Defaults

Parameter	Symbol	Conditions	Min	Max	Unit
JEITA Cold Temperature Limits	I_{JEITA_COLD}	No battery charging occurs.		0	°C
JEITA Cool Temperature Limits	I_{JEITA_COOL}	Battery charging occurs at approximately 50% or 10% of programmed level. See Table 14 for specific charging current reduction levels.	0	10	°C
JEITA Typical Temperature Limits	I_{JEITA_TYP}	Normal battery charging occurs at default and programmed levels.	10	45	°C
JEITA Warm Temperature Limits	I_{JEITA_WARM}	Battery termination voltage (V_{TRM}) is reduced by 100 mV from programmed value.	45	60	°C
JEITA Hot Temperature Limits	I_{JEITA_HOT}	No battery charging occurs.	60		°C

Table 14. JEITA Cool Temperature Limit—Reduced Charge Current Levels

	ICHG JEITA Value (mA)	
ICHG[4:0] Value (mA)	ILIM_JEITA_COOL = 0	ILIM_JEITA_COOL = 1
00000 = 10	10	10
00001 = 20	10	10
00010 = 30	10	10
00011 = 40	20	10
00100 = 50	20	10
00101 = 60	30	10
00110 = 70	30	10
00111 = 80	40	10
01000 = 90	40	10
01001 = 100	50	10
01010 = 110	50	10
01011 = 120	60	10
01100 = 130	60	10

ICHG[4:0] Value (mA)	ICHG JEITA Value (mA)	
	ILIM_JEITA_COOL = 0	ILIM_JEITA_COOL = 1
01101 = 140	70	10
01110 = 150	70	20
01111 = 160	80	20
10000 = 170	80	20
10001 = 180	90	20
10010 = 190	90	20
10011 = 200	100	20
10100 = 210	100	20
10101 = 220	110	20
10110 = 230	110	20
10111 = 240	120	20
11000 = 250	120	30
11001 = 260	130	30
11010 = 270	130	30
11011 = 280	140	30
11100 = 290	140	30
11101 = 300	150	30
11110 = 310	150	30
11111 = 320	160	30

Battery Charger Operational Flow Chart

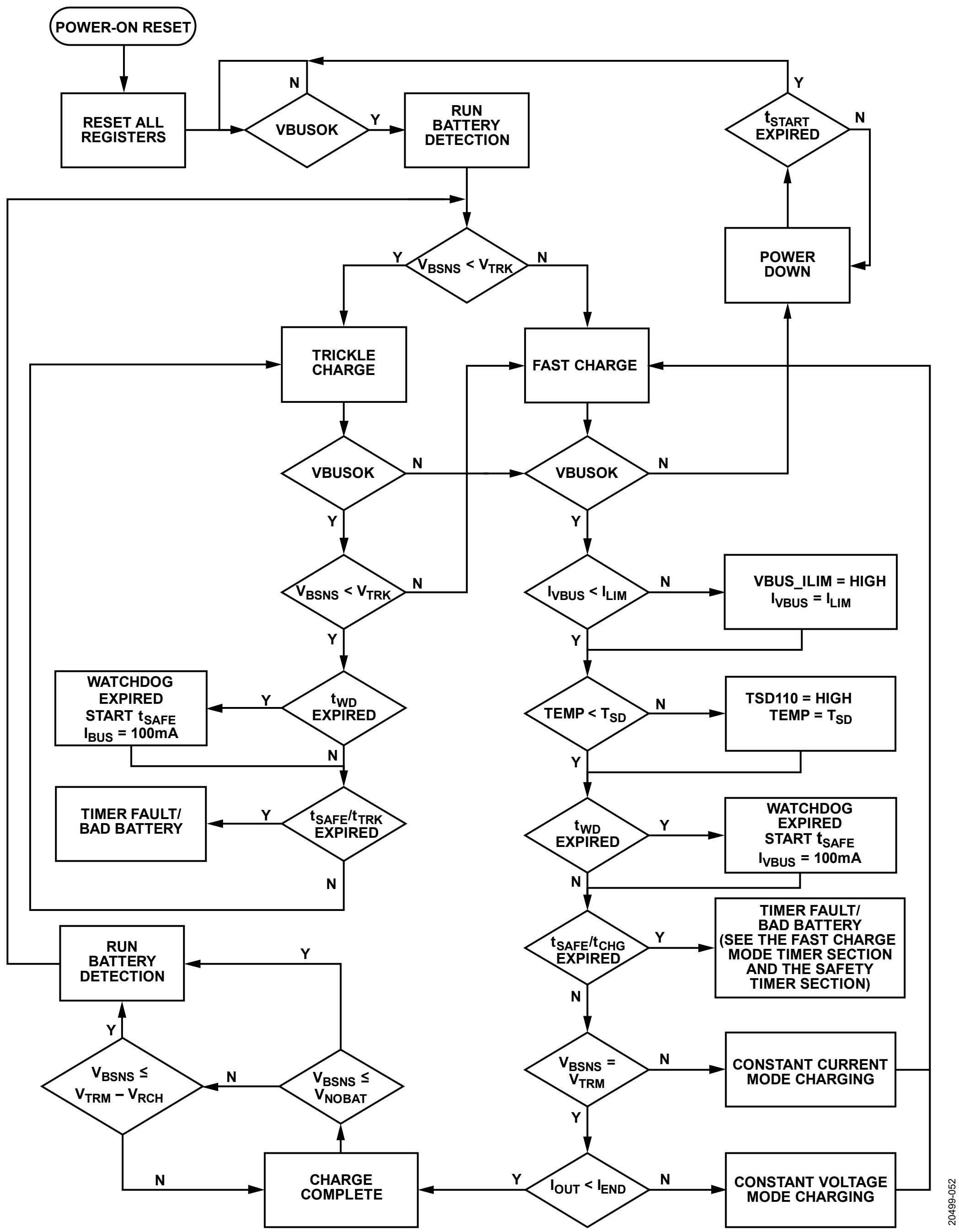


Figure 51. Charger Operational Flowchart

BATTERY FUEL GAUGE

General Description

The ADP5360 Li-Ion battery fuel gauge is optimized through a hybrid algorithm to indicate battery remaining capacity. The battery fuel gauge runs through a coulomb counter and is voltage-based between 0% to 100%. The battery fuel gauge uses a 12-bit ADC to measure the battery node voltage and the battery current. The state of the charge is calculated with an adaptive filter limitation algorithm integrated in the ADP5360. The ten open-circuit battery values and battery capacity are based on the battery characterization written to the V_SOC_x registers of the ADP5360 and used for the state of charge calculation. The sense current information, the battery capacity value, the continuous load current, and the large voltage drop all determine the state of the charge change rate. The fuel gauge operates as a coulomb counter with a high accuracy calculation when high continuous load current is applied. When the battery voltage reaches terminal voltage and charging completes, the battery state of the charge register, BAT_SOC, indicates 100% for battery capacity.

When the state of charge data is lower than the SOC_LOW_TH[1:0] bits configuration, the interrupt asserts, and the SOCLOW_INT bit is set high for as long as the low state of the charge interrupt feature is allowed.

Operation Mode

The ADP5360 fuel gauge default is shutdown mode to provide extremely low standby current consumption from the battery. After enabling the fuel gauge function, the state of charge initializes and calculates the first data only according to the battery voltage. Two operation modes can be selected: active and sleep. The I²C controls fuel gauge operation mode selection.

During active mode, the battery state of charge updates every ten seconds, and the battery voltage and instant current (I_{INS}) are sampled every second. The new mapping state of charge compares to the last state of charge value and then updates using the adaptive state of charge limit. According to the sense current and input battery capacity, the ADP5360 calculates the state of charge limit for a state of charge update each cycle.

During sleep mode, the state of charge update cycle is one minute, and the voltage and the current are sampled every 7.5 seconds. During this mode, the 12-bit ADC uses intervals and shutdown mode to save as much quiescent current as possible. Table 15 shows the fuel gauge quiescent current, ADC sample rate, and state of charge update rate. When the sense current is higher than the sleep current threshold setting (Address 0x27, SLP_CURR[1:0] bits), the ADP5360 fuel gauge exits sleep mode and enters active mode automatically.

Battery Capacity Adjustment with Aging

The ADP5360 features record total battery charged energy reporting when the device powers up, which allows estimation of battery aging.

The 12 BAT_SOCACM_H and BAT_SOCACM_L bits accumulate increased state of charge during every charge cycle. For example, the state of charge increases from 20% to 80% during charging, and these bits add 60 points. 100 points indicates one full charge cycle.

When BAT_SOCACM_H and BAT_SOCACM_L increase and reache 4096 points, and the battery has compiled nearly 41 full charges, then the BAT_SOCACM_H and BAT_SOCACM_L bits overflow and clear. The interrupt SOCACM_INT bit in Regiser 0x34 immediately asserts, and the system can adjust the BAT_CAP register manually or select automatic adjustment by setting the EN_BATCAP_AGE bit high. When selecting the battery aging automatic adjustment function, the battery capacity reduction proportion can be programmed by the BATCAP_AGE bits. When enabling this battery capacity aging automatic adjustment function, the BAT_CAP register cannot be rewritten to because this register is automatically adjusted by the ADP5360.

Battery Capacity Adjustment with Temperature

The Li-Ion battery capacity depends on the ambient operation temperature. The ADP5360 automatically adjusts the battery capacity calculation value based on the temperature variation when setting the EN_BATCAP_TEMP bit high. The temperature information comes from the THR node voltage sense. Therefore, the battery THR function must be active, and the EN_THR bit must be set to high.

The BATCAP_TEMP[1:0] bits can program the battery capacity calculation value adjustment proportion, and this value decreases as the temperature rises. This battery capacity adjustment is only effective when the THR node voltage senses the corresponding range of the TEMP_HIGH_45 to TEMP_LOW_0 bits (see Figure 52 and Table 17).

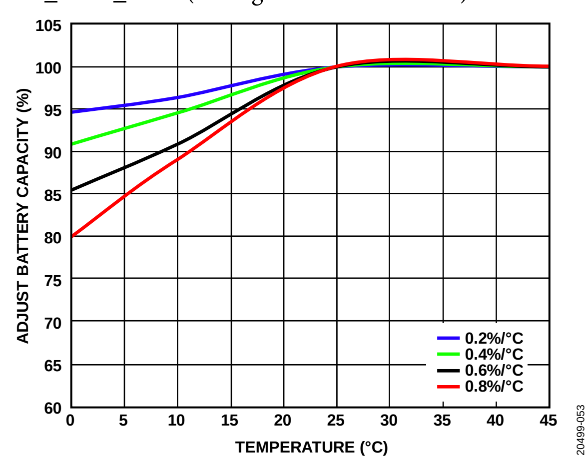
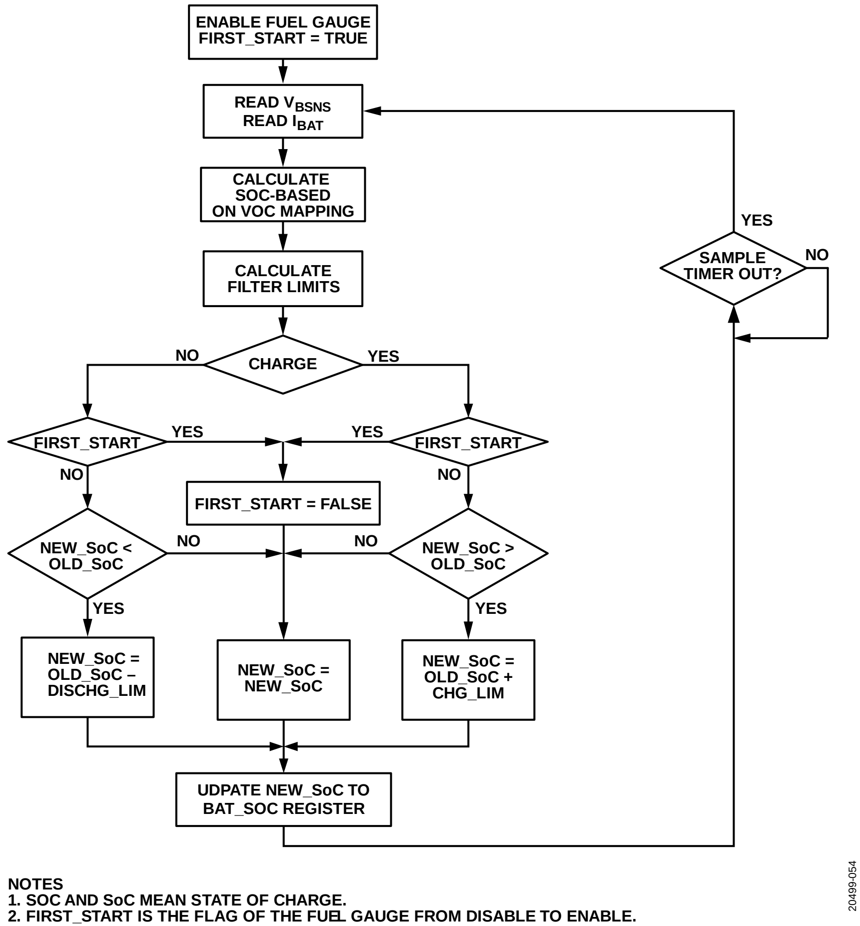


Figure 52. Battery Capacity Adjustment by Temperature in Fuel Gauge

Table 15. Fuel Gauge Operating Mode

Operation Mode	Typical Quiescent Current (µA)	ADC Sample Rate (sec)	State of Charge Update Rate
Sleep	0.2	7.5	1 min
		15	4 min
		30	8 min
		60	16 min
Active	3.5	1	10 sec

Flowchart of State of Charge Calculation



NOTES
1. SOC AND SoC MEAN STATE OF CHARGE.
2. FIRST_START IS THE FLAG OF THE FUEL GAUGE FROM DISABLE TO ENABLE.
3. NEW_SOC IS THE LATEST SOC, AND OLD_SOC IS THE SOC BEFORE THE LATEST SOC.
4. DISCHG_LIM AND CHG_LIM ARE THE ADAPTIVE STATE OF CHANGE LIMITS FOR DISCHARGING AND CHARGING.

Figure 53. Fuel Gauge Algorithm Flowchart (VOC Mapping Indicates Open-Circuit Battery Voltage Corresponding to 10 V_SOC_x Regsiters)

BATTERY PROTECTION

The ADP5360 features a full battery protection feature for Li-Ion and Li-Poly batteries. By default, after V_{ISOB} rises higher than V_{UVLO} and exits from shipment mode, battery protection is enabled. The ADP5360 supports the following fault protections:

- Undervoltage protection when the battery overdischarges
- Overdischarge current protection
- Overvoltage protection when the battery overcharges
- Overcharge current protection

When V_{BSNS} is lower than the battery undervoltage threshold after deglitch time, undervoltage protection triggers, the isolation FET turns off and isolates all system load to the ISOB pin, and the BAT_UV_STATUS bit is set high to indicate the battery status and fault register assertion. During undervoltage protection, the charger allows charge to the battery if the EN_CHGLB bit, Address 0x11, is set to high, and the charger exits undervoltage protection when the battery voltage becomes higher than the undervoltage threshold. The charger does not allow any charge for battery safety consideration if the EN_CHGLB bit is set low. Use the I^2C interface to select the undervoltage threshold and response time.

When the battery discharge current going through the isolation FET increases and rises higher than the overcurrent threshold after deglitch time, the overcurrent protection is triggered, and the isolation FET turns off and isolates all system load to the ISOB pin. This protection behavior can be selected to latch-up protection mode or hiccup mode by setting the OC_DIS_HICCUP bit, Address 0x11. In latch-up protection mode, the isolation FET turns off and shuts down the VSYS output after retrying three times. When the fault is removed, clearing the fault register or a VBUS power reset can recover normal operation. In hiccup protection mode, the isolation FET attempts to turn on after the typical 200 ms shutdown time until the system load fault is removed.

When triggering battery overvoltage protection, the LDO FET turns off, charging stops, and the LDO FET stays in suspend status. Duirng this protection, the isolation FET is selectable and can be turned off or kept turned.

When triggering the battery overcharge current, the LDO FET turns off, charging stops, and the LDO FET stays in suspend status. The isolation FET also turns off and shuts down the VSYS output. If selecting the latch-up overcharge protection mode, the charger remains in suspend status, and the battery does not allow charging after three retries. If selecting hiccup protection mode, the charger always attempts to restart the charge until the charger fault is removed. Clearing the fault register or VBUS power reset can recover normal operation after the fault is removed.

All battery protection function selection must be done when the ADP5360 powers up. Do not change the battery protection function during battery fault.

BUCK REGULATOR OPERATION

Operation Mode

The ADP5360 has two operation modes, PWM and hysteresis that are controlled by the I^2C interface.

PWM Mode

In PWM mode, the buck regulator operates at a fixed 1 MHz frequency that is set by an internal oscillator. At the start of each oscillator cycle, the high-side MOSFET switch turns on and sends a positive voltage across the inductor. The inductor current increases until the current sense signal exceeds the peak inductor current threshold, which turns off the high-side MOSFET switch. This threshold is set by the error amplifier output. During the high-side MOSFET off time, the inductor current decreases through the low-side MOSFET until the next oscillator clock pulse starts a new cycle.

In PWM mode, the regulator can supply up to 500 mA of average output current. The regulator can provide lower voltage ripple in PWM mode, which is useful for noise sensitive applications.

Hysteresis Mode

In hysteresis mode, the buck regulator in the ADP5360 charges the output voltage to a higher value than the nominal output voltage with PWM pulses. The buck regulator charges the output voltage by regulating the constant peak inductor current that is programed by the I^2C interface. When the output sense signal exceeds the hysteresis upper threshold, the regulator enters standby mode. In standby mode, the high-side and low-side MOSFETs and the control circuitry are disabled to allow a low quiescent current as well as a high efficiency performance.

During standby mode, the output capacitor supplies energy into the load, and the output voltage decreases until the voltage falls lower than the hysteresis comparator lower threshold. The buck regulator wakes up and generates the PWM pulses to charge the output again.

Because the output voltage occasionally enters standby mode and then recovers, the output voltage ripple in hysteresis mode is larger than the ripple in PWM mode. The varying switching frequency creates more noise in the system. Therefore, it is recommended to use PWM mode during charging status.

Use the following equation in hysteresis mode to calculate the regulator output current:

$$I_{LOAD1\_HYS} = I_{PEAK1\_HYS}/2$$

where:
I_{LOAD1_HYS} is the regulator output current.
I_{PEAK1_HYS} is the inductor peak current.

The maximum regulator output current is 100 mA when the limitation of the inductor peak current, BUCK_ILIM, is set to 200 mA.

Program Output Voltages

Adjustable output voltage settings are available on the ADP5360 by connecting a resistor through the VID1 pin to the AGND1 and AGND2 pins. The VID detection circuitry works in the start-up period, and the voltage ID code is sampled and held into the internal register and does not change until the next power recycle.

Table 16 lists the output voltage options for the VID1 pin configurations. Additional output voltage options from 0.6 V to 3.75 V with a 50 mV step are available on the ADP5360, and to program these options set the VOUT_BUCKBST[5:0] bits, Address 0x2C via the I^{2}C interface. The ADP5360 also has a fixed output voltage that is programmed via the factory fuse. In this case, connect the VID1 pin to the VIN1 pin.

Table 16. V_{OUT1} Default Set Using the VID1 Pin

VID1 Resistor, R_{VID1} Value (kΩ)	V_{OUT1} Value (V)
100	3.3
68	3.0
47	2.8
36	2.5
27	1.8
20	1.5
15	1.2
10	1.0

For the output voltage settings, the feedback resistor divider is built into the ADP5360, and the feedback pin (FB1) must be tied directly to the output. An ultra low power voltage reference and an integrated high impedance feedback divider network contribute to the low quiescent current. Floating the VID1 pin activates the register default value when powering up.

Enable and Disable

The ADP5360 includes a hardware enable pin (EN1). A logic high on the EN1 pin starts the buck regulator. Due to the low quiescent current design, it is typical for the regulator to start switching after a delay of a few milliseconds from when the EN1 pin is pulled high. Do not pull the EN1 pin high to the ISOB pin because that can cause unexpected leakage current. It is recommended to pull the EN1 pin high to the VSYS pin with a resistor.

The EN_BUCK bit, Address 0x29, can control the buck enable and disable, which is logically ANDed with the EN1 pin. For example, set the EN_BUCK bit high, and use the EN1 pin control buck to enable or to disable. Alternatively, pull the EN1 pin high and set the EN_BUCK bit via the I^{2}C interface.

PGOOD Indication

The VOUT1OK bit, Address 0x2F, indicates whether the buck regulator is working appropriately. A logic high indicates that the output voltage of the buck regulator is higher than 90% (typical rising threshold) of the nominal output. When the regulated output voltage falls lower than 87% (typical falling threshold) of the nominal output, the VOUT1OK bit goes low.

The status indication of the VOUT1OK bit can be masked to the hardware pin output of the PGOOD1 pin or PGOOD2 pin by setting Register PGOODx_MASK with the I^{2}C interface.

Soft Start

The ADP5360 buck regulator has an internal soft start function that ramps up the output voltage in a controlled manner during startup, thereby limiting the inrush current. This feature prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the device. The default typical soft start time is 1 ms for the regulator. Other soft start times (8 ms, 64 ms, and 512 ms) can be programmed for the ADP5360 by the I^{2}C interface.

100% Duty Cycle Operation

When the input voltage approaches the output voltage, the ADP5360 stops switching and enters 100% duty cycle operation. The buck connects the output via the inductor and the internal high-side power switch to the input. When the input voltage is charged again, and the required duty cycle falls to 95% typical, and the buck immediately restarts switching and regulation without allowing overshoot on the output voltage.

Active Discharge

The ADP5360 integrates an optional discharge switch from the switching node to ground. This switch turns on when the associated regulator is disabled to help discharge the output capacitor quickly. The typical value of the discharge switch is 255 Ω for the regulator.

The active discharge feature can be enabled by setting the DISCHG_BUCK bit, Address 0x29, high for the buck regulator.

Current-Limit Protection

The buck regulator in the ADP5360 has protection circuitry that limits the direction and the amount of current to a certain level that flows through the high-side MOSFET and the low-side MOSFET in cycle by cycle mode. The positive current limit on the high-side MOSFET limits the amount of current that can flow from the input to the output. The negative current limit on the low-side MOSFET prevents the inductor current from reversing direction and flowing out of the load.

Short-Circuit Protection

The buck regulator in the ADP5360 includes frequency foldback to prevent current runaway on a hard short in PWM mode. When the output voltage at the feedback pin (FB1) falls lower than 50% of VOUT1 typical, indicating the possibility of a hard short at the output, the switching frequency is reduced to half of the internal oscillator frequency. The reduction in the switching frequency allows more time for the inductor to discharge, preventing a runaway of output current.

Stop Switching

The ADP5360 includes one STP pin that can be configured as a stop pin to allow the user to temporarily stop the buck regulator switching.

When applying a logic high level to the STP pin, the corresponding regulator is forced to stop switching immediately. When applying a logic low level to the STP pin, the regulator resumes switching. Note that tens of ns delay time exists from when the STP signal goes high to when switching fully stops.

The stop signal control is valid only when the regulator is enabled. Otherwise, the stop signal is ignored.

Using the stop signal for hysteresis mode can generate a power-good failure due to the slow transient response.

Set the STP_BUCK bit, Register 0x29, low to disable the buck regulator stop switching feature.

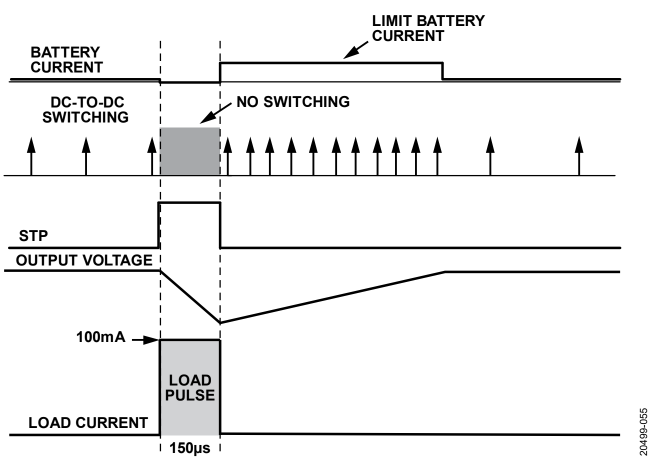


Figure 54. STP Signal Diagram

BUCK BOOST REGULATOR OPERATION

Operation Mode

The buck boost regulator in the ADP5360 is synchronous with the current mode, switching regulators designed to maintain a fixed output voltage from an input supply (VIN2) that can be greater than, equal to, or less than VOUT2.

The buck boost regulator works in hysteresis mode and regulates the output voltage to a slightly higher value than the target output voltage with switching pulses. When the output voltage increases until the output sense signal exceeds the hysteresis upper threshold, the regulator enters sleep mode. In sleep mode, the high-side and low-side MOSFET and a majority of the control circuitry are disabled to allow a low quiescent current as well as high efficiency performance. During sleep mode, the output capacitor supplies the energy into the load, the output voltage decreases until the voltage falls lower than the hysteresis comparator lower threshold, and the regulator wakes up and generates the switching pulses to charge the output again.

Program Output Voltages

The ADP5360 buck boost regulator provides output voltage options from 1.8 V to 2.9 V with a 100 mV step, and 2.95 V to 5.5 V with 50 mV step, which can be programmed by the VOUT_BUCKBST[5:0] bits, Address 0x2C, and set via the I^{2}C interface (see Table 62). The buck boost regulator also provides a fixed output voltage programmed via the factory fuse.

For the output voltage settings, the feedback resistor divider is built in the ADP5360. An ultra low power voltage reference and an integrated high impedance (50 MΩ typical) feedback divider network contribute to the low quiescent current.

Enable and Disable

The ADP5360 includes a hardware enable pin (EN2). A logic high in the EN2 pin starts the buck boost regulator. Because of the low quiescent current design, it is typical for the regulator to start switching after a delay of a few milliseconds from when the EN2 pin pulls high. To avoid unexpected leakage current, do not pull the EN pin high to the ISOB pin. However, do pull the EN2 pin high to the VSYS pin with the resistor.

The I^{2}C register bit, EN_BUCKBST, Address 0x2B, can also control the buck boost enable and disable, which are logically OR'ed with the EN2 pin. For example, set the EN_BUCKBST bit to low, then use the hardware EN2 pin to control the buck boost enable and disable, or pull the EN2 pin low, and then set the EN_BUCKBST bit using the I^{2}C inteface.

PGOOD Indication

The VOUT2OK bit, Address 0x2F, indicates whether the buck boost regulator is working properly. A logic high indicates that the output voltage of the buck boost regulator is higher than 90% (typical rising threshold) of the nominal output. When the regulated output voltage falls lower than 87% (typical falling threshold) of the nominal output, the VOUT2OK bit goes low.

The VOUT2OK bit status indication can be masked to the PGOOD1 pin or PGOOD2 pin by setting the PGOODx_MASK register with the I²C interface.

Soft Start

The ADP5360 buck boost regulator has an internal soft start function that ramps up the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This feature prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the device. The default typical soft start time is 1 ms for the regulator. Other soft start times (8 ms, 64 ms, and 512 ms) can be programmed for the ADP5360 by the I²C interface.

Active Discharge

The ADP5360 integrates an optional discharge switch from the output node to ground. This switch turns on when the associated regulator is disabled to help discharge the output capacitor quickly. The typical value of the discharge switch is 255 Ω for the regulator.

The active discharge feature can be enabled by setting the DISCHG_BUCKBST bit, Address 0x2B, high for the buck boost regulator.

Current-Limit Protection

The buck boost regulator in the ADP5360 includes peak current-limit protection circuitry to limit the amount of positive current flowing through the high-side MOSFET switch. The peak current limit on the power switch limits the amount of current that can flow from the input to the output. The programmable current-limit threshold feature allows for the use of small size inductors for low current applications.

Use the BUCKBST_ILIM[2:0] bits, Address 0x2B, via the I²C interface to program the peak current-limit threshold on the buck boost regulator. Three bit-programmable options provide 100 mA to 800 mA of peak current limit with a 100 mA step peak current threshold range. Use the following equation to find the regulator output current:

$$I_{LOAD2} = V_{IN2} \times I_{PEAK2}/2(V_{IN2} + V_{OUT2})$$

where:
I_{LOAD2} is the regulator output current.
V_{IN2} is the regulator input voltage.
I_{PEAK2} is the inductor peak current.
V_{OUT2} is the output voltage.

The peak current limit is different than the average current limit on the battery input side. The average battery current is a factor in different elements including, but not limited to, the VIN2/VOUT2 relationship, the inductance, the switching frequency, and the peak current-limit threshold. The average battery current limit on each buck or buck boost regulator can be roughly calculated and predicted by these elements. However, the average current-limit accuracy is difficult to guarantee due to variations in inductance and switching frequency. Therefore, a careful calculation must be obtained if the input source is coming from a weak battery, which typically has high output impedance.

Stop Switching

The stop feature also can configure the buck boost regulator with the STP pin input, which allows the user to temporarily stop buck boost regulator switching.

When applyin a logic high level to the STP pin, the corresponding regulator is forced to stop switching immediately. When applying a logic low level to the STP pin, the regulator resumes switching. Note that tens of ns delay time exists from when the STP signal goes high to when switching fully stops.

The stop signal control is valid only when the regulator is enabled. Otherwise, the stop signal is ignored.

Set the STP_BUCKBST bit, Address 0x2B, low to disable the buck boost regulator stop switching feature.

SUPERVISORY

Reset Output

The ADP5360 provides microprocessor supply voltage supervision by controlling the reset input of the microprocessor. When the monitored voltage falls lower than the associated threshold, the $\overline{\text{RESET}}$ pin asserts correspondingly. Asserting the $\overline{\text{RESET}}$ pin quickly ensures that the entire system is reset immediately before any part of the system voltage falls lower than the recommended operating voltage. The default monitor voltage is the buck output voltage (VOUT1) and can be selected as VOUT2 by the I²C interface. The $\overline{\text{RESET}}$ pin monitors both VOUT1 of the buck and VOUT2 of the buck boost when setting the VOUT1_RST bit and VOUT2_RST bit of Address 0x2D both high.

Manual Reset Input

The ADP5360 features a manual reset input. When driving the MR pin low from high with the deglitch time (t_{DG}), the INT pin asserts an interrupt when the EN_MR_INT bit, Address 0x33, is set to high. When the MR pin transitions from low to high, the RESET pin output asserts and remains asserted for the duration of the reset timeout period (t_{RP}) before deasserting. Connect an external pull-up resistor from tthe MR input to the VDD pin for a logic high output. To generate a reset, connect an external push-button switch between the MR pin and ground. Noise immunity is provided on the MR input, and fast transients going in a negative direction are ignored. A 0.1 µF capacitor between the MR pin and ground provides additional noise immunity if required.

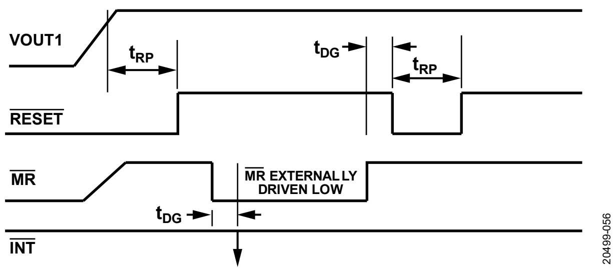


Figure 55. Manual Reset Timing Diagram

When the EN_MR_SD bit, Address 0x2D is set to enable shipment mode, pulling down the MR pin for more than a 12 second time out,and then releasing the MR pin, shuts down all function blocks, and the ADP5360 then enters shipment mode. To exit shipment mode, pull the MR pin low for t_{SH}, and the ADP5360 restarts with the default factory setting registers.

Watchdog Timer

The ADP5360 features a watchdog timer that monitors microprocessor activity. A timer circuit is cleared with every write to the RESET_WD bit, Address 0x2D. If the timer counts through the preset watchdog timeout period (t_{WD}), a RESET output asserts. The microprocessor must toggle the RESET_WD bit to avoid being reset.

When RESET is asserted, the watchdog timer clears and does not count again until the RESET output deasserts. To disable the watchdog timer, set the EN_WD bit, Address 0x2D via the I^2C interface. Note that the watchdog timer is ignored when RESET is not activated.

If the watchdog timer expires without being reset while in charger mode, the ADP5360 charger assumes there is a software problem and triggers t_{SAFE}. For more information, see the Safety Timer section.

SHIPMENT MODE

The ADP5360 provides optional shipment mode as a default status after ISOB powers up. During shipment mode, most function blocks shut down, including the ISOFET and VSYS output voltages that realize an ultralow shutdown current. In addition, during shipment mode, the PGOOD1, PGOOD2, and RESET pins have a high output by default.

Enable shipment mode at initial power up of the ADP5360 by pulling up the ENSD pin. To disable shipment mode, pull down the ENSD pin.

In the case where the VBUS voltage goes higher than the UVLO or the MR pin for t_{SH} is pulled down, the ADP5360 exits shipment mode. To re-enter shipment mode, set the EN_SHIPMODE bit, Address 0x36, to high or pull down the MR pin for 12 seconds.

Note that the EN_MR_SD bit, Address 0x2D must be set to enable the MR shipment function.

FAULT RECOVERY

Before performing fault recovery, ensure that the cause of the fault is rectified.

To recover from a fault status, power off the VBUS pin or write a high to the corresponding bits of the Fault register.

THERMAL MANAGEMENT

Thermal Shutdown

The ADP5360 features a shutdown threshold detector. If the die temperature exceeds T_{SD}, all functions are disabled, and the TSD110 bit, Address 0x2E, is set. The ADP5360 charger can be re-enabled when the die temperature drops lower than the T_{SD} falling limit, and the TSD110 bit is reset. To reset the TSD110 bit, write to the I^2C fault register, THERMISTOR_10C Threshold, Address 0x0D, or cycle the power.

I^{2}C INTERFACE

The ADP5360 includes an I^{2}C-compatible serial interface to control the battery charging, fuel gauge, buck, and buck boost, and to read back the system status.

I^{2}C ADDRESSES

The I^{2}C chip default address is 0x46. Different I^{2}C addresses can be factory programmable. Having different I^{2}C address options helps to avoid I^{2}C address conflicts with other I^{2}C slave chipsets in the system. For different I^{2}C chip address requirements, contact the local Analog Devices sales or distribution representative.

SDA AND SCL PINS

The ADP5360 has two dedicated I^{2}C interface pins, SDA and SCL. SDA is an open-drain line for receiving and transmitting data. SCL is an input line for receiving the clock signal. Pull up these pins to connect external input and output supplies using external resistors.

Serial data is transferred on the rising edge of SCL. The read data is generated at the SDA pin in read mode.

The subaddress content selects which of the ADP5360 registers is written to first. The ADP5360 sends an acknowledgement to the master after the 8-bit data byte is written (see Figure 56 for an example of the I^{2}C write sequence to a single register). The ADP5360 increments the subaddress automatically and starts receiving a data byte at the next register until the master sends an I^{2}C stop as shown in Figure 56.

INTERRUPTS

The ADP5360 provides an interrupt output ($\overline{\text{INT}}$ pin) for an interrupt case. During normal operation, the $\overline{\text{INT}}$ pin is pulled high using an external pull-up resistor. When an interrupt case occurs, the ADP5360 pulls the $\overline{\text{INT}}$ pin low to alert the I^{2}C host that an interrupt case has occurred.

Many different interrupt sources can trigger the $\overline{\text{INT}}$ pin. By default, no interrupt sources are configured. To select one or more interrupt sources to trigger the $\overline{\text{INT}}$ pin, set the corresponding bits to 1 in the INTERRUPT_ENABLE1 and INTERRUPT_ENABLE2 registers.

When the $\overline{\text{INT}}$ pin is triggered, the corresponding bits in the INTERRUPT_FLAG1 and INTERRUPT_FLAG2 registers are set to 1. The interrupt case that triggers the $\overline{\text{INT}}$ pin is read from the INTERRUPT_FLAG1 and INTERRUPT_FLAG2 registers.

To clear an interrupt, write a 1 to the corresponding bit in the INTERRUPT_FLAG1 and INTERRUPT_FLAG2 registers. Otherwise, the ADP5360 power recycles. Reading the interrupt or writing a 0 to the bit does not clear the interrupt.

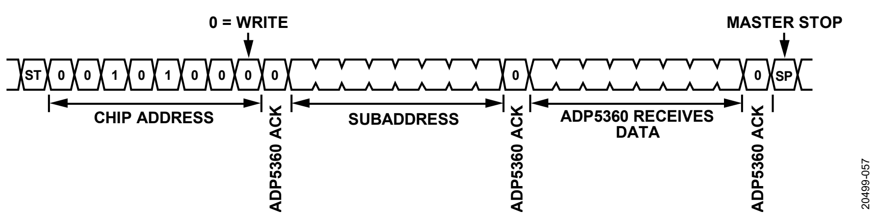


Figure 56. I^{2}C Single Register Write Sequence

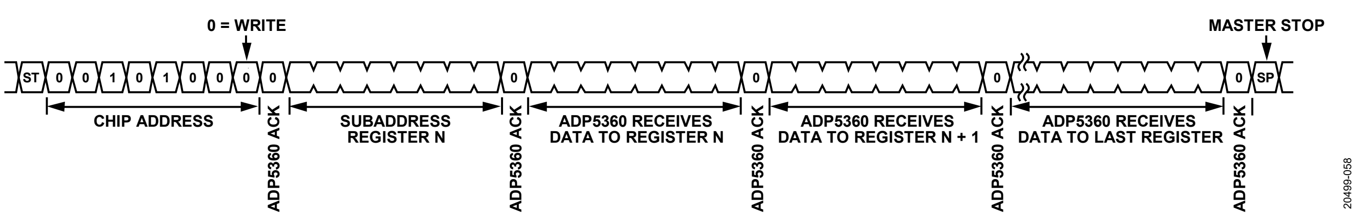


Figure 57. I^{2}C Multiple Register Write Sequence

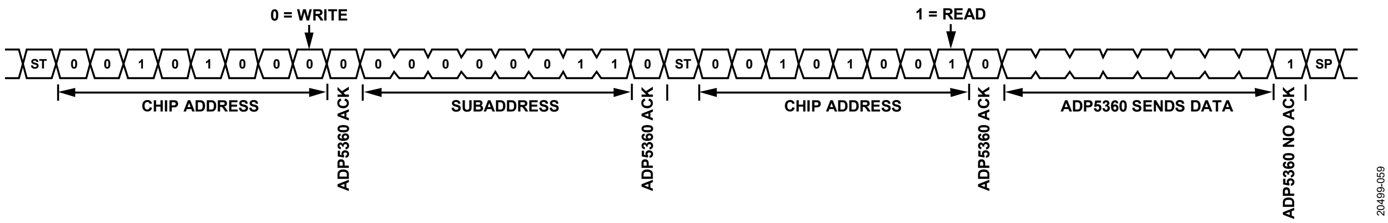


Figure 58. I²C Single Register Read Sequence

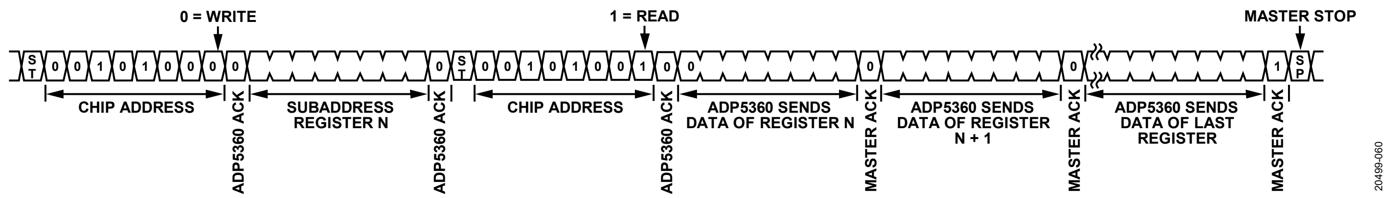


Figure 59. I²C Multiple Register Read Sequence

CONTROL REGISTER MAP

Table 17. Register Map

Address (Hex)	Register Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	Manufacture and Model ID	[7:0]	MANUF[3:0]				MODEL[3:0]			
0x01	Silicon Revision	[7:0]	Reserved				REV[3:0]			
0x02	CHARGER_ VBUS_ILIM	[7:0]	VADPICHG[2:0]			Reserved	VSYSTEM	ILIM[2:0]		
0x03	CHARGER_ TERMINATION_ SETTING	[7:0]	VTRM[5:0]						ITRK_DEAD[1:0]	
0x04	CHARGER_ CURRENT_ SETTING	[7:0]	IEND[2:0]			ICHG[4:0]				
0x05	CHARGER_ VOLTAGE_ THRESHOLD	[7:0]	DIS_RCH	VRCH[1:0]		VTRK_DEAD[1:0]		VWEAK[2:0]		
0x06	CHARGER_ TIMER_ SETTING	[7:0]	Reserved				EN_TEND	EN_CHG_ TIMER	CHG_TMR_PERIOD[1:0]	
0x07	CHARGER_ FUNCTION_ SETTING	[7:0]	EN_JEITA	ILIM_ JEITA_ COOL	Reserved	OFF_ISOFET	EN_LDO	EN_EOC	EN_ ADPICHG	EN_CHG
0x08	CHARGER_ STATUS1	[7:0]	VBUS_OV	ADPICHG	VBUS_ILIM	Reserved		CHARGER_STATUS[2:0]		
0x09	CHARGER_ STATUS2	[7:0]	THR_STATUS[2:0]			BAT_OV_ STATUS	BAT_UV_ STATUS	BAT_CHG_STATUS[2:0]		
0x0A	BATTERY_ THERMISTOR_ CONTROL	[7:0]	ITHR[1:0]		Reserved					EN_THR
0x0B	THERMISTOR_ 60C Threshold	[7:0]	TEMP_HIGH_60[7:0]							
0x0C	THERMISTOR_ 45C Threshold	[7:0]	TEMP_HIGH_45[7:0]							
0x0D	THERMISTOR_ 10C Threshold	[7:0]	TEMP_LOW_10[7:0]							
0x0E	THERMISTOR_ 0C Threshold	[7:0]	TEMP_LOW_0[7:0]							
0x0F	THR_VOLTAGE Low	[7:0]	THR_V_LOW[7:0]							
0x10	THR_VOLTAGE High	[7:0]	Reserved				THR_V_HIGH[11:8]			
0x11	Battery Protection Control	[7:0]	Reserved			ISOFET_ OVCHG	OC_DIS_ HICCUP	OC_CHG_ HICCUP	EN_ CHGLB	EN_ BATPRO
0x12	Battery Protection Undervoltage Setting	[7:0]	UV_DISCH[3:0]				HYS_UV_DISCH[1:0]		DGT_UV_DISCH[1:0]	
0x13	Battery Protection Overcharge Setting	[7:0]	OC_DISCH[2:0]			Reserved	DGT_OC_DISCH[2:0]			Reserved

Address (Hex)	Register Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x14	Battery Protection Overvoltage Setting	[7:0]	OV_CHG[4:0]					HYS_OV_CHG[1:0]		DGT_OV_CHG
0x15	Battery Protection Charge Overcharge Setting	[7:0]	OC_CHG[2:0]			DGT_OC_CHG[1:0]		Reserved		
0x16	V_SOC_0	[7:0]	V_SOC_0[7:0]							
0x17	V_SOC_5	[7:0]	V_SOC_5[7:0]							
0x18	V_SOC_11	[7:0]	V_SOC_11[7:0]							
0x19	V_SOC_19	[7:0]	V_SOC_19[7:0]							
0x1A	V_SOC_28	[7:0]	V_SOC_28[7:0]							
0x1B	V_SOC_41	[7:0]	V_SOC_41[7:0]							
0x1C	V_SOC_55	[7:0]	V_SOC_55[7:0]							
0x1D	V_SOC_69	[7:0]	V_SOC_69[7:0]							
0x1E	V_SOC_84	[7:0]	V_SOC_84[7:0]							
0x1F	V_SOC_100	[7:0]	V_SOC_100[7:0]							
0x20	BAT_CAP	[7:0]	BAT_CAP[7:0]							
0x21	BAT_SOC	[7:0]	Reserved	BAT_SOC[6:0]						
0x22	BAT_SOCACM_CTL	[7:0]	BATCAP_AGE[1:0]		BATCAP_TEMP[1:0]		Reserved		EN_BATCAP_TEMP	EN_BATCAP_AGE
0x23	BAT_SOCACM_H	[7:0]	BAT_SOCACM[11:4]							
0x24	BAT_SOCACM_L	[7:0]	BAT_SOCACM[3:0]				Reserved			
0x25	VBAT_READ_H	[7:0]	VBAT_READ[12:5]							
0x26	VBAT_READ_L	[7:0]	VBAT_READ[4:0]					Reserved		
0x27	FUEL_GAUGE_MODE	[7:0]	SOC_LOW_TH[1:0]		SLP_CURR[1:0]		SLP_TIME[1:0]		FG_MODE	EN_FG
0x28	SOC_RESET	[7:0]	SOC_RESET	Reserved						
0x29	Buck Configure	[7:0]	BUCK_SS[1:0]		BUCK_ILIM[1:0]		BUCK_MODE	STP_BUCK	DISCHG_BUCK	EN_BUCK
0x2A	Buck Output Voltage Setting	[7:0]	BUCK_DLY[1:0]		VOUT_BUCK[5:0]					
0x2B	Buck Boost Configure	[7:0]	BUCKBST_SS[1:0]		BUCKBST_ILIM[2:0]			STP_BUCKBST	DISCHG_BUCKBST	EN_BUCKBST
0x2C	Buck Boost Output Voltage Setting	[7:0]	BUCKBST_DLY[1:0]		VOUT_BUCKBST[5:0]					
0x2D	Supervisory Setting	[7:0]	VOUT1_RST	VOUT2_RST	RESET_TIME	WD_TIME[1:0]		EN_WD	EN_MR_SD	RESET_WD
0x2E	Fault	[7:0]	BAT_UV	BAT_OC	BAT_CHGOC	BAT_CHGOV	Reserved	WD_TIMEOUT	Reserved	TSD110
0x2F	PGOOD_STATUS	[7:0]	Reserved		MR_PRESS	CHG_CMPLT	VBUSOK	BATOK	VOUT2OK	VOUT1OK
0x30	PGOOD1_MASK	[7:0]	PG1_REV	Reserved		CHGCMPLT_MASK1	VBUSOK_MASK1	BATOK_MASK1	VOUT2OK_MASK1	VOUT1OK_MASK1
0x31	PGOOD2_MASK	[7:0]	PG2_REV	Reserved		CHGCMPLT_MASK2	VBUSOK_MASK2	BATOK_MASK2	VOUT2OK_MASK2	VOUT1OK_MASK2

Address (Hex)	Register Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x32	INTERRUPT_ ENABLE1	[7:0]	EN_ SOCLOW_ INT	EN_ SOCACM_ INT	EN_ ADPICHG_ INT	EN_ BATPRO_INT	EN_THR_ INT	EN_BAT_ INT	EN_CHG_ INT	EN_ VBUS_INT
0x33	INTERRUPT_ ENABLE2	[7:0]	EN_MR_ INT	EN_WD_ INT	EN_ BUCKPG_ INT	EN_ BUCKBSTPG_ INT	Reserved			
0x34	INTERRUPT_ FLAG1	[7:0]	SOCLOW_ INT	SOCACM_ INT	ADPICHG_ INT	BATPRO_INT	THR_INT	BAT_INT	CHG_INT	VBUS_INT
0x35	INTERRUPT_ FLAG2	[7:0]	MR_INT	WD_INT	BUCKPG_ INT	BUCKBSTPG_ INT	Reserved			
0x36	SHIPMODE	[7:0]	Reserved							EN_ SHIPMODE

Table 18. Manufacturer and Model ID, Address 0x00 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:4]	MANUF[3:0]	R	0001	The 4-bit manufacturer identification bus.
[3:0]	MODEL[3:0]	R	0000	The 4-bit model identification bus.

Table 19. Silicon Revision, Address 0x01 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:4]	Reserved	R	Not applicable	Reserved.
[3:0]	REV[3:0]	R	1000	The 4-bit silicon revision identification bus.

Table 20. CHARGER_VBUS_ILIM, Address 0x02 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:5]	VADPICHG[2:0]	R/W	100 = 4.6 V	Adaptive Current Limit to VBUS Voltage Threshold Programming. The current to the VBUS voltage threshold can be limited to the following programmed values: 010 = 4.4 V. 011 = 4.5 V. 100 = 4.6 V. 101 = 4.7 V. 110 = 4.8 V. 111 = 4.9 V.
4	Reserved	R	Not applicable	Reserved.
3	VSYSTEM	R/W	0 = V_{TRM} + 200 mV	VSYS Voltage Programming. 0 = V_{TRM} + 200 mV. 1 = 5 V.
[2:0]	ILIM[2:0]	R/W	001 = 100 mA	VBUS Pin Input Current-Limit Programming Bus. The current into the VBUS pin can be limited to the following programmed values: 000 = 50 mA. 001 = 100 mA. 010 = 150 mA. 011 = 200 mA. 100 = 250 mA. 101 = 300 mA. 110 = 400 mA. 111 = 500 mA.

Table 21. CHARGER_TERMINATION_SETTING, Address 0x03 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:2]	VTRM[5:0]	R/W	Factory set	Termination Voltage Programming Bus. The values of the float voltage can be programmed by using the following values: 000000 = 3.56 V. 000001 = 3.58 V. 000010 = 3.60 V. 000011 = 3.62 V. 000100 = 3.64 V. 000101 = 3.66 V. 000110 = 3.68 V. 000111 = 3.70 V. 001000 = 3.72 V. 001001 = 3.74 V. 001010 = 3.76 V. 001011 = 3.78 V. 001100 = 3.80 V. 001101 = 3.82 V. 001110 = 3.84 V. 001111 = 3.86 V. 010000 = 3.88 V. 010001 = 3.90 V. 010010 = 3.92 V. 010011 = 3.94 V. 010100 = 3.96 V. 010101 = 3.98 V. 010110 = 4.00 V. 010111 = 4.02 V. 011000 = 4.04 V. 011001 = 4.06 V. 011010 = 4.08 V. 011011 = 4.10 V. 011100 = 4.12 V. 011101 = 4.14 V. 011110 = 4.16 V. 011111 = 4.18 V. 100000 = 4.20 V. 100001 = 4.22 V. 100010 = 4.24 V. 100011 = 4.26 V. 100100 = 4.28 V. 100101 = 4.30 V. 100110 = 4.32 V. 100111 = 4.34 V. 101000 = 4.36 V. 101001 = 4.38 V. 101010 = 4.40 V. 101011 = 4.42 V. 101100 = 4.44 V. 101101 = 4.46 V. 101110 = 4.48 V. 101111 = 4.50 V.

Bit(s)	Bit Name	Access	Default	Description
				110000 = 4.52 V. 110001 = 4.54 V. 110010 = 4.56 V. 110011 = 4.58 V. 110100 = 4.60 V. 110101 = 4.62 V. 110110 = 4.64 V. 110111 to 111111 = 4.66 V.
[1:0]	ITRK_DEAD[1:0]	R/W	10 = 5 mA	Trickle and Weak Charge Current Programming Bus. The values of the trickle and weak charge currents can be programmed by using the following values: 00 = 1 mA. 01 = 2.5 mA. 10 = 5 mA. 11 = 10 mA.

Table 22. CHARGER_CURRENT_SETTING, Address 0x04 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:5]	IEND[2:0]	R/W	001 = 5 mA	Termination Current Programming Bus. The values of the termination current can be programmed by using the following values: 001 = 5 mA. 010 = 7.5 mA. 011 = 12.5 mA. 100 = 17.5 mA. 101 = 22.5 mA. 110 = 27.5 mA. 111 = 32.5 mA.
[4:0]	ICHG[4:0]	R/W	01001 = 100 mA	Fast Charge Current Programming Bus. The values of the constant current charge can be programmed by using the following values: 00000 = 10 mA. 00001 = 20 mA. 00010 = 30 mA. 00011 = 40 mA. 00100 = 50 mA. 00101 = 60 mA. 00110 = 70 mA. 00111 = 80 mA. 01000 = 90 mA. 01001 = 100 mA. 01010 = 110 mA. 01011 = 120 mA. 01100 = 130 mA. 01101 = 140 mA. 01110 = 150 mA. 01111 = 160 mA. 10000 = 170 mA. 10001 = 180 mA. 10010 = 190 mA. 10011 = 200 mA. 10100 = 210 mA. 10101 = 220 mA. 10110 = 230 mA.

Bit(s)	Bit Name	Access	Default	Description
				10111 = 240 mA. 11000 = 250 mA. 11001 = 260 mA. 11010 = 270 mA. 11011 = 280 mA. 11100 = 290 mA. 11101 = 300 mA. 11110 = 310 mA. 11111 = 320 mA.

Table 23. CHARGER_VOLTAGE_THRESHOLD, Address 0x05 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
7	DIS_RCH		0 = Enable recharge	Recharge Function Disable. 0 = recharge enable. 1 = recharge disable.
[6:5]	VRCH[1:0]	R/W	01 = 120 mV	Recharge Voltage Programming Bus. The values of the recharge threshold can be programmed by using the following values: 01 = 120 mV. 10 = 180 mV. 11 = 240 mV.
[4:3]	VTRK_DEAD[1:0]	R/W	01 = 2.5 V	Trickle to Fast Charge Dead Battery Voltage Programming Bus. The values of the trickle to fast charge threshold can be programmed by using the following values: 00 = 2.0 V. 01 = 2.5 V. 10 = 2.6 V. 11 = 2.9 V.
[2:0]	VWEAK[2:0]	R/W	011 = 3.0 V	Weak Battery Voltage Rising Threshold. The values of the battery voltage can be programmed by using the following values: 000 = 2.7 V. 001 = 2.8 V. 010 = 2.9 V. 011 = 3.0 V. 100 = 3.1 V. 101 = 3.2 V. 110 = 3.3 V. 111 = 3.4 V.

Table 24. CHARGER_TIMER_SETTING, Address 0x06 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:4]	Reserved	R	Not applicable	Reserved.
3	EN_TEND	R/W	0	When low, this bit disables the charge complete timer (t_{END}), and a 32 ms deglitch timer (t_{DG}) remains on this function.
2	EN_CHG_TIMER	R/W	1	When high, the trickle charge timer (t_{TRK}) and the fast charge timer (t_{CHG}) are enabled. When low, t_{TRK} and t_{CHG} are disabled.
[1:0]	CHG_TMR_PERIOD[1:0]	R/W	11	t_{TRK} and t_{CHG} Period. 00 = 15 minutes/150 minutes. 01 = 30 minutes/300 minutes. 10 = 45 minutes/450 minutes. 11 = 60 minutes/600 minutes.

Table 25. CHARGER_FUNCTION_SETTING, Address 0x07 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
7	EN_JEITA	R/W	0	When low, this bit disables the JEITA Li-Ion temperature battery charging specification.
6	ILIM_JEITA_COOL	R/W	0	When in temperature cool mode, select the battery charging current. 0 = approximately 50% of programmed charge current. 1 = approximately 10% of programmed charge current.
5	Reserved	R/W	Not applicable	Reserved.
4	OFF_ISOFET	R/W	0	When high, ISOFET is forced to turn off, and VSYS is shut down only when the battery is present.
3	EN_LDO	R/W	1	When low, the charge LDO is disabled. When high, the charge LDO is enabled.
2	EN_EOC	R/W	1	When high, end of charge is allowed.
1	EN_ADPICHG	R/W	0	When high, the VBUS adaptive current-limit function is enabled during charging. When low, the VBUS adaptive current-limit function is disabled during charging.
0	EN_CHG	R/W	Factory set	When low, charging is disabled. When high and EN_LDO = high, charging is enabled.

Table 26. CHARGER_STATUS1, Address 0x08 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
7	VBUS_OV	R	Not applicable	When high, this bit indicates that the VBUS voltage is over the threshold of V_{VBUS_OK}.
6	ADPICHG	R	Not applicable	When high, this bit indicates that the adaptive charge current is active.
5	VBUS_ILIM	R	Not applicable	When high, this bit indicates that the current into the VBUS pin is limited by the high voltage blocking FET and that the charger is not running at the full programmed I_{CHG}.
[4:3]	Reserved	R	Not applicable	Reserved.
[2:0]	CHARGER_STATUS[2:0]	R	Not applicable	Charger Status Bus. The following values are indications for the charger status: 000 = off. 001 = trickle charge. 010 = fast charge (constant current mode). 011 = fast charge (constant voltage mode). 100 = charge complete. 101 = LDO mode. 110 = trickle or fast charge timer expired. 111 = battery detection.

Table 27. CHARGER_STATUS2, Address 0x09 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:5]	THR_STATUS[2:0]	R	Not applicable	THR Pin Status. The following values are indications for the THR pin NTC resistor value: 000 = off. 001 = battery cold. 010 = battery cool. 011 = battery warm. 100 = battery hot. 111 = thermistor okay.
4	BAT_OV_STATUS	R	Not applicable	Battery Overvoltage Status. 0 = no battery overvoltage protection. 1 = battery overvoltage protection.
3	BAT_UV_STATUS	R	Not applicable	Battery Undervoltage Status. 0 = no battery undervoltage protection. 1 = battery undervoltage protection.

Bit(s)	Bit Name	Access	Default	Description
[2:0]	BAT_CHG_STATUS[2:0]	R	Not applicable	Battery Status Bus. The following values are indications for battery status: 000 = normal. 001 = no battery. 010 = $V_{BSNS} < V_{TRK\_DEAD}$ when in charge. 011 = $V_{TRK} \leq V_{BSNS} < V_{WEAK}$ when in charge. 100 = $V_{BSNS} \geq V_{WEAK}$ when in charge.

Table 28. BATTERY_THERMISTOR_CONTROL, Address 0x0A Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:6]	ITHR[1:0]	R/W	Factory set	Select Battery Thermistor NTC Resistance. The following values are the program values for the battery thermistor NTC resistance: 00 = 60 μA. 01 = 12 μA. 10, 11 = 6 μA.
[5:1]	Reserved	R	Not applicable	Reserved.
0	EN_THR	R/W	0	When high, the ITHR current source is enabled even when the voltage at the VBUS pin is lower than V_{VBUS_OK}.

Table 29. THERMISTOR_60C Threshold, Address 0x0B Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:0]	TEMP_HIGH_60[7:0]	R/W	0x56	Thermistor Voltage Threshold for 60°C. THERMISTOR_60C Voltage Threshold (V) = (TEMP_HIGH_60 × 0.002) (V)

Table 30. THERMISTOR_45C Threshold, Address 0x0C Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:0]	TEMP_HIGH_45[7:0]	R/W	0x8F	Thermistor Voltage Threshold for 45°C THERMISTOR_45C Voltage Threshold (V) = (TEMP_HIGH_45 × 0.002) (V)

Table 31. THERMISTOR_10C Threshold, Address 0x0D Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:0]	TEMP_LOW_10[7:0]	R/W	0x71	Thermistor Voltage Threshold for 10°C THERMISTOR_10C Voltage Threshold (V) = (TEMP_LOW_10 × 0.01) (V)

Table 32. THERMISTOR_0C Threshold, Address 0x0E Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:0]	TEMP_LOW_0[7:0]	R/W	0xB4	Thermistor Voltage Threshold For 0°C THERMISTOR_0C Voltage Threshold (V) = (TEMP_LOW_0 × 0.01) (V)

Table 33. THR_VOLTAGE Low, Address 0x0F Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:0]	THR_V_LOW[7:0]	R	Not applicable	8-Bit Thermistor Node Voltage Low (mV) NTC = THR_V_x[11:0]/ITHR (kΩ)

Table 34. THR_VOLTAGE High, Address 0x10 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:4]	Reserved	R	Not applicable	Reserved
[3:0]	THR_V_HIGH[11:8]	R	Not applicable	4-Bit Thermistor Node Voltage High (mV) NTC = THR_V_x[11:0]/ITHR (kΩ)

Table 35. Battery Protection Control, Address 0x11 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:5]	Reserved	R	Not applicable	Reserved.
4	ISOFET_OVCHG	R/W	0	When low, ISOFET turns on when the battery charging overvoltage protection is triggered. When high, the ISOFET turns off when the battery charging overvoltage protection is triggered.
3	OC_DIS_HICCUP	R/W	0	Battery Discharge Overcurrent Protection Mode Selection. 0 = latch up. 1 = hiccup.
2	OC_CHG_HICCUP	R/W	0	Battery Charge Overcurrent Protection Mode Selection. 0 = latch up. 1 = hiccup.
1	EN_CHGLB	R/W	1	When low, the battery charge is not allowed with the battery undervoltage protection triggered. When high, the battery charge is allowed with the battery undervoltage protection triggered.
0	EN_BATPRO	R/W	Factory set	When low, the battery protection function is disabled. When high, the battery protection function is enabled.

Table 36. Battery Protection Undervoltage Setting, Address 0x12 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:4]	UV_DISCH[3:0]	R/W	Factory set	Battery Undervoltage Protection Threshold. The values of the battery undervoltage protection threshold can be programmed by using the following values: 0000 = 2.05 V. 0001 = 2.10 V. 0010 = 2.15 V. 0011 = 2.20 V. 0100 = 2.25 V. 0101 = 2.30 V. 0110 = 2.35 V. 0111 = 2.40 V. 1000 = 2.45 V. 1001 = 2.50 V. 1010 = 2.55 V. 1011 = 2.60 V. 1100 = 2.65 V. 1101 = 2.70 V. 1110 = 2.75 V. 1111 = 2.80 V.
[3:2]	HYS_UV_DISCH[1:0]	R/W	00 = 2%	Battery Undervoltage Protection for Overdischarge Hysteresis. The values of the battery undervoltage protection can be programmed byusing the following values: 00 = 2% UV_DISCH voltage threshold. 01 = 4% UV_DISCH voltage threshold. 10 = 6% UV_DISCH voltage threshold. 11 = 8% UV_DISCH voltage threshold.
[1:0]	DGT_UV_DISCH[1:0]	R/W	00 = 30 ms	Battery Undervoltage Protection Deglitch Time. The values of the battery undervoltage protection deglitch time can be programmed by using the following values: 00 = 30 ms. 01 = 60 ms. 10 = 120 ms. 11 = 240 ms.

Table 37. Battery Protection Overcharge Setting, Address 0x13 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:5]	OC_DISCH[2:0]	R/W	Factory set	Battery Overcurrent Protection for Overdischarge Threshold. The values of the battery overcurrent protection can be programmed by using the following values: 000 = 50 mA. 001 = 100 mA. 010 = 150 mA. 011 = 200 mA. 100 = 300 mA. 101 = 400 mA. 110 = 500 mA. 111 = 600 mA.
4	Reserved	R	Not applicable	Reserved
[3:1]	DGT_OC_DISCH[2:0]	R/W	011 = 5 ms	Battery Discharge Overcurrent Protection Deglitch Time Setting. The values of the battery discharge overcurrent protection can be programmed by using the following values: 001 = 0.5 ms. 010 = 1 ms. 011 = 5 ms. 100 = 10 ms. 101 = 20 ms. 110 = 50 ms. 111 = 100 ms.
0	Reserved	R	Not applicable	Reserved

Table 38. Battery Protection Overvoltage Setting, Address 0x14 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:3]	OV_CHG[4:0]	R/W	Factory set	Battery Overvoltage Protection Threshold. The values of the battery overvoltage protection threshold can be programmed by using the following values: 00000 = 3.55 V. 00001 = 3.60 V. 00010 = 3.65 V. 00011 = 3.70 V. 00100 = 3.75 V. 00101 = 3.80 V. 00110 = 3.85 V. 00111 = 3.90 V. 01000 = 3.95 V. 01001 = 4.00 V. 01010 = 4.05 V. 01011 = 4.10 V. 01100 = 4.15 V. 01101 = 4.20 V. 01110 = 4.25 V. 01111 = 4.30 V. 10000 = 4.35 V. 10001 = 4.40 V. 10010 = 4.45 V. 10011 = 4.50 V.

Bit(s)	Bit Name	Access	Default	Description
				10100 = 4.55 V. 10101 = 4.60 V. 10110 = 4.65 V. 10111 = 4.70 V. 11000 = 4.75 V. 11001 to 11111 = 4.80 V.
[2:1]	HYS_OV_CHG[1:0]	R/W	00	Battery Overvoltage Protection for Charge Hysteresis. The values of the battery overvoltage protection can be programmed by using the following values: 00 = 2% of the voltage of the OV_CHG threshold. 01 = 4% of the voltage of the OV_CHG threshold. 10 = 6% of the voltage of the OV_CHG threshold. 11 = 8% of the voltage of the OV_CHG threshold.
0	DGT_OV_CHG	R/W	0 = 0.5 sec	Battery Overvoltage Protection Deglitch Time. The values of the battery overvoltage protection deglitch time can be programmed by using the following values: 0 = 0.5 sec. 1 = 1 sec.

Table 39. Battery Protection Charge Overcharge Setting, Address 0x15 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:5]	OC_CHG[2:0]	R/W	Factory set	Battery Overcurrent Protection for Overdischarge Threshold. The values of the battery overcurrent protection can be programmed by using the following values: 000 = 25 mA. 001 = 50 mA. 010 = 100 mA. 011 = 150 mA. 100 = 200 mA. 101 = 250 mA. 110 = 300 mA. 111 = 400 mA.
[4:3]	DGT_OC_CHG[1:0]	R/W	01 = 10 ms	Battery Charge Overcurrent Protection Deglitch Time Setting. The values of the battery charge overcurrent protection can be programmed byusing the following values: 00 = 5 ms. 01 = 10 ms. 10 = 20 ms. 11 = 40 ms.
[2:0]	Reserved	R	Not applicable	Reserved.

FUEL GAUGE REGISTER BIT DESCRIPTIONS

Table 40. V_SOC_0, Address 0x16 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:0]	V_SOC_0[7:0]	R/W	0x7D	Battery Voltage When State of Charge = 0%. The default voltage is 3.5 V. Battery Voltage (V) = (2.5 + V_SOC_0 × 0.008) (V).

Table 41. V_SOC_5, Address 0x17 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:0]	V_SOC_5[7:0]	R/W	0x91	Battery Voltage When State of Charge = 5%. The default voltage is 3.66 V. Battery voltage (V) = (2.5 + V_SOC_5 × 0.008) (V).

Table 42. V_SOC_11, Address 0x18 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:0]	V_SOC_11[7:0]	R/W	0x94	Battery Voltage When State of Charge = 11%. The default voltage is 3.684 V. Battery voltage (V) = (2.5 + V_SOC_11 × 0.008) (V).

Table 43. V_SOC_19, Address 0x19 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:0]	V_SOC_19[7:0]	R/W	0x99	Battery Voltage When State of Charge = 19%. The default voltage is 3.724 V. Battery voltage (V) = (2.5 + V_SOC_19 × 0.008) (V).

Table 44. V_SOC_28, Address 0x1A Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:0]	V_SOC_28[7:0]	R/W	0x9E	Battery Voltage When State of Charge = 28%. The default voltage is 3.764 V. Battery Voltage (V) = (2.5 + V_SOC_28 × 0.008) (V).

Table 45. V_SOC_41, Address 0x1B Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:0]	V_SOC_41[7:0]	R/W	0xA3	Battery Voltage When State of Charge = 41%. The default voltage is 3.804 V. Battery Voltage (V) = (2.5 + V_SOC_41 × 0.008) (V).

Table 46. V_SOC_55, Address 0x1C Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:0]	V_SOC_55[7:0]	R/W	0xAB	Battery Voltage When State of Charge = 55%. The default voltage is 3.868 V. Battery Voltage (V) = (2.5 + V_SOC_55 × 0.008) (V).

Table 47. V_SOC_69, Address 0x1D Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:0]	V_SOC_69[7:0]	R/W	0xB5	Battery Voltage When State of Charge = 69%. The default voltage is 3.948 V. Battery Voltage (V) = (2.5 + V_SOC_69 × 0.008) (V).

Table 48. V_SOC_84, Address 0x1E Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:0]	V_SOC_84[7:0]	R/W	0xC4	Battery Voltage When State of Charge = 84%. The default voltage is 4.068 V. Battery Voltage (V) = (2.5 + V_SOC_84 × 0.008) (V).

Table 49. V_SOC_100, Address 0x1F Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:0]	V_SOC_100[7:0]	R/W	0xD5	Battery Voltage When State of Charge = 100%. The default voltage is 4.204 V. Battery Voltage (V) = (2.5 + V_SOC_100 × 0.008) (V).

Table 50. BAT_CAP, Address 0x20 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:0]	BAT_CAP[7:0]	R/W	0x32	Battery Capacity Input Battery Capacity = (BAT_CAP × 2) mAh

Table 51. BAT_SOC, Address 0x21 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
7	Reserved	R	Not applicable	Reserved
[6:0]	BAT_SOC[6:0]	R	Not applicable	Battery State of Charge Output State of Charge = BAT_SOC %, Only Valued Between 0% to 100%

Table 52. BAT_SOCACM_CTL, Address 0x22 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:6]	BATCAP_AGE[1:0]	R/W	01 = 1.5%	Battery Capacity Reduction Percentage When BAT_SOCACM Overflows. 00 = 0.8 %. 01 = 1.5 %. 10 = 3.1 %. 11 = 6.3 %.
[5:4]	BATCAP_TEMP[1:0]	R/W	00 = 0.2%/°C	Battery Capacity Compensation with Temperature Coefficient. The values of the battery capacity compensation can be programmed by using the following values: 00 = 0.2 %/°C. 01 = 0.4 %/°C. 10 = 0.6 %/°C. 11 = 0.8 %/°C.
[3:2]	Reserved		Not applicable	Reserved.
1	EN_BATCAP_TEMP	R/W	0	Battery Capacity Temperature Compensation Function Selection. 0 = disable battery capacity temperature compensation. 1 = enable battery capacity temperature compensation.
0	EN_BATCAP_AGE	R/W	0	Battery Capacity Aging Compensation Function Selection. 0 = disable battery capacity aging automatic adjustment. 1 = enable battery capacity aging automatic adjustment.

Table 53. BAT_SOCACM_H, Address 0x23 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:0]	BAT_SOCACM[11:4]	R	Not applicable	Highest Eight Bits of an 8-Bit Accumulation of the Charge State Number of Times for Charging = BAT_SOCACM[11:0]/100

Table 54. BAT_SOCACM_L, Address 0x24 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:4]	BAT_SOCACM[3:0]	R	Not applicable	Lowest Four Bits of a 4-Bit Accumulation of the Charge State Number of Times for Charging = BAT_SOCACM[11:0]/100
[3:0]	Reserved	R	Not applicable	Reserved

Table 55. VBAT_READ_H, Address 0x25 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:0]	VBAT_READ[12:5]	R	Not applicable	Battery Voltage Reading of the Highest Eight Bits (mV)

Table 56. VBAT_READ_L, Address 0x26 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:3]	VBAT_READ[4:0]	R	Not applicable	Battery Voltage Reading of the Lowest Five Bits (mV)
[2:0]	Reserved	R	Not applicable	Reserved

Table 57. FUEL_GAUGE_MODE, Address 0x27 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:6]	SOC_LOW_TH[1:0]	R/W	01 = 11%	Indication of Low State of Charge Threshold 00 = 6% 01 = 11% 10 = 21% 11 = 31%
[5:4]	SLP_CURR[1:0]	R/W	01 = 10 mA	Fuel Gauge Sleep Mode Current Threshold 00 = 5 mA 01 = 10 mA 10 = 20 mA 11 = 40 mA

Bit(s)	Bit Name	Access	Default	Description
[3:2]	SLP_TIME[1:0]	R/W	00 = 1 min	Fuel Gauge Update Rate Of The Sleep Mode 00 = 1 min 01 = 4 min 10 = 8 min 11 = 16 min
1	FG_MODE	R/W	0	Fuel Gauge Operation Mode Selection 1 = operate in sleep mode 0 = operate in active mode
0	EN_FG	R/W	0	Fuel Gauge Function Selection 0 = disable fuel gauge 1 = enable fuel gauge

Table 58. SOC_RESET, Address 0x28 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
7	SOC_RESET	W	0	Write 1, then write 0 to refresh the BAT_SOC, VBAT_READ_H, and VBAT_READ_L registers.
[6:0]	Reserved	R	Not applicable	Reserved.

SWITCHING REGULATOR REGISTER BIT DESCRIPTIONS

Table 59. Buck Configure, Address 0x29 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:6]	BUCK_SS[1:0]	R/W	Factory set	Buck Regulator Output Soft Start Time. The values of the soft start time can be programmed by using the following values: 00 = 1 ms. 01 = 8 ms. 10 = 64 ms. 11 = 512 ms.
[5:4]	BUCK_ILIM[1:0]	R/W	11 = 400 mA	Buck Regulator Peak Current Limit. The values of the peak current limit can be programmed by using the following values: 00 = 100 mA. 01 = 200 mA. 10 = 300 mA. 11 = 400 mA.
3	BUCK_MODE	R/W	Factory set	Buck Operate Mode Selection. 0 = hystersis mode. 1 = FPWM mode.
2	STP_BUCK	R/W	0 = disable	Enable Stop Feature to Buck Regulator. 0 = disable pulse stop feature. 1 = enable pulse stop feature.
1	DISCHG_BUCK	R/W	Factory set	Configure Output Discharge Functionality for Buck. 0 = disable output discharge function. 1 = enable output discharge function.
0	EN_BUCK	R/W	Factory set	Buck Output Control. 0 = disable buck output. 1 = enable buck output.

Table 60. Buck Output Voltage Setting, Address 0x2A Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:6]	BUCK_DLY[1:0]	R/W	00 = 0 µs	Buck Switch Delay Time in Hysteresis. The values of the delay time can be programmed by using the following values: 00 = 0 µs. 01 = 5 µs. 10 = 10 µs. 11 = 20 µs.
[5:0]	VOUT_BUCK[5:0]	R/W	Factory set	Buck Output Voltage Setting. The values of the voltage setting can be programmed by using the following values: 000000 = 0.6 V. 000001 = 0.65 V. … 111111 = 3.75 V.

Table 61. Buck Boost Configure, Address 0x2B Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:6]	BUCKBST_SS[1:0]	R/W	Factory set	Buck Boost Regulator Output Soft Start Time. The values of the start time can be programmed byusing the following values: 00 = 1 ms. 01 = 8 ms. 10 = 64 ms. 11 = 512 ms.
[5:3]	BUCKBST_ILIM[2:0]	R/W	011 = 400 mA	Buck Boost Regulator Peak Current Limit. The values of the peak current limit can be programmed by using the following values: 000 = 100 mA. 001 = 200 mA. 010 = 300 mA. 011 = 400 mA. 100 = 500 mA. 101 = 600 mA. 110 = 700 mA. 111 = 800 mA.
2	STP_BUCKBST	R/W	0 = disable	Enable Stop Feature to Buck Boost Regulator. 0 = disable pulse stop feature. 1 = enable pulse stop feature.
1	DISCHG_BUCKBST	R/W	Factory set	Configure Output Discharge Functionality for Buck Boost. 0 = disable output discharge function. 1 = enable output discharge function.
0	EN_BUCKBST	R/W	Factory set	Buck Boost Output Control. 0 = disable buck boost output. 1 = enable buck boost output.

Table 62. Buck Boost Output Voltage Setting, Address 0x2C Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:6]	BUCKBST_DLY[1:0]	R/W	00 = 0 µs	Buck Boost Switch Delay Time in Hysteresis. The values of the delay time can be programmed by using the following values: 00 = 0 µs. 01 = 5 µs. 10 = 10 µs. 11 = 20 µs.

Bit(s)	Bit Name	Access	Default	Description
[5:0]	VOUT_BUCKBST[5:0]	R/W	Factory set	Buck Boost Output Voltage Setting. The values of the voltage setting can be programmed by using the following values: 000000 = 1.8 V with 100 mV step. 000001 = 1.9 V with 100 mV step. … 001011 = 2.9 V with 100 mV step. 001100 = 2.95 V with 50 mV step. … 111111 = 5.5 V with 50 mV step.

SUPERVISORY REGISTER BIT DESCRIPTIONS

Table 63. Supervisory Setting, Address 0x2D Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
7	VOUT1_RST	R/W	1	Buck Output Voltage Monitor to $\overline{\text{RESET}}$ Selection. 0 = disable buck voltage monitor to $\overline{\text{RESET}}$. 1 = enable buck voltage monitor to $\overline{\text{RESET}}$.
6	VOUT2_RST	R/W	0	Buck Boost Output Voltage Monitor to $\overline{\text{RESET}}$ Selection. 0 = disable buck boost voltage monitor to $\overline{\text{RESET}}$. 1 = snable buck boost voltage monitor to $\overline{\text{RESET}}$.
5	RESET_TIME	R/W	0 = 200 ms	$\overline{\text{RESET}}$ Timeout Period Selection. The values of the period selection can be programmed by using the following values: 0 = 200 ms. 1 = 1.6 sec.
[4:3]	WD_TIME[1:0]	R/W	00 = 12.5 sec	Watchdog Timeout Period Selection. The values of the period selection can be programmed by using the following values: 00 = 12.5 sec. 01 = 25.6 sec. 10 = 50 sec. 11 = 100 sec.
2	EN_WD	R/W	0 = disable	When high, the watchdog timer function is enabled. When low, the watchdog timer function is disabled.
1	EN_MR_SD	R/W	0 = disable	When high, the device enters shipment mode after $\overline{\text{MR}}$ presses low for 12 sec. When low, disable $\overline{\text{MR}}$ to enter shipment mode.
0	RESET_WD	W	0	When high, the watchdog safety timer resets. The RESET_WD bit is reset automatically.

STATUS AND FAULT REGISTER BIT DESCRIPTIONS

Table 64. Fault, Address 0x2E Bit Descriptions[1]

Bit(s)	Bit Name	Access	Default	Description
7	BAT_UV[1]	R/W	0	When high, this bit indicates that the battery is undervoltage when overdischarging.
6	BAT_OC[1]	R/W	0	When high, this bit indicates that the battery is overcurrent during overdischarge.
5	BAT_CHGOC[1]	R/W	0	When high, this bit indicates that the battery is overcurrent during overcharge.
4	BAT_CHGOV[1]	R/W	0	When high, this bit indicates that the battery is overvoltage during overcharge.
3	Reserved	R	Not applicable	Reserved.
2	WD_TIMEOUT[1]	R/W	0	When high, watchdog timeout occurred.
1	Reserved	R/W	0	Reserved.
0	TSD110[1]	R/W	0	When high, the temperature shutdown fault occurs.

[1] To reset the fault bits in the fault register, cycle power on the VBUS pin or write high to the corresponding bits of the fault register.

Table 65. PGOOD_STATUS Register, Address 0x2F Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:6]	Reserved	R	Not applicable	Reserved.
5	MR_PRESS	R	Not applicable	When high, this bit indicates that the $\overline{MR}$ pin is pulled to low after t_{DG}.
4	CHG_CMPLT	R	Not applicable	This bit shows battery charge complete. 0 = the charger is not in charge complete status. 1 = the charger is in charge complete status.
3	VBUSOK	R	Not applicable	This bit shows the real-time status of the VBUS pin voltage. 0 = the voltage of the VBUS pin is lower than V_{VBUS_OK} or higher than V_{VBUS_OV}. 1 = the voltage of the VBUS pin is higher than V_{VBUS_OK} and lower than V_{VBUS_OV}.
2	BATOK	R	Not applicable	This bit shows the real-time status of the battery voltage. This bit is only active when the fuel gauge function is enabled. 0 = battery voltage is less than V_{WEAK}. 1 = battery voltage is more than V_{WEAK}.
1	VOUT2OK	R	Not applicable	This bit shows real-time power good status for the buck boost regulator. This bit is only effective in buck boost standalone fixed output mode. 0 = buck boost regulator power-good status is low. 1 = buck boost regulator power-good status is high.
0	VOUT1OK	R	Not applicable	This bit shows real-time power-good status for the buck regulator. This bit is not effective if the buck is configured as load switch mode. 0 = buck power-good status is low. 1 = buck power-good status is high.

Table 66. PGOOD1_MASK Register, Address 0x30 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
7	PG1_REV	R/W	Factory set	This bit configures the active low output of the PGOOD1 pin. 0 = disable active low. 1 = enable active low.
[6:5]	Reserved		Not applicable	Reserved.
4	CHGCMPLT_MASK1	R/W	0	This bit configures the external PGOOD1 pin. 0 = does not send the output charger complete signal to the external PGOOD1 pin. 1 = sends the output charger complete signal to the external PGOOD1 pin.
3	VBUSOK_MASK1	R/W	Factory set	This bit configures the external PGOOD1 pin. 0 = does not send the output VBUS voltage status signal to the external PGOOD1 pin. 1 = sends the output VBUS voltage status signal to the external PGOOD1 pin.
2	BATOK_MASK1	R/W	0	This bit configures the external PGOOD1 pin. 0 = does not send the output battery voltage okay signal to the external PGOOD1 pin. 1 = sends the output battery voltage okay signal to the external PGOOD1 pin.
1	VOUT2OK_MASK1	R/W	0	This bit configures the external PGOOD1 pin for buck boost output. 0 = does not send the output buck boost PGOOD signal to the external PGOOD1 pin. 1 = sends the output buck boost PGOOD signal to the external PGOOD1 pin.
0	VOUT1OK_MASK1	R/W	Factory set	This bit configures the external PGOOD1 pin. This bit is not effective if the buck is configured in load switch mode. 0 = does not send the output buck PGOOD signal to the external PGOOD1 pin. 1 = sends the output buck PGOOD signal to the external PGOOD1 pin.

Table 67. PGOOD2_MASK Register, Address 0x31 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
7	PG2_REV	R/W	0	This bit configures the active low output of the PGOOD2 pin output. 0 = disable active low. 1 = enable active low.
[6:5]	Reserved		Not applicable	Reserved.
4	CHGCMPLT_MASK2	R/W	0	This bit configures the external PGOOD2 pin. 0 = does not send the output charger complete signal to the external PGOOD2 pin. 1 = sends the output charger complete signal to the external PGOOD2 pin.
3	VBUSOK_MASK2	R/W	0	This bit configures the external PGOOD2 pin. 0 = does not send the output VBUS voltage status signal to the external PGOOD2 pin. 1 = sends the output VBUS voltage status signal to the external PGOOD2 pin.
2	BATOK_MASK2	R/W	0	This bit configures the external PGOOD2 pin. 0 = does not send the output battery voltage okay signal to the external PGOOD2 pin. 1 = sends the output battery voltage okay signal to the external PGOOD2 pin.
1	VOUT2OK_MASK2	R/W	0	This bit configures the external PGOOD2 pin for buck boost output. 0 = does not send the output buck boost PGOOD signal to the external PGOOD2 pin. 1 = sends the output buck boost PGOOD signal to the external PGOOD2 pin.
0	VOUT1OK_MASK2	R/W	0	This bit configures the external PGOOD2 pin. This bit is not effective if the buck is configured in load switch mode. 0 = does not send the output buck PGOOD signal to the external PGOOD2 pin. 1 = sends the output buck PGOOD signal to the external PGOOD2 pin.

Table 68. INTERRUPT_ENABLE1 Register, Address 0x32 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
7	EN_SOCLOW_INT	R/W	0	When high, the battery low state of the charge interrupt is allowed.
6	EN_SOCACM_INT	R/W	0	When high, the state of e tcharge accumulation interrupt is allowed.
5	EN_ADPICHG_INT	R/W	0	When high, the VBUS adaptive charge current-limit interrupt is allowed.
4	EN_BATPRO_INT	R/W	0	When high, the battery protection interrupt is allowed.
3	EN_THR_INT	R/W	0	When high, the THR temperature threshold interrupt is allowed.
2	EN_BAT_INT	R/W	0	When high, the battery voltage threshold interrupt is allowed.
1	EN_CHG_INT	R/W	0	When high, the charger mode change interrupt is allowed.
0	EN_VBUS_INT	R/W	0	When high, the VBUS pin voltage threshold interrupt is allowed.

Table 69. INTERRUPT_ENABLE2 Register, Address 0x33 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
7	EN_MR_INT	R/W	0	When high, the $\overline{\text{MR}}$ press interrupt is allowed.
6	EN_WD_INT	R/W	0	When high, the watchdog alarm interrupt is allowed.
5	EN_BUCKPG_INT	R/W	0	When high, the VOUT1OK change interrupt is allowed.
4	EN_BUCKBSTPG_INT	R/W	0	When high, the VOUT2OK change interrupt is allowed.
[3:0]	Reserved	R/W	Not applicable	Reserved.

Table 70. INTERRUPT_FLAG1 Register, Address 0x34 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
7	SOCLOW_INT[1]	R	Not applicable	When high, this bit indicates an interrupt caused by low battery voltage.
6	SOCACM_INT[1]	R	Not applicable	When high, this bit indicates an interrupt caused by state of charge accumulation to 4096 points and an overflow of points.
5	ADPICHG_INT	R	Not applicable	When high, this bit indicates an interrupt caused by VBUS input current-limit adaptive regulation.
4	BATPRO_INT[1]	R	Not applicable	When high, this bit indicates an interrupt caused by battery protection triggered with battery fault events.
3	THR_INT[1]	R	Not applicable	When high, this bit indicates an interrupt caused by THR temperature thresholds.
2	BAT_INT[1]	R	Not applicable	When high, this bit indicates an interrupt caused by battery voltage thresholds.
1	CHG_INT[1]	R	Not applicable	When high, this bit indicates an interrupt caused by a charger mode change.
0	VBUS_INT[1]	R	Not applicable	When high, this bit indicates an interrupt caused by VBUS voltage threshold.

[1] When reading the register, the interrupt bit resets automatically.

Table 71. INTERRUPT_FLAG2 Register, Address 0x35 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
7	MR_INT[1]	R	Not applicable	When high, this bit indicates an interrupt caused by the $\overline{\text{MR}}$ press.
6	WD_INT[1]	R	Not applicable	When high, this bit indicates an interrupt caused by the watchdog alarm.
5	BUCKPG_INT[1]	R	Not applicable	When high, this bit indicates an interrupt caused by a VOUT1OK trigger.
4	BUCKBSTPG_INT[1]	R	Not applicable	When high, this bit indicates an interrupt caused by a VOUT2OK trigger.
[3:0]	Reserved	R	Not applicable	Reserved.

[1] When reading the register, the interrupt bit resets automatically.

Table 72. SHIPMODE Register, Address 0x36 Bit Descriptions

Bit(s)	Bit Name	Access	Default	Description
[7:1]	Reserved	R	Not applicable	Reserved.
0	EN_SHIPMODE	R/W	0	When high, the ADP5360 enters shipment mode. When low, shipment mode is disabled.

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUITS

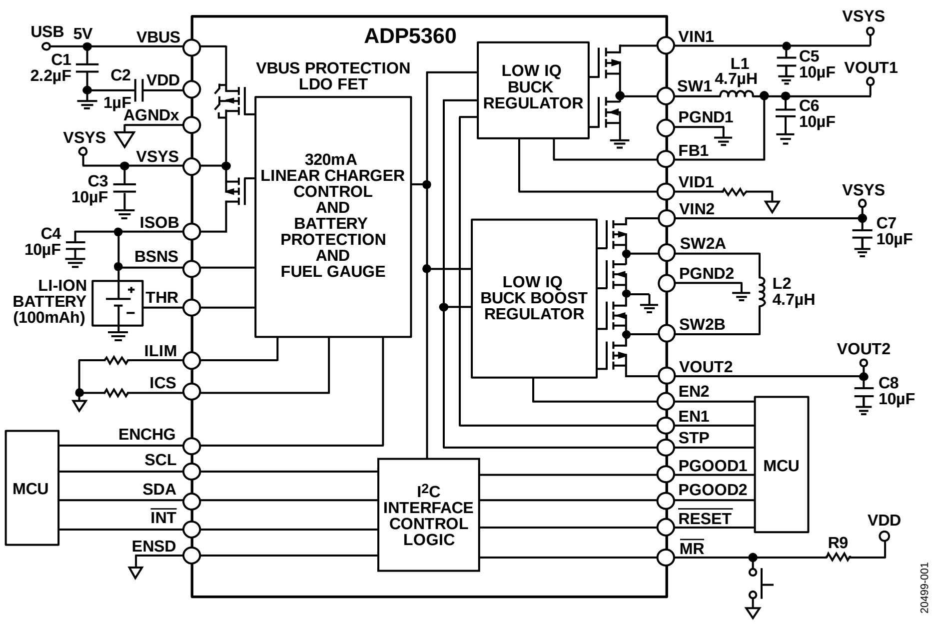


Figure 60. ADP5360 Application Diagram

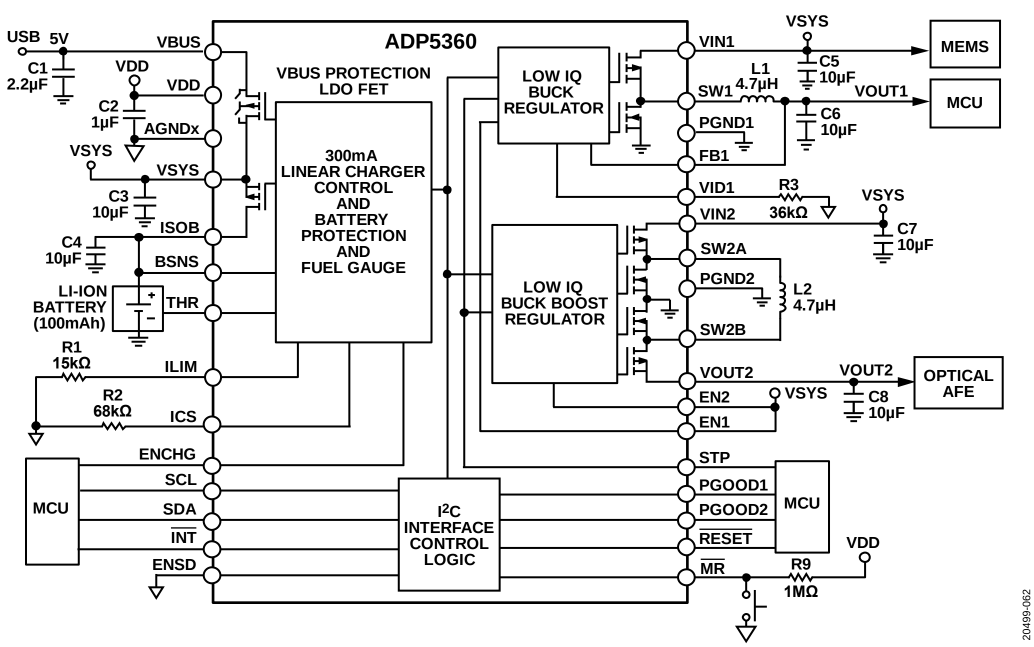


Figure 61. Li-Ion Battery Charger Application in Healthcare Portable

EXTERNAL COMPONENTS

VBUS Capacitor Selection

According to the USB specification, USB peripherals have a detectable change in capacitance on VBUS when VBUS is attached. The peripheral device VBUS bypass capacitance must be at least 1 µF but not larger than 10 µF. The combined capacitance for the VBUS pin and the VDD pin must not exceed 10 µF at any temperature or dc bias condition. Suggested VBUS capacitors are shown in Table 73.

Table 73. Suggested VBUS Capacitors

Vendor	Product Number	Value (µF)	Voltage (V)	Size
Murata	GRM155R61E225ME15D	2.2	25	0402
Yageo	CC0402MRX5R8BB225	2.2	25	0402

VDD Capacitor Selection

The internal supply voltage of the ADP5360 is equipped with a noise suppressing capacitor at VDD. Use typical VDD capacitance (1 µF). However, do not exceed 10 µF during operation. Do not connect any external voltage source, any resistive load, or any other current load to VDD. Suggested VDD capacitors are shown in Table 74.

Table 74. Suggested VDD Capacitors

Vendor	Product Number	Value (µF)	Voltage (V)	Size
Murata	GRM155R60J105KE19D	1	6.3	0402
Yageo	CC0402KRX5R5BB105	1	6.3	0402

VSYS Capacitor Selection

To guarantee the performance of the charger in various operation modes, including trickle charge, constant current charge, and constant voltage charge, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application. The total VSYS capacitance consists of all capacitors when VSYS is tied together with the input node of the buck and buck boost regulators.

The VSYS capacitance must be ≥10 µF. Suggested VSYS capacities are shown in Table 75.

Table 75. Suggested VSYS, ISOB, VIN1, VIN2, V_{OUT1}, and VOUT2 Capacitors

Vendor	Product Number	Value (µF)	Voltage (V)	Size
Murata	GRM155R60J106ME44D	10	6.3	0402
Yageo	CC0402MRX5R5BB106	10	6.3	0402

ISOB Capacitor Selection

The ISOB effective capacitance must be ≥4.7 µF at any point during operation. Typically, a nominal capacitance of 10 µF is required to fulfill the condition at all points of operation. Suggestions for an ISOB capacitor are show in Table 75.

Buck Input Capacitor Selection

An input capacitor is required to reduce the input voltage ripple, input ripple current, and source impedance. Place the input capacitor as close as possible to the VIN1 pin. Use the following equation to determine the rms input current:

$$I_{RMS} \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

For most applications, the VIN1 pin ties together with the VSYS pin. The VSYS capacitance is effective, therefore, a 1 µF capacitor is sufficient for the VIN1 pin. The input capacitor can be increased without any limit for better input voltage filtering. Suggested VIN1 capacitors are show in Table 75.

Buck Inductor Selection

The high switching frequency of the ADP5360 buck converter allows the selection of small chip inductors when the buck operates in FPWM mode.

Use the following equation to calculate the peak-to-peak inductor current ripple ($I_{RIPPLE1}$):

$$I_{RIPPLE1} = V_{OUT1} \times ((V_{IN1} - V_{OUT1}))/(V_{IN1} \times f_{SW} \times L1)$$

where:
V_{OUT1} is the buck output voltage.
V_{IN1} is the buck input voltage at the VIN1 node.
f_{SW} is the buck switching frequency.
$L1$ is the buck output inductor value.

The minimum dc current rating of the inductor must be greater than the inductor peak current (I_{PEAK1}). To calculate I_{PEAK1}, use the following equation:

$$I_{PEAK1} = I_{LOAD1(MAX)} + I_{RIPPLE1}$$

where $I_{LOAD(MAX)}$ is the output current load.

Inductor conduction losses are caused by the flow of current through the inductor, which has an associated internal dc resistance (DCR). Larger inductors have smaller DCR values that can decrease inductor conduction losses. Inductor core losses are related to the magnetic permeability of the core material. Because the buck regulators are high switching frequency dc-to-dc converters, shielded ferrite core material is recommended for low core losses and low electromagnetic interference (EMI).

Suggested buck inductors are shown in Table 76.

Buck Output Capacitor Selection

Output capacitance is required to minimize the output voltage overshoot and undershoot and to minimize the output ripple significantly both in hysteresis mode and FPWM mode. Capacitors with low equivalent series resistance (ESR) values produce the lowest output ripple in FPWM mode.

Suggested buck output capacitors are shown in Table 75.

Buck Boost Input Capacitor Selection

An input capacitor is required to reduce the input voltage ripple, input ripple current, and source impedance. Place the input capacitor as close as possible to the VIN2 pin.

For most applications, the VIN2 pin ties together with the VSYS pin. The VSYS capacitance is effective, therefore, a 1 μF capacitor is sufficient for the VIN2 pin. The input capacitor can be increased without any limit for better input voltage filtering. Suggested VIN2 capacitors are show in Table 75.

Buck Boost Inductor Selection

Inductor conduction losses are caused by the flow of current through the inductor, which has an associated internal DCR. Larger inductors have smaller DCR values that can decrease inductor conduction losses. Inductor core losses are related to the magnetic permeability of the core material.

Suggested buck boost inductors are shown in Table 76.

Buck Boost Output Capacitor Selection

Output capacitance is required to minimize the output voltage overshoot and undershoot and to minimize the output ripple significantly in hysteresis mode.

Suggested buck boost output capacitors are shown in Table 75.

Table 76. Recommended Inductors

Vendor	Model	Inductance (μH)	Dimensions (mm)	DCR (mΩ)	Rated Current (I_R) (A)
Wurth	74479776247A	4.7	2.0 × 1.6 × 1.0	140	1.2
TDK	MLP2016H4R7	4.7	2.0 × 1.6 × 0.85	160	1.1

PCB LAYOUT GUIDELINES

Poor layout can affect ADP5360 performance, causing EMI and electromagnetic compatibility (EMC) problems, ground bounce, and voltage losses, as well as affect regulation and stability. A good layout is implemented using the following guidelines:

- Place the decoupling capacitor, inductor, input capacitor, and output capacitor as close as possible to the ADP5360.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.
- Use a dedicated trace to connect the BSNS pin to the battery pack output node for accurate sensing of the battery voltage.
- Use 0603 size or 0402 size resistors and capacitors to achieve the smallest possible footprint solution on boards where space is limited.

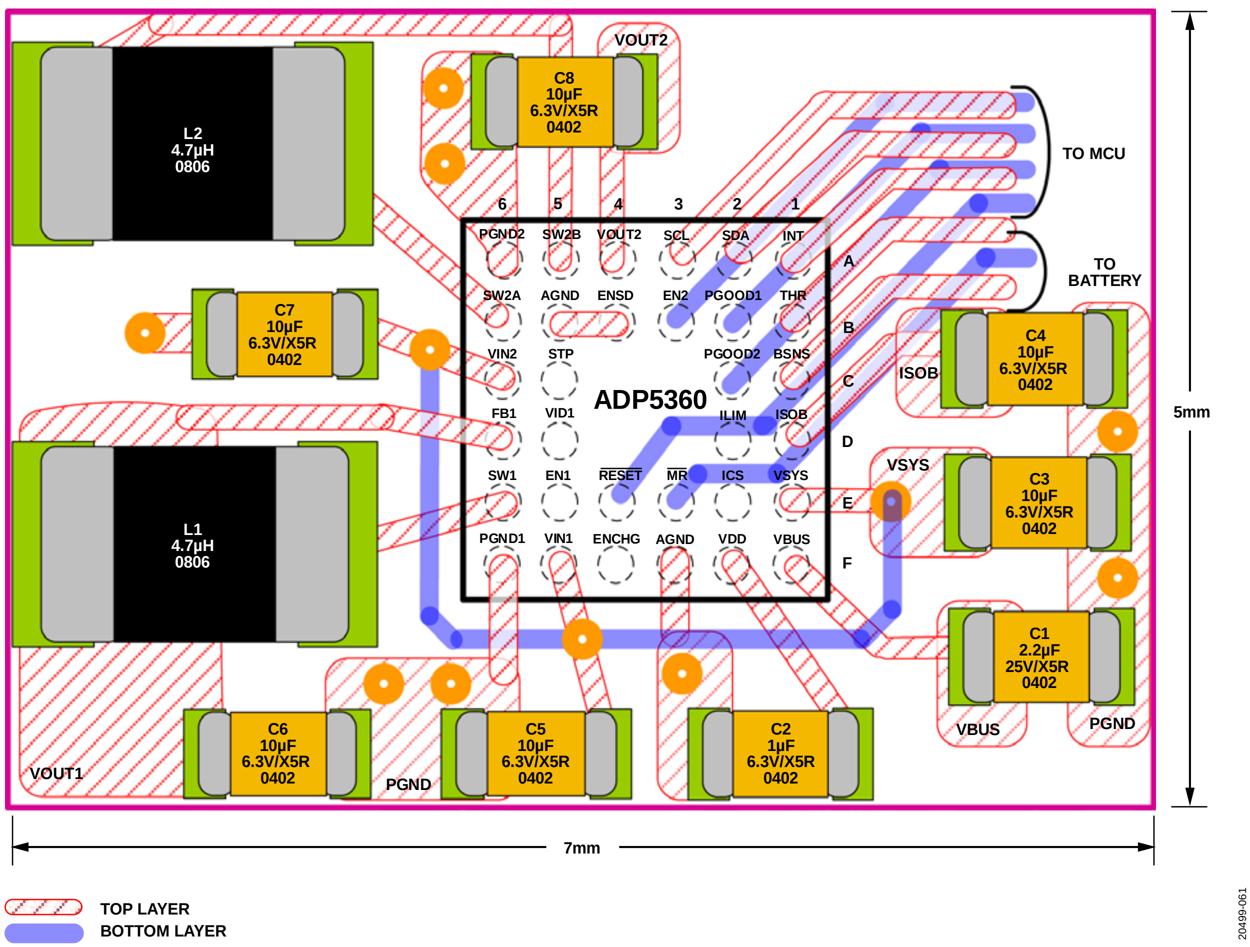


Figure 62. Recommend Layout

FACTORY-PROGRAMMABLE OPTIONS

Table 77. Fuse-Programmable Trim Options for the Different Modes of the ADP5360

Parameter	Value	Default Setting
I^2C Address	0x46 0x56 0x66 0x76	0x46
EN_CHG	Enable charger Disable charger	Disable charger
ITHR	60 µA 12 µA 6 µA	60 µA
VTRM	3.96 V 4.06 V 4.16 V 4.26 V 4.36 V 4.36 V 4.46 V 4.46 V	4.16 V
EN_BATPRO	Disable battery protection function Enable battery protection function	Enable battery protection function
UV_DISCH	2.2 V 2.5 V 2.6 V 2.8 V	2.5 V
OC_DISCH	100 mA 200 mA 400 mA 600 mA	600 mA
OV_CHG	4.25 V 4.30 V 4.40 V 4.50 V	4.30 V
OC_CHG	100 mA 150 mA 200 mA 400 mA	150 mA for the ADP5360ACBZ-1-R7 and 400 mA for the ADP5360ACBZ-2-R7
EN_BUCK	Disable buck output Enable buck output	Enable buck output
BUCK_SS	1 ms 8 ms 64 ms 512 ms	1 ms
BUCK_MODE	Hystersis mode FPWM mode	Hystersis mode
DISCHG_BUCK	Disable output discharge function Enable output discharge function	Disable output discharge function

Parameter	Value	Default Setting
VOUT_BUCK	1.0 V 1.2 V 1.5 V 1.8 V 2.5 V 2.8 V 3.0 V 3.3 V	1.2 V for the ADP5360ACBZ-1-R7 and 1.8 V for the ADP5360ACBZ-2-R7
EN_BUCKBST	Disable buck boost output Enable buck boost output	Disable buck boost output
BUCKBST_SS	1 ms 8 ms 64 ms 512 ms	1 ms
DISCHG_BUCKBST	Disable output discharge function Enable output discharge function	Disable output discharge function
VOUT_BUCKBST	2.5 V 3.3 V 3.6 V 4.0 V 4.2 V 4.6 V 5.0 V 5.5 V	3.3 V for the ADP5360ACBZ-2-R7 and 5.0 V for the ADP5360ACBZ-1-R7
PG1_REV	Disable PGOOD1 pin output active low Enable PGOOD1 pin output active low	Disable PGOOD1 pin output active low
VBUSOK_MASK1	Do not output the V_{VBUS} voltage status signal to the external PGOOD1 pin Output the V_{VBUS} voltage status signal to the external PGOOD1 pin	Do not output the V_{VBUS} voltage status signal to the external PGOOD1 pin
VOUT1OK_MASK1	Do not output the buck PGOOD signal to the external PGOOD1 pin Output the buck PGOOD signal to the external PGOOD1 pin	Do not output the buck PGOOD signal to the external PGOOD1 pin

OUTLINE DIMENSIONS

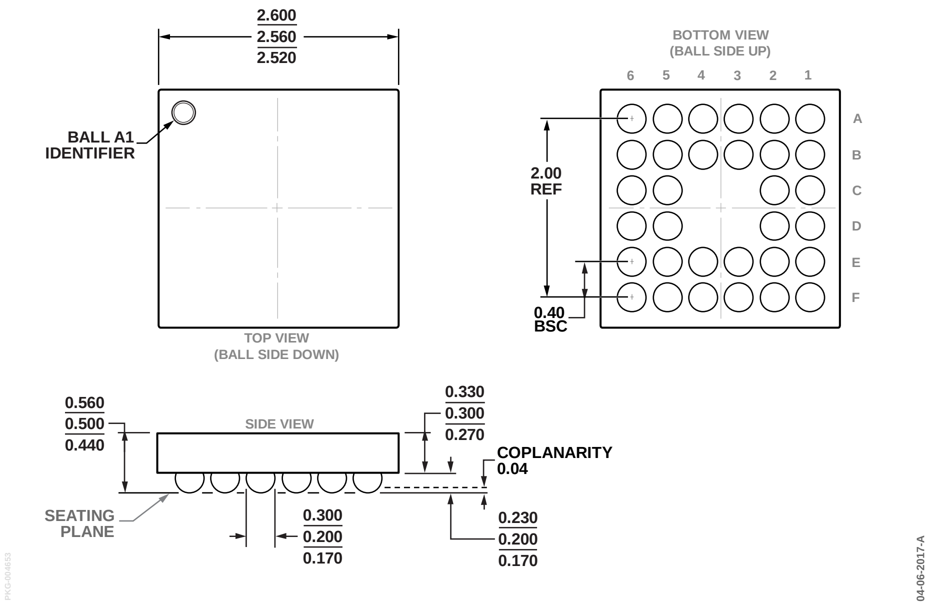


Figure 63. 32-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP5360ACBZ-1-R7	−40°C to +85°C	32-Ball Wafer Level Chip Scale Package [WLCSP]	CB-32-2
ADP5360ACBZ-2-R7	−40°C to +85°C	32-Ball Wafer Level Chip Scale Package [WLCSP]	CB-32-2
ADP5360CB-EVALZ		Evaluation Board Assembled with ADP5360ACBZ-1-R7	

[1] Z = RoHS Compliant Part.

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).