Low Frequency to 3 GHz, Dual VGA with Output Common-Mode and DC Offset Control

Data Sheet

ADRF6521

FEATURES

- **Dual, matched VGAs**
- **Maximum voltage gain: 18 dB**
- **Gain control attenuation range: 21 dB typical for T_A = 25°C**
- **±1 dB gain flatness bandwidth: 2.5 GHz typical**
- **IMD2 and IMD3 (1.5 V p-p output level)**
  - **−56.8 dBc typical and −75 dBc typical, respectively, at VGN = 1.5 V, 980 MHz and 1000 MHz tones**
- **HD2 and HD3 (1.5 V p-p output level)**
  - **−75 dBc typical and −73.7 dBc typical, respectively, at VGN = 1.5 V, fundamental at 500 MHz**
  - **−55.9 dBc typical and −57.5 dBc typical, respectively, at VGN = 1.5 V, fundamental at 1 GHz**
- **Noise figure**
  - **10.5 dB typical at maximum gain and at 500 MHz**
  - **14.8 dB at maximum gain and at 2 GHz**
  - **Noise figure decreases dB for dB with gain backoff**
- **100 Ω differential input impedance**
- **≤16 Ω differential output impedance**
- **Programmable**
  - **Output DC offset nominal range: ±400 mV**
  - **Output common-mode control: > ±200 mV for VOCM = ±0.2 V**
- **Single- or dual-supply operation with power-down feature**
  - **Single supply: VPOS = 5 V, VNEG = 0 V (nominal)**
  - **Dual supply: VPOS = 3 V, VNEG =−2 V (nominal)**

APPLICATIONS

- **Point-to-point and point-to-multipoint radios**
- **Baseband IQ receivers**
- **Diversity receivers**
- **ADC drivers**
- **Instrumentation**
- **Medical**

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

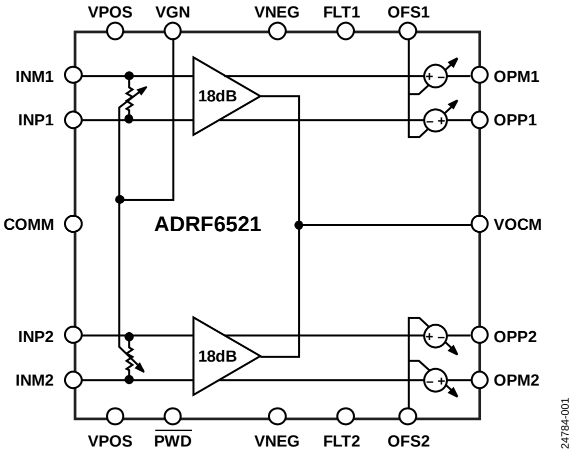

Figure 1.

GENERAL DESCRIPTION

The ADRF6521 is a dual, fully differential, low noise and low distortion variable gain amplifier (VGA). The high spurious-free dynamic range over the gain range makes the ADRF6521 ideal for communication systems with dense constellations, multiple carriers, and nearby interferers.

The VGA has a 21 dB attenuation range with a typical voltage gain of 18 dB. The differential input impedance is 100 Ω, while the differential output impedance is 16 Ω. The ±1 dB gain flatness bandwidth is 2.5 GHz. The output buffers are capable of swinging 1.5 V p-p into 100 Ω loads at >55 dBc for second-order and third-order intermodulation distortion (IMD2 and IMD3), and for second and third harmonic distortion (HD2 and HD3) from low frequency to 1 GHz. Variable output dc offset control is accomplished with the OFS1 and OFS2 pins, and the output common-mode can be controlled with the VOCM pin.

The ADRF6521 flexibly operates from a single +5 V supply or from a range of dual supplies and consumes a total supply current of 200 mA. When fully disabled, it consumes 25 mA typical. The ADRF6521 is fabricated in an advanced silicon-germanium BiCMOS process and is available in a 20-lead, exposed pad, 3 mm × 3 mm LFCSP. Performance is specified over the −40°C to +85°C temperature range.

Rev. 0 **Document Feedback**

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
Simplified Functional Block Diagram ... 1
General Description ... 1
Revision History ... 2
Specifications ... 3
Absolute Maximum Ratings ... 7
  Thermal Resistance ... 7
  Electrostatic Discharge (ESD) Ratings ... 7
  ESD Caution ... 7
Pin Configuration and Function Descriptions ... 8
Typical Performance Characteristics ... 9
  Single-Supply Operation ... 9
  Dual-Supply Operation ... 19
Theory of Operation ... 29
  Input VVAs ... 29
  Amplifiers ... 29
  Output Common-Mode Voltage ... 29
  Output DC Offset Circuit ... 29
  Gain Control Interface ... 30
  Power-Down Function ... 30
Applications Information ... 31
  Basic Connections ... 31
  Supply Decoupling ... 31
  Input Signal Path ... 31
  Output Signal Path ... 31
  Enable and Disable Function ... 32
  Gain Pin (VGN) Decoupling ... 32
  Output Impedance Matching ... 32
  Single-Supply Operation ... 32
  Dual-Supply Operation ... 32
  Avoiding Latch-Up ... 32
Outline Dimensions ... 33
  Ordering Guide ... 33

REVISION HISTORY

11/2020—Revision 0: Initial Version

SPECIFICATIONS

For single-supply operation, VPOS = 5 V, VNEG = 0 V nominal, and VOCM = 2.5 V, and for dual-supply operation, VPOS = 3 V, VNEG = −2 V nominal, and VOCM = 0 V, unless otherwise noted. T_A = 25°C and load impedance (Z_{LOAD}) = 186 Ω, unless otherwise noted. Voltages on VOCM, OFS1, and OFS2 are with respect to COMM (analog ground).

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RESPONSE	Single-supply operation				
±1 dB Gain Flatness Bandwidth	Channel 1 or 2, maximum gain		2.5		GHz
−3 dB Bandwidth	Maximum gain		3.25		GHz
Pass-Band Flatness	Defined as difference between value at 100 kHz and 1 GHz		0.5		dB
Gain Matching	Channel A and Channel B at same gain				
	Less than 1 GHz		±0.2		dB
	Less than 3 GHz		±0.4		dB
Group Delay					
Variation	From 500 MHz to 1 GHz		0.1		ns
Matching	Frequency = 1 GHz		±25		ps
	Frequency = 3 GHz		±40		ps
INPUT STAGE	INP1, INM1, INP2, INM2				
Maximum Input Swing	At minimum gain, VGN = 0 V		8		V p-p
Differential Input Impedance			100		Ω
Input Common-Mode	(VPOS + VNEG)/2, ac coupling recommended				
	VOCM undriven, single-supply operation		2.5		V
	VOCM undriven, dual-supply operation		0.5		V
GAIN CONTROL	VGN (ground referenced)				
Voltage Range[1, 2]	Minimum		0		V
	Maximum		1.5		V
Voltage Gain	VGN = 1.5 V, maximum gain		18		dB
	VGN = 0 V, minimum gain		−3		dB
Attenuation Range	T_A = 25°C		21		dB
	−40°C ≤ T_A ≤ +85°C		>20		dB
Gain Slope			45		mV/dB
Gain Error	VGN voltage (V_{VGN}) range = 500 mV to 1000 mV		0.2		dB
VGA Step Response Time	Through full attenuator range				
Rise Time	From 10% to 90% of output		240		ns
Fall Time	From 90% to 10% of output		250		ns
COMMON-MODE CONTROL[3]	VOCM (VPOS and VNEG supply referenced)				
Default Value	VOCM floating (nominal)		$(V_{VPOS} + V_{VNEG})/2$		V
Voltage Range[1]	Minimum		$(V_{VPOS} + V_{VNEG})/2 - 1$		V
	Maximum		$(V_{VPOS} + V_{VNEG})/2 + 1$		V
Output Common Mode[4]	$(V_{OPP1} + V_{OPM1})/2$ or $(V_{OPP2} + V_{OPM2})/2$				
	VOCM = 0 V		0		V
	VOCM = 0.2 V		200		mV
	VOCM = −0.2 V		−200		mV
	VOCM = ±0.3 V, functional maximum		±300		mV
DC OFFSET CONTROL	OFS1 and OFS2 (ground referenced)				
Voltage Range[1, 2]	Minimum		0		V
	Maximum		1.5		V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Output DC Offset	(V_{OPP1} − V_{OPM1}) or (V_{OPP2} − V_{OPM2})				
	OFS1 and OFS2 = 0.75 V (nominal)		<20		mV
	OFS1 and OFS2 = 1.2 V		400		mV
	OFS1 and OFS2 = 0.3 V		−400		mV
	OFS1 and OFS2 = 0 V		−600		mV
	OFS1 and OFS2 = 1.5 V		600		mV
DC Offset Channel to Channel Mismatch	OFS1 and OFS2 = 0.75 V		6.2		mV
OUTPUT STAGE	OPP1, OPM1, OPP2, and OPM2				
Maximum Output Swing	At maximum gain, load resistance (R_{LOAD}) = 186 Ω		5.64		V p-p
	IMD2, IMD3, HD2, and HD3 are > 55 dBc at a 100 Ω interface[5]		1.5		V p-p
Output 1 dB Compression Point (OP1dB)	Frequency = 1 GHz, gain = 18 dB, R_{LOAD} = 186 Ω		>6		dBV[6]
	At 100 Ω interface[5]		> 0.6		dBV[6]
Differential Output Impedance			≤16		Ω
NOISE AND DISTORTION					
Single-Supply Operation					
Output Noise Density	Input impedance (Z_{IN}) = 100 Ω at 100 Ω interface[5]				
	VGN = 1.5 V at 500 MHz		−159.9		dBV/Hz
	VGN = 0.75 V at 500 MHz		−161		dBV/Hz
	VGN = 0 V at 500 MHz		−161.5		dBV/Hz
	VGN = 1.5 V at 2 GHz		−155		dBV/Hz
	VGN = 0.75 V at 2 GHz		−157		dBV/Hz
	VGN = 0 V at 2 GHz		−157.4		dBV/Hz
Noise Figure					
	VGN = 1.5 V at 500 MHz		12.3		dB
	VGN = 0.75 V at 500 MHz		21.5		dB
	VGN = 0 V at 500 MHz		31.5		dB
	VGN = 1.5 V at 2 GHz		16.3		dB
	VGN = 0.75 V at 2 GHz		24.5		dB
	VGN = 0 V at 2 GHz		34.3		dB
Second Harmonic Distortion, HD2	1.5 V p-p output level				
	VGN = 1.5 V, fundamental at 500 MHz		−75		dBc
	VGN = 0.75 V, fundamental at 500 MHz		−76		dBc
	VGN = 0 V, fundamental at 500 MHz		−77		dBc
	VGN = 1.5 V, fundamental at 1 GHz		−55.9		dBc
	VGN = 0.75 V, fundamental at 1 GHz		−54		dBc
	VGN = 0 V, fundamental at 1 GHz		−41		dBc
Third Harmonic Distortion, HD3	1.5 V p-p output level				
	VGN = 1.5 V, fundamental at 500 MHz		−73.7		dBc
	VGN = 0.75 V, fundamental at 500 MHz		−72		dBc
	VGN = 0 V, fundamental at 500 MHz		−72.6		dBc
	VGN = 1.5 V, fundamental at 1 GHz		−57.5		dBc
	VGN = 0.75 V, fundamental at 1 GHz		−68		dBc
	VGN = 0 V, fundamental at 1 GHz		−62		dBc
IMD2	1.5 V p-p output level				
	VGN = 1.5 V, 480 MHz and 500 MHz tones		−74		dBc
	VGN = 0.75 V, 480 MHz and 500 MHz tones		−62		dBc
	VGN = 0 V, 480 MHz and 500 MHz tones		−53		dBc
	VGN = 1.5 V, 980 MHz and 1000 MHz tones		−56.8		dBc
	VGN = 0.75 V, 980 MHz and 1000 MHz tones		−54		dBc
	VGN = 0 V, 980 MHz and 1000 MHz tones		−45		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
IMD3	1.5 V p-p output level				
	VGN = 1.5 V, 480 MHz and 500 MHz tones		−74		dBc
	VGN = 0.75 V, 480 MHz and 500 MHz tones		−77		dBc
	VGN = 0 V, 480 MHz and 500 MHz tones		−73		dBc
	VGN = 1.5 V, 980 MHz and 1000 MHz tones		−75		dBc
	VGN = 0.75 V, 980 MHz and 1000 MHz tones		−82		dBc
	VGN = 0 V, 980 MHz and 1000 MHz tones		−76		dBc
Input Second-Order Intercept Point (IIP2)					
	VGN = 1.5 V, 480 MHz and 500 MHz tones		44.9		dBV
	VGN = 0.75 V, 480 MHz and 500 MHz tones		44.5		dBV
	VGN = 0 V, 480 MHz and 500 MHz tones		45		dBV
	VGN = 1.5 V, 980 MHz and 1000 MHz tones		27.5		dBV
	VGN = 0.75 V, 980 MHz and 1000 MHz tones		36.3		dBV
	VGN = 0 V, 980 MHz and 1000 MHz tones		36.7		dBV
Input Third-Order Intercept Point (IIP3)					
	VGN = 1.5 V, 480 MHz and 500 MHz tones		7.9		dBV
	VGN = 0.75 V, 480 MHz and 500 MHz tones		20.1		dBV
	VGN = 0 V, 480 MHz and 500 MHz tones		28.5		dBV
	VGN = 1.5 V, 980 MHz and 1000 MHz tones		8.2		dBV
	VGN = 0.75 V, 980 MHz and 1000 MHz tones		23.3		dBV
	VGN = 0 V, 980 MHz and 1000 MHz tones		29.7		dBV
Dual-Supply Operation					
Output Noise Density	Z_{IN} = 100 Ω at 100 Ω interface[5]				
	VGN = 1.5 V at 500 MHz		−161.7		dBV/Hz
	VGN = 0.75 V at 500 MHz		−162.2		dBV/Hz
	VGN = 0 V at 500 MHz		−162.1		dBV/Hz
	VGN = 1.5 V at 2 GHz		−158.2		dBV/Hz
	VGN = 0.75 V at 2 GHz		−158.4		dBV/Hz
	VGN = 0 V at 2 GHz		−158.7		dBV/Hz
Noise Figure					
	VGN = 1.5 V at 500 MHz		10.5		dB
	VGN = 0.75 V at 500 MHz		20		dB
	VGN = 0 V at 500 MHz		31.3		dB
	VGN = 1.5 V at 2 GHz		14.8		dB
	VGN = 0.75 V at 2 GHz		24.5		dB
	VGN = 0 V at 2 GHz		34.4		dB
HD2	1.5 V p-p output level				
	VGN = 1.5 V, fundamental at 500 MHz		−79		dBc
	VGN = 0.75 V, fundamental at 500 MHz		−93		dBc
	VGN = 0 V, fundamental at 500 MHz		−79		dBc
	VGN = 1.5 V, fundamental at 1 GHz		−59		dBc
	VGN = 0.75 V, fundamental at 1 GHz		−53		dBc
	VGN = 0 V, fundamental at 1 GHz		−40.5		dBc
HD3	1.5 V p-p output level				
	VGN = 1.5 V, fundamental at 500 MHz		−72		dBc
	VGN = 0.75 V, fundamental at 500 MHz		−75		dBc
	VGN = 0 V, fundamental at 500 MHz		−72		dBc
	VGN = 1.5 V, fundamental at 1 GHz		−57		dBc
	VGN = 0.75 V, fundamental at 1 GHz		−70		dBc
	VGN = 0 V, fundamental at 1 GHz		−62.5		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
IMD2	1.5 V p-p output level				
	VGN = 1.5 V, 480 MHz and 500 MHz tones		−74		dBc
	VGN = 0.75 V, 480 MHz and 500 MHz tones		−60.9		dBc
	VGN = 0 V, 480 MHz and 500 MHz tones		−53		dBc
	VGN = 1.5 V, 980 MHz and 1000 MHz tones		−58		dBc
	VGN = 0.75 V, 980 MHz and 1000 MHz tones		−55		dBc
	VGN = 0 V, 980 MHz and 1000 MHz tones		−46		dBc
IMD3	1.5 V p-p output level				
	VGN = 1.5 V, 480 MHz and 500 MHz tones		−80		dBc
	VGN = 0.75 V, 480 MHz and 500 MHz tones		−86		dBc
	VGN = 0 V, 480 MHz and 500 MHz tones		−73.5		dBc
	VGN = 1.5 V, 980 MHz and 1000 MHz tones		−71.6		dBc
	VGN = 0.75 V, 980 MHz and 1000 MHz tones		−87		dBc
	VGN = 0 V, 980 MHz and 1000 MHz tones		−76		dBc
IIP2					
	VGN = 1.5 V, 480 MHz and 500 MHz tones		44.9		dBV
	VGN = 0.75 V, 480 MHz and 500 MHz tones		43.4		dBV
	VGN = 0 V, 480 MHz and 500 MHz tones		45		dBV
	VGN = 1.5 V, 980 MHz and 1000 MHz tones		28.7		dBV
	VGN = 0.75 V, 980 MHz and 1000 MHz tones		37.3		dBV
	VGN = 0 V, 980 MHz and 1000 MHz tones		37.7		dBV
IIP3					
	VGN = 1.5 V, 480 MHz and 500 MHz tones		10.9		dBV
	VGN = 0.75 V, 480 MHz and 500 MHz tones		25.5		dBV
	VGN = 0 V, 480 MHz and 500 MHz tones		28.7		dBV
	VGN = 1.5 V, 980 MHz and 1000 MHz tones		6.5		dBV
	VGN = 0.75 V, 980 MHz and 1000 MHz tones		25.8		dBV
	VGN = 0 V, 980 MHz and 1000 MHz tones		29.7		dBV
POWER AND ENABLE	VPOS, VNEG, COMM, and $\overline{\text{PWD}}$				
Supply Voltage Range	VPOS > COMM ≥ VNEG				
VPOS − VNEG	Minimum		4		V
	Maximum		5		V
VPOS	Minimum		2.5		V
	Maximum		5		V
VNEG	Minimum		−2.5		V
	Maximum		0		V
Total Supply Current	$\overline{\text{PWD}}$ high voltage		200		mA
Disable Current	$\overline{\text{PWD}}$ = VNEG		25		mA
$\overline{\text{PWD}}$ Voltage Range	Minimum		VNEG		V
	Maximum		VNEG + 3.3		V
Enable Threshold			VNEG + 2.7		V
Disable Threshold			VNEG + 0.3		V
Enable Response Time	Delay following $\overline{\text{PWD}}$ low to high transition		<20		ns
Disable Response Time	Delay following $\overline{\text{PWD}}$ high to low transition		<8		ns

[1] Voltages beyond this range, but below the absolute maximum ratings, may cause latch-up problems.
[2] The voltage range is the functional range of the pin.
[3] V_{VPOS} is the VPOS voltage, and V_{VNEG} is the VNEG voltage.
[4] V_{OPP1} is the OPP1 voltage, V_{OPM1} is the OPM1 voltage, V_{OPP2} is the OPP2 voltage, and V_{OPM2} is the OPM2 voltage.
[5] Voltage levels at the interface are between the 43 Ω back termination resistors and 100 Ω differential load. This interface is −5.4 dB lower in voltage level than the output of the ADRF6521.
[6] X dBV = 20 × log10(x V rms/1 V rms). 0 dBV is equivalent to 1 V rms.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltages: VPOS − VNEG	5.25 V
$\overline{\text{PWD}}$	VNEG + 3.3 V
INP1, INM1, INP2, and INM2	VPOS + 0.5 V
OPP1, OPM1, OPP2, and OPM2	VPOS + 0.5 V
OFS1, OFS2	VPOS + 0.5 V
VOCM	VPOS + 0.5 V
VGN	VPOS + 0.5 V
Internal Power Dissipation	1.53 W
Temperature	
Maximum Junction	125°C
Operating Range	−40°C to +85°C
Storage Range	−65°C to +150°C
Lead (Soldering 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
CP-20-19	62.25	52.8	°C/W

[1] Based on simulation with JEDEC Standard JESD-51, using a 2S2P board.
[2] Based on simulation with JEDEC Standard JESD-51, using a 1S0P board.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRF6521

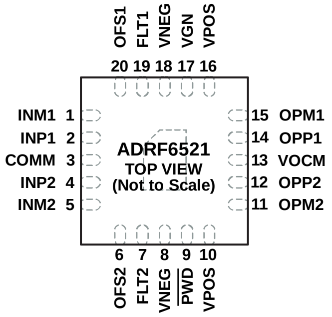
Table 4. ADRF6521, 20-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±1000	1B
FICDM	±1250	4

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE EXPOSED PAD IS INTERNALLY CONNECTED TO VNEG AND MUST BE SOLDERED TO THE NEGATIVE SUPPLY RAIL.

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Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2	INM1, INP1	Channel 1 Differential Inputs, 100 Ω Differential Input Impedance. (VPOS + VNEG)/2 nominal common mode.
3	COMM	Analog Ground.
4, 5	INP2, INM2	Channel 2 Differential Inputs, 100 Ω Differential Input Impedance. (VPOS + VNEG)/2 nominal common mode.
6	OFS2	Channel 2 Output DC Offset Control. Nominal control range from 0.3 V to 1.2 V relative to analog ground. A 0.75 V on OFSx produces a 0 V output offset voltage. OFS2 is not self biased. OFS2 must be driven. Left unconnected, OFS2 is pulled to ground via an on-chip 5 kΩ resistor, which forces the output dc offset to be −700 mV. Voltages greater than 1.5 V but less than the absolute maximum ratings may cause latch-up.
7	FLT2	Channel 2 Filter Pin. Connect FLT2 to the negative supply via a 1 µF capacitor.
8, 18	VNEG	Analog Negative Supply Voltage. For single-supply operation, set VNEG to 0 V nominal, and for dual-supply operation, set VNEG to −2 V nominal. Keep (VPOS − VNEG) ≤ 5 V, VNEG ≤ COMM ≤ VPOS, and −2.5 V ≤ VNEG ≤ 0 V to keep the voltage at the allowable pin voltage related to the voltage on the VPOS pin. Pins are electrically connected on chip and to the exposed pad. Connect both VNEG pins and the exposed pad to the negative supply voltage.
9	$\overline{\text{PWD}}$	Chip Power Down. Pull to VNEG supply to disable both channels. Leave unconnected to enable. Keep $V_{\overline{PWD}}$ ≤ (VNEG + 3.3 V).
10, 16	VPOS	Analog Positive Supply Voltage. For single-supply operation, set VPOS to 5 V nominal, and for dual-supply operation, set VPOS to 3 V nominal. Keep (VPOS − VNEG) ≤ 5 V, VNEG ≤ COMM ≤ VPOS, and VPOS ≥ 2.3 V to keep the voltage at the allowable pin voltage related to the voltage on the VNEG pin. Pins are electrically connected on chip. Connect both VPOS pins to the positive supply voltage.
11, 12	OPM2, OPP2	Channel 2 Differential Outputs. These outputs have a 16 Ω differential output impedance.
13	VOCM	Output Common-Mode Voltage Control. The nominal control range is (VPOS + VNEG)/2 − 200 mV to (VPOS + VNEG)/2 + 200 mV. A 0 V on VOCM is a 0 V output common-mode voltage. Self biased to (VPOS + VNEG)/2. Voltages greater than (V_{VPOS} + V_{VNEG})/2 ± 1 V but less than the absolute maximum ratings may cause latch-up.
14, 15	OPP1, OPM1	Channel 2 Differential Outputs. These outputs have a 16 Ω differential output impedance.
17	VGN	VGA Analog Gain Control. The VGN pins operate from 0 V to 1.5 V with 45 mV/dB gain scaling. Voltages greater than 1.5 V but less than the absolute maximum ratings may cause latch-up.
19	FLT1	Channel 1 Filter Pin. Connect FLT1 to a negative supply via a 1 µF capacitor.
20	OFS1	Channel 1 Output DC Offset Control. Nominal control range from 0.3 V to 1.2 V relative to analog ground. A 0.75 V on OFSx produces a 0 V output offset voltage. OFS1 is not self biased. OFS1 must be driven. Left unconnected, OFS1 is pulled to ground via an on-chip 5 kΩ resistor, which forces the output dc offset to be −700 mV.
EP		Exposed Pad. The exposed pad is internally connected to VNEG and must be soldered to the negative supply rail.

TYPICAL PERFORMANCE CHARACTERISTICS

SINGLE-SUPPLY OPERATION

VPOS = 5 V, VNEG = 0 V, T_A = 25°C, Z_{LOAD} = 186 Ω, VGN = 1.5 V, VOCM = 2.5 V, OFS1 = OFS2 = 0.75 V, output level = 1.5 V p-p, and 43 Ω back termination resistors de-embedded, unless otherwise noted. Noise figure measured with 100 Ω differential input termination. Worst case IMD2 and IMD3 tone reported. V_{OFSx} sweeps = 0 V, 0.4 V, 0.75 V, or 1.2 V. VOCM sweeps = 2.4 V, 2.5 V, or 2.6 V.

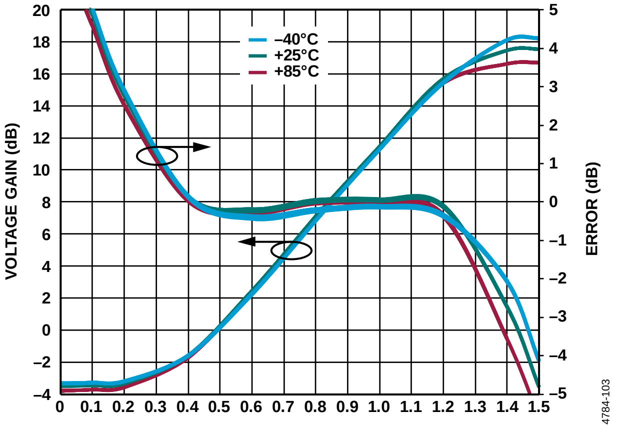


Figure 3. Voltage Gain and Error vs. VGN Voltage over Temperature at 500 MHz

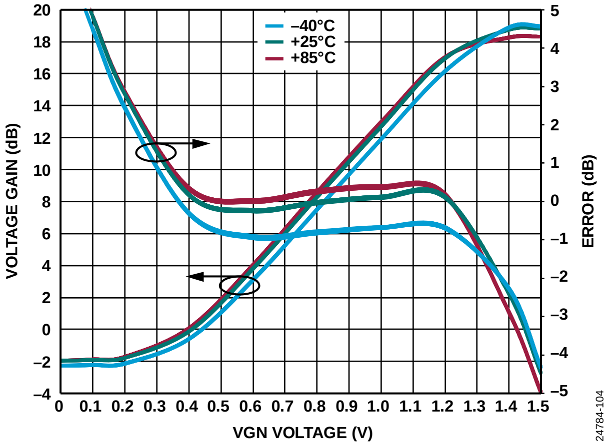


Figure 4. Voltage Gain and Error vs. VGN Voltage over Temperature at 2 GHz

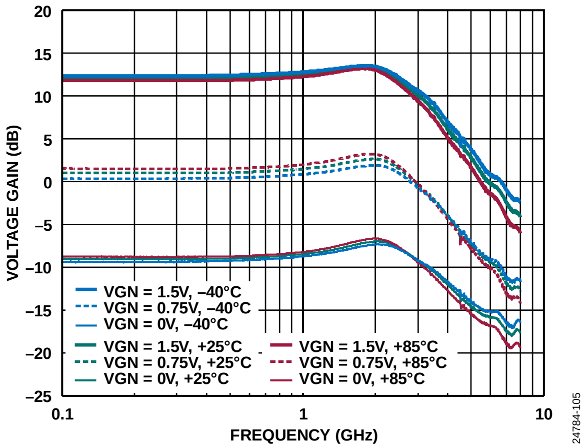


Figure 5. Voltage Gain vs. Frequency over Temperature and VGN, 43 Ω Back Terminations not De-Embedded

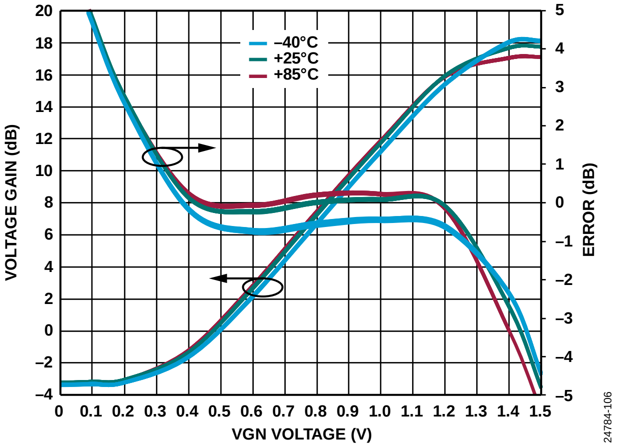


Figure 6. Voltage Gain and Error vs. VGN Voltage over Temperature at 1 GHz

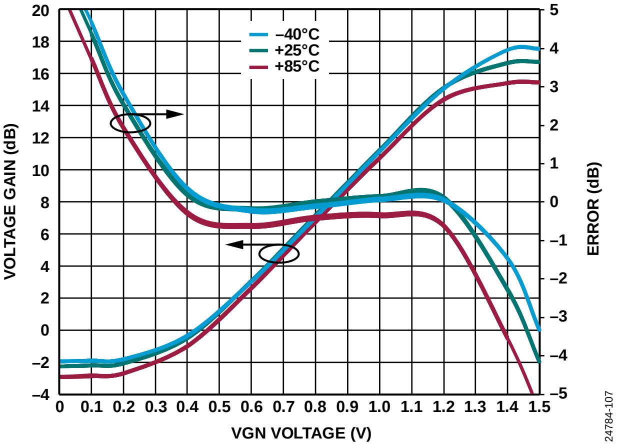


Figure 7. Voltage Gain and Error vs. VGN Voltage over Temperature at 3 GHz

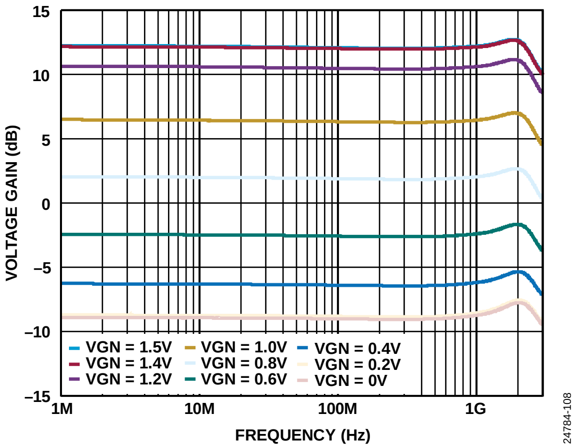


Figure 8. Voltage Gain vs. Frequency over 200 mV VGN Steps, 43 Ω Back Terminations not De-Embedded

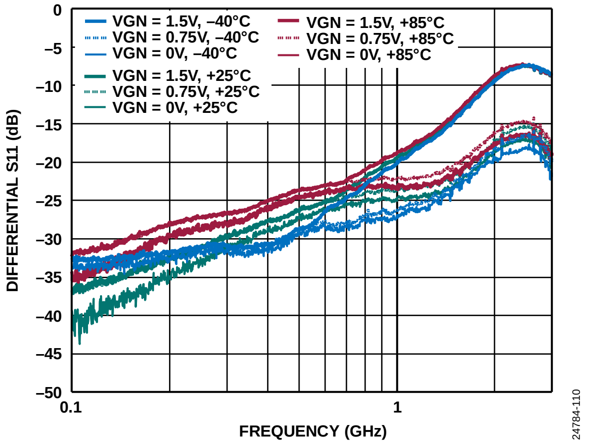


Figure 9. Differential Input Return Loss (S11) vs. Frequency over Temperature and VGN

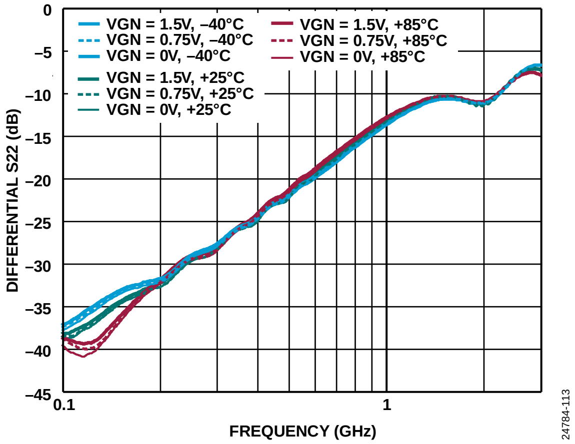


Figure 12. Differential Output Return Loss (S22) vs. Frequency over Temperature and VGN

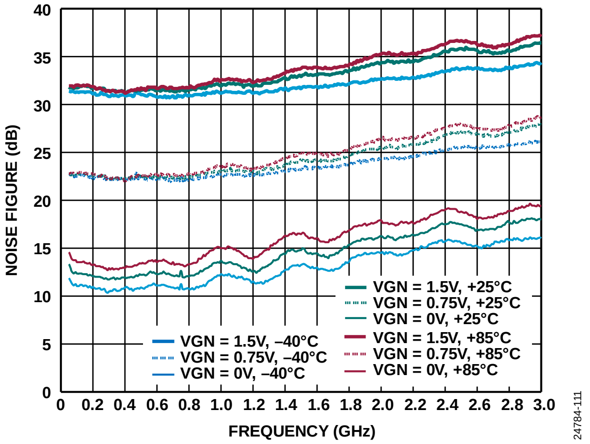


Figure 10. Noise Figure vs. Frequency over Temperature and VGN

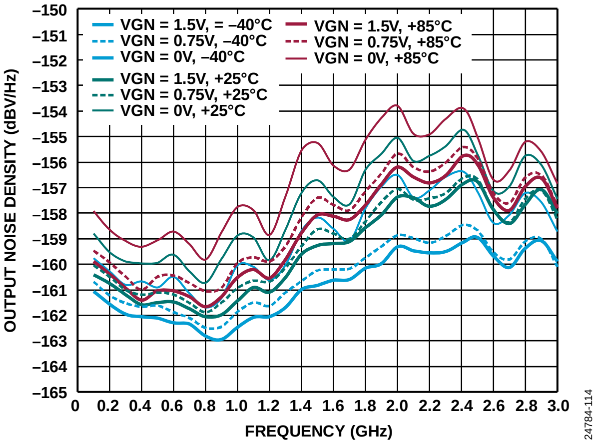


Figure 13. Output Noise Density vs. Frequency over Temperature and VGN

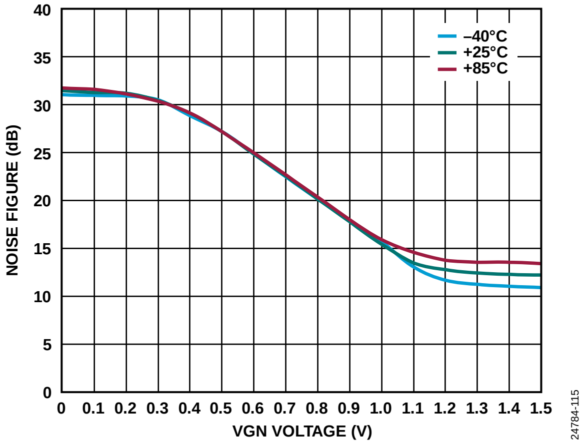


Figure 11. Noise Figure vs. VGN Voltage over Temperature at 500 MHz

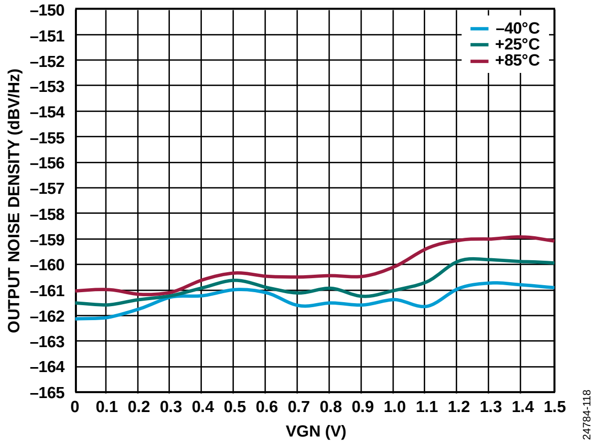


Figure 14. Output Noise Density vs. VGN over Temperature at 500 MHz

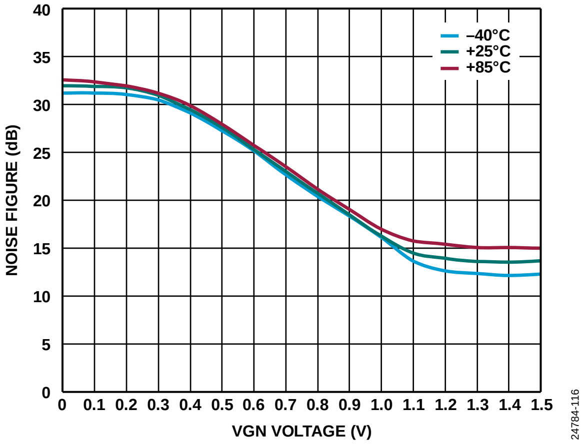


Figure 15. Noise Figure vs. VGN Voltage over Temperature, at 1 GHz

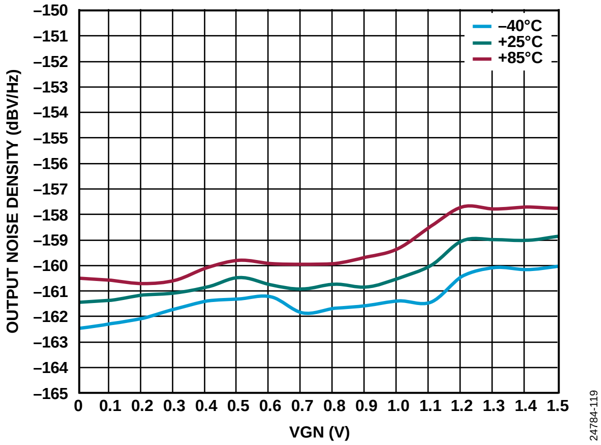


Figure 18. Output Noise Density vs. VGN over Temperature at 1 GHz

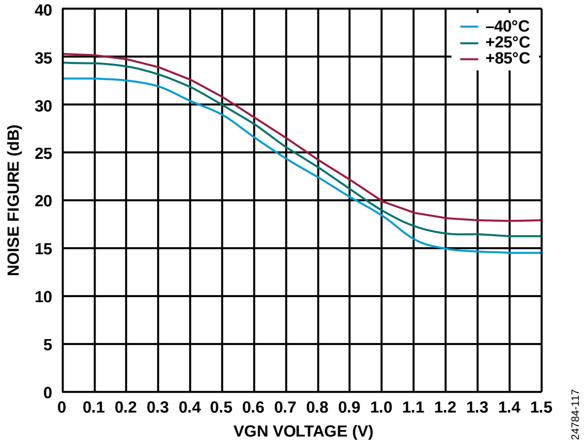


Figure 16. Noise Figure vs. VGN Voltage over Temperature, at 2 GHz

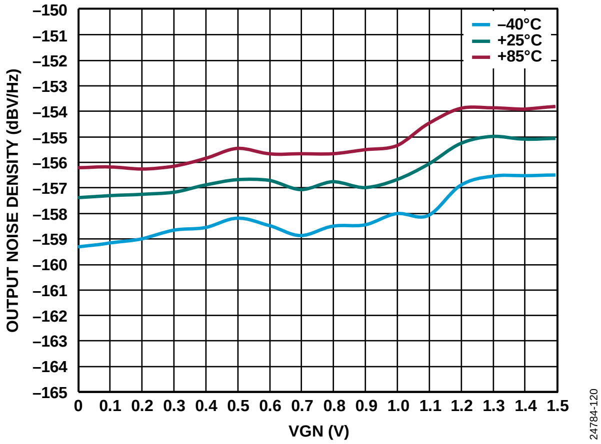


Figure 19. Output Noise Density vs. VGN over Temperature at 2 GHz

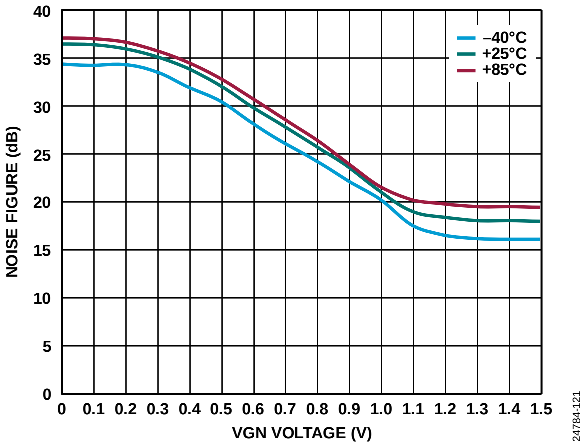


Figure 17. Noise Figure vs. VGN Voltage over Temperature at 3 GHz

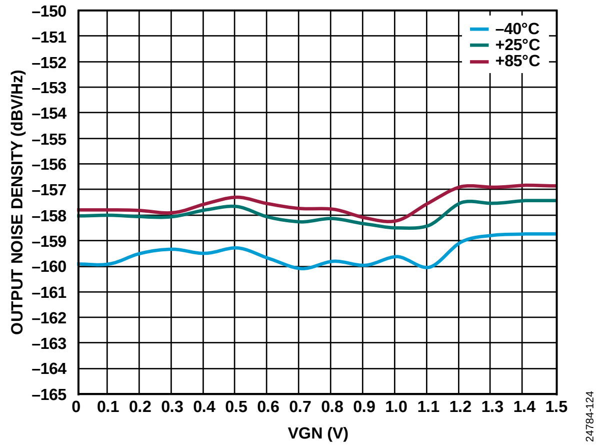


Figure 20. Output Noise Density vs. VGN over Temperature at 3 GHz

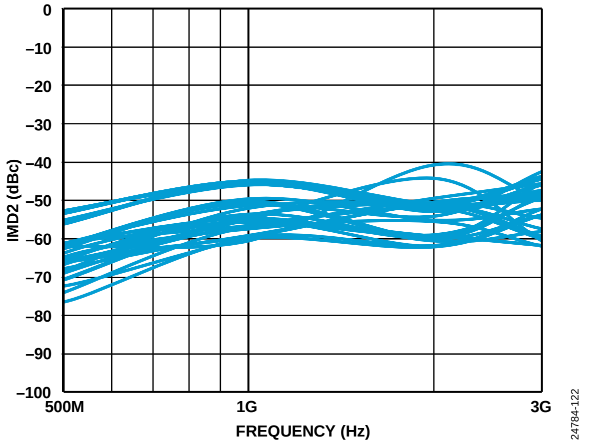


Figure 21. IMD2 vs. Frequency over VGN and OFSx

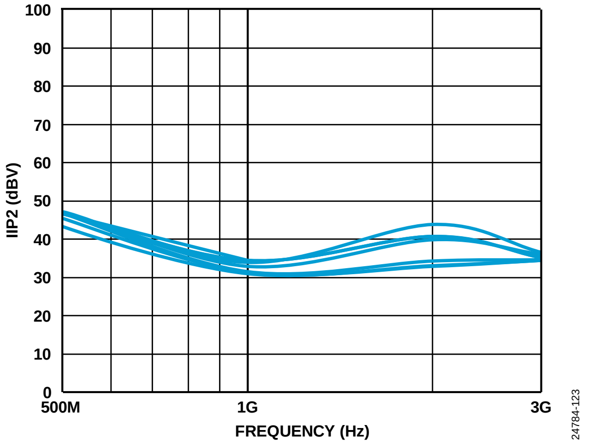


Figure 22. IIP2 vs. Frequency over VGN

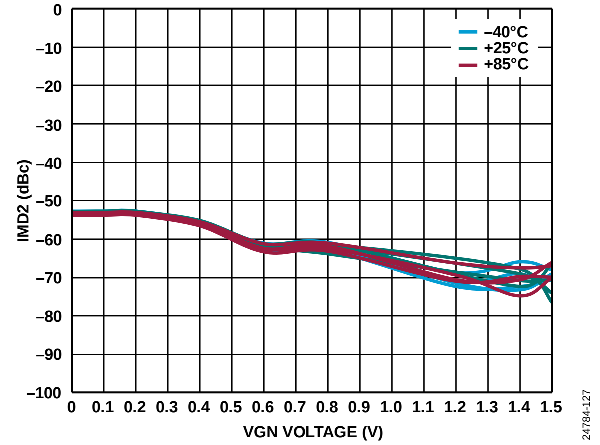


Figure 23. IMD2 vs. VGN Voltage over Temperature and OFSx at 500 MHz

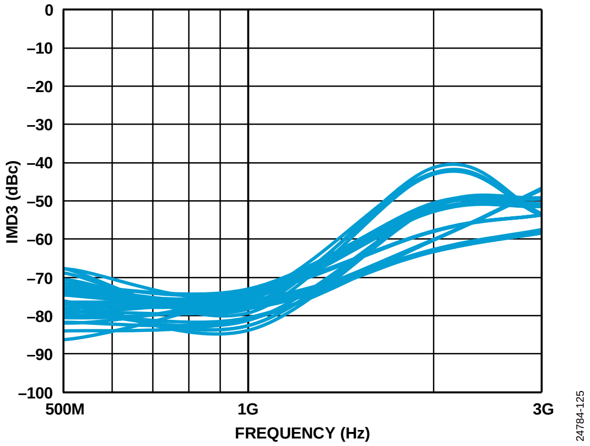


Figure 24. IMD3 vs. Frequency over VGN and OFSx

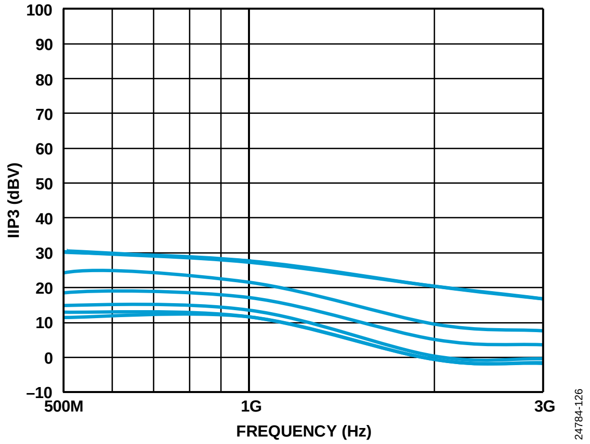


Figure 25. IIP3 vs. Frequency over VGN

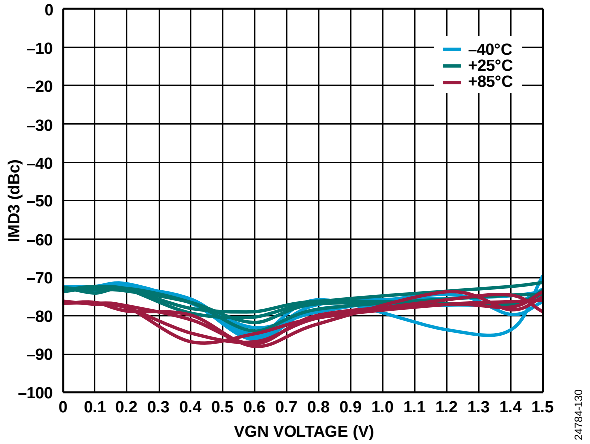


Figure 26. IMD3 vs. VGN Voltage over Temperature and OFSx at 500 MHz

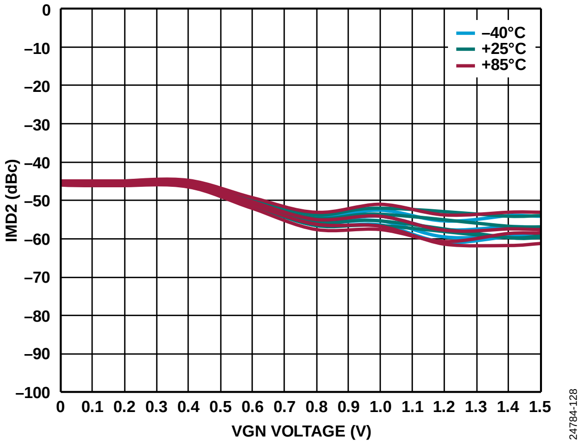


Figure 27. IMD2 vs. VGN Voltage over Temperature and OFSx at 1 GHz

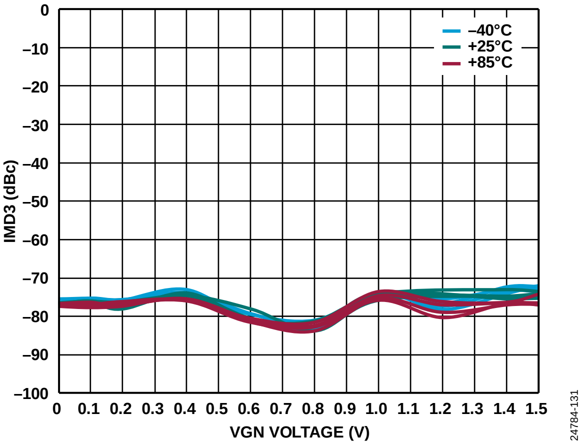


Figure 30. IMD3 vs. VGN Voltage over Temperature and OFSx at 1 GHz

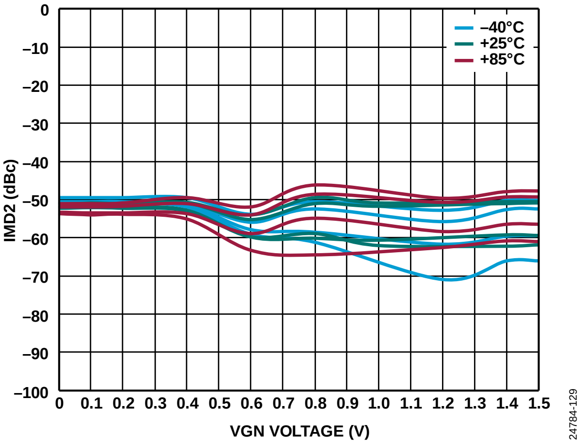


Figure 28. IMD2 vs. VGN Voltage, over Temperature and OFSx at 2 GHz

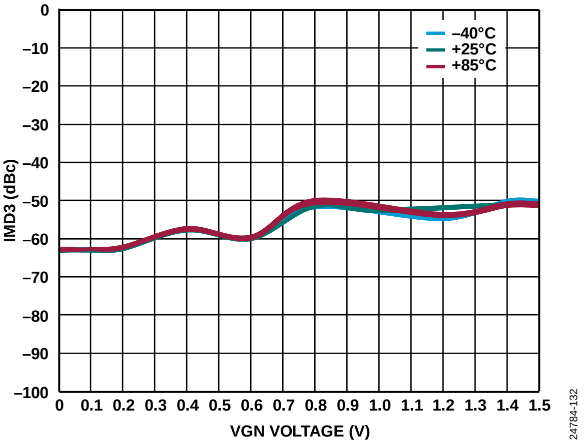


Figure 31. IMD3 vs. VGN Voltage over Temperature and OFSx at 2 GHz

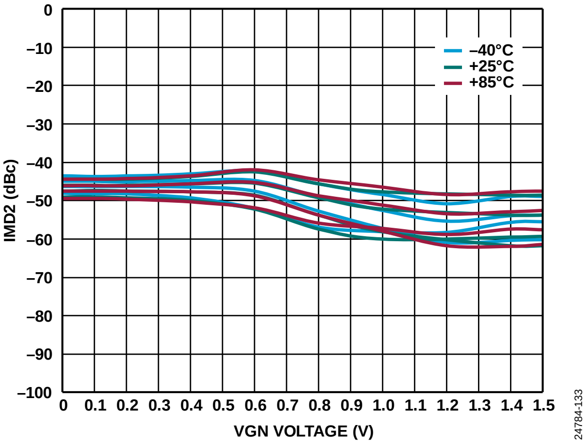


Figure 29. IMD2 vs. VGN Voltage over Temperature and OFSx at 3 GHz

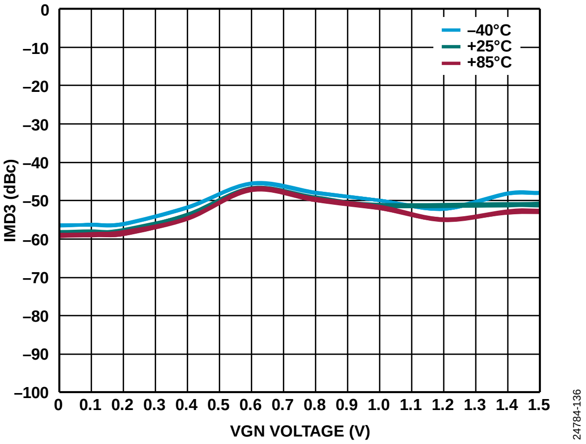


Figure 32. IMD3 vs. VGN Voltage over Temperature and OFSx at 3 GHz

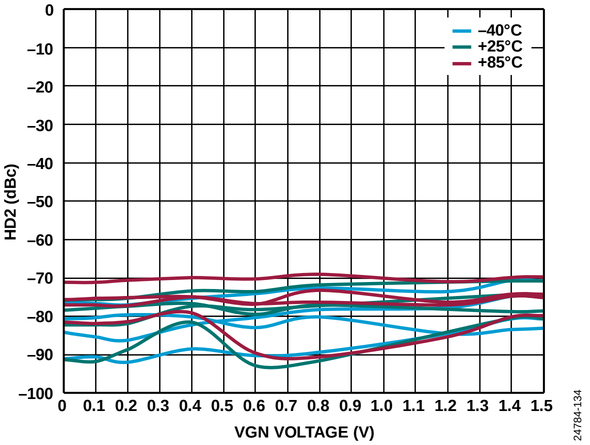


Figure 33. HD2 vs. VGN Voltage over Temperature and OFSx at 500 MHz

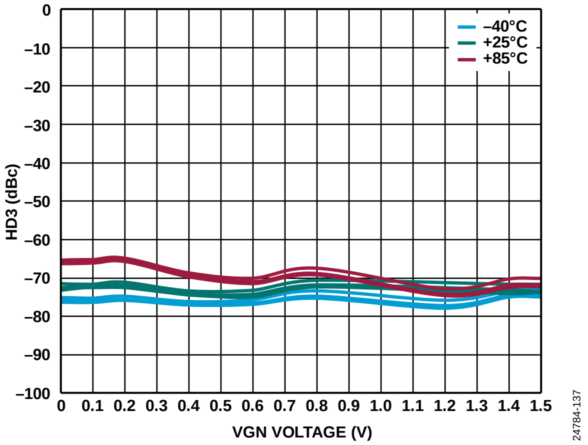


Figure 36. HD3 vs. VGN Voltage over Temperature and OFSx at 500 MHz

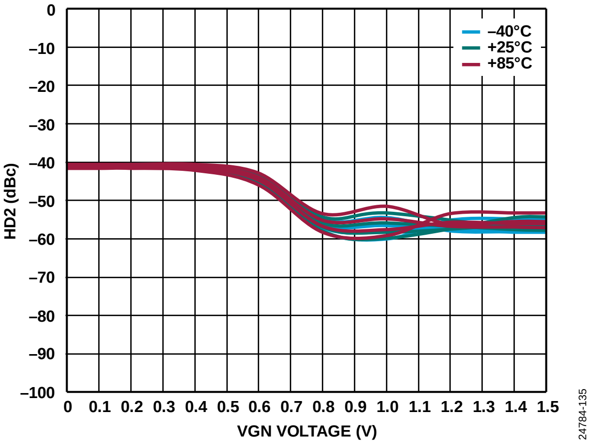


Figure 34. HD2 vs. VGN Voltage over Temperature and OFSx at 1 GHz

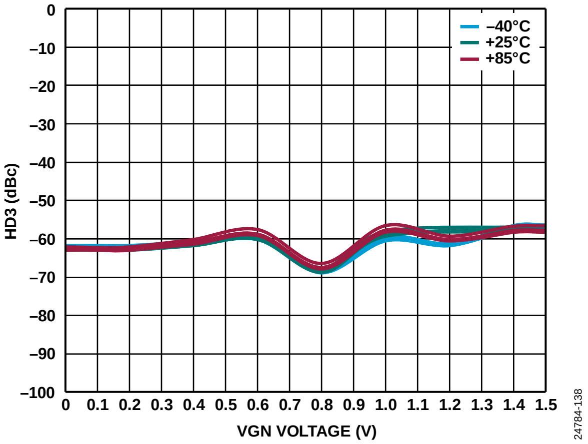


Figure 37. HD3 vs. VGN Voltage over Temperature and VOCM at 1 GHz

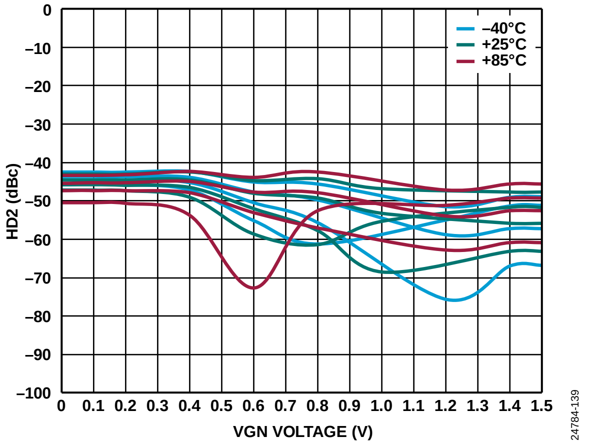


Figure 35. HD2 vs. VGN Voltage over Temperature and OFSx at 2 GHz

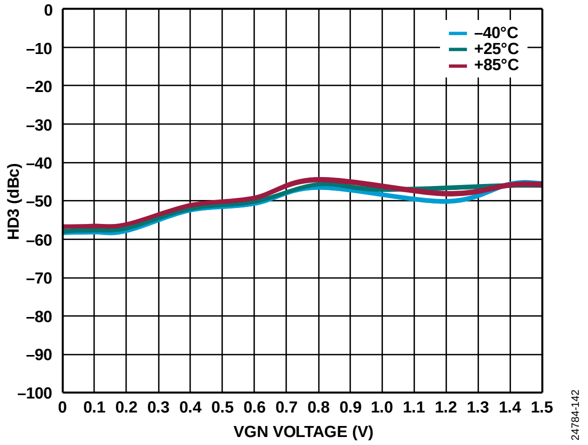


Figure 38. HD3 vs. VGN Voltage over Temperature and OFSx at 2 GHz

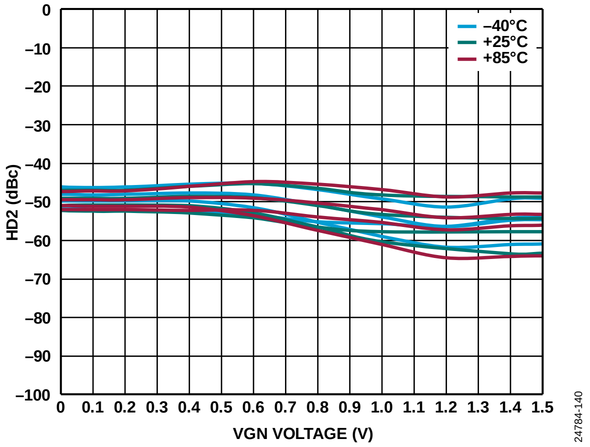


Figure 39. HD2 vs. VGN Voltage over Temperature and OFSx at 3 GHz

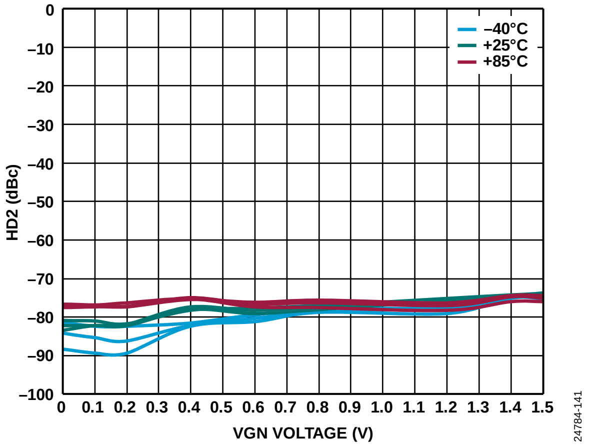


Figure 40. HD2 vs. VGN Voltage over Temperature and VOCM at 500 MHz

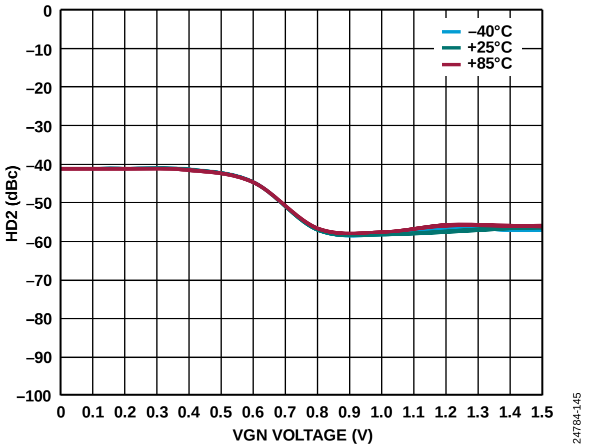


Figure 41. HD2 vs. VGN Voltage over Temperature and VOCM at 1 GHz

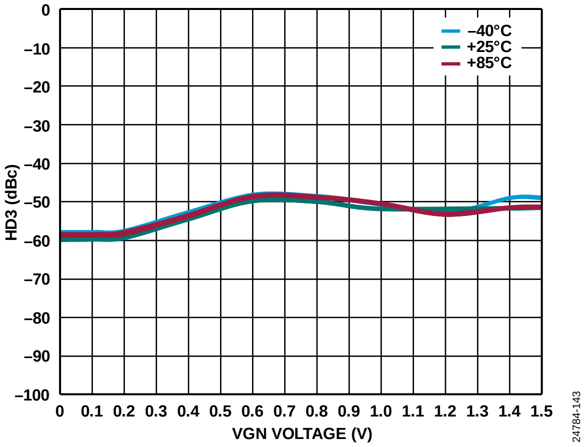


Figure 42. HD3 vs. VGN Voltage over Temperature and OFSx at 3 GHz

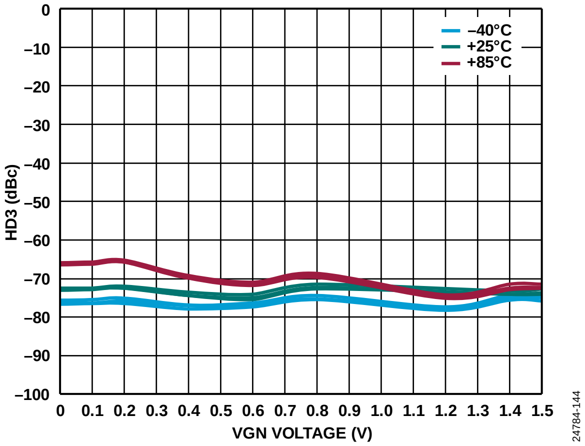


Figure 43. HD3 vs. VGN Voltage over Temperature and VOCM at 500 MHz

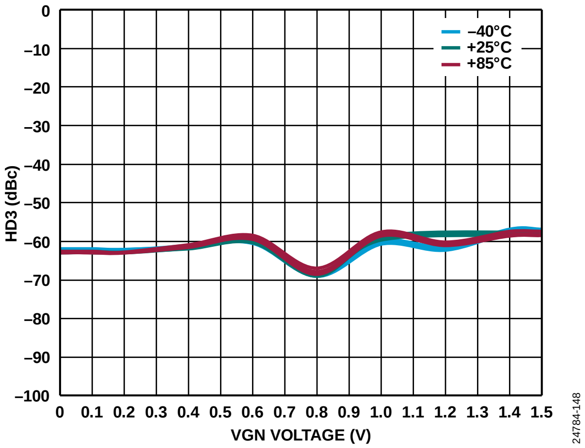


Figure 44. HD3 vs. VGN Voltage over Temperature and VOCM at 1 GHz

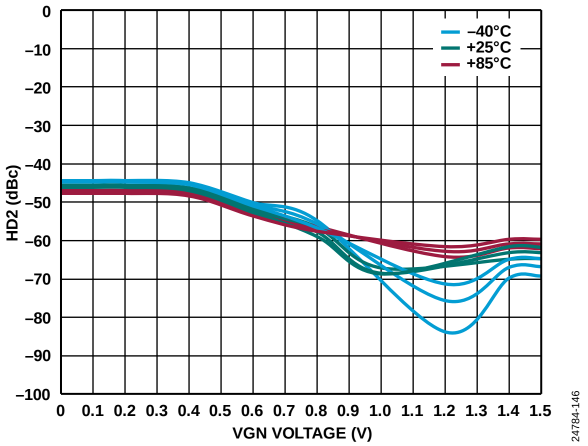


Figure 45. HD2 vs. VGN Voltage over Temperature and VOCM at 2 GHz

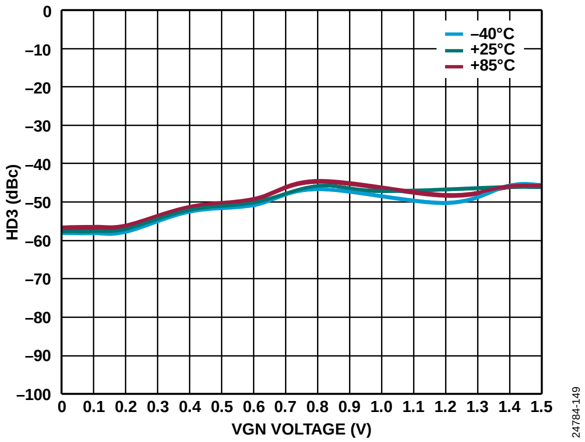


Figure 48. HD3 vs. VGN Voltage over Temperature and VOCM at 2 GHz

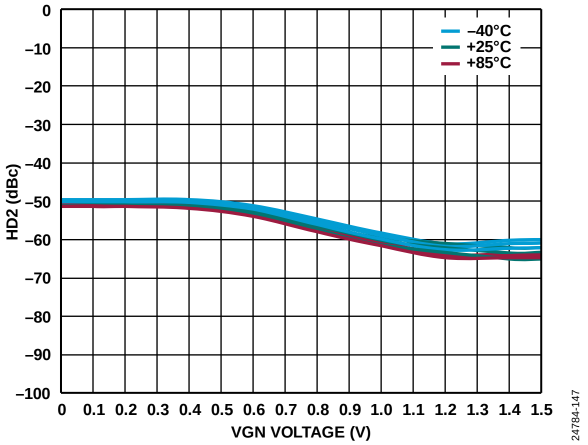


Figure 46. HD2 vs. VGN Voltage over Temperature and VOCM at 3 GHz

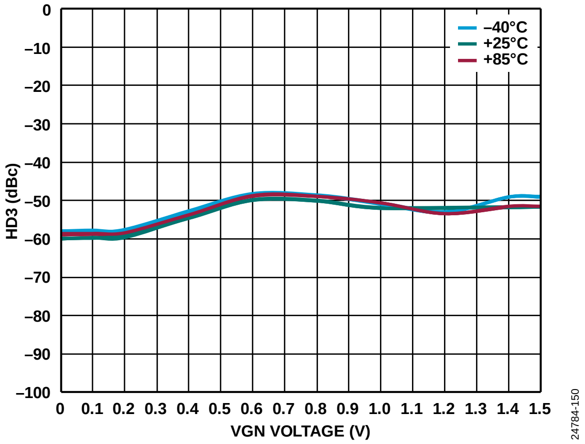


Figure 49. HD3 vs. VGN Voltage over Temperature and VOCM at 3 GHz

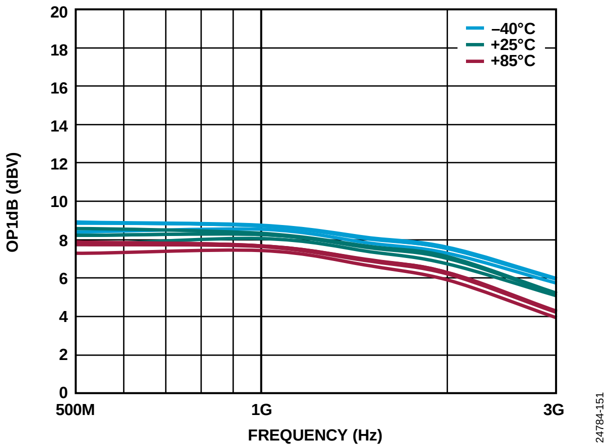


Figure 47. OP1dB vs. Frequency over Temperature and OFSx

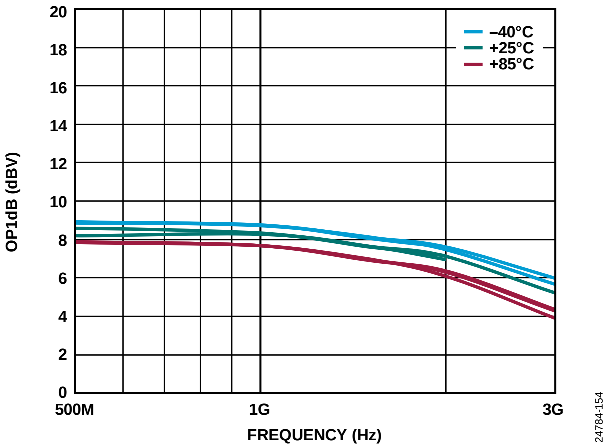


Figure 50. OP1dB vs. Frequency over Temperature and VOCM

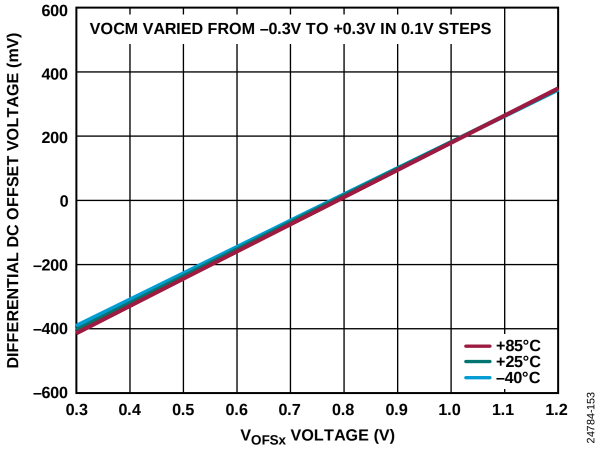


Figure 51. Differential DC Offset Voltage vs. V_{OFSx} Voltage over Temperature and VOCM

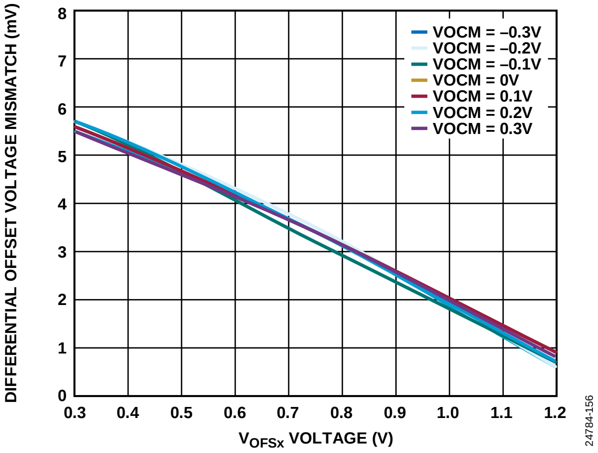


Figure 54. Differential Offset Voltage Mismatch (Channel to Channel) vs. V_{OFSx} Voltage over VOCM

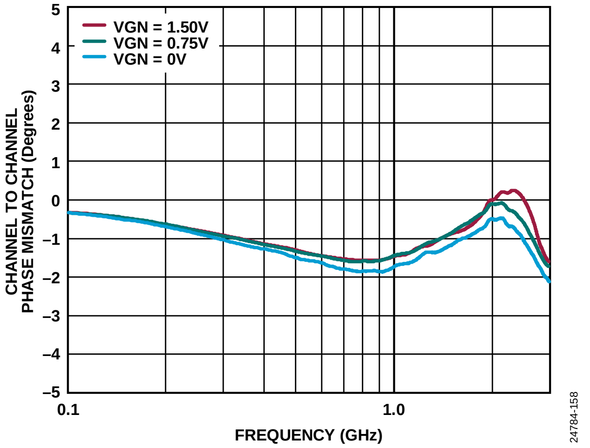


Figure 52. Channel to Channel Phase Mismatch vs. Frequency over VGN

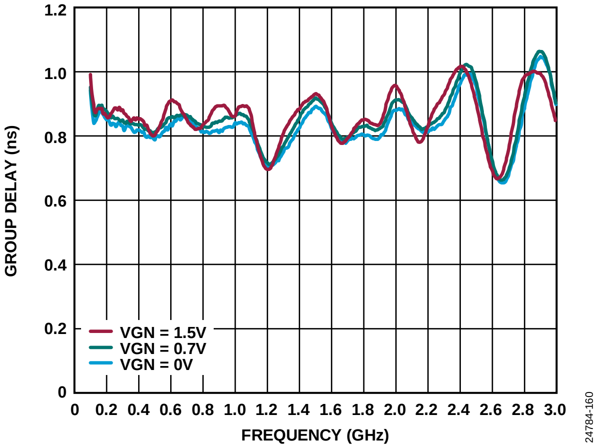


Figure 55. Group Delay vs. Frequency over VGN

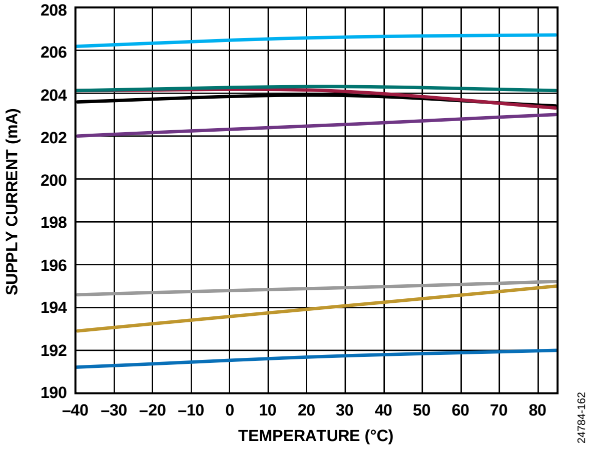


Figure 53. Supply Current vs. Temperature for Multiple Devices

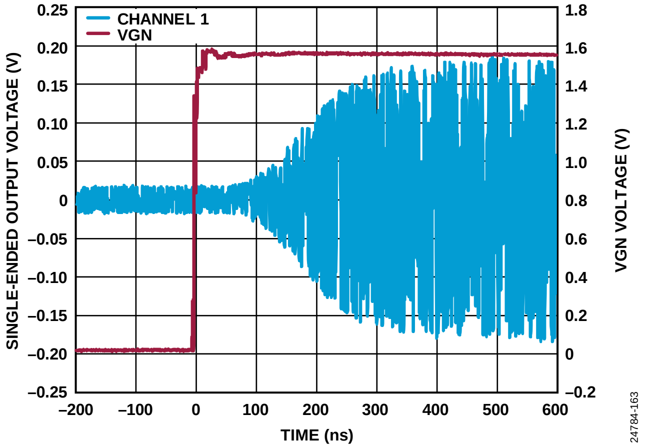


Figure 56. VGA Step Response Rise Time, Minimum to Maximum Gain

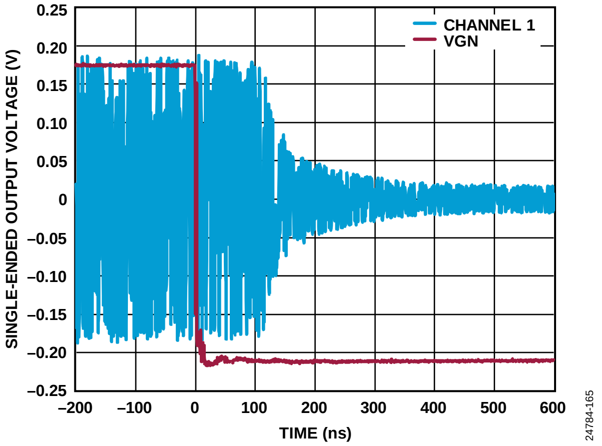


Figure 57. VGA Step Response Fall Time, Maximum to Minimum Gain

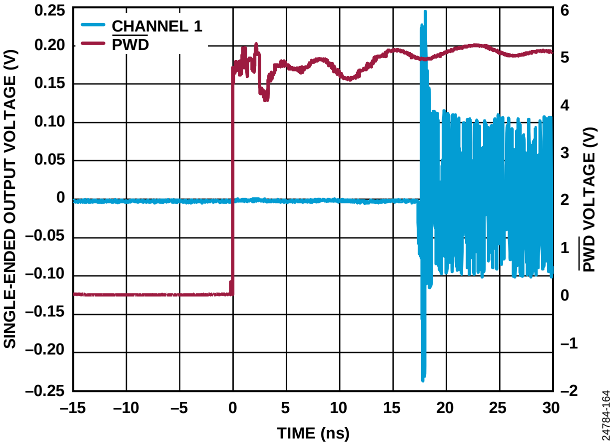


Figure 59. Enable Response Time

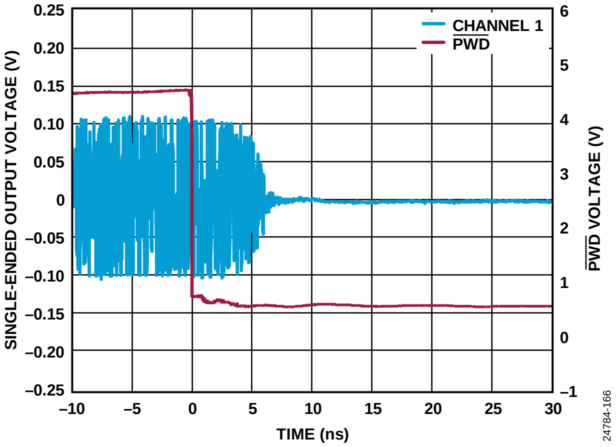


Figure 58. Disable Response Time

DUAL-SUPPLY OPERATION

VPOS = 3 V and VNEG = −2 V, T_A = 25°C, Z_{LOAD} = 186 Ω, VGN = 1.5 V, VOCM = 0 V, OFS1 = OFS2 = 0.75 V, output level = 1.5 V p-p, and 43 Ω back termination de-embedded, unless otherwise noted. Noise figure measured with 100 Ω differential input termination. Worst case IMD2 and IMD3 tone reported. V_{OFSx} sweeps = 0 V, 0.4 V, 0.75 V, or 1.2 V. VOCM sweeps = −0.1 V, 0 V, or +0.1 V.

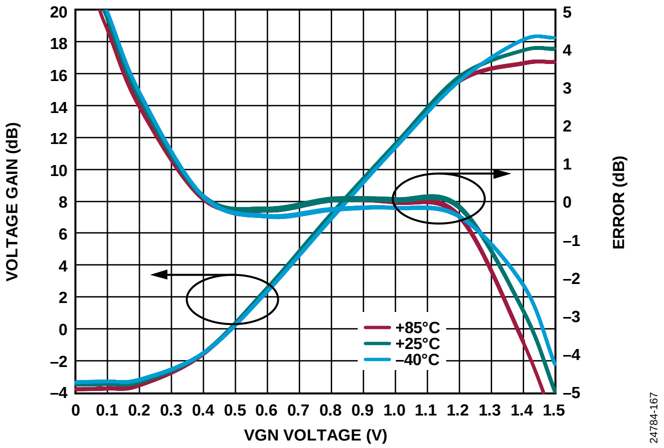


Figure 60. Voltage Gain and Error vs. VGN Voltage over Temperature at 500 MHz

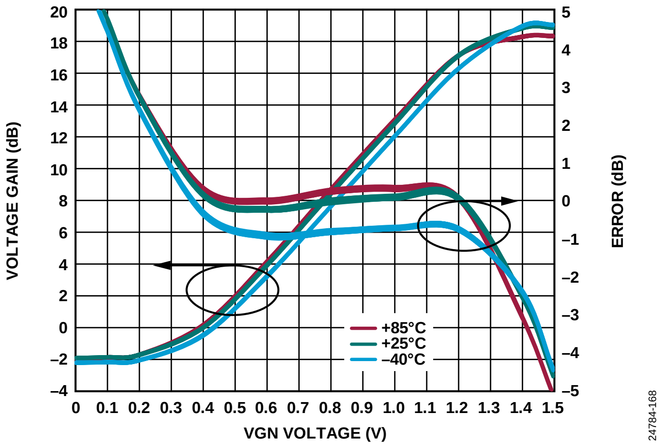


Figure 63. Voltage Gain and Error vs. VGN Voltage over Temperature at 1 GHz

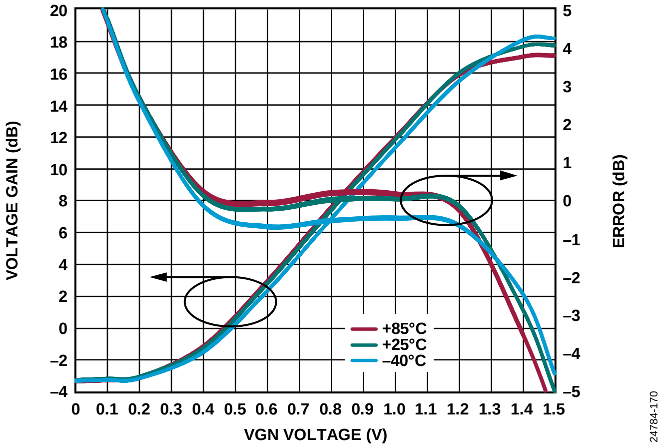


Figure 61. Voltage Gain and Error vs. VGN Voltage over Temperature at 2 GHz

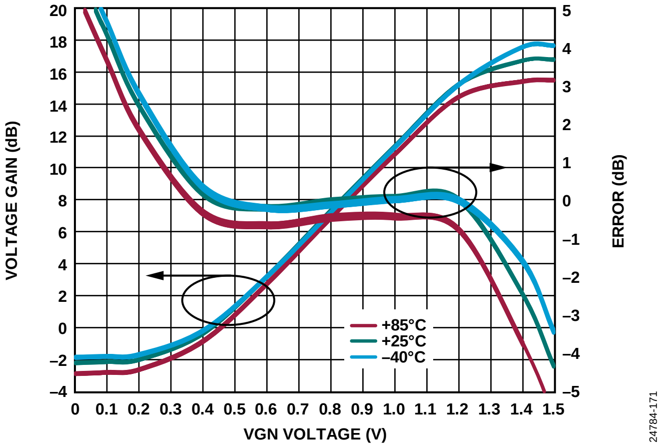


Figure 64. Voltage Gain and Error vs. VGN Voltage over Temperature at 3 GHz

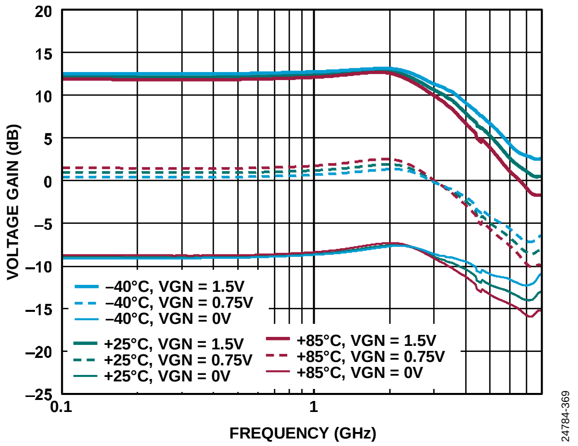


Figure 62. Voltage Gain vs. Frequency, over Temperature and VGN, 43 Ω Back Terminations not De-Embedded

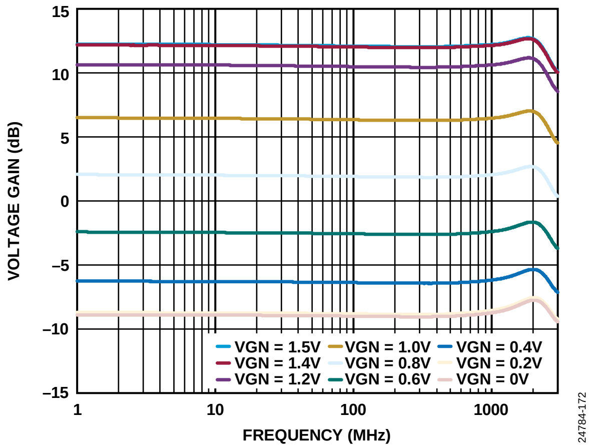


Figure 65. Voltage Gain vs. Frequency over 200 mV VGN Steps, 43 Ω Back Terminations not De-Embedded

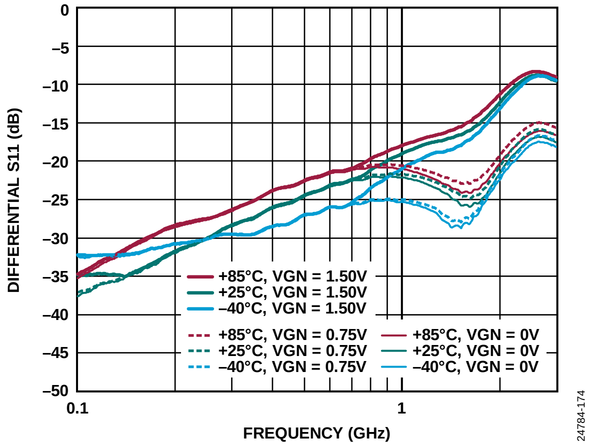


Figure 66. Differential S11 vs. Frequency over Temperature and VGN

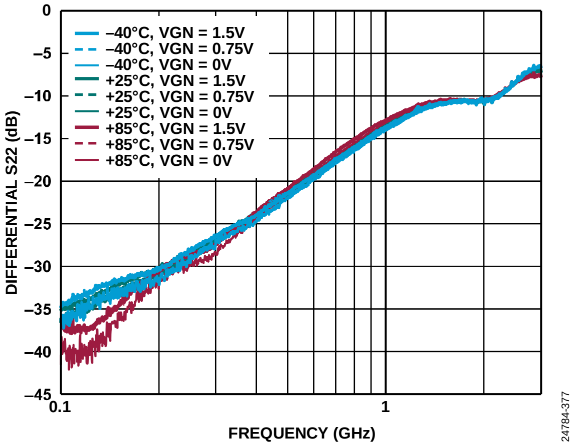


Figure 69. Differential S22 vs. Frequency over Temperature and VGN with 43 Ω Back Terminations

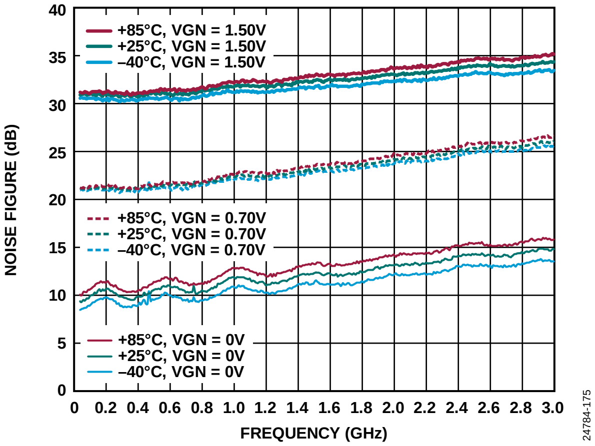


Figure 67. Noise Figure vs. Frequency over Temperature and VGN

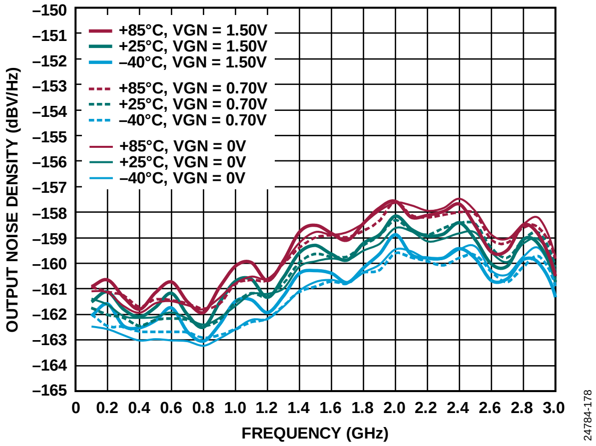


Figure 70. Output Noise Density vs. Frequency over Temperature and VGN

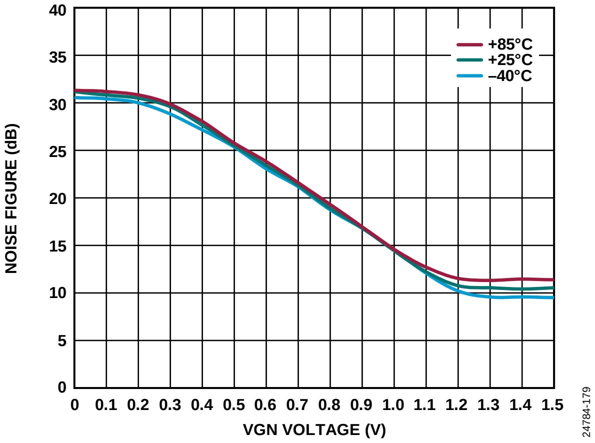


Figure 68. Noise Figure vs. VGN Voltage over Temperature at 500 MHz

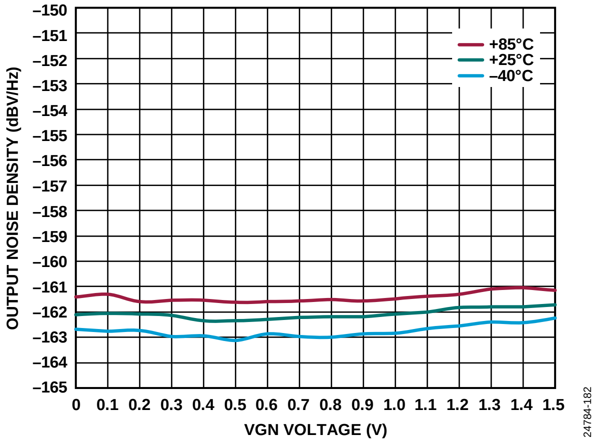


Figure 71. Output Noise Density vs. VGN Voltage over Temperature at 500 MHz

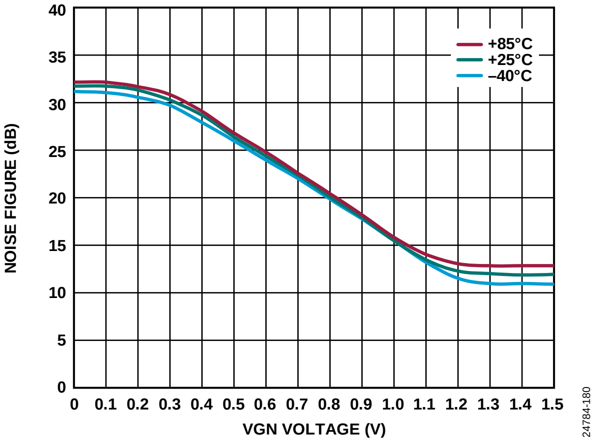


Figure 72. Noise Figure vs. VGN Voltage over Temperature at 1 GHz

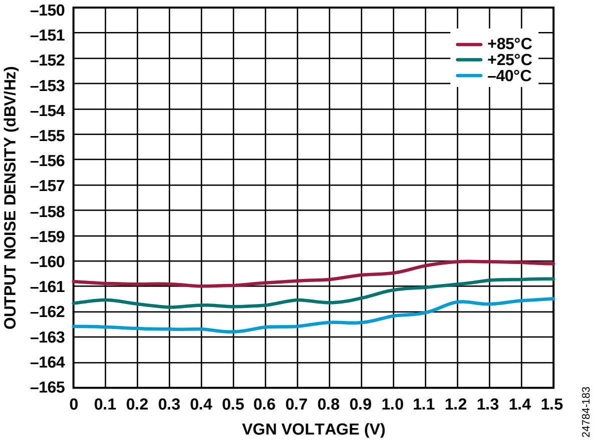


Figure 75. Output Noise Density vs. VGN Voltage over Temperature at 1 GHz

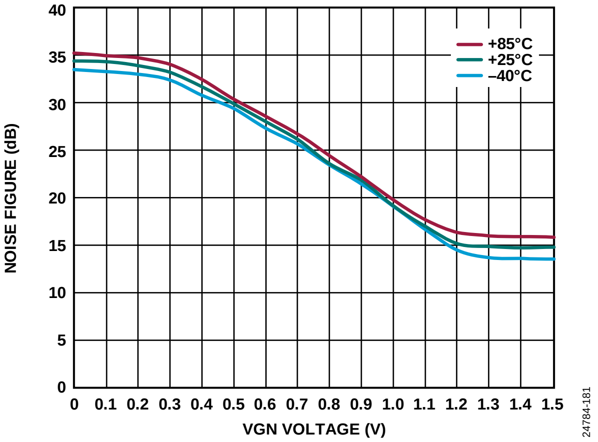


Figure 73. Noise Figure vs. VGN Voltage over Temperature at 2 GHz

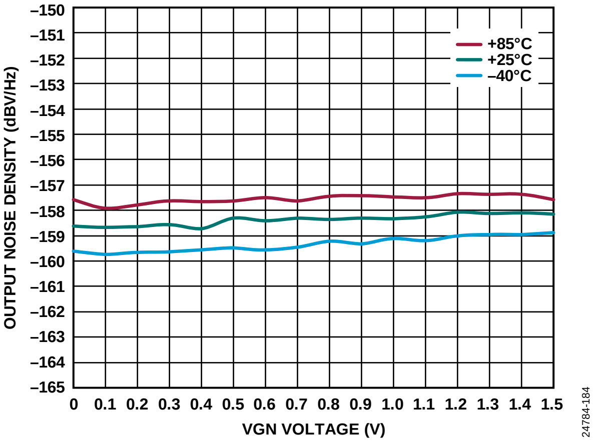


Figure 76. Output Noise Density vs. VGN Voltage over Temperature at 2 GHz

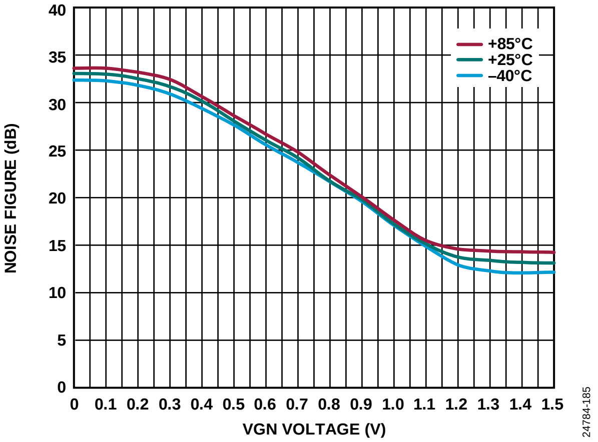


Figure 74. Noise Figure vs. VGN Voltage over Temperature at 3 GHz

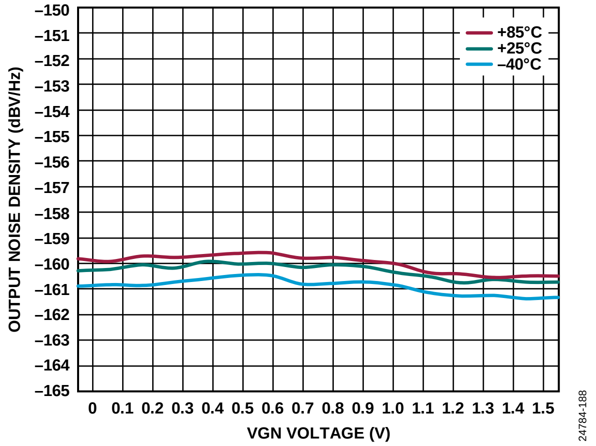


Figure 77. Output Noise Density vs. VGN Voltage over Temperature at 3 GHz

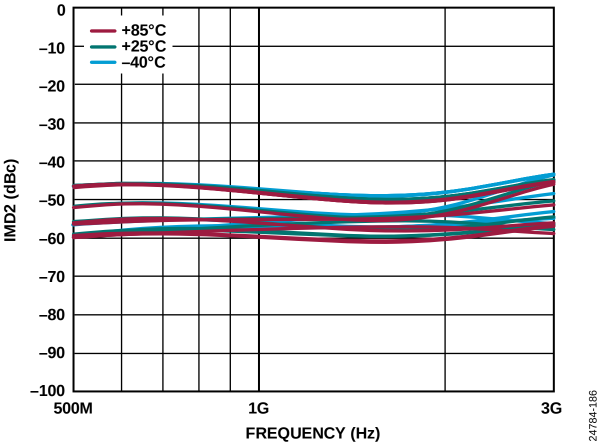


Figure 78. IMD2 vs. Frequency over Temperature and VGN

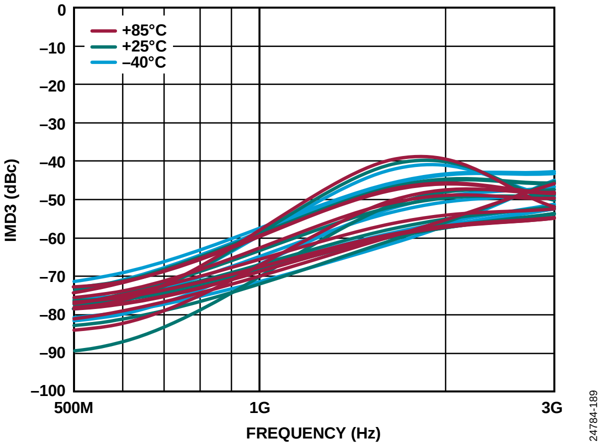


Figure 81. IMD3 vs. Frequency over Temperature and VGN

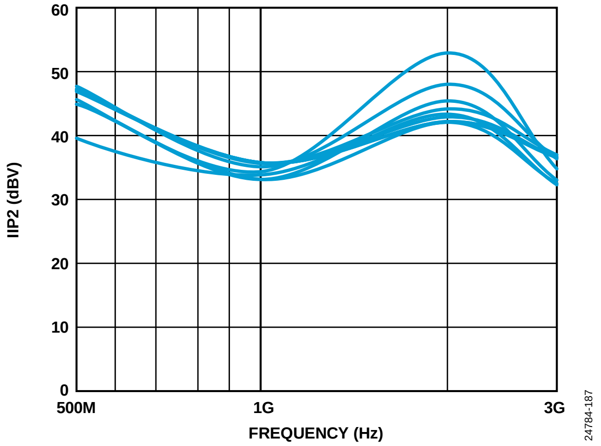


Figure 79. IIP2 vs. Frequency over VGN in 200 mV Steps

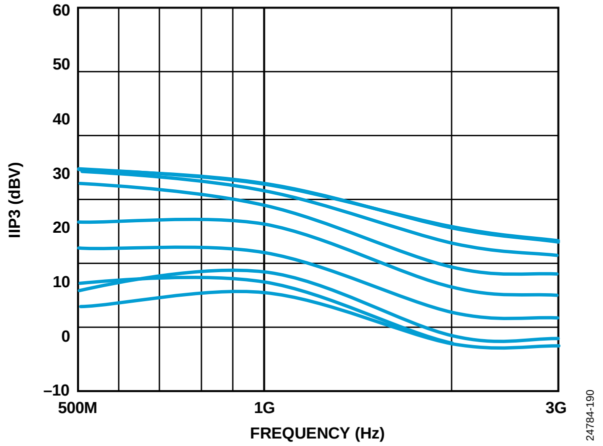


Figure 82. IIP3 vs. Frequency over VGN in 200 mV Steps

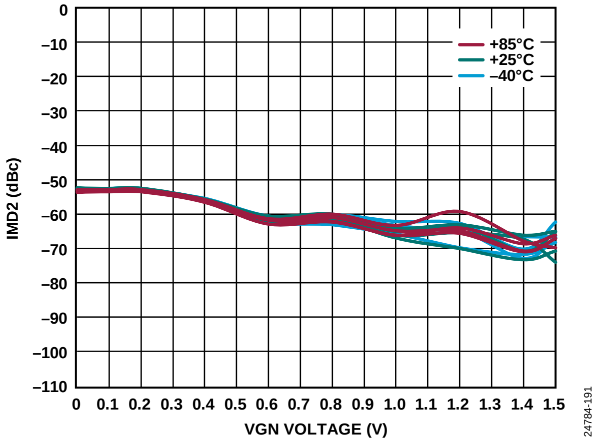


Figure 80. IMD2 vs. VGN Voltage over Temperature and OFSx at 500 MHz

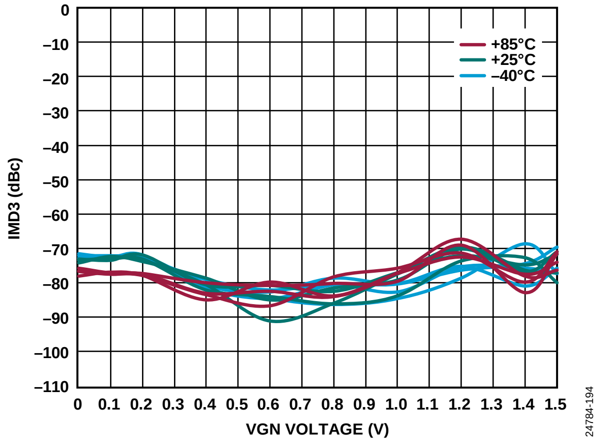


Figure 83. IMD3 vs. VGN Voltage over Temperature and OFSx at 500 MHz

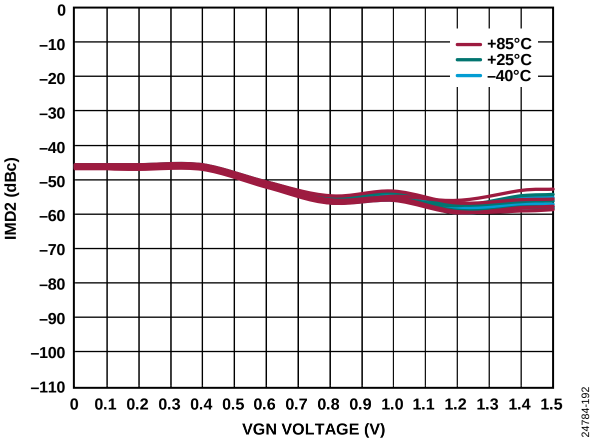


Figure 84. IMD2 vs. VGN Voltage over Temperature and OFSx at 1 GHz

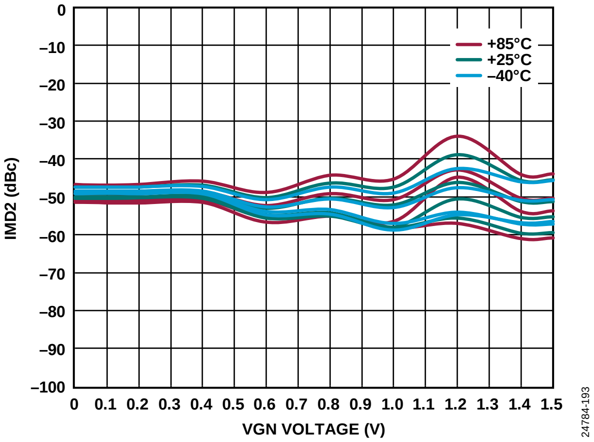


Figure 85. IMD2 vs. VGN Voltage over Temperature and OFSx at 2 GHz

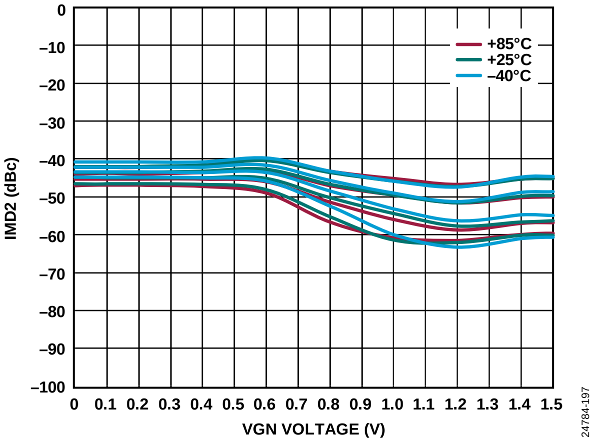


Figure 86. IMD2 vs. VGN Voltage over Temperature and OFSx at 3 GHz

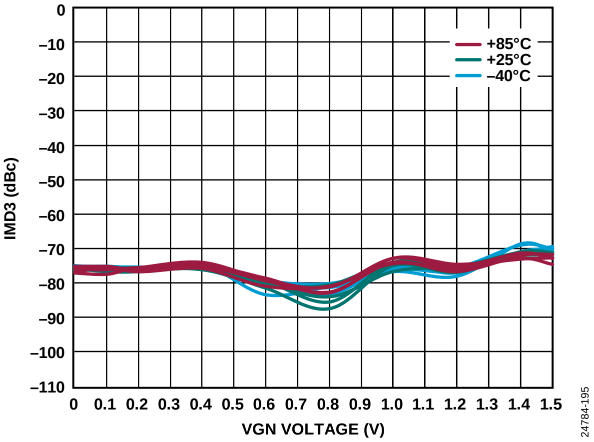


Figure 87. IMD3 vs. VGN Voltage over Temperature and OFSx at 1 GHz

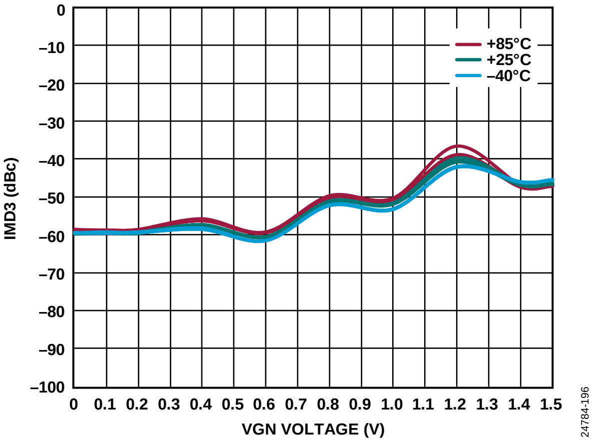


Figure 88. IMD3 vs. VGN Voltage over Temperature and OFSx at 2 GHz

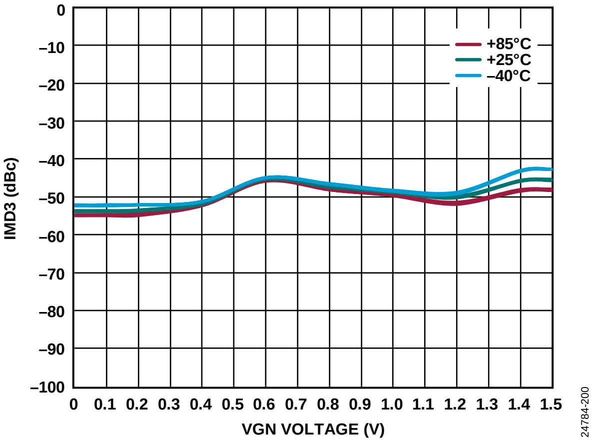


Figure 89. IMD3 vs. VGN Voltage over Temperature and OFSx at 3 GHz

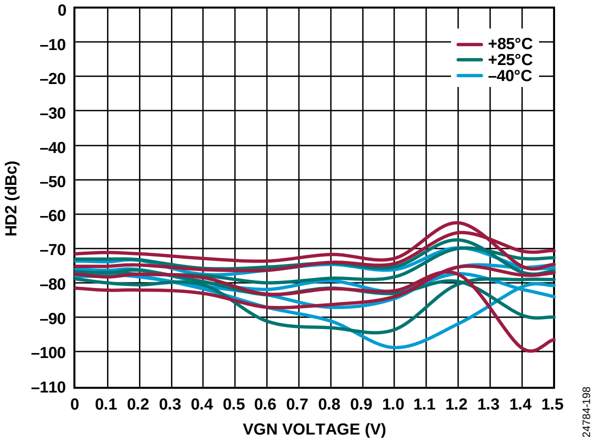


Figure 90. HD2 vs. VGN Voltage over Temperature and OFSx at 500 MHz

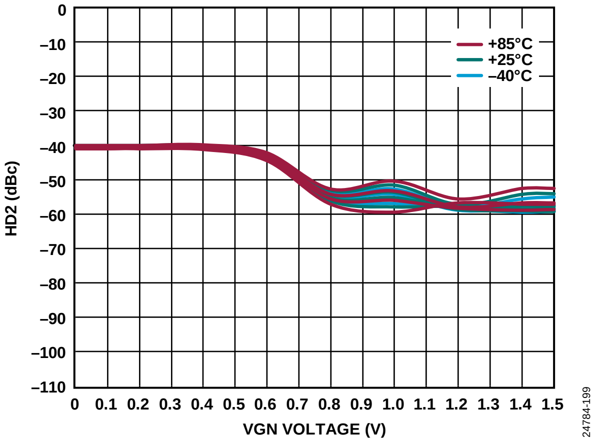


Figure 91. HD2 vs. VGN Voltage over Temperature and OFSx at 1 GHz

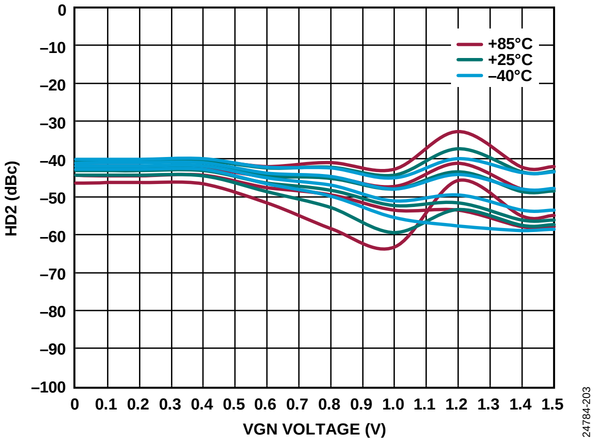


Figure 92. HD2 vs. VGN Voltage over Temperature and OFSx at 2 GHz

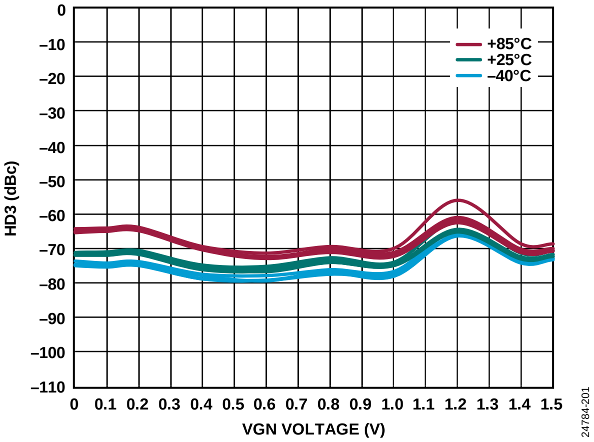


Figure 93. HD3 vs. VGN Voltage over Temperature and OFSx at 500 MHz

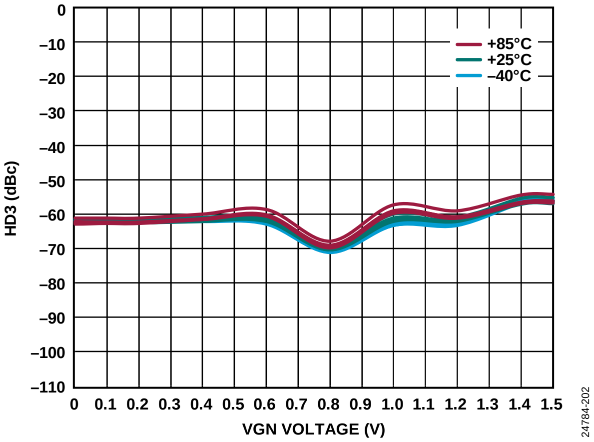


Figure 94. HD3 vs. VGN Voltage over Temperature and OFSx at 1 GHz

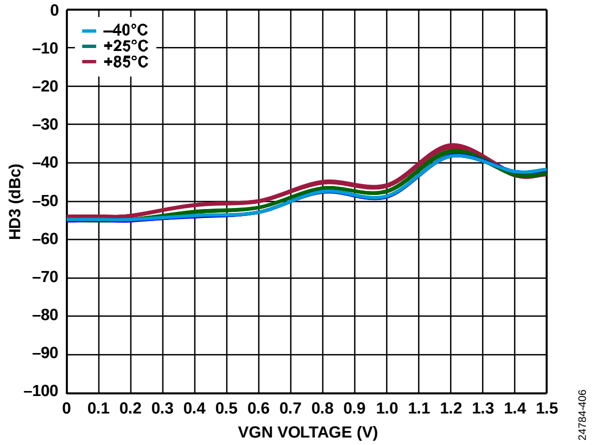


Figure 95. HD3 vs. VGN Voltage over Temperature and OFSx at 2 GHz

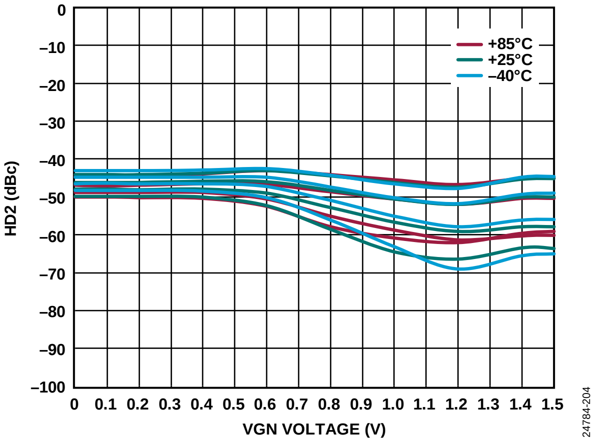


Figure 96. HD2 vs. VGN Voltage over Temperature and OFSx at 3 GHz

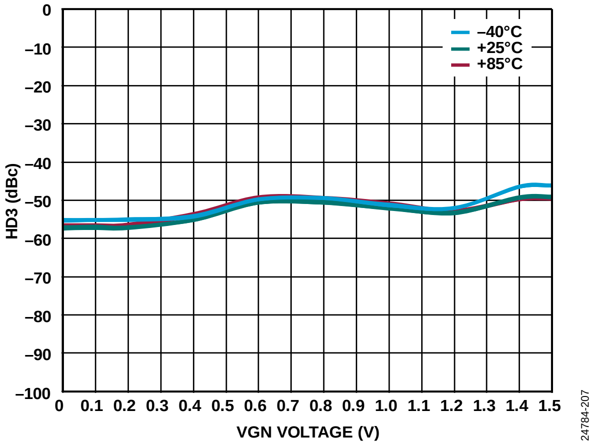


Figure 99. HD3 vs. VGN Voltage over Temperature and OFSx at 3 GHz

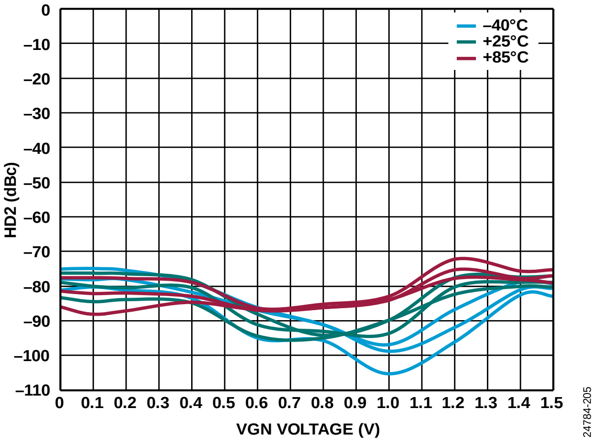


Figure 97. HD2 vs. VGN Voltage over Temperature and VOCM at 500 MHz

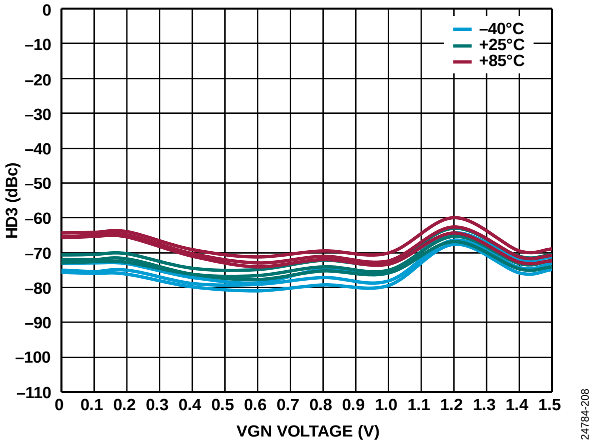


Figure 100. HD3 vs. VGN Voltage over Temperature and VOCM at 500 MHz

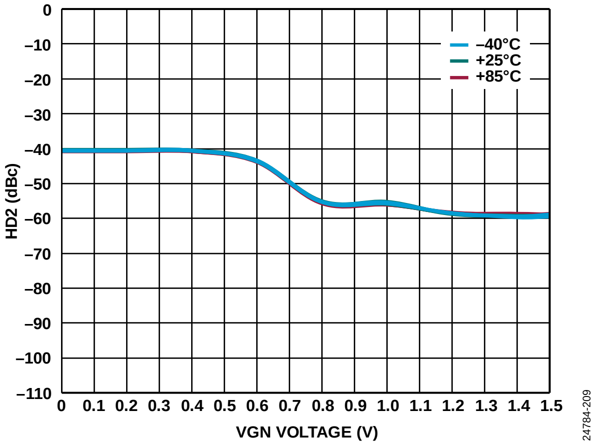


Figure 98. HD2 vs. VGN Voltage over Temperature and VOCM at 1 GHz

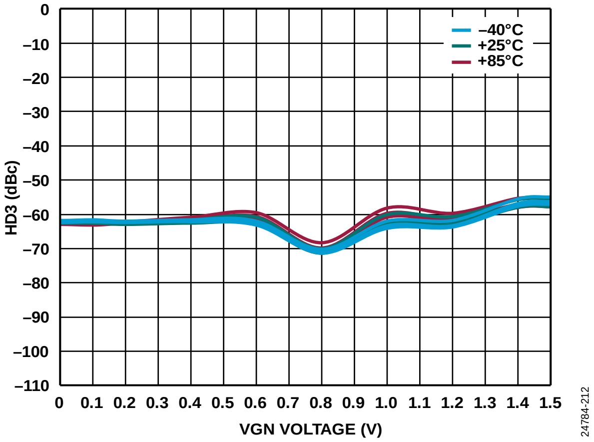


Figure 101. HD3 vs. VGN Voltage over Temperature and VOCM at 1 GHz

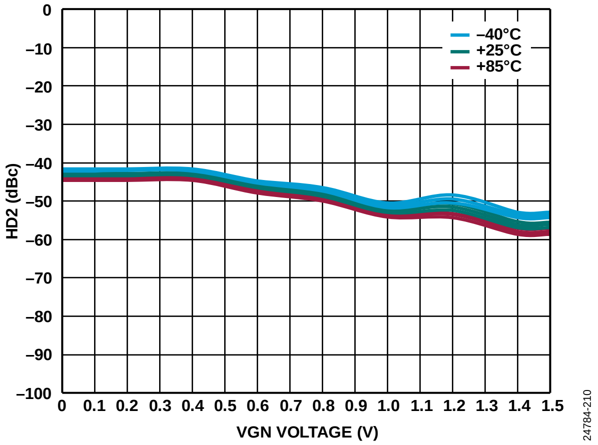


Figure 102. HD2 vs. VGN Voltage over Temperature and VOCM at 2 GHz

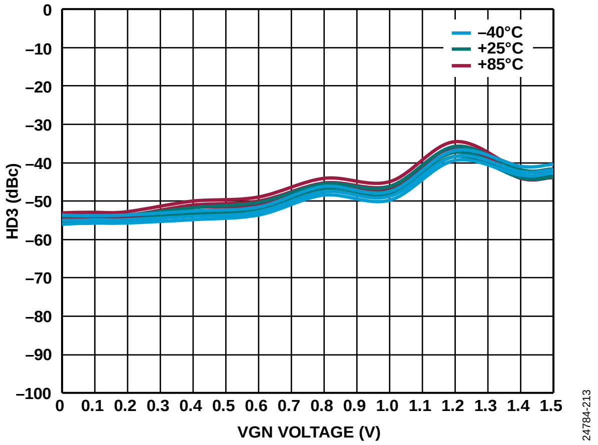
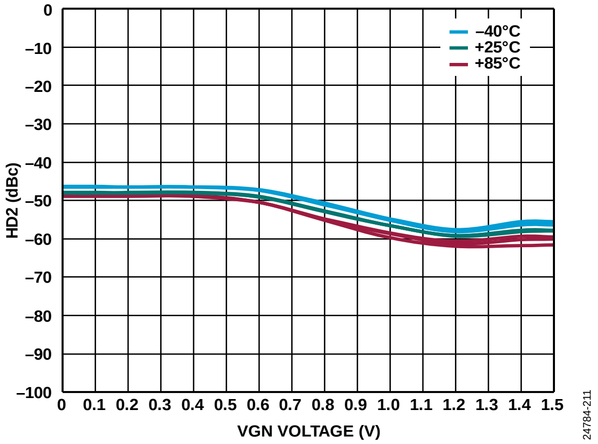


Figure 105. HD3 vs. VGN Voltage over Temperature and VOCM at 2 GHz



`Figure 103. HD2 vs. VGN Voltage over Temperature and VOCM at 3 GHz

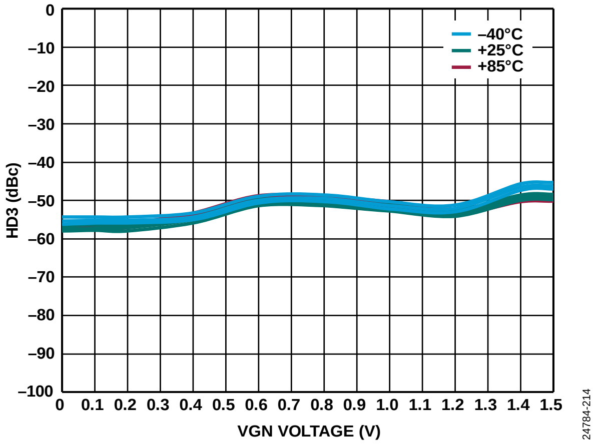


Figure 106. HD3 vs. VGN Voltage over Temperature and VOCM at 3 GHz

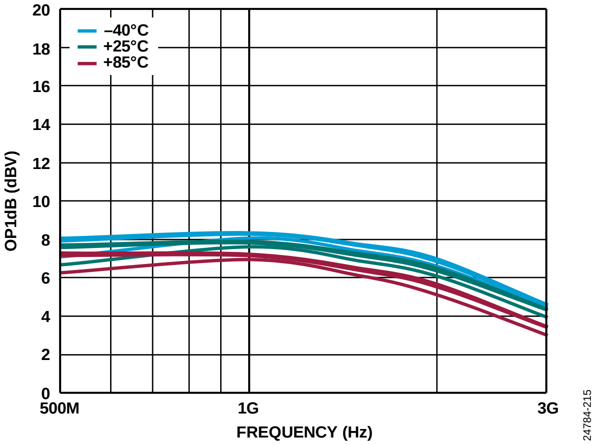


Figure 104. OP1dB vs. Frequency over Temperature and OFSx at Maximum Gain

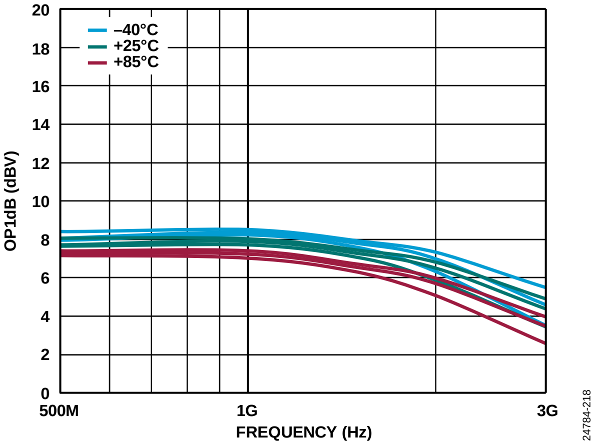


Figure 107. OP1dB vs. Frequency over Temperature and VOCM at Maximum Gain

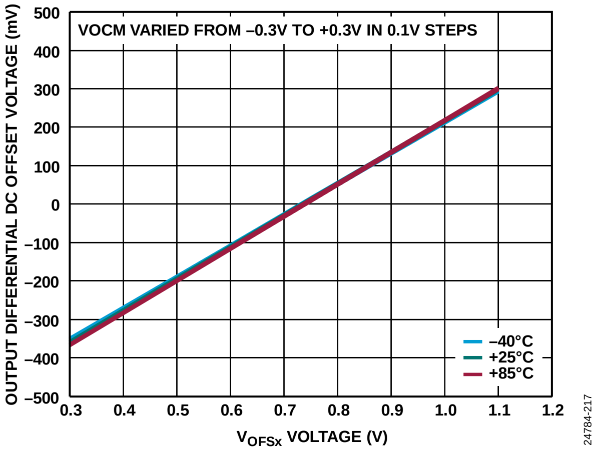


Figure 108. Output Differential DC Offset Voltage vs. V_{OFSx} Voltage over Temperature and VOCM

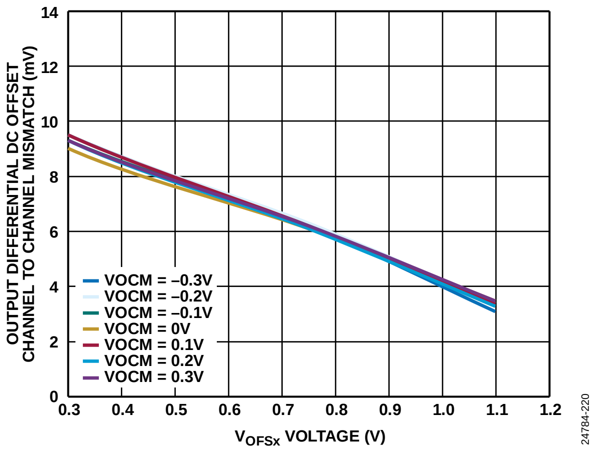


Figure 111. Output Differential DC Offset Channel to Channel Mismatch vs. V_{OFSx} Voltage over VOCM

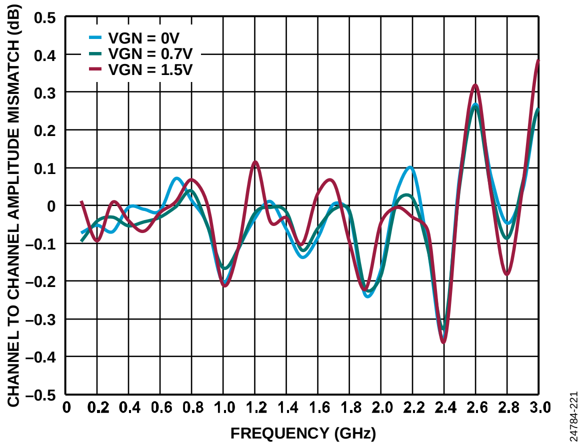


Figure 109. Channel to Channel Amplitude Mismatch vs. Frequency over VGN

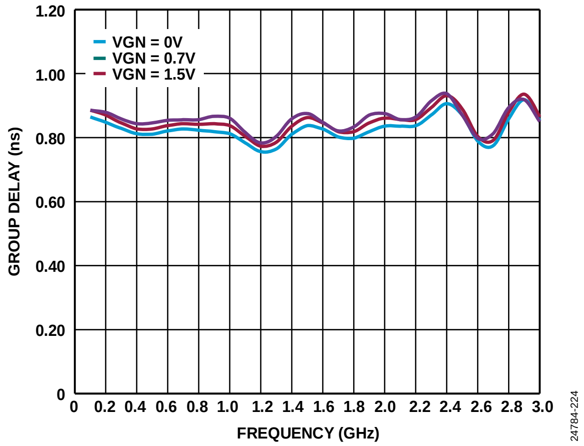


Figure 112. Group Delay vs. Frequency over VGN

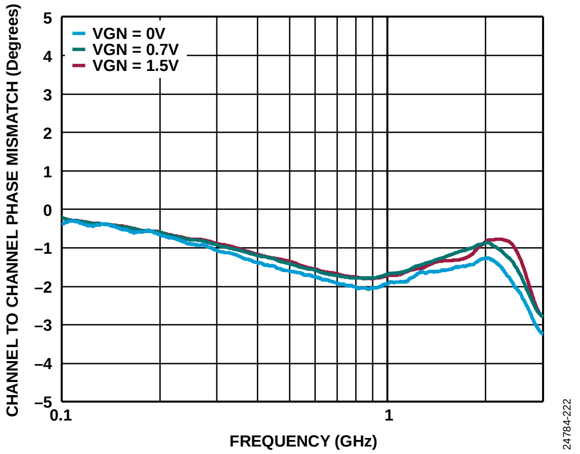


Figure 110. Channel to Channel Phase Mismatch vs. Frequency over VGN

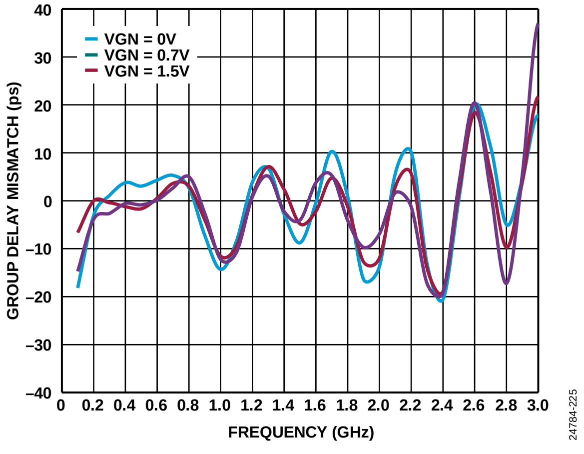


Figure 113. Group Delay Mismatch (Channel to Channel) vs. Frequency over VGN

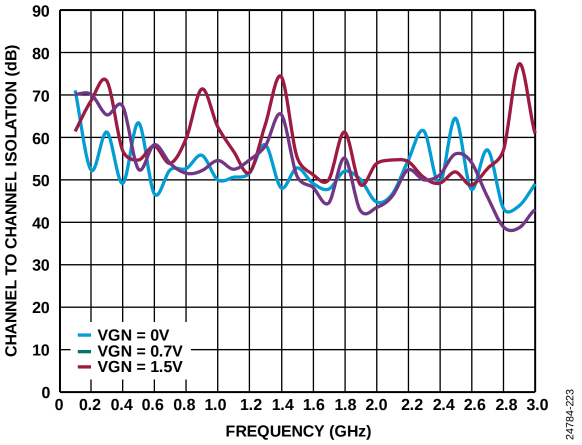


Figure 114. Channel to Channel Isolation vs. Frequency over VGN

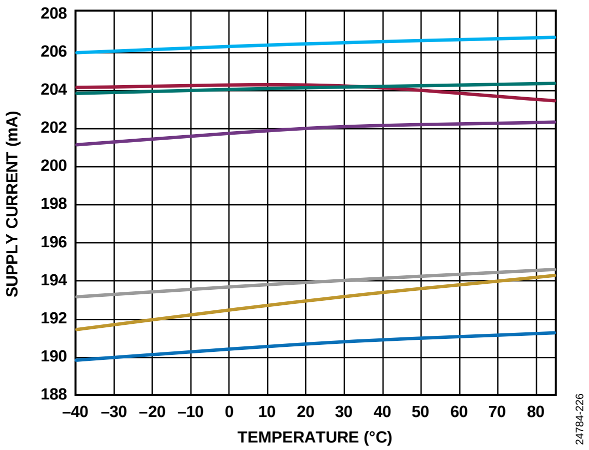


Figure 117. Supply Current vs. Temperature over Multiple Devices

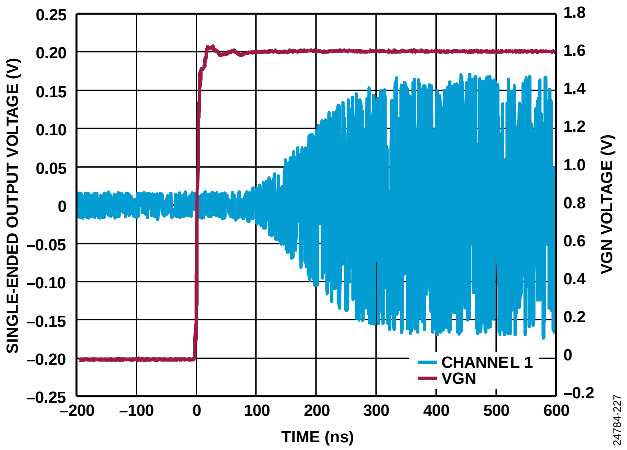


Figure 115. VGA Step Response Time, Minimum to Maximum Gain

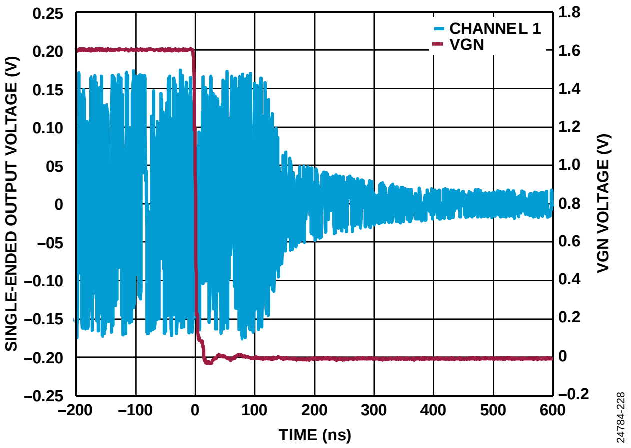


Figure 118. VGA Step Response Time, Maximum to Minimum Gain

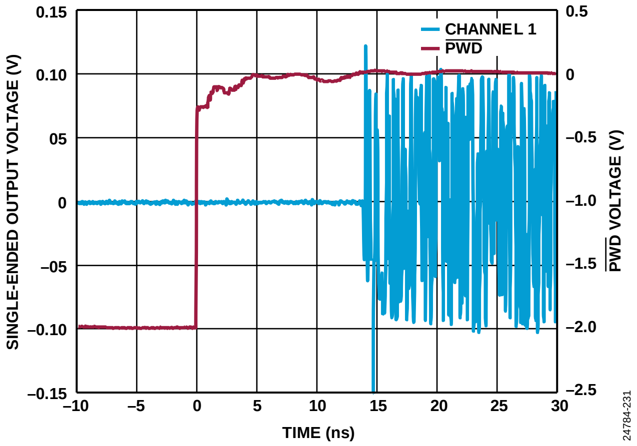


Figure 116. Enable Response Time

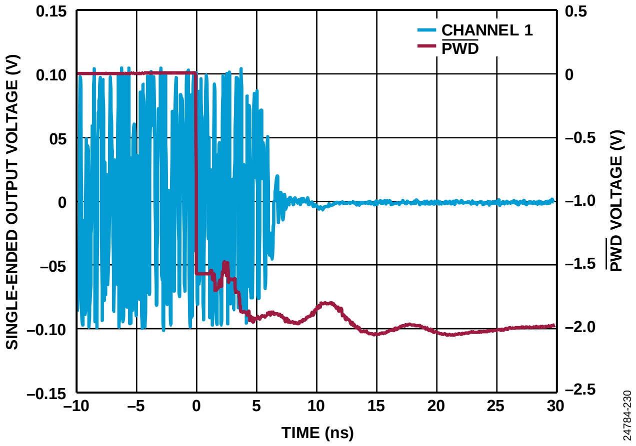


Figure 119. Disable Response Time

THEORY OF OPERATION

The ADRF6521 is a highly linear, dual channel VGA with a −3 dB frequency response of 3.25 GHz. The ADRF6521 consists of a matched pair of VGAs, each consisting of a voltage variable attenuator (VVA) designed to have 21 dB of attenuation range at room temperature (T_A = 25°C), followed by an 18 dB amplifier, producing a gain range from +18 dB to −3 dB.

The output stage has the ability to change its common-mode voltage and have a purposeful dc offset voltage. The output common-mode voltage range and output dc offset voltage range are adjustable up to ±200 mV and ±400 mV, respectively, while still maintaining the high linearity outlined in Table 1. Larger ranges are possible, but linearity degrades. Figure 120 shows the simplified block diagram of a single channel.

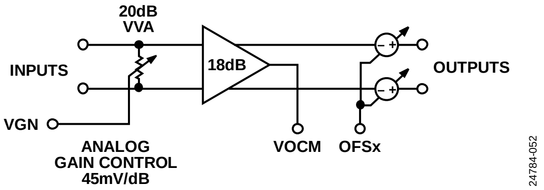


Figure 120. Simplified Functional Block Diagram for a Single Channel

The entire differential signal chain is dc-coupled. However it is recommended to ac-couple the input signal paths. The gain setting control for the two channels is a shared pin (VGN), ensuring close matching of their magnitude and phase responses. The ADRF6521 is fully disabled by pulling $\overline{\text{PWD}}$ to the VNEG supply.

INPUT VVAs

The input VVAs are designed to have high linearity and excellent log conformance. The VVAs have a differential input impedance of 100 Ω and an attenuation range of 21 dB, which decreases slightly over temperature. If the input must be dc-coupled, the output common mode of the previous stage must match the voltage on the VOCM pin. The topology of an input VGA, for example, the VVA located at the input of the device, is such that the noise figure degrades dB for dB as attenuation increases. The VVA maintains its high linearity across its full range of attenuation.

AMPLIFIERS

The ADRF6521 amplifiers use the same core as the ADL5569. The amplifiers have a low output impedance (<20 Ω), and the R_F to R_G on-chip resistor ratio is approximately 8×, which creates the 18 dB of differential voltage gain. The amplifiers are designed to drive subsequent amplifier stages and are capable of high linearity with 1.5 V p-p two-tone signals into 100 Ω differential loads.

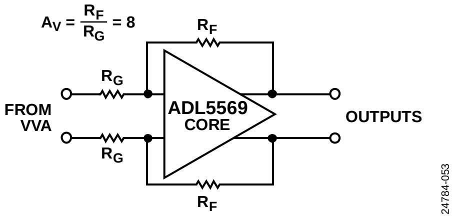


Figure 121. 18 dB Amplifier for a Single Channel

OUTPUT COMMON-MODE VOLTAGE

The output common-mode voltage is set internally to (VPOS + VNEG)/2, with an on-chip resister divider (see Figure 122). This voltage can be adjusted ±200 mV via the VOCM pin and the ADRF6521 still maintains IMD2, IMD3, HD2, and HD3 of −55 dBc or better. There is a 1 to 1 mapping between the control voltage applied to VOCM and the output common-mode voltage.

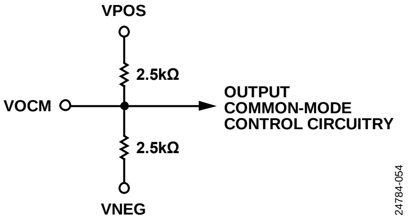


Figure 122. VOCM Simplified Circuit

OUTPUT DC OFFSET CIRCUIT

The output dc offset on each channel of the ADRF6521 can be independently nulled out to account for the small inherent dc offsets of the VVA and amplifier. For applications such as predistortion, the output dc offset voltage of each channel can intentionally be increased up to ±400 mV in addition to the ±200 mV output common-mode range, while still maintaining high linearity. Adjusting the output common-mode and the output dc offset voltage more than a combined 400 mV from the nominal voltage on any output pin causes the linearity to degrade, possibly to IMDx and/or HDx levels worse than −55 dBc.

The output dc offset voltage is defined as follows:

$$V_{OFS\_DC} = V_{OPPx} - V_{OPMx}$$

where V_{OPPx} and V_{OPMx} are the dc voltages on the OPP1 and OPM1 or the OPP2 and OPM2 output pins.

The output dc offset voltage is controlled via the OFS1 pin and OFS2 pin, shown in Figure 120 and Figure 124 as a generic OFSx pin. The output dc offset voltage is fundamentally caused by injecting a differential current into the input of the amplifier. The differential current consists of the following:

- A reference current (I_{REF}), which is added to both the positive and negative legs of the differential path
- A bipolar offset current (I_{OFS}), which is added on one leg of the differential path and subtracted from the other leg

The reference current is a static current, but the bipolar offset current is controlled via the respective OFSx pins. Both currents are injected between the 18 dB amplifier and VVA. Because the offset current is bipolar, the output dc offset voltage goes up to +400 mV or down to −400 mV. The nominal closed form equation between the control voltage on the FLTx pins and the output dc offset voltage is

$$V_{DC\_OFFSET\_DIFF} = 0.89 \times V_{OFSx} - 0.668\text{ V}$$

DC Offset Loop High-Pass Corner

The ADRF6521 has dc offset loops that null any signal below their low-pass frequency corner, which is set by a combination of the internal 35 pF capacitor plus any external capacitor decoupled to VNEG from OFSx.

Although the dc offset loops have a low-pass response, the signal paths show a high-pass response because the loops null any low frequency signal below their low-pass corner. The following equation shows the relationship between the high-pass corner observed on the signal paths and the value of the external capacitor decoupled to VNEG, which is called C_{OFS}:

$$f_{HP}\text{ (Hz)} = 60/(C_{OFS}\text{ (µF)} + 35 \times 10^{-6})$$

With C_{OFS} = 1 µF, the high-pass corner in Hz is calculated as:

$$f_{HP}\text{ (Hz)} = 60/(1 + 35 \times 10^{-6}) = 60\text{ Hz}$$

The feedback loop shown in Figure 124 creates the output dc offset voltage. The differential to single-ended amplifier samples the differential output, converts the signal into single-ended mode, and averages the signal with a capacitor connected to VNEG. This averaged version of the output is compared to the dc voltage applied to the OFSx pin(s) with the transconductance amplifier (gm). The output differential current of the gm stage is injected between the R_F and R_G resistors of the 18 dB amplifier. The feedback loop forces the differential current of the gm amplifier to increase or decrease until the averaged voltage from the differential to single-ended amplifier is equal to the applied OFSx voltage. This differential current injected at the input of the amplifier creates an intentional dc offset voltage at the input, which is then amplified and seen on the output pins, OPPx and OPMx.

The output dc offset circuits are filtered on each channel via the FLT1 and FLT2 pins, for Channel 1 and Channel 2, respectively. Connect both pins to the negative supply via a 1 µF capacitor. There is an on-chip capacitance of 35 pF on each FLTx node.

GAIN CONTROL INTERFACE

The ADRF6521 has a linear-in-dB gain control interface. The gain control slope is maintained at 22.2 dB/V over temperature, supply, and process as gain varies from 250 mV to 1200 mV.

The gain function is given by

$$Gain\text{ (dB)} = 22.2 \times V_{VGN} - 8.5$$

where V_{VGN} is the voltage on the VGN gain pin in volts.

The gain control voltage range is from 0 V to 1.5 V, with respect to analog ground.

POWER-DOWN FUNCTION

The power-down function is accomplished via the $\overline{\text{PWD}}$ pin. By default, the device is enabled via the resistive divider shown in Figure 123. Assert the $\overline{\text{PWD}}$ pin to the same potential as VNEG to reduce the current consumption to roughly 25 mA. Do not apply a voltage more than VNEG + 3.3 V on the $\overline{\text{PWD}}$ pin. Higher voltages may cause damage to the device.

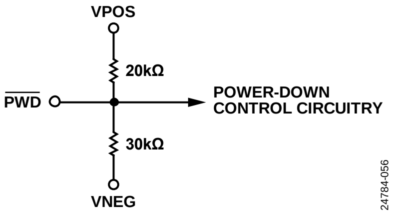


Figure 123. Simplified Power Down Interface

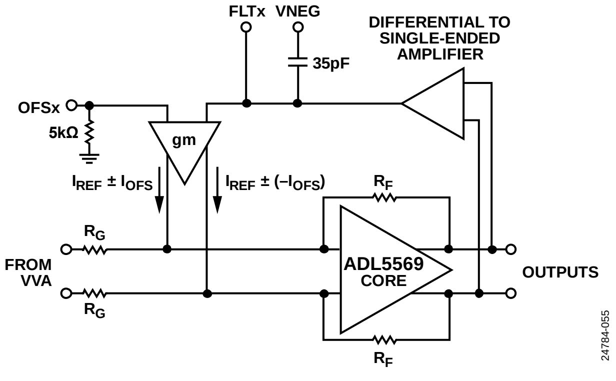


Figure 124. Output DC Offset Circuit for a Single Channel

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 125 shows the basic connections for a typical ADRF6521 application.

SUPPLY DECOUPLING

Decouple each supply pin, VPOS and VNEG, to ground with at least one low inductance, surface-mount ceramic capacitor of 0.1 µF placed as close as possible to the ADRF6521 device.

INPUT SIGNAL PATH

Each signal path has an input VGA, accessed through the INP1, INM1, INP2, and INM2 pins, which sets a differential input impedance of 100 Ω.

The inputs can be dc-coupled or ac-coupled, but ac coupling is strongly recommended. There is no mechanism to change the common-mode voltage. Therefore, if the user wants to use dc coupling, the common-mode voltage of the previous stage must match the ADRF6521 input common-mode voltage of (VPOS + VNEG)/2 V.

OUTPUT SIGNAL PATH

The low impedance (20 Ω) output buffers are designed to drive a 100 Ω impedance load. However, the buffers can drive larger resistive loads. The output pins (OPP1, OPM1, OPP2, and OPM2) sit at a nominal output common-mode voltage of (VPOS + VNEG)/2 V. The outputs can be dc-coupled or ac-coupled. However, dc coupling is required to take advantage of the output dc offset voltage functionality. To change the output common-mode voltage, the user must apply a dc voltage to the VOCM pin different than (VPOS + VNEG)/2 V. Left open, VOCM defaults to (VPOS + VNEG)/2 V. To change the output dc offset voltage, the user must apply a voltage to the OFS1 and OFS2 pins different than 0.75 V. Left open, these pins are pulled to ground via an on-chip 5 kΩ resistor, which creates an approximately −670 mV dc output offset.

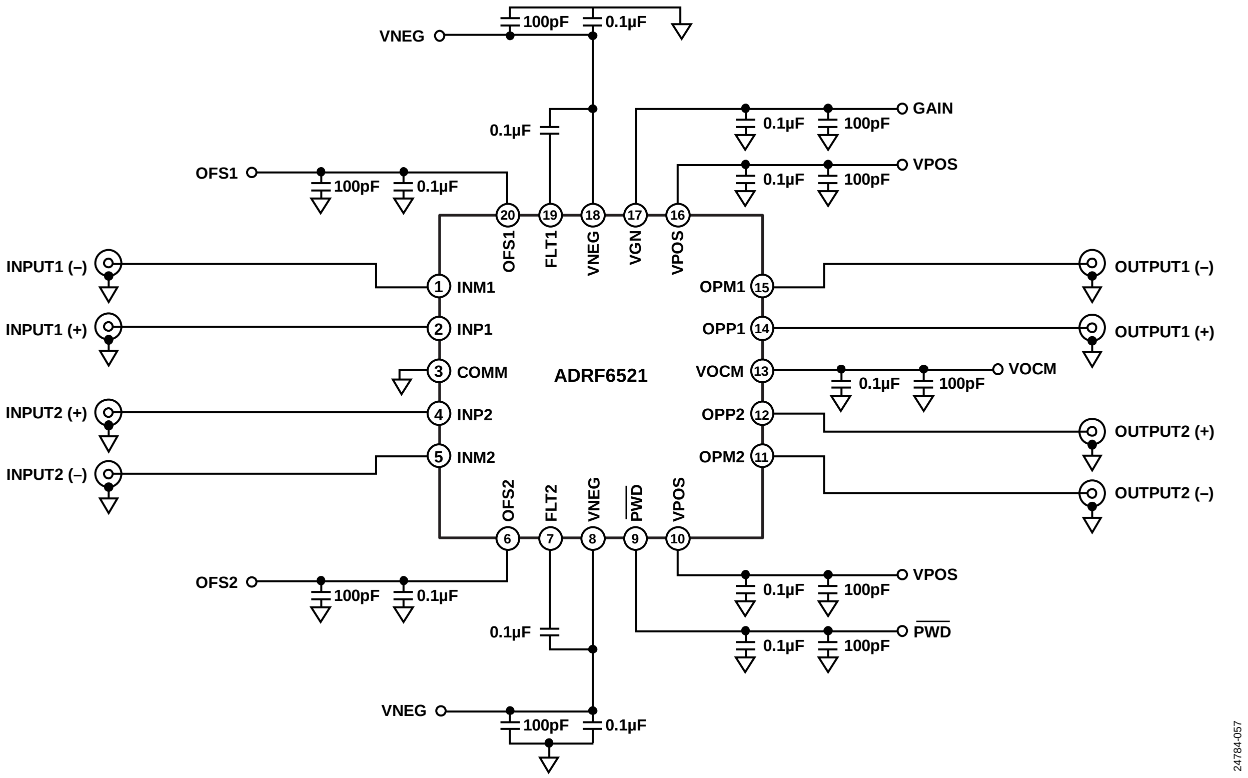


Figure 125. Basic Connections

ENABLE AND DISABLE FUNCTION

To enable the ADRF6521, leave the $\overline{\text{PWD}}$ pin open or pull this pin to VNEG + 3.0 V. Driving the $\overline{\text{PWD}}$ pin to VNEG disables the device, reducing the current consumption to approximately 25 mA at room temperature.

GAIN PIN (VGN) DECOUPLING

The ADRF6521 has one analog gain control pin, VGN. The gain changes when an applied VGN voltage is between 0 V and 1.5 V. Maximum voltage on the VGN pin is equal to the voltage applied to VPOS. Use at least one low inductance, surface-mount ceramic capacitor with a value of 0.1 μF and one 1000 pF in parallel to ground on the gain pin (VGN) to decouple to ground.

OUTPUT IMPEDANCE MATCHING

The ADRF6521 natively has a low differential output impedance of ≤16 Ω. Depending on the PCB design of the user and the S22 requirements, matching the output impedance to 100 Ω differential may be desirable. To achieve a match looking towards the output pins, place a pair of 43 Ω series resistors as close as possible to the output pins (OPP1, OPM1, OPP2, and OPM2).

The installation of these 43 Ω resistors decreases the voltage level of the signal by roughly 6 dB, and thus decreases the maximum gain of the VGA to 12 dB. This loss of signal level is usually acceptable because of the high linearity of the ADRF6521. That is, the ADRF6521 can operate at twice the output signal level (with respect to no matching resistors), and still maintain −55 dBc IMD2 and IMD3 and HD2 and HD3 levels or better.

Note that when using series matching resistors, the output dc offset voltage is also reduced by the same amount as the RF signal level.

If a full 100 Ω match is not required and a greater than 12 dB gain value is more important, the user can decrease the series resistor value until an optimum trade-off between the gain and the output match is found.

SINGLE-SUPPLY OPERATION

The ADRF6521 can operate on a 5 V single supply. Connect VNEG to analog ground. The output common-mode voltage defaults to 2.5 V in this configuration. The nominal range of ±200 mV still applies. A larger range is possible, however, linearity performance degrades.

DUAL-SUPPLY OPERATION

Apply a nominal supply voltage of +2.5 V to the VPOS supply pin, and −2.5 V to the VNEG supply pin. This setup yields a nominal output common-mode voltage of 0 V, and the output dc offset voltage moves above and below ground according to what voltage is applied to the OFSx pins.

When using a dual supply, ensure the following supply constraints:

- 4 V ≤ (VPOS − VNEG) ≤ 5 V.
- VNEG ≤ COMM ≤ VPOS
- VPOS ≥ 2.5 V

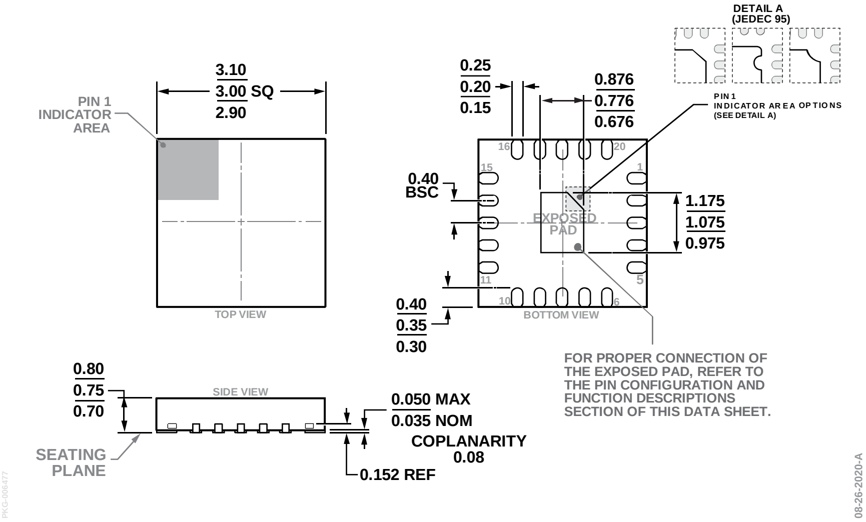
AVOIDING LATCH-UP

To avoid latch-up when the device is operational or when the device is powering up, do not apply a voltage greater than the following:

- 1.5 V (relative to ground) to the control pins (VGN, OFS1, and OFS2).
- $(V_{VPOS} + V_{VNEG})/2 \pm 1$ V to the control pin VOCM

If the RF input must be dc coupled, the common-mode voltage must be the same as the VOCM pin voltage, which must be limited to (VPOS + VNEG)/2 ± 0.2 V. If while powered down and dc coupled a dc voltage with a magnitude greater than (VPOS + VNEG)/2 ± 0.2 V is applied, this dc voltage must return within the common-mode limit before powering up the ADRF6521.

OUTLINE DIMENSIONS



FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

Figure 126. 20-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 Package Height
(CP-20-19)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF6521ACPZ	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-19
ADRF6521ACPZ-R7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP], 7" Tape and Reel	CP-20-19
ADRF6521-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Parts.

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