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Evaluating the ADRF6521 Low Frequency to 3 GHz Dual VGA with Output Common-Mode and DC Offset Control

FEATURES

Standard single-ended interfacing
Differential interfacing available
Supply voltage(s) easily applied to test loop(s)
Dual-supply capable
Analog gain control applied to test loop

EVALUATION KIT CONTENTS

ADRF6521-EVALZ evaluation board

EQUIPMENT NEEDED

6 GHz signal generator
6 GHz spectrum analyzer
3-channel power supply
Single-supply setup requires 250 mA on 1 channel
Dual-supply setup requires 250 mA on 2 channels and capable of sinking current for the negative supply voltage
Digital multimeter/voltmeter
VNA

DOCUMENTS NEEDED

ADRF6521 data sheet

GENERAL DESCRIPTION

This user guide describes the ADRF6521-EVALZ kit for the ADRF6521 dual-channel variable gain amplifier (VGA) and how to configure the evaluation board to evaluate the ADRF6521 in a single-ended and differential configuration.

The ADRF6521-EVALZ allows the user to test all the functions and features offered by the ADRF6521 including analog gain control, output common-mode control, and output dc offset control. Signal path traces are matched and are intuitively laid out on the four corners of the evaluation board, providing easy interfacing with other evaluation boards.

A full description and complete specifications for the ADRF6521 are provided in the ADRF6521 data sheet and must be consulted in conjunction with this user guide when using the evaluation board.

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REVISION HISTORY

11/2020—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPHS

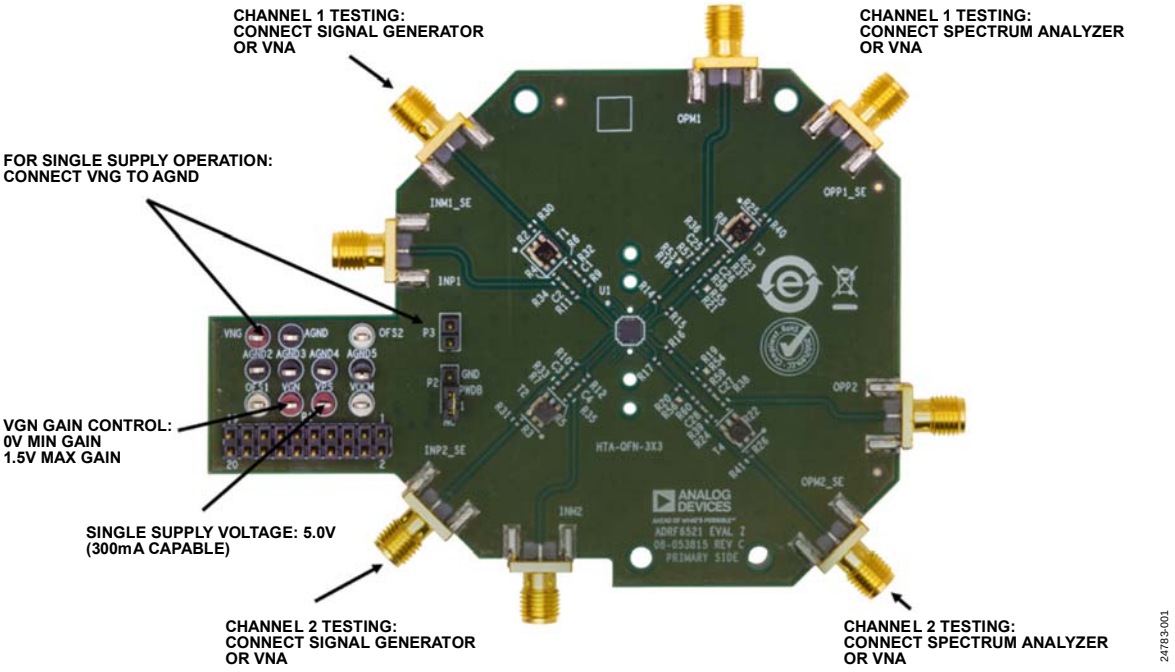

Figure 1. Layout of the ADRF6521-EVALZ

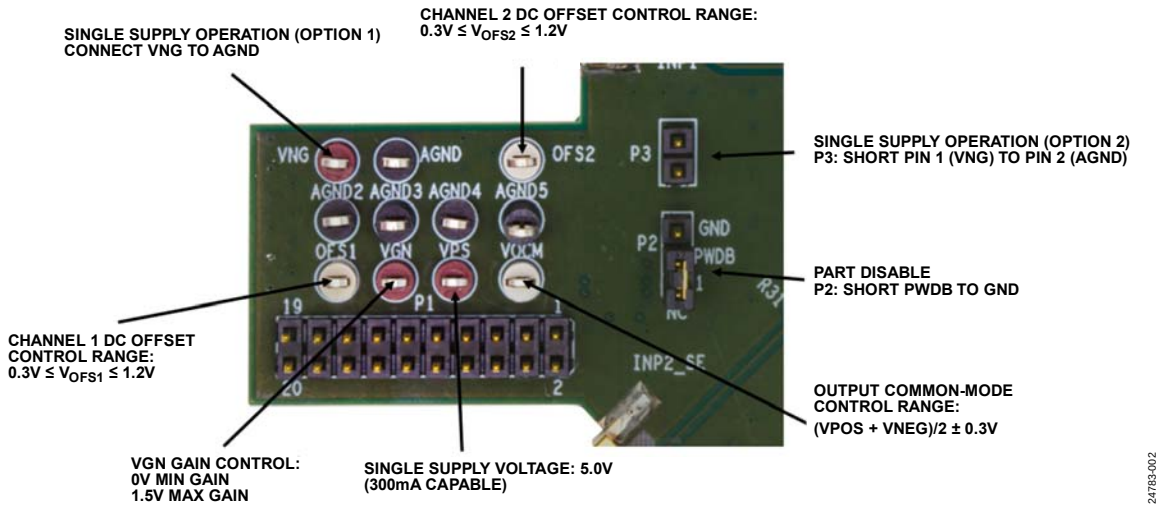

Figure 2. Layout of the ADRF6521-EVALZ (Zoomed)

EVALUATION BOARD HARDWARE

SETTING UP THE EVALUATION BOARD

Setting up the ADRF6521-EVALZ for single-supply operation includes the following steps:

1. Connect a signal generator or vector network analyzer (VNA) to the Subminiature Version A (SMA) INM1_SE connector (for the Channel 1 input) or to the SMA INP2_SE connector (for the Channel 2 input).
2. Connect a spectrum analyzer or VNA to the SMA OPP1_SE connector (for the Channel 1 output) or OPM2_SE (for the Channel 2 output).
3. Connect a 5.0 V power supply capable of 250 mA to the red VPS test point.
4. Connect the red VNG test point to AGND.
5. Apply 0 V (minimum gain) to the VGN test point.
6. Check that all SMA connectors and test points are securely connected before using the ADRF6521-EVALZ.

Power Up and Enable

Apply 5 V between the red VPS test point and one of the analog grounds to power up the ADRF6521. The AGND, AGND2, AGND3, AGND4, and AGND5 analog ground test points are shorted together.

The P2 header disables the ADRF6521. Pin 1 of the P2 header is a no connect, Pin 2 is connected to the $\overline{\text{PWD}}$ pin on the ADRF6521, and Pin 3 is connected to the negative supply pin, VNEG. Short Pin 2 and Pin 3 to disable the ADRF6521. Leave $\overline{\text{PWD}}$ floating to enable the ADRF6521. There is a 20 kΩ on-chip resistor to the VPOS pin, and a 30 kΩ on-chip resistor to the VNEG pin that creates a voltage divider that enables the device. Do not apply a higher voltage than VNEG + 3.3 V to $\overline{\text{PWD}}$, or else damage may occur.

If the ADRF6521-EVALZ is connected and working properly, upon power-up, the evaluation board draws approximately 200 mA of bias current from the supply voltage at the VPS test point.

More information on power up and enable can be found in the ADRF6521 data sheet.

Inputs and Outputs

The ADRF6521-EVALZ is set up in a single-ended configuration for easy evaluation and testing with 50 Ω test equipment. For use of Channel 1 on the ADRF6521, use the INM1_SE SMA connector for the input and the OPP1_SE SMA connector for the output. On Channel 2 on the ADRF6521, use INP2_SE and OPM2_SE.

The evaluation board can convert to a differential configuration for convenient interfacing to differential I/Q demodulators and analog-to-digital converters (ADCs) on the ADRF6521 inputs and outputs, respectively. See the Evaluation Board Setup Options section for more information.

Gain Control

The ADRF6521 has only analog gain control, achieved by applying a voltage between 0 V (minimum gain) and 1.5 V (maximum gain) to the red VGN test point. VGN controls the variable gain amplifiers for both Channel 1 and Channel 2.

Output DC Offset Control

The ADRF6521 has two output dc offset control pins, one for each channel. Apply a 750 mV ± 450 mV voltage to the OFS1 and/or OFS2 white test points to control the output dc offsets for Channel 1 and Channel 2, respectively. Left open, OFS1 and OFS2 are pulled to ground with an on-chip 5 kΩ resistor. When the OFS1 and OFS2 points are pulled to ground, the output dc offset voltage rails to its negative maximum value, which is the OPP1 and OPP2 pins set to approximately 350 mV below the common-mode, while the OPM1 and OPM2 pins are set approximately 350 mV above the common mode. OFS1 and OFS2 must be driven externally for the ADRF6521 output dc offset circuit to operate properly.

The nominal output dc offset control range is shown in Table 1 and is calculated as follows:

$$Output\ DC\ Offset = V_{DC\_OPPx} - V_{DC\_OPMx}$$

where:
V_{DC_OPPx} is the dc voltage on the OPP1 pin or the OPP2 pin.
V_{DC_OPMx} is the dc voltage on the OPM1 pin or the OPM2 pin.

Table 1. Applied V_{OFSx} Voltage to Output DC Offset

V_{OFSx} (V)	Output DC Offset (mV)
1.2	+400
0.3	−400

The x = 1 or 2 in Table 1. Greater output dc offsets are possible, but linearity may suffer depending on the magnitude of the signal.

Output Common-Mode Control

The ADRF6521 output common-mode voltage defaults to (VPOS + VNEG)/2 when VOCM is not loaded or driven. Apply a ±200 mV (nominal) voltage around (VPOS + VNEG)/2 to the white VOCM test point to change the voltage. With a single-supply of 5 V, the nominal output common-mode voltage is 2.5 V, with a range of 2.3 V to 2.7 V.

Table 2. Applied VOCM Voltage to Output Common Mode

VOCM (V)	Output Common Mode (V)	Min/Max
(VPOS + VNEG)/2 – 0.3 V	(VPOS + VNEG)/2 – 0.3 V	Min
(VPOS + VNEG)/2 + 0.3 V	(VPOS + VNEG)/2 + 0.3 V	Max

P1 Header

The ADRF6521-EVALZ has a 100 mil header that is connected to the following ADRF6521 pins directly:

- VPOS
- VNEG
- COMM (analog ground)
- VGN

- VOCM
- OFS1
- OFS2

The P1 header also provides access for measuring the dc voltage on each output pin via 10 kΩ resistors. These measurement nodes are named in the following list:

- OPP1_SENSE
- OPM1_SENSE
- OPP2_SENSE
- OPM2_SENSE

To control the power-down function of the device via P1, R13 must be populated as a 0 Ω, 0402 resistor. See Figure 7 for the exact connections to the pins on P1.

EVALUATION BOARD SETUP OPTIONS

Differential Signal Path Setup

The ADRF6521-EVALZ comes configured as single-ended. The ADRF6521-EVALZ allows users to operate the ADRF6521 with differential inputs and/or outputs.

To configure the Channel 1 input for differential operation, perform the following sequence:

1. Depopulate R2, R4, and R6.
2. Populate R30, R32, and R34.

To configure the Channel 2 input for differential operation, perform the following sequence:

1. Depopulate R3, R5, and R7.
2. Populate R31, R33, and R35.

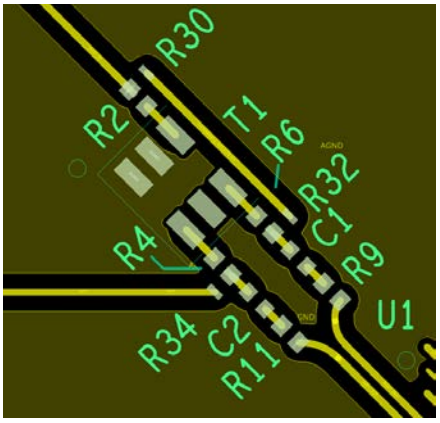

Figure 3. Layout of Channel 1 Input Showing Pad Locations

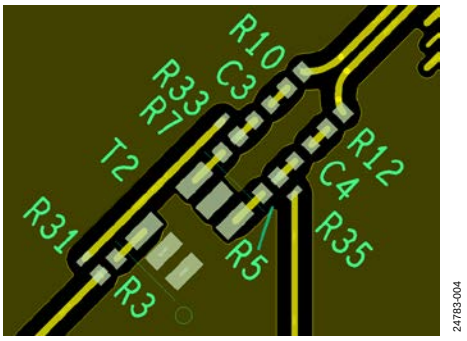

Figure 4. Layout of Channel 2 Input Showing Pad Locations

To configure the Channel 1 output for differential operation, perform the following sequence:

1. Depopulate R8, R23, and R25.
2. Populate R36, R37, and R40.

To configure the Channel 2 output for differential operation, perform the following sequence:

1. Depopulate R22, R24, and R26.
2. Populate R38, R39, and R41.

On the ADRF6521-EVALZ, choosing C11 and C12 to be equal to 1 µF sets the high pass corner to 60 Hz.

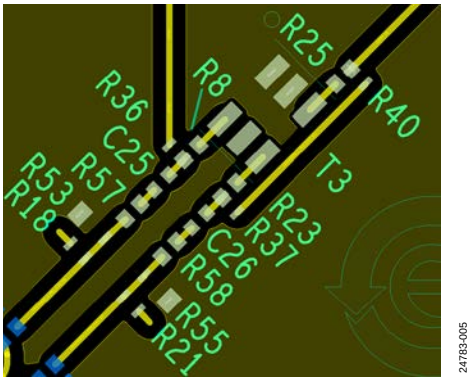

Figure 5. Layout of Channel 1 Output Showing Pad Locations

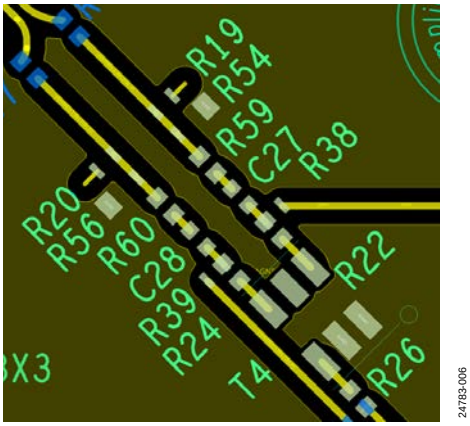

Figure 6. Layout of Channel 2 Output Showing Pad Locations

Loss and Gain of the Input and Output Networks

The ADRF6521-EVALZ has Mini-Circuits TCM2-43X+2:1 baluns (T1 and T2) on the input signal paths. Ideally, because the baluns are a 2:1 ratio, the voltage signal level must be approximately 3 dB larger on the differential side of the balun and there is no power loss. However, the baluns have approximately 1.6 dB of insertion loss at 500 MHz. Therefore, the effective voltage gain must be about 1.4 dB from the SMA connectors to the respective input pins of the ADRF6521.

The output signal paths have the same 2:1 baluns as the inputs do (T3 and T4), and have 43 Ω series resistors: R14, R15, R16, and R17. The series resistors are lossy. From the output pins of the ADRF6521 to the OPP1_SE or OPM2_SE SMA connectors, the voltage and power of the signal attenuates by approximately 9.8 dB and 4.3 dB, respectively.

Users must account for the losses of the input and output networks when applying signals on the input SMA connectors (INM1_SE and INP2_SE) and measuring signals on the output SMA connectors (OPP1_SE and OPM2_SE).

DC Coupling

The input of the ADRF6521 is self biased at (VPOS + VNEG)/2. If dc coupling on the input is required using the evaluation board, ensure that the common mode of the previous stage matches the input common mode of (VPOS + VNEG)/2 of the ADRF6521. On a single-supply setup of 5 V, the common-mode voltage is 2.5 V. To dc couple the input of the ADRF6521-EVALZ, configure the input path for differential operation (see the Differential Signal Path Setup section), and do the following:

- For Channel 1, replace C1 and C2 with 0 Ω, 0402 resistors.
- For Channel 2, replace C3 and C4 with 0 Ω, 0402 resistors.

The output of the ADRF6521 is nominally self biased to (VPOS + VNEG)/2 when VOCM is floating and OFSx is driven to 0.75 V (the OFSx pins must be driven for the ADRF6521 to operate properly). To dc couple the output of the ADRF6521-EVALZ, configure the output path for differential operation (see the Differential Signal Path Setup section), and do the following:

- For Channel 1, replace C25 and C26 with 0 Ω, 0402 resistors.
- For Channel 2, replace C27 and C28 with 0 Ω, 0402 resistors.

Input Networks

The ADRF6521-EVALZ comes from the factory with the ADRF6521 impedance matched to a 50 Ω source impedance presented by the signal generator or VNA via the T1 and T2 baluns. The 50 Ω source impedance is transformed to 100 Ω via the 2:1 baluns and presented to the 100 Ω input impedance of the ADRF6521.

Output Networks

The ADRF6521-EVALZ comes from the factory with the output loaded with 186 Ω differential, which is technically mismatched from the low 14 Ω output impedance of the ADRF6521 output buffers. This loading is achieved with the T3 and T4 baluns as well as the 43 Ω series resistors, R14, R15, R16, and R17. These resistors serve as back termination resistors that sit as close to the ADRF6521 output pins as possible to minimize peaking, and are intended to match the ADRF6521 to a pair of 50 Ω transmission lines.

Single Supply vs. Dual Supply

The ADRF6521 has two supply pins: a positive supply pin, VPOS, and a negative supply pin, VNEG (these are connected to the VPS and VNG test points, respectively). The voltage applied to these pins must always satisfy the following conditions:

- VPOS − VNEG ≤ 5 V
- VNEG ≤ COMM (ground) ≤ VPOS
- 2.5 V ≤ VPOS ≤ 5 V
- −2.5 V ≤ VNEG ≤ 0 V

For single-supply operation, connect the VPS red test point to an allowable voltage (nominally 5 V), and connect the VNG red test point to AGND.

For dual-supply operation, connect the VPS test point to the desired positive voltage, and connect the VNG test point to the desired negative voltage, ensuring that all aforementioned voltage supply conditions are followed. A common supply configuration is VPS = +2.5 V and VNG = −2.5 V. Note that this setup sets the nominal output common-mode voltage to 0 V if VOCM is undriven.

EVALUATION BOARD SCHEMATIC AND ARTWORK

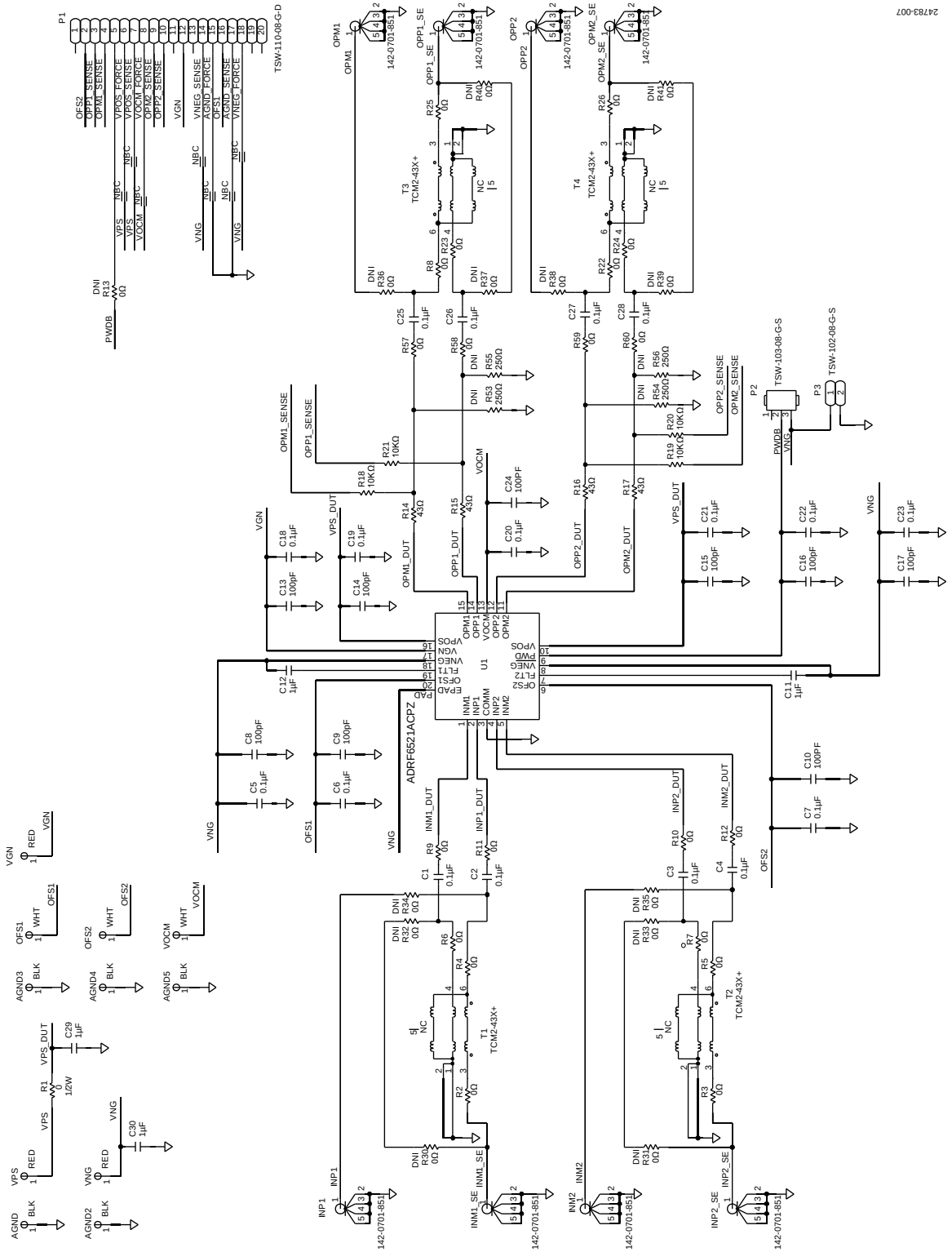

Figure 7. ADRF6521-EVALZ Main Schematic

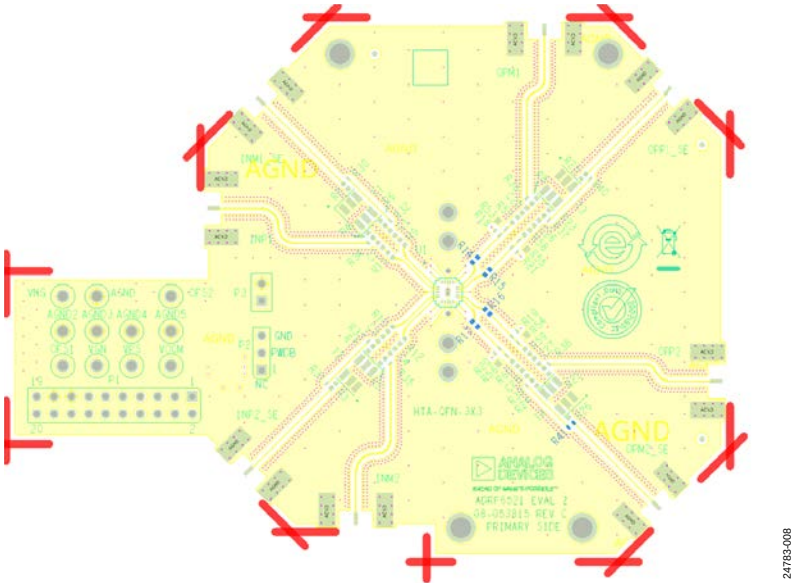

Figure 8. ADRF6521-EVALZ Silkscreen, Top View

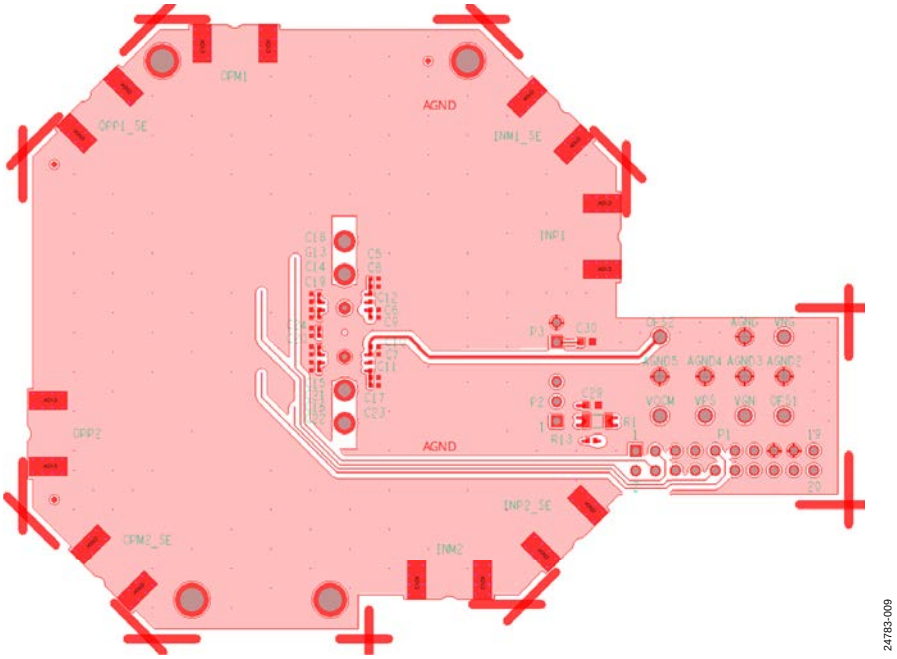

Figure 9. ADRF6521-EVALZ Silkscreen, Bottom View

ORDERING INFORMATION

BILL OF MATERIALS

Table 3. ADRF6521-EVALZ Bill of Materials (Installed)

Reference Designator	Description	Part Number	Manufacturer
U1	IC, dual VGAs with output common mode and dc offset control	ADRF6521-ACPZ	Analog Devices, Inc.
C1, C2, C3, C4, C5, C6, C7, C18, C19, C20, C21, C22, C23, C25, C26, C27, C28	Ceramic capacitors X7R 0402, general-purpose, 0.1 µF	C0402C104J4RACTU	KEMET
C8, C9, C10, C13, C14, C15, C16, C17, C24	Ceramic capacitors C0G, 0402, 100 pF	500R07N101JV4T	Johanson Dielectrics
C11, C12	Ceramic capacitors, X5R	CL05A105MO5NNNC	Samsung
C29, C30	Ceramic capacitors, high multilayer, X7R	UMK107AB7105KA-T	Taiyo Yuden
R1	Resistor, high power thick film chip, 1206, 0 Ω	CRCW12060000Z0EAHP	Vishay
R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R22, R23, R24, R25, R26, R57, R58, R59, R60	Resistor chips, thick films, SMD jumper, R0402, 0 Ω	RMCF0402ZT0R00	Stackpole Electronics, Inc.
R14, R15, R16, R17	Resistors, film chip, R0402, 43 Ω	CR10B430JT	MULTICOMP (SPC)
R18, R19, R20, R21	Resistors, thick film chip, R0402,10 kΩ	CRCW040210K0FKED	VISHAY
P1	20-position header connector, male, 0.100"	TSW-110-08-G-D	Samtec
P2	3-position header connector, male, 0.100"	TSW-103-08-G-S	Samtec
P3	2-position header connector, 0.100"	TSW-102-08-G-S	Samtec
T1 to T4	RF balun, 10 MHz to 4 GHz, 1:2	TCM2-43X+	Mini Circuits
INM1_SE, INM2, INP1, INP2_SE, OPM1, OPM2_SE, OPP1_SE, OPP2	SMA connector jacks, 50 Ω, end launch, female receptacle	142-0701-851	Cinch
VGN, VNG, VPS	Connector PCB test point, red	TP-104-01-02	Components Corporation
OFS1, OFS2, VOCM	Connector PCB test point, white	TP-104-01-09	Components Corporation
AGND, AGND2, AGND3, AGND4, AGND5	Connector PCB test point, black	TP-104-01-00	Components Corporation

Table 4. ADRF6521-EVALZ Bill of Materials (Not Installed)

Reference Designator	Description	Part Number	Manufacturer
R13, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41	Resistor chips, SMD jumper, 0 Ω	RMCF0402ZT0R00	Stackpole Electronics, Inc.
R53, R54, R55, R56	Resistor thin film chip, 0603, 250 Ω	PLT0603Z2500AST5	VISHAY

Table 5. ADRF6521-EVALZ Bill of Materials (Mechanical Parts)

Reference Designator	Description	Part Number	Manufacturer
Not Applicable (Installed on P2)	Socket, two-position, 0.100" pitch, connector shunt (see the Power Up and Enable section for instructions)	SNT-100-BK-G	Samtec

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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