2050 MHz to 3000 MHz Quadrature Modulator with 2500 MHz to 2900 MHz Frac-N PLL and Integrated VCO

Data Sheet **ADRF6704**

FEATURES

IQ modulator with integrated fractional-N PLL
Output frequency range: 2050 MHz to 3000 MHz
Internal LO frequency range: 2500 MHz to 2900 MHz
Output P1dB: 12.1 dBm @ 2700 MHz
Output IP3: 27.2 dBm @ 2700 MHz
Noise floor: −158.3 dBm/Hz @ 2700 MHz
Baseband bandwidth: 750 MHz (3 dB)
SPI serial interface for PLL programming
Integrated LDOs and LO buffer
Power supply: 5 V/226 mA
40-lead 6 mm × 6 mm LFCSP

APPLICATIONS

Cellular communications systems
- **GSM/EDGE, CDMA2000, W-CDMA, TD-SCDMA, LTE**

Broadband wireless access systems
Satellite modems

GENERAL DESCRIPTION

The ADRF6704 provides a quadrature modulator and synthesizer solution within a small 6 mm × 6 mm footprint while requiring minimal external components.

The ADRF6704 is designed for RF outputs from 2050 MHz to 3000 MHz. The low phase noise VCO and high performance quadrature modulator make the ADRF6704 suitable for next generation communication systems requiring high signal dynamic range and linearity. The integration of the IQ modulator, PLL, and VCO provides for significant board savings and reduces the BOM and design complexity.

The integrated fractional-N PLL/synthesizer generates a 2× f_{LO} input to the IQ modulator. The phase detector together with an external loop filter is used to control the VCO output. The VCO output is applied to a quadrature divider. To reduce spurious components, a sigma-delta (Σ-Δ) modulator controls the programmable PLL divider.

The IQ modulator has wideband differential I and Q inputs, which support baseband as well as complex IF architectures. The single-ended modulator output is designed to drive a 50 Ω load impedance and can be disabled.

The ADRF6704 is fabricated using an advanced silicon-germanium BiCMOS process. It is available in a 40-lead, exposed-paddle, Pb-free, 6 mm × 6 mm LFCSP package. Performance is specified from −40°C to +85°C. A lead-free evaluation board is available.

Table 1.

Part No.	Internal LO Range	IQ Modulator ±3 dB RF Output Range
ADRF6701	750 MHz	400 MHz
	1150 MHz	1250 MHz
ADRF6702	1550 MHz	1200 MHz
	2150 MHz	2400 MHz
ADRF6703	2100 MHz	1550 MHz
	2600 MHz	2650 MHz
ADRF6704	2500 MHz	2050 MHz
	2900 MHz	3000 MHz

FUNCTIONAL BLOCK DIAGRAM

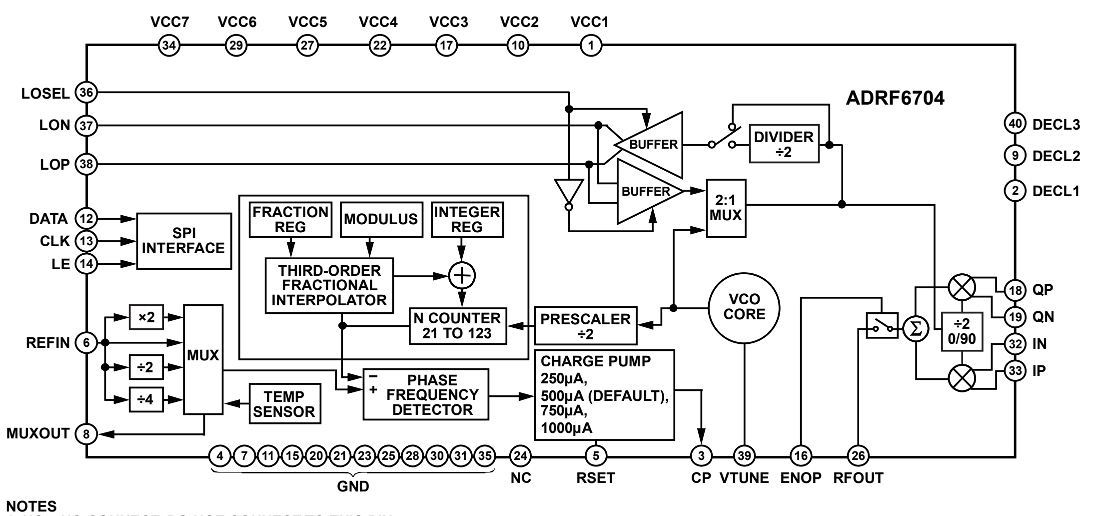

Figure 1.

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REVISION HISTORY

10/11—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V; T_A = 25°C; baseband I/Q amplitude = 1 V p-p differential sine waves in quadrature with a 500 mV dc bias; baseband I/Q frequency (f_{BB}) = 1 MHz; f_{PFD} = 38.4 MHz; f_{REF} = 153.6 MHz at +4 dBm Re:50 Ω (1 V p-p); 130 kHz loop filter, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPERATING FREQUENCY RANGE	IQ modulator (±3 dB RF output range)	2050		3000	MHz
	PLL LO range	2500		2900	MHz
RF OUTPUT = 2500 MHz	RFOUT pin				
Nominal Output Power	Baseband VIQ = 1 V p-p differential		6.2		dBm
IQ Modulator Voltage Gain	RF output divided by baseband input voltage		2.2		dB
OP1dB			12.9		dBm
Carrier Feedthrough			−41.2		dBm
Sideband Suppression			−42.4		dBc
Quadrature Error			±1		Degrees
I/Q Amplitude Balance			0.06		dB
Second Harmonic	$P_{OUT} − P (f_{LO} ± (2 × f_{BB}))$		−67		dBc
Third Harmonic	$P_{OUT} − P (f_{LO} ± (3 × f_{BB}))$		−45.6		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} ≈ −2 dBm per tone		65.4		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} ≈ −2 dBm per tone		25.4		dBm
Noise Floor	I/Q inputs = 0 V differential with 500 mV dc bias, 20 MHz carrier offset		−157.8		dBm/Hz
RF OUTPUT = 2700 MHz	RFOUT pin				
Nominal Output Power	Baseband VIQ = 1 V p-p differential		5.5		dBm
IQ Modulator Voltage Gain	RF output divided by baseband input voltage		1.5		dB
OP1dB			12.1		dBm
Carrier Feedthrough			−40.6		dBm
Sideband Suppression			−37.7		dBc
Quadrature Error			0 to 2		Degrees
I/Q Amplitude Balance			0.06		dB
Second Harmonic	$P_{OUT} − P (f_{LO} ± (2 × f_{BB}))$		−66		dBc
Third Harmonic	$P_{OUT} − P (f_{LO} ± (3 × f_{BB}))$		−47.1		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} ≈ −2 dBm per tone		63.8		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} ≈ −2 dBm per tone		27.2		dBm
Noise Floor	I/Q inputs = 0 V differential with 500 mV dc bias, 20 MHz carrier offset		−158.3		dBm/Hz
RF OUTPUT = 2900 MHz	RFOUT pin				
Nominal Output Power	Baseband VIQ = 1 V p-p differential		4.1		dBm
IQ Modulator Voltage Gain	RF output divided by baseband input voltage		0.1		dB
OP1dB			11.8		dBm
Carrier Feedthrough			−41.5		dBm
Sideband Suppression			−32.7		dBc
Quadrature Error			1 to 2.8		Degrees
I/Q Amplitude Balance			0.1		dB
Second Harmonic	$P_{OUT} − P (f_{LO} ± (2 × f_{BB}))$		−67		dBc
Third Harmonic	$P_{OUT} − P (f_{LO} ± (3 × f_{BB}))$		−51.4		dBc
Output IP2	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} ≈ −2 dBm per tone		62.7		dBm
Output IP3	$f1_{BB}$ = 3.5 MHz, $f2_{BB}$ = 4.5 MHz, P_{OUT} ≈ −2 dBm per tone)		29.6		dBm
Noise Floor	I/Q inputs = 0 V differential with 500 mV dc bias, 20 MHz carrier offset		−157.5		dBm/Hz
SYNTHESIZER SPECIFICATIONS	Synthesizer specifications referenced to the modulator output				
Internal LO Range		2500		2900	MHz
Figure of Merit (FOM)[1]			−221.4		dBc/Hz/Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REFERENCE CHARACTERISTICS	REFIN, MUXOUT pins				
REFIN Input Frequency		11		160	MHz
REFIN Input Capacitance			4		pF
Phase Detector Frequency		22		40	MHz
MUXOUT Output Level	Low (lock detect output selected)			0.25	V
	High (lock detect output selected)	2.7			V
MUXOUT Duty Cycle			50		%
CHARGE PUMP					
Charge Pump Current	Programmable to 250 µA, 500 µA, 750 µA, 1000 µA		500		µA
Output Compliance Range		1		2.8	V
PHASE NOISE (FREQUENCY = 2500 MHz, f_{PFD} = 38.4 MHz)	Closed loop operation (see Figure 35 for loop filter design)				
	10 kHz offset		−100.9		dBc/Hz
	100 kHz offset		−100		dBc/Hz
	1 MHz offset		−126		dBc/Hz
	10 MHz offset		−148.3		dBc/Hz
Integrated Phase Noise	1 kHz to 10 MHz integration bandwidth		0.37		°rms
Reference Spurs	$f_{PFD}/2$		−111		dBc
	f_{PFD}		−87.3		dBc
	$f_{PFD} \times 2$		−93.6		dBc
	$f_{PFD} \times 3$		−92.8		dBc
	$f_{PFD} \times 4$		−98.2		dBc
PHASE NOISE (FREQUENCY = 2700 MHz, f_{PFD} = 38.4 MHz)	Closed loop operation (see Figure 35 for loop filter design)				
	10 kHz offset		−97.7		dBc/Hz
	100 kHz offset		−97.6		dBc/Hz
	1 MHz offset		−126.1		dBc/Hz
	10 MHz offset		−148.4		dBc/Hz
Integrated Phase Noise	1 kHz to 10 MHz integration bandwidth		0.46		°rms
Reference Spurs	$f_{PFD}/2$		−110.4		dBc
	f_{PFD}		−89.9		dBc
	$f_{PFD} \times 2$		−92		dBc
	$f_{PFD} \times 3$		−89.9		dBc
	$f_{PFD} \times 4$		−94.5		dBc
PHASE NOISE (FREQUENCY = 2900 MHz, f_{PFD} = 38.4 MHz)	Closed loop operation (see Figure 35 for loop filter design)				
	10 kHz offset		−92.3		dBc/Hz
	100 kHz offset		−96.4		dBc/Hz
	1 MHz offset		−125.2		dBc/Hz
	10 MHz offset		−148.5		dBc/Hz
Integrated Phase Noise	1 kHz to 10 MHz integration bandwidth		0.62		°rms
Reference Spurs	$f_{PFD}/2$		−110.7		dBc
	f_{PFD}		−90.9		dBc
	$f_{PFD} \times 2$		−89.8		dBc
	$f_{PFD} \times 3$		−92.1		dBc
	$f_{PFD} \times 4$		−93.7		dBc
RF OUTPUT HARMONICS	Measured at RFOUT, frequency = 2700 MHz				
	Second harmonic		−44.4		dBc
	Third harmonic		−76.7		dBc
LO INPUT/OUTPUT	LOP, LON				
Output Frequency Range	Divide by 2 circuit in LO path enabled	2500		2900	MHz
	Divide by 2 circuit in LO path disabled	5000		5800	MHz
LO Output Level at 2700 MHz	1× LO mode, into a 50 Ω load, LO buffer enabled		−2		dBm
LO Input Level	Externally applied 2× LO, PLL disabled		0		dBm
LO Input Impedance	Externally applied 2× LO, PLL disabled		50		Ω

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
BASEBAND INPUTS	IP, IN, QP, QN pins				
I and Q Input DC Bias Level		400	500	600	mV
Bandwidth	P_{OUT} ≈ −7 dBm, RF flatness of IQ modulator output calibrated out				
	0.5 dB		350		MHz
	3 dB		750		MHz
Differential Input Impedance			920		Ω
Differential Input Capacitance			1		pF
LOGIC INPUTS	CLK, DATA, LE, ENOP, LOSEL				
Input High Voltage, V_{INH}		1.4		3.3	V
Input Low Voltage, V_{INL}		0		0.7	V
Input Current, I_{INH}/I_{INL}			0.1		µA
Input Capacitance, C_{IN}			5		pF
TEMPERATURE SENSOR	VPTAT voltage measured at MUXOUT				
Output Voltage	T_A = 25°C, RL ≥10 kΩ (LO buffer disabled)		1.579		V
Temperature Coefficient	T_A = −40°C to +85°C, RL ≥10 kΩ		3.8		mV/°C
POWER SUPPLIES	VCC1, VCC2, VCC3, VCC4, VCC5, VCC6, VCC7				
Voltage Range		4.75	5	5.25	V
Supply Current	Normal Tx mode (PLL and IQMOD enabled, LO buffer disabled)		226		mA
	Tx mode using external LO input (internal VCO/PLL disabled)		135		mA
	Tx mode with LO buffer enabled		276		mA
	Power-down mode		22		mA

[1] The figure of merit (FOM) is computed as phase noise (dBc/Hz) – 10log10(f_{PFD}) – 20log10(f_{LO}/f_{PFD}). The FOM was measured across the full LO range, with f_{REF} = 80 MHz, f_{REF} power = 10 dBm (500 V/µs slew rate) with a 40 MHz f_{PFD}. The FOM was computed at 50 kHz offset.

TIMING CHARACTERISTICS

Table 3.

Parameter	Limit	Unit	Test Conditions/Comments
t_1	20	ns min	LE to CLK setup time
t_2	10	ns min	DATA to CLK setup time
t_3	10	ns min	DATA to CLK hold time
t_4	25	ns min	CLK high duration
t_5	25	ns min	CLK low duration
t_6	10	ns min	CLK to LE setup time
t_7	20	ns min	LE pulse width

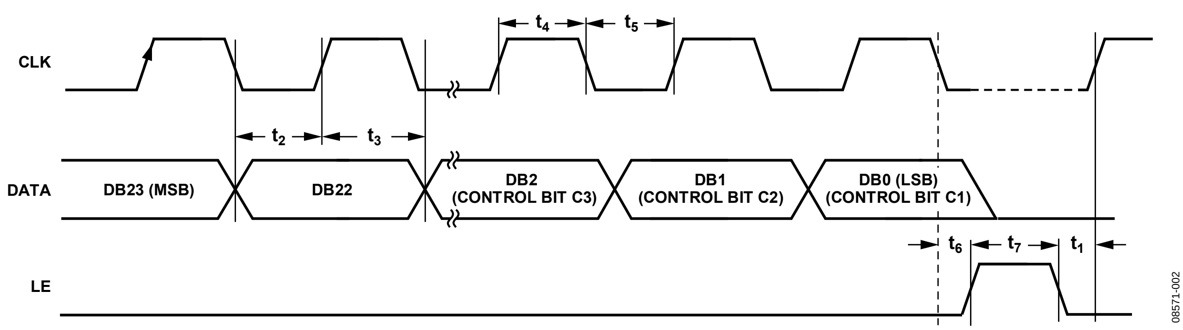

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage (VCC1 to VCC7)	5.5 V
Digital I/O, CLK, DATA, LE	−0.3 V to +3.6 V
LOP, LON	18 dBm
IP, IN, QP, QN	−0.5 V to +1.5 V
REFIN	−0.3 V to +3.6 V
θ_{JA} (Exposed Paddle Soldered Down)[1]	35°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

[1] Per JDEC standard JESD 51-2.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

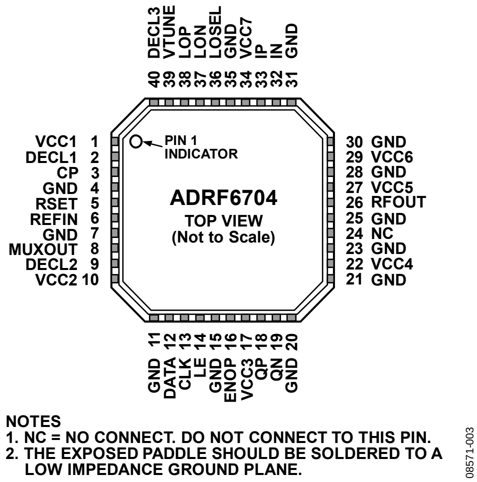

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 10, 17, 22, 27, 29, 34	VCC1, VCC2, VCC3, VCC4, VCC5, VCC6, VCC7	Power Supply Pins. The power supply voltage range is 4.75 V to 5.25 V. Drive all of these pins from the same power supply voltage. Decouple each pin with 100 pF and 0.1 µF capacitors located close to the pin.
2	DECL1	Decoupling Node for Internal 3.3 V LDO. Decouple this pin with 100 pF and 0.1 µF capacitors located close to the pin.
3	CP	Charge Pump Output Pin. Connect VTUNE to this pin through the loop filter.
4, 7, 11, 15, 20, 21, 23, 25, 28, 30, 31, 35	GND	Ground. Connect these pins to a low impedance ground plane.
24	NC	Do not connect to this pin.
5	RSET	Charge Pump Current. The nominal charge pump current can be set to 250 µA, 500 µA, 750 µA, or 1000 µA using DB10 and DB11 of Register 4 and by setting DB18 to 0 (CP reference source). In this mode, no external RSET is required. If DB18 is set to 1, the four nominal charge pump currents ($I_{NOMINAL}$) can be externally tweaked according to the following equation: $R_{SET} = \left(\frac{217.4 \times I_{CP}}{I_{NOMINAL}} \right) - 37.8\Omega$ where I_{CP} is the base charge pump current in microamps. For further details on the charge pump current, see the Register 4—PLL Charge Pump, PFD, and Reference Path Control section.
6	REFIN	Reference Input. The nominal input level is 1 V p-p. Input range is 11 MHz to 160 MHz. This pin has high input impedance and should be ac-coupled. If REFIN is being driven by laboratory test equipment, the pin should be externally terminated with a 50 Ω resistor (place the ac-coupling capacitor between the pin and the resistor). When driven from an 50 Ω RF signal generator, the recommended input level is 4 dBm.
8	MUXOUT	Multiplexer Output. This output allows a digital lock detect signal, a voltage proportional to absolute temperature (VPTAT), or a buffered, frequency-scaled reference signal to be accessed externally. The output is selected by programming DB21 to DB23 in Register 4.
9	DECL2	Decoupling Node for 2.5 V LDO. Connect 100 pF, 0.1 µF, and 10 µF capacitors between this pin and ground.
12	DATA	Serial Data Input. The serial data input is loaded MSB first with the three LSBs being the control bits.
13	CLK	Serial Clock Input. This serial clock input is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. Maximum clock frequency is 20 MHz.

Pin No.	Mnemonic	Description
14	LE	Latch Enable. When the LE input pin goes high, the data stored in the shift registers is loaded into one of the six registers, the relevant latch being selected by the first three control bits of the 24-bit word.
16	ENOP	Modulator Output Enable/Disable. See Table 6.
18, 19, 32, 33	QP, QN, IN, IP	Modulator Baseband Inputs. Differential in-phase and quadrature baseband inputs. These inputs should be dc-biased to 0.5 V.
26	RFOUT	RF Output. Single-ended, 50 Ω internally biased RF output. RFOUT must be ac-coupled to its load.
36	LOSEL	LO Select. This digital input pin determines whether the LOP and LON pins operate as inputs or outputs. This pin should not be left floating. LOP and LON become inputs if the LOSEL pin is set low and the LDRV bit of Register 5 is set low. External LO drive must be a 2× LO. In addition to setting LOSEL and LDRV low and providing an external 2× LO, the LXL bit of Register 5 (DB4) must be set to 1 to direct the external LO to the IQ modulator. LON and LOP become outputs when LOSEL is high or if the LDRV bit of Register 5 (DB3) is set to 1. A 1× LO or 2× LO output can be selected by setting the LDIV bit of Register 5 (DB5) to 1 or 0 respectively (see Table 7).
37, 38	LON, LOP	Local Oscillator Input/Output. The internally generated 1× LO or 2× LO is available on these pins. When internal LO generation is disabled, an external 1× LO or 2× LO can be applied to these pins.
39	VTUNE	VCO Control Voltage Input. This pin is driven by the output of the loop filter. Nominal input voltage range on this pin is 1.3 V to 2.5 V.
40	DECL3	Decoupling Node for VCO LDO. Connect a 100 pF capacitor and a 10 µF capacitor between this pin and ground.
	EP	Exposed Paddle. The exposed paddle should be soldered to a low impedance ground plane.

Table 6. Enabling RFOUT

ENOP	Register 5 Bit DB6	RFOUT
X[1]	0	Disabled
0	X[1]	Disabled
1	1	Enabled

[1] X = don't care.

Table 7. LO Port Configuration[1, 2]

LON/LOP Function	LOSEL	Register 5 Bit DB5(LDIV)	Register 5 Bit DB4(LXL)	Register 5 Bit DB3 (LDRV)
Input (2× LO)	0	X	1	0
Output (Disabled)	0	X	0	0
Output (1× LO)	0	0	0	1
Output (1× LO)	1	0	0	0
Output (1× LO)	1	0	0	1
Output (2× LO)	0	1	0	1
Output (2× LO)	1	1	0	0
Output (2× LO)	1	1	0	1

[1] X = don't care.
[2] LOSEL should not be left floating.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V; T_A = 25°C; baseband I/Q amplitude = 1 V p-p differential sine waves in quadrature with a 500 mV dc bias; baseband I/Q frequency (f_{BB}) = 1 MHz; f_{PFD} = 38.4 MHz; f_{REF} = 153.6 MHz at +4 dBm Re:50 Ω (1 V p-p); 130 kHz loop filter, unless otherwise noted.

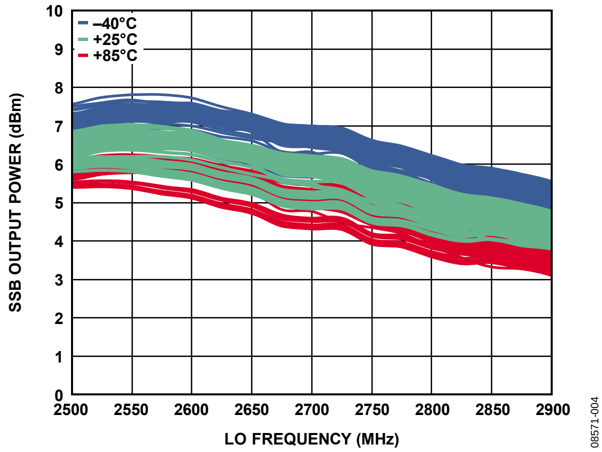

Figure 4. Single Sideband (SSB) Output Power (P_{OUT}) vs. LO Frequency (f_{LO}) and Temperature; Multiple Devices Shown

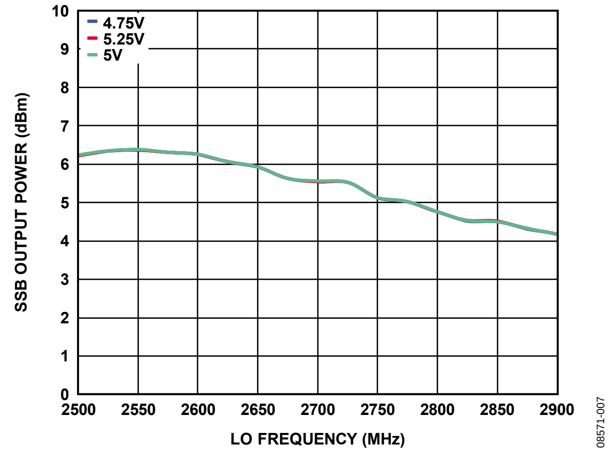

Figure 7. Single Sideband (SSB) Output Power (P_{OUT}) vs. LO Frequency (f_{LO}) and Power Supply; Multiple Devices Shown

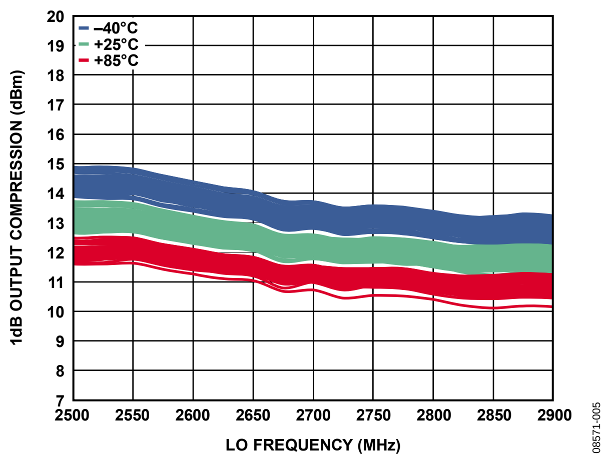

Figure 5. SSB Output 1dB Compression Point (OP1dB) vs. LO Frequency (f_{LO}) and Temperature; Multiple Devices Shown

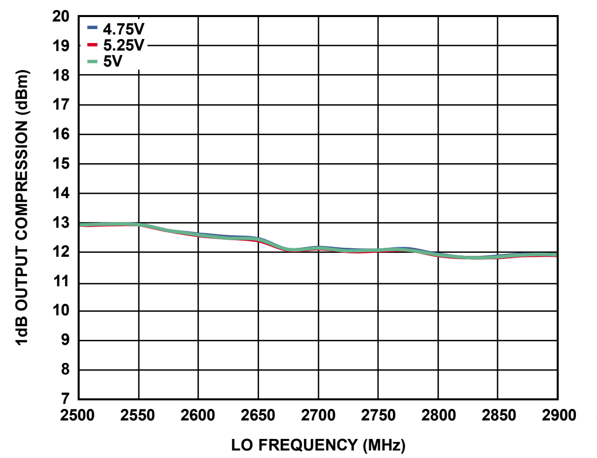

Figure 8. SSB Output 1dB Compression Point (OP1dB) vs. LO Frequency (f_{LO}) and Power Supply

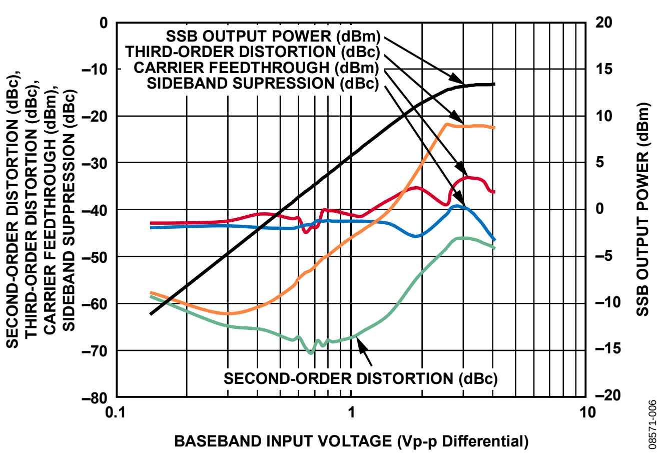

Figure 6. SSB Output Power, Second- and Third-Order Distortion, Carrier Feedthrough, and Sideband Suppression vs. Baseband Differential Input Voltage (f_{OUT} = 2500 MHz)

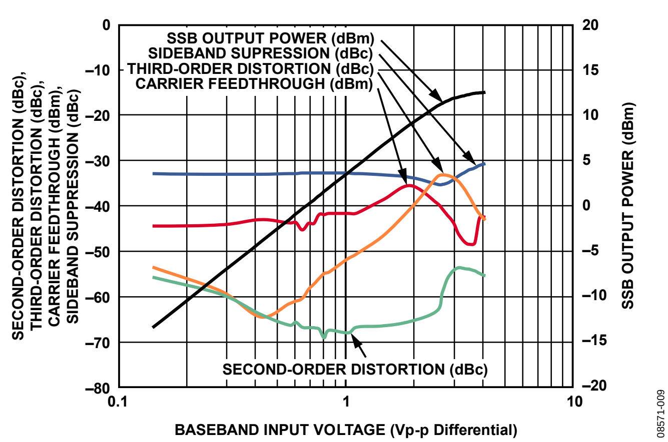

Figure 9. SSB Output Power, Second- and Third-Order Distortion, Carrier Feedthrough, and Sideband Suppression vs. Baseband Differential Input Voltage (f_{OUT} = 2900 MHz)

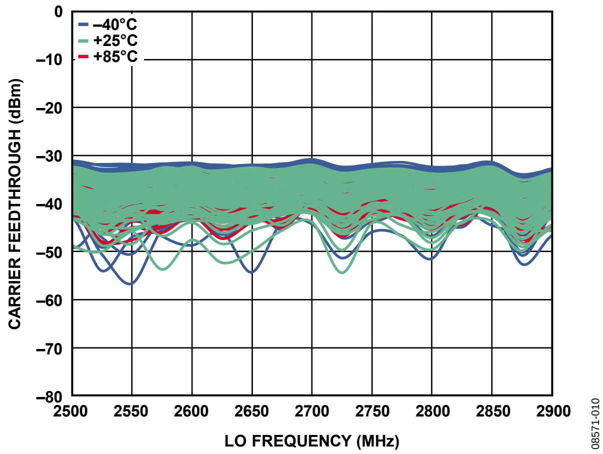

Figure 10. Carrier Feedthrough vs. LO Frequency (f_{LO}) and Temperature; Multiple Devices Shown

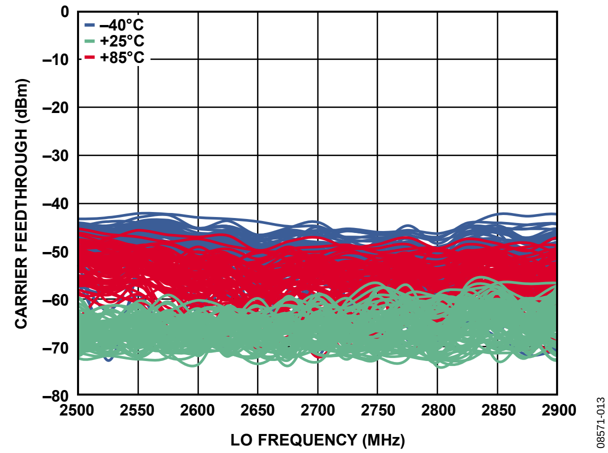

Figure 13. Carrier Feedthrough vs. LO Frequency (f_{LO}) and Temperature After Nulling at 25°C; Multiple Devices Shown

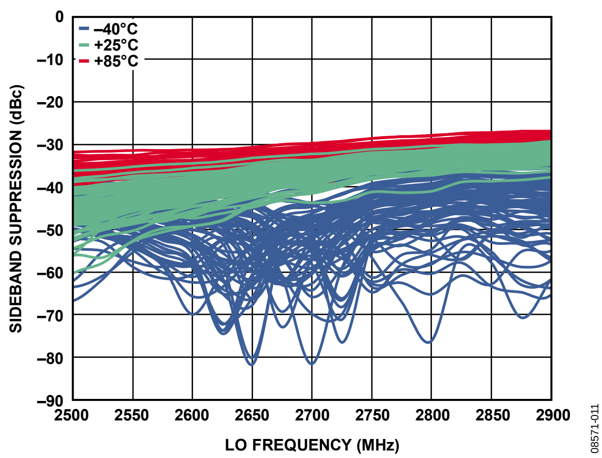

Figure 11. Sideband Suppression vs. LO Frequency (f_{LO}) and Temperature; Multiple Devices Shown

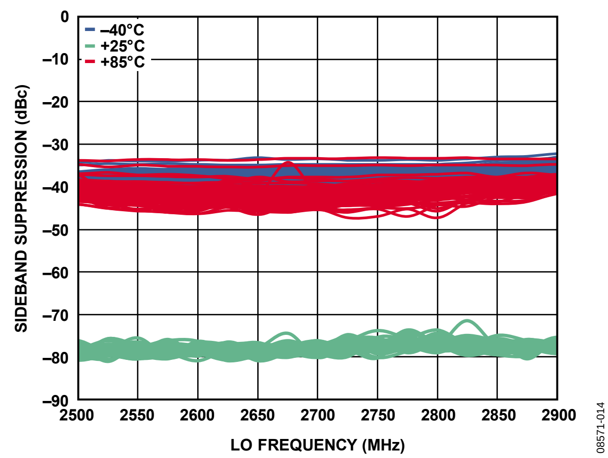

Figure 14. Sideband Suppression vs. LO Frequency (f_{LO}) and Temperature After Nulling at 25°C; Multiple Devices Shown

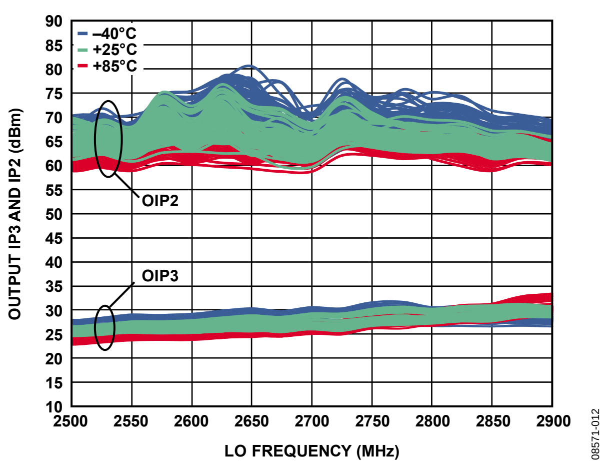

Figure 12. OIP3 and OIP2 vs. LO Frequency (f_{LO}) and Temperature ($P_{OUT} \approx -2$ dBm per Tone); Multiple Devices Shown

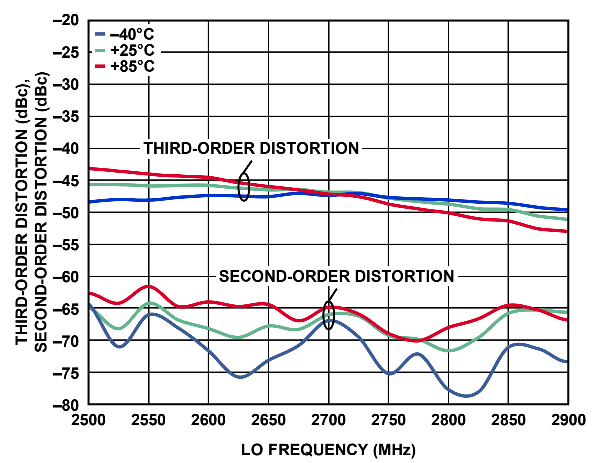

Figure 15. Second- and Third-Order Distortion vs. LO Frequency (f_{LO}) and Temperature

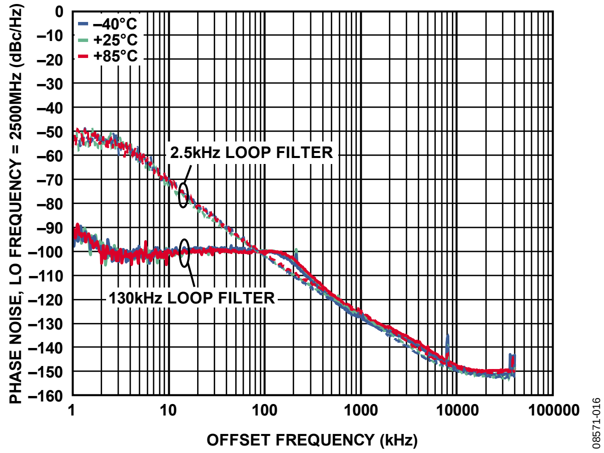

Figure 16. Phase Noise vs. Offset Frequency and Temperature, f_{LO} = 2500 MHz

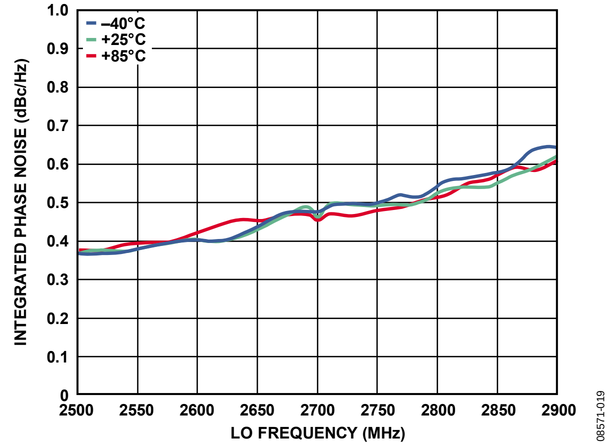

Figure 19. Integrated Phase Noise vs. LO Frequency

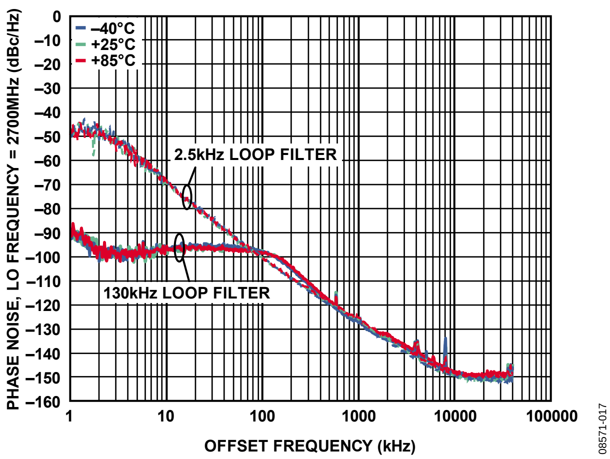

Figure 17. Phase Noise vs. Offset Frequency and Temperature, f_{LO} = 2700 MHz

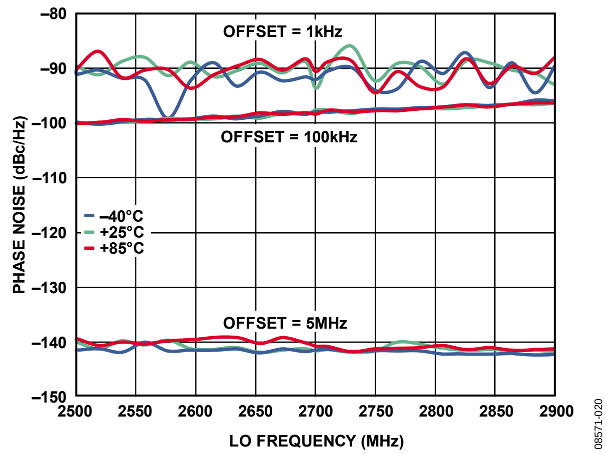

Figure 20. Phase Noise vs. LO Frequency at 1 kHz, 100 kHz, and 5 MHz Offsets

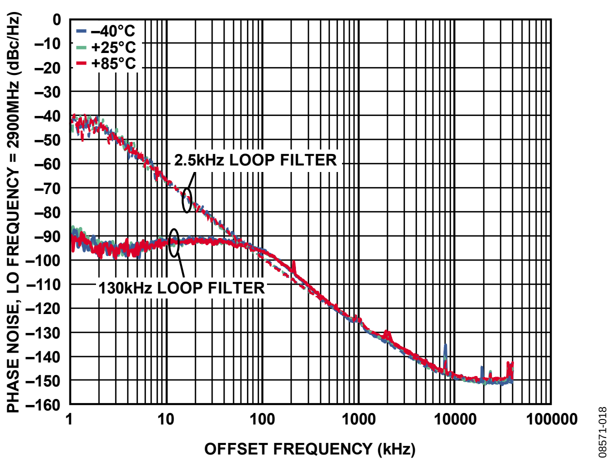

Figure 18. Phase Noise vs. Offset Frequency and Temperature, f_{LO} = 2900 MHz

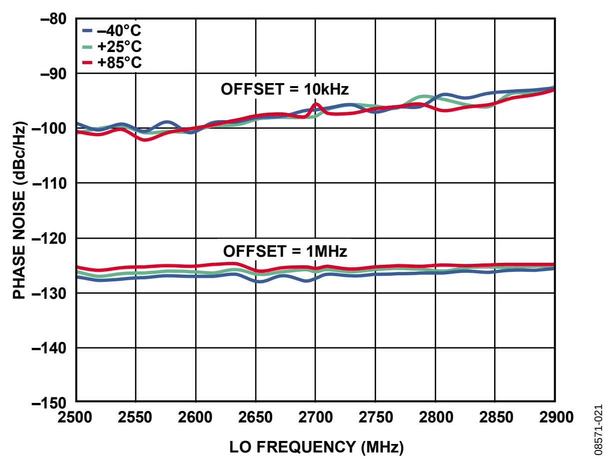

Figure 21. Phase Noise vs. LO Frequency at 10 kHz and 1 MHz Offsets

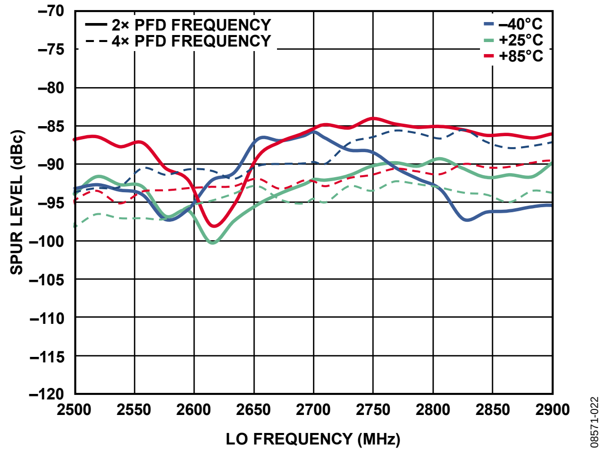

Figure 22. PLL Reference Spurs vs. LO Frequency (2× PFD and 4× PFD) at Modulator Output

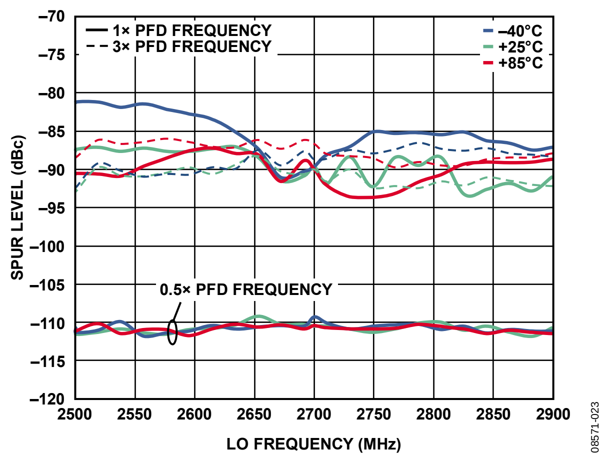

Figure 23. PLL Reference Spurs vs. LO Frequency (0.5× PFD, 1× PFD, and 3× PFD) at Modulator Output

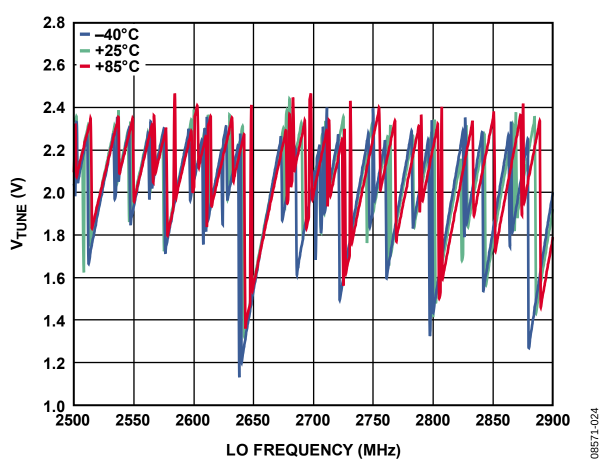

Figure 24. VTUNE vs. LO Frequency and Temperature

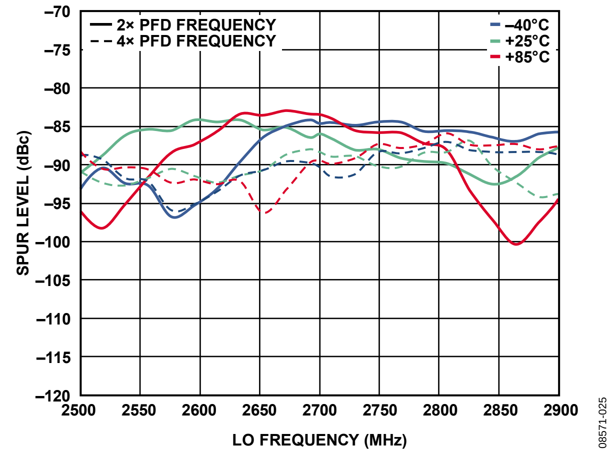

Figure 25. PLL Reference Spurs vs. LO Frequency (2× PFD and 4× PFD) at LO Output

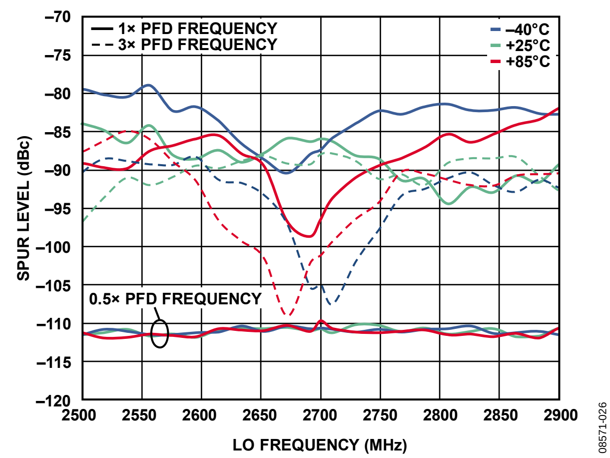

Figure 26. PLL Reference Spurs vs. LO Frequency (0.5× PFD, 1× PFD, and 3× PFD) at LO Output

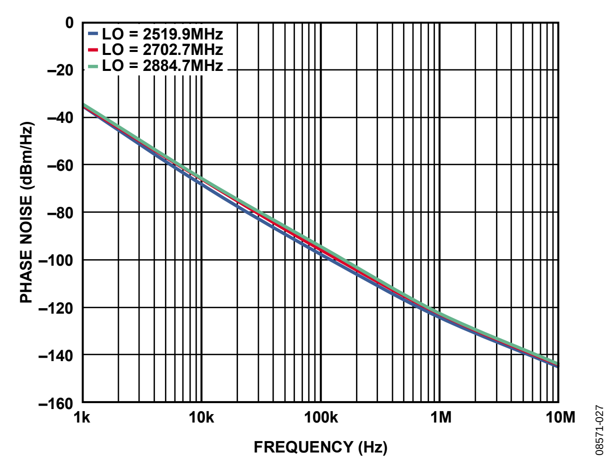

Figure 27. Open-Loop VCO Phase Noise at 2519.9 MHz, 2702.7 MHz, and 2884.7 MHz

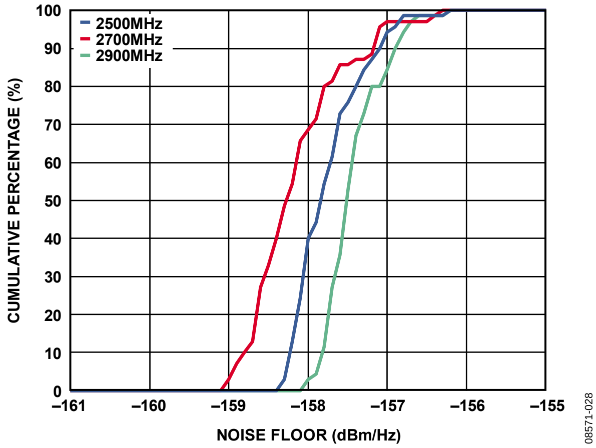

Figure 28. IQ Modulator Noise Floor Cumulative Distributions at 2500 MHz, 2700 MHz, and 2900 MHz

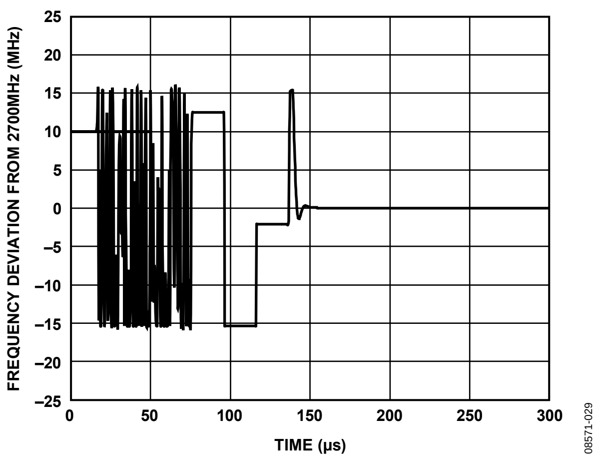

Figure 29. Frequency Deviation from LO Frequency at LO = 2.71 GHz to 2.7 GHz vs. Lock Time

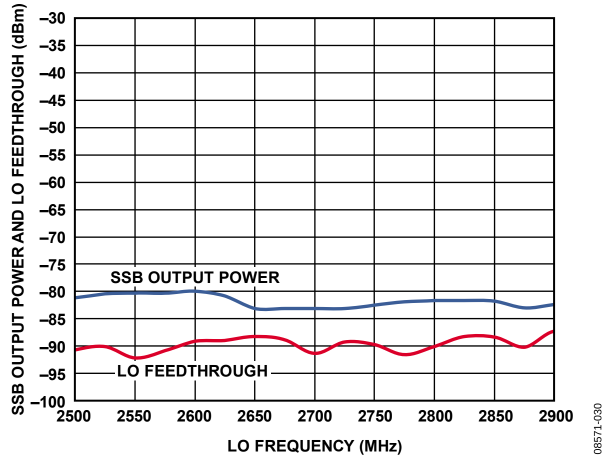

Figure 30. SSB Output Power and LO Feedthrough with RF Output Disabled

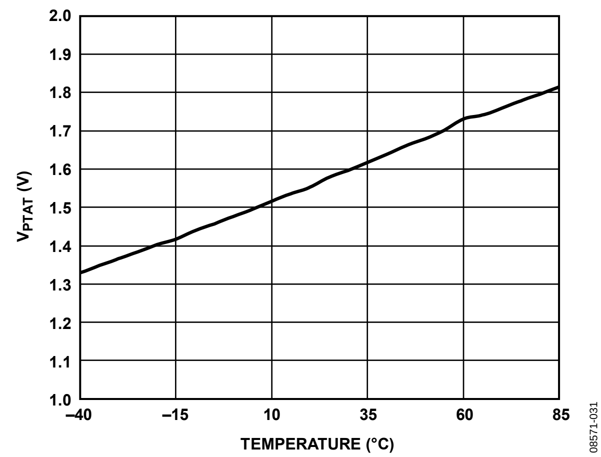

Figure 31. VPTAT Voltage vs. Temperature

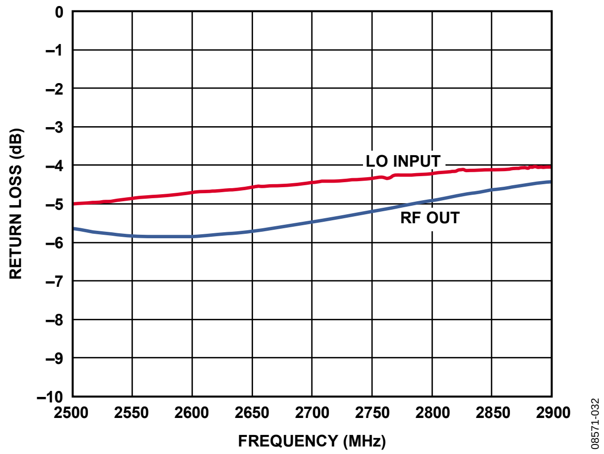

Figure 32. Input Return Loss of LO Input (LON, LOP Driven Through MABA-07159 1:1 Balun) and Output Return Loss of RFOUT vs. Frequency

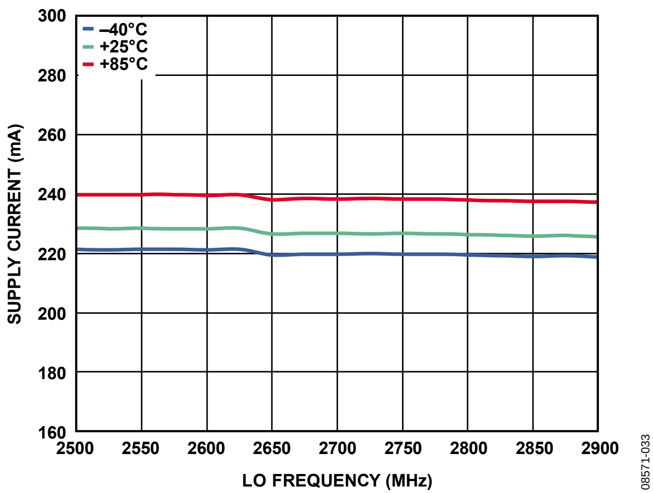

Figure 33. Power Supply Current vs. Frequency and Temperature (PLL and IQMOD Enabled, LO Buffer Disabled)

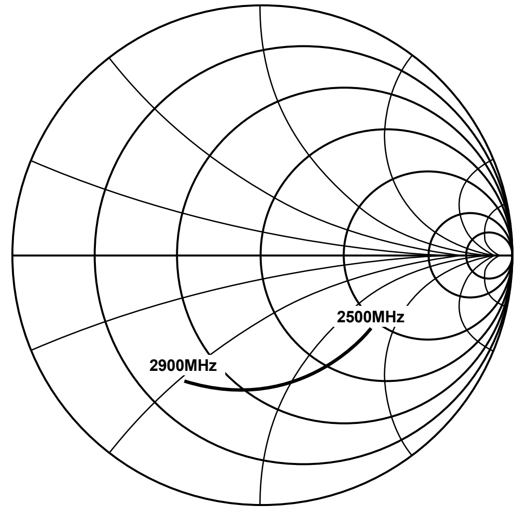

Figure 34. Smith Chart Representation of RF Output

THEORY OF OPERATION

The ADRF6704 integrates a high performance IQ modulator with a state of the art fractional-N PLL. The ADRF6704 also integrates a low noise VCO. The programmable SPI port allows the user to control the fractional-N PLL functions and the modulator optimization functions. This includes the capability to operate with an externally applied LO.

The quadrature modulator core within the ADRF6704 is a part of the next generation of industry-leading modulators from Analog Devices, Inc. The baseband inputs are converted to currents and then mixed to RF using high performance NPN transistors. The mixer output currents are transformed to a single-ended RF output using an integrated RF transformer balun. The high performance active mixer core, coupled with the low-loss RF transformer balun results in an exceptional OIP3 and OP1dB, with a very low output noise floor for excellent dynamic range. The use of a passive transformer balun rather than an active output stage leads to an improvement in OIP3 with no sacrifice in noise floor. At 2700 MHz the ADRF6704 typically provides an output P1dB of 12.1 dBm, OIP3 of 27.2 dBm, and an output noise floor of −158.3 dBm/Hz. Typical image rejection under these conditions is −37.7 dBc with no additional I and Q gain compensation.

PLL + VCO

The fractional divide function of the PLL allows the frequency multiplication value from REFIN to the LOP/LON outputs to be a fractional value rather than restricted to an integer as in traditional PLLs. In operation, this multiplication value is INT + (FRAC/MOD) where INT is the integer value, FRAC is the fractional value, and MOD is the modulus value, all of which are programmable via the SPI port. In previous fractional-N PLL designs, the fractional multiplication was achieved by periodically changing the fractional value in a deterministic way. The downside of this was often spurious components close to the fundamental signal. In the ADRF6704, a sigma delta modulator is used to distribute the fractional value randomly, thus significantly reducing the spurious content due to the fractional function.

BASIC CONNECTIONS FOR OPERATION

Figure 35 shows the basic connections for operating the ADRF6704 as they are implemented on the device's evaluation board. The seven power supply pins should be individually decoupled using 100 pF and 0.1 μF capacitors located as close as possible to the pins. A single 10 μF capacitor is also recommended. The three internal decoupling nodes (labeled DECL3, DECL2, and DECL1) should be individually decoupled with capacitors as shown in Figure 35.

The four I and Q inputs should be driven with a bias level of 500 mV. These inputs are generally dc-coupled to the outputs of a dual DAC (see the DAC-to-IQ Modulator Interfacing and IQ Filtering sections for more information).

A 1 V p-p (0.353 V rms) differential sine wave on the I and Q inputs results in a single sideband output power of +5.5 dBm (at 2700 MHz) at the RFOUT pin (this pin should be ac-coupled as shown in Figure 35). This corresponds to an IQ modulator voltage gain of +1.5 dB.

The reference frequency for the PLL (typically 1 V p-p between 11 MHz and 160 MHz) should be applied to the REFIN pin, which should be ac-coupled. If the REFIN pin is being driven from a 50 Ω source (for example, a lab signal generator), the pin should be terminated with 50 Ω as shown in Figure 35 (an RF drive level of +4 dBm should be applied). Multiples or fractions of the REFIN signal can be brought back off-chip at the multiplexer output pin (MUXOUT). A lock-detect signal and an analog voltage proportional to the ambient temperature can also be brought out on this pin by setting the appropriate bits on (DB21-DB23) in Register 4 (see the Register Description section).

EXTERNAL LO

The internally generated local oscillator (LO) signal can be brought off-chip as either a 1× LO or a 2× LO (via pins LOP and LON) by asserting the LOSEL pin and making the appropriate internal register settings. The LO output must be disabled whenever the RF output of the IQ modulator is disabled.

The LOP and LON pins can also be used to apply an external LO. This can be used to bypass the internal PLL/VCO. To turn off the PLL Register 6, Bits[20:17] must be zero.

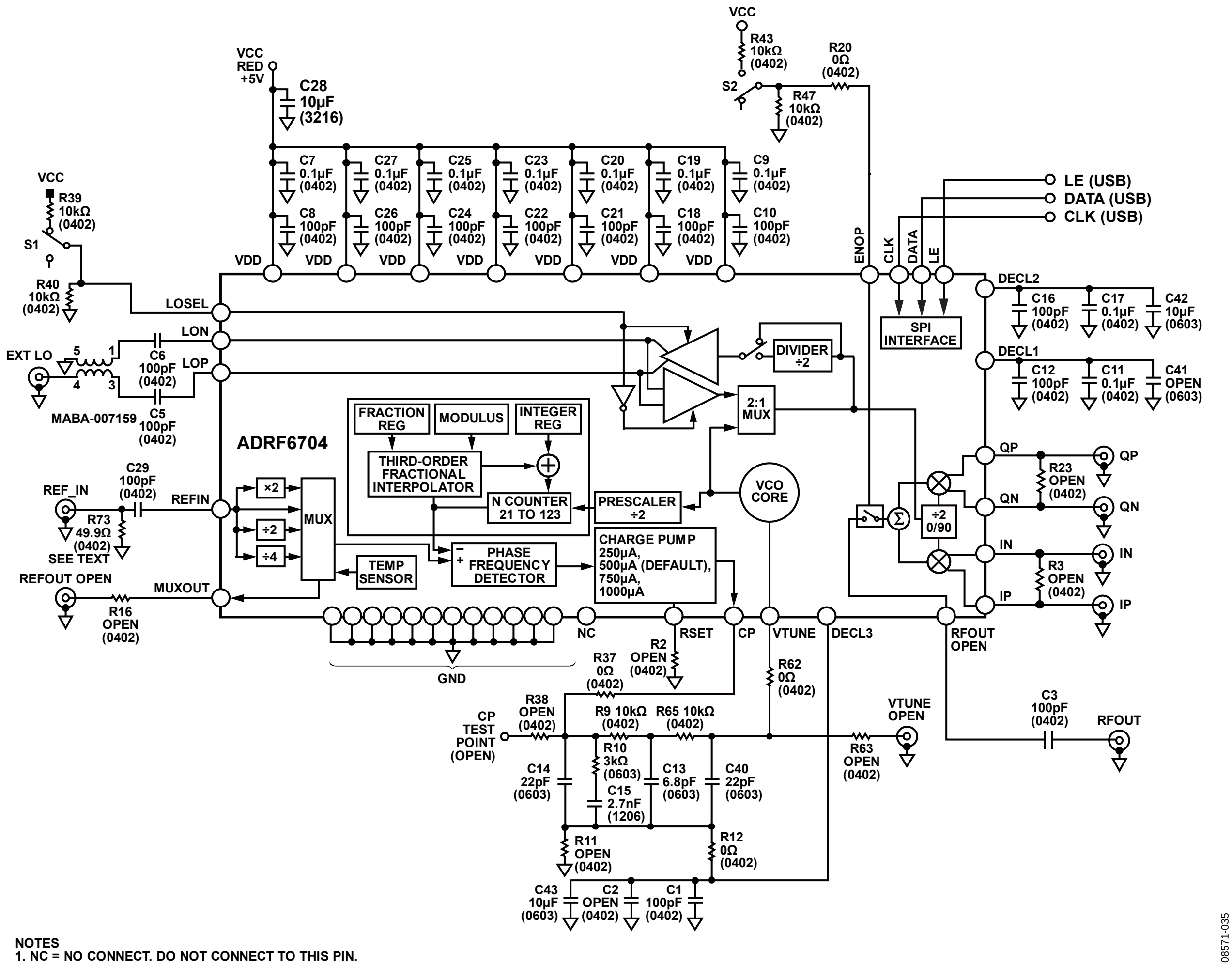

Figure 35. Basic Connections for Operation (Loop Filter Set to 130 kHz)

LOOP FILTER

The loop filter is connected between the CP and VTUNE pins. The return for the loop filter components should be to Pin 40 (DECL3). The loop filter design in Figure 35 results in a 3 dB loop bandwidth of 130 kHz. The ADRF6704 closed loop phase noise was also characterized using a 2.5 kHz loop filter design. The recommended components for both filter designs are shown in Table 8. For assistance in designing loop filters with other characteristics, download the most recent revision of ADIsimPLL™ from www.analog.com/adisimpll.

Table 8. Recommended Loop Filter Components

Component	130 kHz Loop Filter	2.5 kHz Loop Filter
C14	22 pF	0.1 µF
R10	3 kΩ	68 Ω
C15	2.7 nF	4.7 µF
R9	10 kΩ	270 Ω
C13	6.8 pF	47 nF
R65	10 kΩ	0 Ω
C40	22 pF	Open
R37	0 Ω	0 Ω
R11	Open	Open
R12	0 Ω	0 Ω

DAC-TO-IQ MODULATOR INTERFACING

The ADRF6704 is designed to interface with minimal components to members of the Analog Devices, Inc., family of TxDACs®. These dual-channel differential current output DACs provide an output current swing from 0 mA to 20 mA. The interface described in this section can be used with any DAC that has a similar output.

An example of an interface using the AD9122 TxDAC is shown in Figure 36. The baseband inputs of the ADRF6704 require a dc bias of 500 mV. The average output current on each of the outputs of the AD9122 is 10 mA. Therefore, a single 50 Ω resistor to ground from each of the DAC outputs results in an average current of 10 mA flowing through each of the resistors, thus producing the desired 500 mV dc bias for the inputs to the ADRF6704.

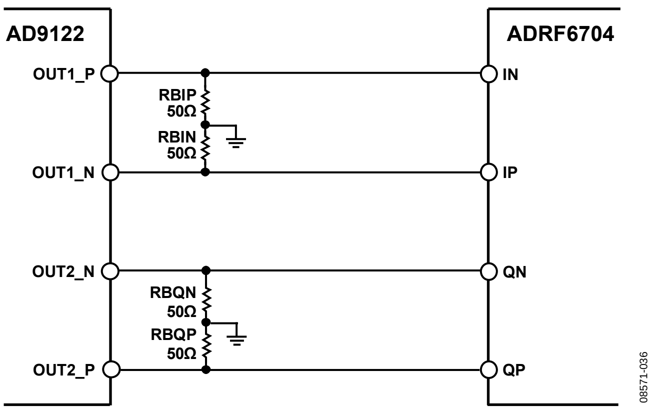

Figure 36. Interface Between the AD9122 and ADRF6704 with 50 Ω Resistors to Ground to Establish the 500 mV DC Bias for the ADRF6704 Baseband Inputs

The AD9122 output currents have a swing that ranges from 0 mA to 20 mA. With the 50 Ω resistors in place, the ac voltage swing going into the ADRF6704 baseband inputs ranges from 0 V to 1 V (with the DAC running at 0 dBFS). So the resulting drive signal from each differential pair is 2 V p-p differential with a 500 mV dc bias.

ADDING A SWING-LIMITING RESISTOR

The voltage swing for a given DAC output current can be reduced by adding a third resistor to the interface. This resistor is placed in the shunt across each differential pair, as shown in Figure 37. It has the effect of reducing the ac swing without changing the dc bias already established by the 50 Ω resistors.

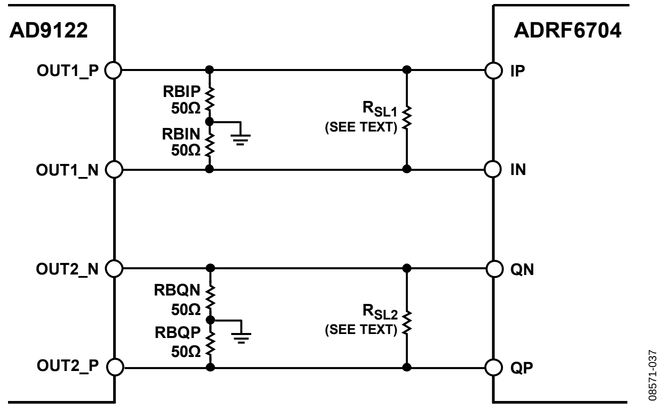

Figure 37. AC Voltage Swing Reduction Through the Introduction of a Shunt Resistor Between the Differential Pair

The value of this ac voltage swing limiting resistor (R_{SL} as shown in Figure 37) is chosen based on the desired ac voltage swing and IQ modulator output power. Figure 38 shows the relationship between the swing-limiting resistor and the peak-to-peak ac swing that it produces when 50 Ω bias-setting resistors are used. A higher value of swing-limiting resistor will increase the output power of the ADRF6704 and signal-to-noise ratio (SNR) at the cost if higher intermodulation distortion. For most applications, the optimum value for this resistor will be between 100 Ω and 300 Ω.

When setting the size of the swing-limiting resistor, the input impedance of the I and Q inputs should be taken into account. The I and Q inputs have a differential input resistance of 920 Ω. As a result, the effective value of the swing-limiting resistance is 920 Ω in parallel with the chosen swing-limiting resistor. For example, if a swing-limiting resistance of 200 Ω is desired (based on Figure 37), the value of R_{SL} should be set such that

$$200\ \Omega = (920 \times R_{SL})/(920 + R_{SL})$$

resulting in a value for R_{SL} of 255 Ω.

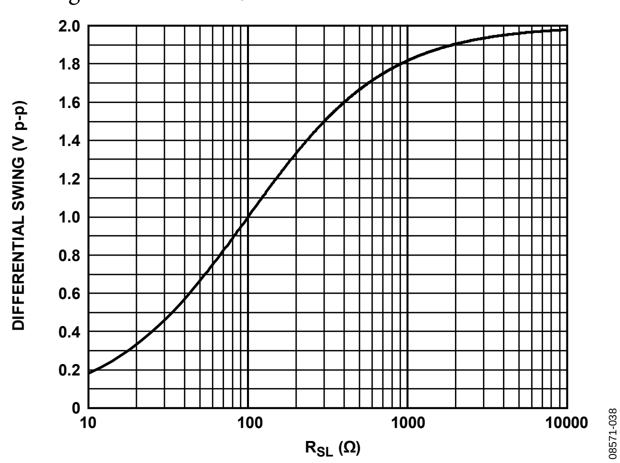

Figure 38. Relationship Between the AC Swing-Limiting Resistor and the Peak-to-Peak Voltage Swing with 50 Ω Bias-Setting Resistors

IQ FILTERING

An antialiasing filter must be placed between the DAC and modulator to filter out Nyquist images and broadband DAC noise. The interface for setting up the biasing and ac swing discussed in the Adding a Swing-Limiting Resistor section, lends itself well to the introduction of such a filter. The filter can be inserted between the dc bias setting resistors and the ac swing-limiting resistor. Doing so establishes the input and output impedances for the filter.

Unless a swing-limiting resistor of 100 Ω is chosen, the filter must be designed to support different source and load impedances. In addition, the differential input capacitance of the I and Q inputs (1 pF) should be factored into the filter design. Modern filter design tools allow for the simulation and design of filters with differing source and load impedances as well as inclusion of reactive load components.

BASEBAND BANDWIDTH

Figure 39 shows the frequency response of the ADRF6704's baseband inputs. This plot shows 0.5 dB and 3 dB bandwidths of 350 MHz and 750 MHz respectively. Any flatness variations across frequency at the ADRF6704 RF output have been calibrated out of this measurement.

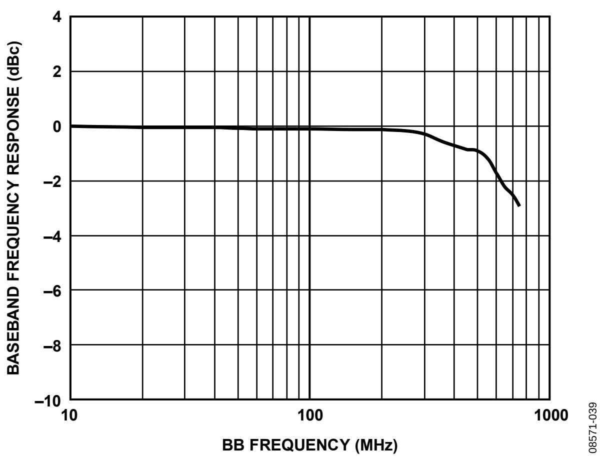

Figure 39. Baseband Bandwidth

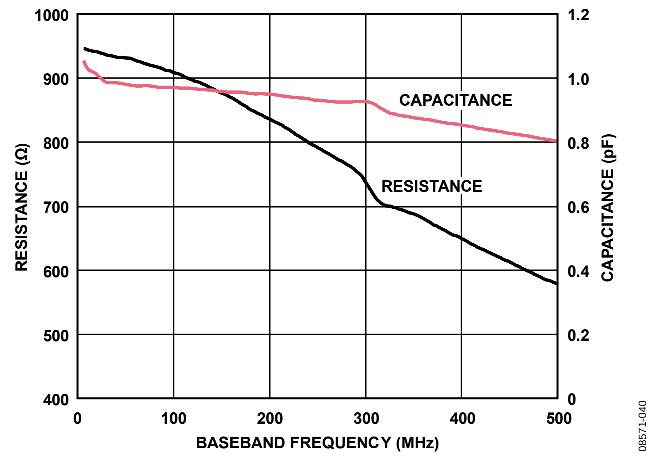

Figure 40. Differential Baseband Input R and Input C Equivalents (Shunt R and Shunt C)

DEVICE PROGRAMMING AND REGISTER SEQUENCING

The device is programmed via a 3-pin SPI port. The timing requirements for the SPI port are shown in Table 3 and Figure 2.

Seven programmable registers, each with 24 bits, control the operation of the device. The register functions are listed in Table 9. The seven registers should initially be programmed in reverse order, starting with Register 6 and finishing with Register 0. Once all seven registers have been initially programmed, any of the registers can be updated without any attention to sequencing.

Software is available on the ADRF6704 product page at www.analog.com that allows programming of the evaluation board from a PC running Windows® XP or Windows Vista.

To operate correctly under Windows XP, Version 3.5 of Microsoft .NET must be installed. To run the software on a Windows 7 PC, XP emulation mode must be used (using Virtual PC).

REGISTER SUMMARY

Table 9. Register Functions

Register	Function
Register 0	Integer divide control (for the PLL)
Register 1	Modulus divide control (for the PLL)
Register 2	Fractional divide control (for the PLL)
Register 3	Σ-Δ modulator dither control
Register 4	PLL charge pump, PFD, and reference path control
Register 5	LO path and modulator control
Register 6	VCO control and VCO enable

REGISTER DESCRIPTION

REGISTER 0—INTEGER DIVIDE CONTROL (DEFAULT: 0x0001C0)

With Register 0, Bits[2:0] set to 000, the on-chip integer divide control register is programmed as shown in Figure 41.

Divide Mode

Divide mode determines whether fractional mode or integer mode is used. In integer mode, the RF VCO output frequency (f_{VCO}) is calculated by

$$f_{VCO} = 2 \times f_{PFD} \times (INT) \quad (1)$$

where:
f_{VCO} is the output frequency of the internal VCO.
f_{PFD} is the frequency of operation of the phase-frequency detector.
INT is the integer divide ratio value (21 to 123 in integer mode).

Integer Divide Ratio

The integer divide ratio bits are used to set the integer value in Equation 2. The INT, FRAC, and MOD values make it possible to generate output frequencies that are spaced by fractions of the PFD frequency. The VCO frequency (f_{VCO}) equation is

$$f_{VCO} = 2 \times f_{PFD} \times (INT + (FRAC/MOD)) \quad (2)$$

where:
INT is the preset integer divide ratio value (24 to 119 in fractional mode).
MOD is the preset fractional modulus (1 to 2047).
$FRAC$ is the preset fractional divider ratio value (0 to MOD − 1).

RESERVED													DIVIDE MODE	INTEGER DIVIDE RATIO							CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	DM	ID6	ID5	ID4	ID3	ID2	ID1	ID0	C3(0)	C2(0)	C1(0)

DM	DIVIDE MODE
0	FRACTIONAL (DEFAULT)
1	INTEGER

ID6	ID5	ID4	ID3	ID2	ID1	ID0	INTEGER DIVIDE RATIO
0	0	1	0	1	0	1	21 (INTEGER MODE ONLY)
0	0	1	0	1	1	0	22 (INTEGER MODE ONLY)
0	0	1	0	1	1	1	23 (INTEGER MODE ONLY)
0	0	1	1	0	0	0	24
...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...
0	1	1	1	0	0	0	56 (DEFAULT)
...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...
1	1	1	0	1	1	1	119
1	1	1	1	0	0	0	120 (INTEGER MODE ONLY)
1	1	1	1	0	0	1	121 (INTEGER MODE ONLY)
1	1	1	1	0	1	0	122 (INTEGER MODE ONLY)
1	1	1	1	0	1	1	123 (INTEGER MODE ONLY)

08571-041

Figure 41. Register 0—Integer Divide Control Register Map

REGISTER 1—MODULUS DIVIDE CONTROL (DEFAULT: 0x003001)

With Register 1, Bits[2:0] set to 001, the on-chip modulus divide control register is programmed as shown in Figure 42.

Modulus Value

The modulus value is the preset fractional modulus ranging from 1 to 2047.

REGISTER 2—FRACTIONAL DIVIDE CONTROL (DEFAULT: 0x001802)

With Register 2, Bits[2:0] set to 010, the on-chip fractional divide control register is programmed as shown in Figure 43.

Fractional Value

The FRAC value is the preset fractional modulus ranging from 0 to <MDR.

RESERVED										MODULUS VALUE											CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	MD10	MD9	MD8	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	C3(0)	C2(0)	C1(1)

MD10	MD9	MD8	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	MODULUS VALUE
0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	1	0	2
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
1	1	0	0	0	0	0	0	0	0	0	1536 (DEFAULT)
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
1	1	1	1	1	1	1	1	1	1	1	2047

08571-042

Figure 42. Register 1—Modulus Divide Control Register Map

RESERVED										FRACTIONAL VALUE											CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0	C3(0)	C2(1)	C1(0)

FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0	FRACTIONAL VALUE
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
0	1	1	0	0	0	0	0	0	0	0	768 (DEFAULT)
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
											<MDR

FRACTIONAL VALUE MUST BE LESS THAN MODULUS.

08571-043

Figure 43. Register 2—Fractional Divide Control Register Map

REGISTER 3—Σ-Δ MODULATOR DITHER CONTROL (DEFAULT: 0x10000B)

With Register 3, Bits[2:0] set to 011, the on-chip Σ-Δ modulator dither control register is programmed as shown in Figure 44. The recommended and default setting for dither enable is enabled (1). The default value of the dither magnitude (15) should be set to a recommended value of 1.

The dither restart value can be programmed from 0 to $2^{17} - 1$, though a value of 1 is typically recommended.

	DITHER MAGNITUDE		DITHER ENABLE	DITHER RESTART VALUE																	CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	DITH1	DITH0	DEN	DV16	DV15	DV14	DV13	DV12	DV11	DV10	DV9	DV8	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0	C3(0)	C2(1)	C1(1)

DITH1	DITH0	DITHER MAGNITUDE
0	0	15 (DEFAULT)
0	1	7
1	0	3
1	1	1 (RECOMMENDED)

DEN	DITHER ENABLE
0	DISABLE
1	ENABLE (DEFAULT, RECOMMENDED)

DV16	DV15	DV14	DV13	DV12	DV11	DV10	DV9	DV8	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0	DITHER RESTART VALUE
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0x00001 (DEFAULT)
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0x1FFFF

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Figure 44. Register 3—Σ-Δ Modulator Dither Control Register Map

REGISTER 4—PLL CHARGE PUMP, PFD, AND REFERENCE PATH CONTROL (DEFAULT: 0x12A7E4)

With Register 4, Bits[2:0] set to 100, the on-chip charge pump, PFD, and reference path control register is programmed as shown in Figure 45.

CP Current

The nominal charge pump current can be set to 250 μA, 500 μA, 750 μA, or 1000 μA using DB10 and DB11 of Register 4 and by setting DB18 to 0 (CP reference source).

In this mode, no external RSET is required. If DB18 is set to 1, the four nominal charge pump currents ($I_{NOMINAL}$) can be externally tweaked according to the following equation:

$$R_{SET} = \left(\frac{217.4 \times I_{CP}}{I_{NOMINAL}}\right) - 37.8\,\Omega \quad (3)$$

where I_{CP} is the base charge pump current in microamps.

The PFD phase offset multiplier ($\theta_{PFD,OFS}$), which is set by Bits[16:12] of Register 4, causes the PLL to lock with a nominally fixed phase offset between the PFD reference signal and the divided-down VCO signal. This phase offset is used to linearize the PFD-to-CP transfer function and can improve fractional spurs. The magnitude of the phase offset is determined by the following equation:

$$|\Delta\Phi|(\text{deg}) = 22.5\frac{\theta_{PFD,OFS}}{I_{CP,MULT}} \quad (4)$$

The default value of the phase offset multiplier (10 × 22.5°) should be set to a recommended value of 6 × 22.5°.

This phase offset can be either positive or negative depending on the value of DB17 in Register 4.

The reference frequency applied to the PFD can be manipulated using the internal reference path source. The external reference frequency applied can be internally scaled in frequency by 2×, 1×, 0.5×, or 0.25×. This allows a broader range of reference frequency selections while keeping the reference frequency applied to the PFD within an acceptable range.

The device also has a MUXOUT pin that can be programmed to output a selection of several internal signals. The default mode is to provide a lock-detect output to allow the user to verify when the PLL has locked to the target frequency. In addition, several other internal signals can be passed to the MUXOUT pin as described in Figure 35.

REF OUPUT MUX SELECT			INPUT REF PATH		CP CURRENT REF SOURCE	PFD POL	PFD PHASE OFFSET MULTIPLIER					CP CURRENT		CP SOURCE	CP CONTROL		PFD EDGE		PFD ANTI-BACKLASH DELAY		CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RMS2	RMS1	RMS0	RS1	RS0	CPM	CPBD	CPB4	CPB3	CPB2	CPB1	CPB0	CPP1	CPP0	CPS	CPC1	CPC0	PE1	PE0	PAB1	PAB0	C3(1)	C2(0)	C1(0)

PAB1	PAB0	PFD ANTIBACKLASH DELAY
0	0	0ns (DEFAULT)
1	0	0.5ns
0	1	0.75ns
1	1	0.9ns

PE0	REFERENCE PATH EDGE SENSITIVITY
0	FALLING EDGE (RECOMMENDED)
1	RISING EDGE (DEFAULT)

PE1	DIVIDER PATH EDGE SENSITIVITY
0	FALLING EDGE (RECOMMENDED)
1	RISING EDGE (DEFAULT)

CPC1	CPC0	CHARGE PUMP CONTROL
0	0	BOTH ON
0	1	PUMP DOWN
1	0	PUMP UP
1	1	TRISTATE (DEFAULT)

CPS	CHARGE PUMP CONTROL SOURCE
0	CONTROL BASED ON STATE OF DB7/DB8 (CP CONTROL)
1	CONTROL FROM PFD (DEFAULT)

CPP1	CPP0	CHARGE PUMP CURRENT
0	0	250µA
0	1	500µA (DEFAULT)
1	0	750µA
1	1	1000µA

CPB4	CPB3	CPB2	CPB1	CPB0	PFD PHASE OFFSET MULTIPLIER
0	0	0	0	0	$0 \times 22.5°/I_{CP,MULT}$
0	0	0	0	1	$1 \times 22.5°/I_{CP,MULT}$
0	0	1	1	0	$6 \times 22.5°/I_{CP,MULT}$ (RECOMMENDED)
0	1	0	1	0	$10 \times 22.5°/I_{CP,MULT}$ (DEFAULT)
1	0	0	0	0	$16 \times 22.5°/I_{CP,MULT}$
1	1	1	1	1	$31 \times 22.5°/I_{CP,MULT}$

CPBD	PFD PHASE OFFSET POLARITY
0	NEGATIVE
1	POSITIVE (DEFAULT)

CPM	CHARGE PUMP CURRENT REFERENCE SOURCE
0	INTERNAL (DEFAULT)
1	EXTERNAL

RS1	RS0	INPUT REF PATH SOURCE
0	0	2× REFIN
1	0	REFIN (DEFAULT)
0	1	0.5× REFIN
1	1	0.25× REFIN

RMS2	RMS1	RMS0	REF OUTPUT MUX SELECT
0	0	0	LOCK DETECT (DEFAULT)
0	0	1	VPTAT
0	1	0	REFIN (BUFFERED)
0	1	1	0.5× REFIN (BUFFERED)
1	0	0	2× REFIN (BUFFERED)
1	0	1	TRISTATE
1	1	0	RESERVED
1	1	1	RESERVED

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Figure 45. Register 4—PLL Charge Pump, PFD, and Reference Path Control Register Map

REGISTER 5—LO PATH AND MODULATOR CONTROL (DEFAULT: 0X0000E5)

With Register 5, Bits[2:0] set to 101, the LO path and modulator control register is programmed as shown in Figure 46.

The modulator output or the complete modulator can be disabled using the modulator bias enable and modulator output enable addresses of Register 5.

The LO port (LOP and LON pins) can be used to apply an external 2× LO (that is, bypass internal PLL) to the IQ modulator. A differential LO drive of 0 dBm is recommended.

The LO port can also be used as an output where a 2× LO or 1× LO can be brought out and used to drive another mixer. The nominal output power provided at the LO port is 3 dBm. The mode of operation of the LO port is determined by the status of the LOSEL pin (3.3 V logic) along with the settings in a number of internal registers (see Table 10).

Table 10. LO Port Configuration[1, 2]

LON/LOP Function	LOSEL	Register 5, Bit DB5 (LDIV)	Register 5, Bit DB4 (LXL)	Register 5, Bit DB3 (LDRV)
Input (2× LO)	0	X	1	0
Output (Disabled)	0	X	0	0
Output (1× LO)	0	0	0	1
Output (1× LO)	1	0	0	0
Output (1× LO)	1	0	0	1
Output (2× LO)	0	1	0	1
Output (2× LO)	1	1	0	0
Output (2× LO)	1	1	0	1

[1] X = don't care.
[2] LOSEL should not be left floating.

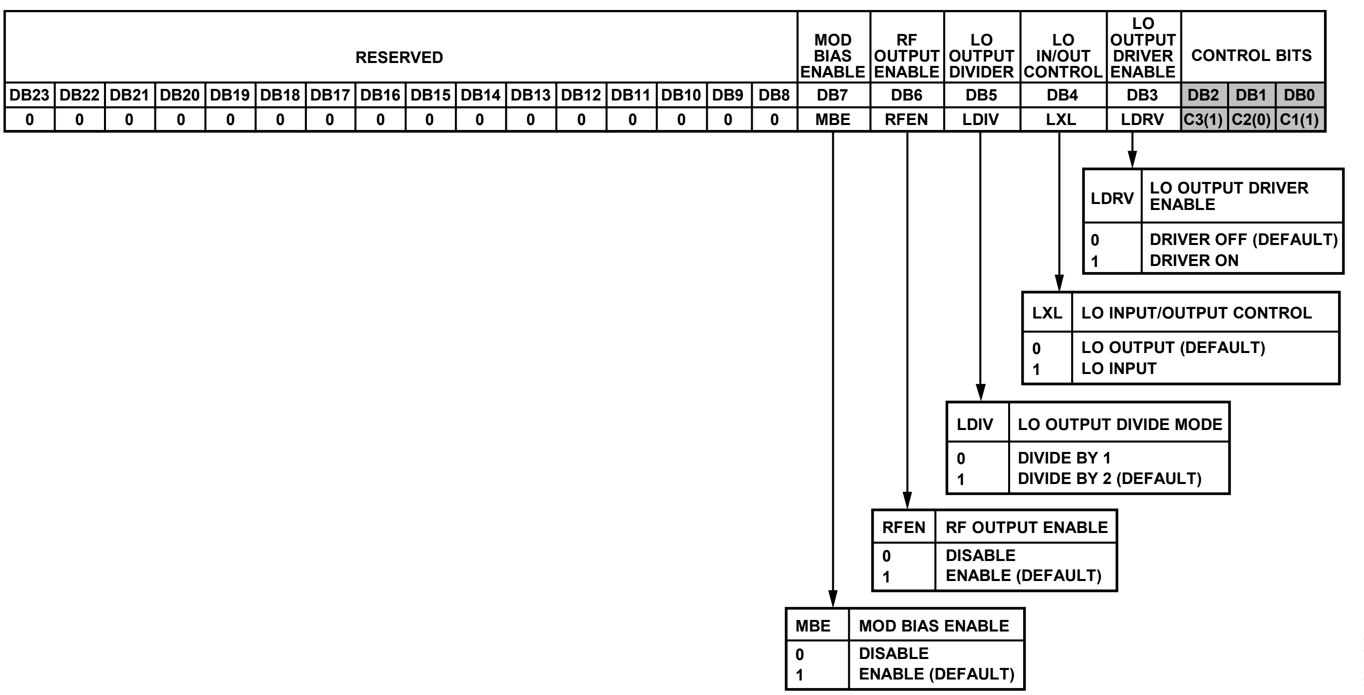


Figure 46. Register 5—LO Path and Modulator Control Register Map

REGISTER 6—VCO CONTROL AND VCO ENABLE (DEFAULT: 0X1E2106)

With Register 6, Bits[2:0] set to 110, the VCO control and enable register is programmed as shown in Figure 47.

The VCO tuning band is normally selected automatically by the band calibration algorithm, although the user can directly select the VCO band using Register 6.

The VCO BS SRC bit (DB9) determines whether the result of the calibration algorithm is used to select the VCO band or if the band selected is based on the value in VCO band select (DB8 to DB3).

The VCO amplitude can be controlled through Register 6. The VCO amplitude setting can be controlled between 0 and 63. The default value of 8 should be set to a recommended value of 63.

The internal VCOs can be disabled using Register 6.

The internal charge pump can be disabled through Register 6. By default, the charge pump is enabled.

To turn off the PLL (for example, if the ADRF6704 is being driven by an external LO), set Register 6, Bits[20:17] to zero.

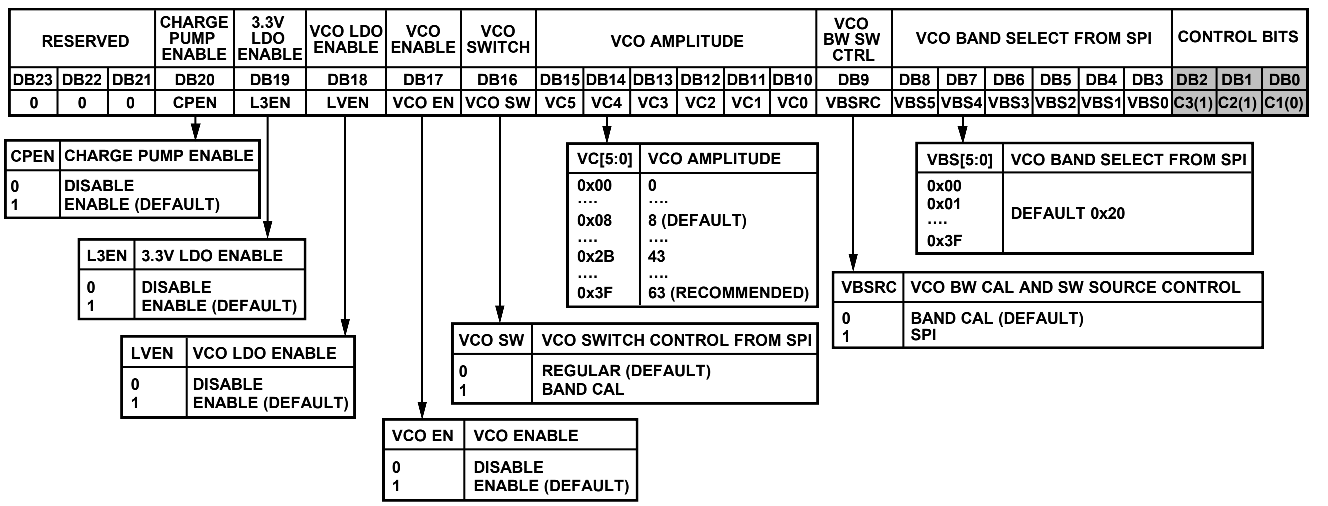


Figure 47. Register 6—VCO Control and VCO Enable Register Map

CHARACTERIZATION SETUPS

Figure 48 and Figure 49 show characterization bench setups used to characterize the ADRF6704. The setup shown in Figure 48 was used to do most of the testing. An automated VEE program was used to control equipment over the IEEE bus. The setup was used to measure SSB, OIP2, OIP3, OP1dB, LO, and USB NULL.

For phase noise and reference spurs measurements, see the phase noise setup on Figure 49. Phase noise was measured on LO and modulator output.

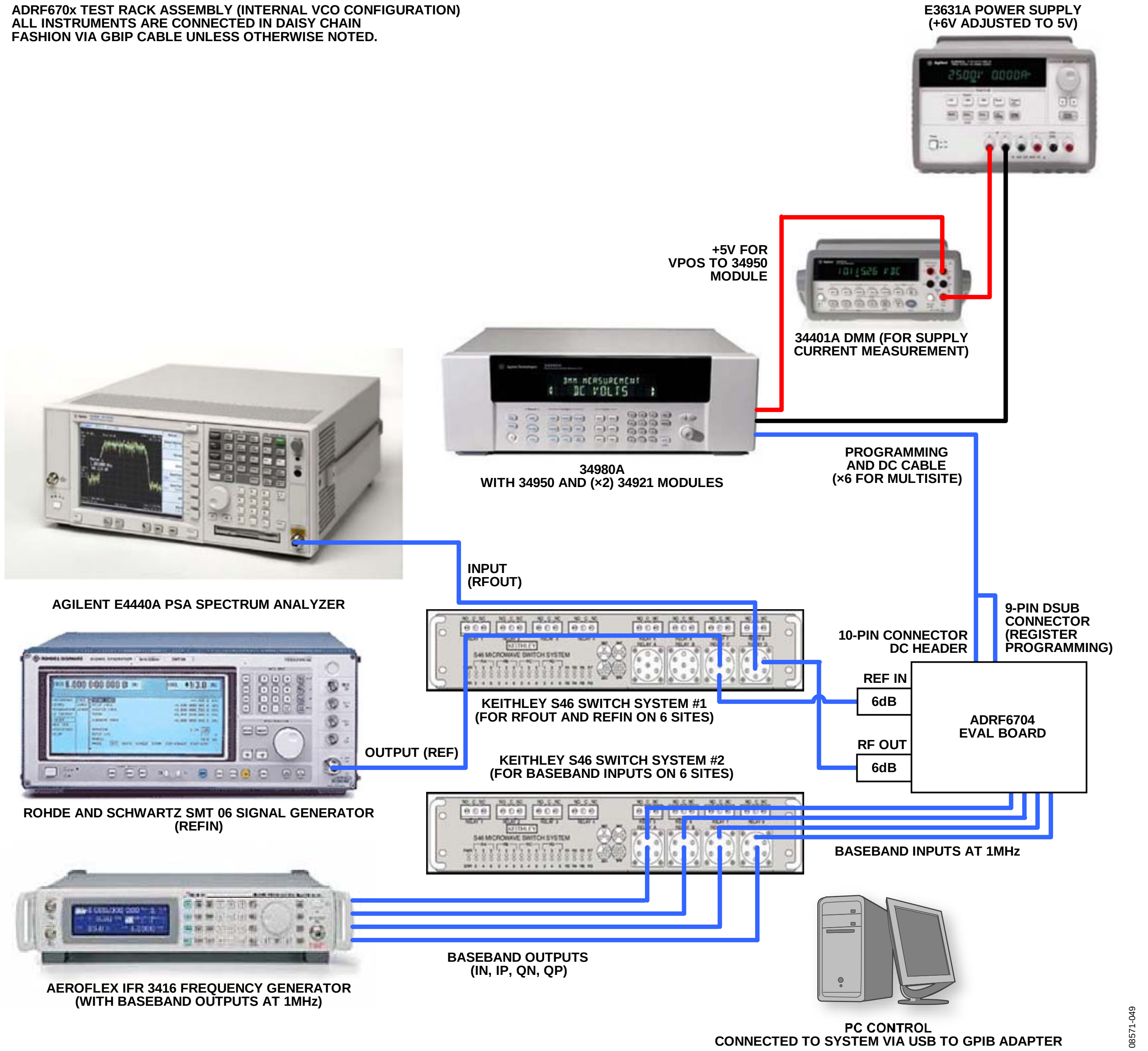


Figure 48. General Characterization Setup

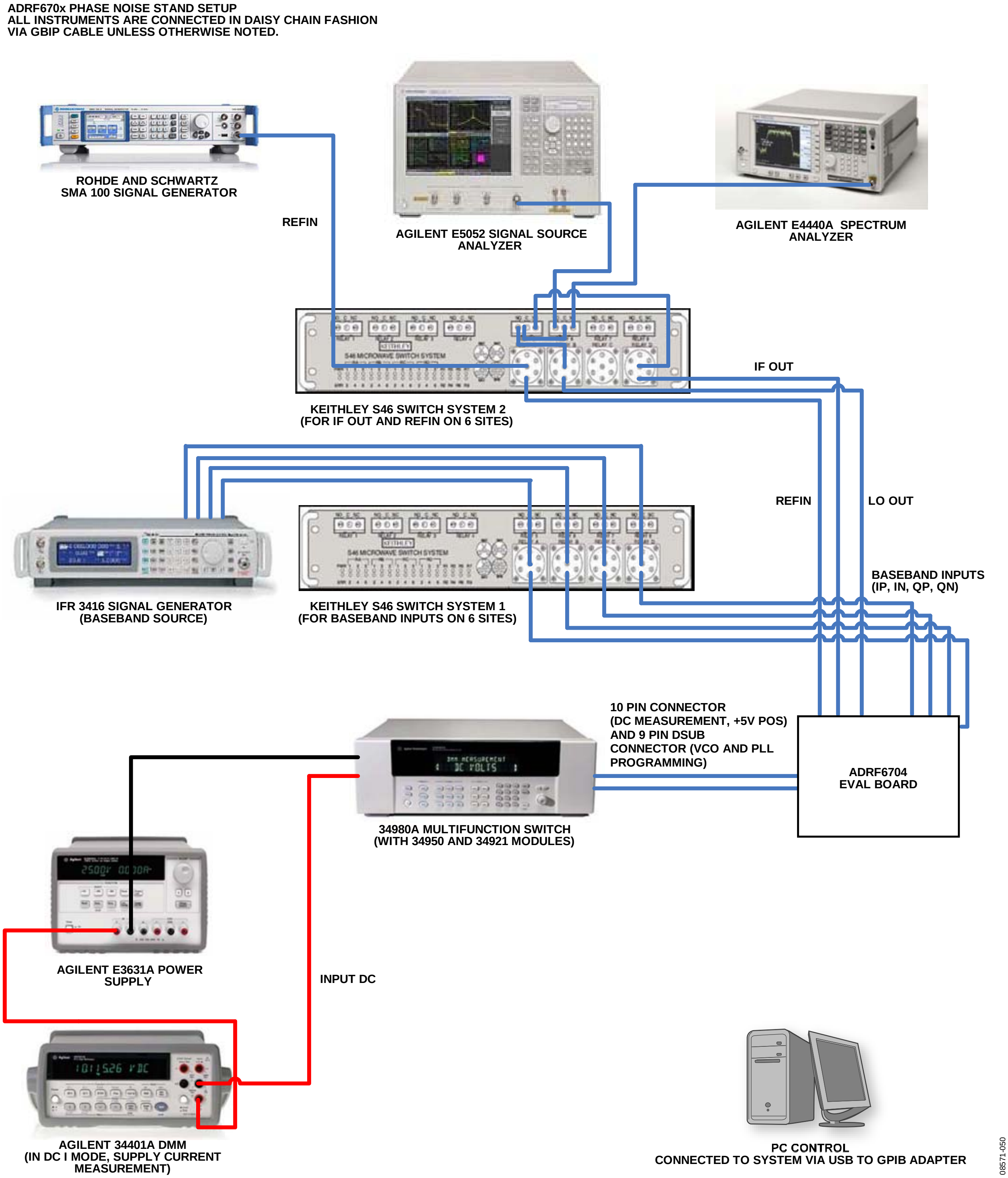


Figure 49. Characterization Setup for Phase Noise and Reference Spur Measurements

EVALUATION BOARD

Figure 51 shows the schematic of the device's RoHS-compliant evaluation board. This board was designed using Rogers 4350 material to minimize losses at high frequencies. FR4 material would also be adequate but with the slightly higher trace loss of this material.

Whereas the on-board USB interface circuitry of the evaluation board is powered directly from the PC, the main section of the evaluation board requires a separate 5 V power supply.

The evaluation board is designed to operate using the internal VCO (default configuration) of the device. Additional configuration options for the evaluation board are described in Table 11.

The serial port of the ADRF6704 can be programmed from a PC's USB port (a USB cable is provided with the evaluation board). The on-board USB interface circuitry can if desired be bypassed by removing the 0 Ω resistors, R15, R17, and R18 (see Figure 51) and driving the ADRF6704 serial interface through the P3 4-pin header (P3 must be first installed, Samtec TSW-104-08-G-S).

EVALUATION BOARD CONTROL SOFTWARE

USB-based programming software is available to download from the ADRF6704 product page at www.analog.com (Evaluation Board Software Rev 6.1.0). To install the software, download and extract the zip file. Then run the following installation file: **ADRF6X0X_6p1p0_customer_installer.exe**.

To operate correctly under Windows XP, Version 3.5 of Microsoft .NET must be installed. To run the software on a Windows 7 PC, XP emulation mode must be used (using Virtual PC).

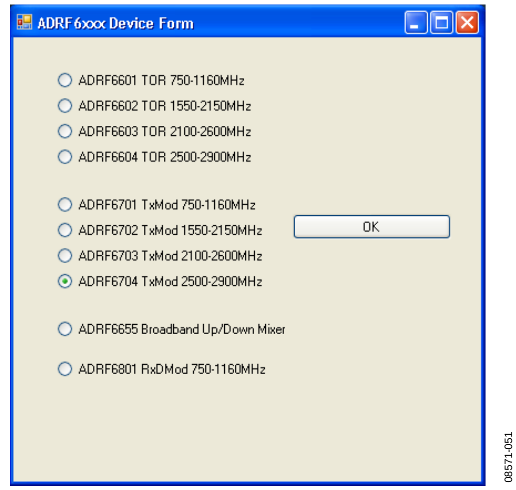
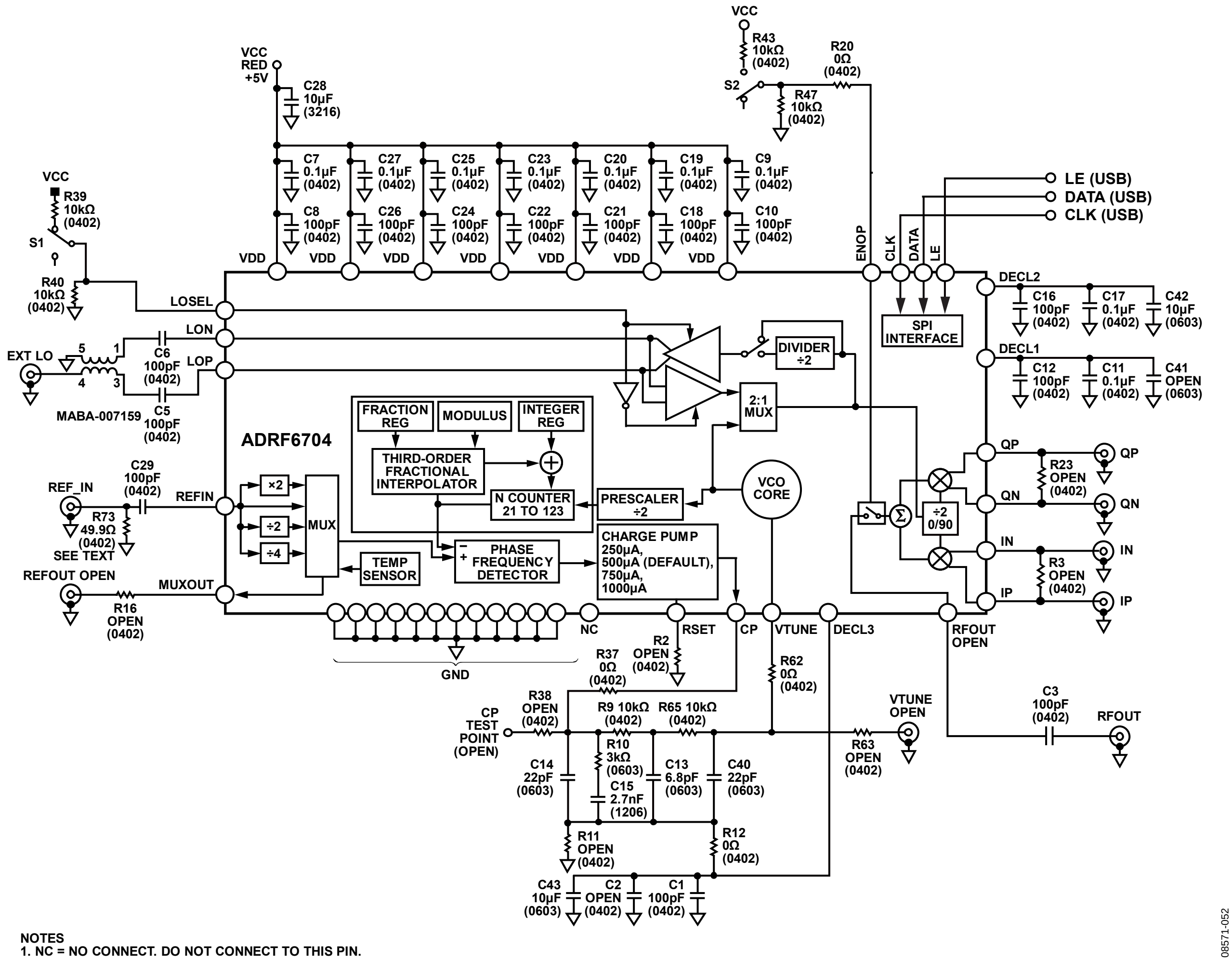


Figure 50. Control Software Opening Menu

Figure 50 shows the opening window of the software where the user selects the device being programmed. Figure 54 shows a screen shot of the control software's main controls with the default settings displayed. The text box in the bottom left corner provides an immediate indication of whether the software is successfully communicating with the evaluation board. If the evaluation board is connected to the PC via the USB cable provided and the software is successfully communicating with the on-board USB circuitry, this text box shows the following message: **ADRF6X0X eval board connected**.



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 51. Evaluation Board Schematic (Loop Filter Set to 130 kHz)

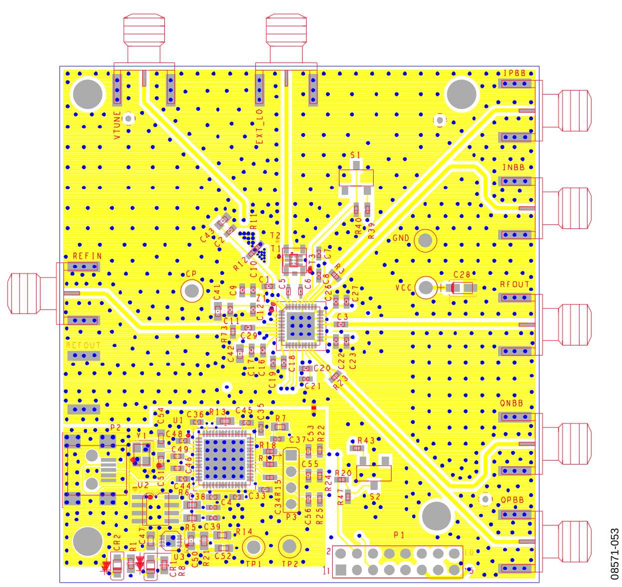


Figure 52. Evaluation Board Top Layer

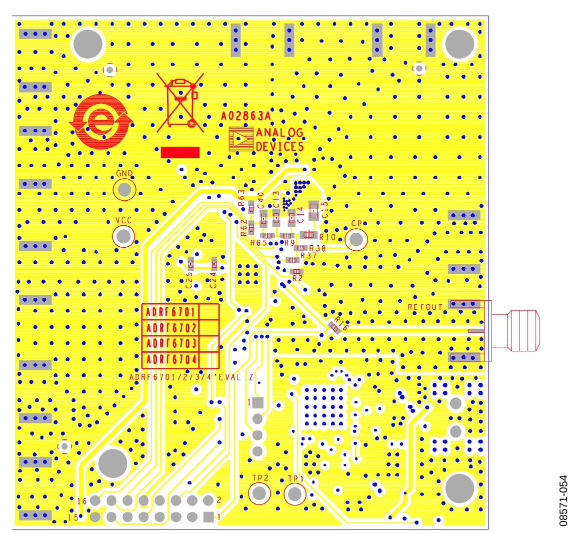


Figure 53. Evaluation Board Bottom Layer

Table 11. Evaluation Board Configuration Options

Component	Description	Default Condition/Option Settings
S1, R39, R40	LO select. Switch and resistors to ground LOSEL pin. The LOSEL pin setting in combination with internal register settings, determines whether the LOP/LON pins function as inputs or outputs. With the LOSEL pin grounded, register settings can set the LOP/LON pins to be inputs or outputs.	
EXT LO, T3	LO input/output. An external 1× LO or 2× LO can be applied to this single-ended input connector. Alternatively, the internal 1× or 2× LO can be brought out on this pin. The differential LO signal on LOP and LON is converted to a single-ended signal using a broadband 1:1 balun (Macom MABA-007159, 4.5 MHz to 3000 MHz frequency range). The balun footprint on the evaluation board is also designed to accommodate Johanson baluns: 3600BL14M050 (1:1, 3.3 GHz to 3.9 GHz) and 3700BL15B050E (1:1, 3.4 GHz to 4 GHz).	T3 = Macom MABA-007159 EXT LO SMA connector = installed
REFIN SMA Connector, R73	Reference input. The input reference frequency for the PLL is applied to this connector. Input resistance is set by R73 (49.9 Ω).	F_{REFIN} = 153.6 MHz R73 = 49.9 Ω
REFOUT SMA Connector, R16	Multiplexer output. The REFOUT connector connects directly to the device's MUXOUT pin. The on-board multiplexer can be programmed to bring out the following signals: REFIN, 2× REFIN, REFIN/2, REFIN/4, Temperature sensor output voltage (VPTAT), Lock detect indicator.	REFOUT SMA connector = open R16 = open
CP Test Point, R38	Charge pump test point. The unfiltered charge pump signal can be probed at this test point. Note that this pin should not be probed during critical measurements such as phase noise.	CP = open R38 = open
C13, C14, C15, C40R9, R10, R37, R65	Loop filter. Loop filter components.	See Table 8
R11, R12, R62, R63, VTUNE SMA Connector	When the internal VCO is enabled, the loop filter components connect directly to the VTUNE pin (Pin 39) by installing a 0 Ω resistor in R62. In addition, the loop filter components should be returned to Pin 40 (DECL3) by installing a 0 Ω resistor in R12.	R12 = 0 Ω (0402) R11 = open (0402) R62 = 0 Ω (0402) R63 = open (0402) VTUNE = open
R2	RSET. This pin is unused and should be left open.	R2 = open (0402)
R23, R3	Baseband input termination. Termination resistors for the baseband filter of the DAC can be placed on R23 and R3. In addition to terminating the baseband filters, these resistors also scale down the baseband voltage from the DAC without changing the bias level. These resistors are generally set in the 100 Ω to 300 Ω range.	R3 = R23 = open (0402)
P3 4-Pin Header, R15, R17, R18	USB circuitry bypass. The USB circuitry can be bypassed, allowing for the serial port of the ADRF6704 to be driven directly. P3 (Samtec TSW-104-08-G-S) must be installed, and 0 Ω resistors (R15, R17 and R18) must be removed.	P3 = open R15, R17, R18 = 0 Ω (0402)

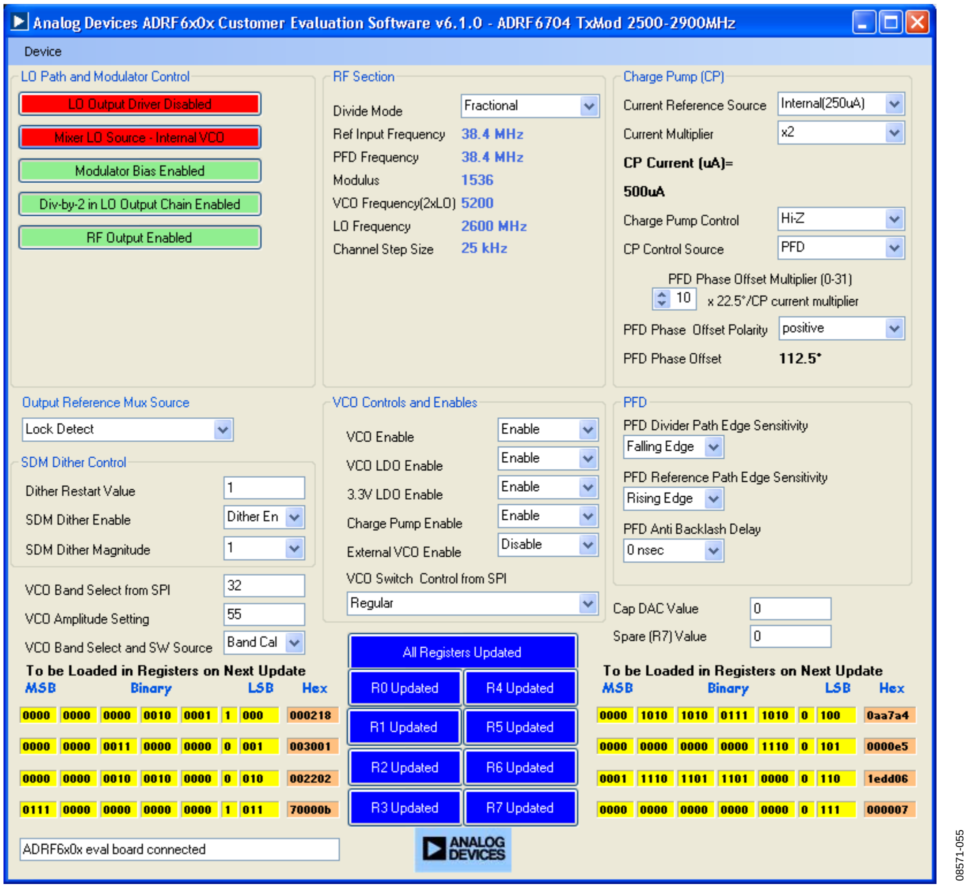


Figure 54. Main Controls of the Evaluation Board Control Software

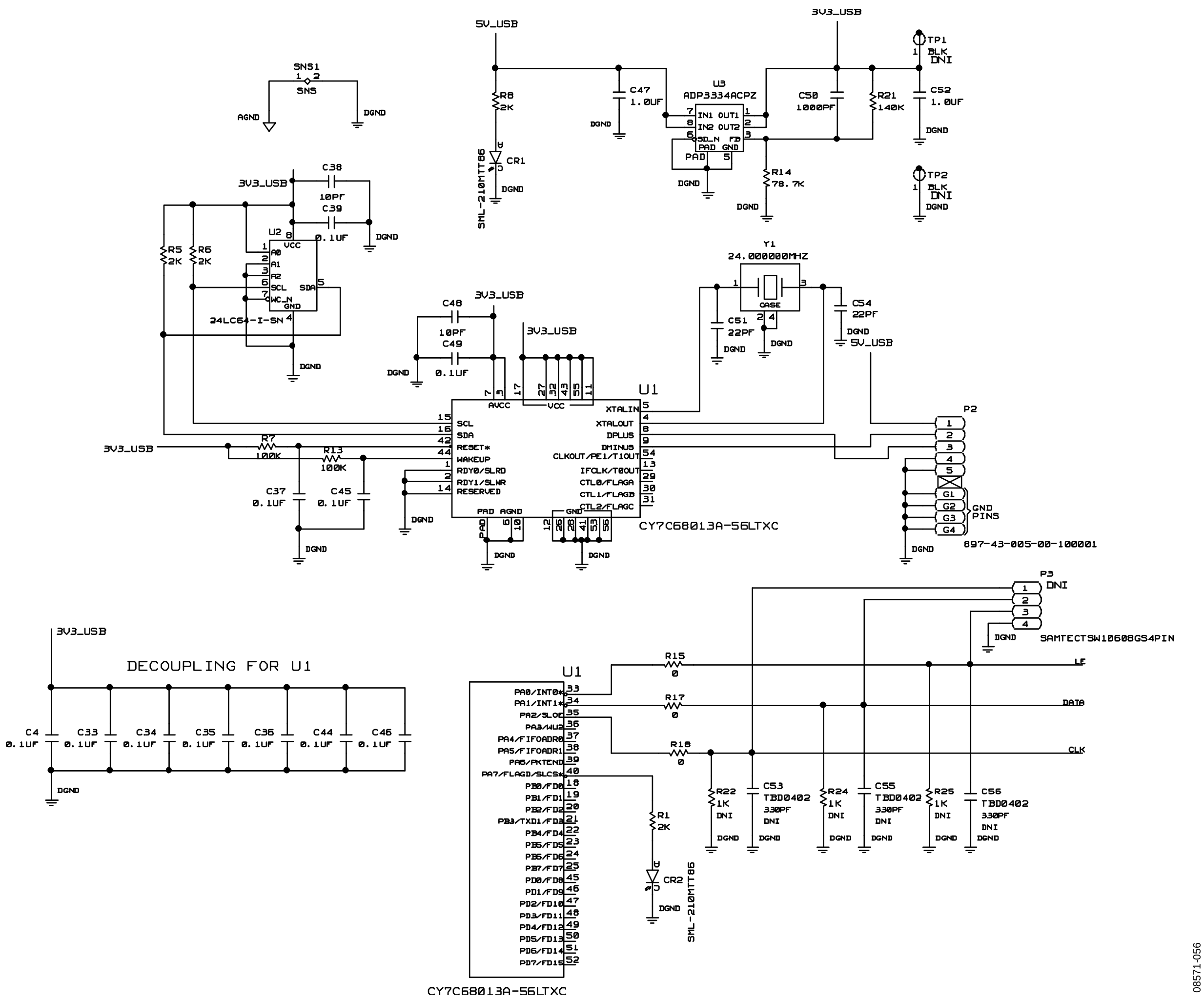


Figure 55. USB Interface Circuitry on the Customer Evaluation Board

OUTLINE DIMENSIONS

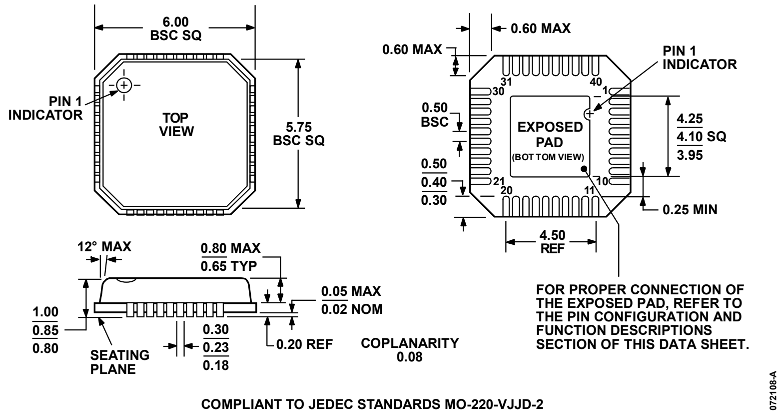


Figure 56. 40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
6 mm × 6 mm Body, Very Thin Quad
(CP-40-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range (°C)	Package Description	Package Option
ADRF6704ACPZ-R7	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-40-1
ADRF6704-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES