6 GHz to 18 GHz, Front-End IC

Data Sheet

ADTR1107

FEATURES

- Operates from 6 GHz to 18 GHz
- 25 dBm typical transmit state P_{SAT}
- 22 dB typical transmit state small signal gain
- 18 dB typical receive state small signal gain
- 2.5 dB typical receive state noise figure
- Coupled power amplifier output for power detection

APPLICATIONS

- Phased array antenna
- Military radar
- Weather radar
- Communication links
- Electronic warfare

FUNCTIONAL BLOCK DIAGRAM

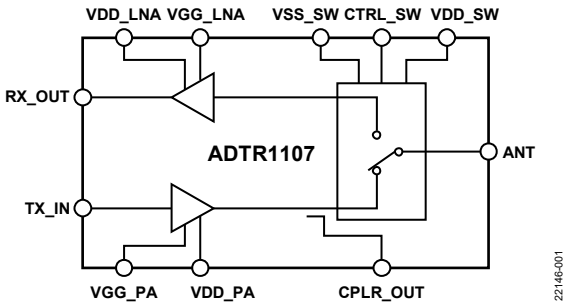

Figure 1.

GENERAL DESCRIPTION

The ADTR1107 is a compact, 6 GHz to 18 GHz, front-end IC with an integrated power amplifier, low noise amplifier (LNA), and a reflective single-pole double-throw (SPDT) switch. These integrated features make the device ideal for phased array antenna and radar applications. The front-end IC offers 25 dBm of saturated output power (P_{SAT}) and 22 dB small signal gain in transmit state, and 18 dB small signal gain and 2.5 dB noise figure in receive state. The device has a directional coupler for power detection. The input/outputs (I/Os) are internally matched to 50 Ω. The ADTR1107 is supplied in a 5 mm × 5 mm, 24-terminal, land grid array (LGA) package.

Rev. A
Document Feedback

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REVISION HISTORY

4/2020—Rev. 0 to Rev. A

Changes to VDD_LNA Parameter, Table 4 ... 5

1/2020—Revision 0: Initial Version

SPECIFICATIONS

Transmit state, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, VDD_SW = 3.3 V, VSS_SW = −3.3 V, CTRL_SW = 0 V, receive state off (VDD_LNA = 0 V, VGG_LNA = 0 V), T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OVERALL FUNCTION						
Frequency Range		6		14	GHz	
TRANSMIT STATE						
Small Signal Gain		19.5	21.5		dB	TX_IN to ANT
Gain Flatness			±0.8		dB	
Input Return Loss			13		dB	TX_IN to ANT
Output Return Loss			15		dB	TX_IN to ANT
Output 1 dB Compression (OP1dB)		21	23		dBm	TX_IN to ANT
Saturated Output Power (P_{SAT})			25		dBm	
Output Third-Order Intercept (OIP3)			31		dBm	TX_IN to ANT output power (P_{OUT}) per tone = 8 dBm
Noise Figure			9		dB	TX_IN to ANT
Coupling Factor			23.5		dB	Coupling factor = ANT P_{OUT} − CPLR_OUT P_{OUT}
Isolation						
TX_IN to RX_OUT			40		dB	Receive state off
ANT to RX_OUT			64		dB	Receive state off
RF Settling Time						
0.1 dB			17		ns	50% CTRL_SW to 0.1 dB of final RF output
0.05 dB			22		ns	50% CTRL_SW to 0.05 dB of final RF output
Switching Speed						
Rise and Fall Time	t_{RISE}, t_{FALL}		2		ns	10% to 90% of RF output
Turn On and Turn Off Time	t_{ON}, t_{OFF}		10		ns	50% CTRL_SW to 90% of RF output
VDD_PA		3.3	5.0	5.5	V	
Quiescent Current (I_{DQ}_PA)			220		mA	Adjust VGG_PA voltage between −1.75 V and −0.25 V to achieve the desired I_{DQ}_PA

Transmit state, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, VDD_SW = 3.3 V, VSS_SW = −3.3 V, CTRL_SW = 0 V, receive state off, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OVERALL FUNCTION						
Frequency Range		14		18	GHz	
TRANSMIT STATE						
Small Signal Gain		20	22		dB	TX_IN to ANT
Gain Flatness			±0.6		dB	
Input Return Loss			12		dB	TX_IN to ANT
Output Return Loss			11		dB	TX_IN to ANT
OP1dB		19	21.5		dBm	TX_IN to ANT
P_{SAT}			24		dBm	TX_IN to ANT
OIP3			31.5		dBm	TX_IN to ANT P_{OUT} per tone = 8 dBm
Noise Figure			6.5		dB	TX_IN to ANT
Coupling Factor			18		dB	Coupling factor = ANT P_{OUT} − CPLR_OUT P_{OUT}
Isolation						
TX_IN to RX_OUT			39		dB	Receive state off
ANT to RX_OUT			64		dB	Receive state off

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RF Settling Time						
0.1 dB			17		ns	50% CTRL_SW to 0.1 dB of final RF output
0.05 dB			22		ns	50% CTRL_SW to 0.05 dB of final RF output
Switching Speed						
Rise and Fall Time	t_{RISE}, t_{FALL}		2		ns	10% to 90% of RF output
Turn On and Turn Off Time	t_{ON}, t_{OFF}		10		ns	50% CTRL_SW to 90% of RF output
VDD_PA		3.3	5.0	5.5	V	
I_{DQ}_PA			220		mA	Adjust VGG_PA voltage between −1.75 V and −0.25 V to achieve the desired I_{DQ}_PA

Receive state, self biased, VDD_LNA = 3.3 V, VGG_LNA = 0 V, VDD_SW = 3.3 V, VSS_SW = −3.3 V, CTRL_SW = 3.3 V, transmit state off (VDD_PA = 0 V, VGG_PA = −1.75 V), T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OVERALL FUNCTION						
Frequency Range		6		14	GHz	
RECEIVE STATE						
Small Signal Gain		15.5	17.5		dB	ANT to RX_OUT
Gain Flatness			±0.6		dB	
Input Return Loss			13		dB	ANT to RX_OUT
Output Return Loss			14		dB	ANT to RX_OUT
OP1dB		12	14		dBm	ANT to RX_OUT
P_{SAT}			16		dBm	
OIP3			26		dBm	ANT to RX_OUT P_{OUT} per tone = 0 dBm
Noise Figure			2.5		dB	ANT to RX_OUT
Isolation						
ANT to TX_IN			32		dB	Transmit state off
RX_OUT to TX_IN			48		dB	Transmit state off
RF Settling Time						
0.1 dB			17		ns	50% CTRL_SW to 0.1 dB of final RF output
0.05 dB			22		ns	50% CTRL_SW to 0.05 dB of final RF output
Switching Speed						
Rise and Fall Time	t_{RISE}, t_{FALL}		2		ns	10% to 90% of RF output
Turn On and Turn Off Time	t_{ON}, t_{OFF}		10		ns	50% CTRL_SW to 90% of RF output
VDD_LNA		2.0	3.3	3.6	V	
I_{DQ}_LNA			80		mA	Self biased

Receive state, self biased, VDD_LNA = 3.3 V, VGG_LNA = 0 V, VDD_SW = 3.3 V, VSS_SW = −3.3 V, CTRL_SW = 3.3 V, transmit state off, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OVERALL FUNCTION						
Frequency Range		14		18	GHz	
RECEIVE STATE						
Small Signal Gain		16	18		dB	ANT to RX_OUT
Gain Flatness			±0.9		dB	
Input Return Loss			13		dB	ANT to RX_OUT
Output Return Loss			18		dB	ANT to RX_OUT
OP1dB		12	14		dBm	ANT to RX_OUT
P_{SAT}			16.5		dBm	ANT to RX_OUT

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OIP3			25.5		dBm	ANT to RX_OUT P_{OUT} per tone = 0 dBm
Noise Figure			3		dB	ANT to RX_OUT
Isolation						
ANT to TX_IN			26		dB	Transmit state off
RX_OUT to TX_IN			46		dB	Transmit state off
RF Settling Time						
0.1 dB			17		ns	50% CTRL_SW to 0.1 dB of final RF output
0.05 dB			22		ns	50% CTRL_SW to 0.05 dB of final RF output
Switching Speed						
Rise and Fall Time	t_{RISE}, t_{FALL}		2		ns	10% to 90% of RF output
Turn On and Turn Off Time	t_{ON}, t_{OFF}		10		ns	50% CTRL_SW to 90% of RF output
VDD_LNA		2.0	3.3	3.6	V	
I_{DQ}_LNA			80		mA	Self biased

SPDT switch bias at VDD_SW = 3.3 V, VSS_SW = −3.3 V.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						VDD_SW and VSS_SW
Positive	IDD_SW		14		µA	
Negative	ISS_SW		120		µA	
DIGITAL CONTROL INPUTS						CTRL_SW
Voltage						
Low		0		0.8	V	
High		1.2		3.3	V	
Current (Low and High)			<1		µA	

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Transmit State (PA On), Receive State Off	
VDD_PA	5.5 V
VGG_PA	−2 V to +0 V
Continuous Wave (CW) RF Input Power (RFIN) at TX_IN	20 dBm
Continuous Power Dissipation (P_{DISS}) (T_A = 85°C, Derate 18.98 mW/°C Above 85°C)	1.71 W
Receive State (LNA On), Transmit State Off	
VDD_LNA	4 V
VGG_LNA	−2 V to +0.2 V
CW RFIN at ANT	20 dBm
P_{DISS} (T_A = 85°C, Derate 5.04 mW/°C Above 85°C)	0.453 W
Transmit and Receive States	
Output Load Voltage Standing Wave Ratio (VSWR)	7:1
VDD_SW Range	−0.3 V to +3.6 V
VSS_SW Range	−3.6 V to +0.3 V
VDD_CTRL Range	−0.3 V to VDD + 0.3 V
Channel Temperature	175°C
Maximum Peak Reflow Temperature (Moisture Sensitivity Level 3, MSL3)[1]	260°C
Storage Temperature Range	−40°C to +125°C
Operating Temperature Range	−40°C to +85°C
ESD Sensitivity (Human Body Model)	Class 1B (Passed ±500 V)

[1] See the Ordering Guide section for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the thermal resistance from the operating portion of the device to the outside surface of the package (case) closest to the device mounting area.

Table 7. Thermal Resistance[1]

Package Type	θ_{JC} Transmit State	θ_{JC} Receive State	Unit
CC-24-8	52.7	198.4	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with 36 thermal vias. Refer to the JEDEC standard JESD51 for additional information.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 8. Signal Path Truth Table

State	CTRL_SW	RF Signal Path
Transmit	Low	TX_IN to ANT
Receive	High	ANT to RX_OUT

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

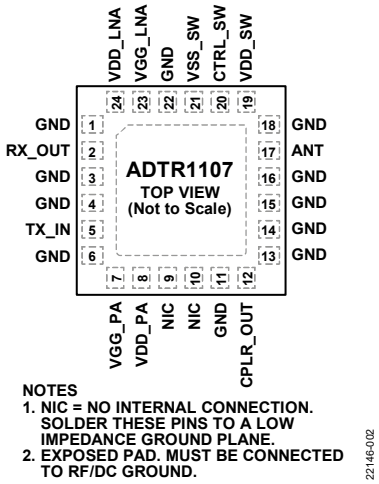

Figure 2. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 4, 6, 11, 13 to 16, 18, 22	GND	Ground. Solder these pins to a low impedance ground plane.
2	RX_OUT	Receive Path Output. This pin is dc-coupled to ground and ac matched to 50 Ω.
5	TX_IN	Transmit Path Input. This pin is dc-coupled to ground and ac matched to 50 Ω.
7	VGG_PA	Power Amplifier Gate Bias. This pin is used to set the desired quiescent current of the amplifier.
8	VDD_PA	Power Amplifier Drain Bias Voltage.
9, 10	NIC	No Internal Connection. Solder these pins to a low impedance ground plane.
12	CPLR_OUT	Transmit Path Coupled Port. This port is used in connection with a detector to monitor transmitted power.
17	ANT	RF Common Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω.
19	VDD_SW	SPDT Switch Positive Bias Voltage.
20	CTRL_SW	Switch Digital Control. This pin controls the state of the SPDT switch.
21	VSS_SW	SPDT Switch Negative Bias Voltage.
23	VGG_LNA	LNA Gate Voltage Bias. This pin is used to set the desired quiescent current of the LNA. If this pin is supplied with 0 V or is connected to ground, the LNA runs in self bias mode at a typical current of 80 mA.
24	VDD_LNA	LNA Drain Voltage Bias.
	EPAD	Exposed Pad. Must be connected to RF/dc ground.

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

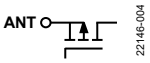

Figure 4. ANT Interface Schematic

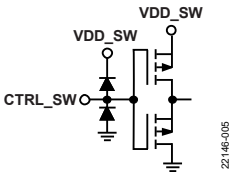

Figure 5. CTRL_SW and VDD_SW Interface Schematic

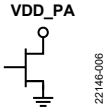

Figure 6. VDD_PA Interface Schematic

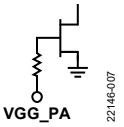

Figure 7. VGG_PA Interface Schematic

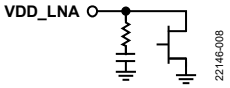

Figure 8. VDD_LNA Interface Schematic

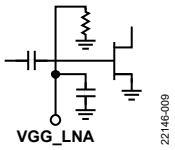

Figure 9. VGG_LNA Interface Schematic

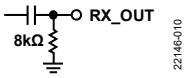

Figure 10. RX_OUT Interface Schematic

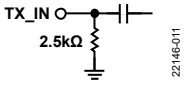

Figure 11. TX_IN Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

TRANSMIT STATE

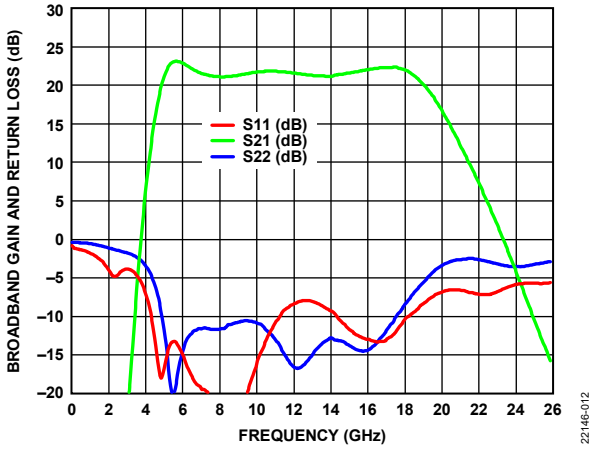

Figure 12. Broadband Gain and Return Loss vs. Frequency, 10 MHz to 26 GHz, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

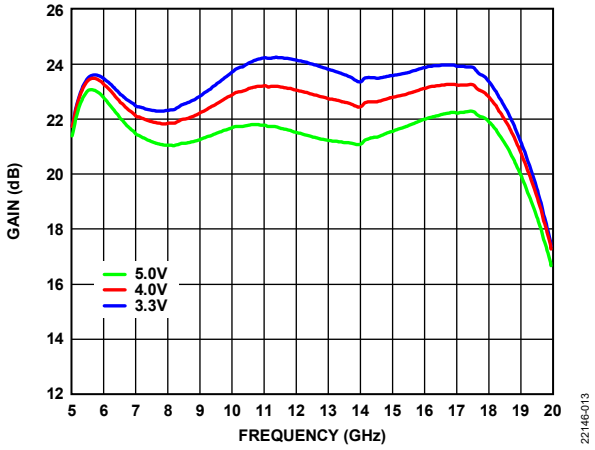

Figure 13. Gain vs. Frequency for Various VDD_PA, Transmit State, Path = TX_IN to ANT, I_{DQ}_PA = 220 mA, Receive State Off

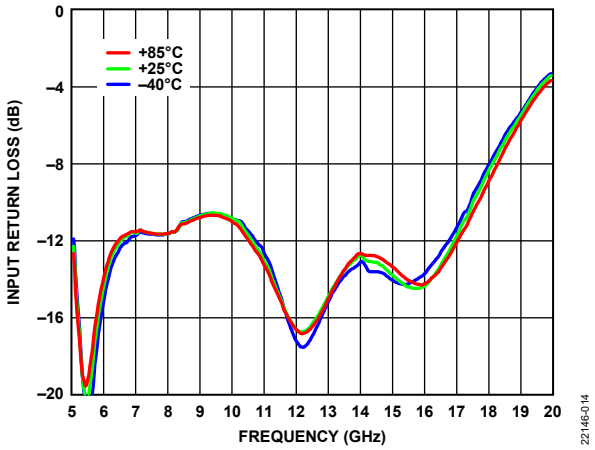

Figure 14. Input Return Loss vs. Frequency for Various Temperatures, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

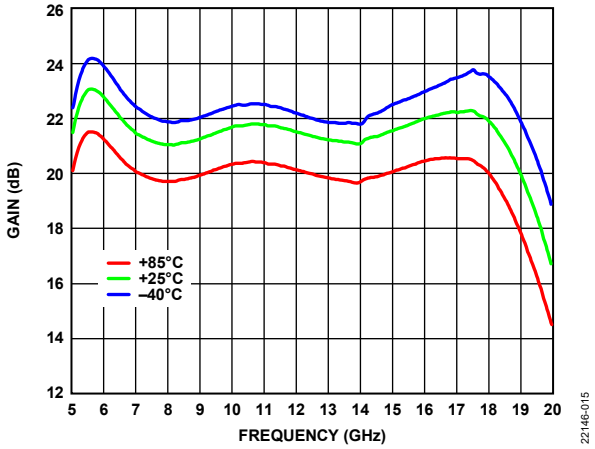

Figure 15. Gain vs. Frequency for Various Temperatures, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

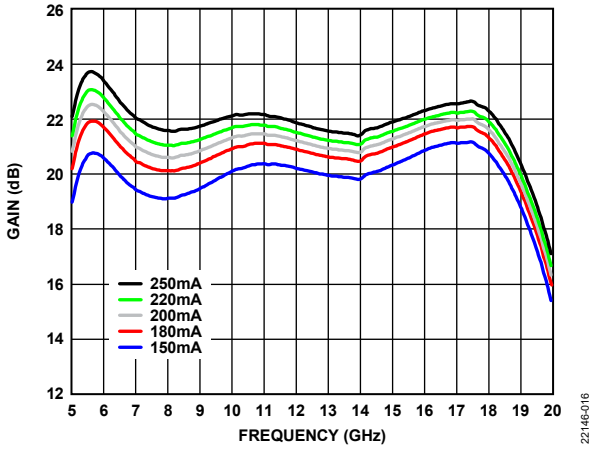

Figure 16. Gain vs. Frequency for Various I_{DQ}_PA, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, Receive State Off

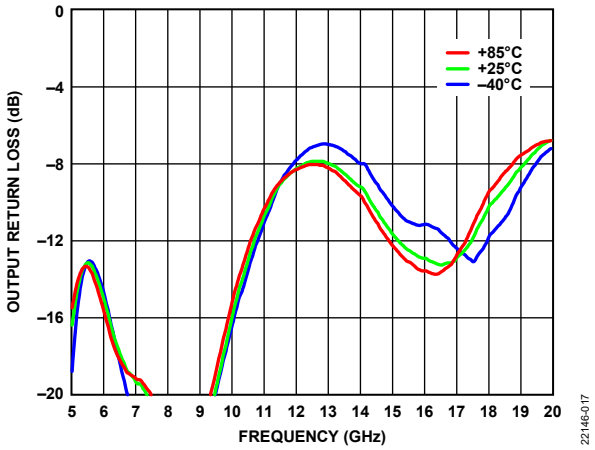

Figure 17. Output Return Loss vs. Frequency for Various Temperatures, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

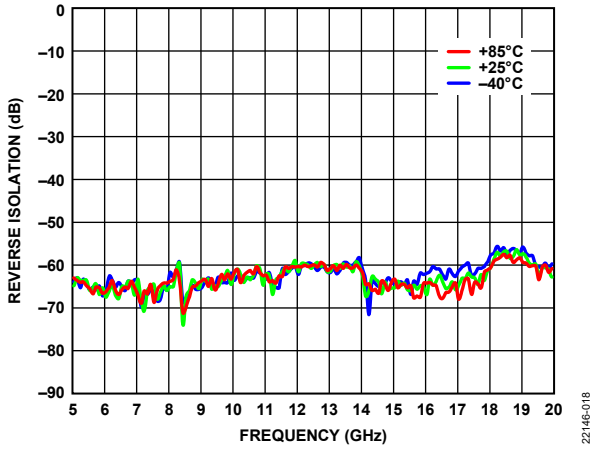

Figure 18. Reverse Isolation vs. Frequency for Various Temperatures,Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

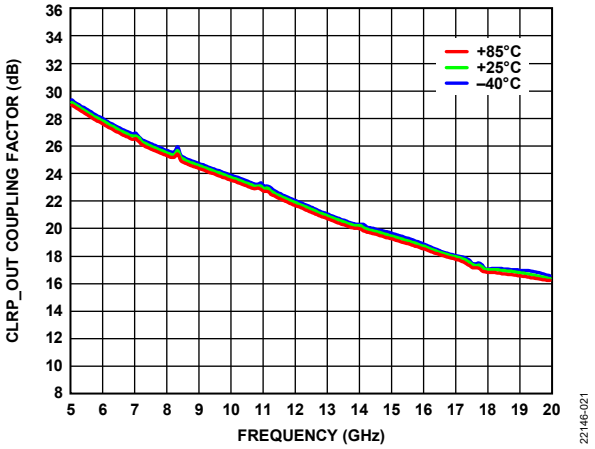

Figure 21. CLPR_OUT Coupling Factor vs. Frequency for Various Temperatures, Transmit State, Coupling Factor = ANT P_{OUT} – CPLR_OUT P_{OUT}, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

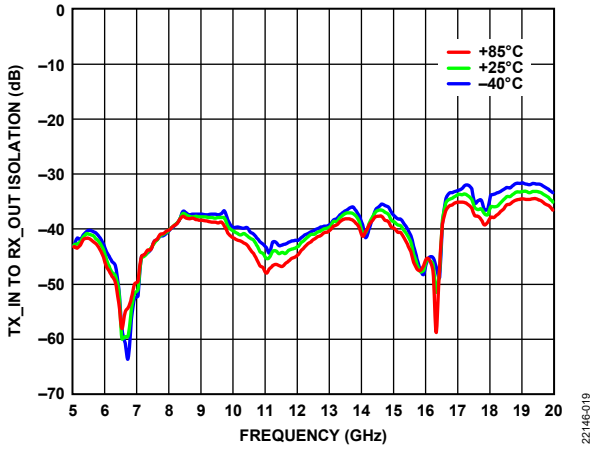

Figure 19. TX_IN to RX_OUT Isolation vs. Frequency for Various Temperatures, Transmit State, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

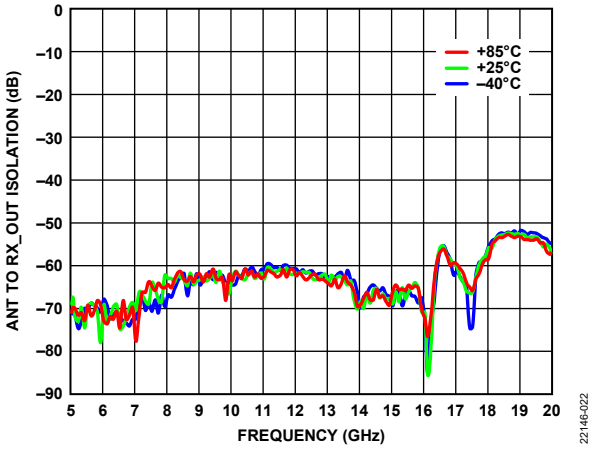

Figure 22. ANT to RX_OUT Isolation vs. Frequency for Various Temperatures, Transmit State, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

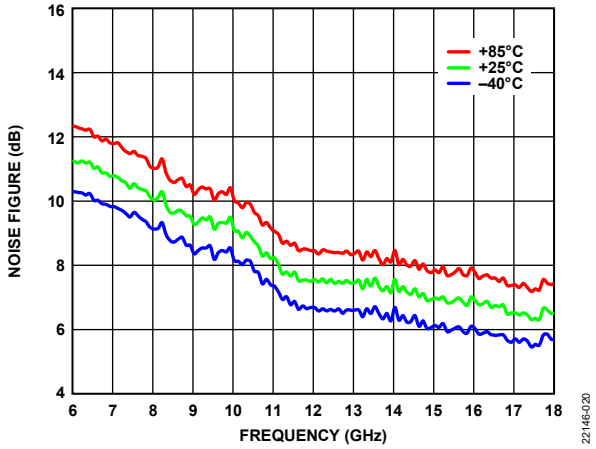

Figure 20. Noise Figure vs. Frequency for Various Temperatures, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

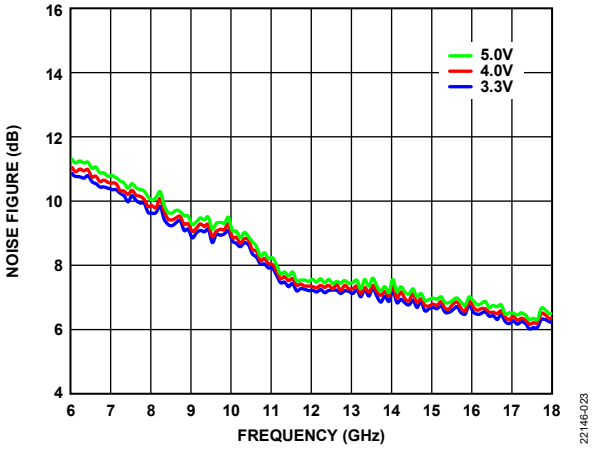

Figure 23. Noise Figure vs. Frequency for Various VDD_PA, Transmit State, Path = TX_IN to ANT, I_{DQ}_PA = 220 mA, Receive State Off

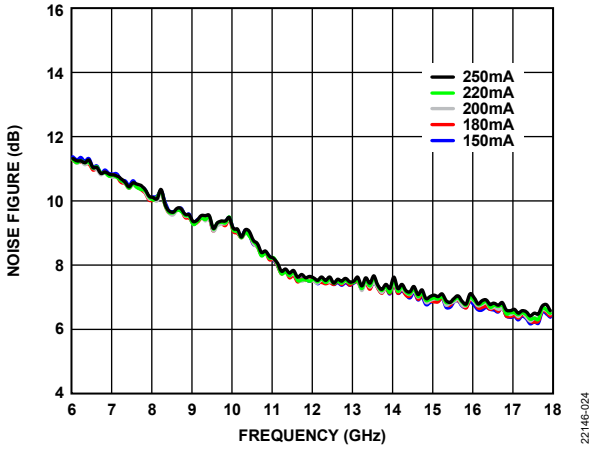

Figure 24. Noise Figure vs. Frequency for Various I_{DQ}_PA, Transmit State , Path = TX_IN to ANT, VDD_PA = 5 V, Receive State Off

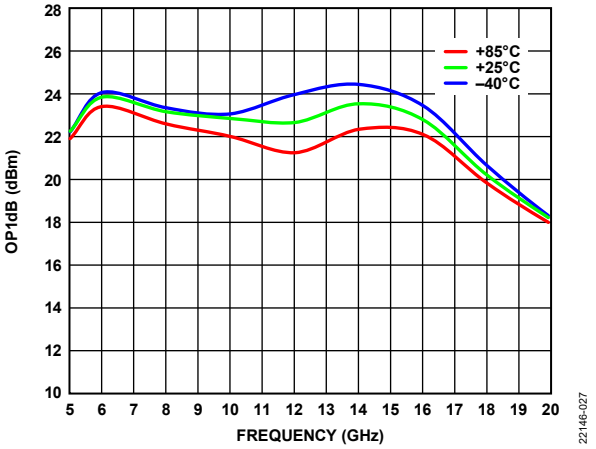

Figure 27. OP1dB vs. Frequency for Various Temperatures,Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

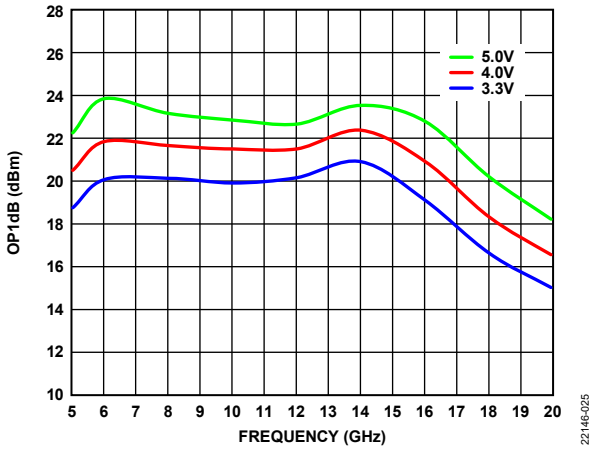

Figure 25. OP1dB vs. Frequency for Various VDD_PA, Transmit State, Path = TX_IN to ANT, I_{DQ}_PA = 220 mA, Receive State Off

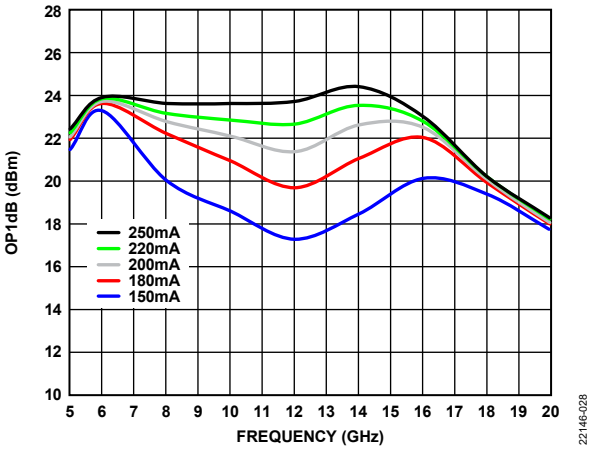

Figure 28. OP1dB vs. Frequency for Various I_{DQ}_PA, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, Receive State Off

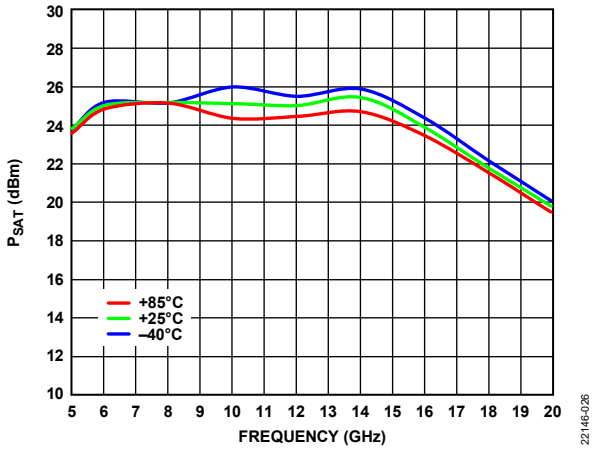

Figure 26. P_{SAT} vs. Frequency for Various Temperatures, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

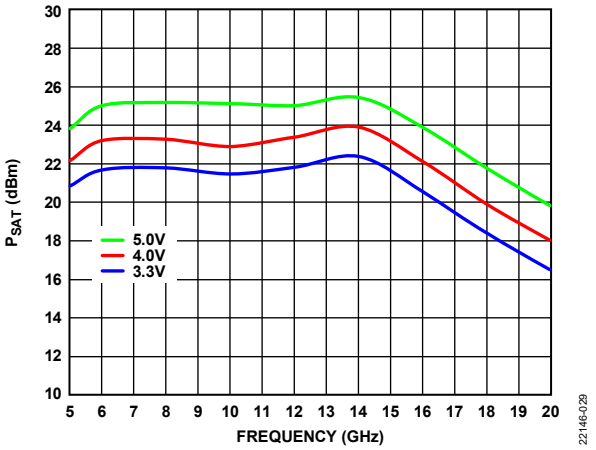

Figure 29. P_{SAT} vs. Frequency for Various VDD_PA, Transmit State, Path = TX_IN to ANT, I_{DQ}_PA = 220 mA, Receive State Off

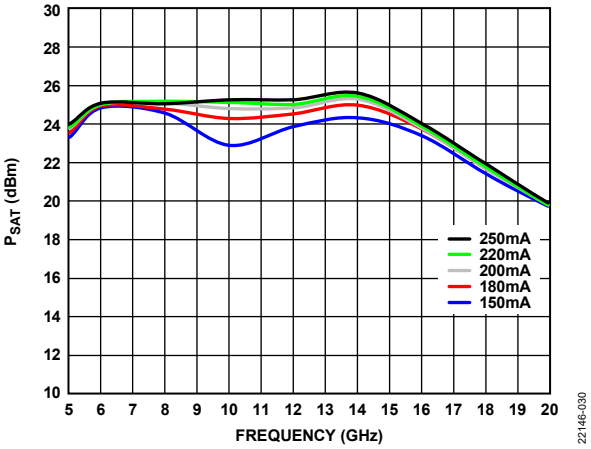

Figure 30. P_{SAT} vs. Frequency for Various I_{DQ}_PA,Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, Receive State Off

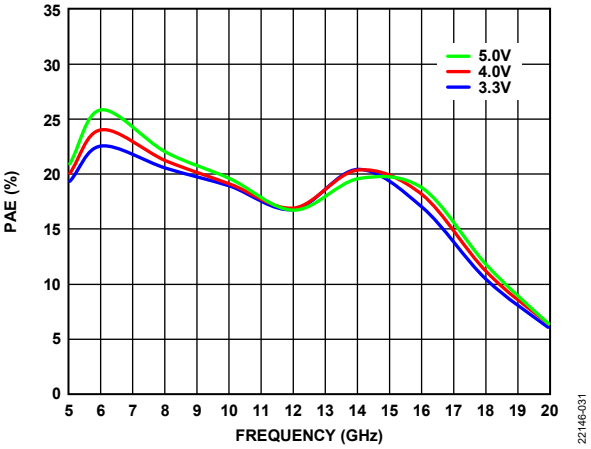

Figure 31. Power Added Efficiency (PAE) vs. Frequency for Various VDD_PA, Transmit State, Path = TX_IN to ANT, I_{DQ}_PA = 220 mA, Receive State Off, PAE Measured at P_{SAT}

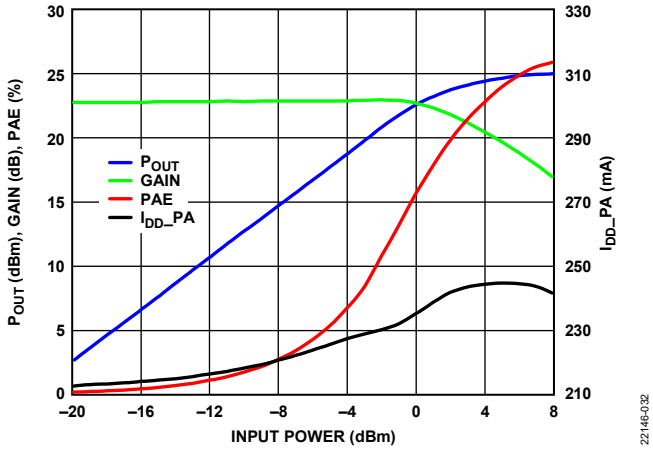

Figure 32. P_{OUT}, Gain, PAE and Power Amplifier Supply Current (I_{DD}_PA) vs. Input Power, 6 GHz, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

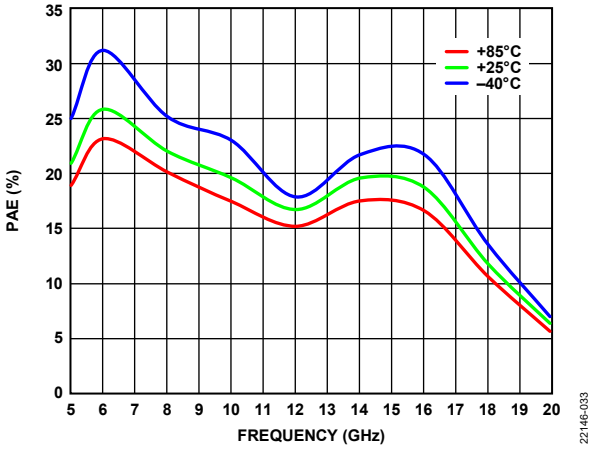

Figure 33. PAE vs. Frequency for Various Temperatures, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off, PAE Measured at P_{SAT}

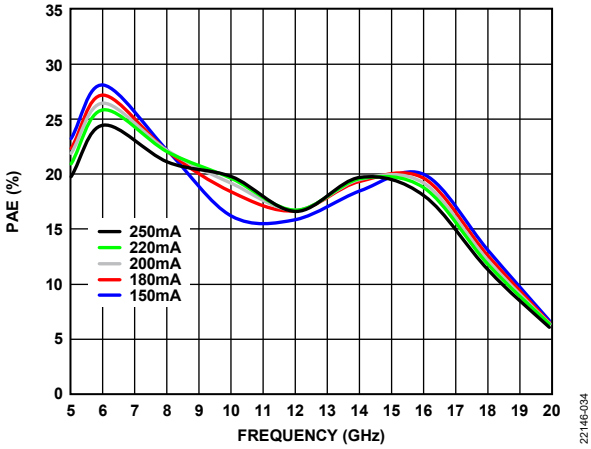

Figure 34. PAE vs. Frequency for Various I_{DQ}_PA, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, Receive State Off, PAE Measured at P_{SAT}

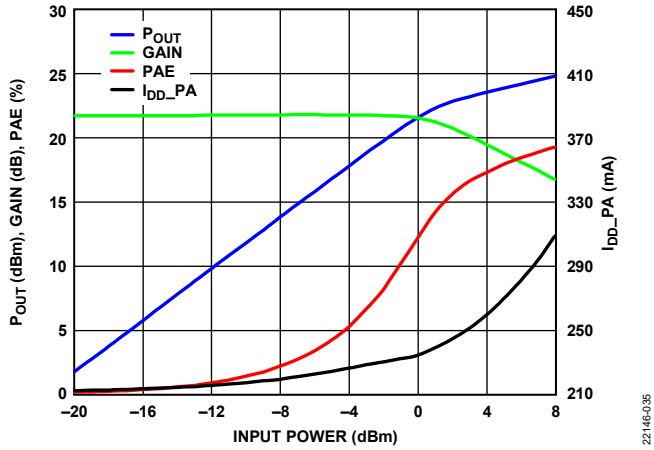

Figure 35. P_{OUT}, Gain, PAE and I_{DD}_PA vs. Input Power, 10 GHz, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

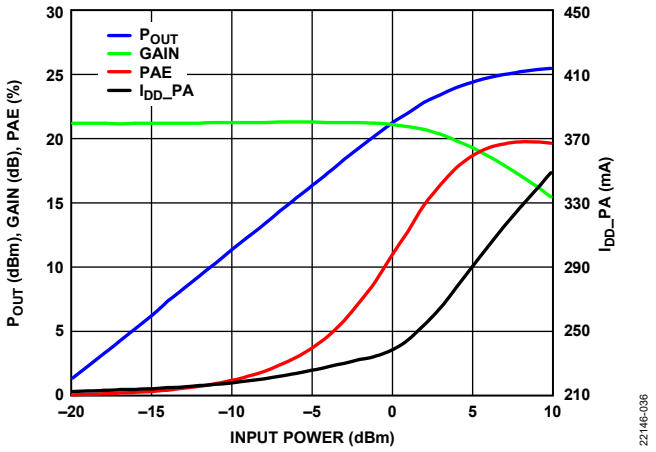

Figure 36. P_{OUT}, Gain, PAE and I_{DD}_PA vs. Input Power, 14 GHz, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

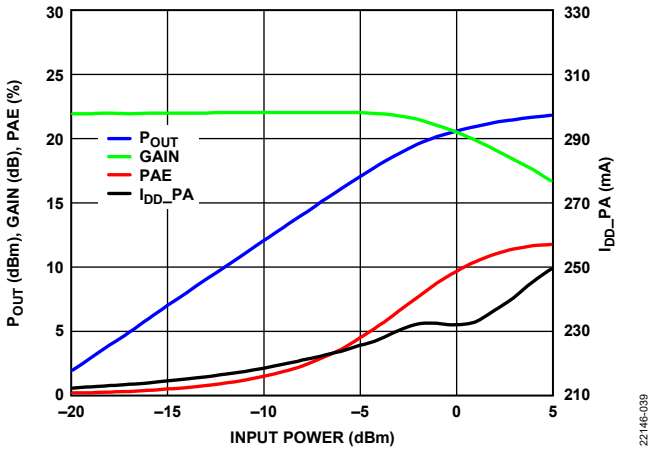

Figure 39. P_{OUT}, Gain, PAE and I_{DD}_PA vs. Input Power, 18 GHz, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

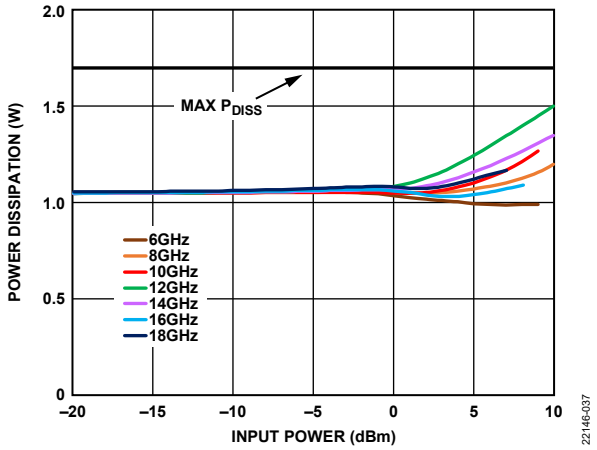

Figure 37. Power Dissipation vs. Input Power at T_A = 85°C, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

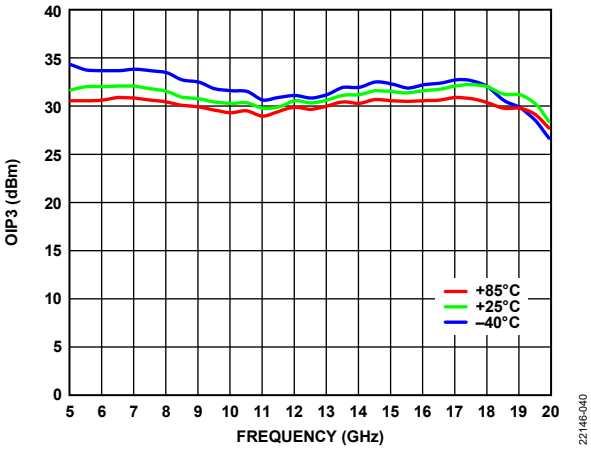

Figure 40. OIP3 vs. Frequency for Various Temperatures, P_{OUT}/Tone = 8 dBm, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

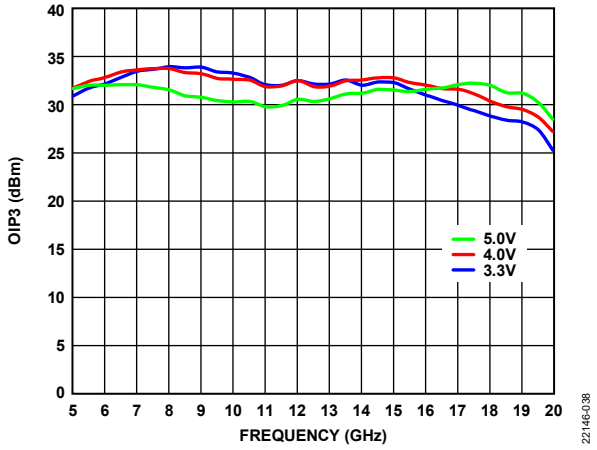

Figure 38. OIP3 vs. Frequency for Various VDD_PA, P_{OUT}/Tone = 8 dBm, Transmit State, Path = TX_IN to ANT, I_{DQ}_PA = 220 mA, Receive State Off

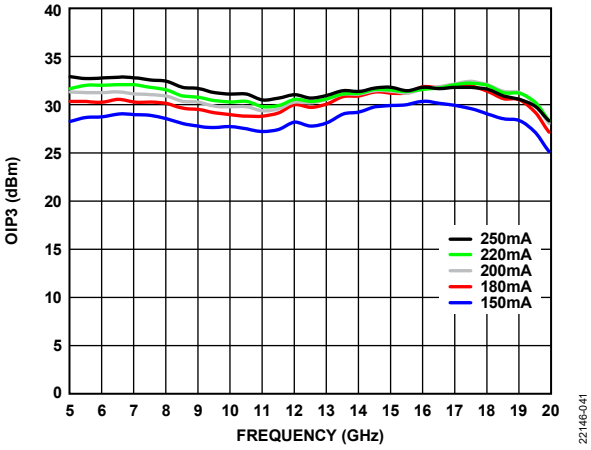

Figure 41. OIP3 vs. Frequency for Various I_{DQ}_PA, P_{OUT}/Tone = 8 dBm, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, Receive State Off

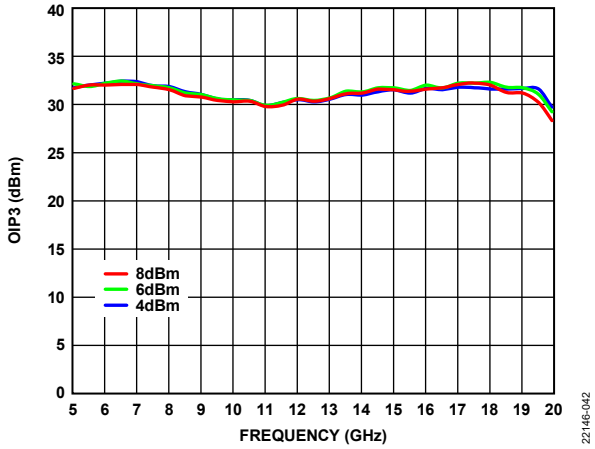

Figure 42. OIP3 vs. Frequency for Various P_{OUT}/Tone, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

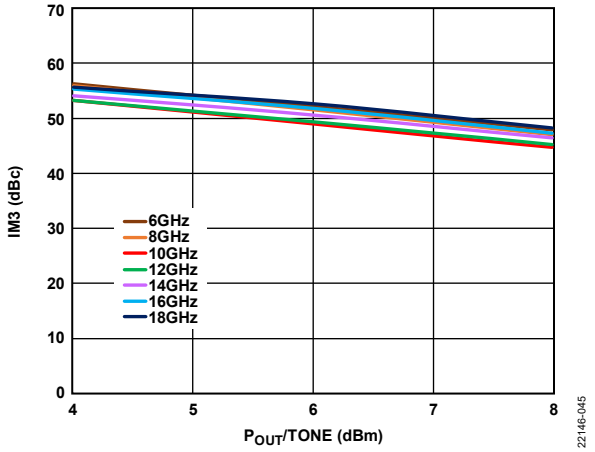

Figure 45. Third-Order Intermodulation Distortion Relative to Carrier (IM3) vs. P_{OUT}/Tone, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

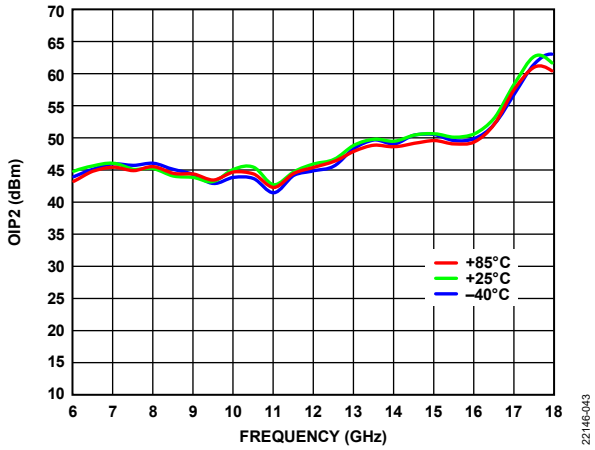

Figure 43. Output Second-Order Intercept (OIP2) vs. Frequency for Various Temperatures, P_{OUT}/Tone = 8 dBm, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

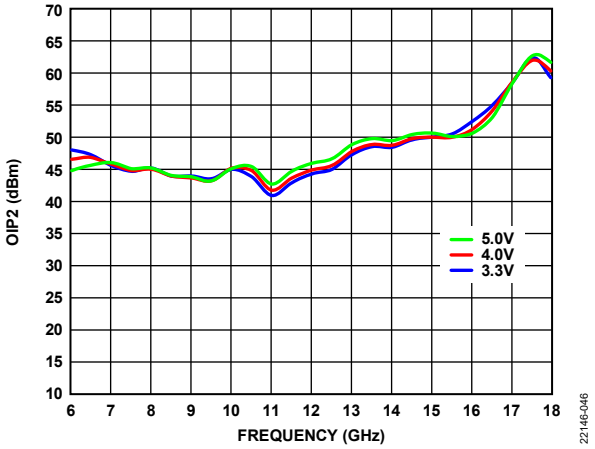

Figure 46. OIP2 vs. Frequency for Various VDD_PA, P_{OUT}/Tone = 8 dBm, Transmit State, Path = TX_IN to ANT, I_{DQ}_PA = 220 mA, Receive State Off

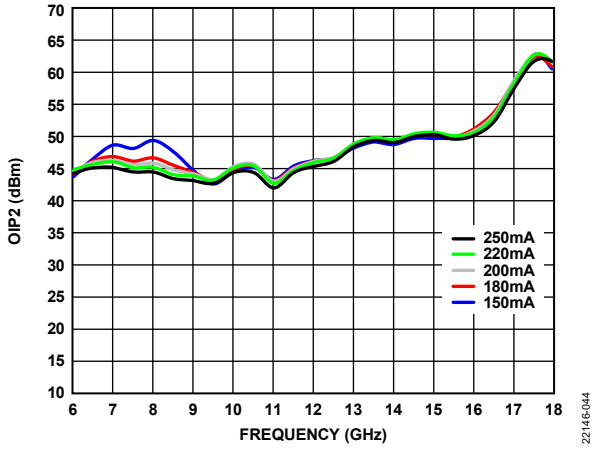

Figure 44. OIP2 vs. Frequency for Various I_{DQ}_PA, P_{OUT}/Tone = 8 dBm, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, Receive State Off

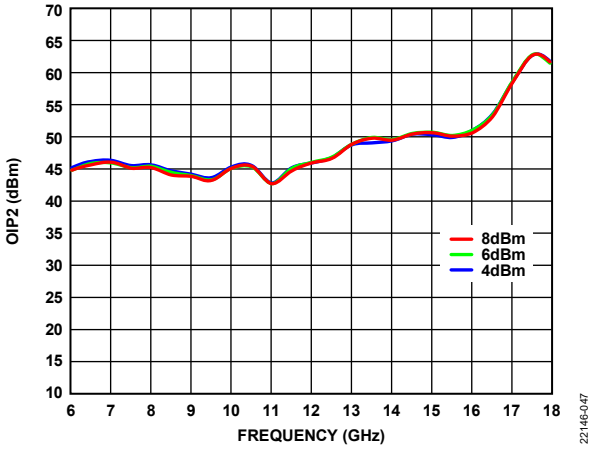

Figure 47. OIP2 vs. Frequency for Various P_{OUT}/Tone, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

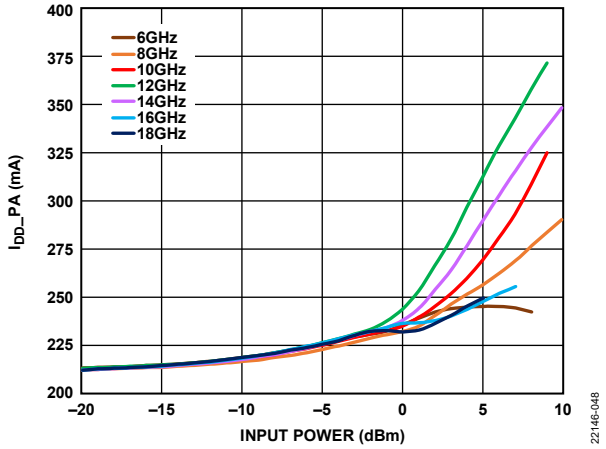

Figure 48. I_{DD}_PA vs. Input Power for Various Frequencies, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

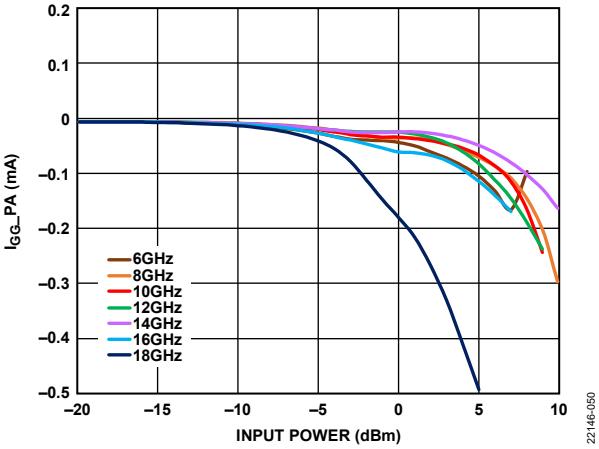

Figure 50. Power Amplifier Gate Current (I_{GG}_PA) vs. Input Power for Various Frequencies, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, I_{DQ}_PA = 220 mA, Receive State Off

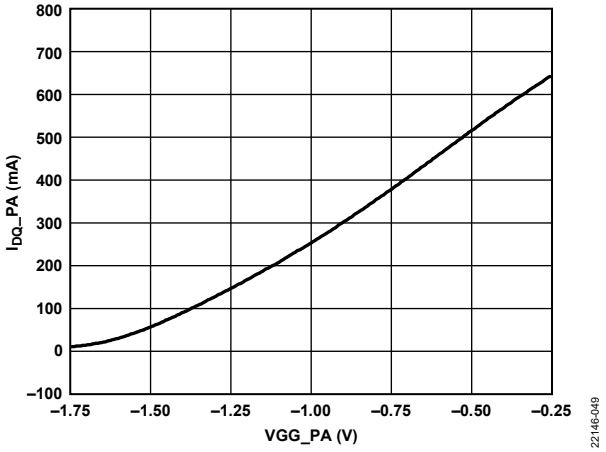

Figure 49. I_{DQ}_PA vs. VGG_PA, VDD_PA = 5 V, Transmit State, Path = TX_IN to ANT, VDD_PA = 5 V, Receive State Off

RECEIVE STATE

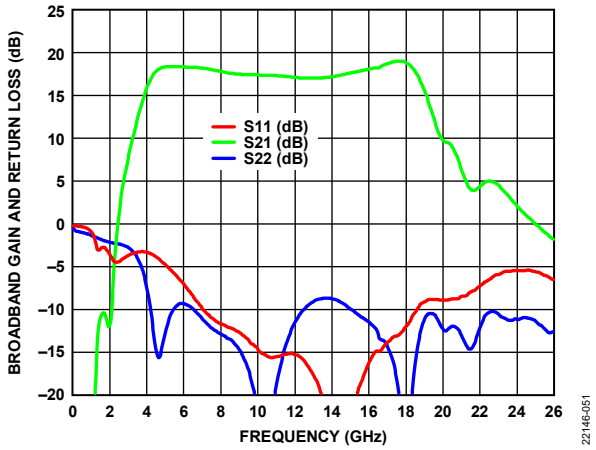

Figure 51. Broadband Gain and Return Loss vs. Frequency, 10 MHz to 26 GHz, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State Off

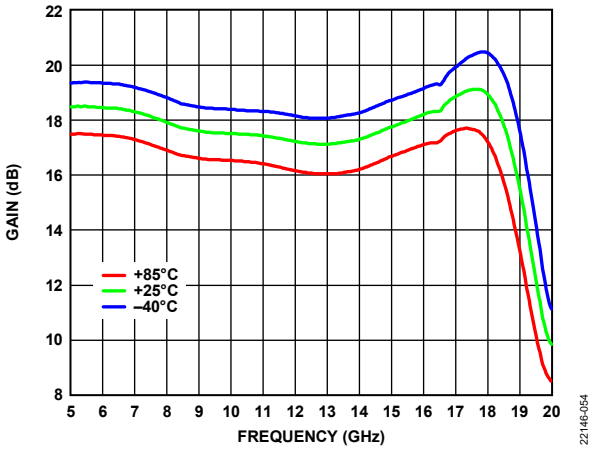

Figure 54. Gain vs. Frequency for Various Temperatures, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State Off

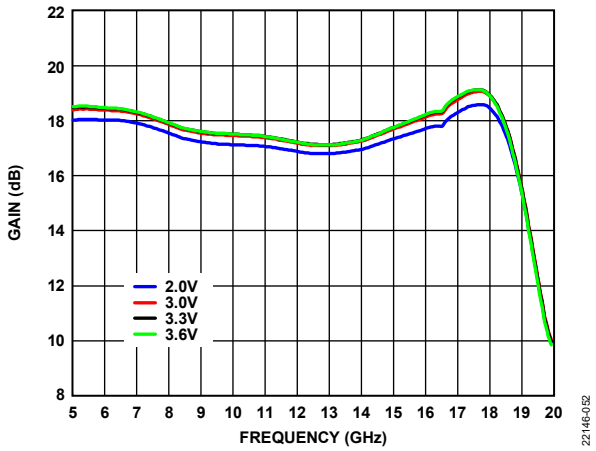

Figure 52. Gain vs. Frequency for Various VDD_LNA, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VGG_LNA = 0 V, Transmit State Off

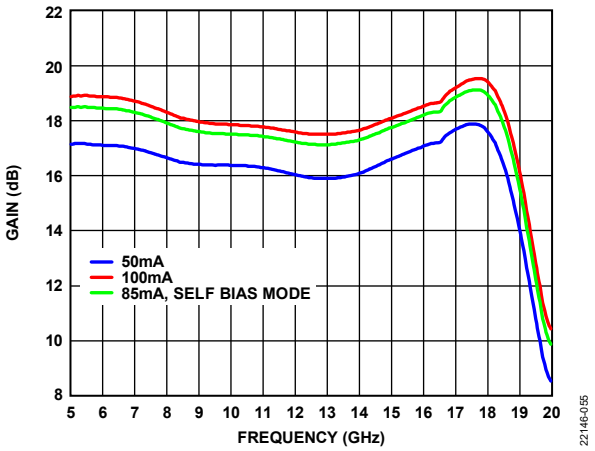

Figure 55. Gain vs. Frequency for Various I_{DQ}_LNA, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, Controlled VGG_LNA, Transmit State Off

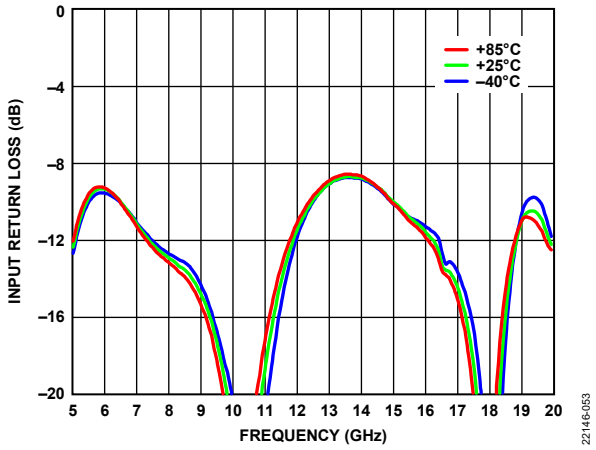

Figure 53. Input Return Loss vs. Frequency for Various Temperatures, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State Off

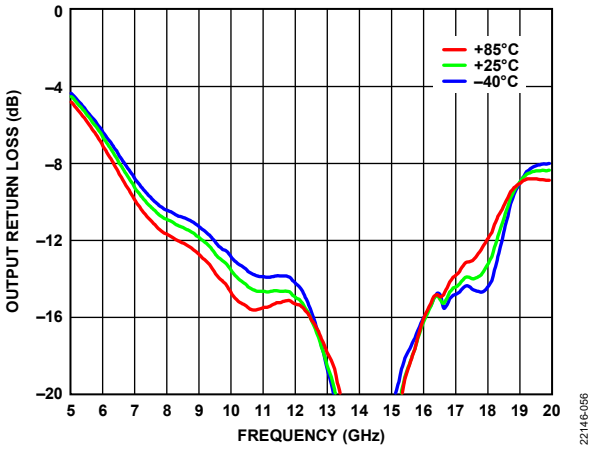

Figure 56. Output Return Loss vs. Frequency for Various Temperatures, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State Off

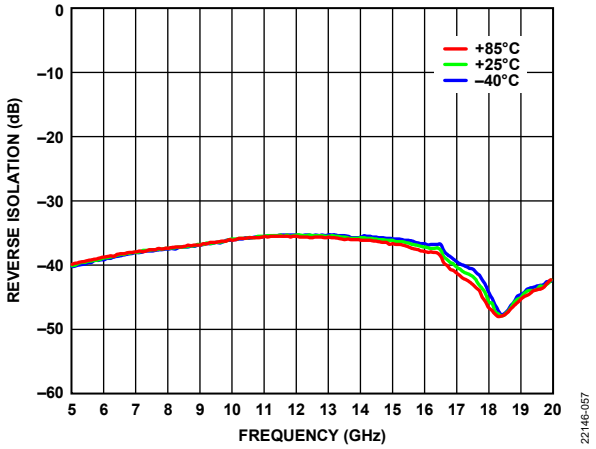

Figure 57. Reverse Isolation vs. Frequency for Various Temperatures, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State Off

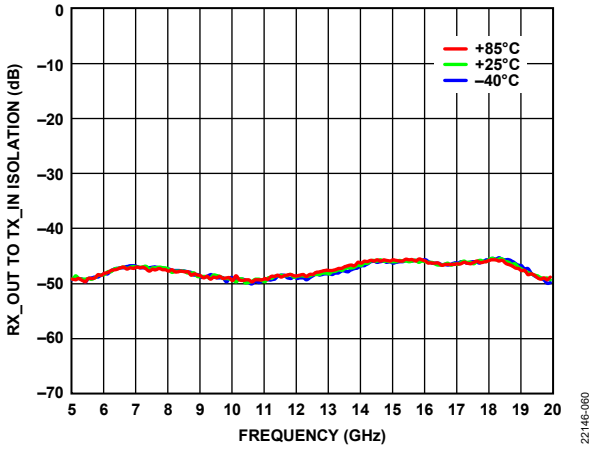

Figure 60. RX_OUT to TX_IN Isolation vs. Frequency for Various Temperatures, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State Off

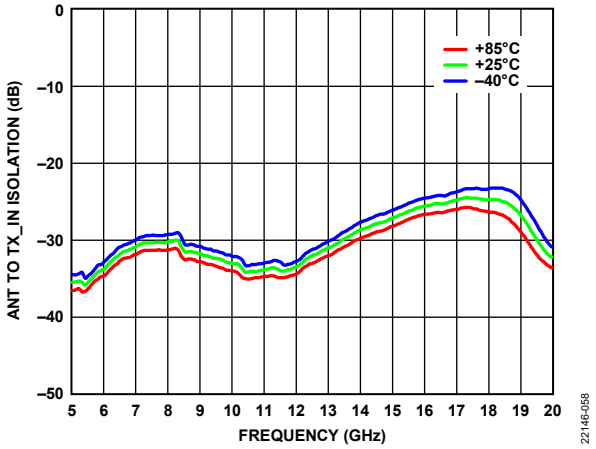

Figure 58. ANT to TX_IN Isolation vs. Frequency for Various Temperatures, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State Off

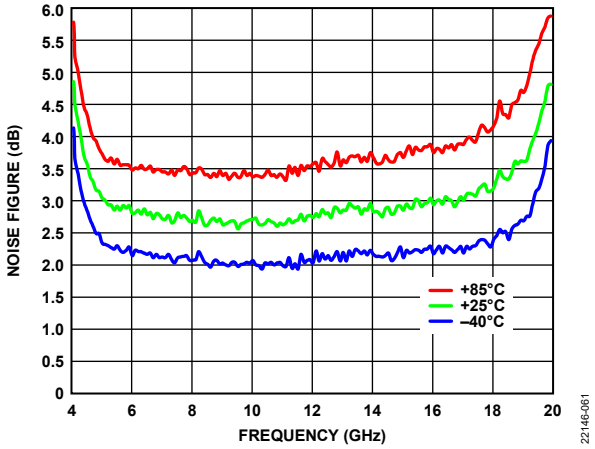

Figure 61. Noise Figure vs. Frequency for Various Temperatures, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State Off

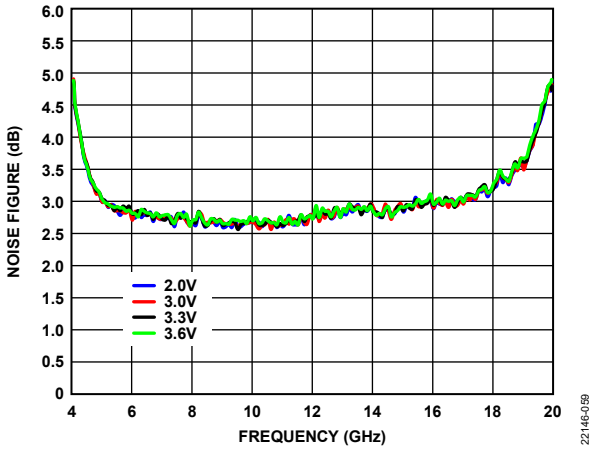

Figure 59. Noise Figure vs. Frequency for Various VDD_LNA, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VGG_LNA = 0 V, Transmit State Off

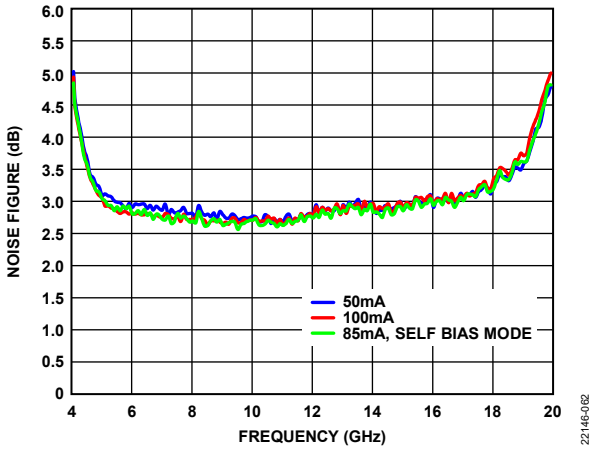

Figure 62. Noise Figure vs. Frequency for Various I_{DQ}_LNA, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, Controlled VGG_LNA, Transmit State Off

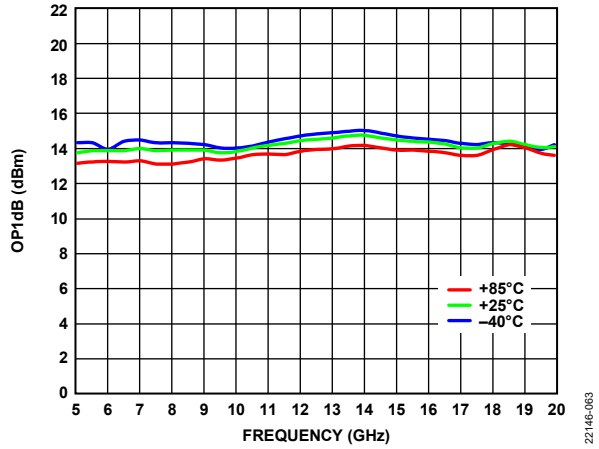

Figure 63. OP1dB vs. Frequency for Various Temperatures, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State Off

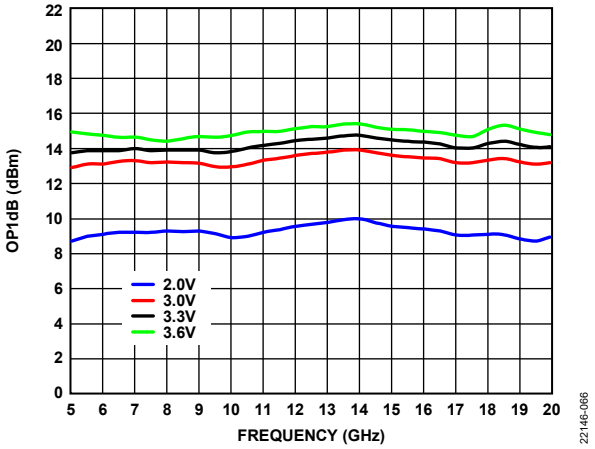

Figure 66. OP1dB vs. Frequency for Various VDD_LNA, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VGG_LNA = 0 V, Transmit State Off

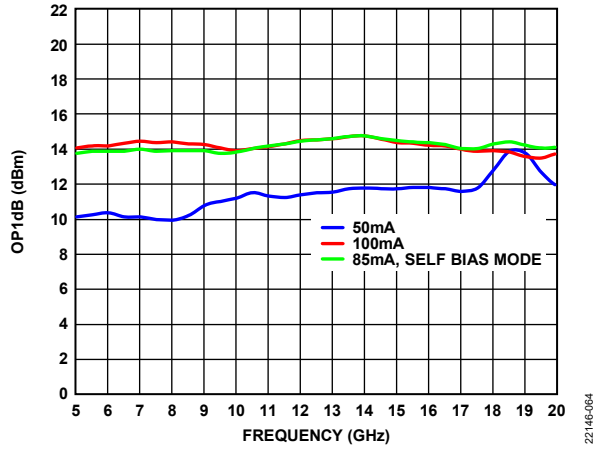

Figure 64. OP1dB vs. Frequency for Various I_{DQ}_LNA, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, Controlled VGG_LNA, Transmit State Off

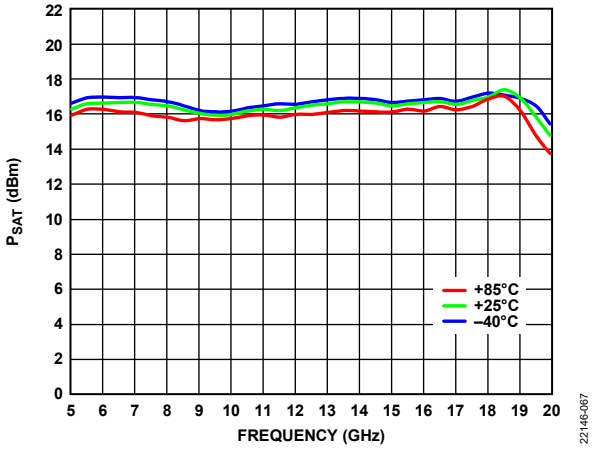

Figure 67. P_{SAT} vs. Frequency for Various Temperatures, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State = Off

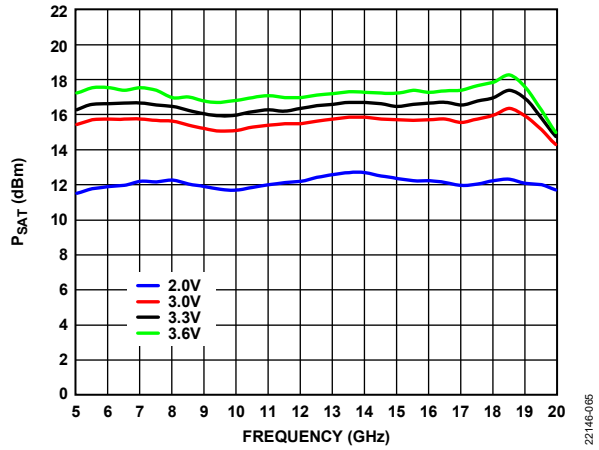

Figure 65. P_{SAT} vs. Frequency for Various VDD_LNA, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VGG_LNA = 0 V, Transmit State Off

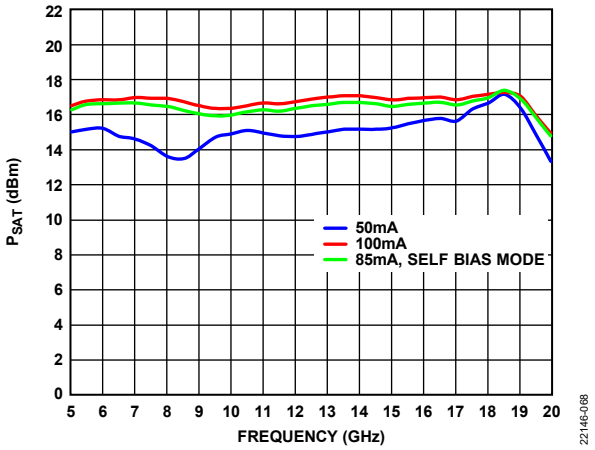

Figure 68. P_{SAT} vs. Frequency for Various I_{DQ}_LNA, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, Controlled VGG_LNA, Transmit State Off

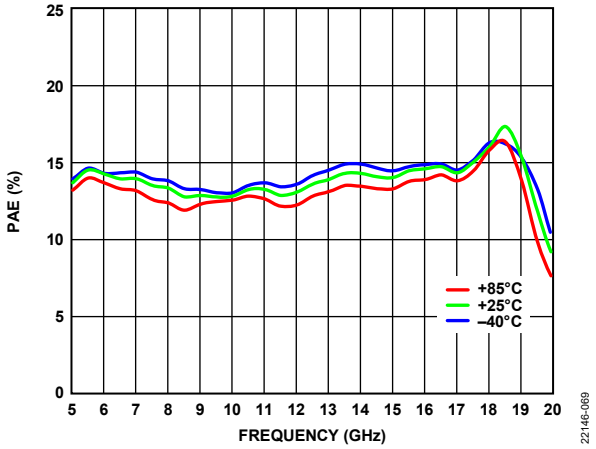

Figure 69. PAE vs. Frequency for Various Temperatures, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State Off, PAE Measured at P_{SAT}

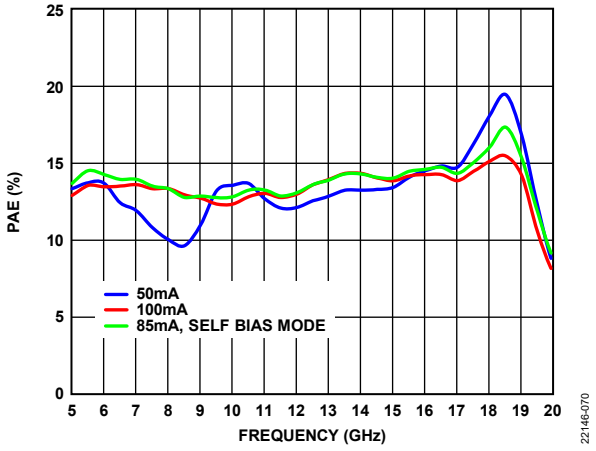

Figure 70. PAE vs. Frequency for Various I_{DQ}_LNA, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, Controlled VGG_LNA, Transmit State Off, PAE Measured at P_{SAT}

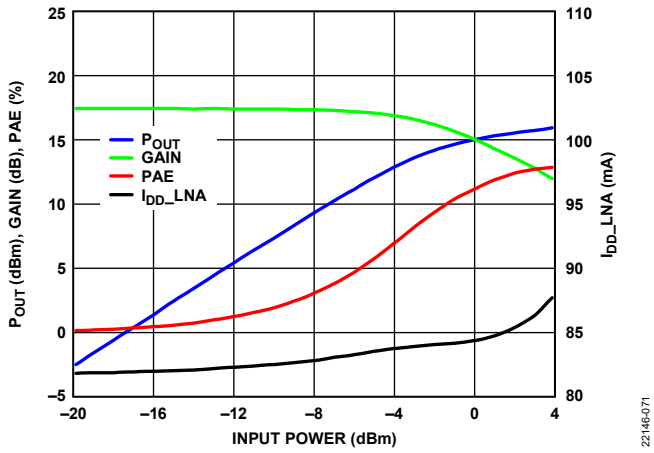

Figure 71. P_{OUT}, Gain, PAE and I_{DD}_LNA vs. Input Power, 10 GHz, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA= 0 V, Transmit State Off

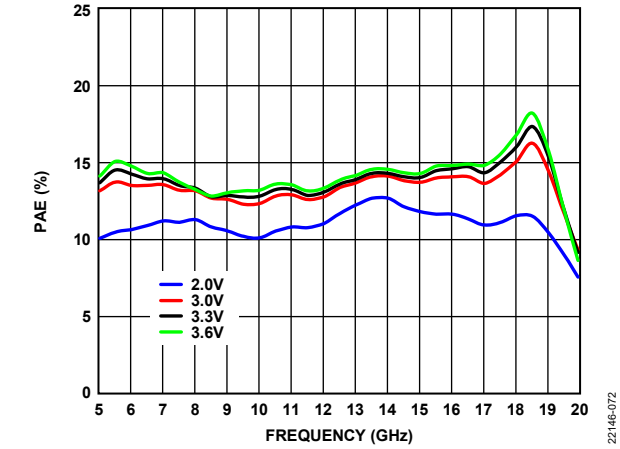

Figure 72. PAE vs. Frequency for Various VDD_LNA, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VGG_LNA = 0 V, Transmit State Off, PAE Measured at P_{SAT}

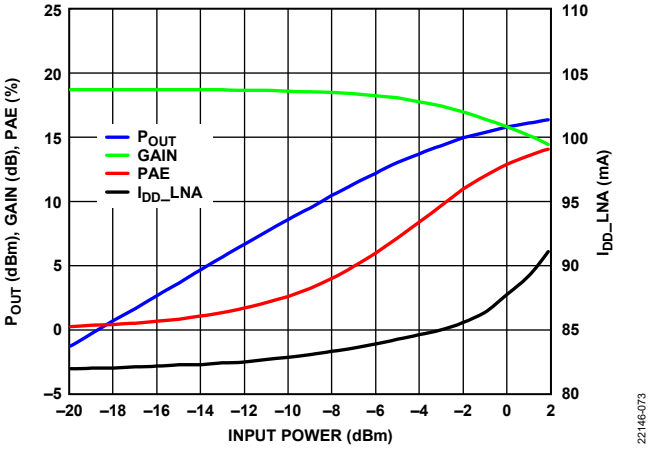

Figure 73. P_{OUT}, Gain, PAE and I_{DD}_LNA vs. Input Power, 6 GHz, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA= 0 V, Transmit State Off

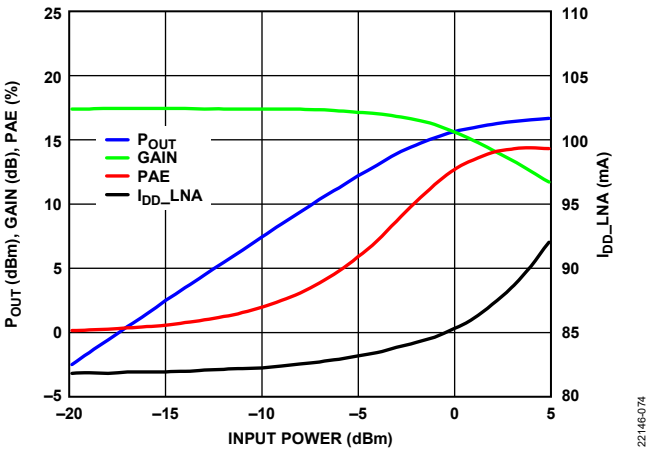

Figure 74. P_{OUT}, Gain, PAE and I_{DD}_LNA vs. Input Power, 14 GHz, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA= 0 V, Transmit State Off

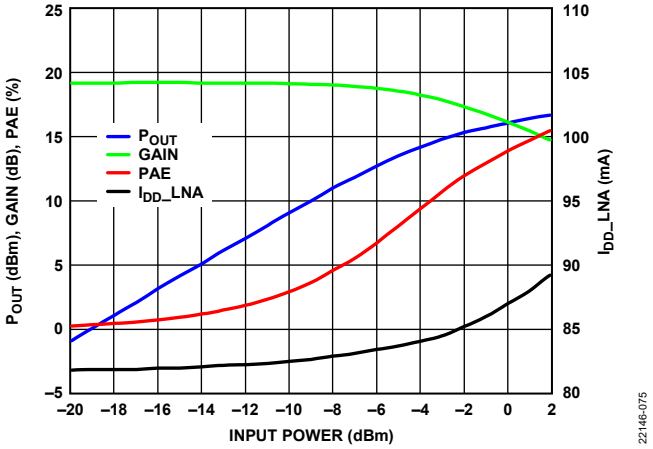

Figure 75. P_{OUT}, Gain, PAE and I_{DD}_LNA vs. Input Power, 18 GHz, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State Off

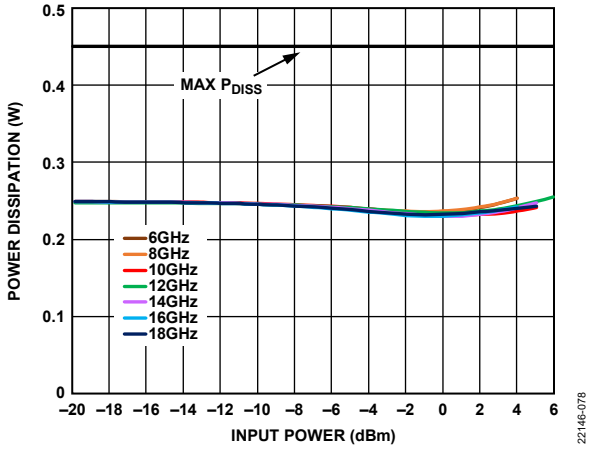

Figure 78. Power Dissipation vs. Input Power at T_A = 85°C, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State Off

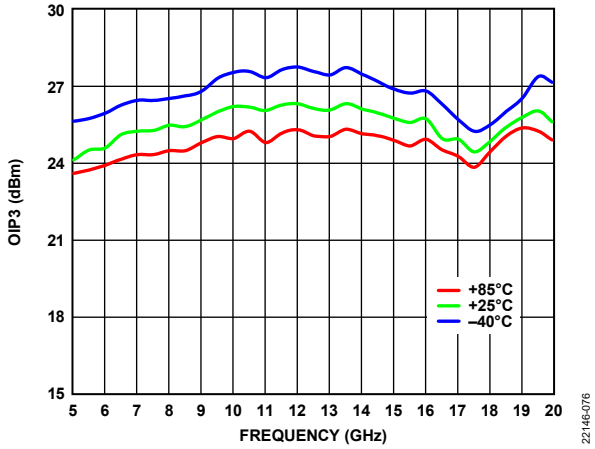

Figure 76. OIP3 vs. Frequency for Various Temperatures, P_{OUT}/Tone = 0 dBm, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State Off

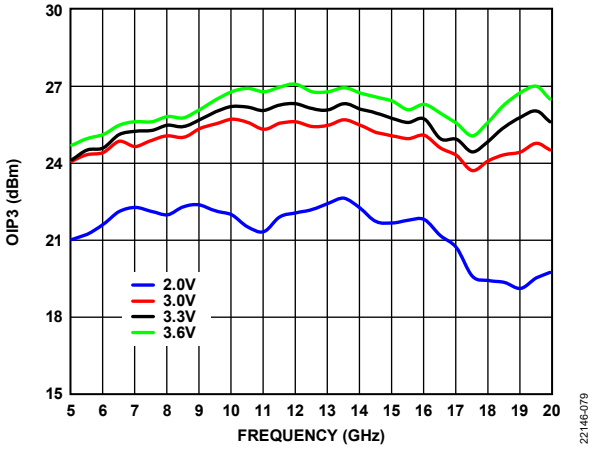

Figure 79. OIP3 vs. Frequency for Various VDD_LNA, P_{OUT}/Tone = 0 dBm, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VGG_LNA = 0 V, Transmit State Off

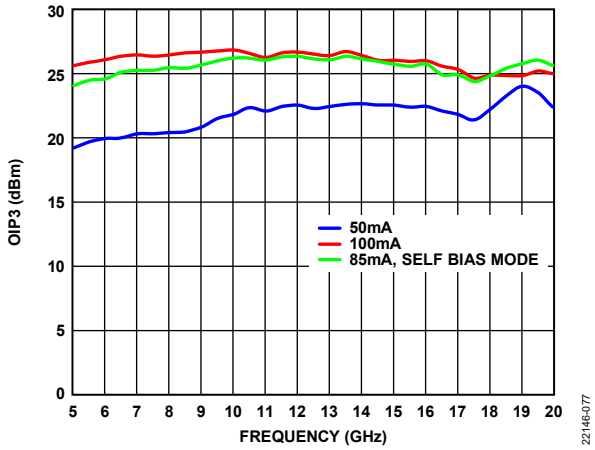

Figure 77. OIP3 vs. Frequency for Various I_{DQ}_LNA, P_{OUT}/Tone = 0 dBm, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, Controlled VGG_LNA, Transmit State Off

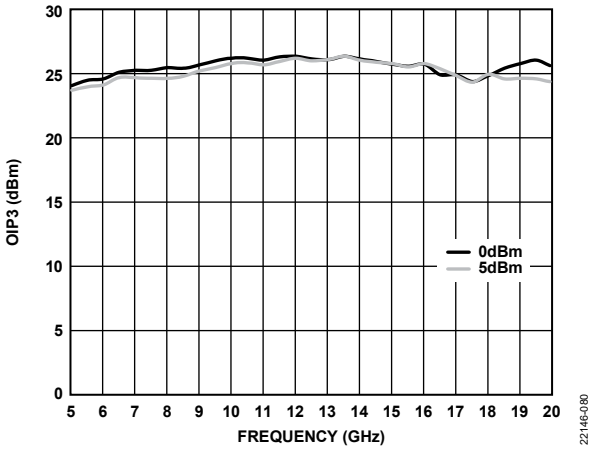

Figure 80. OIP3 vs. Frequency for Various P_{OUT}/Tone, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State Off

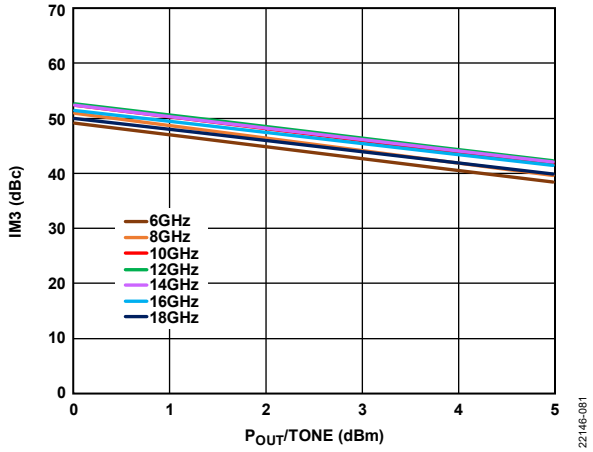

Figure 81. IM3 vs. P_{OUT}/Tone, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State Off

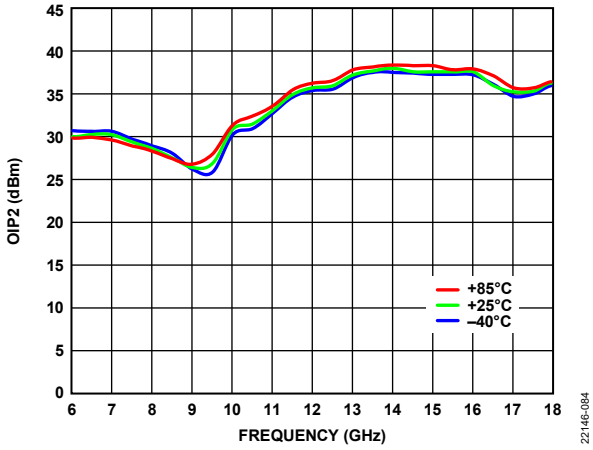

Figure 84. OIP2 vs. Frequency for Various Temperatures, P_{OUT}/Tone = 0 dBm, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State Off

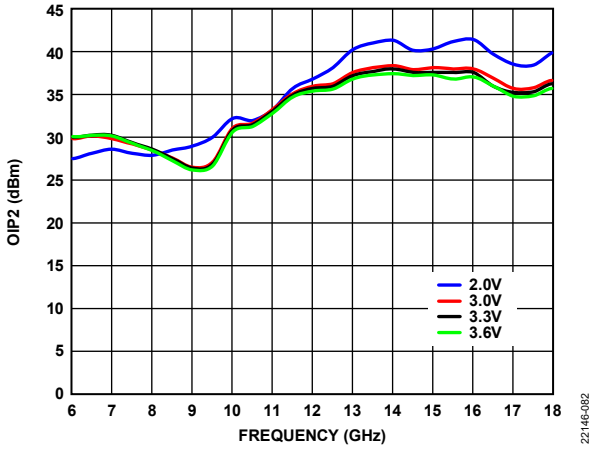

Figure 82. OIP2 vs. Frequency for Various VDD_LNA, P_{OUT}/Tone = 0 dBm, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VGG_LNA = 0 V, Transmit State Off

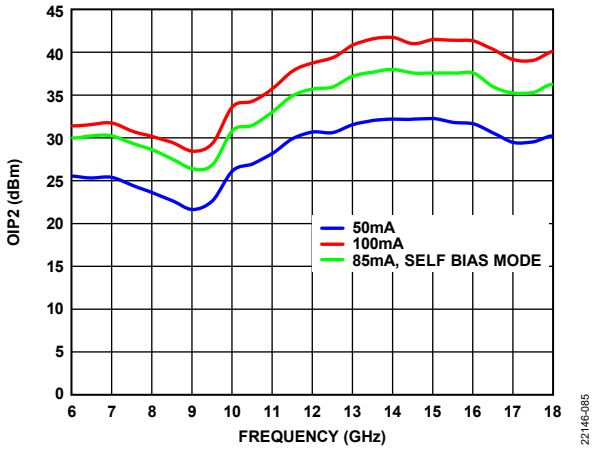

Figure 85. OIP2 vs. Frequency for Various I_{DQ}_LNA, P_{OUT}/Tone = 0 dBm, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, Controlled VGG_LNA, Transmit State Off

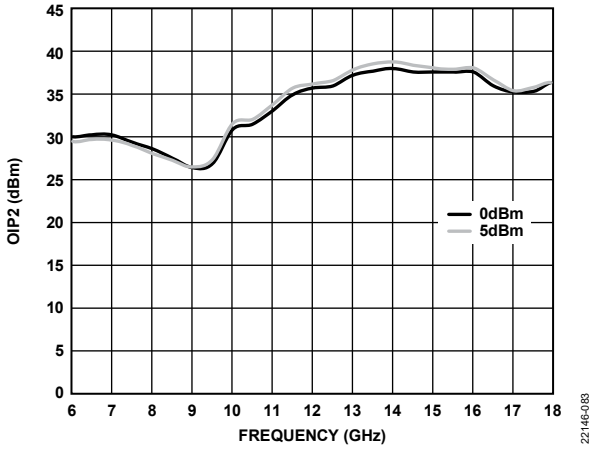

Figure 83. OIP2 vs. Frequency for Various P_{OUT}/Tone, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State Off

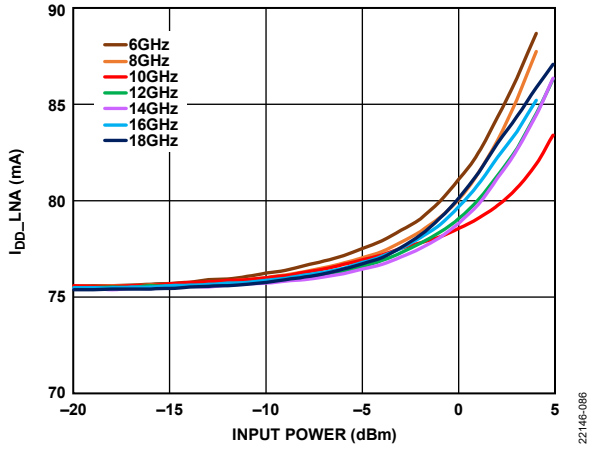

Figure 86. I_{DD}_LNA vs. Input Power for Various Frequencies, Receive State, Path = ANT to RX_OUT, Self Biased Mode, VDD_LNA = 3.3 V, VGG_LNA = 0 V, Transmit State Off

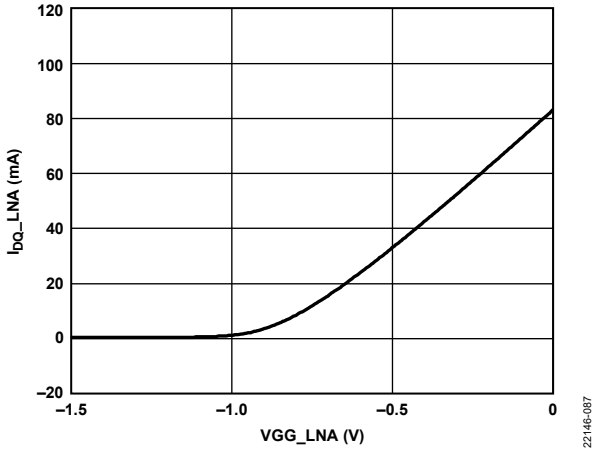

Figure 87. I_{DQ}_LNA vs. VGG_LNA, VDD_LNA = 3.3 V, Controlled VGG_LNA, Receive State, Path = ANT to RX_OUT, Transmit State Off

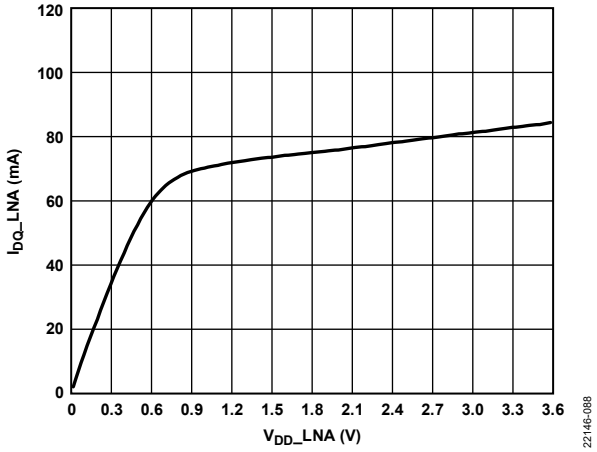

Figure 88. I_{DQ}_LNA vs. V_{DD}_LNA, Self Biased Mode, VGG_LNA = 0 V, Receive State, Path = ANT to RX_OUT, Transmit State Off

THEORY OF OPERATION

The ADTR1107 is a multichip transmit/receive module that consists of an LNA, a medium power amplifier, and a silicon SPDT reflective switch. The ANT antenna port is dc-coupled to 0 V and no dc block is required at this port when the RF line potential is equal to 0 V. The switch has an integrated driver to perform logic functions internally and provides a simplified complementary metal-oxide semiconductor (CMOS)/low voltage transistor to transistor logic (LVTTL)-compatible control interface. The driver features a single digital control input pin, CTRL_SW. The logic level applied to CTRL_SW determines whether the ADTR1107 is in transmit state or receive state (see Table 8).

The receive path contains a self biased LNA with optional bias control using the VGG_LNA pin for bias adjustment. For self biased operation, the VGG_LNA pin is set to 0 V or connected to ground. The receive path output (RX_OUT) is dc-coupled to ground through an 8 kΩ resistor. No dc block is required at this port when the RF line potential is equal to 0 V.

The transmit path contains a power amplifier. The bias current is set using VGG_PA. The transmit path input (TX_IN) is dc-coupled to ground through a 2.5 kΩ resistor. No dc block is required at this port when the RF line potential is equal to 0 V. A directional coupler is incorporated into the ADTR1107 to allow for monitoring of the transmit power level.

APPLICATIONS INFORMATION

The basic connections for operating the ADTR1107 are shown in Figure 89. The power amplifier on the transmit path is biased with +5 V on the VDD_PA pin and a voltage from −1.75 V to −0.25 V is applied to the VGG_PA pin to achieve 220 mA quiescent current.

The LNA on the receive path operates as either self biased or external biased mode. For self biased mode, apply 3.3 V to the VDD_LNA pin and leave the VGG_LNA pin supplied with 0 V or connected to ground. For external biased mode, apply +3.3 V to the VDD_LNA pin and adjust the VGG_LNA pin with a voltage range of −1.5 V to 0 V to achieve the desired I_{DQ}_PA.

The SPDT switch is biased with +3.3 V on the VDD_SW pin and −3.3 V on the VSS_SW pin. The CTRL_SW pin sets the path state shown in Table 8. High logic state is set at 3.3 V and low logic state is set at 0 V.

All required decoupling capacitors for the dc power supply lines are internal to the ADTR1107.

RECOMMENDED BIAS SEQUENCING

The recommended bias sequence during transmit state power-up is as follows:

1. Connect all GND pins to ground.
2. Set the VDD_SW pin to 3.3 V.
3. Set the VSS_SW pin to −3.3 V.
4. Set the CTRL_SW pin to 0 V.
5. Set the VGG_LNA pin to 0 V.
6. Set the VDD_LNA pin to 0 V.
7. Set the VGG_PA pin to −1.75 V.
8. Set the VDD_PA pin to 5 V.
9. Increase the VGG_PA voltage to achieve the desired I_{DQ}_PA.
10. Apply the RF signal to the TX_IN pin.

The recommended transmit state bias sequence during power-down is as follows:

1. Turn off the RF signal.
2. Decrease the VGG_PA voltage to −1.75 V.
3. Set the VDD_PA pin to 0 V.
4. Set the VSS_SW pin to 0 V.
5. Set the VDD_SW pin to 0 V.

The recommended bias sequence during receive state power-up is as follows:

1. Connect all GND pins to ground.
2. Set the VDD_SW pin to 3.3 V.
3. Set the VSS_SW pin to −3.3 V.
4. Set the CTRL_SW pin to 3.3 V.
5. Set the VGG_PA pin to −1.75 V.
6. Set the VDD_PA pin to 0 V.
7. Set the VGG_LNA pin to 0 V.
8. Set the VDD_LNA pin to 3.3 V.
9. Apply the RF signal to the ANT pin.

The recommended receive state bias sequence during power-down is as follows:

1. Turn off the RF signal.
2. Set the VDD_LNA pin to 0 V.
3. Set the CTRL_SW pin to 0 V.
4. Set the VSS_SW pin to 0 V.
5. Set the VDD_SW pin to 0 V.

All measurements and data shown in this data sheet were taken using the typical application circuit (see Figure 89) and biased per the conditions in this section, unless otherwise noted. The bias conditions described in this section are the operating points recommended to optimize the overall device performance. Operation using other bias conditions can result in performance that differs from what is shown in the Typical Performance Characteristics section. To obtain optimal performance while not damaging the device, follow the recommended biasing sequences described in this section and adhere to the values shown in the Absolute Maximum Ratings section.

TYPICAL APPLICATION CIRCUIT

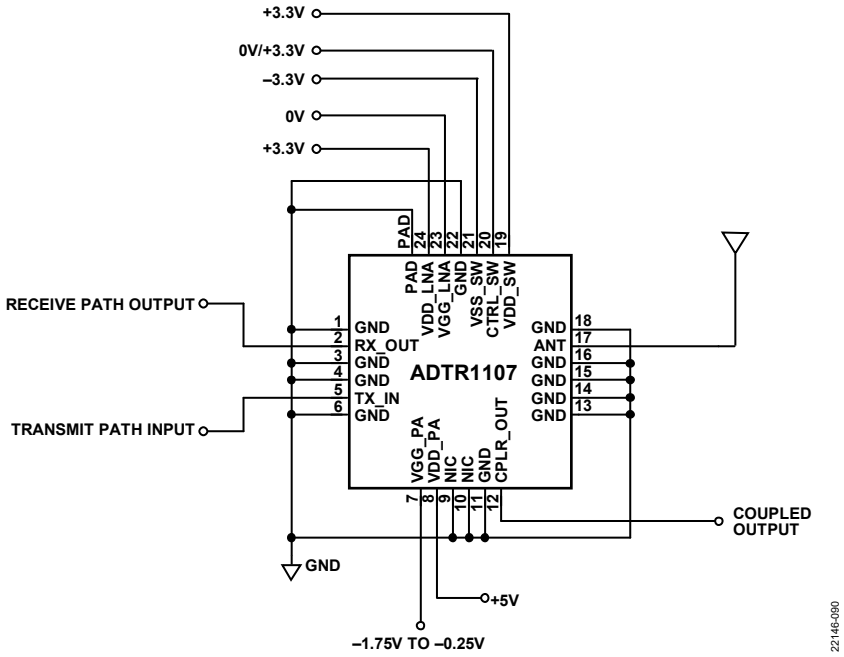

Figure 89. Typical Application Circuit

INTERFACING THE ADTR1107 TO THE ADAR1000 X BAND AND KU BAND BEAMFORMER

ADTR1107 can be interfaced to the ADAR1000 X band and Ku band quad beamformer IC, as shown in Figure 91. Note that only a single channel of the ADAR1000 is shown in Figure 91 and additional components have been omitted for clarity. The ADAR1000 provides multiple bias voltages and control signals, resulting in a glueless interface and no need for any additional control signals to the ADTR1107. The gate voltage for the ADTR1107 power amplifier (VGG_PA) is provided by the ADAR1000 PA_BIAS3 pin. One of four independent negative gate voltages is needed for power amplifier gate biasing. Each voltage is set by an 8-bit digital-to-analog converter (DAC) with an output voltage range of 0 V to −4.8 V. The typical gate voltage required to bias the ADTR1107 power amplifier is −1.1 V (see Figure 49). This voltage can be asserted by the ADAR1000 TR input pin (rising edge enables the power amplifier) or by a serial peripheral interface (SPI) write. Asserting the ADAR1000 TR pin switches the polarity of the ADAR1000 TR_SW_NEG pin and TR_SW_POS pin. The TR_SW_POS pin can drive the gates of up to four switches and can be used to control the ADTR1107 SPDT switch.

While the ADTR1107 LNA gate voltage is self biased (the VGG_LNA pin is connected to 0 V or grounded), the voltage can also be controlled from the ADAR1000. In this case, there is a single LNA_BIAS voltage (0 V to −4.8 V) controlled by an 8-bit DAC that can be used to bias four ADTR1107 devices connected to each ADAR1000.

The ADTR1107 CPLR_OUT coupler output can be tied back to one of the four ADAR1000 RF detector inputs (DET1 to DET4). These diode based RF detectors have an input range of −20 dBm to +10 dBm. The coupling factor of the ADTR1107 directional coupler ranges from 28 dB at 6 GHz to 18 dB at 18 GHz. At 12 GHz, with a coupling factor of 22 dB and a maximum power amplifier output of 26 dBm, the coupled output power is a maximum of 4 dBm. If the coupler output is connected directly to the detector input, this connection provides a detection range of 24 dB. Figure 90 shows the relationship between the ADTR1107 output power and the ADC code of the ADAR1000 detector at 12 GHz. In this case, the ADTR1107 output power is swept to a maximum level of approximately 22 dBm.

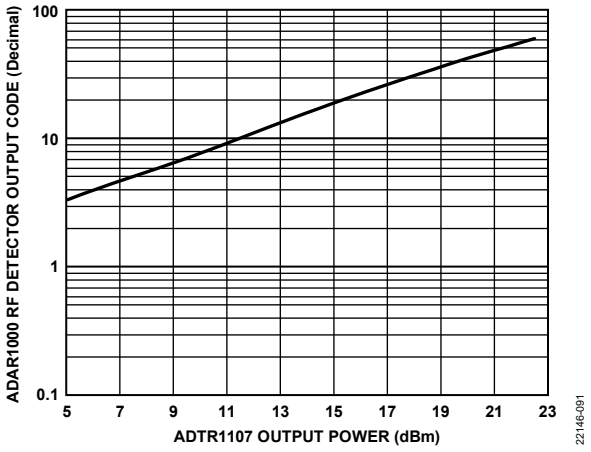

Figure 90. ADAR1000 RF Detector Output Code vs. ADTR1107 Output Power at 12 GHz

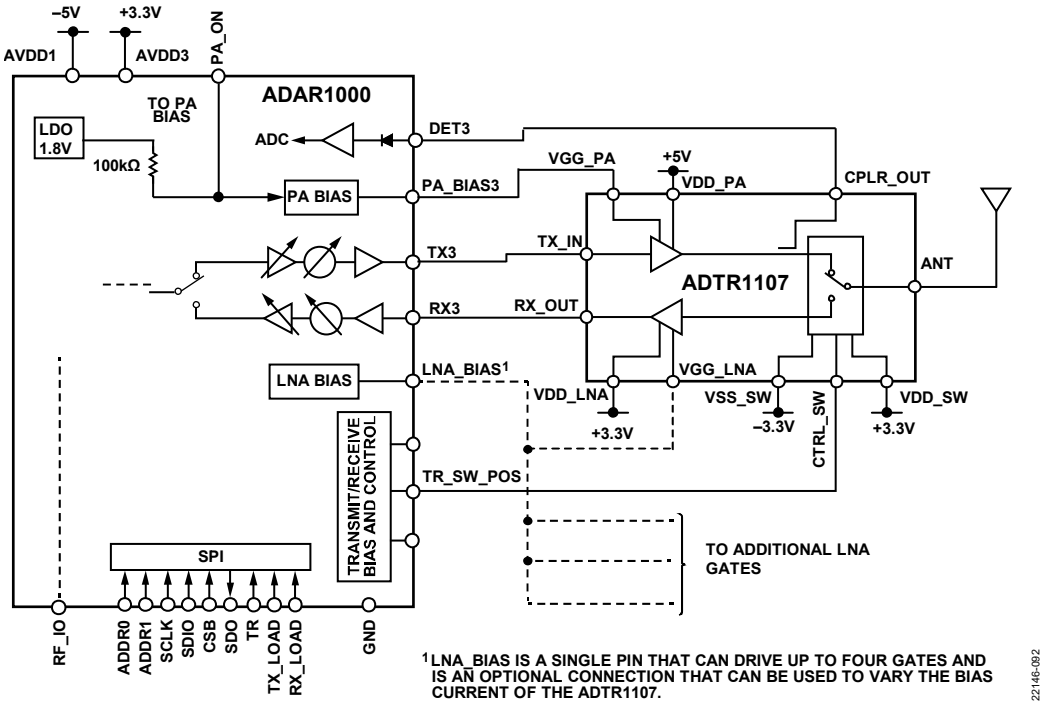

Figure 91. Interfacing the ADTR1107 to the ADAR1000 X and Ku Band Beamformer, One Channel Shown

OUTLINE DIMENSIONS

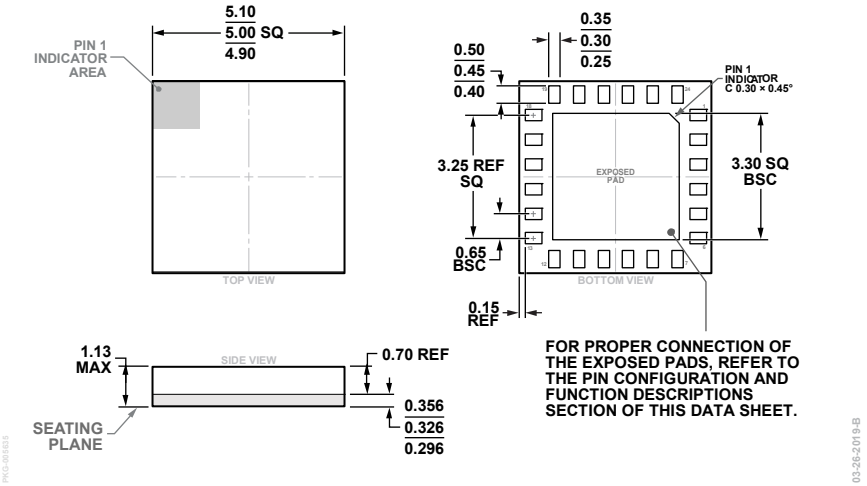

Figure 92. 24-Terminal Land Grid Array [LGA]
(CC-24-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description[3]	Package Option
ADTR1107ACCZ	−40°C to +85°C	3	24-Terminal Land Grid Array [LGA]	CC-24-8
ADTR1107ACCZ-R7	−40°C to +85°C	3	24-Terminal Land Grid Array [LGA]	CC-24-8
ADTR1107-EVAL			Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] See the Absolute Maximum Ratings section for additional information.
[3] The lead finish of the ADTR1107ACCZ and the ADTR1107ACCZ-R7 is nickel palladium gold (NiPdAu).

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