ANALOG DEVICES

Dual-Channel Digital Isolators, 5 kV

Data Sheet

ADuM2200/ADuM2201

FEATURES

High isolation voltage: 5000 V rms
Enhanced system-level ESD performance per IEC 61000-4-x
Low power operation
- **5 V operation**
  - **1.6 mA per channel maximum at 0 Mbps to 1 Mbps**
  - **3.7 mA per channel maximum at 10 Mbps**
- **3.3 V operation**
  - **1.4 mA per channel maximum at 0 Mbps to 1 Mbps**
  - **2.4 mA per channel maximum at 10 Mbps**

3.3 V/5 V level translation
High temperature operation: 105°C and 125°C options
High data rate: dc to 10 Mbps (NRZ)
Precise timing characteristics
- **3 ns maximum pulse width distortion**
- **3 ns maximum channel-to-channel matching**

High common-mode transient immunity: >25 kV/μs
16-lead SOIC wide body package version (RW-16)
16-lead SOIC wide body enhanced creepage version (RI-16-2)
Safety and regulatory approvals
- **UL recognition: 5000 V rms for 1 minute per UL 1577**
- **CSA Component Acceptance Notice 5A (RI-16-2 package)**
  - **IEC 60601-1: 250 V rms (reinforced)**
  - **IEC 60950-1: 400 V rms (reinforced)**
- **VDE certificate of conformity**
  - **DIN V VDE V 0884-10 (VDE V 0884-10):2006-12**
  - **V_{IORM} = 848 V peak**

Qualified for automotive applications

APPLICATIONS

General-purpose, high voltage, multichannel isolation
Medical equipment
Power supplies
RS-232/RS-422/RS-485 transceiver isolation
Hybrid electric vehicles, battery monitors, and motor drives

GENERAL DESCRIPTION

The ADuM2200/ADuM2201[1] are 2-channel digital isolators based on Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics that are superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *i*Coupler devices remove the design difficulties commonly associated with optocouplers. Typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *i*Coupler digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with these *i*Coupler products. Furthermore, *i*Coupler devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The ADuM2200/ADuM2201 isolators provide two independent isolation channels in two channel configurations with data rates up to 10 Mbps (see the Ordering Guide). Both parts operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems, as well as enabling voltage translation functionality across the isolation barrier. The ADuM2200/ADuM2201 isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

Similar to the ADuM3200/ADuM3201 isolators, the ADuM2200/ADuM2201 isolators contain various circuit and layout enhancements that provide increased capability relative to system-level IEC 61000-4-x testing (ESD, burst, and surge). The precise capability in these tests for either the ADuM3200/ADuM3201 or ADuM2200/ADuM2201 products is strongly determined by the design and layout of the user's board or module. For more information, see the AN-793 Application Note, *ESD/Latch-Up Considerations with iCoupler Isolation Products*.

FUNCTIONAL BLOCK DIAGRAMS

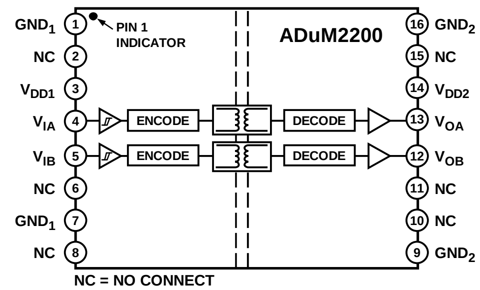

Figure 1. ADuM2200

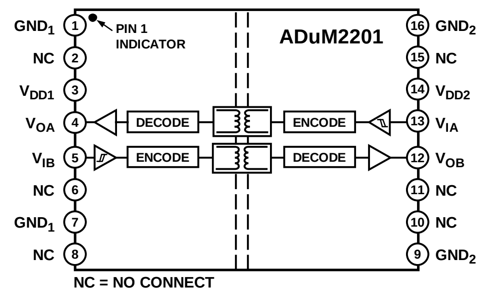

Figure 2. ADuM2201

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents pending.

Rev. G Document Feedback

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All voltages are relative to their respective grounds. 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5.0 V.

Table 1.

Parameter	Symbol	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS									C_L = 15 pF, CMOS levels
Pulse Width	PW	1000			100			ns	Within PWD limit
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	20		150	20		50	ns	50% input to 50% output
Pulse Width Distortion	PWD			40			3	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature						5		ps/°C	
Propagation Delay Skew	t_{PSK}			100			15	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			50			3	ns	
Opposing Directional	t_{PSKOD}			50			15	ns	

Table 2.

Parameter	Symbol	1 Mbps—A Grade, B Grade Min	1 Mbps—A Grade, B Grade Typ	1 Mbps—A Grade, B Grade Max	10 Mbps—B Grade Min	10 Mbps—B Grade Typ	10 Mbps—B Grade Max	Unit
SUPPLY CURRENT (NO LOAD)								
ADuM2200	I_{DD1}		1.3	1.8		3.5	4.6	mA
	I_{DD2}		1.0	1.6		2.0	2.8	mA
ADuM2201	I_{DD1}		1.1	1.6		3.1	4.2	mA
	I_{DD2}		1.3	1.9		3.1	4.0	mA

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments[1]
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	5.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	4.8		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI (Q)}$		0.4	0.8	mA	All inputs at logic low
Quiescent Output Supply Current	$I_{DDO (Q)}$		0.5	0.6	mA	All inputs at logic low
Dynamic Input Supply Current	$I_{DDI (D)}$		0.19		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO (D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F					10% to 90%
A Grade			10		ns	
B Grade			2.5		ns	
Common-Mode Transient Immunity[2]	|CM|	25	35		kV/μs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	

[1] I_{Ox} is the Channel x output current, where x = A or B, V_{IxH} is the input side logic high, and V_{IxL} is the input side logic low.
[2] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All voltages are relative to their respective grounds. 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V.

Table 4.

		A Grade			B Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS									C_L = 15 pF, CMOS levels
Pulse Width	PW	1000			100			ns	Within PWD limit
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	20		150	20		60	ns	50% input to 50% output
Pulse Width Distortion	PWD								$\|t_{PLH} - t_{PHL}\|$
A Grade and B Grade				40			3	ns	
WA Grade and WB Grade				40			4	ns	
Change vs. Temperature						5		ps/°C	
Propagation Delay Skew	t_{PSK}			100			22	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			50			3	ns	
Opposing Directional	t_{PSKOD}			50			22	ns	

Table 5.

		1 Mbps—A Grade, B Grade			10 Mbps—B Grade			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SUPPLY CURRENT (NO LOAD)								
ADuM2200	I_{DD1}		0.8	1.3		2.2	3.2	mA
	I_{DD2}		0.7	1.0		1.3	1.7	mA
ADuM2201	I_{DD1}		0.7	1.3		1.9	2.5	mA
	I_{DD2}		0.8	1.6		1.9	2.5	mA

Table 6.

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**[1]
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	3.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	2.8		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI (Q)}$		0.3	0.5	mA	All inputs at logic low
Quiescent Output Supply Current	$I_{DDO (Q)}$		0.3	0.5	mA	All inputs at logic low
Dynamic Input Supply Current	$I_{DDI (D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO (D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F					10% to 90%
A Grade			10		ns	
B Grade			3		ns	
Common-Mode Transient Immunity[2]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	

[1] I_{Ox} is the Channel x output current, where x = A or B, V_{IxH} is the input side logic high, and V_{IxL} is the input side logic low.
[2] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V OPERATION

All voltages are relative to their respective grounds. 4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V, V_{DD2} = 5.0 V.

Table 7.

Parameter	Symbol	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit	Test Conditions/ Comments
SWITCHING SPECIFICATIONS									C_L = 15 pF, CMOS levels
Pulse Width	PW	1000			100			ns	Within PWD limit
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	15		150	15		55	ns	50% input to 50% output
Pulse Width Distortion	PWD								$\|t_{PLH} - t_{PHL}\|$
A Grade and B Grade				40			3	ns	
WA Grade and WB Grade				40			4	ns	
Change vs. Temperature						5		ps/°C	
Propagation Delay Skew	t_{PSK}			50			22	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			50			3	ns	
Opposing Directional	t_{PSKOD}			50			22	ns	

Table 8.

Parameter	Symbol	1 Mbps—A Grade, B Grade Min	Typ	Max	10 Mbps—B Grade Min	Typ	Max	Unit
SUPPLY CURRENT (NO LOAD)								
ADuM2200	I_{DD1}		1.3	1.8		3.5	4.6	mA
	I_{DD2}		0.7	1.0		1.3	1.7	mA
ADuM2201	I_{DD1}		1.1	1.6		3.1	4.2	mA
	I_{DD2}		0.8	1.6		1.9	2.5	mA

Table 9.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments[1]
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI (Q)}$		0.4	0.8	mA	All inputs at logic low
Quiescent Output Supply Current	$I_{DDO (Q)}$		0.3	0.5	mA	All inputs at logic low
Dynamic Input Supply Current	$I_{DDI (D)}$		0.19		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO (D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F					10% to 90%
A Grade			10		ns	
B Grade			3		ns	
Common-Mode Transient Immunity[2]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	

[1] I_{Ox} is the Channel x output current, where x = A or B, V_{IxH} is the input side logic high, and V_{IxL} is the input side logic low.
[2] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V OPERATION

All voltages are relative to their respective grounds. 3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = 5.0 V, V_{DD2} = 3.3 V.

Table 10.

		A Grade			B Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS									C_L = 15 pF, CMOS levels
Pulse Width	PW	1000			100			ns	Within PWD limit
Data Rate				1			10	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	15		150	15		55	ns	50% input to 50% output
Pulse Width Distortion	PWD								$\lvert t_{PLH} - t_{PHL} \rvert$
A Grade and B Grade				40			3	ns	
WA Grade and WB Grade				40			4	ns	
Change vs. Temperature						5		ps/°C	
Propagation Delay Skew	t_{PSK}			50			22	ns	Between any two units
Channel Matching									
Codirectional	t_{PSKCD}			50			3	ns	
Opposing Directional	t_{PSKOD}			50			22	ns	

Table 11.

		1 Mbps—A Grade, B Grade			10 Mbps—B Grade			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SUPPLY CURRENT (NO LOAD)								
ADuM2200	I_{DD1}		0.8	1.3		2.2	3.2	mA
	I_{DD2}		1.0	1.6		2.0	2.8	mA
ADuM2201	I_{DD1}		0.7	1.3		1.9	2.5	mA
	I_{DD2}		1.3	1.9		3.1	4.0	mA

Table 12.

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**[1]
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.3	0.5	mA	All inputs at logic low
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.5	0.6	mA	All inputs at logic low
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F					10% to 90%
A Grade			10		ns	
B Grade			2.5		ns	
Common-Mode Transient Immunity[2]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	

[1] I_{Ox} is the Channel x output current, where x = A or B, V_{IxH} is the input side logic high, and V_{IxL} is the input side logic low.
[2] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS

Table 13.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4		pF	
IC Junction-to-Ambient Thermal Resistance	$θ_{JA}$		45		°C/W	

[1] This device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM2200/ADuM2201 are approved by the organizations listed in Table 14. Refer to Table 19 and the Insulation Lifetime section for more information about the recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 14.

UL	CSA	CQC	VDE
Recognized Under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Approved under CQC11-471543-2012	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single Protection, 5000 V rms Isolation Voltage	Basic insulation per CSA 60950-1-07 and IEC 60950-1, 600 V rms (848 V peak) maximum working voltage RW-16 package: reinforced insulation per CSA 60950-1-07 and IEC 60950-1, 380 V rms (537 V peak) maximum working voltage; reinforced insulation per IEC 60601-1, 125 V rms (176 V peak) maximum working voltage RI-16-2 package: reinforced insulation per CSA 60950-1-07 and IEC 60950-1, 400 V rms (565 V peak) maximum working voltage; reinforced insulation per IEC 60601-1, 250 V rms (353 V peak) maximum working voltage	Basic insulation per GB4943.1-2011, 600 V rms (848 V peak) maximum working voltage, tropical climate, altitude ≤ 5000 m RW-16 package: reinforced insulation per GB4943.1-2011, 380 V rms (537 V peak) maximum working voltage, tropical climate, altitude ≤ 5000 m RI-16 package: reinforced insulation per 400 V rms (565 V peak) maximum working voltage, tropical climate, altitude ≤ 5000 m	Reinforced insulation, 848 V peak
File E214100	File 205078	File: CQC14001105917	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM2200/ADuM2201 is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec (current leakage detection limit = 10 μA).
[2] In accordance with DIN V VDE V 0884-10 (VDE V 0884-10):2006-12, each ADuM2200/ADuM2201 is proof tested by applying an insulation test voltage ≥1592 V peak for 1 sec (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the components designates DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 15.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	8.0 min	mm	Distance measured from input terminals to output terminals, shortest distance through air along the PCB mounting plane, as an aid to PC board layout
Minimum External Tracking (Creepage)	L(I02)			Measured from input terminals to output terminals, shortest distance path along body
RW-16 Package		7.7 min	mm	
RI-16-2 Package		8.3 min	mm	
Minimum Internal Distance (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303, Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

INSULATION CHARACTERISTICS (DIN V VDE V 0884-10 (VDE V 0884-10):2006-12)

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits. The asterisk (*) marking branded on the components designates DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 approval for 848 V peak working voltage.

Table 16.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 400 V rms			I to IV	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	848	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V peak
Input-to-Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1273	V peak
After Input and/or Safety Tests Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1018	V peak
Highest Allowable Overvoltage	Transient overvoltage, $t_{TR} = 10$ sec	V_{TR}	6000	V peak
Surge Isolation Voltage	V peak = 10 kV, 1.2 μs rise time, 50 μs, 50% fall time	V_{IOSM}	6000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure; see Figure 3			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	2.78	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

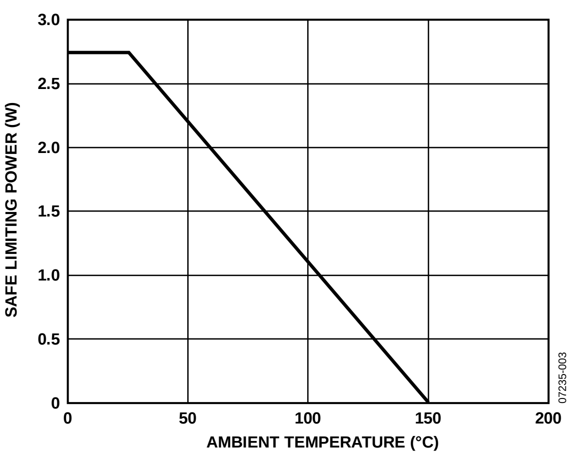


Figure 3. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 17.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A			
A Grade and B Grade		−40	+105	°C
WA Grade and WB Grade		−40	+125	°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	3.0	5.5	V
Input Signal Rise and Fall Times			1.0	ms

[1] All voltages are relative to their respective grounds.

ABSOLUTE MAXIMUM RATINGS

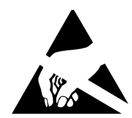
Table 18.

Parameter	Rating
Storage Temperature (T_{ST})	−65°C to +150°C
Ambient Operating Temperature (T_A)	−40°C to +125°C
Supply Voltage (V_{DD1}, V_{DD2})[1]	−0.5 V to +7.0 V
Input Voltage (V_{IA}, V_{IB})[1, 2]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage (V_{OA}, V_{OB})[1, 2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[3]	
Side 1 (I_{O1})	−18 mA to +18 mA
Side 2 (I_{O2})	−22 mA to +22 mA
Common-Mode Transients[4]	−100 kV/μs to +100 kV/μs

[1] All voltages are relative to their respective grounds.
[2] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the PCB Layout section.
[3] See Figure 3 for maximum rated current values for various temperatures.
[4] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 19. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Reinforced Insulation	1131	V peak	50-year minimum lifetime
DC Voltage			
Reinforced Insulation	1131	V peak	50-year minimum lifetime

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

Table 20. ADuM2200 Truth Table (Positive Logic)

V_{IA} Input[1]	V_{IB} Input[1]	V_{DD1} State	V_{DD2} State	V_{OA} Output[1]	V_{OB} Output[1]	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	H	H	Outputs return to the input state within 1 μs of V_{DDI} power restoration.
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1 μs of V_{DDO} power restoration.

[1] H is logic high, L is logic low, and X is don't care.

Table 21. ADuM2201 Truth Table (Positive Logic)

V_{IA} Input[1]	V_{IB} Input[1]	V_{DD1} State	V_{DD2} State	V_{OA} Output[1]	V_{OB} Output[1]	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	Indeterminate	H	Outputs return to the input state within 1 μs of V_{DDI} power restoration.
X	X	Powered	Unpowered	H	Indeterminate	Outputs return to the input state within 1 μs of V_{DDO} power restoration.

[1] H is logic high, L is logic low, and X is don't care.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

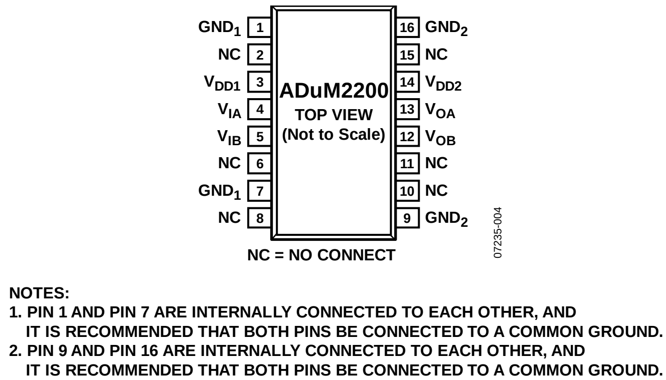
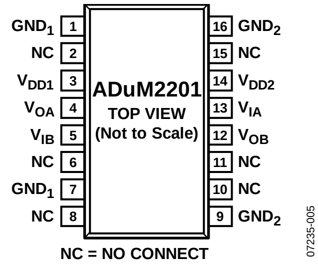


Figure 4. ADuM2200 Pin Configuration

Table 22. ADuM2200 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 1 and Pin 7 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
2	NC	No Internal Connection.
3	V_{DD1}	Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V.
4	V_{IA}	Logic Input A.
5	V_{IB}	Logic Input B.
6	NC	No Internal Connection.
8	NC	No Internal Connection.
9, 16	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 16 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
10	NC	No Internal Connection.
11	NC	No Internal Connection.
12	V_{OB}	Logic Output B.
13	V_{OA}	Logic Output A.
14	V_{DD2}	Supply Voltage for Isolator Side 2, 3.0 V to 5.5 V.
15	NC	No Internal Connection.



NOTES:
1. PIN 1 AND PIN 7 ARE INTERNALLY CONNECTED TO EACH OTHER, AND IT IS RECOMMENDED THAT BOTH PINS BE CONNECTED TO A COMMON GROUND.
2. PIN 9 AND PIN 16 ARE INTERNALLY CONNECTED TO EACH OTHER, AND IT IS RECOMMENDED THAT BOTH PINS BE CONNECTED TO A COMMON GROUND.

Figure 5. ADuM2201 Pin Configuration

Table 23. ADuM2201 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 1 and Pin 7 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
2	NC	No Internal Connection.
3	V_{DD1}	Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V.
4	V_{OA}	Logic Output A.
5	V_{IB}	Logic Input B.
6	NC	No Internal Connection.
8	NC	No Internal Connection.
9, 16	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 16 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
10	NC	No Internal Connection.
11	NC	No Internal Connection.
12	V_{OB}	Logic Output B.
13	V_{IA}	Logic Input A.
14	V_{DD2}	Supply Voltage for Isolator Side 2, 3.0 V to 5.5 V.
15	NC	No Internal Connection.

TYPICAL PERFORMANCE CHARACTERISTICS

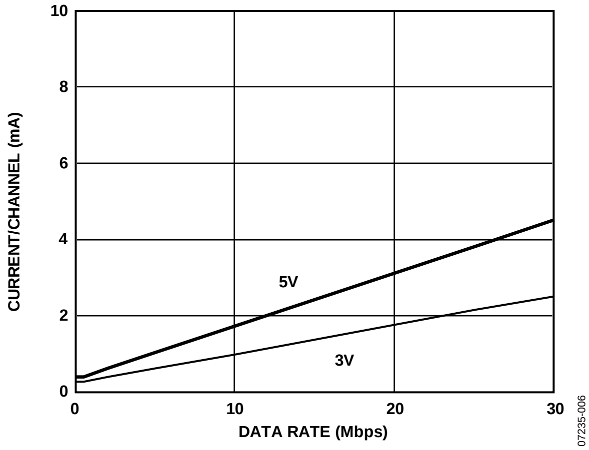


Figure 6. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3.3 V Operation (No Output Load)

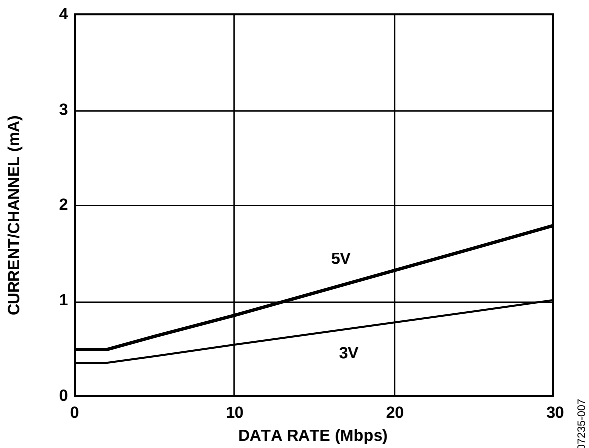


Figure 7. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3.3 V Operation (No Output Load)

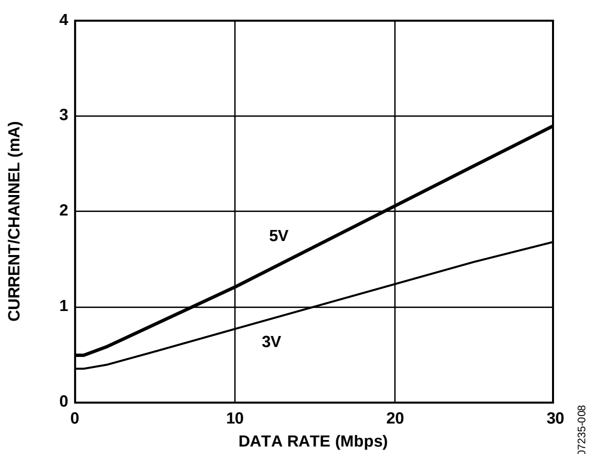


Figure 8. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3.3 V Operation (15 pF Output Load)

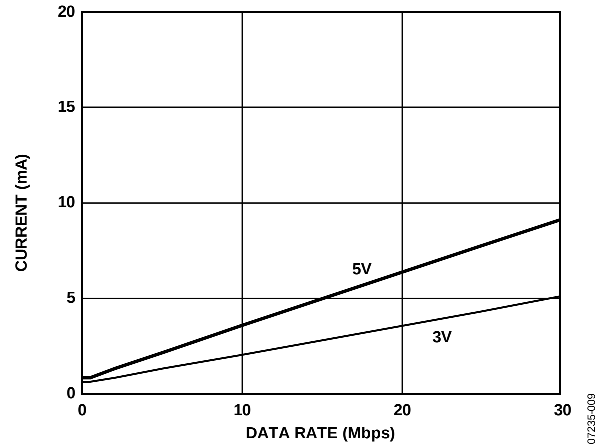


Figure 9. Typical ADuM2200 V_{DD1} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

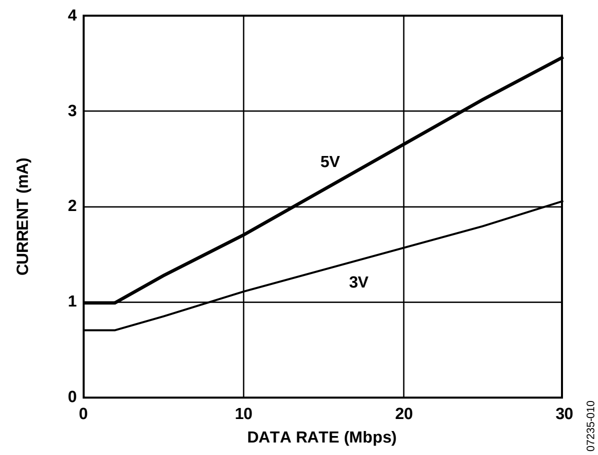


Figure 10. Typical ADuM2200 V_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

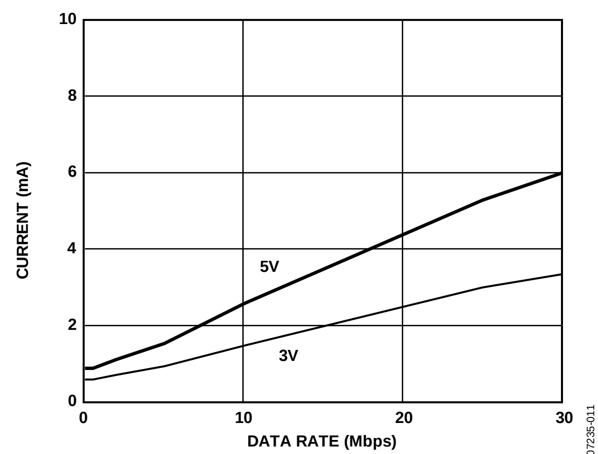


Figure 11. Typical ADuM2201 V_{DD1} or V_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM2200/ADuM2201 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 12). Bypass capacitors are most conveniently connected between Pin 1 and Pin 3 for V_{DD1} and between Pin 14 and Pin 16 for V_{DD2}. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 2 mm. Consider bypassing between Pin 3 and Pin 7 and between Pin 9 and Pin 14 unless the ground pair on each package side is connected close to the package.

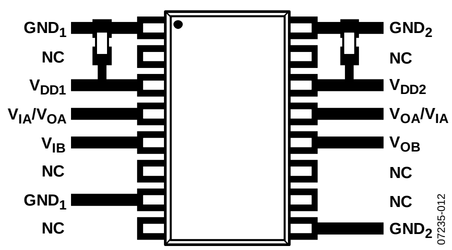


Figure 12. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur affects all pins equally on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the absolute maximum ratings for the device as specified in Table 18, thereby leading to latch-up or permanent damage.

See the AN-1109 Application Note for board layout guidelines.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the length of time it takes for a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output.

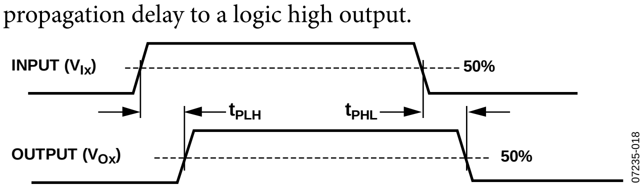


Figure 13. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM2200/ADuM2201 component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM2200/ ADuM2201 components operated under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 µs, a periodic set of refresh pulses indicative of the correct input state is sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than approximately 5 µs, the input side is assumed to be unpowered or nonfunctional, and the isolator output is forced to a default state by the watchdog timer circuit (see Table 20 and Table 21).

The limitation on the magnetic field immunity of the ADuM2200/ ADuM2201 is set by the condition in which induced voltage in the transformer receiving coil is large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3.3 V operating condition of the ADuM2200/ADuM2201 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at approximately 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2;\ n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density (gauss).
r_n is the radius of the nth turn in the receiving coil (cm).
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM2200/ ADuM2201 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 14.

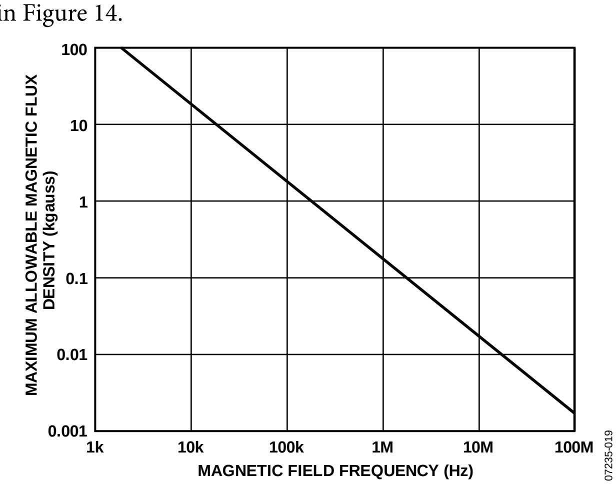


Figure 14. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This voltage is approximately 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM2200/ADuM2201 transformers. Figure 15 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 15, the ADuM2200/ADuM2201 are immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted, a 0.5 kA current placed 5 mm away from the ADuM2200/ADuM2201 is required to affect the operation of the component.

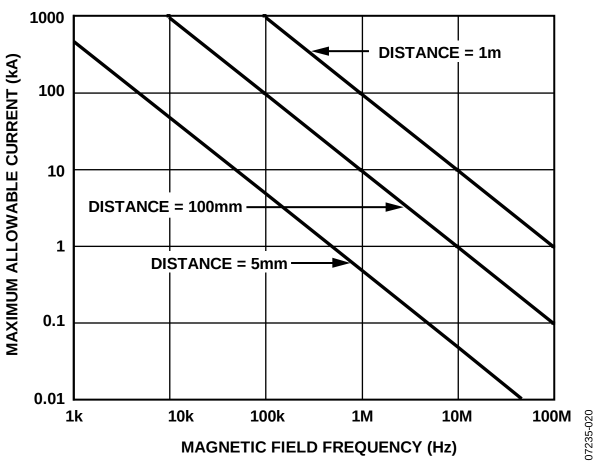


Figure 15. Maximum Allowable Current for Various Current-to-ADuM2200/ADuM2201 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces can induce error voltages sufficiently large to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM2200/ADuM2201 isolators is a function of the supply voltage, the channel data rate, and the channel output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \qquad f \leq 0.5f_r$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)} \qquad f > 0.5f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO\,(Q)} \qquad f \leq 0.5f_r$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \qquad f > 0.5f_r$$

where:

$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).

C_L is the output load capacitance (pF).

V_{DDO} is the output supply voltage (V).

f is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).

f_r is the input stage refresh rate (Mbps).

To calculate the total I_{DD1} and I_{DD2}, the supply currents for each input and output channel corresponding to I_{DD1} and I_{DD2} are calculated and totaled.

Figure 6 and Figure 7 provide per-channel supply currents as a function of data rate for an unloaded output condition. Figure 8 provides per-channel supply current as a function of data rate for a 15 pF output condition. Figure 9 through Figure 11 provide total I_{DD1} and I_{DD2} as a function of data rate for the ADuM2200/ADuM2201 channel configurations.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM2200/ADuM2201 devices.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 19 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM2200/ADuM2201 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates, depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 16, Figure 17, and Figure 18 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the bipolar ac condition determines the maximum working voltage recommended by Analog Devices.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 19 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to either the unipolar ac or dc voltage cases.

Any cross-insulation voltage waveform that does not conform to Figure 17 or Figure 18 should be treated as a bipolar ac waveform and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 19.

Note that the voltage presented in Figure 17 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

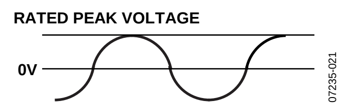


Figure 16. Bipolar AC Waveform

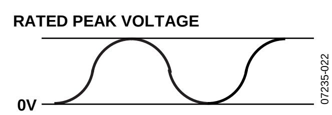


Figure 17. Unipolar AC Waveform

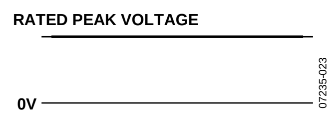


Figure 18. DC Waveform

OUTLINE DIMENSIONS

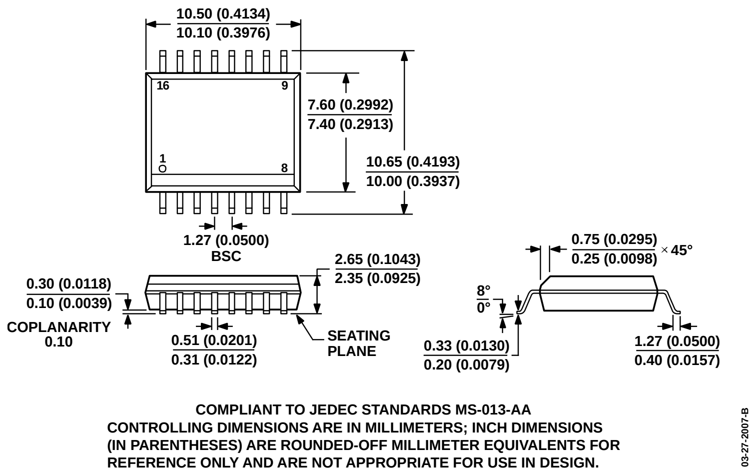


Figure 19. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

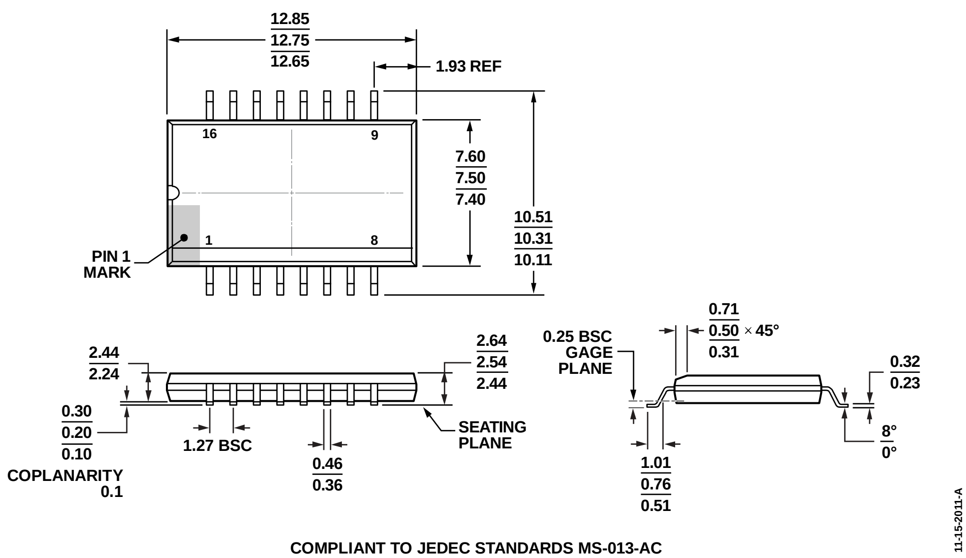


Figure 20. 16-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]
Wide Body
(RI-16-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range	Package Description	Package Option
ADuM2200ARIZ	2	0	1	150	40	−40°C to +105°C	16-Lead SOIC_IC	RI-16-2
ADuM2200ARWZ	2	0	1	150	40	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM2200WARWZ	2	0	1	150	40	−40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM2200BRIZ	2	0	10	50	3	−40°C to +105°C	16-Lead SOIC_IC	RI-16-2
ADuM2200BRWZ	2	0	10	50	3	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM2200WBRWZ	2	0	10	50	3	−40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM2201ARIZ	1	1	1	150	40	−40°C to +105°C	16-Lead SOIC_IC	RI-16-2
ADuM2201ARWZ	1	1	1	150	40	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM2201WARWZ	1	1	1	150	40	−40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM2201BRIZ	1	1	10	50	3	−40°C to +105°C	16-Lead SOIC_IC	RI-16-2
ADuM2201BRWZ	1	1	10	50	3	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM2201WBRWZ	1	1	10	50	3	−40°C to +125°C	16-Lead SOIC_W	RW-16

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.
[3] Tape and reel is available. The addition of an -RL suffix designates a 13″ (1,000 units) tape and reel option.

AUTOMOTIVE PRODUCTS

The ADuM2200W and ADuM2201W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

D07235-0-9/15(G)