Dual-Channel, Digital Isolators, Enhanced System-Level ESD Reliability

Data Sheet

ADuM3200/ADuM3201

FEATURES

Enhanced system-level ESD performance per IEC 61000-4-x
High temperature operation: 125°C
Narrow body, RoHS-compliant, 8-lead SOIC
Low power operation
- **5 V operation**
  - **1.7 mA per channel maximum at 0 Mbps to 2 Mbps**
  - **3.7 mA per channel maximum at 10 Mbps**
  - **7.0 mA per channel maximum at 25 Mbps**
- **3.3 V operation**
  - **1.5 mA per channel maximum at 0 Mbps to 2 Mbps**
  - **2.5 mA per channel maximum at 10 Mbps**
  - **5.2 mA per channel maximum at 25 Mbps**

Bidirectional communication
3.3 V/5 V level translation
High data rate: dc to 25 Mbps (NRZ)
Precise timing characteristics
- **3 ns maximum pulse width distortion**
- **3 ns maximum channel-to-channel matching**

High common-mode transient immunity: >25 kV/μs
Safety and regulatory approvals
- **UL recognition: 2500 V rms for 1 minute per UL 1577**
- **CSA Component Acceptance Notice 5A**
- **VDE Certificate of Conformity**
  - **DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12**
  - **V_{IORM} = 560 V peak**

Qualified for automotive applications

APPLICATIONS

Size-critical multichannel isolation
SPI interface/data converter isolation
RS-232/RS-422/RS-485 transceiver isolation
Digital field bus isolation
Hybrid electric vehicles, battery monitor

GENERAL DESCRIPTION

The ADuM3200/ADuM3201[1] are dual-channel, digital isolators based on the Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *i*Coupler devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *i*Coupler digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with these *i*Coupler products. Furthermore, *i*Coupler devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The ADuM3200/ADuM3201 isolators provide two independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide). They operate with 3.3 V or 5 V supply voltages on either side, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. The ADuM3200W and ADuM3201W are automotive grade versions qualified for 125°C operation.

In comparison to the ADuM1200/ADuM1201 isolators, the ADuM3200/ADuM3201 isolators contain various circuit and layout changes to provide increased capability relative to system-level IEC 61000-4-x testing (ESD, burst, and surge). The precise capability in these tests for either the ADuM1200/ADuM1201 or ADuM3200/ADuM3201 products is strongly determined by the design and layout of the user board or module. For more information, see the AN-793 Application Note, *ESD/Latch-Up Considerations with iCoupler Isolation Products.*

FUNCTIONAL BLOCK DIAGRAMS

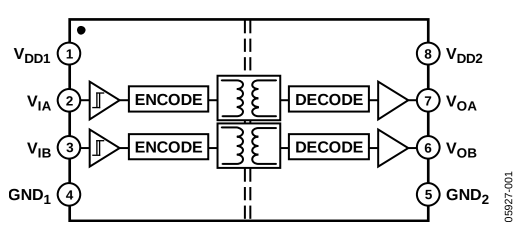

Figure 1. ADuM3200 Functional Block Diagram

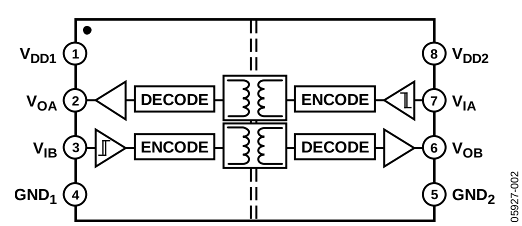

Figure 2. ADuM3201 Functional Block Diagram

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,329.

Rev. F Document Feedback

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REVISION HISTORY

5/2016—Rev. E to Rev. F

7/2015—Rev. D to Rev. E

10/2014—Rev. C to Rev. D

2/2012—Rev. B to Rev. C

11/2011—Rev. A to Rev. B

6/2007—Rev. 0 to Rev. A

7/2006—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V, 105°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 1.

Parameter	Symbol	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	C Grade Min	C Grade Typ	C Grade Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS												
Data Rate				1			10			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	20		150	20		50	20		45	ns	50% input to 50% output
Pulse Width Distortion	PWD			40			3			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			6			5			5		ps/°C	
Pulse Width	PW	1000			100			40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			100			15			15	ns	Between any two units
Channel Matching												
Codirectional	t_{PSKCD}			50			3			3	ns	
Opposing-Direction	t_{PSKOD}			50			15			15	ns	
Output Rise/Fall Time	t_R/t_F		10			2.5			2.5		ns	10% to 90%

Table 2.

Parameter	Symbol	1 Mbps—A Grade, B Grade, and C Grade Min	Typ	Max	10 Mbps—B Grade and C Grade Min	Typ	Max	25 Mbps—C Grade Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT												
ADuM3200	I_{DD1}		1.3	1.8		3.5	4.6		7.7	10.0	mA	No load
	I_{DD2}		1.0	1.6		2.0	2.8		3.8	4.9	mA	No load
ADuM3201	I_{DD1}		1.1	1.6		3.1	4.2		6.9	8.9	mA	No load
	I_{DD2}		1.3	1.9		3.1	4.0		6.1	8.3	mA	No load

Table 3. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDX}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.8	mA	V_{IA} = V_{IB} = 0 V
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.5	0.6	mA	V_{IA} = V_{IB} = 0 V
Dynamic Input Supply Current	$I_{DDI(D)}$		0.19		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDX}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3.3 V, 105°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 4.

Parameter	Symbol	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	C Grade Min	C Grade Typ	C Grade Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS												
Data Rate				1			10			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	20		150	20		60	20		55	ns	50% input to 50% output
Pulse Width Distortion	PWD											
ADuM3200				40			3			3	ns	$\|t_{PLH} - t_{PHL}\|$
ADuM3201				40			4			4	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			6			5			5		ps/°C	
Pulse Width	PW	1000			100			40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			100			22			16	ns	Between any two units
Channel Matching												
Codirectional	t_{PSKCD}			50			3			3	ns	
Opposing-Direction	t_{PSKOD}			50			22			16	ns	
Output Rise/Fall Time	t_R/t_F		3.0			3.0			3.0		ns	10% to 90%

Table 5.

Parameter	Symbol	1 Mbps—A Grade, B Grade, and C Grade Min	Typ	Max	10 Mbps—B Grade and C Grade Min	Typ	Max	25 Mbps—C Grade Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT												
ADuM3200	I_{DD1}		0.8	1.3		2.2	3.2		4.8	6.4	mA	No load
	I_{DD2}		0.7	1.0		1.3	1.7		2.3	3.0	mA	No load
ADuM3201	I_{DD1}		0.7	1.3		1.9	2.5		4.1	5.3	mA	No load
	I_{DD2}		0.8	1.6		1.9	2.5		3.7	5.1	mA	No load

Table 6. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDX}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.3	0.5	mA	V_{IA} = V_{IB} = 0 V
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.3	0.5	mA	V_{IA} = V_{IB} = 0 V
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDX}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V, 105°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF, and CMOS signal levels, unless otherwise noted.

Table 7.

		A Grade			B Grade			C Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS												
Data Rate				1			10			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	15		150	15		55	15		50	ns	50% input to 50% output
Pulse Width Distortion	PWD			40			3			3	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			6			5			5		ps/°C	
Pulse Width	PW	1000			100			40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			50			22			15	ns	Between any two units
Channel Matching												
Codirectional	t_{PSKCD}			50			3			3	ns	
Opposing-Direction	t_{PSKOD}			50			22			15	ns	
Output Rise/Fall Time	t_R/t_F		3.0			3.0			3.0		ns	10% to 90%

Table 8.

		1 Mbps—A Grade, B Grade, and C Grade			10 Mbps—B Grade and C Grade			25 Mbps—C Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SUPPLY CURRENT												
ADuM3200	I_{DD1}		1.3	1.8		3.5	4.6		7.7	10.0	mA	No load
	I_{DD2}		0.7	1.0		1.3	1.7		2.3	3.0	mA	No load
ADuM3201	I_{DD1}		1.1	1.6		3.1	4.2		6.9	8.9	mA	No load
	I_{DD2}		0.8	1.6		1.9	2.5		3.7	5.1	mA	No load

Table 9. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDX}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.8	mA	V_{IA} = V_{IB} = 0 V
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.3	0.5	mA	V_{IA} = V_{IB} = 0 V
Dynamic Input Supply Current	$I_{DDI(D)}$		0.19		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DDX}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V, 105°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V, V_{DD2} = 5.0 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 10.

Parameter	Symbol	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	C Grade Min	C Grade Typ	C Grade Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS												
Data Rate				1			10			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	15		150	15		55	15		50	ns	50% input to 50% output
Pulse Width Distortion	PWD											
ADuM3200				40			3			3	ns	$\|t_{PLH} - t_{PHL}\|$
ADuM3201				40			4			4	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			6			5			5		ps/°C	
Pulse Width	PW	1000			100			40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			50			22			15	ns	Between any two units
Channel Matching												
Codirectional	t_{PSKCD}			50			3			3	ns	
Opposing-Direction	t_{PSKOD}			50			22			15	ns	
Output Rise/Fall Time	t_R/t_F		2.5			2.5			2.5		ns	10% to 90%

Table 11.

Parameter	Symbol	1 Mbps—A Grade, B Grade, and C Grade Min	Typ	Max	10 Mbps—B Grade and C Grade Min	Typ	Max	25 Mbps—C Grade Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT												
ADuM3200	I_{DD1}		0.8	1.3		2.2	3.2		4.8	6.4	mA	No load
	I_{DD2}		1.0	1.6		2.0	2.8		3.8	4.9	mA	No load
ADuM3201	I_{DD1}		0.7	1.3		1.9	2.5		4.1	5.3	mA	No load
	I_{DD2}		1.3	1.9		3.1	4.0		6.1	8.3	mA	No load

Table 12. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0. 1	V_{DDx}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDX}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.3	0.5	mA	V_{IA} = V_{IB} = 0 V
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.5	0.6	mA	V_{IA} = V_{IB} = 0 V
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDX}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—5 V, 125°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 13.

		WA Grade			WB Grade			WC Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS												
Data Rate				1			10			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	20		150	20		50	20		45	ns	50% input to 50% output
Pulse Width Distortion	PWD			40			3			3	ns	$\|t_{PLH} − t_{PHL}\|$
Change vs. Temperature			6			5			5		ps/°C	
Pulse Width	PW	1000			100			40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			100			15			15	ns	Between any two units
Channel Matching												
Codirectional	t_{PSKCD}			50			3			3	ns	
Opposing-Direction	t_{PSKOD}			50			15			15	ns	
Output Rise/Fall Time	t_R/t_F		2.5			2.5			2.5		ns	10% to 90%

Table 14.

		1 Mbps—WA Grade, WB Grade, and WC Grade			10 Mbps—WB Grade and WC Grade			25 Mbps—WC Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/ Comments**
SUPPLY CURRENT												
ADuM3200	I_{DD1}		1.3	2.0		3.5	4.6		7.7	10.0	mA	No load
	I_{DD2}		1.0	1.6		1.7	2.8		3.1	3.9	mA	No load
ADuM3201	I_{DD1}		1.1	1.5		2.6	3.4		5.3	6.8	mA	No load
	I_{DD2}		1.3	1.8		3.1	4.0		6.4	8.3	mA	No load

Table 15. For All Models

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDX}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.8	mA	V_{IA} = V_{IB} = 0 V
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.5	0.6	mA	V_{IA} = V_{IB} = 0 V
Dynamic Input Supply Current	$I_{DDI(D)}$		0.19		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDX}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3.3 V, 125°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 16.

Parameter	Symbol	WA Grade Min	WA Grade Typ	WA Grade Max	WB Grade Min	WB Grade Typ	WB Grade Max	WC Grade Min	WC Grade Typ	WC Grade Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS												
Data Rate				1			10			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	20		150	20		60	20		55	ns	50% input to 50% output
Pulse Width Distortion	PWD											
ADuM3200				40			3			3	ns	$\|t_{PLH} − t_{PHL}\|$
ADuM3201				40			4			4	ns	$\|t_{PLH} − t_{PHL}\|$
Change vs. Temperature			6			5			5		ps/°C	
Pulse Width	PW	1000			100			40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			100			22			16	ns	Between any two units
Channel Matching												
Codirectional	t_{PSKCD}			50			3			3	ns	
Opposing-Direction	t_{PSKOD}			50			22			16	ns	
Output Rise/Fall Time	t_R/t_F		3.0			3.0			3.0		ns	10% to 90%

Table 17.

Parameter	Symbol	1 Mbps—WA Grade, WB Grade, and WC Grade Min	Typ	Max	10 Mbps—WB Grade and WC Grade Min	Typ	Max	25 Mbps—WC Grade Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT												
ADuM3200	I_{DD1}		0.8	1.3		2.0	3.2		4.3	6.4	mA	No load
	I_{DD2}		0.7	1.0		1.1	1.7		1.8	2.4	mA	No load
ADuM3201	I_{DD1}		0.7	1.3		1.5	2.1		3.0	4.2	mA	No load
	I_{DD2}		0.8	1.6		1.9	2.4		3.6	5.1	mA	No load

Table 18. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDX}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.3	0.5	mA	V_{IA} = V_{IB} = 0 V
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.3	0.5	mA	V_{IA} = V_{IB} = 0 V
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDX}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V, 125°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 19.

Parameter	Symbol	WA Grade Min	WA Grade Typ	WA Grade Max	WB Grade Min	WB Grade Typ	WB Grade Max	WC Grade Min	WC Grade Typ	WC Grade Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS												
Data Rate				1			10			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	15		150	15		55	15		50	ns	50% input to 50% output
Pulse Width Distortion	PWD			40			3			3	ns	$\|t_{PLH} − t_{PHL}\|$
Change vs. Temperature			6			5			5		ps/°C	
Pulse Width	PW	1000			100			40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			50			22			15	ns	Between any two units
Channel Matching												
Codirectional	t_{PSKCD}			50			3			3	ns	
Opposing-Direction	t_{PSKOD}			50			22			15	ns	
Output Rise/Fall Time	t_R/t_F		3.0			3.0			3.0		ns	10% to 90%

Table 20.

Parameter	Symbol	1 Mbps—WA Grade, WB Grade, and WC Grade Min	Typ	Max	10 Mbps—WB Grade and WC Grade Min	Typ	Max	25 Mbps—WC Grade Min	Typ	Max	Unit	Test Conditions/ Comments
SUPPLY CURRENT												
ADuM3200	I_{DD1}		1.3	2.0		3.5	4.6		7.7	10.0	mA	No load
	I_{DD2}		0.7	1.0		1.1	1.7		1.8	2.4	mA	No load
ADuM3201	I_{DD1}		1.1	1.5		2.6	3.4		5.3	6.8	mA	No load
	I_{DD2}		0.8	1.6		1.9	2.4		3.6	5.1	mA	No load

Table 21. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDX}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.8	mA	V_{IA} = V_{IB} = 0 V
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.3	0.5	mA	V_{IA} = V_{IB} = 0 V
Dynamic Input Supply Current	$I_{DDI(D)}$		0.19		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDX}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V, 125°C OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V, V_{DD2} = 5.0 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 22.

Parameter	Symbol	WA Grade Min	WA Grade Typ	WA Grade Max	WB Grade Min	WB Grade Typ	WB Grade Max	WC Grade Min	WC Grade Typ	WC Grade Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS												
Data Rate				1			10			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	15		150	15		55	15		50	ns	50% input to 50% output
Pulse Width Distortion	PWD											
ADuM3200				40			3			3	ns	$\|t_{PLH} - t_{PHL}\|$
ADuM3201				40			4			4	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			6			5			5		ps/°C	
Pulse Width	PW	1000			100			40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			50			22			15	ns	Between any two units
Channel Matching												
Codirectional	t_{PSKCD}			50			3			3	ns	
Opposing-Direction	t_{PSKOD}			50			22			15	ns	
Output Rise/Fall Time	t_R/t_F		2.5			2.5			2.5		ns	10% to 90%

Table 23.

Parameter	Symbol	1 Mbps—WA Grade, WB Grade, and WC Grade Min	Typ	Max	10 Mbps—WB Grade and WC Grade Min	Typ	Max	25 Mbps—WC Grade Min	Typ	Max	Unit	Test Conditions/ Comments
SUPPLY CURRENT												
ADuM3200	I_{DD1}		0.8	1.3		2.0	3.2		4.3	6.4	mA	No load
	I_{DD2}		1.0	1.6		1.7	2.8		3.1	3.9	mA	No load
ADuM3201	I_{DD1}		0.7	1.3		1.5	2.1		3.0	4.2	mA	No load
	I_{DD2}		1.3	1.8		3.1	4.0		6.4	8.3	mA	No load

Table 24. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDX}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.3	0.5	mA	V_{IA} = V_{IB} = 0 V
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.5	0.6	mA	V_{IA} = V_{IB} = 0 V
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDX}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS

Table 25.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		1.0		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	$θ_{JCI}$		46		°C/W	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 2	$θ_{JCO}$		41		°C/W	

[1] The device is considered a 2-terminal device; Pin 1, Pin 2, Pin 3, and Pin 4 are shorted together, and Pin 5, Pin 6, Pin 7, and Pin 8 are shorted together.

REGULATORY INFORMATION

The ADuM3200/ADuM3201 devices are approved by the organizations listed in Table 26. Refer to Table 31 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 26.

UL	CSA	CQC	VDE
Recognized Under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Approved under CQC11-471543-2012	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12[2]
Single/Basic 2500 V rms Isolation Voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage, functional insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage	Basic insulation per GB4943.1-2011, 400 V rms (588 V peak) maximum working voltage, tropical climate, altitude ≤ 5000 meters	Reinforced insulation, 560 V peak
File E214100	File 205078	File CQC14001117250	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM3200/ADuM3201 is proof-tested by applying an insulation test voltage ≥3000 V rms for 1 second (current leakage detection limit = 5 μA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM3200/ADuM3201 is proof-tested by applying an insulation test voltage ≥1050 V peak for 1 second (partial discharge detection limit = 5 pC). An asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 27.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	4.90 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.01 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking on the package denotes DIN V VDE V 0884-10 approval for a 560 V peak working voltage.

Table 28.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	V_{PR}	1050	V peak
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC	V_{PR}		
After Environmental Tests Subgroup 1			896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		672	V peak
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 seconds	V_{TR}	4000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Case Temperature		T_S	150	°C
Side 1 Current		I_{S1}	160	mA
Side 2 Current		I_{S2}	170	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	>10^9	Ω

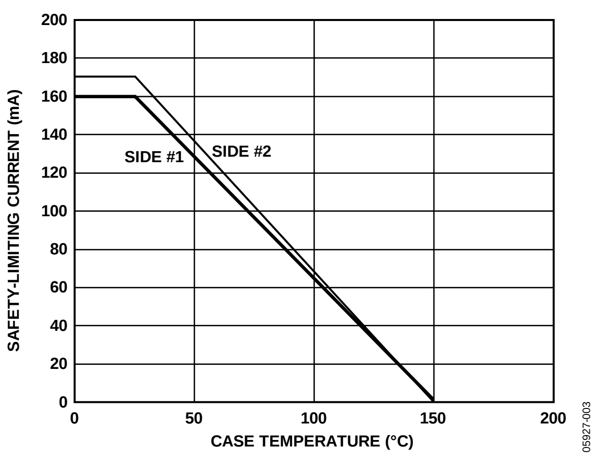


Figure 3. Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature, per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 29.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A			
ADuM3200A/ADuM3201A		−40	+105	°C
ADuM3200B/ADuM3201B		−40	+105	°C
ADuM3200C/ADuM3201C		−40	+105	°C
ADuM3200WA/ADuM3201WA		−40	+125	°C
ADuM3200WB/ADuM3201WB		−40	+125	°C
ADuM3200WC/ADuM3201WC		−40	+125	°C
Supply Voltages[1]	V_{DD1}, V_{DD2}			
ADuM3200A/ADuM3201A		3.0	5.5	V
ADuM3200B/ADuM3201B		3.0	5.5	V
ADuM3200C/ADuM3201C		3.0	5.5	V
ADuM3200WA/ADuM3201WA		3.0	5.5	V
ADuM3200WB/ADuM3201WB		3.0	5.5	V
ADuM3200WC/ADuM3201WC		3.0	5.5	V
Maximum Input Signal Rise and Fall Times			1.0	ms

[1] All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

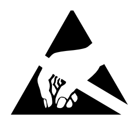
Table 30.

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Ambient Operating Temperature (T_A)	−40°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})[1]	−0.5 V to +7.0 V
Input Voltage (V_{IA}, V_{IB})[1, 2]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage (V_{OA}, V_{OB})[1, 2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current, per Pin (I_O)[3]	−22 mA to +22 mA
Common-Mode Transients (CM_L, CM_H)[4]	−100 kV/μs to +100 kV/μs

[1] All voltages are relative to their respective ground.
[2] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.
[3] See Figure 3 for maximum rated current values for various temperatures.
[4] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 31. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Functional Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Basic Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10
DC Voltage			
Functional Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Basic Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

Table 32. ADuM3200 Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	H	H	Outputs return to the input state within 1 μs of V_{DDI} power restoration.
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1 μs of V_{DDO} power restoration.

Table 33. ADuM3201 Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	Indeterminate	H	Outputs return to the input state within 1 μs of V_{DDI} power restoration.
X	X	Powered	Unpowered	H	Indeterminate	Outputs return to the input state within 1 μs of V_{DDO} power restoration.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

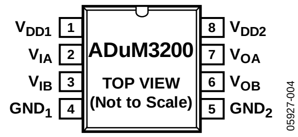


Figure 4. ADuM3200 Pin Configuration

Table 34. ADuM3200 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. Ground reference for Isolator Side 1.
5	GND_2	Ground 2. Ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

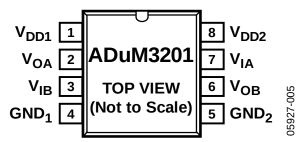


Figure 5. ADuM3201 Pin Configuration

Table 35. ADuM3201 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{OA}	Logic Output A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. Ground reference for Isolator Side 1.
5	GND_2	Ground 2. Ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{IA}	Logic Input A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

TYPICAL PERFORMANCE CHARACTERISTICS

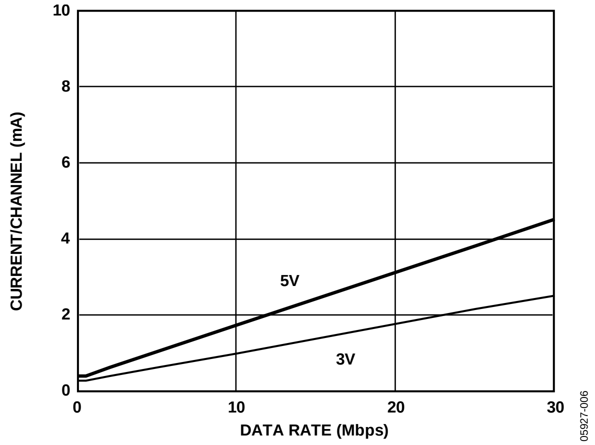


Figure 6. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation

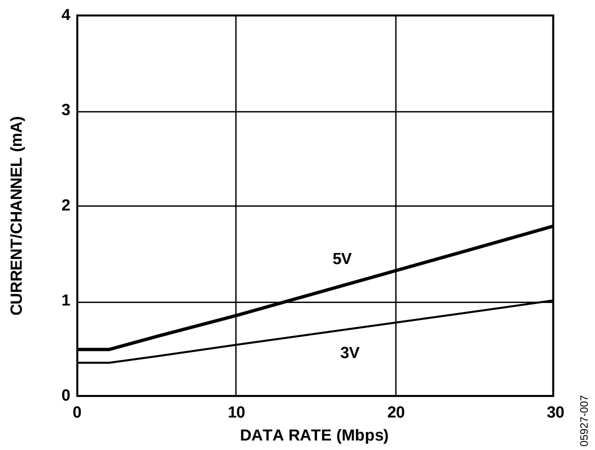


Figure 7. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

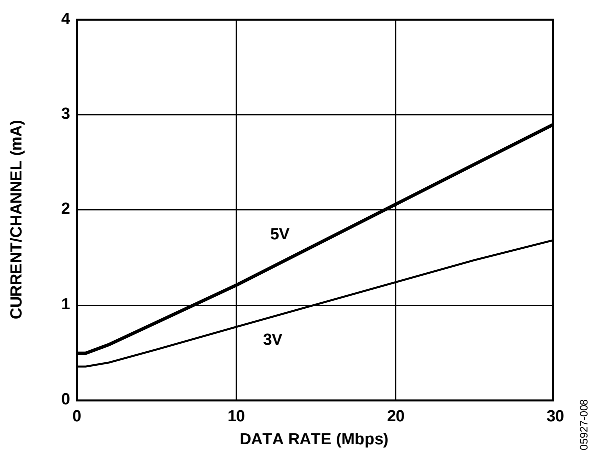


Figure 8. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

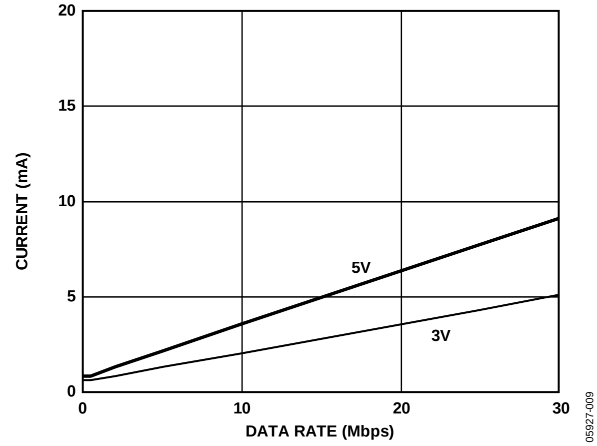


Figure 9. Typical ADuM3200 I_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

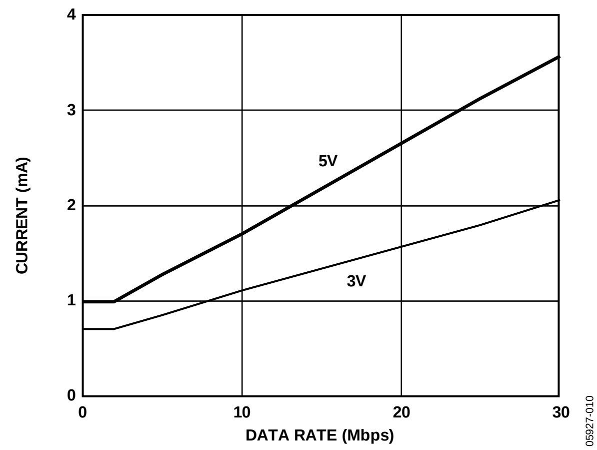


Figure 10. Typical ADuM3200 I_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

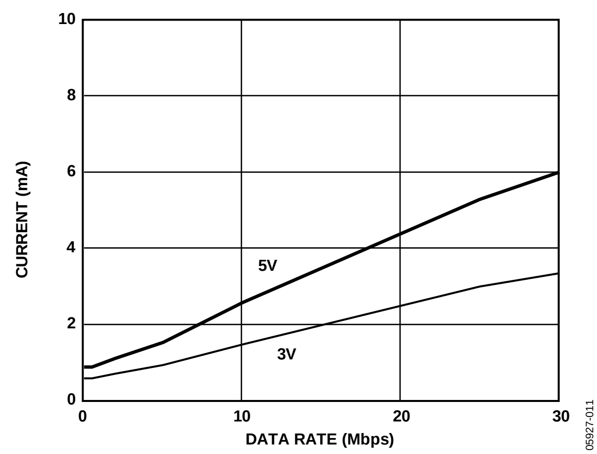


Figure 11. Typical ADuM3201 I_{DD1} or I_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

APPLICATION INFORMATION

PC BOARD LAYOUT

The ADuM3200/ADuM3201 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins. The capacitor value must be between 0.01 μF and 0.1 μF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 20 mm. See the AN-1109 Application Note for board layout guidelines.

SYSTEM-LEVEL ESD CONSIDERATIONS AND ENHANCEMENTS

System-level ESD reliability (for example, per IEC 61000-4-x) is highly dependent on system design which varies widely by application. The ADuM3200/ADuM3201 incorporate many enhancements to make ESD reliability less dependent on system design. The enhancements include:

- ESD protection cells added to all input/output interfaces.
- Key metal trace resistances reduced using wider geometry and paralleling of lines with vias.
- The SCR effect inherent in CMOS devices minimized by use of guarding and isolation technique between PMOS and NMOS devices.
- Areas of high electric field concentration eliminated using 45° corners on metal traces.
- Supply pin overvoltage prevented with larger ESD clamps between each supply pin and the respective ground.

While the ADuM3200/ADuM3201 improve system-level ESD reliability, they are no substitute for a robust system-level design. See the AN-793 Application Notes, *ESD/Latch-Up Considerations with iCoupler Isolation Product*, for detailed recommendations on board layout and system-level design.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high.

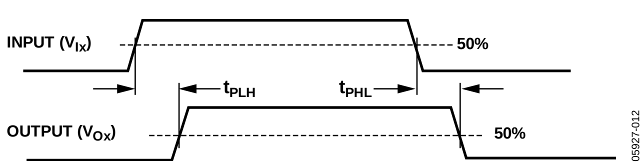


Figure 12. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal timing is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM3200/ADuM3201 component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM3200/ADuM3201 components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is therefore either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions of more than ~1 μs at the input, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than about 5 μs, the input side is assumed to be unpowered or nonfunctional, in which case, the isolator output is forced to a default state (see Table 32 and Table 33) by the watchdog timer circuit.

The ADuM3200/ADuM3201 are extremely immune to external magnetic fields. The limitation on the ADuM3200/ADuM3201 magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM3200/ADuM3201 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2,\ n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the nth turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM3200/ADuM3201 and an imposed requirement that the induced voltage is at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 13.

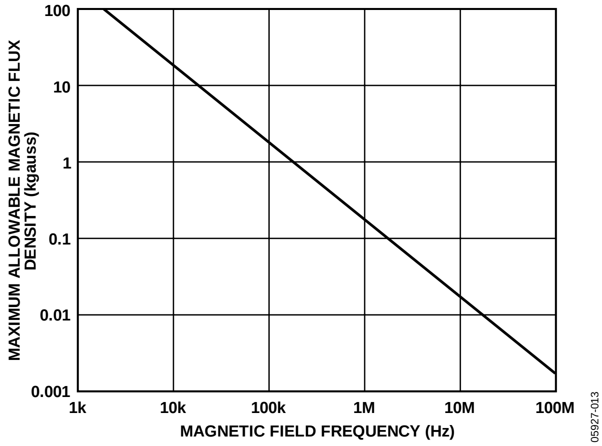


Figure 13. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and had the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM3200/ADuM3201 transformers. Figure 14 expresses these allowable current magnitudes as a function of frequency for selected distances. As seen, the ADuM3200/ADuM3201 are extremely immune and can be affected only by extremely large currents operated at high frequency and very close to the component. For the 1 MHz example, one must place a 0.5 kA current 5 mm away from the ADuM3200/ADuM3201 to affect the component operation.

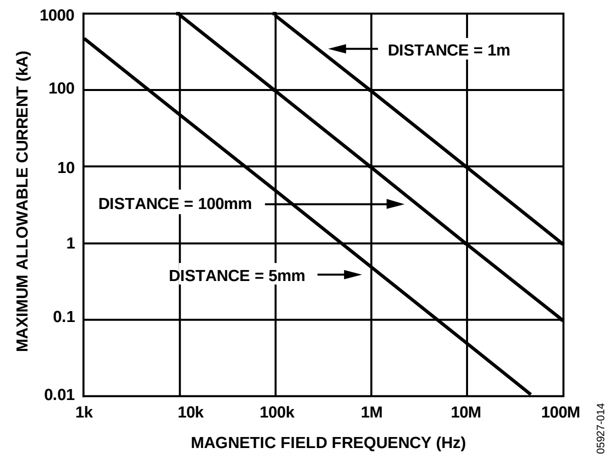


Figure 14. Maximum Allowable Current for Various Current-to-ADuM3200/ADuM3201 Spacings

Note that at combinations of strong magnetic fields and high frequencies, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the threshold of succeeding circuitry. Care must be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM3200/ ADuM3201 isolator is a function of the supply voltage, the channel data rate, and the channel output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \qquad f \le 0.5f_r$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)} \qquad f > 0.5f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO\,(Q)} \qquad f \le 0.5f_r$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10^{-3}) \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \qquad f > 0.5f_r$$

where:

$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
C_L is the output load capacitance (pF).
V_{DDO} is the output supply voltage (V).
f is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).
f_r is the input stage refresh rate (Mbps).
$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total I_{DD1} and I_{DD2} supply current, the supply currents for each input and output channel corresponding to I_{DD1} and I_{DD2} are calculated and totaled. Figure 6 provides per-channel input supply currents as a function of data rate.

Figure 7 and Figure 8 provide per-channel output supply currents as a function of data rate for an unloaded output condition and for a 15 pF output condition, respectively. Figure 9 through Figure 11 provide total I_{DD1} and I_{DD2} supply current as a function of data rate for ADuM3200 and ADuM3201 channel configurations.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation depends upon the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM3200/ADuM3201.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 31 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition, and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life.

The insulation lifetime of the ADuM3200/ADuM3201 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 15, Figure 16, and Figure 17 illustrate these different isolation voltage waveforms.

A bipolar ac voltage environment is the most stringent. The goal of a 50-year operating lifetime under the ac bipolar condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 31 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to either the unipolar ac or dc voltage cases. Any cross-insulation voltage waveform that does not conform to Figure 16 or Figure 17 must be treated as a bipolar ac waveform and the peak voltage must be limited to the 50-year lifetime voltage value listed in Table 31.

Note that the voltage presented in Figure 16 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

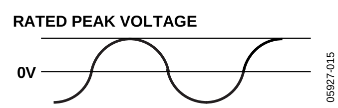


Figure 15. Bipolar AC Waveform

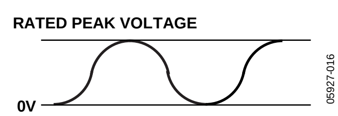


Figure 16. Unipolar AC Waveform

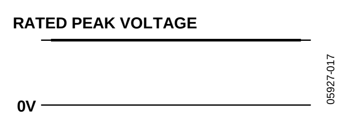


Figure 17. DC Waveform

OUTLINE DIMENSIONS

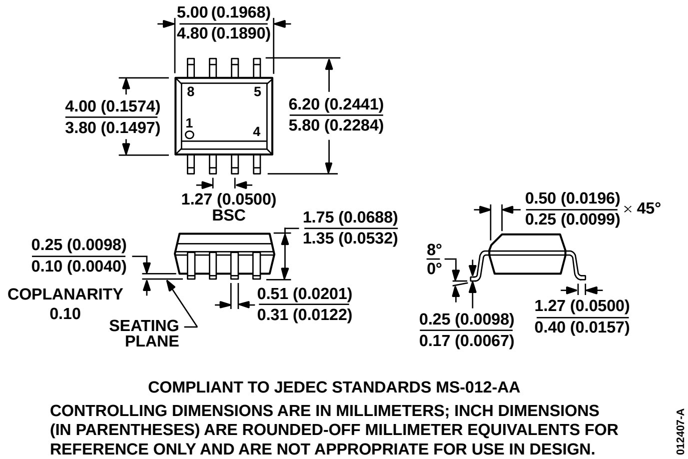


Figure 18. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters (inches)

ORDERING GUIDE

Model[1, 2]	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range (°C)	Package Description	Package Option
ADuM3200ARZ	2	0	1	150	40	−40 to +105	8-Lead SOIC_N	R-8
ADuM3200ARZ-RL7	2	0	1	150	40	−40 to +105	8-Lead SOIC_N	R-8
ADuM3200BRZ	2	0	10	50	3	−40 to +105	8-Lead SOIC_N	R-8
ADuM3200BRZ-RL7	2	0	10	50	3	−40 to +105	8-Lead SOIC_N	R-8
ADuM3200CRZ	2	0	25	45	3	−40 to +105	8-Lead SOIC_N	R-8
ADuM3200CRZ-RL7	2	0	25	45	3	−40 to +105	8-Lead SOIC_N	R-8
ADuM3200WARZ	2	0	1	150	40	−40 to +125	8-Lead SOIC_N	R-8
ADuM3200WARZ-RL7	2	0	1	150	40	−40 to +125	8-Lead SOIC_N	R-8
ADuM3200WBRZ	2	0	10	50	3	−40 to +125	8-Lead SOIC_N	R-8
ADuM3200WBRZ-RL7	2	0	10	50	3	−40 to +125	8-Lead SOIC_N	R-8
ADuM3200WCRZ	2	0	25	45	3	−40 to +125	8-Lead SOIC_N	R-8
ADuM3200WCRZ-RL7	2	0	25	45	3	−40 to +125	8-Lead SOIC_N	R-8
ADuM3201ARZ	1	1	1	150	40	−40 to +105	8-Lead SOIC_N	R-8
ADuM3201ARZ-RL7	1	1	1	150	40	−40 to +105	8-Lead SOIC_N	R-8
ADuM3201BRZ	1	1	10	50	3	−40 to +105	8-Lead SOIC_N	R-8
ADuM3201BRZ-RL7	1	1	10	50	3	−40 to +105	8-Lead SOIC_N	R-8
ADuM3201CRZ	1	1	25	45	3	−40 to +105	8-Lead SOIC_N	R-8
ADuM3201CRZ-RL7	1	1	25	45	3	−40 to +105	8-Lead SOIC_N	R-8
ADuM3201WARZ	1	1	1	150	40	−40 to +125	8-Lead SOIC_N	R-8
ADuM3201WARZ-RL7	1	1	1	150	40	−40 to +125	8-Lead SOIC_N	R-8
ADuM3201WBRZ	1	1	10	50	3	−40 to +125	8-Lead SOIC_N	R-8
ADuM3201WBRZ-RL7	1	1	10	50	3	−40 to +125	8-Lead SOIC_N	R-8
ADuM3201WCRZ	1	1	25	45	3	−40 to +125	8-Lead SOIC_N	R-8
ADuM3201WCRZ-RL7	1	1	25	45	3	−40 to +125	8-Lead SOIC_N	R-8

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADuM3200W/ADuM3201W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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