

FEATURES

Enhanced system-level ESD performance per IEC 61000-4-x

High temperature operation: 125°C

Narrow-body, RoHS compliant, 8-lead SOIC

Low power operation

5 V operation

1.7 mA per channel maximum at 0 Mbps to 1 Mbps

4.1 mA per channel maximum at 10 Mbps

8.6 mA per channel maximum at 25 Mbps

3.3 V operation

1.5 mA per channel maximum at 0 Mbps to 1 Mbps

2.5 mA per channel maximum at 10 Mbps

5.2 mA per channel maximum at 25 Mbps

High common-mode transient immunity: >25 kV/μs

Safety and regulatory approvals (pending)

UL recognition: 2500 V rms for 1 minute per UL 1577

CSA Component Acceptance Notice 5A

VDE certificate of conformity

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12

$V_{IORM} = 560 V_{PEAK}$

ENHANCED FEATURES

Supports defense and aerospace applications (AQEC standard)

Military temperature range (–55°C to +125°C)

Controlled manufacturing baseline

Enhanced product change notification

Qualification data available on request

APPLICATIONS

Size critical multichannel isolation

Serial peripheral interface (SPI)/data converter isolation

RS-232/RS-422/RS-485 transceiver isolation

Digital field bus isolation

Hybrid electric vehicles, battery monitors

GENERAL DESCRIPTION

The ADuM3200-EP/ADuM3201-EP¹ are dual-channel, digital isolators based on the Analog Devices, Inc., iCoupler® technology. Combining high speed CMOS and monolithic transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices.

The ADuM3200-EP/ADuM3201-EP isolators provide two independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide). They operate with 3.3 V or 5 V supply voltages on either side, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier.

In comparison to the ADuM1200-EP isolator, the ADuM3200-EP/ADuM3201-EP isolators contain various circuit and layout changes to provide increased capability relative to system-level IEC 61000-4-x testing (ESD, burst, and surge). The precise capability in these tests for either the ADuM1200-EP or ADuM3200-EP/ADuM3201-EP products is strongly determined by the design and layout of the board or module. For more information, see the AN-793 Application Note, *ESD/Latch-Up Considerations with iCoupler Isolation Products*.

For additional application and technical information, see the ADuM3200/ADuM3201 data sheet.

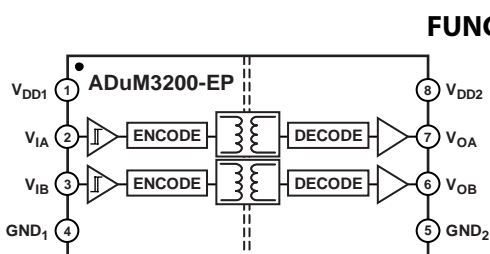


Figure 1. ADuM3200-EP Functional Block Diagram

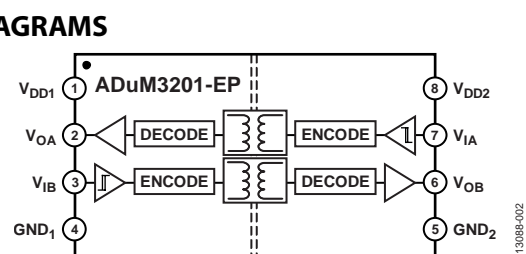


Figure 2. ADuM3201-EP Functional Block Diagram

¹ Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,329.

Rev. B

[Document Feedback](#)

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REVISION HISTORY

3/16—Rev. A to Rev. B

Changes to Logic High Output Voltages Parameter and Logic Low Output Parameter, Table 3	3
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8/15—Rev. 0 to Rev. A

Changed $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ to $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	Throughout
Changes to Logic High Output Voltages Parameter, Table 3	3
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5/15—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V, 125°C OPERATION

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 5\text{ V}$. Minimum/maximum specifications apply over the entire recommended operation range: $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$, and $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $C_L = 15\text{ pF}$ and CMOS signal levels, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	20		45	ns	50% input to 50% output
Pulse Width Distortion	PWD			3	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			5		ps/°C	
Pulse Width	PW	40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			15	ns	Between any two units
Channel Matching						
Codirectional	t_{PSKCD}			3	ns	
Opposing Direction	t_{PSKOD}			15	ns	
Output Rise/Fall Time	t_r/t_f		2.5		ns	10% to 90%

Table 2.

Parameter	Symbol	1 Mbps			10 Mbps			25 Mbps			Unit	Test Conditions/Comments
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT												
ADuM3200-EP	I_{DD1}	1.3	1.8		3.5	4.6		7.7	10.0		mA	No load
	I_{DD2}	1.0	1.6		2.0	2.8		3.8	4.9		mA	No load
ADuM3201-EP	I_{DD1}	1.1	1.6		3.1	4.2		6.8	8.9		mA	No load
	I_{DD2}	1.3	1.9		3.1	4.0		6.1	8.3		mA	No load

Table 3. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments	
DC SPECIFICATIONS							
Logic High Input Threshold	V_{IH}	$0.7 V_{DDx}$			V		
Logic Low Input Threshold	V_{IL}				$0.3 V_{DDx}$	V	
Logic High Output Voltages	V_{OH}	$V_{DDx} - 0.1$	V_{DDx}		V	$I_{Ox} = -20\ \mu\text{A}, V_{Ix} = V_{IxH}$	
		$V_{DDx} - 0.5$	$V_{DDx} - 0.2$		V	$I_{Ox} = -3.2\ \text{mA}, V_{Ix} = V_{IxH}$	
Logic Low Output Voltages	V_{OL}	0.0			0.1	V	$I_{Ox} = 20\ \mu\text{A}, V_{Ix} = V_{IxL}$
		0.2			0.4	V	$I_{Ox} = 3.2\ \text{mA}, V_{Ix} = V_{IxL}$
Input Current per Channel	I_i	-10	+0.01	+10	μA	$0\text{ V} \leq V_{Ix} \leq V_{DDx}$	
Supply Current per Channel							
Quiescent Input Supply Current	$I_{DD1(Q)}$	0.4			0.8	mA	$V_{IA} = V_{IB} = 0\text{ V}$
Quiescent Output Supply Current	$I_{DDO(Q)}$	0.5			0.6	mA	$V_{IA} = V_{IB} = 0\text{ V}$
Dynamic Input Supply Current	$I_{DD1(D)}$	0.19				mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$	0.05				mA/Mbps	
AC SPECIFICATIONS							
Common-Mode Transient Immunity ¹	$ CM $	25	35		kV/ μs	$V_{Ix} = V_{DDx}, V_{CM} = 1000\text{ V}$, transient magnitude = 800 V	
Refresh Rate	f_r	1.2				Mbps	

¹ $|CM|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{OUT} > 0.8 V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3.3 V, 125°C OPERATION

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 3.3\text{ V}$. Minimum/maximum specifications apply over the entire recommended operation range: $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$, and $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $C_L = 15\text{ pF}$ and CMOS signal levels, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	20		55	ns	50% input to 50% output
Pulse Width Distortion	PWD					
ADuM3200-EP				3	ns	$ t_{PLH} - t_{PHL} $
ADuM3201-EP				4	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			5		ps/°C	
Pulse Width	PW	40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			16	ns	Between any two units
Channel Matching						
Codirectional	t_{PSKCD}			3	ns	
Opposing Direction	t_{PSKOD}			16	ns	
Output Rise/Fall Time	t_R/t_F		3.0		ns	10% to 90%

Table 5.

Parameter	Symbol	1 Mbps			10 Mbps			25 Mbps			Unit	Test Conditions/Comments
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT												
ADuM3200-EP	I_{DD1}	0.8	1.3		2.2	3.2		4.8	6.4		mA	No load
	I_{DD2}	0.7	1.0		1.3	1.7		2.3	3.0		mA	No load
ADuM3201-EP	I_{DD1}	0.7	1.3		1.9	2.5		4.1	5.3		mA	No load
	I_{DD2}	0.8	1.6		1.9	2.5		3.7	5.1		mA	No load

Table 6. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	$0.7 V_{DDx}$			V	
Logic Low Input Threshold	V_{IL}				$0.3 V_{DDx}$	V
Logic High Output Voltages	V_{OH}	$V_{DDx} - 0.1$	V_{DDx}		V	$I_{Ox} = -20\ \mu\text{A}, V_{Ix} = V_{IxH}$
		$V_{DDx} - 0.5$	$V_{DDx} - 0.2$		V	$I_{Ox} = -3.2\ \text{mA}, V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OL}	0.0		0.1	V	$I_{Ox} = 20\ \mu\text{A}, V_{Ix} = V_{IxL}$
		0.2		0.4	V	$I_{Ox} = 3.2\ \text{mA}, V_{Ix} = V_{IxL}$
Input Current per Channel	I_i	-10	+0.01	+10	μA	$0\text{ V} \leq V_{Ix} \leq V_{DDx}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$	0.3		0.5	mA	$V_{IA} = V_{IB} = 0\text{ V}$
Quiescent Output Supply Current	$I_{DDO(Q)}$	0.3		0.5	mA	$V_{IA} = V_{IB} = 0\text{ V}$
Dynamic Input Supply Current	$I_{DDI(D)}$	0.10			mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$	0.03			mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity ¹	$ CM $	25	35		kV/ μs	$V_{Ix} = V_{DDx}, V_{CM} = 1000\text{ V}$, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	

¹ $|CM|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{OUT} > 0.8 V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V, 125°C OPERATION

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = 5\text{ V}$, $V_{DD2} = 3.3\text{ V}$. Minimum/maximum specifications apply over the entire recommended operation range: $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$, and $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $C_L = 15\text{ pF}$ and CMOS signal levels, unless otherwise noted.

Table 7.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	15		50	ns	50% input to 50% output
Pulse Width Distortion	PWD			3	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			5		ps/°C	
Pulse Width	PW	40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			15	ns	Between any two units
Channel Matching						
Codirectional	t_{PSKCD}			3	ns	
Opposing Direction	t_{PSKOD}			15	ns	
Output Rise/Fall Time	t_R/t_F		3.0		ns	10% to 90%

Table 8.

Parameter	Symbol	1 Mbps			10 Mbps			25 Mbps			Unit	Test Conditions/Comments
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT												
ADuM3200-EP	I_{DD1}	1.3	1.8		3.5	4.6		7.7	10.0		mA	No load
	I_{DD2}	0.7	1.0		1.3	1.7		2.3	3.0		mA	No load
ADuM3201-EP	I_{DD1}	1.1	1.6		3.1	4.2		6.8	8.9		mA	No load
	I_{DD2}	0.8	1.6		1.9	2.5		3.7	5.1		mA	No load

Table 9. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	$0.7 V_{DDx}$			V	
Logic Low Input Threshold	V_{IL}				V	
Logic High Output Voltages	V_{OH}	$V_{DDx} - 0.1$	V_{DDx}	$0.3 V_{DDx}$	V	$I_{Ox} = -20\ \mu\text{A}$, $V_{Ix} = V_{IxH}$
		$V_{DDx} - 0.5$	$V_{DDx} - 0.2$		V	$I_{Ox} = -3.2\ \text{mA}$, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OL}	0.0			V	$I_{Ox} = 20\ \mu\text{A}$, $V_{Ix} = V_{IxL}$
		0.2			V	$I_{Ox} = 3.2\ \text{mA}$, $V_{Ix} = V_{IxL}$
Input Current per Channel	I_i	-10	+0.01	+10	μA	$0\text{ V} \leq V_{Ix} \leq V_{DDx}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$	0.4			mA	$V_{IA} = V_{IB} = 0\text{ V}$
Quiescent Output Supply Current	$I_{DDO(Q)}$	0.3			mA	$V_{IA} = V_{IB} = 0\text{ V}$
Dynamic Input Supply Current	$I_{DDI(D)}$	0.19			mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$	0.03			mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity ¹	$ CM $	25	35		kV/ μs	$V_{Ix} = V_{DDx}$, $V_{CM} = 1000\text{ V}$, transient magnitude = 800 V
Refresh Rate	f_r	1.2			Mbps	

¹ $|CM|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{OUT} > 0.8 V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V, 125°C OPERATION

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = 3.3\text{ V}$, $V_{DD2} = 5.0\text{ V}$. Minimum/maximum specifications apply over the entire recommended operation range: $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$, and $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $C_L = 15\text{ pF}$ and CMOS signal levels, unless otherwise noted.

Table 10.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	15		50	ns	50% input to 50% output
Pulse Width Distortion	PWD					
ADuM3200-EP				3	ns	$ t_{PLH} - t_{PHL} $
ADuM3201-EP				4	ns	$ t_{PLH} - t_{PHL} $
Change vs. Temperature			5		ps/°C	
Pulse Width	PW	40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			15	ns	Between any two units
Channel Matching						
Codirectional	t_{PSKCD}			3	ns	
Opposing Direction	t_{PSKOD}			15	ns	
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%

Table 11.

Parameter	Symbol	1 Mbps			10 Mbps			25 Mbps			Unit	Test Conditions/Comments
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT												
ADuM3200-EP	I_{DD1}	0.8	1.3		2.2	3.2		4.8	6.4		mA	No load
	I_{DD2}	1.0	1.6		2.0	2.8		3.8	4.9		mA	No load
ADuM3201-EP	I_{DD1}	0.7	1.3		1.9	2.5		4.1	5.3		mA	No load
	I_{DD2}	1.3	1.9		3.1	4.0		6.1	8.3		mA	No load

Table 12. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	$0.7 V_{DDx}$			V	
Logic Low Input Threshold	V_{IL}				$0.3 V_{DDx}$	
Logic High Output Voltages	V_{OH}	$V_{DDx} - 0.1$	V_{DDx}		V	$I_{Ox} = -20\ \mu\text{A}$, $V_{Ix} = V_{IxH}$
		$V_{DDx} - 0.5$	$V_{DDx} - 0.2$		V	$I_{Ox} = -3.2\ \text{mA}$, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	$I_{Ox} = 20\ \mu\text{A}$, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	$I_{Ox} = 3.2\ \text{mA}$, $V_{Ix} = V_{IxL}$
Input Current per Channel	I_i	-10	+0.01	+10	μA	$0\text{ V} \leq V_{Ix} \leq V_{DDx}$
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.3	0.5	mA	$V_{IA} = V_{IB} = 0\text{ V}$
Quiescent Output Supply Current	$I_{DDO(Q)}$		0.5	0.6	mA	$V_{IA} = V_{IB} = 0\text{ V}$
Dynamic Input Supply Current	$I_{DDI(D)}$		0.10		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.05		mA/Mbps	
AC SPECIFICATIONS						
Common-Mode Transient Immunity ¹	$ CM $	25	35		kV/ μs	$V_{Ix} = V_{DDx}$, $V_{CM} = 1000\text{ V}$, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	

¹ $|CM|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{OUT} > 0.8 V_{DD}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS**Table 13.**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output) ¹	R _{I-O}		10 ¹²		Ω	
Capacitance (Input to Output) ¹	C _{I-O}		1.0		pF	f = 1 MHz
Input Capacitance	C _I		4.0		pF	
IC Junction to Case Thermal Resistance, Side 1	θ _{JCI}		46		°C/W	Thermocouple located at center of package underside
IC Junction to Case Thermal Resistance, Side 2	θ _{JCO}		41		°C/W	

¹ The device is considered a 2-terminal device; Pin 1, Pin 2, Pin 3, and Pin 4 are shorted together, and Pin 5, Pin 6, Pin 7, and Pin 8 are shorted together.

REGULATORY INFORMATION

The ADuM3200-EP/ADuM3201-EP devices are pending approval by the organizations listed in Table 14. Refer to Table 19 for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table 14.

UL (Pending)	CSA (Pending)	VDE (Pending)
Recognized Under UL 1577 Component Recognition Program ¹	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 ²
Single/Basic 2500 V rms Isolation Voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V _{PEAK}) maximum working voltage Functional insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V _{PEAK}) maximum working voltage	Reinforced insulation, 560 V _{PEAK}
File E214100	File 205078	File 2471900-4880-0001

¹ In accordance with UL 1577, each ADuM3200-EP/ADuM3201-EP is proof tested by applying an insulation test voltage ≥3000 V rms for 1 sec.

² In accordance with DIN V VDE V 0884-10, each ADuM3200-EP/ADuM3201-EP is proof tested by applying an insulation test voltage ≥1050 V_{PEAK} for 1 sec (partial discharge detection limit = 5 pC). An asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY RELATED SPECIFICATIONS**Table 15.**

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Tracking (Creepage)	L(I02)	4.0	mm min	Measured from input terminals to output terminals, shortest distance path along package body
Minimum External Air Gap (Clearance)	L(I01)	4.0	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L(PCB)	4.0 ¹	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		0.017	mm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material group (DIN VDE 0110, 1/89, Table 1)

¹ This value is for information only, to aid in PCB design. Package clearance is identical to creepage as specified in L(I02).

INSULATION CHARACTERISTICS (DIN V VDE V 0884-10 (VDE V 0884-10):2006-12)

These isolators are suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking on the package denotes DIN V VDE V 0884-10 approval for a 560 V_{PEAK} working voltage.

Table 16.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms			I to IV I to III I to II	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V _{IORM}	560	V _{PEAK}
Input to Output Test Voltage, Method B1	V _{IORM} × 1.875 = V _{PR} , 100% production test, t _m = 1 sec, partial discharge < 5 pC	V _{PR}	1050	V _{PEAK}
Input to Output Test Voltage, Method A After Environmental Tests Subgroup 1	V _{IORM} × 1.6 = V _{PR} , t _m = 60 sec, partial discharge < 5 pC	V _{PR}	896	V _{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V _{IORM} × 1.2 = V _{PR} , t _m = 60 sec, partial discharge < 5 pC		672	V _{PEAK}
Highest Allowable Overvoltage	Transient overvoltage, t _{TR} = 10 sec	V _{TR}	4000	V _{PEAK}
Surge Isolation Voltage	V _{PEAK} = 10 kV, 1.2 μs rise time, 50 μs, 50% fall time	V _{IOSM}	4000	V _{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Case Temperature		T _S	150	°C
Total Power Dissipation at 25°C		P _S	1.56	W
Insulation Resistance at T _S	V _{IO} = 500 V	R _S	>10 ⁹	Ω

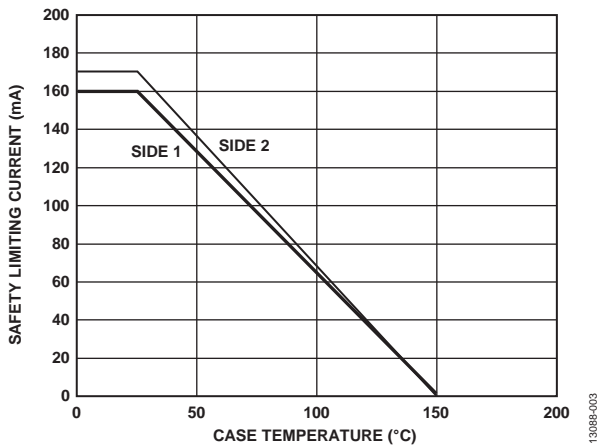


Figure 3. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 17.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Supply Voltages ¹	V _{DD1} , V _{DD2}	3.0	5.5	V
Maximum Input Signal Rise and Fall Times			1.0	ms
Start-Up Current	I _{DD1} , I _{DD2}	20		mA

¹ All voltages are relative to their respective ground.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 18.

Parameter	Rating
Storage Temperature (T_{ST})	-55°C to $+150^\circ\text{C}$
Ambient Operating Temperature (T_A)	-55°C to $+125^\circ\text{C}$
Supply Voltages (V_{DD1} , V_{DD2}) ¹	-0.5 V to $+7.0\text{ V}$
Input Voltages (V_{IA} , V_{IB}) ^{1,2}	-0.5 V to $V_{DD1} + 0.5\text{ V}$
Output Voltages (V_{OA} , V_{OB}) ^{1,2}	-0.5 V to $V_{DDO} + 0.5\text{ V}$
Average Output Current, per Pin (I_O) ³	-22 mA to $+22\text{ mA}$
Common-Mode Transients (CM_L , CM_H) ⁴	$-100\text{ kV}/\mu\text{s}$ to $+100\text{ kV}/\mu\text{s}$

¹ All voltages are relative to their respective ground.

² V_{DD1} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.

³ See Figure 3 for maximum rated current values for various temperatures.

⁴ Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 19. Maximum Continuous Working Voltage¹

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V_{PEAK}	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Functional Insulation	1131	V_{PEAK}	Maximum approved working voltage per IEC 60950-1
Basic Insulation	560	V_{PEAK}	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10
DC Voltage			
Functional Insulation	1131	V_{PEAK}	Maximum approved working voltage per IEC 60950-1
Basic Insulation	560	V_{PEAK}	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10

¹ Refers to continuous voltage magnitude imposed across the isolation barrier.

Table 20. ADuM3200-EP Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
High	High	Powered	Powered	High	High	
Low	Low	Powered	Powered	Low	Low	
High	Low	Powered	Powered	High	Low	
Low	High	Powered	Powered	Low	High	
X ¹	X ¹	Unpowered	Powered	High	High	Outputs return to the input state within 1 μs of V_{DD1} power restoration.
X ¹	X ¹	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1 μs of V_{DDO} power restoration.

¹ X means don't care.

Table 21. ADuM3201-EP Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
High	High	Powered	Powered	High	High	
Low	Low	Powered	Powered	Low	Low	
High	Low	Powered	Powered	High	Low	
Low	High	Powered	Powered	Low	High	
X ¹	X ¹	Unpowered	Powered	Indeterminate	High	Outputs return to the input state within 1 μs of V_{DD1} power restoration.
X ¹	X ¹	Powered	Unpowered	High	Indeterminate	Outputs return to the input state within 1 μs of V_{DDO} power restoration.

¹ X means don't care.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

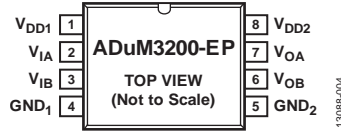


Figure 4. ADuM3200-EP Pin Configuration

Table 22. ADuM3200-EP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{DD1}	Supply Voltage for Isolator Side 1.
2	V _{IA}	Logic Input A.
3	V _{IB}	Logic Input B.
4	GND ₁	Ground 1. Ground reference for Isolator Side 1.
5	GND ₂	Ground 2. Ground reference for Isolator Side 2.
6	V _{OB}	Logic Output B.
7	V _{OA}	Logic Output A.
8	V _{DD2}	Supply Voltage for Isolator Side 2.

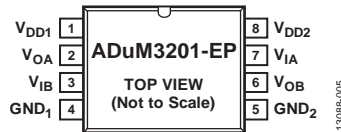


Figure 5. ADuM3201-EP Pin Configuration

Table 23. ADuM3201-EP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{DD1}	Supply Voltage for Isolator Side 1.
2	V _{OA}	Logic Output A.
3	V _{IB}	Logic Input B.
4	GND ₁	Ground 1. Ground reference for Isolator Side 1.
5	GND ₂	Ground 2. Ground reference for Isolator Side 2.
6	V _{OB}	Logic Output B.
7	V _{IA}	Logic Input A.
8	V _{DD2}	Supply Voltage for Isolator Side 2.

TYPICAL PERFORMANCE CHARACTERISTICS

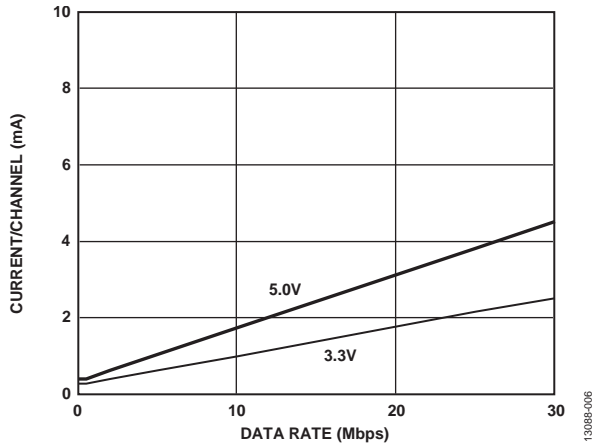


Figure 6. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3.3 V Operation

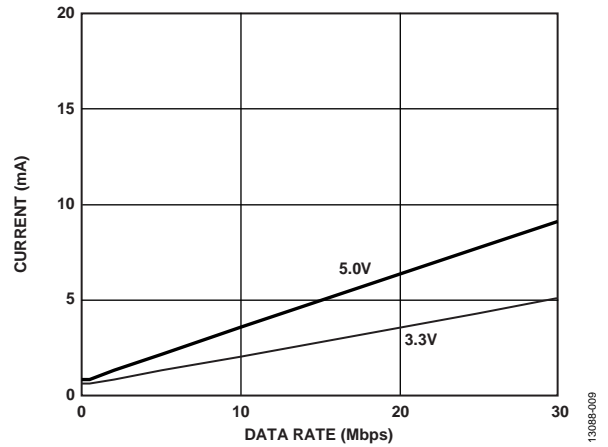


Figure 9. Typical ADuM3200-EP I_{DD1} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

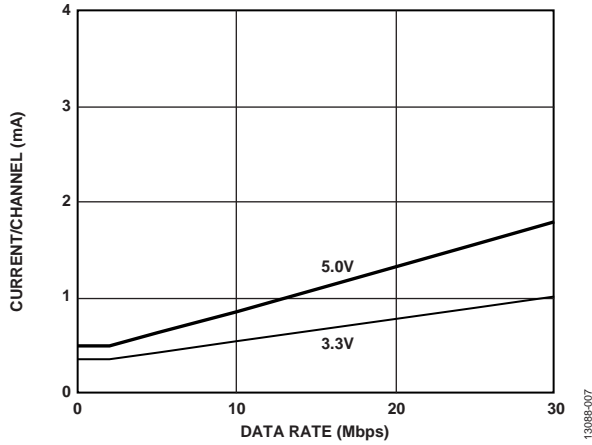


Figure 7. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3.3 V Operation (No Output Load)

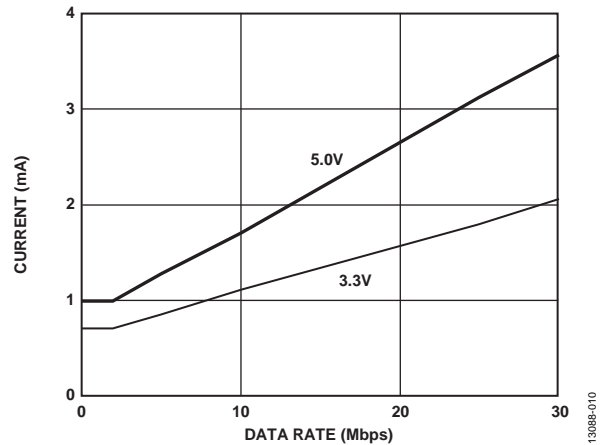


Figure 10. Typical ADuM3200-EP I_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

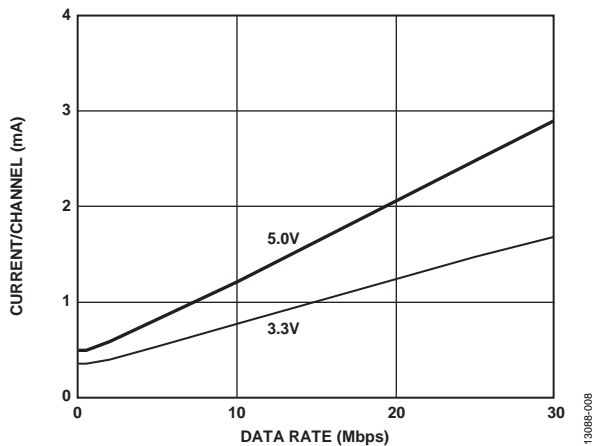


Figure 8. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3.3 V Operation (15 pF Output Load)

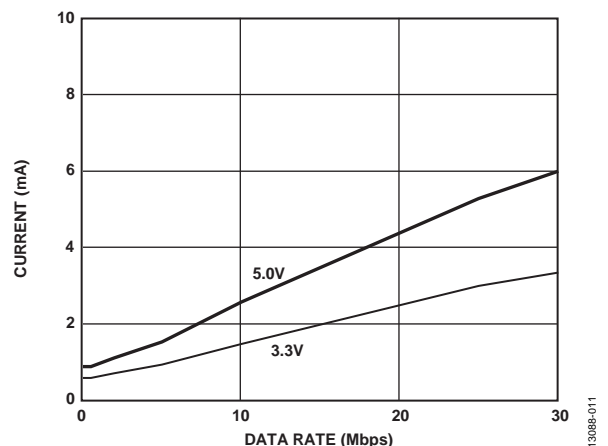
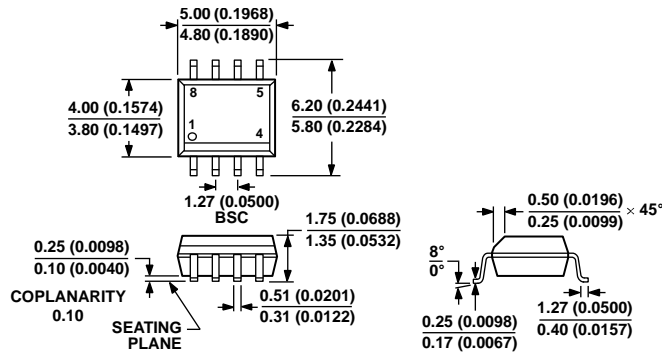


Figure 11. Typical ADuM3201-EP I_{DD1} or I_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 12. 8-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body (R-8)
 Dimensions shown in millimeters (inches)

ORDERING GUIDE

Model ¹	No. of Inputs, V _{DD1} Side	No. of Inputs, V _{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range	Package Description	Package Option
ADuM3200TRZ-EP	2	0	25	45	3	-55°C to +125°C	8-Lead SOIC_N	R-8
ADuM3200TRZ-EP-RL7	2	0	25	45	3	-55°C to +125°C	8-Lead SOIC_N	R-8
ADuM3201TRZ-EP	1	1	25	45	3	-55°C to +125°C	8-Lead SOIC_N	R-8
ADuM3201TRZ-EP-RL7	1	1	25	45	3	-55°C to +125°C	8-Lead SOIC_N	R-8

¹ Z = RoHS Compliant Part.

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