Single Gate, Adjustable Slew Rate, Isolated Gate Driver, 3 A Short-Circuit (<3 Ω)

Data Sheet

ADuM4122

FEATURES

- 2 A output current per output pin (<3 Ω R_{DSON_X})
- 3 A peak short-circuit current
- 3.3 V to 6.5 V, V_{DD1}
- 4.5 V to 35 V, V_{DD2}
- Positive going threshold, UVLO at 3.3 V V_{DD1}
- Multiple positive going thresholds, UVLO options on V_{DD2}
  - Grade A: 4.4 V (typical) positive going threshold, UVLO
  - Grade B: 7.3 V (typical) positive going threshold, UVLO
  - Grade C: 11.3 V (typical) positive going threshold, UVLO
- Precise timing characteristics
  - 48 ns maximum propagation delay for falling edge
- CMOS input logic levels
- High common-mode transient immunity: >150 kV/µs
- High junction temperature operation: 125°C
- Default low output
- Selectable slew rate control
- Safety and regulatory approvals (pending)
  - UL recognition per UL 1577
    - 5 kV rms for 1 minute
  - CSA Component Acceptance Notice 5A
  - VDE certificate of conformity (pending)
    - DIN V VDE V 0884-10
    - V_{IORM} = 849 V peak
- Wide-body, 8-lead SOIC_IC

APPLICATIONS

- Switching power supplies
- Isolated IGBT and MOSFET gate drivers
- Industrial inverters

GENERAL DESCRIPTION

The ADuM4122 is an isolated, single device, dual output driver that uses *i*Coupler® technology to provide precision isolation. The ADuM4122 provides 5 kV rms isolation in the wide-body, 8-lead SOIC package. These isolation components combine high speed complementary metal-oxide semiconductor (CMOS) and monolithic transformer technology to provide performance characteristics superior to alternatives (such as a combination of pulse transformers and gate drivers).

The ADuM4122 operates with an input supply voltage range from 3.3 V to 6.5 V, providing compatibility with lower voltage systems. Unlike gate drivers that employ high voltage level translation methodologies, the ADuM4122 offers true galvanic isolation between the input and the output regions.

The ADuM4122 includes two output pins that facilitate slew rate control of two output drive strengths. The V_{OUT} pin follows the logic of the V_{IN+} pin, while the boosting output, V_{OUT_SRC}, can be toggled to follow the V_{IN+} pin or to go high-Z. The toggling of the slew rate is controlled by the primary side. Slew rate control can allow for electromagnetic interference (EMI) mitigation and voltage overshoot control.

An internal thermal shutdown sets outputs low if internal temperatures on the ADuM4122 exceed the thermal shutdown temperature.

As a result, the ADuM4122 provides reliable control over the switching characteristics of insulated gate bipolar transistor (IGBT) and metal-oxide semiconductor field effect transistor (MOSFET) configurations over a wide range of switching voltages, allowing for simple slew rate control.

FUNCTIONAL BLOCK DIAGRAM

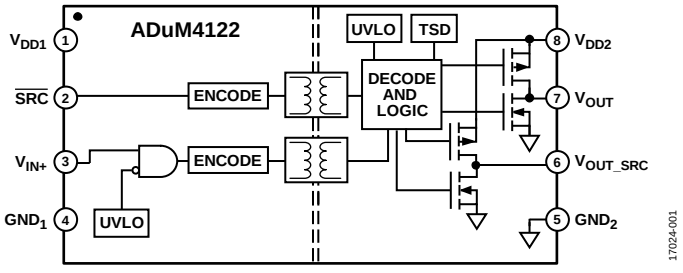

Figure 1.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,239. Other patents pending.

Rev. 0 Document Feedback

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REVISION HISTORY

2/2019—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

Low-side voltages are referenced to GND_1. High side voltages are referenced to GND_2: 3.3 V ≤ V_{DD1} ≤ 6.5 V, 4.5 V ≤ V_{DD2} ≤ 35 V, and T_J = −40°C to +125°C. All minimum and maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_J = 25°C, V_{DD1} = 5.0 V, and V_{DD2} = 15 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
High Side Power Supply						
V_{DD2} Input Voltage	V_{DD2}	4.5		35	V	
V_{DD2} Input Current, Quiescent	$I_{DD2(Q)}$		2	4	mA	Not switching
Logic Supply						
V_{DD1} Input Voltage	V_{DD1}	3.3		6.5	V	
Input Current	I_{DD1}		1.5	2.5	mA	V_{IN+} = low, $\overline{SRC}$ = high
	I_{DD1}		6	10	mA	V_{IN+} = low, $\overline{SRC}$ = low
	I_{DD1}		6	10	mA	V_{IN+} = high, $\overline{SRC}$ = high
	I_{DD1}		11	17	mA	V_{IN+} = high, $\overline{SRC}$ = low
V_{IN+} and $\overline{SRC}$ Logic Input						
V_{IN+} and $\overline{SRC}$ Input Current	I_{IN}	−1	+0.01	+1	µA	
Logic High Input Voltage	V_{IH}	0.7 × V_{DD1}			V	3.3 V ≤ V_{DD1} ≤ 5 V
		3.5			V	V_{DD1} > 5 V
Logic Low Input Voltage	V_{IL}			0.3 × V_{DD1}	V	3.3 V ≤ V_{DD1} ≤ 5 V
				1.5	V	V_{DD1} > 5 V
Undervoltage Lockout (UVLO)						
V_{DD1}						
Positive Going Threshold	$V_{VDD1UV+}$		3.2	3.3	V	
Negative Going Threshold	$V_{VDD1UV-}$	3.0	3.1		V	
Hysteresis	$V_{VDD1UVH}$		0.1		V	
V_{DD2}						
Grade A						
Positive Going Threshold	$V_{VDD2UV+}$		4.4	4.5	V	
Negative Going Threshold	$V_{VDD2UV-}$	4.1	4.2		V	
Hysteresis	$V_{VDD2UVH}$		0.2		V	
Grade B						
Positive Going Threshold	$V_{VDD2UV+}$		7.3	7.5	V	
Negative Going Threshold	$V_{VDD2UV-}$	6.9	7.1		V	
Hysteresis	$V_{VDD2UVH}$		0.2		V	
Grade C						
Positive Going Threshold	$V_{VDD2UV+}$		11.3	11.6	V	
Negative Going Threshold	$V_{VDD2UV-}$	10.8	11.1		V	
Hysteresis	$V_{VDD2UVH}$		0.2		V	
Thermal Shutdown (TSD)						
TSD Positive Edge	T_{TSD_POS}		155		°C	
TSD Hysteresis	T_{TSD_HYST}		30		°C	
V_{OUT} NMOS Gate Resistance[1]	R_{DSON_N}		1.1	2.3	Ω	Tested at 250 mA, V_{DD2} = 15 V
			1.1	2.3	Ω	Tested at 500 mA, V_{DD2} = 15 V
V_{OUT} PMOS Gate Resistance[1]	R_{DSON_P}		1.4	3	Ω	Tested at 250 mA, V_{DD2} = 15 V
			1.4	3	Ω	Tested at 500 mA, V_{DD2} = 15 V
V_{OUT_SRC} NMOS Gate Resistance	R_{DSON_N}		1.1	2.3	Ω	Tested at 250 mA, V_{DD2} = 15 V
			1.1	2.3	Ω	Tested at 500 mA, V_{DD2} = 15 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
V_{OUT_SRC} PMOS Gate Resistance	R_{DSON_P}		1.4	3	Ω	Tested at 250 mA, V_{DD2} = 15 V
			1.4	3	Ω	Tested at 500 mA, V_{DD2} = 15 V
Peak Current	I_{PK}		2		A	V_{DD2} = 12 V, 5 Ω gate resistance
Short-Circuit Peak Current Minimum	I_{SC_PK}		3		A	V_{DD2} = 5 V
SWITCHING SPECIFICATIONS						
Pulse Width	PW	50			ns	V_{DD1} = 5 V, V_{DD2} = 15 V
Propagation Delay[2]					ns	
Rising Edge	t_{DLH}	14	22	40	ns	V_{DD1} = 5 V, V_{DD2} = 15 V
Falling Edge	t_{DHL}	18	30	48	ns	V_{DD1} = 5 V, V_{DD2} = 15 V
Skew	t_{PSK}			36	ns	
Rising Edge	t_{PSKLH}			28	ns	
Falling Edge	t_{PSKHL}			30	ns	
Pulse Width Distortion	t_{PWD}		8	30	ns	V_{DD1} = 5 V, V_{DD2} = 15 V
Output Rise and Fall Time (20% to 80%)	t_R/t_F	8	17	25	ns	V_{DD1} = 5 V, V_{DD2} = 15 V, equivalent load capacitance (C_L) = 2.2 nF, on path external series resistance (R_{GON}) = off path external series resistance (R_{GOFF}) = 4.7 Ω
Required Time Before Next Edge	t_{NE}			100	ns	V_{DD1} = 5 V, V_{DD2} = 15 V
Common-Mode Transient Immunity (CMTI)	|CM|					
Static CMTI[3]		150			kV/µs	Common-mode voltage (V_{CM}) = 1500 V
Dynamic CMTI[4]		150			kV/µs	V_{CM} = 1500 V

[1] NMOS means N-type metal-oxide semiconductor and PMOS means P-type metal-oxide semiconductor.
[2] The t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH}, to the output rising 20% level of the V_{OUT} signal or the V_{OUT_SRC} signal. The t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL}, to the output falling 80% threshold of the V_{OUT} signal or the V_{OUT_SRC} signal. See Figure 29 for waveforms of propagation delay parameters.
[3] The static CMTI is defined as the largest dV/dt between GND_1 and GND_2, with inputs held either high or low, such that the output voltage remains either above 0.8 × V_{DD2} for output high or 0.8 V for output low. Operation with transients above recommended levels can cause momentary data upsets.
[4] The dynamic CMTI is defined as the largest dV/dt between GND_1 and GND_2, with the switching edge coincident with the transient test pulse. Operation with transients above the recommended levels can cause momentary data upsets.

REGULATORY INFORMATION

The ADuM4122 is pending approval by the organizations listed in Table 2.

Table 2.

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC (Pending)
UL1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	Certified under CQC11-471543-2012
Single Protection, 5000 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2:	Reinforced insulation, 849 V peak, V_{IOSM} = 10 kV peak	GB4943.1-2011
	Basic insulation at 800 V rms (1131 V peak)	Basic insulation 849 V peak, V_{IOSM} = 16 kV peak	Basic insulation at 800 V rms (1131 V peak)
	Reinforced insulation at 400 V rms (565 V peak)		Reinforced insulation at 400 V rms (565 V peak)
	IEC 60601-1 Edition 3.1:		
	Basic insulation 1 means of patient protection (1 MOPP), 500 V rms (707 V peak)		
	Reinforced insulation (2 MOPP), 250 V rms (1414 V peak)		
	CSA 61010-1-12 and IEC 61010-1 third edition		
	Basic insulation at: 600 V rms mains, 800 V secondary (1089 V peak)		
	Reinforced insulation at: 300 V rms mains, 400 V secondary (565 V peak)		
File E214100	File 205078	File 2471900-4880-0001	File (pending)

PACKAGE SPECIFICATIONS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input Side to High-Side Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input Side to High-Side Output)[1]	C_{I-O}		2.0		pF	
Input Capacitance	C_I		4.0		pF	

[1] The ADuM4122 is considered a 2-terminal device. Pin 1 through Pin 3 are shorted together, and Pin 4 through Pin 6 are shorted together.

INSULATION AND SAFETY SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		5000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	8 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L(PCB)	8.3 min	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the printed circuit board (PCB) mounting plane
Minimum Internal Gap (Internal Clearance)		25.5 min	µm	Minimum distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		I		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation within the safety limit data only. Maintenance of the safety data is ensured by protective circuits.

Table 5. VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 600 V rms			I to IV	
Climatic Classification[1]			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V peak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1274	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1019	V peak
Highest Allowable Overvoltage		V_{IOTM}	7000	V peak
Surge Isolation Voltage Basic	V peak = 16 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	16,000	V peak
Surge Isolation Voltage Reinforced	V peak = 16 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	10,000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Maximum Junction Temperature		T_S	150	°C
Safety Total Dissipated Power		P_S	1.52	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

[1] The climatic category indicates the climatic conditions under which the capacitor can be operated. According to IEC 60068-1, the climatic category is expressed by a three group coding, in this case, 40/105/21. The first group indicates the lower category temperature (−40°C). The second group indicates the upper category temperature (+105°C). The third group indicates the number of days (21) that the capacitor can withstand within specified limits if exposed to a relative humidity of 95% and a temperature of 40°C.

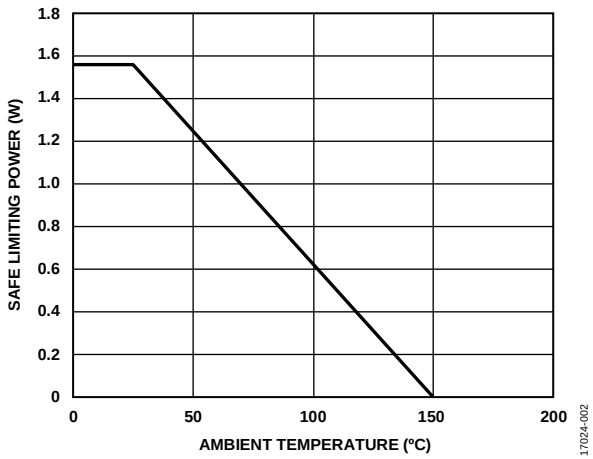

Figure 2. ADuM4122 Thermal Derating Curve, Dependence of Safety Limiting Values on Ambient Temperature, per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 6.

Parameter	Value
Operating Temperature Range (T_J)	−40°C to +125°C
Supply Voltages	
V_{DD1} to GND_1	3.3 V to 6.5 V
V_{DD2} to GND_2	4.5 V to 35 V

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted

Table 7.

Parameter	Rating
Storage Temperature Range (T_{ST})	−55°C to +150°C
Junction Operating Temperature Range (T_J)	−40°C to +150°C
Supply Voltages	
V_{DD1} to GND_1	−0.3 V to +7 V
V_{DD2} to GND_2	−0.3 V to +40 V
Input Voltages	
V_{IN+}[1]	−0.3 V to +7 V
$\overline{SRC}$[1]	−0.3 V to +7 V
Output Voltages	
V_{OUT}	−0.3 V to V_{DD2} + 0.3 V
V_{OUT_SRC}	−0.3 V to V_{DD2} + 0.3 V
Common-Mode Transients |CM|[2]	−200 kV/µs to +200 kV/µs

[1] Rating assumes V_{DD1} is greater than 3.3 V. V_{IN+} is rated up to 6.5 V when V_{DD1} is unpowered.
[2] |CM| refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to the PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient thermal resistance, and Ψ_{JT} is the junction to top characterization parameter.

Table 8. Thermal Resistance

Package Type[1]	θ_{JA}	Ψ_{JT}	Unit
RI-8-1	81.7	2.4	°C/W

[1] 4-layer PCB.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 9. Maximum Continuous Working Voltage[1]

Parameter	Rating	Constraint
AC Voltage		
Bipolar Waveform		
Basic Insulation	849 V peak	Lifetime limited by insulation lifetime, per VDE-0884-11
Reinforced Insulation	707 V peak	Lifetime limited by insulation lifetime, per VDE-0884-11
Unipolar Waveform		
Basic Insulation	1697 V peak	Lifetime limited by insulation lifetime, per VDE-0884-11
Reinforced Insulation	1356 V peak	Lifetime limited by package creepage, per IEC 60664-1
DC Voltage		
Basic Insulation	1660 V peak	Lifetime limited by package creepage, per IEC 60664-1
Reinforced Insulation	830 V peak	Lifetime limited by package creepage, per IEC 60664-1

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

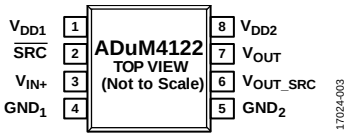

Figure 3. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 3.3 V to 6.5 V.
2	$\overline{SRC}$	Slew Rate Control Selection. Active logic low.
3	V_{IN+}	Noninverting Gate Drive Logic Input.
4	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V_{OUT_SRC}	Slew Rate Control Output. When $\overline{SRC}$ is low, V_{OUT_SRC} follows V_{IN+}. Connect this pin to the gate being driven through an external series resistor.
7	V_{OUT}	Gate Drive Output. Connect this pin to the gate being driven through an external series resistor.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

TRUTH TABLE

Table 11. Truth Table (Positive Logic)[1]

V_{IN+} Input	$\overline{SRC}$ Input	V_{DD1} State	V_{DD2} State	V_{OUT} Output	V_{OUT_SRC} Output
L	H	Powered	Powered	L	High-Z
L	L	Powered	Powered	L	L
H	H	Powered	Powered	H	High-Z
H	L	Powered	Powered	H	H
X	X	Unpowered	Powered	L	High-Z
X	X	Powered	Unpowered	High-Z	High-Z

[1] X means don't care, L means low, and H means high.

TYPICAL PERFORMANCE CHARACTERISTICS

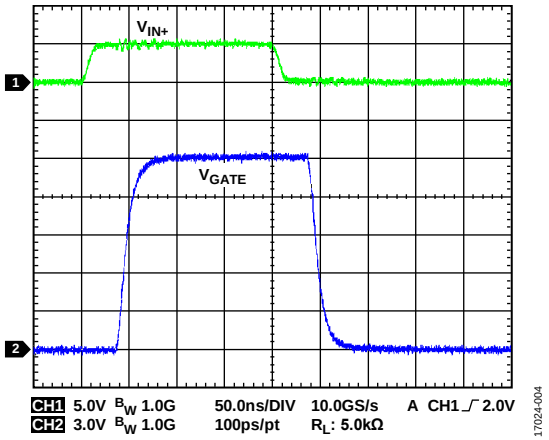

Figure 4. V_{IN+} to V_{GATE} Waveform, V_{DD1} = 5 V, V_{DD2} = 15 V, 10 Ω Gate Resistors, 2 nF Load, $\overline{SRC}$ Low

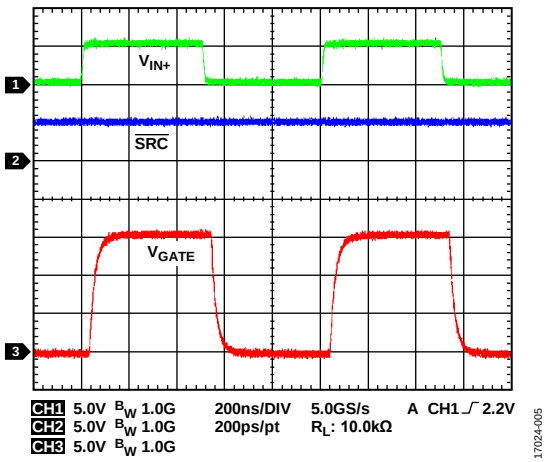

Figure 5. V_{IN+} to V_{GATE} Waveform, V_{DD1} = 5 V, V_{DD2} = 15 V, 10 Ω Gate Resistors, 2 nF Load, Both Edges Slow

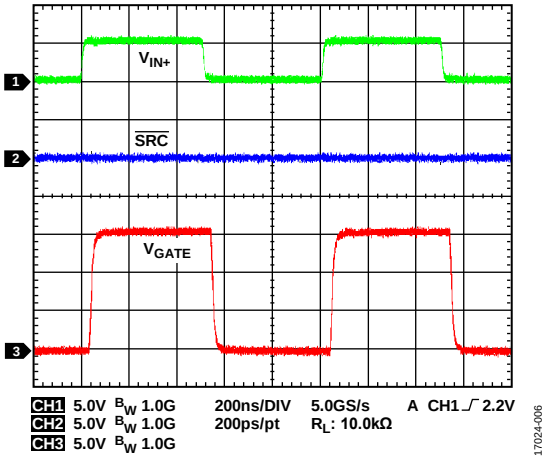

Figure 6. V_{IN+} to V_{GATE} Waveform, V_{DD1} = 5 V, V_{DD2} = 15 V, 10 Ω Gate Resistors, 2 nF Load, Both Edges Fast

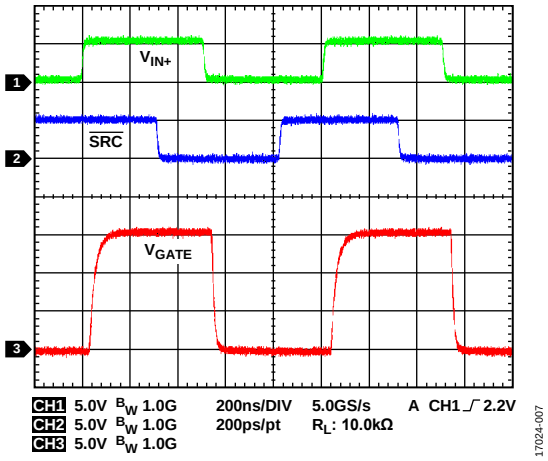

Figure 7. V_{IN+} to V_{GATE} Waveform, V_{DD1} = 5 V, V_{DD2} = 15 V, 10 Ω Gate Resistors, 2 nF Load, Falling Edge Fast

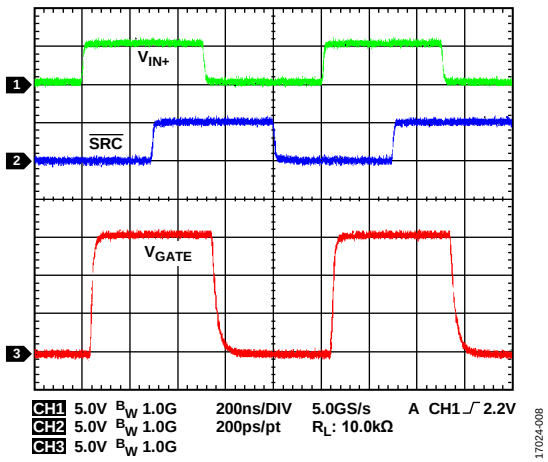

Figure 8. V_{IN+} to V_{GATE}, V_{DD1} = 5 V, V_{DD2} = 15 V, 10 Ω Gate Resistors, 2 nF Load, Rising Edge Fast

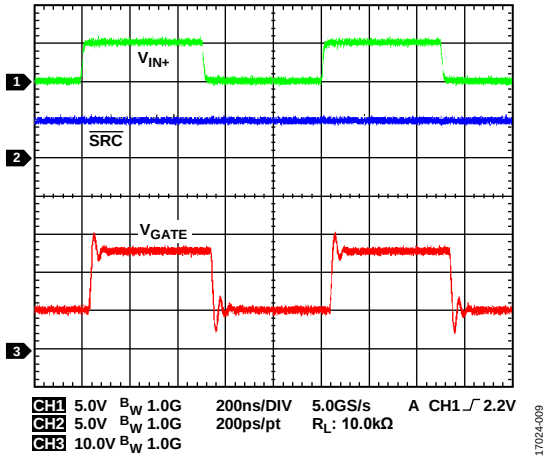

Figure 9. V_{IN+} to V_{GATE} Waveform, V_{DD1} = 5 V, V_{DD2} = 15 V, 0 Ω Gate Resistors, 2 nF Load, Both Edges Slow

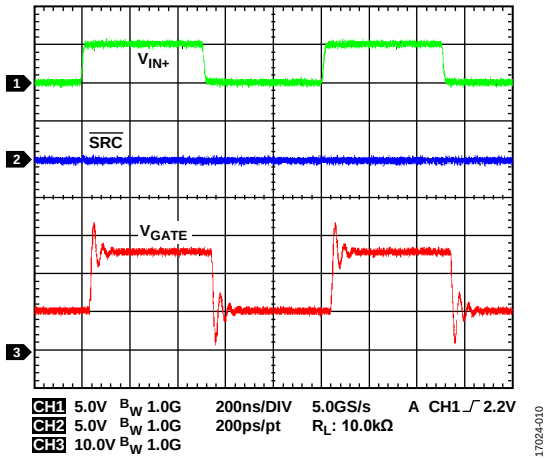

Figure 10. V_{IN+} to V_{GATE} Waveform, V_{DD1} = 5 V, V_{DD2} = 15 V, 0 Ω Gate Resistors, 2 nF Load, Both Edges Fast

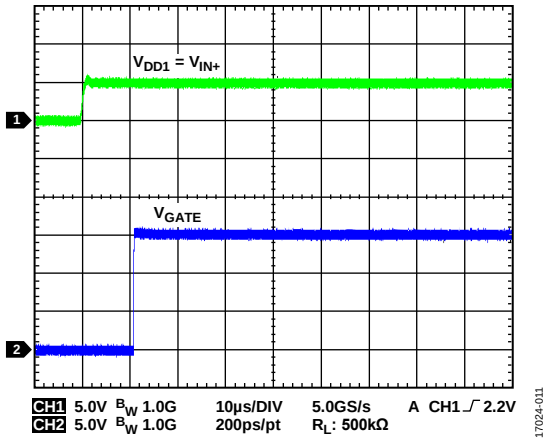

Figure 11. V_{DD1} to Output Valid, V_{DD2} = 15 V, 10 Ω Gate Resistors

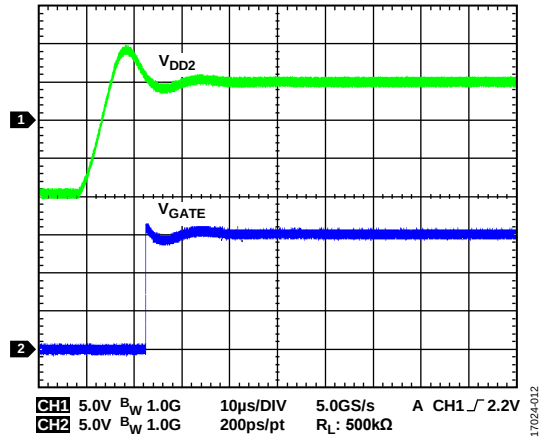

Figure 12. V_{DD2} to Output Valid, V_{DD1} = 5 V, 10 Ω Gate Resistors, 2 nF Load

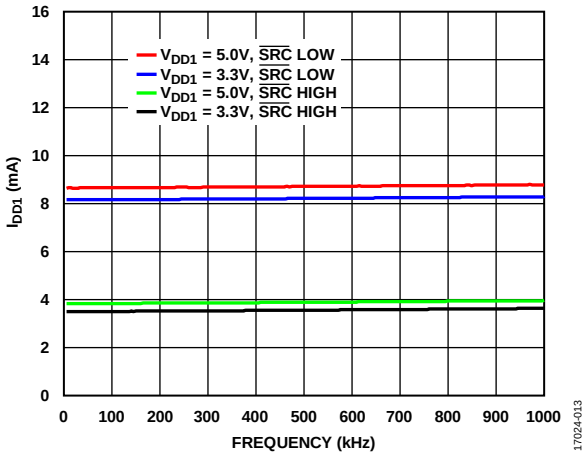

Figure 13. I_{DD1} vs. Frequency, 50% Duty Cycle

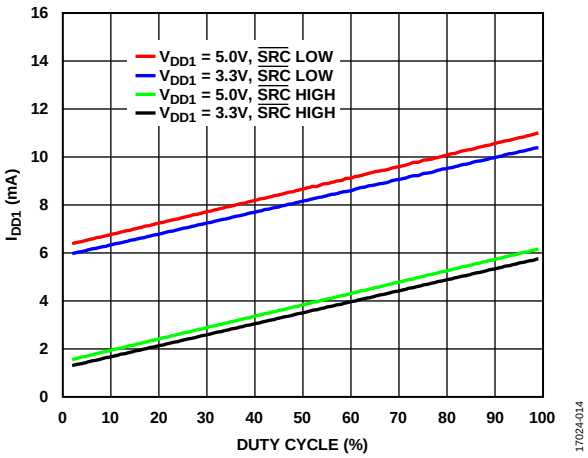

Figure 14. I_{DD1} vs. Duty Cycle, 10 kHz Input Signal

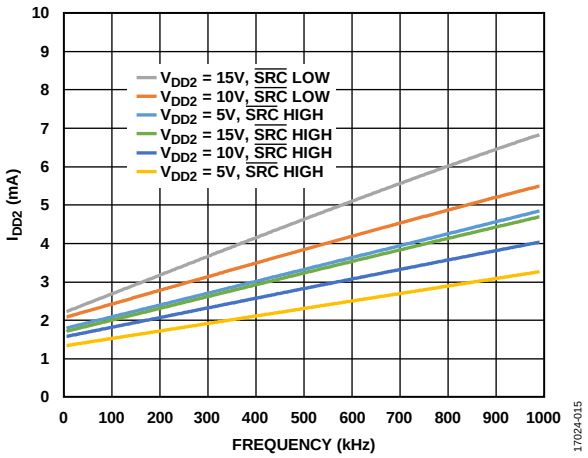

Figure 15. I_{DD2} vs. Frequency, 50% Duty Cycle, No Load

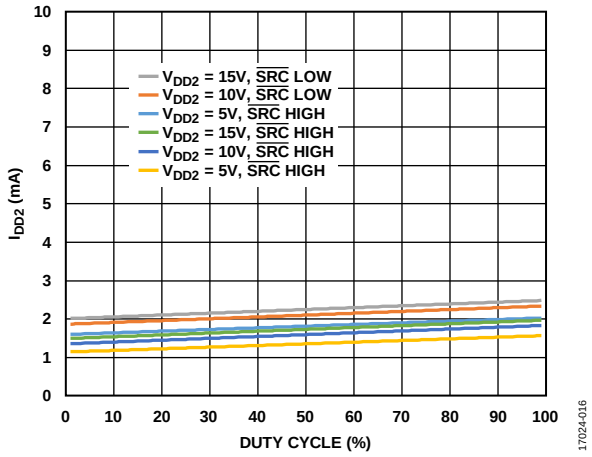

Figure 16. I_{DD2} vs. Duty Cycle, 10 kHz Input Signal, No Load

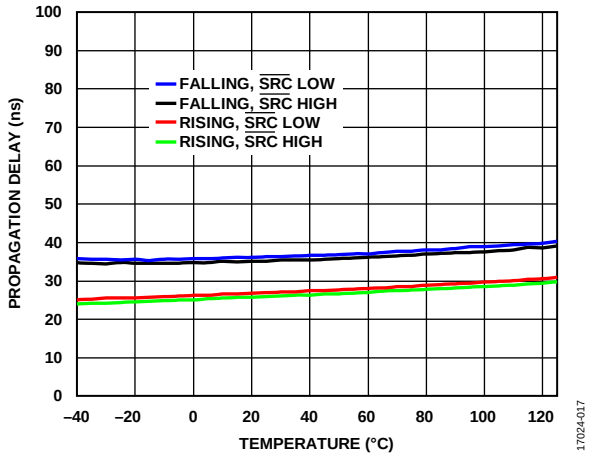

Figure 17. Propagation Delay vs. Temperature, V_{DD1} = 5 V, V_{DD2} = 15 V, 10 Ω Gate Resistors, 2 nF Load

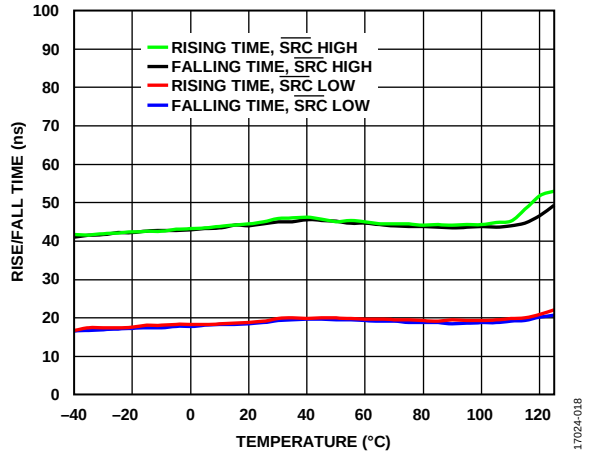

Figure 18. Rise/Fall Time vs. Temperature, V_{DD1} = 5 V, V_{DD2} = 15 V, 10 Ω Gate Resistors, 2 nF Load

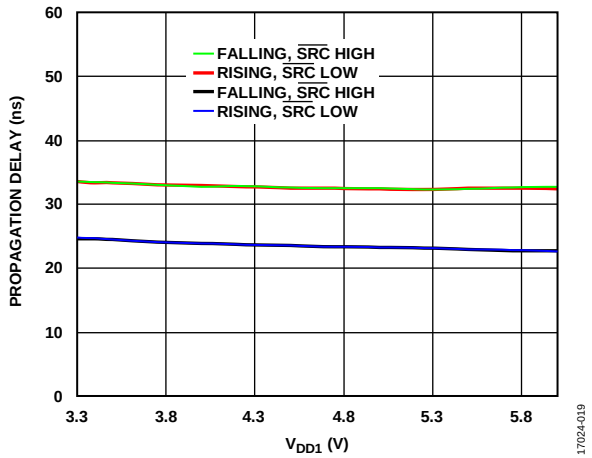

Figure 19. Propagation Delay vs. V_{DD1}, V_{DD2} = 15 V, 10 Ω Gate Resistors, 2 nF Load

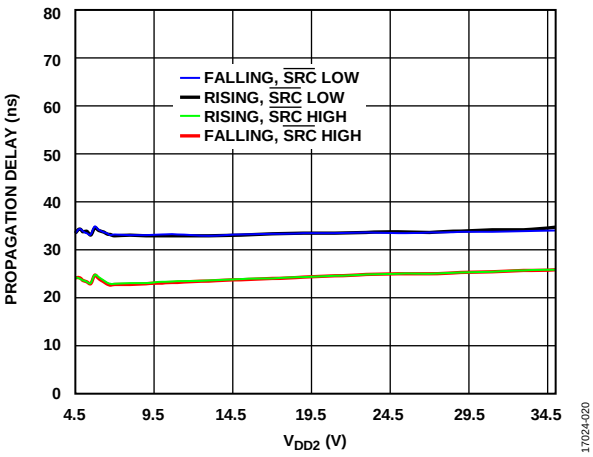

Figure 20. Propagation Delay vs. V_{DD2}, V_{DD1} = 5 V, 10 Ω Gate Resistors, 2 nF Load

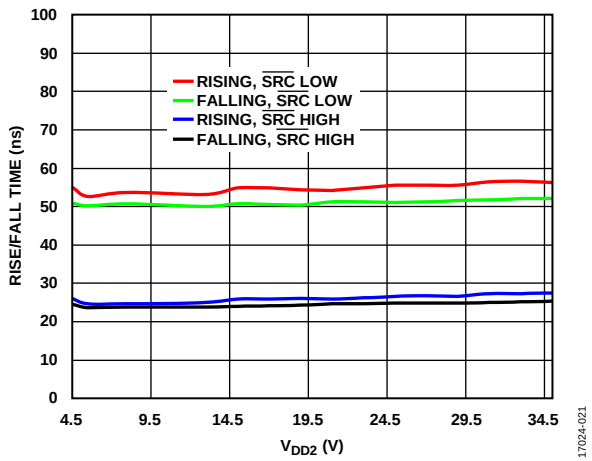

Figure 21. Rise/Fall Time vs. V_{DD2}, V_{DD1} = 5 V, 10 Ω Gate Resistors, 2 nF Load

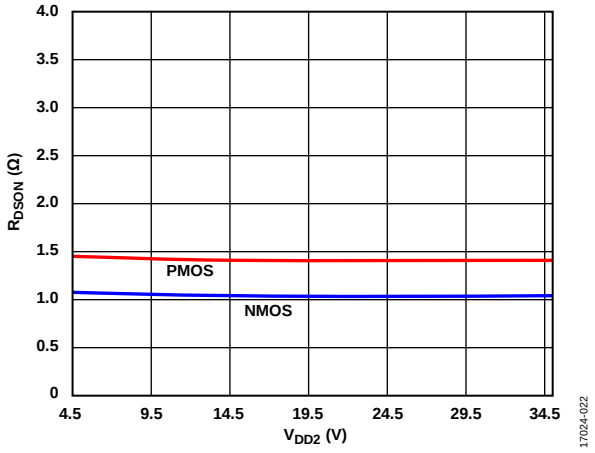

Figure 22. R_{DSON} vs. V_{DD2}, V_{OUT}

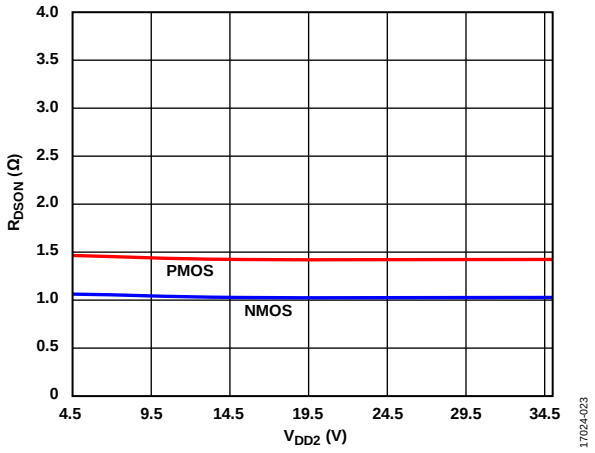

Figure 23. R_{DSON} vs. V_{DD2}, V_{OUT_SRC}

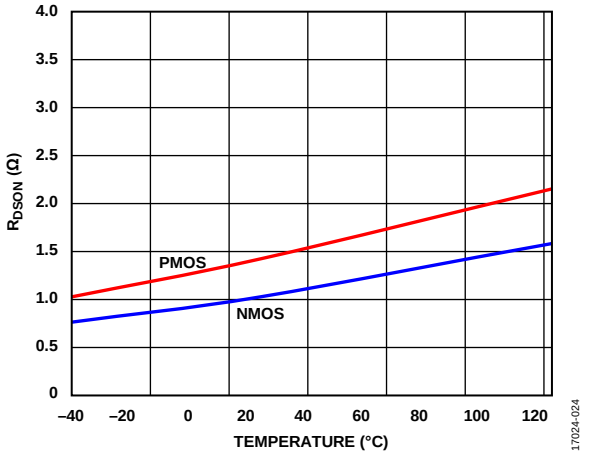

Figure 24. R_{DSON} vs. Temperature, V_{OUT}

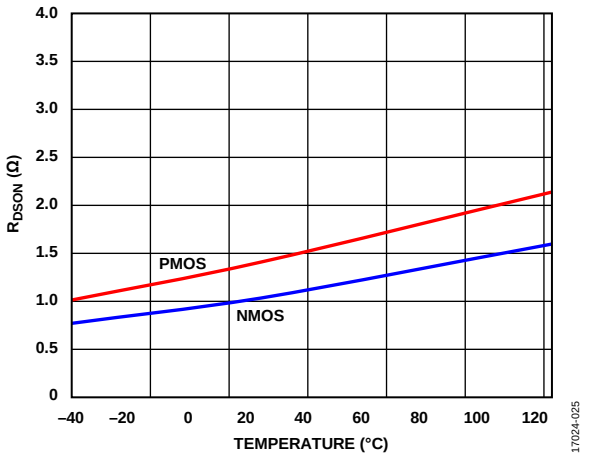

Figure 25. R_{DSON} vs. Temperature, V_{OUT_SRC}

THEORY OF OPERATION

Gate drivers are required in situations where fast rise times of switching device gates are desired. The gate signals for enhancement type power devices are referenced to a source or emitter node. The gate driver must be able to follow this source or emitter node. Because the gate driver must be able to follow this source or emitter node, isolation is necessary between the controlling signal and the output of the gate driver in topologies where the source or emitter nodes swing, such as a half bridge. Gate switching times are a function of the drive strength of the gate driver. Buffer stages before a CMOS output reduce total delay time and increase the final drive strength of the driver.

The ADuM4122 achieves isolation between the control side and the output side of the gate driver by using a high frequency carrier that transmits data across the isolation barrier with *i*Coupler chip scale transformer coils separated by layers of polyimide isolation. The ADuM4122 uses positive logic on/off keying (OOK) encoding, in which a high signal is transmitted by the presence of the carrier frequency across the *i*Coupler chip scale transformer coils. Positive logic encoding ensures that a low signal is seen on the output when the input side of the gate driver is unpowered. A low state is the most common safe state in enhancement mode power devices and can drive in situations where shoot-through conditions are present. The architecture of the ADuM4122 is designed for high CMTI and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and differential coil layout. Figure 26 shows the encoding used by the ADuM4122.

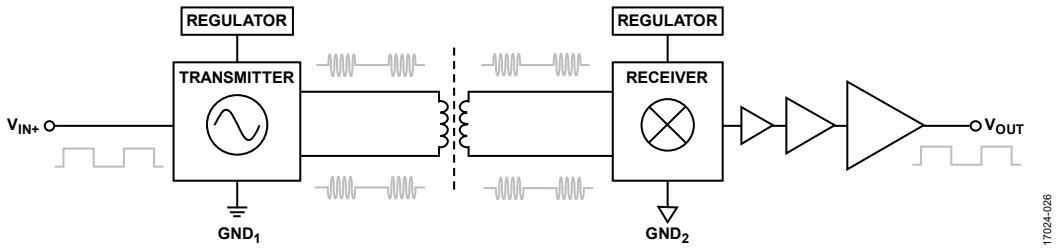

Figure 26. Operational Block Diagram of OOK Encoding

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM4122 isolated gate drivers require no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input supply pin and output supply pin, as shown in Figure 27. Use a small ceramic capacitor with a value between 0.01 µF and 0.1 µF to provide a high frequency bypass. It is recommended to also add a 10 µF capacitor to V_{DD2} to provide the charge required to drive the gate capacitance at the ADuM4122 outputs. On the V_{DD2}, avoid bypass capacitor use of vias or use multiple vias to reduce the inductance in bypassing. The total lead length between both ends of the smaller capacitor and the input supply pin or output power supply pin must not exceed 20 mm.

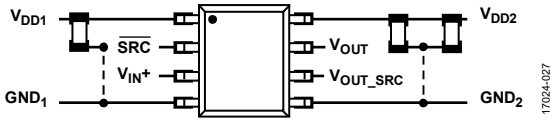

Figure 27. Recommended PCB Layout

SLEW RATE CONTROL

The ADuM4122 allows slew rate control that can be used by varying available turn on paths and turn off paths for the gate of the device being driven. The V_{OUT} pin reacts to the V_{IN+} pin with a propagation delay. The $\overline{SRC}$ pin controls whether the V_{OUT_SRC} pin is high impedance, or whether the V_{OUT_SRC} pin follows the input logic of the V_{IN+} pin. There is a delay in transition between the high impedance and gate driver output states. The V_{OUT_SRC} pin transitions between the two modes on the next outgoing edge of the V_{OUT} pin when a change in $\overline{SRC}$ occurs at least t_{NE} before the next edge of V_{IN+}. When $\overline{SRC}$ is high, the V_{OUT_SRC} pin is high impedance. When $\overline{SRC}$ is low, the V_{OUT_SRC} pin follows the positive logic on V_{IN+}, delayed by a propagation delay.

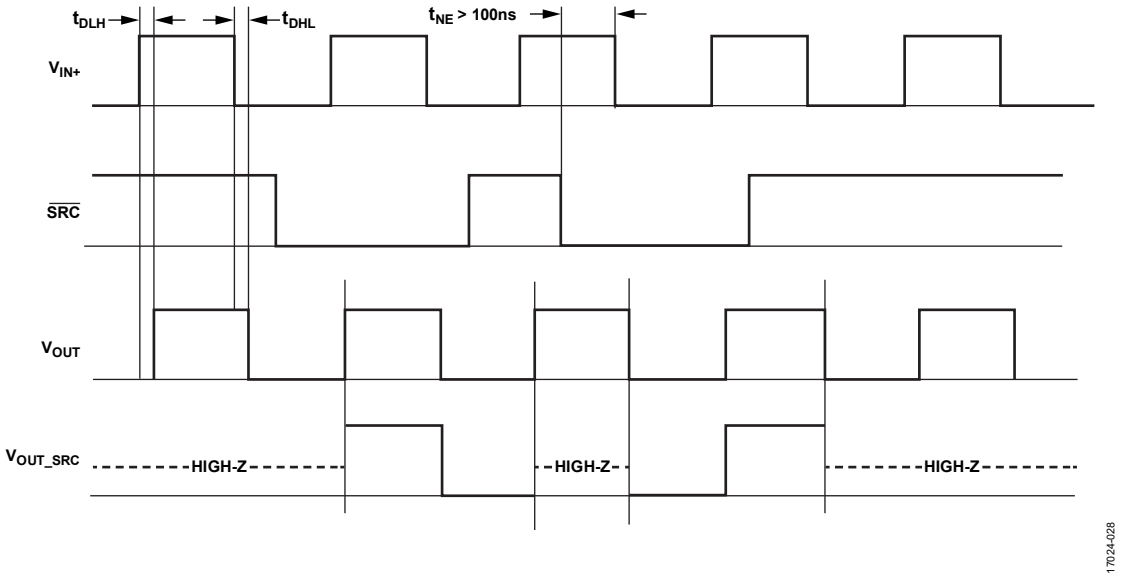

Figure 28. Example Timing Diagram

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time a logic signal takes to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output. The ADuM4122 specifies t_{DLH} as the time between the rising input high logic threshold (V_{IH}) to the output rising 20% threshold (see Figure 29). Likewise, t_{DHL} is defined as the time between the input falling logic low threshold (V_{IL}) and the output falling 80% threshold. The rise and fall times are dependent on the loading conditions and are not included in the propagation delay, as is the industry standard for gate drivers.

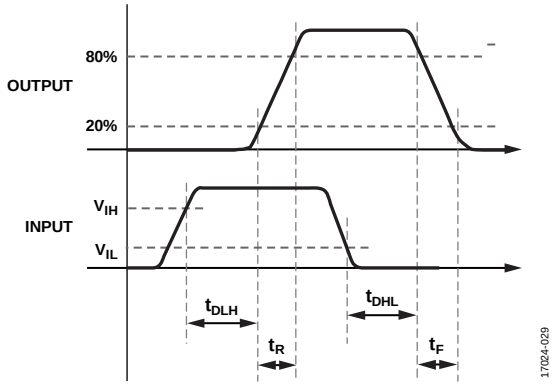

Figure 29. Propagation Delay Parameters

Channel to channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM4122 component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM4122 components operating under the same conditions.

PEAK CURRENT RATING

The ADuM4122 has two output channels to drive a single device gate. Each output channel is connected to the gate through an external series gate resistor to control drive strength and to spread the power dissipation of driving the gate to outside the gate driver IC. Although the output driver MOSFETs of the gate driver IC are able to source or sink more than 3 A (per V_{OUT} and V_{OUT_SRC}), this use case is rarely seen in application. Due to the size of standard external series gate resistors, it is common to see peak currents around 2 A in application. Figure 30 shows a short-circuit peak current graph for both the source and sink output driver MOSFETs of the ADuM4122.

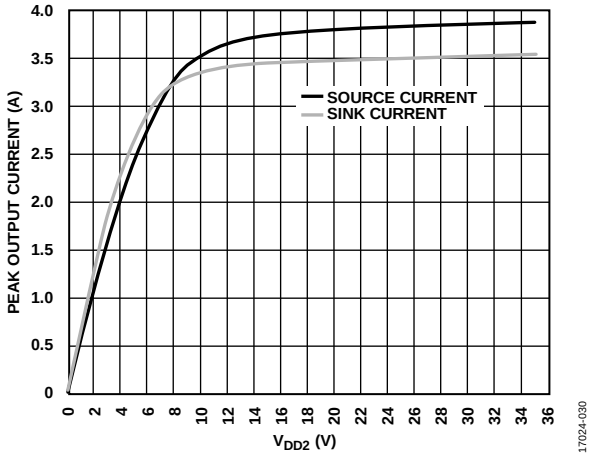

Figure 30. Source/Sink Short-Circuit Peak Currents (Simulation)

UNDERVOLTAGE LOCKOUT

The ADuM4122 has UVLO protections for both the primary and secondary side of the device. If either the primary or secondary side voltages are below the falling edge UVLO, the device outputs a low signal. After the ADuM4122 is powered so that it is greater than the rising edge UVLO threshold, the device outputs the signal found at the input. Hysteresis is built in to the UVLO to account for small voltage source ripple. The primary side UVLO thresholds for all ADuM4122 models are the same. The secondary output UVLO thresholds vary by model, as detailed in Table 12.

Table 12. List of Model Options

Model Number	UVLO (V)
ADuM4122ARIZ	4.5
ADuM4122BRIZ	7.5
ADuM4122CRIZ	11.6

OUTPUT LOAD CHARACTERISTICS

The ADuM4122 output signals depend on the characteristics of the output load, which is typically an N-channel MOSFET. Model the driver output response to an N-channel MOSFET load with a switch output resistance (R_{SW}), an inductance due to the PCB trace (L_{TRACE}), a series gate resistor (R_{GATE}), and a gate to source capacitance (C_{GS}), as shown in Figure 31.

R_{SW} is the switch resistance of the internal ADuM4122 driver output, which is less than 3 Ω. R_{GATE} is the intrinsic gate resistance of the MOSFET or IGBT and any external series resistance. A MOSFET or IGBT that requires a 2 A gate driver has a typical intrinsic gate resistance of about 1 Ω, and a C_{GS} of 2 nF to 10 nF. L_{TRACE} is the inductance of the PCB trace and typically has a value of <5 nH for a well designed layout with a very short, wide connection from the ADuM4122 output to the gate of the MOSFET or IGBT.

The following equation defines the quality factor (Q) of the resistor, inductor, and capacitor (RLC) circuit, which indicates how the ADuM4122 output responds to a step change. For a well damped output, Q is less than one. Adding a series gate resistance dampens the output response.

$$Q = \frac{1}{(R_{SW} + R_{GATE})} \times \sqrt{\frac{L_{TRACE}}{C_{GS}}}$$

Output ringing is reduced by adding a series gate resistance to dampen the response. The waveform shown in Figure 6 shows a correctly damped example with a 2 nF load and 10 Ω external series gate resistors. The waveform shown in Figure 10 shows an underdamped example with a 2 nF load and 0 Ω external series gate resistors.

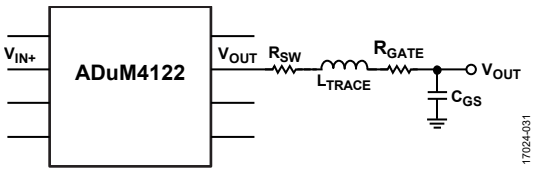

Figure 31. RLC Model of the Gate of an N-Channel MOSFET

POWER DISSIPATION

When driving a MOSFET or IGBT gate, the driver must dissipate power. This power is not insignificant and can lead to TSD if considerations are not made. The gate of an IGBT can be approximately simulated as a capacitive load. Due to Miller capacitance and other nonlinearities, it is common practice to take the stated input capacitance of a given MOSFET or IGBT (C_{ISS}) and multiply that by a factor of 3 to 5 to arrive at a conservative estimate of the approximate load being driven. The estimated total power dissipation in the system due to switching action is given by the following equation:

$$P_{DISS} = C_{EST} \times (V_{DD2} - GND_2)^2 \times f_{SW}$$

where:
P_{DISS} is power dissipation.
$C_{EST} = C_{ISS} \times 5$.
f_{SW} is the switching frequency of the IGBT.

Alternately, the gate charge can be used as follows:

$$P_{DISS} = Q_G \times (V_{DD2} - GND_2) \times f_{SW}$$

where Q_G is the total gate charge of the device being driven.

This power dissipation is shared between the internal on resistances of the internal gate driver switches, and the external gate resistances, R_{GON} and R_{GOFF}. The ratio of the internal gate resistances to the total series resistance allows the calculation of losses seen within the ADuM4122 device.

$$P_{DISS\_ADuM4122} = P_{DISS} \times 0.5(R_{DSON\_P}/(R_{GON} + R_{DSON\_P}) + 0.5(R_{DSON\_N}/(R_{GOFF} + R_{DSON\_N}))$$

where:
R_{DSON_P} is the internal resistance of the turn off path.
R_{DSON_N} is the internal resistance of the turn on path.

Multiplying the power dissipation found inside the chip by the θ_{JA} gives the rise above ambient temperature that the ADuM4122 experiences.

$$T_{ADuM4122} = \theta_{JA} \times P_{DISS\_ADuM4122} + T_A$$

where:
$T_{ADuM4122}$ is the internal temperature of the ADuM4122.
$P_{DISS\_ADuM4122}$ is the power dissipated inside the ADuM4122.
T_A is the ambient temperature the device is operating in.

For the device to remain within specification, $T_{ADUM4122}$ must not exceed 125°C. If $T_{ADuM4122}$ exceeds the TSD rising edge, the device enters TSD and the output remains low until the TSD falling edge is crossed.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by regulatory agencies, Analog Devices, Inc. carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM4122.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 9 summarize the peak voltage for 20 years of service life for a bipolar ac operating condition, and the maximum CSA and VDE approved working voltages. In many cases, the approved working voltage is higher than the 20-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM4122 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 32, Figure 33, and Figure 34 illustrate these different isolation voltage waveforms.

A bipolar ac voltage environment is the worst condition for *i*Coupler products and is the 20-year operating lifetime that Analog Devices recommends for maximum working voltage. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. Unipolar ac or dc voltage operation allows operation at higher working voltages while still achieving a 20-year service life. Any cross insulation voltage waveform that does not conform to Figure 33 or Figure 34 must be treated as a bipolar ac waveform, and its peak voltage must be limited to the 20-year lifetime voltage value listed in Table 9.

The voltage presented in Figure 33 is shown as sinusoidal for illustration purposes only. This voltage is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

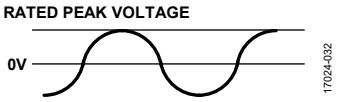

Figure 32. Bipolar AC Waveform

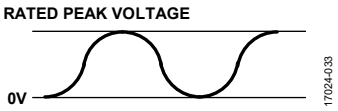

Figure 33. Unipolar AC Waveform

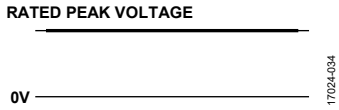

Figure 34. DC Waveform

TYPICAL APPLICATIONS

A typical application of the ADuM4122 is shown in Figure 35. Regular drive strength is dictated by the external series gate resistor, R_{G1}. When the $\overline{SRC}$ pin is held low, there is a second charge and discharge path available through the external series gate resistor, R_{G2}, providing higher drive strength to the gate of the power device. When the $\overline{SRC}$ pin is held high, the V_{OUT_SRC} output goes in to a high impedance mode so that the only charge and discharge path is through R_{G1}.

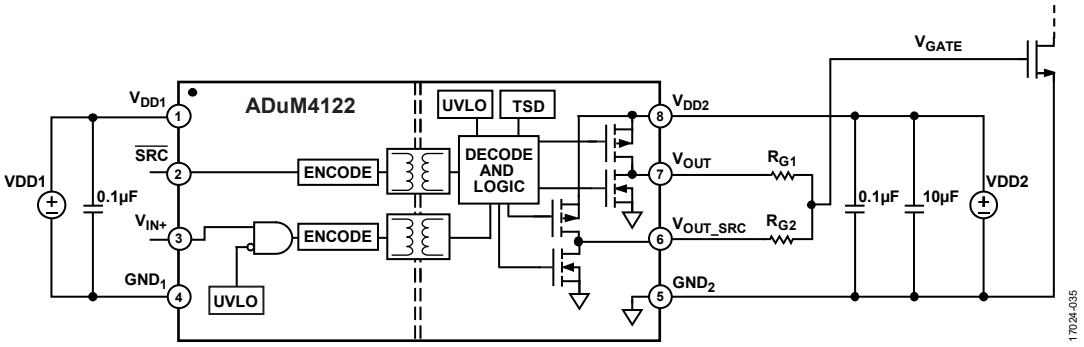

Figure 35. Typical Application

OUTLINE DIMENSIONS

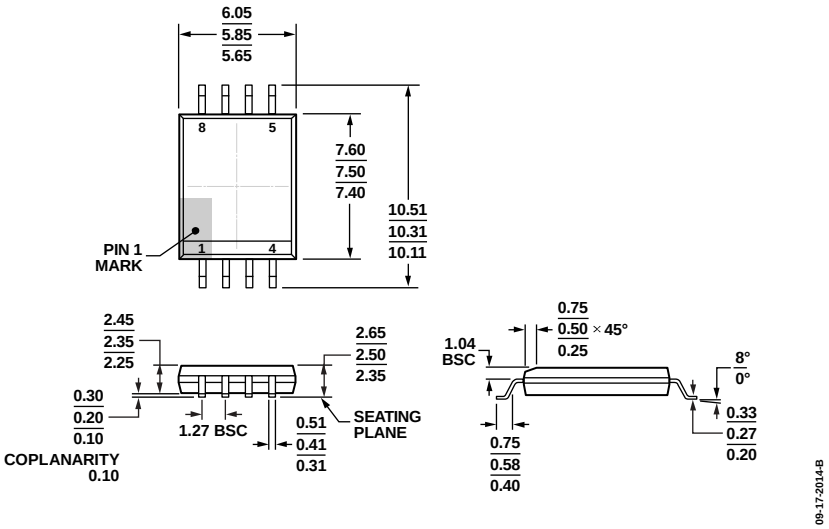

Figure 36. 8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]
Wide Body
(RI-8-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	No. of Channels	Output Peak Current (A)	Minimum Output Voltage (V)	Temperature Range	Package Description	Package Option
ADuM4122ARIZ	1	2	4.5	−40°C to +125°C	8-Lead SOIC_IC	RI-8-1
ADuM4122ARIZ-RL	1	2	4.5	−40°C to +125°C	8-Lead SOIC_IC, 13″ Tape and Reel	RI-8-1
ADuM4122BRIZ	1	2	7.5	−40°C to +125°C	8-Lead SOIC_IC	RI-8-1
ADuM4122BRIZ-RL	1	2	7.5	−40°C to +125°C	8-Lead SOIC_IC, 13″ Tape and Reel	RI-8-1
ADuM4122CRIZ	1	2	11.6	−40°C to +125°C	8-Lead SOIC_IC	RI-8-1
ADuM4122CRIZ-RL	1	2	11.6	−40°C to +125°C	8-Lead SOIC_IC, 13″ Tape and Reel	RI-8-1
EVAL-ADuM4122EBZ					Evaluation Board	

[1] Z = RoHS Compliant Part.

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